Crystalfontz America, Inc.
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Specification

For

LCD Module

CFAF320240F-T-TS

PRELIMINARY

MODULE: **CFAF320240F-T-TS**

CUSTOMER:

REV	DESCRIPTION	DATE
1	FIRST ISSUE	2008/11/17

TZD	INITIAL	DATE
APREPARED BY		2008/11/17
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

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PRELIMINARY

Revision History

Rev.	Comment	Date
1	Original Version	2008-11-17

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1 General Specifications

Item	☑Standard Value	Unit
Display Pattern	☑Graphic ☐Character ☐Segment ☐_____ ☐with ICON	
Color	☐ Mono. ☐Grayscale ☑ 16.7M	
Module Dimension (W x H x T)	77.6(W)X 64.4(H)X3.1(T)	mm
Viewing Area (W x H)	70.08(W)X52.56(H)	mm
Active Area (W x H)	70.08(W)X52.56(H)	mm
Character Size (W x H)	/	mm
Character Pitch (W x H)	/	mm
DOT Size (W x H)	0.063(W)×0.209(H)	mm
DOT Pitch (W x H)	0.219(W)×0.219(H)	mm
LCD Type	☐TN, Positive ☐TN, Negative ☐HTN, Positive ☐HTN, Negative	
	☐STN, Yellow-Green ☐STN, Gray ☐STN, BluE ☐FSTN, Positive ☐FSTN, Negative	
	☐_____ ☐FM LCD ☑TFT	
Polarizer Type	☐Transflective ☑Transmissive ☐Reflective ☐Anti-Glare	
View Direction	6H ☑12H ☐____	
LCD Controller & Driver	SSD2119	
LCD Driving Method	1/240duty, 1/15bias	
Interface Type	Serial ☐I²C ☐4-line SPI ☐3-line SPI ☐____	
	Parallel ☐6800 ☑8080 ☐4-bit ☐_____	
Backlight Type	☑ LED ☐Bottom ☑Single Side ☐Dual Side	
	☐_____ ☐EL ☐CCFL	
Backlight Color	☐Yellow-Green ☑White ☐Amber ☐Blue ☐Red ☐_____	
EL/CCFL Driver type	☐Build-in ☐External	
DC-DC Converter	☑Build-in ☐External	
Operation Temperature	T_{OPL} = -20 T_{OPH} =+70	°C
Storage Temperature	T_{STL} = -30 T_{STH} = +80	°C

Note:

T_{OPL}: Lowest Operation Temperature.

T_{OPH}: Highest Operation Temperature.

T_{STL}: Lowest Storage Temperature.

T_{STH}: Highest Storage Temperature.

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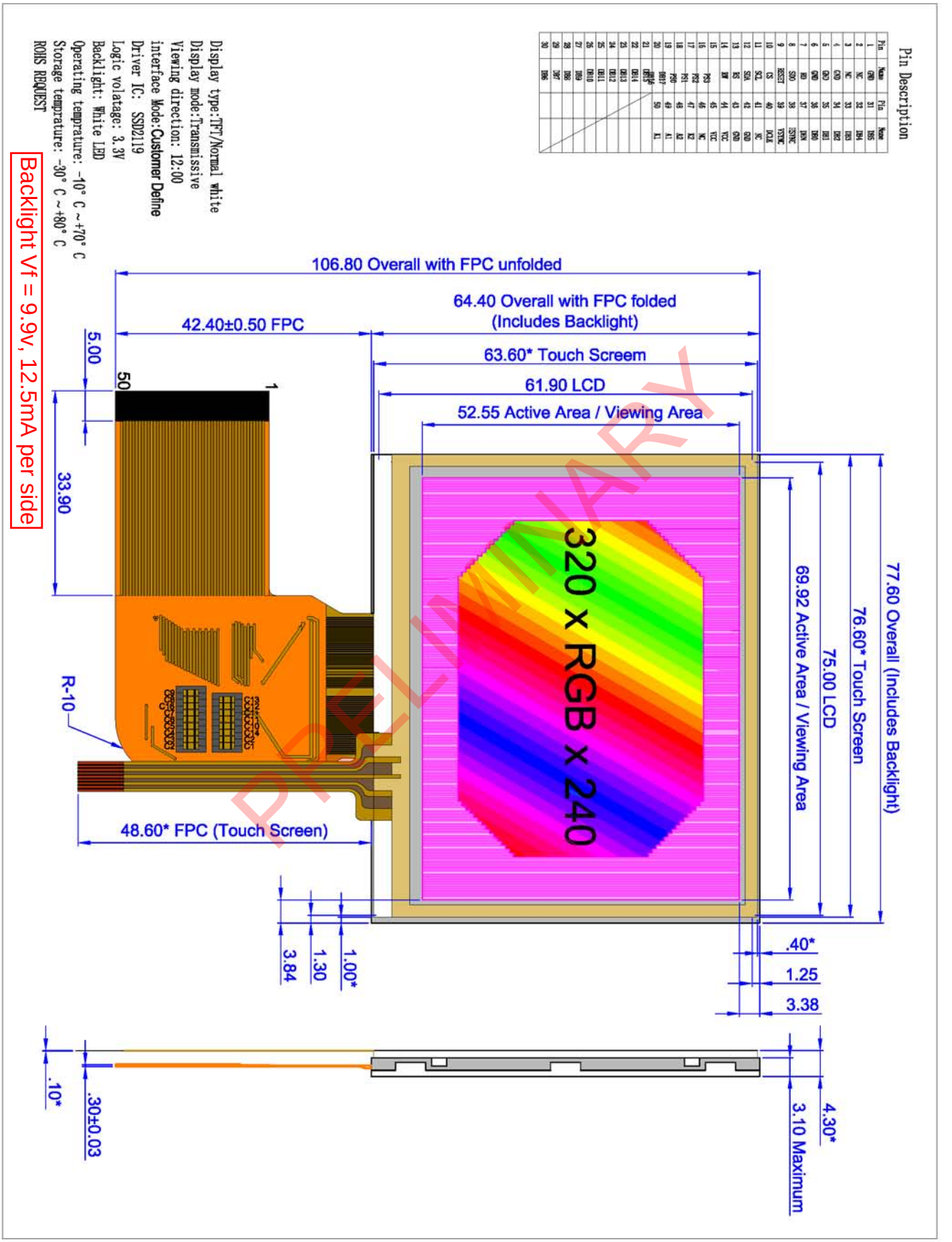
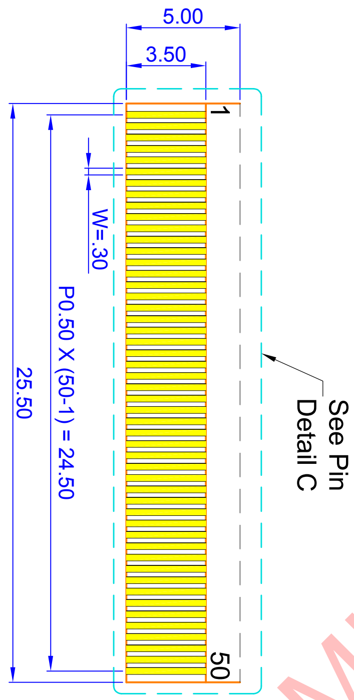
2 Mechanical Diagram



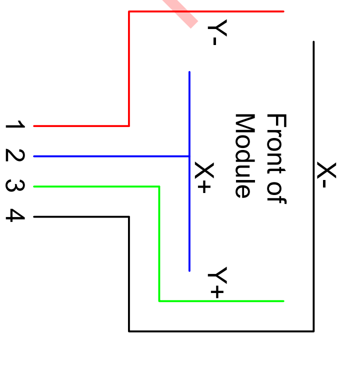
Note: 1. Tolerance is ±0.2 mm unless specified.
2. FPC = Flexible Printed Circuit.
3. Diagonal = 3.44"



Pin Detail

Pin Detail C

1	GND
2	NC
3	NC
4	GND
5	GND
6	GND
7	$\overline{RD}_{8080}$
8	SD0
9	$\overline{RST}$
10	$\overline{CS}$
11	SCL
12	SI
13	$D/\overline{C}$
14	$\overline{WR}_{8080}$
15	PS3
16	PS2
17	PS1
18	PS0
19	DB17
20	DB16
21	DB15
22	DB14
23	DB13
24	DB12
25	DB11
26	DB10
27	DB09
28	DB08
29	DB07
30	DB06
31	DB05
32	DB04
33	DB03
34	DB02
35	DB01
36	DB0
37	DEN
38	HSYNC
39	VSYNC
40	DCLK
41	NC
42	GND
43	GND
44	V_{LOGIC}
45	V_{LOGIC}
46	NC
47	K2
48	A2
49	A1
50	K1



Touch Screen Pin Detail

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3 I/O Terminal

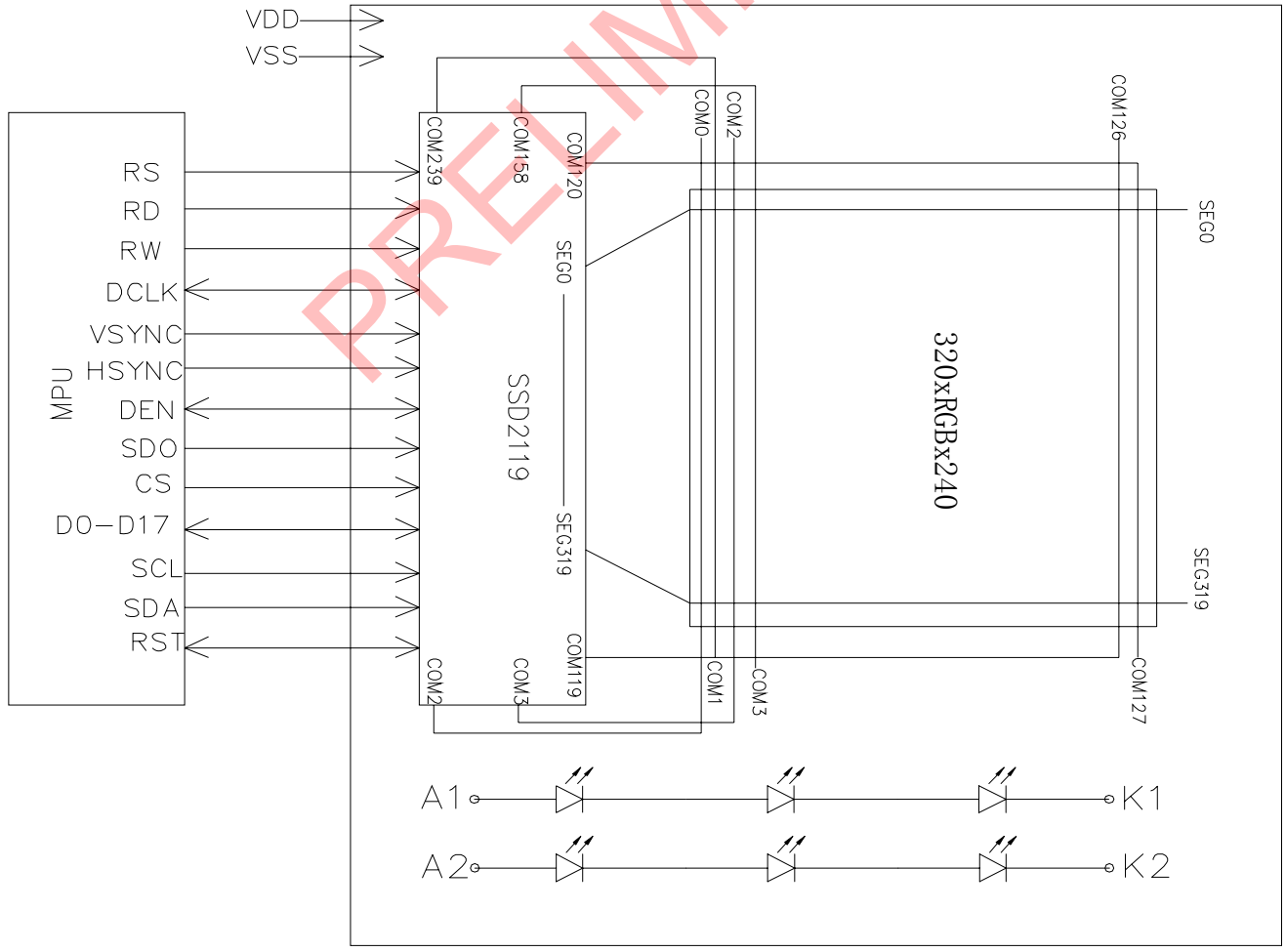
<table>
<tr><th>Pin NO.</th><th>Symbol</th><th>Level</th><th>Function</th></tr>
<tr><td>1</td><td>GND</td><td>L</td><td>Ground</td></tr>
<tr><td>2-3</td><td>NC</td><td>--</td><td>--</td></tr>
<tr><td>4-6</td><td>GND</td><td>L</td><td>Ground</td></tr>
<tr><td>7</td><td>RD</td><td>H/L</td><td>6800-system : E (enable signal)
8080-system : RD (read strobe signal)
Serial mode : Not used and should be connected to V_{DDIO} or V_{ss}</td></tr>
<tr><td>8</td><td>SDO</td><td>H/L</td><td>Data output pin in serial interface</td></tr>
<tr><td>9</td><td>RESET</td><td>H/L</td><td>System reset pin.
- An active low pulse at this pin will reset the IC, Connect to V_{DDIO} in normal operation</td></tr>
<tr><td>10</td><td>CS</td><td>H/L</td><td>CS : Chip select pin for 6800/8080 Parallel Interface
SCS : Chip Select pin for Serial Mode Interface</td></tr>
<tr><td>11</td><td>SCL</td><td>H/L</td><td>Serial clock input</td></tr>
<tr><td>12</td><td>SDA</td><td>H/L</td><td>Data input pin in serial interface</td></tr>
<tr><td>13</td><td>RS</td><td>H/L</td><td>Data or command
DC : Parallel Interface
SDC : Serial Interface</td></tr>
<tr><td>14</td><td>RW</td><td>H/L</td><td>6800-system : RW (indicates read cycle when High, write cycle when Low)
8080-system : WR (write strobe signal)</td></tr>
<tr><td>15-18</td><td>PS3-PS0</td><td>H/L</td><td>
<table>
<tr><th>PS3</th><th>PS2</th><th>PS1</th><th>PS0</th><th>Interface Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-bit 6800 parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>16-bit 8080 parallel interface</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>9-bit generic D[9:16] (262k colour) + 3-wire SPI If 65K color, D12 shorts to D17 internally</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit generic (262k colour) + 3-wire SPI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit generic (262k colour) + 3-wire SPI</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>6-bit generic D[8:3] (262k colour) + 3-wire SPI</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>18-bits 6800 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9-bits 6800 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-bit 8080 parallel interface</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>9-bit 8080 parallel interface</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>3-wire SPI</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire SPI</td></tr>
</table>
</td></tr>
<tr><td>19-36</td><td>DB17-DB0</td><td>H/L</td><td>Data bus</td></tr>
<tr><td>37</td><td>DEN</td><td>H/L</td><td>Display enable pin from controller.</td></tr>
<tr><td>38</td><td>HSYNC</td><td>H/L</td><td>Line Synchronization input</td></tr>
</table>

PRELIMINARY

39	VSYNC	H/L	Frame/Ram Write Synchronization input
40	DCLK	H/L	Dot-clock signal and oscillator source. A non-stop external clock must be provided to that pin even at front or black porch non-display period.
41	NC	--	
42-43	GND	L	Ground
44-45	VCC	H	Power supply
46	NC	--	
47	K2	L	Backlight-
48	A2	H	Backlight+
49	A1	H	Backlight+
50	K1	L	Backlight-

PRELIMINARY

3.2 Block Diagram



4. Electro-optical Specifications

4.1 Absolute Maximum Ratings

Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
VDDIO	Supply Voltage	-0.3 to +4.0	V
VCI	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{DDIO} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, strong electric fields, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occured. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices. It is advised that proper precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range VSS ≤ VDDIO ≤ VCI ≤ V_{OUT}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

4.2 Optical Characteristics

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 1.4 to 3.6V, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.4	-	3.6	V
VCI	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO whichever is higher	-	3.6	V
VGH	Gate driver High Output Voltage Booster efficiency	No panel loading; 4x or 5x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	88	90	-	%
		No panel loading; 6x booster; ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	82	84	-	%
VCIX2	VCIX2 primary booster efficiency	No panel loading, ITO for CYP, CYN, VCIX2, VCI and VCHS = 10 Ohm	83	85	-	%
VGH	Gate driver High Output Voltage		9	-	18	V
VGL	Gate driver Low Output Voltage		-15	-	-6	V
VcomH	Vcom High Output Voltage		V_{CI} + 0.5	-	5	V
VcomL	Vcom Low Output Voltage		$-V_{CIM}$+0.5	-	-1	V
VLCD63	Max. Source Voltage		-	-	6	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DDIO}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA

PRELIMINARY

C_{IN}	Logic Pins Input Capacitance			-	5	7.5	pF
R_{SON}	Source drivers output resistance			-	1	-	kΩ
R_{GON}	Gate drivers output resistance			-	500	-	Ω
R_{CON}	Vcom output resistance			-	200	-	Ω
I_{dp}(262k)	Display current for 262k	Vddio= 1.8V, Vci = 2.8V, 5x/-5x(VGH/VGL) booster ratio. Full color current consumption, without panel loading	Ivdd	-	150	300	uA
			Ivci	-	2.5	8	mA
I_{dp}(8 color)	Display current for 8 color mode	Vddio= 1.8V, Vci = 2.8V, +5/-3(VGH/VGL) booster ratio Current consumption for 8 color partial display, without panel loading	Ivdd	-	120	300	µA
			Ivci	-	1	5	mA
I_{slp}	Sleep mode current	Oscillator off, no source/gate output, Ram read write halt. Send command R10-0001 (sleep mode), R00-0000 (stop osc)	Ivdd	-	30	100	µA
			Ivci	-	40	200	µA

Remark: Ivdd = Ivddio

PRELIMINARY

4.3 Timing Characteristics

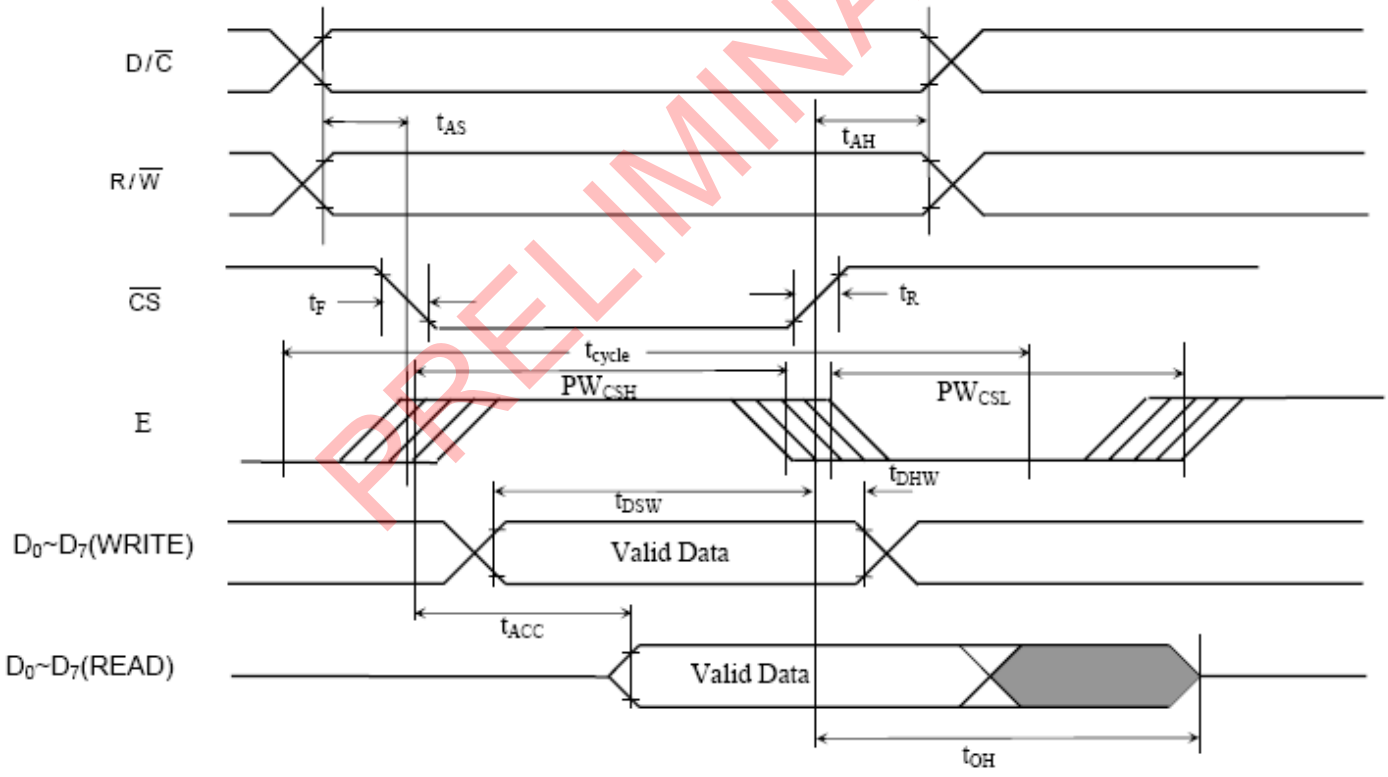
Table 13-1: Parallel 6800 Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS}	Address Setup Time (R/$\overline{W}$)	0	-	-	ns
t_{AH}	Address Hold Time (R/$\overline{W}$)	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time (/CS)	-	-	4	ns
t_F	Fall time (/CS)	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

Figure 13-1: Parallel 6800-series Interface Timing Characteristics



PRELIMINARY

Table 13-2: Parallel 8080 Timing Characteristics

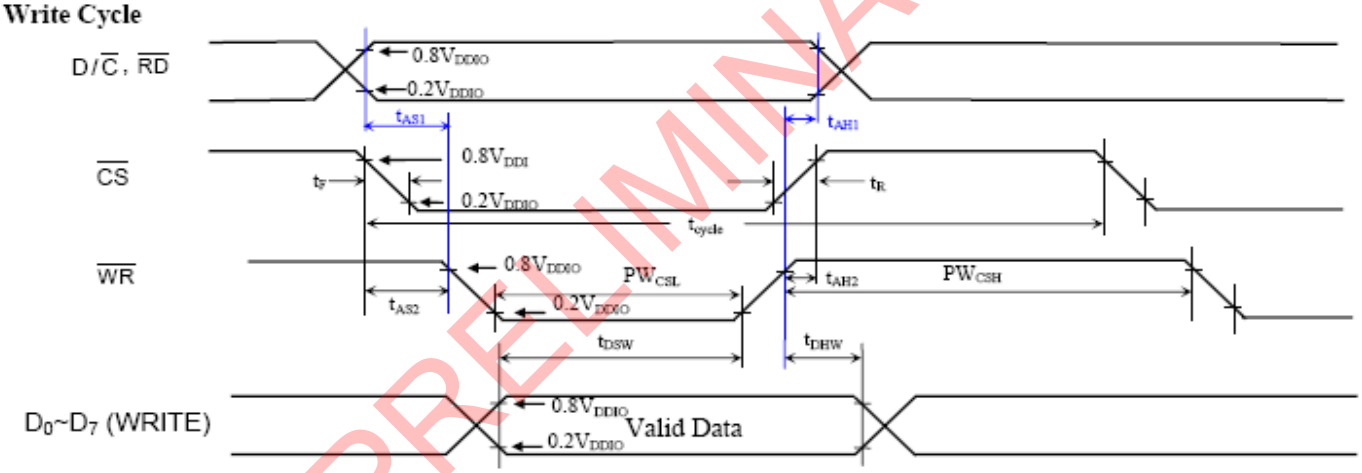
(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	75	-	-	ns
t_{cycle}	Clock Cycle Time (read cycle)	1000	-	-	ns
t_{AS1}	Address Setup Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AH1}	Address Hold Time between (R/$\overline{W}$) and D/$\overline{C}$	0	-	-	ns
t_{AS2}	Address Setup Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{AH2}	Address Hold Time between (R/$\overline{W}$) and $\overline{CS}$	0	-	-	ns
t_{DSW}	Data Setup Time (D0~D7, WRITE)	5	-	-	ns
t_{DHW}	Data Hold Time (D0~D7, WRITE))	5	-	-	ns
t_{ACC}	Data Access Time (D0~D7, READ)	250	-	-	ns
t_{OH}	Output Hold time (D0~D7, READ)	100	-	-	ns
PW_{CSL}	Pulse width /CS low (write cycle)	40	-	-	ns
PW_{CSH}	Pulse width /CS high (write cycle)	25	-	-	ns
PW_{CSL}	Pulse width /CS low (read cycle)	500	-	-	ns
PW_{CSH}	Pulse width /CS high (read cycle)	500	-	-	ns
t_R	Rise time (/CS)	-	-	4	ns
t_F	Fall time (/CS)	-	-	4	ns

Note: CS can be pulled low during the write cycle, only /RW is needed to be toggled

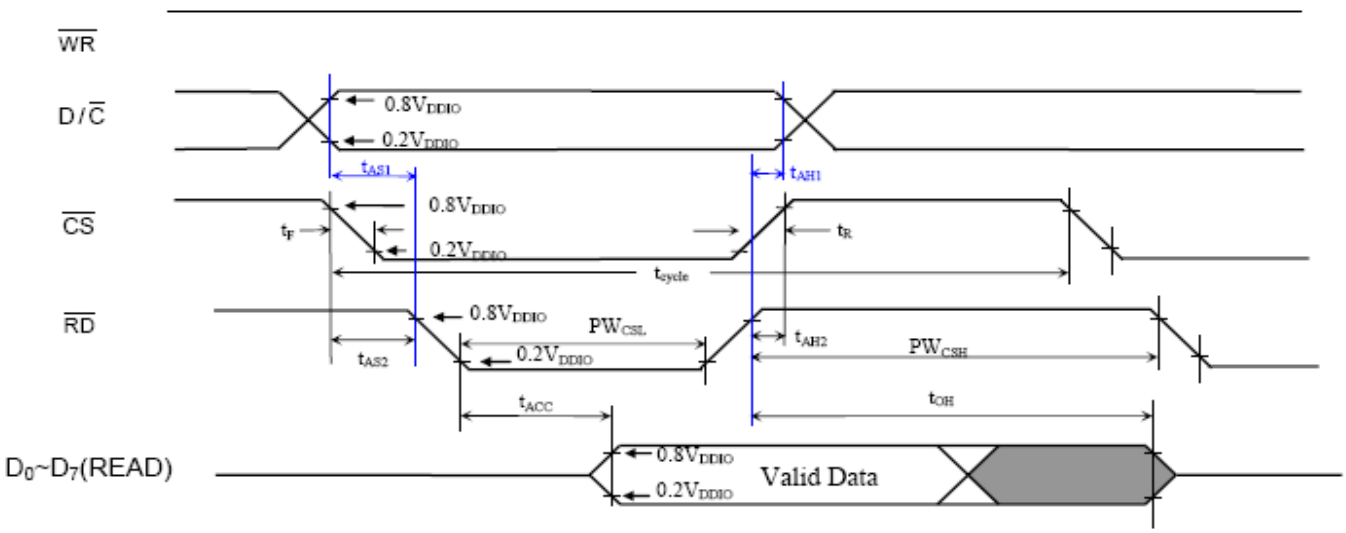
Figure 13-2: Parallel 8080-series Interface Timing Characteristics

Write Cycle



Remark: It's highly recommended that $\overline{RD}$ remains high for the whole write cycle

Read Cycle



PRELIMINARY

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Table 13-3: Serial Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	77	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	4	-	-	ns
t_{AH}	Register select Hold Time	5	-	-	ns
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	5	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	38	-	-	ns
t_{CLKH}	Clock High Time	38	-	-	ns
t_R	Rise time	-	-	4	ns
t_F	Fall time	-	-	4	ns

PRELIMINARY

Figure 13-3: 4 wire Serial Timing Characteristics

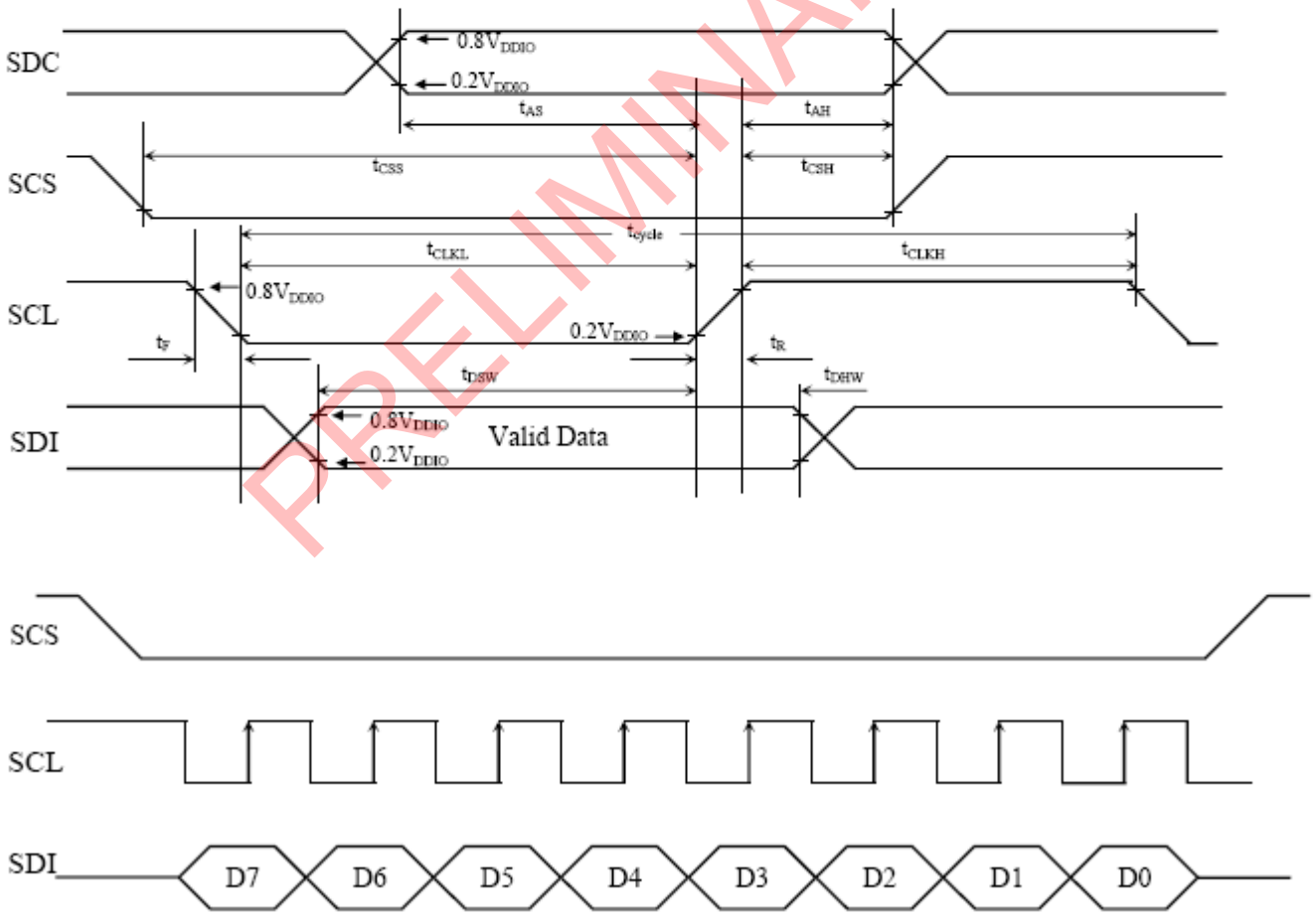


Table 13-4: RGB Timing Characteristics

(T_A = -40 to 85°C, V_{DDIO} = 1.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
f_{DOTCLK}	DOTCLK Frequency (70Hz frame rate)	1	5.5	8.2	MHz
t_{DOTCLK}	DOTCLK Period	122	182	1000	us
t_{VSYS}	Vertical Sync Setup Time	20	-	-	ns
t_{VSYH}	Vertical Sync Hold Time	20	-	-	ns
t_{HSYS}	Horizontal Sync Setup Time	20	-	-	ns
t_{HSYH}	Horizontal Sync Hold Time	20	-	-	ns
t_{HV}	Phase difference of Sync Signal Falling Edge	0	-	320	t_{DOTCLK}
t_{CLK}	DOTCLK Low Period	61	-	-	ns
t_{CKH}	DOTCLK High Period	61	-	-	ns
t_{DS}	Data Setup Time	25	-	-	ns
t_{DH}	Data hold Time	25	-	-	ns
t_{RES}	Reset pulse width	8			ns

Note: External clock source must be provided to DOTCLK pin of SSD2119. The driver will not operate in absence of the clocking signal.

PRELIMINARY

Figure 13-4: RGB Timing Characteristics

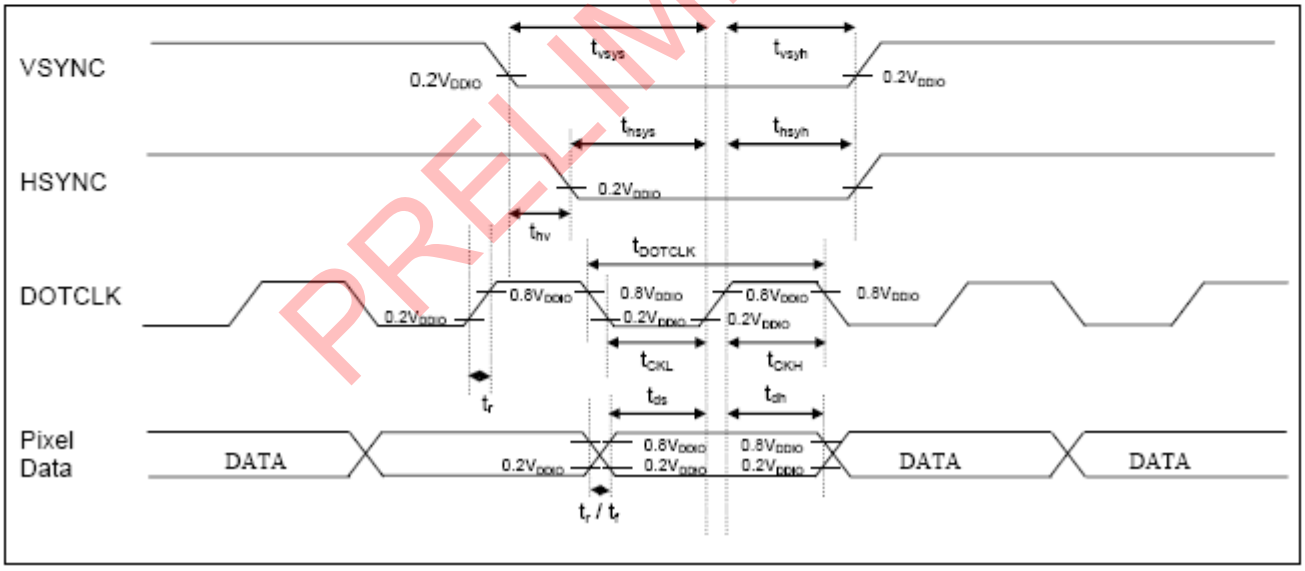
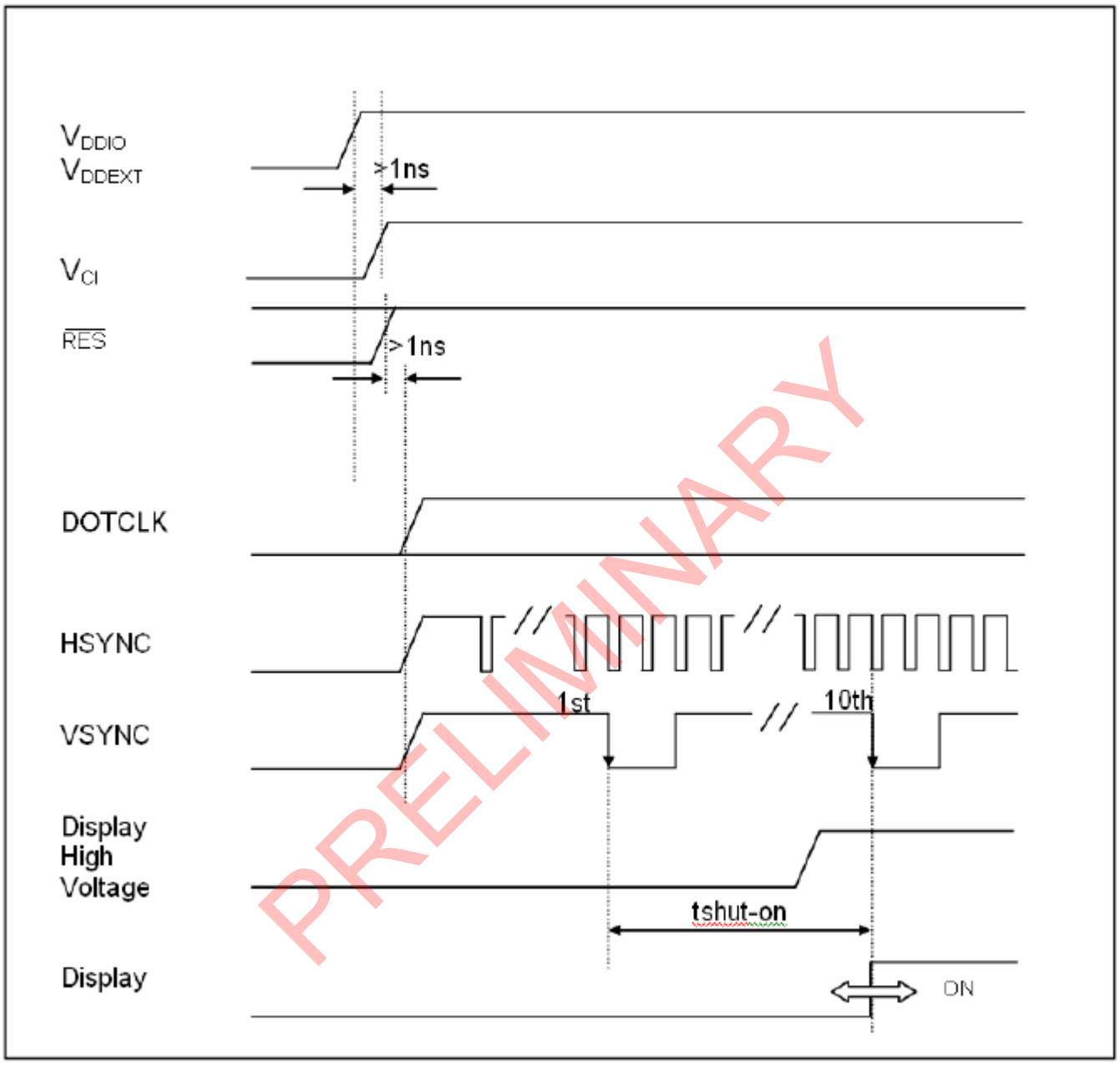


Figure 13-5: Power Up Sequence



PRELIMINARY

5 Programming

5.1 Instruction Table

Table 8-1: Command Table

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R00h	Oscillation Start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	GD	BGR	SM	TB	0	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
	(3AEFh)			0	0	1	1	1	0	1	0	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW7	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	All GAMAS[2:0] setting 8 color (6AE4h)			0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	DIV1	DIV0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
	(5308h)			0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0004h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R0Fh	Gate scan start position	0	1	0	0	0	0	0	0	0	SCN8	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R10h	Sleep mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R11h	Entry mode	0	1	VS mode	DFM1	DFM0	0	Demode	WMode	Nosync	DMode	TY1	TY0	ID1	ID0	AM	0	0	0
	(6230h)			0	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0
R15h	Entry mode	0	1	0	0	0	0	0	0	0	0	0	0	0	0	INVDOT	INVDEN	INVHS	INVVS
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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(continued)

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R25h	Frame Frequency	0	1	OSC3	OSC2	OSC1	OSC0	0	0	0	0	0	0	0	0	0	0	0	0
	(8000h)			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R28h	VCOM OTP (000Ah)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (80C0h)	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R41h	Vertical scroll control (1)	0	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R42h	Vertical scroll control (2)	0	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R44h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
	(EF00h)			1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
R45h	Horizontal RAM address start position	0	1	0	0	0	0	0	0	0	HSA8	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R46h	Horizontal RAM address end position	0	1	0	0	0	0	0	0	0	HEA8	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
	(013Fh)			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
R48h	First window start	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R49h	First window end	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Ah	Second window start	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Bh	Second window end	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
	(00EFh)			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R4Eh	Set GDDRAM X address counter	0	1	0	0	0	0	0	0	0	0	XAD7	XAD6	XAD5	XAD4	XAD3	XAD2	XAD1	XAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R4Fh	Set GDDRAM Y address counter	0	1	0	0	0	0	0	0	0	YAD8	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Note: In R01h, bits REV, BGR, RL, CM will override the corresponding hardware pins settings.
Setting R28h as 0x0006 is required before setting R25h and R29h registers.

Appendix

1Definitions of Optical Characteristic

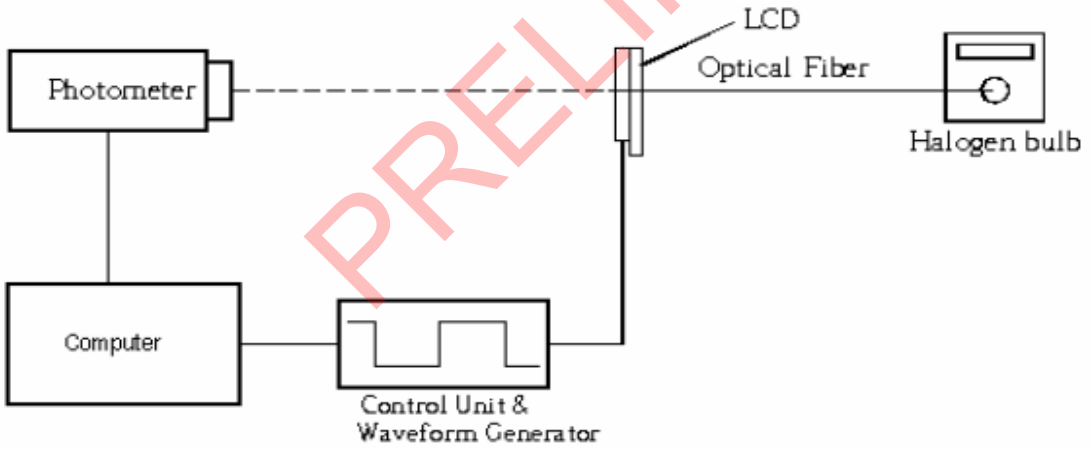
1.1 Contrast Ratio Test

A) Contrast ratio is calculated by the following formula when the output voltage is obtained fi
electro-optical test system.
B) Test Condition: Accord to the LCD's driving method and operating voltage (V_{LCD}).
C) Formula:

$$Contrast\ Ratio\ (Positive\ type) = \frac{Photometer\ output\ voltage\ when\ non-select\ waveform\ is\ a}{Photometer\ output\ voltage\ when\ select\ waveform\ is\ app}$$

$$Contrast\ Ratio\ (Negative\ type) = \frac{Photometer\ output\ voltage\ when\ select\ waveform\ is\ app}{Photometer\ output\ voltage\ when\ non-select\ waveform\ is\ a}$$

D) Test system:



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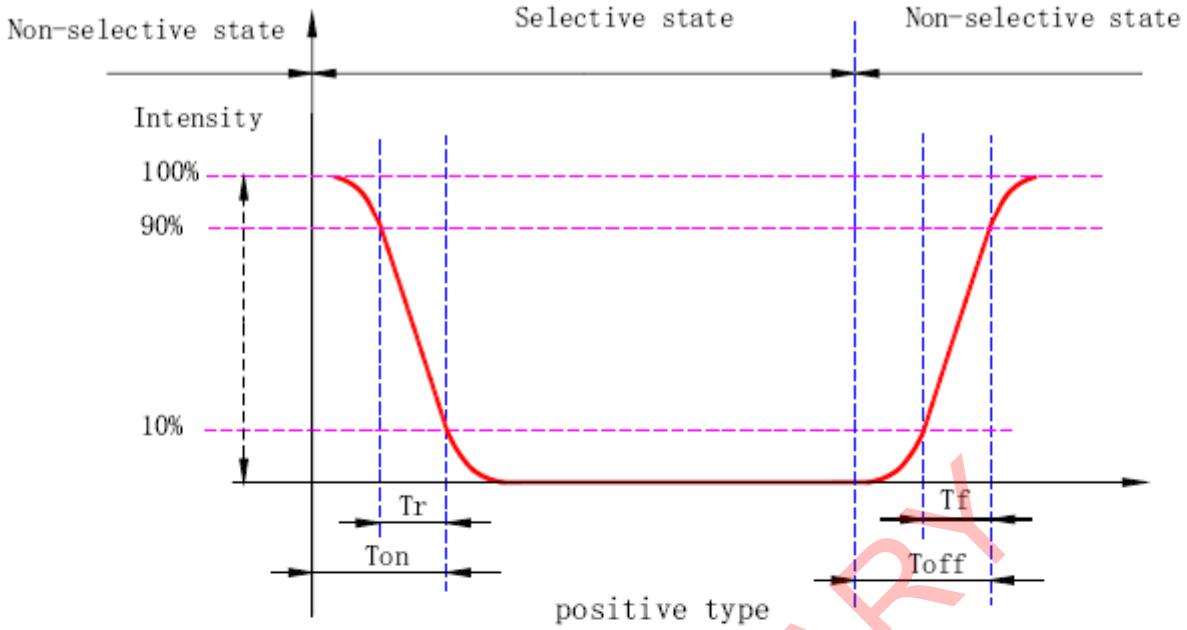
1.2 Response time

1.2.1 Positive type

A) Rise time is defined as the time required for the transmission to change from 90% to 10%.
B) Fall time is defined as the time required for the transmission to change from 10% to 90%.
C) On time is defined as the time required for the transmission to change from 100% to 10%.

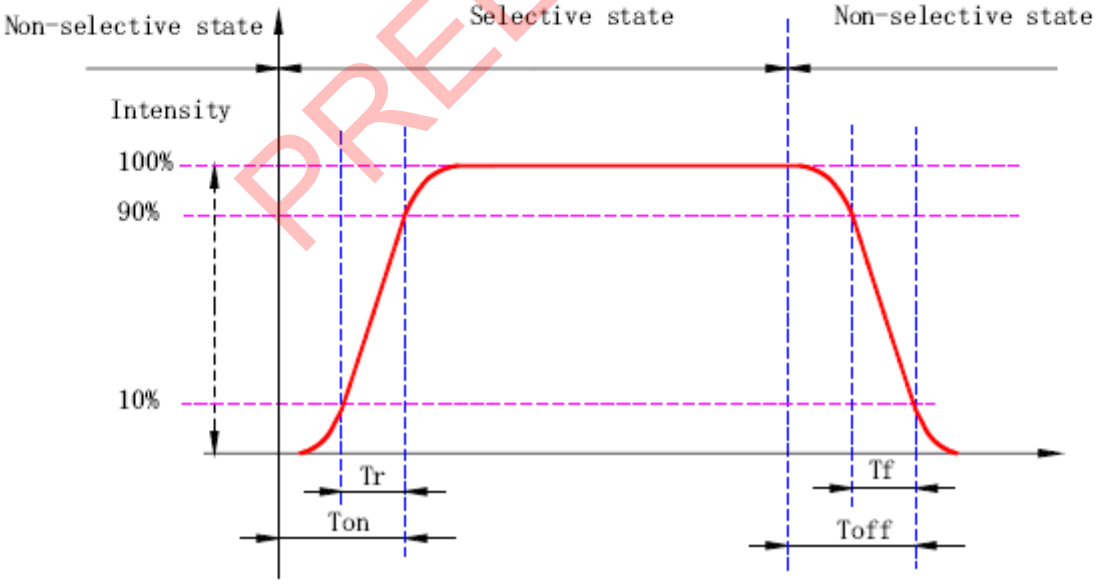
D) Off time is defined as the time required for the transmission to change from 0% to 90%.



positive type

1.2.1 Negative type

A) Rise time is defined as the time required for the transmission to change from 10% to 90%.
B) Fall time is defined as the time required for the transmission to change from 90% to 10%.
C) On time is defined as the time required for the transmission to change from 0% to 90%.
D) Off time is defined as the time required for the transmission to change from 100% to 10%.



negative type

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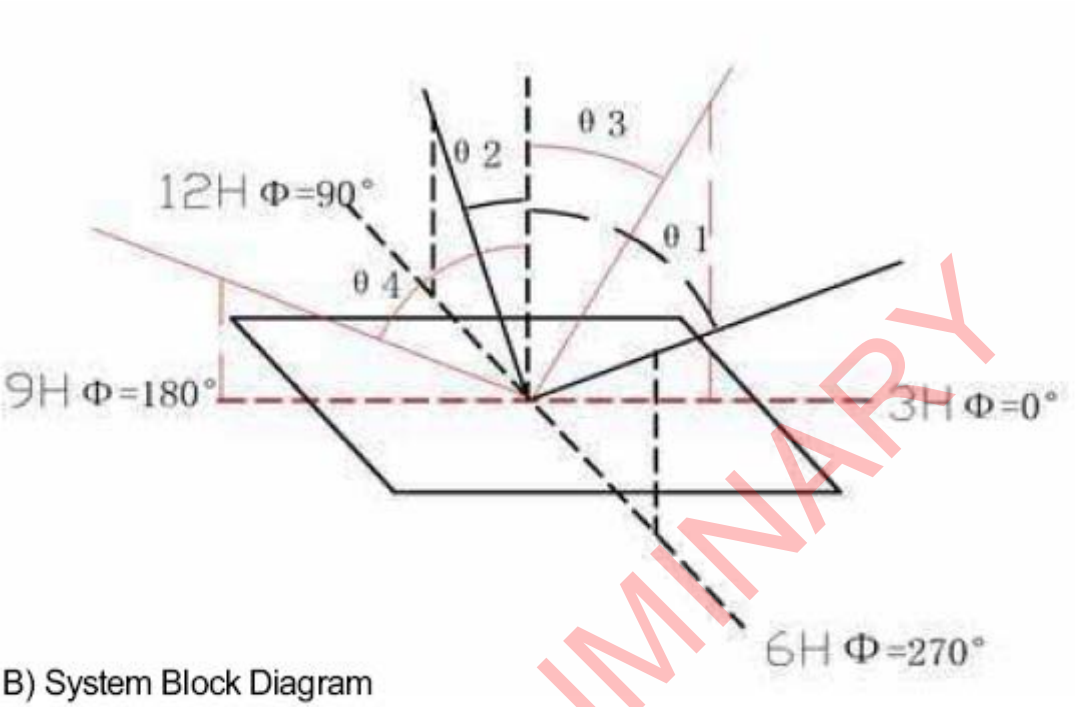
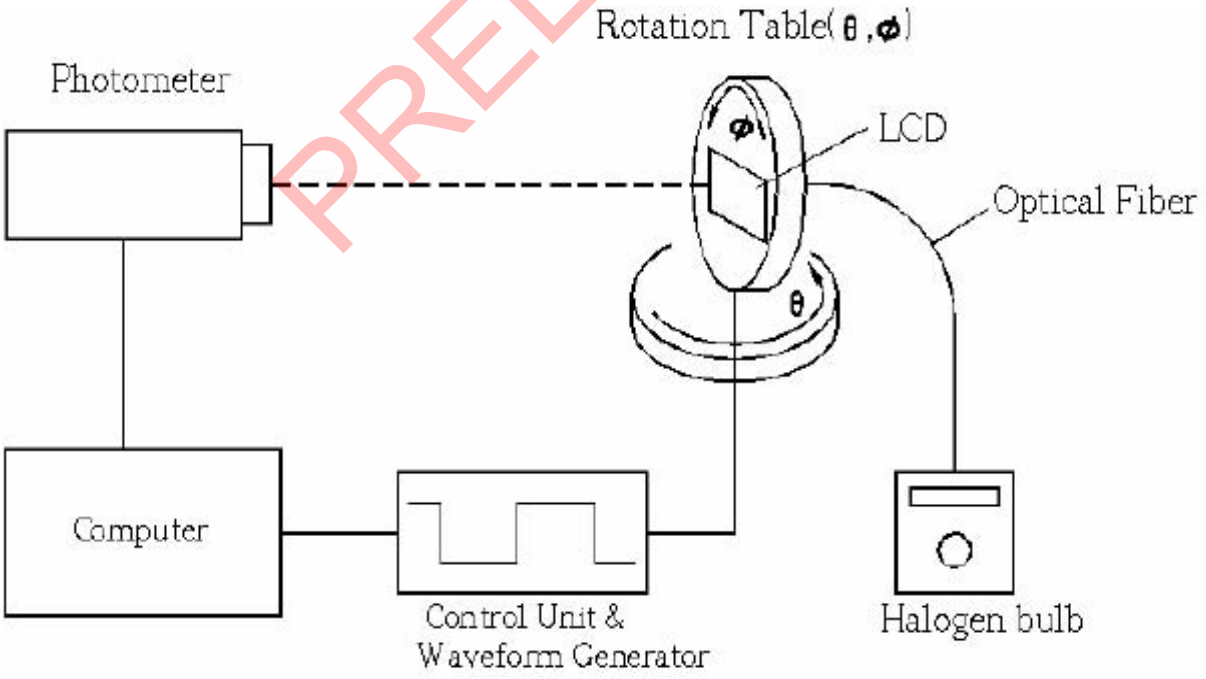
2 Viewing Angle

A) Viewing angle is definition



B) System Block Diagram



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