ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2018-04-25
for
CFAP200200A1-0154

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CONTENTS

1. General Information

Datasheet Revision History
Datasheet Release Date: **2018-04-25** Datasheet for the CFAP200200A1-0154 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

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2. Description Overview

This ePaper display is a TFT active matrix electrophoretic display with interface and a reference system design. The 1.54" active area contains 200x200 pixels and has 1-bit white/black full display capabilities. An integrated circuit contains a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

3. Features

- 200x200 Pixels
- High Contrast
- High Reflectance
- Ultra-Wide Viewing Angle
- Ultra-Low Power Consumption
- Pure Reflective Mode
- Bi-Stable Display
- Commercial Temperature Range
- Landscape or Portrait Mode
- Antiglare Hard-Coated Front-Surface
- Low Current Deep Sleep Mode
- On-Chip Display RAM
- Low Voltage Detect for Supply Voltage
- Internal Temperature Sensor
- 10-byte OTP Space for Module Identification
- Waveform Stored in On-Chip OTP
- Serial Peripheral Interface Available
- On-Chip Oscillator
- On-Chip Booster and Regulator Control for Generating VCOM, Gate and Source Driving Voltage
- I^2C Signal Master Interface to Read External Temperature Sensor

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.54	inch	-
Display Resolution	200 (H) × 200 (W)	pixel	dpi: 183
Active Area	27.6 (H) × 27.6 (W)	mm	-
Pixel Pitch	0.138 × 0.138	mm	-
Pixel Configuration	Square	-	-
Outline Dimension	31.80 (H) × 36.32 (W) × 1.05 (D)	mm	-
Weight (typical)	2.2	g	-

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Single	Description	Remark
1	NC	No Connection and Do Not Connect with Other NC Pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	VGL	Negative Gate Driving Voltage	
5	VGH	Positive Gate Driving Voltage	
6	TSCL	I^2C Interface to Digital Temperature Sensor Clock Pin	
7	TSDA	I^2C Interface to Digital Temperature Sensor Data Pin	
8	BS1	Bus Selection Pin	Note 5-5
9	BUSY	Busy State Output Pin	Note 5-4
10	RES#	Reset	Note 5-3
11	D/C#	Command / Data Control Pin	Note 5-2
12	CS#	Chip Select Input Pin	Note 5-1
13	D0	Serial Clock Pin (SPI)	
14	D1	Serial Data Pin (SPI)	
15	VDDIO	Power for Interface Logic Pins	
16	VCI	Power Supply Pin for Chip	
17	VSS	Ground	
18	VDD	Core Logic Power Pin	
19	VPP	Power Supply for OTP Programming	
20	VSH	Positive Source Driving Voltage	
21	PREVGH	Positive Supply Pin for VGH and VSH	
22	VSL	Negative Source Driving Voltage	
23	PREVGL	Power Supply Pin for VCOM, VGL, and VSL	
24	VCOM	VCOM Driving Voltage	

Note (5-1): This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note (5-2): This pin (D/C#) is the Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note (5-3): This pin (RES#) is the reset signal input. The reset is active LOW.

Note (5-4): This pin (BUSY) is the Busy state output pin. When busy is LOW, the operation of chip should not be interrupted and no commands should be issued to the module. The driver IC will put Busy pin LOW when the driver IC is working such as

- Outputting Display Waveform; or
- Communicating with Digital Temperature Sensor

Note (5-5): This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “LOW”, 4-line SPI is selected. When it is “HIGH”, 3-line SPI (9 bits SPI) is selected. Please refer to the table below.

Table: Bus Interface Selection

BS1	MPU Interface
L	4-Lines Serial Peripheral Interface (SPI)
H	3-Lines Serial Peripheral Interface (SPI) – 9 bits SPI

6. MCU Interface

6.1. MCU Serial Peripheral Interface (4-Wire SPI)

The 4-wire SPI consists of SCLK (serial clock), SDIN (serial data), D/C# and CS#. D0 acts as SCLK and D1 acts as SDIN.

Function	CS# Pin	D/C# Pin	SCLK Pin
Write Command	L	L	↑
Write Data	L	H	↑

Note: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, … D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

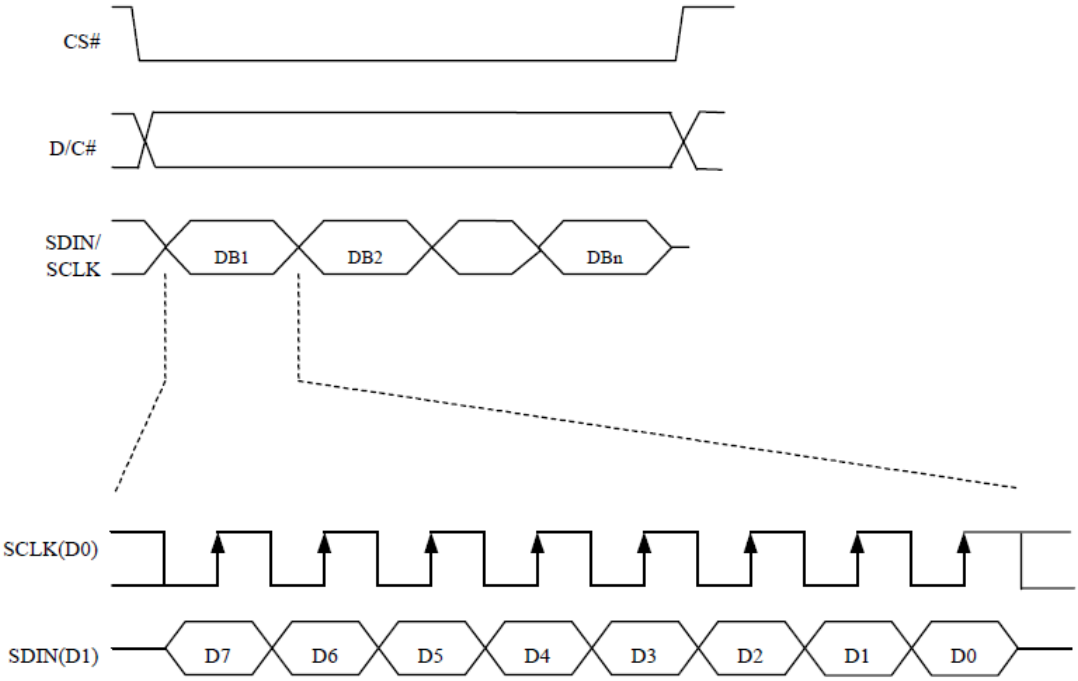


Figure 6-1: Write Procedure in 4-Wire Serial Peripheral Interface Mode

6.2. MCU Serial Peripheral Interface (3-Wire SPI)

The 3-wire serial interface consists of SCLK (serial clock), SDIN (serial data) and CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits that will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Function	CS# Pin	D/C# Pin	SCLK Pin
Write Command	L	Tie LOW	↑
Write Data	L	Tie LOW	↑

Note: ↑stands for rising edge of signal

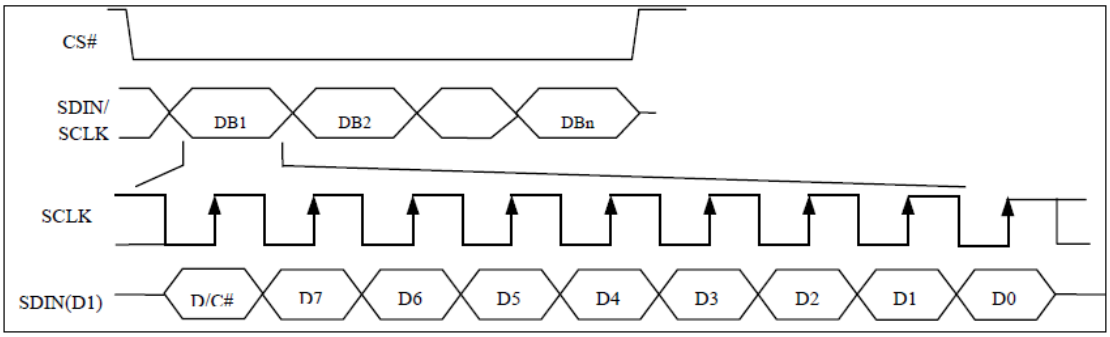


Figure 6-2: Write Procedure in 3-Wire Serial Peripheral Interface Mode

6.3. External Temperature Sensor Operation

There are two ways to let the module get to the ambient temperature:

1. Use the external temperature sensor interface. The module provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing. TSDA will be treated as SDA line and TSCL will be treated as SCL line. They are required connecting with the external pull-up resistors when they are used to connect to the temperature sensor, then the module will check the temperature automatically.
2. Use any kinds of external temperature sensor to get the temperature value then converted to hex format, then use the SPI interface send command 0x1A and the temperature value into the module. To convert the temperature value to hex:
   - When the Temperature value MSByte bit D11 = 0, the temperature is positive and value (DegC) = + (Temperature value)/16
   - When the Temperature value MSByte bit D11 = 1, the temperature is negative and value (DegC) = ~ (2's complement of Temperature value)/16

12-bit Binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

7. Command Table

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output Control</td><td rowspan="4">Set the number of gate. Setting for 152 gates is:
Set A[8:0] = 0C7h
Set B[2:0] = 00h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>0</td><td>0C</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Booster Soft Start Control</td><td rowspan="4">Set A[7:0] = CFh[POR]
Set B[7:0] = CEh[POR]
Set C[7:0] = 8Dh[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>B_6</td><td>B_5</td><td>B_4</td><td>B_3</td><td>B_2</td><td>B_1</td><td>B_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>1</td><td>C_6</td><td>C_5</td><td>C_4</td><td>C_3</td><td>C_2</td><td>C_1</td><td>C_0</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep Mode</td><td rowspan="2">Deep Sleep Mode Control
<table><tr><th>A[0]:</th><th>Description</th></tr><tr><td>0</td><td>Normal Mode [POR]</td></tr><tr><td>1</td><td>Enter Deep Sleep Mode</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_0</td></tr>
</table>

0	0	11	0	0	0	1	0	0	0	1	Data Entry Mode Setting	Define data entry sequence A[1:0] = ID[1:0] Address automatic increment / decrement setting. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register).	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display	Option for Display Update

<table>
<tr>
<td>0</td><td>1</td><td></td><td>A_7</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td>Update Control 1</td>
<td>Bypass Option used for Pattern Display, which is used for display the RAM content into the Display

OLD RAM Bypass option
A[7]
A[7] = 1: Enable bypass
A[7] = 0: Disable bypass [POR]
A[4] value will be used as for bypass.
A[4] = 0 [POR]
A[1:0] Initial Update Option – Source Control

<table>
<tr><th>A[1:0]</th><th>GSC</th><th>GSD</th></tr>
<tr><td>01 [POR]</td><td>GS0</td><td>GS1</td></tr>
</table>
</td>
</tr>
</table>

0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

	Parameter (in Hex)
Enable Clock Signal, Then Enable CP Then Load Temperature value Then Load LUT Then INIITIAL DISPLAY Then PATTERN DISPLAY Then Disable CP Then Disable OSC	FF[POR]
To Enable Clock Signal (CLKEN=1)	80
To Enable Clock Signal, then Enable CP (CLKEN=1, CPEN=1)	C0
To INITIAL DISPLAY + PATTEN DISPLAY	0C
To INITIAL DISPLAY	08
To DISPLAY PATTEN	04
To Disable CP, then Disable Clock Signal (CLKEN=1, CPEN=1)	03
To Disable Clock Signal (CLKEN=1)	01

Remarks:
CLKEN=1
If CLS=VDDIO then Enable OSC.
If CLS=VSS then Enable External Clock.

CLKEN=0:
If CLS=VDDIO then Disable OSC and INTERNAL CLOCK Signal = VSS.

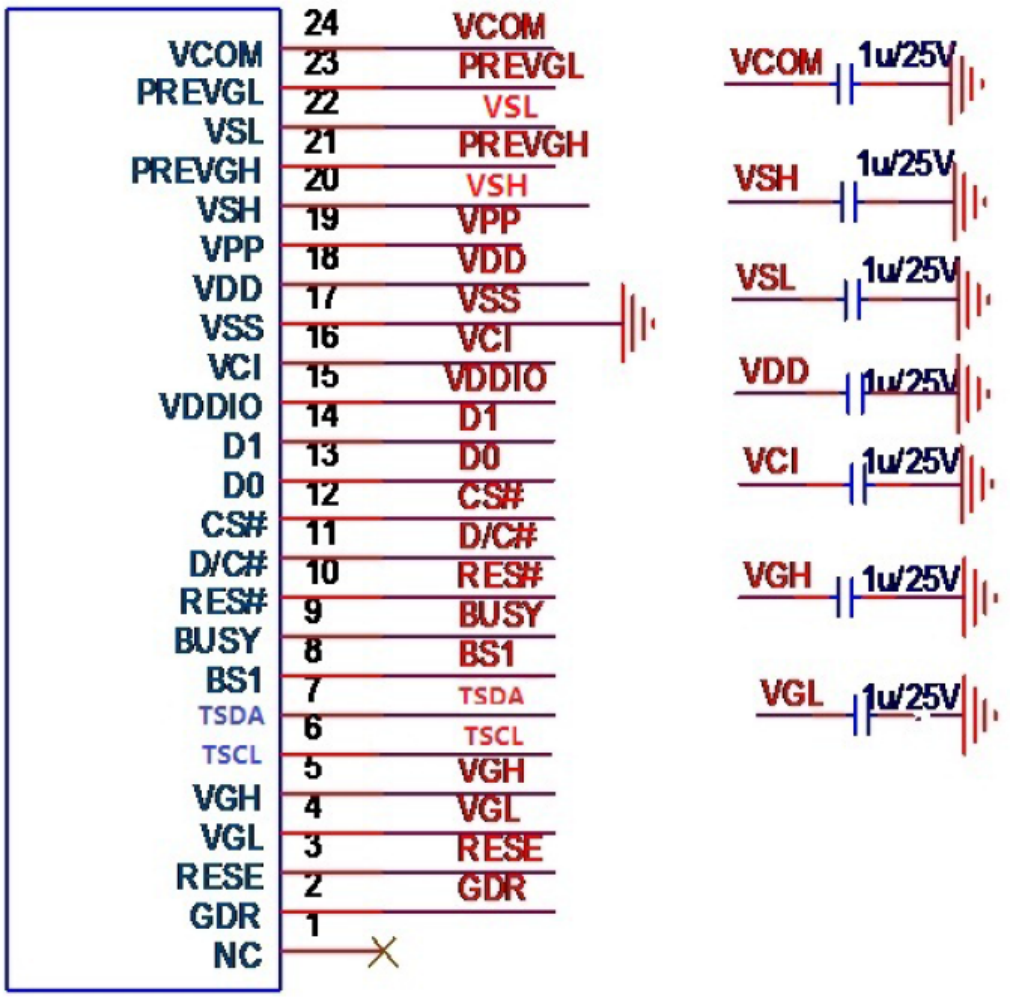
<table>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers
will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Write VCOM Register</td><td>Write VCOM register from MCU interface.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>32</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Write LUT Register</td><td>Write LUT register from MCU [240 bits], (excluding the VSH/VSL and Dummy bit)</td></tr>
<tr><td>0
0
0
…
0
0</td><td>1
1
1
…
1
1</td><td colspan="9">LUT
[30 bytes]</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Set Dummy Line Period</td><td>Set A[7:0] = 1Bh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Set Gate Line Width</td><td>Set B[3:0] = Bh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Border Waveform Control</td><td>Select border waveform for VBD
A [7] Follow Source at Initial Update Display
A[7]=0: [POR]
A[7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE.
A[6] Select GS Transition/ Fix Level for VBD
A[6]=0: Select GS Transition A[3:0] for VBD
A[6]=1: Select FIX level Setting A[5:4] for VBD [POR]
A[5:4] Fix Level Setting for VBD

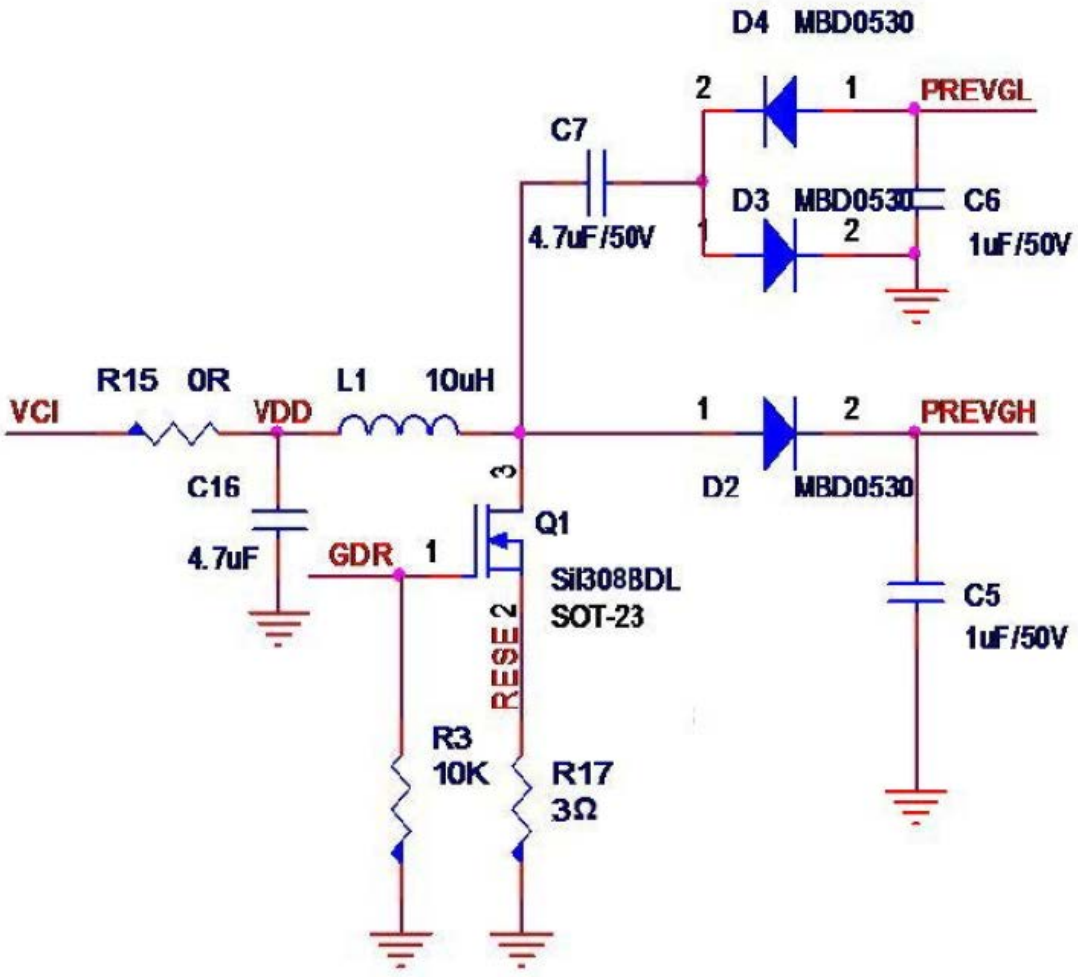
<table><tr><th>A[5:4]</th><th>VBD level</th></tr><tr><td>00</td><td>VSS</td></tr><tr><td>01</td><td>VSH</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11 [POR]</td><td>HiZ</td></tr></table>
A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0])

<table><tr><th>A[1:0]</th><th>GSC</th><th>GSD</th></tr><tr><td>01 [POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>0</td><td>0</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
</table>

0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0] = 00h B[4:0] = 18h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set RAM Y - address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0] = 0C7h B[8:0] = 0000h
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] = 00h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0] = 0C7h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read Commands.

8. Reference Circuit




D4 MBD0530
2
1
PREVGL
C7
4.7uF/50V
D3 MBD0530
C6
1uF/50V
2
1
R15 0R
L1 10uH
VCI
VDD
1
2
PREVGH
C16
4.7uF
3
Q1
GDR
1
Si1308BDL
SOT-23
D2 MBD0530
C5
1uF/50V
RESE2
R3
10K
R17
3Ω

9. Maximum Ratings

9.1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.5 to +4.0	V
Operating Temp. range	T_{OPR}	0 to +50	°C
Storage Temp. range	T_{STG}	-25 to +60	°C
Humidity Range	RH	40~70	%
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

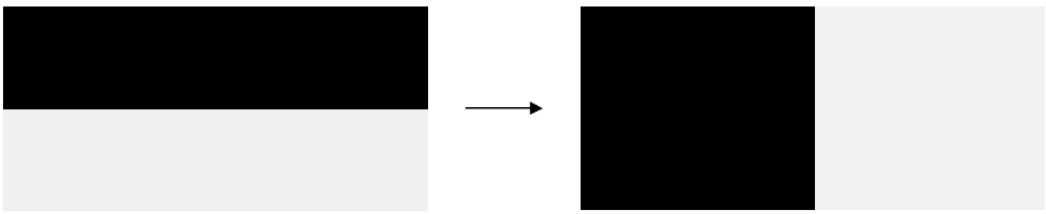
9.2. DC Characteristics

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, T_{OPR} = 25°C

Parameter	Symbol	Conditions	Application Pin	Min	Typ	Max	Unit
Logic Supply Voltage	V_{CI}	-	V_{CI}	2.4	3.3	3.7	V
High Level Input Voltage	V_{IH}	-	D1 (SDIN), D0 (SCLK), CS#, D/C#, RES#, BS1	$0.8V_{DDIO}$	-	V_{CI}	V
Low Level Input Voltage	V_{IL}	-	0		-	$0.2V_{DDIO}$	V
High Level Output Voltage	V_{OH}	IOH= -100uA	V_{CI}-0.4	$0.9V_{DDIO}$	-	-	V
Low Level Output Voltage	V_{OL}	IOL= 100uA	0	-	-	$0.1V_{DDIO}$	V
Module Operating Current	I_{UPDATE}	-	-	-	4	-	mA
Deep Sleep Mode	I_{SLEEP}	V_{CI}=3.3V	-	-	0.6	1	uA

The typical power consumption is measured with the following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern, shown below.

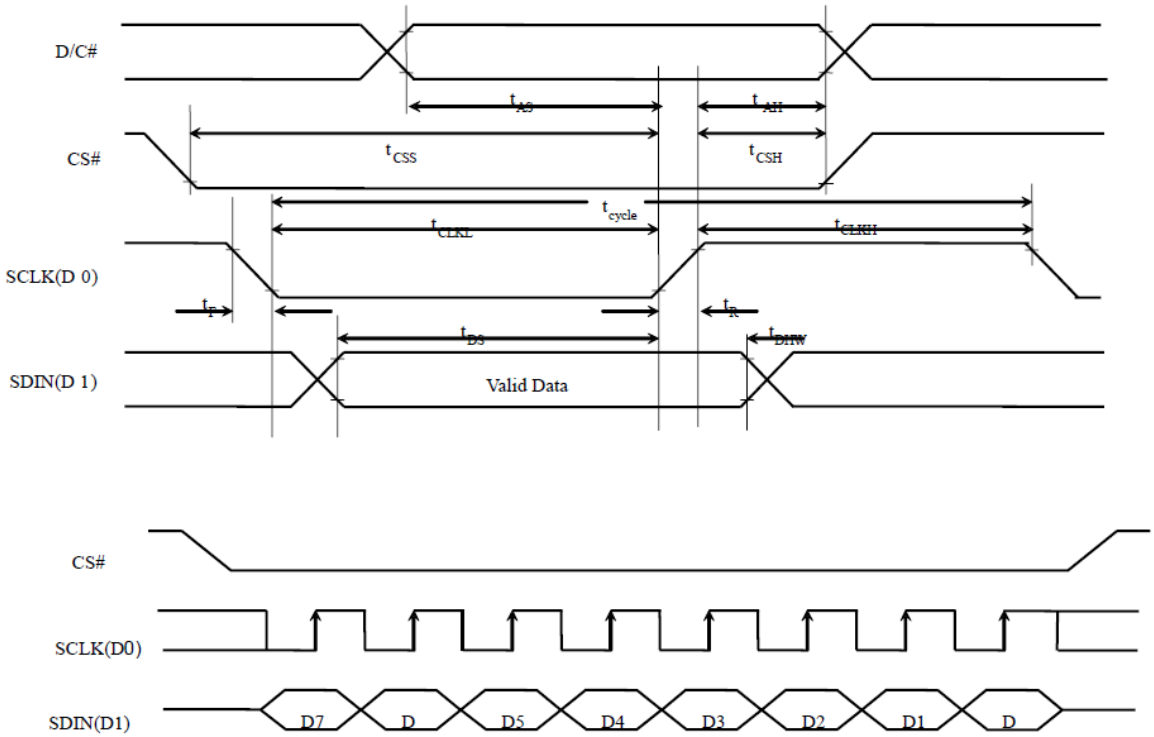
Note: The standby power is the consumed power when the panel controller is in standby mode. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz. V_{COM} is recommended to be set in the range of assigned value ±0.1V.



10. Serial Peripheral Interface Timing

The following specifications apply for: V_{SS} = 0V, V_{CI} = 2.4V to 3.7V, T_{OPR} = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

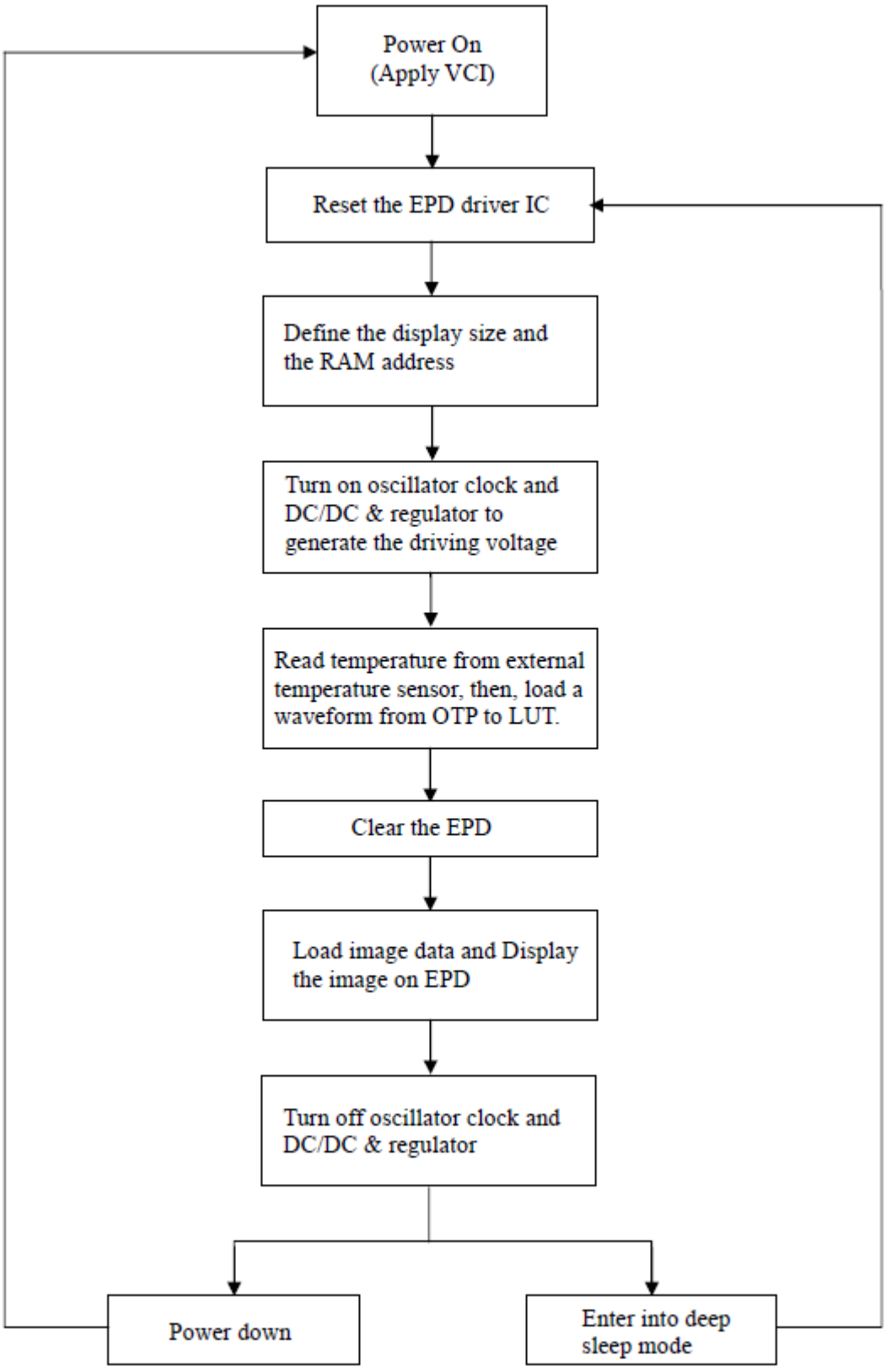


11. Power Consumption

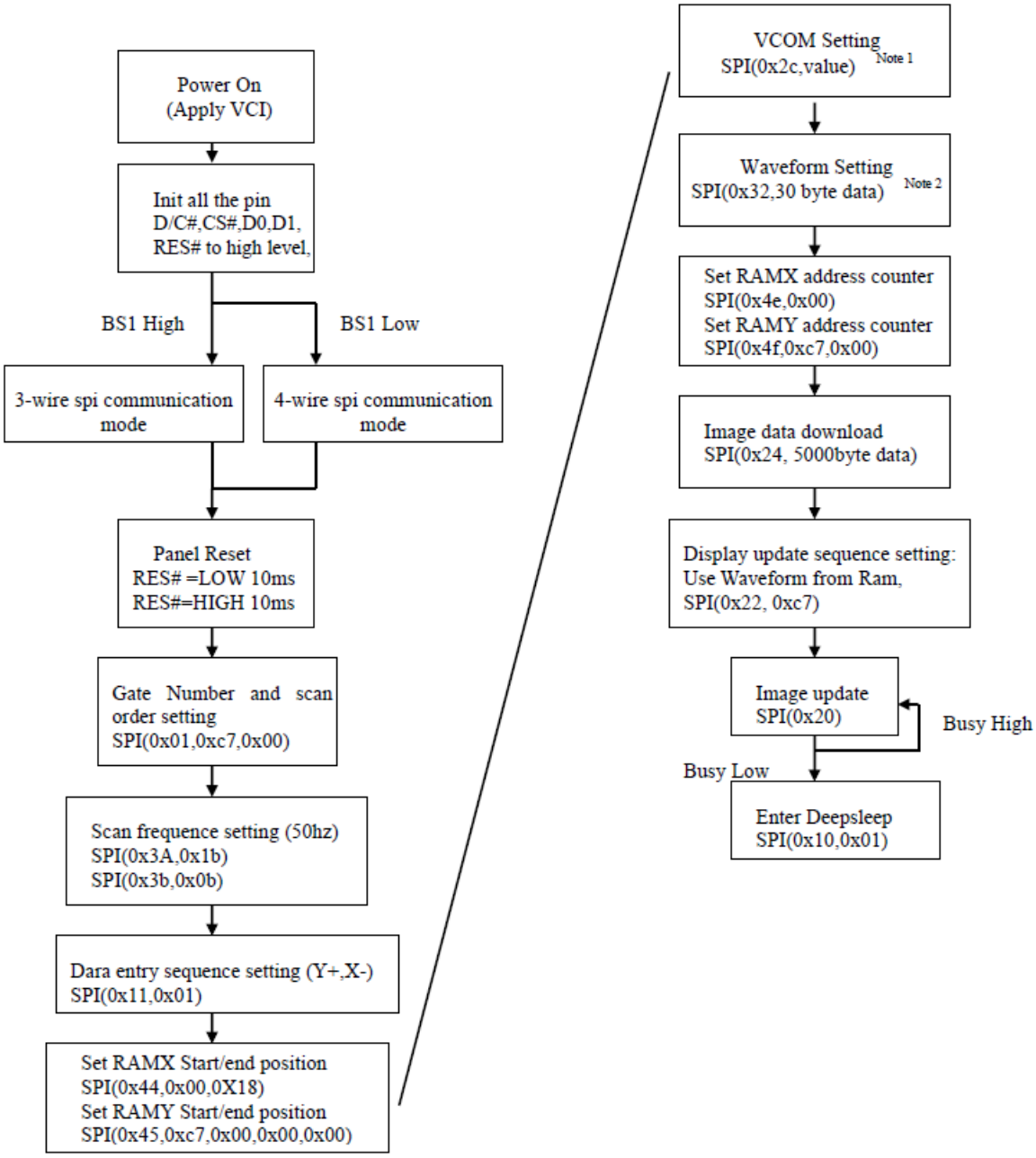
Parameter	Symbol	Condition	Typ	Max	Unit
Panel power consumption during Update	-	25°C	23	-	mA
Deep Sleep Mode	-	25°C	0.6	-	µA

12. Typical Operating Sequence

12.1. Normal Operation Flow



12.2. Refernce Program Code



Note 1: The VCOM setting for different batches, EPD is different.

Note 2: The Waveform setting for different batches, EPD is different.

13. Optical Characteristics

13.1. Specifications

Measurements are made with the illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Type	Max	Unit	Note
R	Reflectance	White	30	35	-	%	13-1
Gn	2Gray Level	-	-	DS+(WS-DS) x n (m-1)	-	L*	-
CR	Contrast Ratio	Indoor	-	10	-	-	-
Panel's Life	-	0°C~50°C	-	1,000,000 times or 5 years	-	-	13-2

WS: White State, DS: Dark State
m: 2

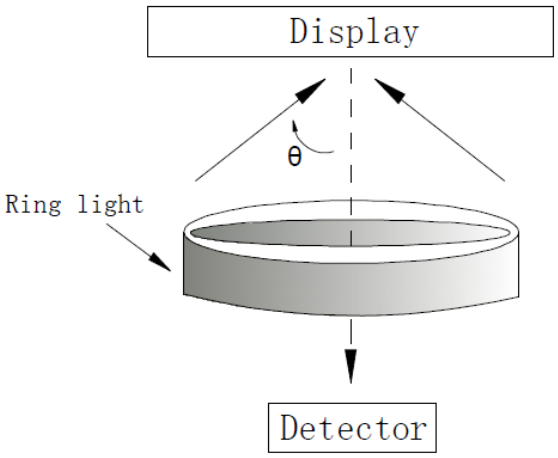
Note (13-1): Luminance meter: Eye – One Pro Spectrophotometer
Note (13-2): Panel life is guaranteed when worked in temperatures below 0 degrees or above 50 degrees.

13.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

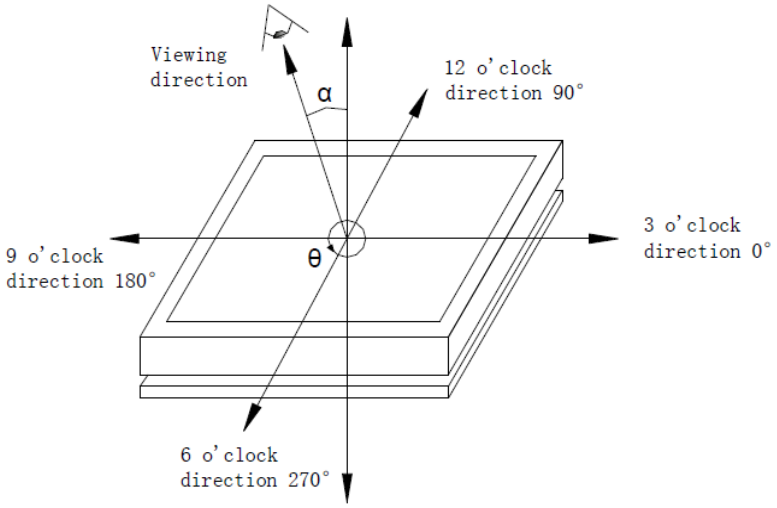


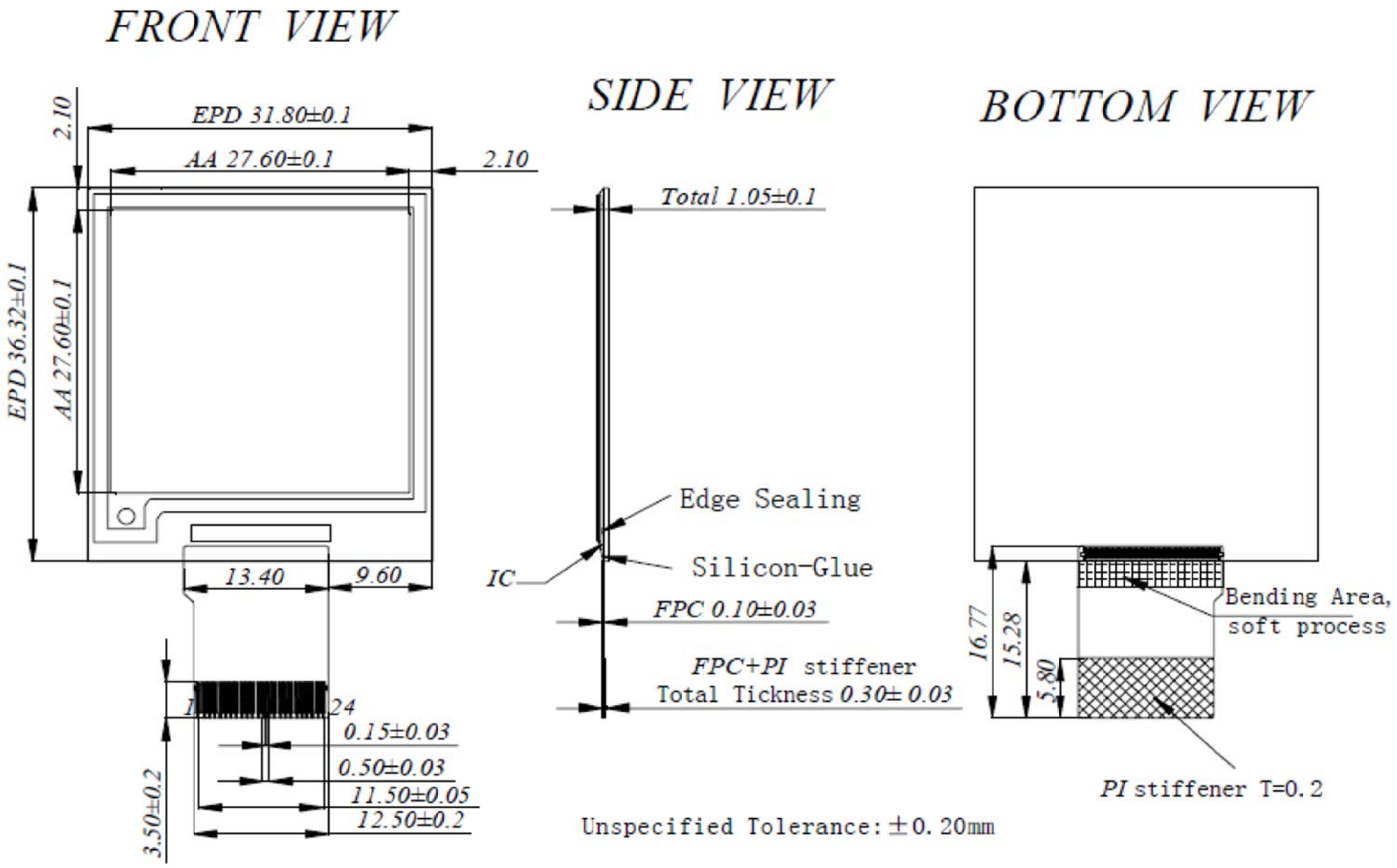
13.3. Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{CENTER} / $L_{WHITE\ BOARD}$)

L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{WHITE\ BOARD}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

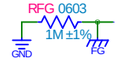




Crystalfontz	PART NUMBER(S) CFAP200200A1-0154	SCALE Not to Scale	COPYRIGHT © 2018 BY CRYSTALFONTZ AMERICA, INC. WWW.CRYSTALFONTZ.COM
	DRAWING NUMBER CFAP200200A1-0154 master	UNITS Millimeters	DATE 2018-04-25

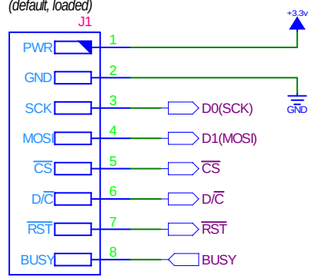
REV	ENGINEER	DATE	REMARKS
0v0	BAC	2018-04-04	Initial Creation
0v1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CN FPC
-	-	-	-
-	-	-	-
-	-	-	-

ESD border discharge

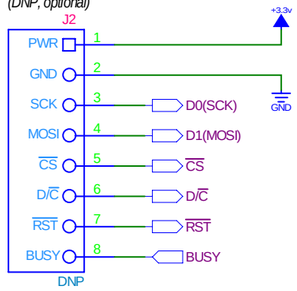


Scope Ground

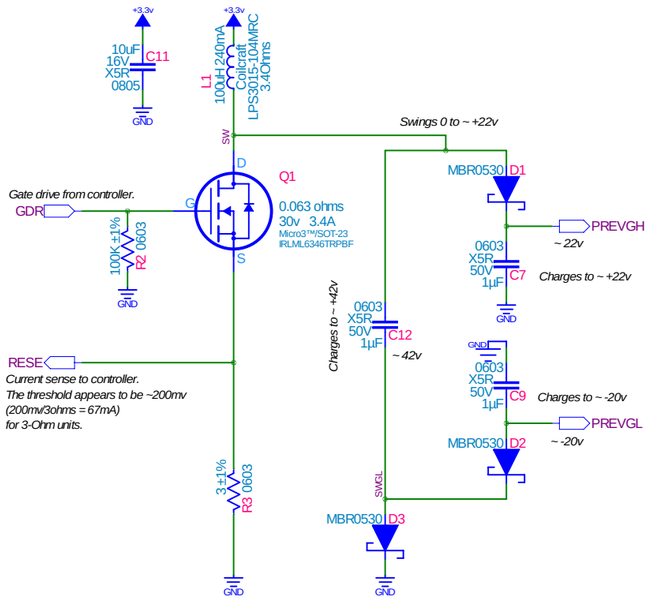
0.1" low-profile SMT header (default, loaded)

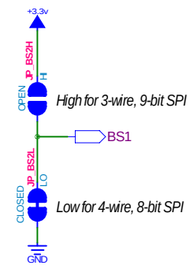


Holes for 0.1" through-hole header (DNP, optional)

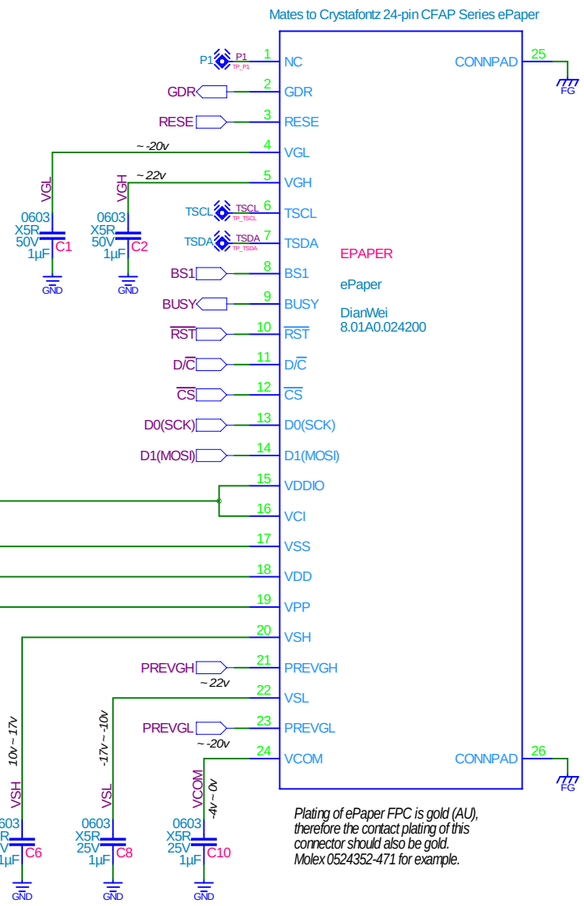


VOLTAGE GENERATION





Mates to Crystafontz 24-pin CFAP Series ePaper



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CFA-10084: ePaper Adapter Board 24-pin (3-ohm)

Page 1 / 1 : Schematic

PRODUCT NAME:	PRODUCT REVISION:	PCB NUMBER:	PCB REVISION:
CFA-10084	0v1	PCB-10084	0v1