ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2018-05-07
for
CFAP176264B0-0270

Crystalfontz America, Inc.
12412 East Saltese Avenue
Spokane Valley, WA 99216-0357
Phone: 888-206-9720
Fax: 509-892-1203
Email: support@crystalfontz.com
URL: www.crystalfontz.com

CONTENTS

1. General Information

Datasheet Revision History
Datasheet Release Date: **2018-05-07** Datasheet for the CFAP176264B0-0270 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

Disclaimer
Certain applications using Crystalfontz America, Inc. products may involve potential risks of death, personal injury, or severe property or environmental damage (“Critical Applications”). CRYSTALFONTZ AMERICA, INC. PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. Inclusion of Crystalfontz America, Inc. products in such applications is understood to be fully at the risk of the customer. In order to minimize risks associated with customer applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazard. Please contact us if you have any questions concerning potential risk applications. Crystalfontz America, Inc. assumes no liability for applications assistance, customer product design, software performance, or infringements of patents or services described herein. Nor does Crystalfontz America, Inc. warrant or represent that any license, either express or implied, is granted under any patent right, copyright, or other intellectual property right of Crystalfontz America, Inc. covering or relating to any combination, machine, or process in which our products or services might be or are used. All specifications in datasheets on our website are, to the best of our knowledge, accurate but not guaranteed. Corrections to specifications are made as any inaccuracies are discovered. Company and product names mentioned in this publication are trademarks or registered trademarks of their respective owners.

2. Description Overview

This ePaper display is a TFT active matrix electrophoretic display with interface and a reference system design. The 2.7" active area contains 264x176 pixels and has 1-bit black/white full display capabilities. An integrated circuit contains a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

3. Features

- High Contrast
- High Reflectance
- Ultra-Wide Viewing Angle
- Ultra-Low Power Consumption
- Pure Reflective Mode
- Bi-Stable Display
- Commercial Temperature Range
- Landscape or Portrait Mode
- Antiglare Hard-Coated Front-Surface
- Low Current Deep Sleep Mode
- On-Chip Display RAM
- Waveform Stored in On-Chip OTP
- Serial Peripheral Interface Available
- On-Chip Oscillator
- On-Chip Booster and Regulator Control for Generating V_{COM}, Gate and Source Driving Voltage
- I^2C Signal Master Interface to Read External Temperature Sensor
- Available in COG Package IC Thickness 280um

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.7	inch	-
Display Resolution	264 (H) × 176 (W)	pixel	dpi: 117
Active Area	57.288 (H) × 38.192 (W)	mm	-
Pixel Pitch	0.217 × 0.217	mm	-
Pixel Configuration	Square	-	-
Outline Dimension	70.42 (H) × 45.8 (W) × 0.98 (D)	mm	-
Weight (typical)	6.0	g	-

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Type	Single	Description	Remark
1	-	NC	No Connection and Do Not Connect with Other NC Pins	Keep Open
2	O	GDR	This Pin is N-MOS Gate Control	
3	P	RESE	Current Sense Input for the Control Loop	
4	P	VSLR	Negative Source Voltage for Red	
5	P	VSL	Negative Source Voltage	
6	O	TSCL	I^2C Clock for External Temperature Sensor	
7	I/O	TSDA	I^2C Data for External Temperature Sensor	
8	I	BS	Input Interface Setting	Note 5-5
9	O	BUSY_N	This Pin Indicates the Driver Status	Note 5-4
10	I	RST_N	Reset	Note 5-3
11	I	DC	Serial Communication Command / Data Input	Note 5-2
12	I	CSB	Serial Communication Chip Select	Note 5-1
13	I	SCL	Serial Communication Clock Input	
14	I/O	SDA	Serial Communication Data Input	
15	P	VDDIO	I/O Voltage Supply	
16	P	VDD	Digital / Analog Power	
17	P	VSS	Digital Ground	
18	P	VDD	Voltage Input & Output	
19	P	VOTP	OTP Program Power	
20	P	VSH	Positive Source Voltage	
21	P	VGH	Positive Gate Voltage	
22	P	VSHR	Positive Source Voltage for Red	
23	P	VGL	Negative Gate Voltage	
24	O	VCOM	VCOM Output	

Note (5-1): This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note (5-2): This pin (DC) is the Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note (5-3): This pin (RST_N) is the reset signal input. The reset is active LOW.

Note (5-4): This pin (BUSY_N) is the Busy_N state output pin. When Busy_N is LOW, the operation of the chip should not be interrupted and no commands should be issued to the module. The driver IC will put Busy_N pin LOW when the driver IC is working such as

- Outputting Display Waveform; or
- Programming with OTP
- Communicating with Digital Temperature Sensor

Note (5-5): This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is “LOW”, 4-line SPI is selected. When it is “HIGH”, 3-line SPI (9 bits SPI) is selected. Please refer to the table below.

Table: Bus Interface Selection

BS1	MPU Interface
L	4-Lines Serial Peripheral Interface (SPI)
H	3-Lines Serial Peripheral Interface (SPI) – 9 bits SPI

6. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0:-: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	ES[1],RES[0],LUT_EN, BWR,UD, SHL, SHD_N, RST_N	07h
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	-	-	-	-	#	#	VDS_EN,VDG_EN	03h
		0	1	-	-	-	-	-	#	#	#	VCOM_HV, VGHL_LV[1], VGHL_LV[0]	20h
		0	1	-	-	#	#	#	#	#	#	VDH[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDL[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDHR[5:0]	03h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OFF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	03h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	00h
		0	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	26h
8	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1		A5h
9	Data Start Transmission 1 (DTM1)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	#	#	#	#	#		00h
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-	Data_flag	00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Partial Data Start Transmission 1 (PDTM1)	0	0	0	0	0	1	0	1	0	0		14h
		0	1	#	#	#	#	#	#	#	#		00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
13	Partial Data Start Transmission 2 (PDTM2)	0	0	0	0	0	1	0	1	0	1		15h
		0	1	#	#	#	#	#	#	#	#		00h
14	Partial Display Refresh (PDRF)	0	0	0	0	0	1	0	1	1	0		16h
		0	1	#	#	#	#	#	#	#	#		00h
15	LUT for VCOM (LUT1)	0	0	0	0	1	0	0	0	0	0		20h
16	White to White LUT (LUTWW)	0	0	0	0	1	0	0	0	0	1		21h
17	Black to White LUT (LUTBW/LUTR)	0	0	0	0	1	0	0	0	1	0		22h
18	White to Black LUT (LUTWB/LUTW)	0	0	0	0	1	0	0	0	1	1		23h
19	Black to Black LUT (LUTBB/LUTB)	0	0	0	0	1	0	0	1	0	0		24h
20	PLL Control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	#	#	#	#	#	#	#	SEL_DIV[1:0], SEL_F[4:0]	3Ch
21	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3]/TS[7:0]	00h
		1	1	#	#	#	-	-	-	-	-	D[2:0]/-	00h
22	Temperature Sensor Calibration (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	#	#	#	#	TSE,TO[3:0]	00h
23	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
24	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
25	V_{COM} and Data Interval Setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[1:0],DDX[1:0],CDI[3:0]	D7h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
26	Low Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	-	-	-	-	-	-	-	LPD		-
27	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
28	TCON Resolution (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	-	-	-	-	-	-	-	#	HRES[8]	00h
		0	1	#	#	#	#	#	#	#	-	HRES[7:1]	00h
		0	1	-	-	-	-	-	-	-	#	VRES[8]	00h
		0	1	#	#	#	#	#	#	#	#	VRES[7:0]	00h
29	Source & Gate Start Setting	0	0	0	1	1	0	0	0	1	0		62h
		0	1	-	-	-	-	-	-	-	#	S_start[8]	00h
		0	1	#	#	#	#	#	#	#	#	S_start[7:0]	00h
		0	1	-	-	-	#	-	-	-	#	gscan, G_start[8]	00h
		0	1	#	#	#	#	#	#	#	#	G-start[7:0]	00h
30	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	-	#	#	#	#	#	#	I^2C_ERR,I^2C_BUSY_N, Data_flag, PON, POF, BUSY_N	02h
31	Auto Measure V_{COM} (AMV)	0	0	1	0	0	0	0	0	0	0		80h
		1	1	-	-	#	#	#	#	#	#	AMV[1:0], XON, AMVS, AMV, AMVE	10h
32	V_{COM} Value (VV)	0	0	1	0	0	0	0	0	0	1		81h
		0	1	-	#	#	#	#	#	#	#	VV[6:0]	00h
33	VCM_DC Setting Register (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	#	#	#	#	#	#	#	VDCS[6:0]	00h
34	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0h
		0	1	1	0	1	0	0	1	0	1		A5h
35	Active Program (APG)	0	0	1	0	1	0	0	0	0	1		A1h
36	Read OTP Data (ROTP)	0	0	1	0	1	0	0	0	1	0		A2h
		1	1	#	#	#	#	#	#	#	#		-

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	LUT_EN	BWR	UD	SHL	SHD_N	RST_N

RES [1:0]: Display Resolution setting (source x gate)

00b: 320x300 (Default)

01b: 300x200

10b: 296x160

11b: 296x128

LUT_EN: LUT selection setting

0: Using LUT from OTP. (Default)

1: Using LUT from register

BWR: Color selecting setting

0: Pixel with B/W/Red. Run both LU1 and LU2. (Default)

1: Pixel with B/W. Run LU1 only.

UD: Gate Scan Direction

0: Scan down. First line to last line: Gn → …→ G1 (Default)

1: Scan up. (Default) First line to last line: G1 → … → Gn

SHL: Source Shift direction

0: Shift left. First data to last data: Sn → … → S1

1: Shift right. First data to last data: S1 → … → Sn (Default)

SHD_N: Booster Switch

0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating.

1: Booster ON (Default)

When SHD_N becomes LOW, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will be based on previous condition and keep floating.

RST_N: Soft Reset

0: No effect.

1: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V. (Default)

When RST_N becomes LOW, the driver will be reset; all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will be based on previous condition and keep floating.

(2) Power Setting Register (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]	
	0	1	-	-	VDH[5:0]					
	0	1	-	-	VDL[5:0]					
	0	1	-	-	VDHR[5:0]					

VDS_EN: Source power selection

0: External source power from VDH/VDL pins.

1: Internal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection

0: External VDNS power from VGH/VGL pins (VDNG_EN open)

1: Internal DC/DC function for generating VGH/VGL

VCOM_HV: VCOM Voltage Level

0: VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC

1: VCOML=VGH, VCOML=VGL

VGHL_LV [1:0]: VGH / VGL Voltage Level selection

VGHL_LV	VGHL Voltage Level
00(Default)	VGH=16V, VGL= -16V
01	VGH=15V, VGL= -15V
10	VGH=14V, VGL= -14V
11	VGH=13V, VGL= -13V

VDH [5:0]: Internal VDH power selection for B/W pixel. (Default value: 100110b)

VDH	VDH_V	VDH	VDH_V
000000	2.4V	…	…
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

VDL [5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V
000000	-2.4V	…	…
000001	-2.6V	100110	-10.0V
000010	-2.8V	100111	-10.2V
000011	-3.0V	101000	-10.4V
000100	-3.2V	101001	-10.6V
000101	-3.4V	101010	-10.8V
000110	-3.6V	101011	-11.0V
000111	-3.8V	(others)	-11.0V

VDHR [5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR	VDHR _V	VDHR	VDHR _V
000000	2.4V	…	…
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

(3) Power OFF (PWR) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will power off following the Power Off Sequence.

After the Power Off command, BUSY_N signal will drop form HIGH to LOW. When finishing the power off sequence, BUSY_N signal will rise from LOW to HIGH.

This command will turn off the charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but the register data will be kept until VDD becomes OFF.

Source Driver output and VCOM will remain as the previous condition, which may have 2 conditions: 0V or floating.

(4) Power OFF Sequence Setting (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	VSH_OFF[1:0]		VSL_OFF[1:0]		VSHR_OFF[1:0]	

VSHR_OFF [1:0]: 00:5ms (Default) 01:10ms 10:20ms 11:40ms

VSL_OFF [1:0]: 00:5ms (Default) 01:10ms 10:20ms 11:40ms

VSH_OFF [1:0]: 00:5ms (Default) 01:10ms 10:20ms 11:40ms

(5) Power ON (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON following the Power ON Sequence.

After the Power ON command, BUSY_N signal will drop from HIGH to LOW. When finishing the power off sequence, BUSY_N signal will rise from LOW to HIGH.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	0	1

This command allows the user to read the temperature sensor or detect low power in the power off mode. After power on measure command, driver will switch on relevant command with LOW Power detection (R51H) and temperature measurement (R40H).

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting Data Transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA [7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 100mS

BTPHA [5:3]: Driving strength of phase A.

000b: strength 1 001b: strength 2 **010b: strength 3**
011b: strength4 100b: strength 5 101b: strength 6
110b: strength 7 111b: strength 8 (strongest)

BTPHA [2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB [7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 100mS

BTPHB [5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3**
011b: strength4 100b: strength 5 101b: strength 6
110b: strength 7 111b: strength 8 (strongest)

BTPHB [2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC [5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3**
011b: strength4 100b: strength 5 101b: strength 6
110b: strength 7 111b: strength 8 (strongest)

BTPHC [2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(9) Data Start Transmission 1 (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting Data Transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and writes the data to SRAM. When data transmission is complete, command 11H must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

(10) Data Stop (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping Data Transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10H) or “Data Stop” (R11H) commands and when data_flag=1, BUSY_N signal will become “0” and refreshing of panel starts. This command only actives when BUSY_N=”1”.

(11) Display Refresh Command (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the Display	0	0	0	0	0	1	0	0	1	0

After this command is issued, the driver will refresh the display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY_N signal will become “0”. This command is only active when BUSY_N=”1”.

(12) Partial Data Start Transmission 1 Register (R14H)

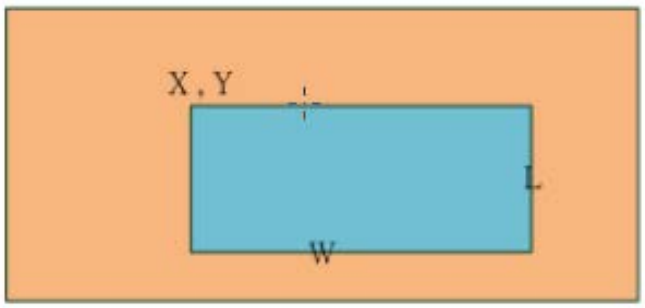
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Data Start Transmission 1	0	0	0	0	0	1	0	1	0	0
	0	1	-	-	-	-	-	-	-	X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
	-	-	-	-	-	-	-	-	-	Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1	-	-	-	-	-	-	-	W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0
	-	-	-	-	-	-	-	-	-	L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]
	0	1	Kpixel1	Kpixel2	Kpixel3	Kpixel4	Kpixel5	Kpixel6	Kpixel7	Kpixel8
	0	1	-	-	-	-	-	-	-	-
	0	1	Kpixel (n-7)	Kpixel (n-6)	Kpixel (n-5)	Kpixel (n-4)	Kpixel (n-3)	Kpixel (n-2)	Kpixel (n-1)	Kpixel (n)

This command starts transmitting data and writes the data to SRAM. When data transmission is complete, command 11H must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

Partial Update Location and Area



NOTE: X and W should be the multiple of 8.

(13) Partial Data Start Transmission 2 Register (R15H)

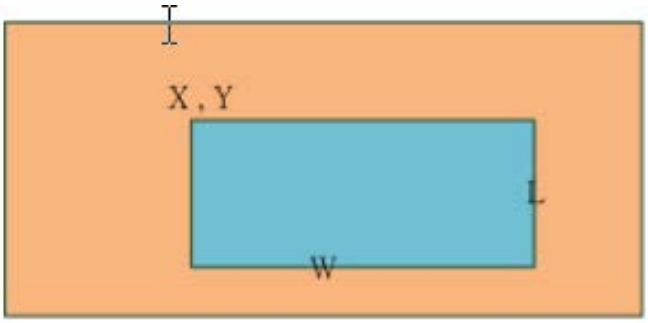
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Data Start Transmission 2	0	0	0	0	0	1	0	1	0	1
	0	1	-	-	-	-	-	-	-	X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
	-	-	-	-	-	-	-	-	-	Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1	-	-	-	-	-	-	-	W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0
	-	-	-	-	-	-	-	-	-	L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]
	0	1	Kpixel1	Kpixel2	Kpixel3	Kpixel4	Kpixel5	Kpixel6	Kpixel7	Kpixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Kpixel (n-7)	Kpixel (n-6)	Kpixel (n-5)	Kpixel (n-4)	Kpixel (n-3)	Kpixel (n-2)	Kpixel (n-1)	Kpixel (n)

This command starts transmitting data and writes the data to SRAM. When data transmission is complete, command 11H must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM.

Partial Update Location and Area

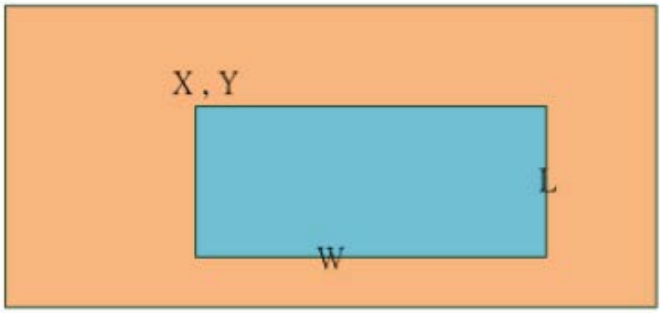


NOTE: X and W should be the multiple of 8.

(14) Partial Display Refresh Command (R16H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Display Refresh	0	0	0	0	0	1	0	1	1	1
	0	1	DFV_EN	-	-	-	-	-	-	X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
	-	-	-	-	-	-	-	-	-	Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1	-	-	-	-	-	-	-	W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	W[2]	W[1]	W[0]
	-	-	-	-	-	-	-	-	-	L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]

When this command is sent the driver will refresh the display (data/VCOM) base on SRAM data and LUT. Only the area (X, Y, W, L) will update. The other pixel outputs will follow VCOM LUT. After the display refresh command, the BUSY_N signal will become “0”.



NOTE: X and W should be the multiple of 8.

DFV_EN: data follow VCOM function on display area.

DFV_EN=1: Only effective in B/W mode, if pixel from “New Data” SRAM is equal to “Old Data” SRAM on the display area, the pixel output would follow VCOM LUT.

DFV_EN=0: Data doesn’t follow VCOM LUT.

This command is only active when BUSY_N = “1”.

(15) VCOM LUT (LUTC) (R20H)

This command builds the Look-up Table for VCOM

(16) W2W LUT (LUTWW) (R21H)

This command builds the Look-up Table for White-to-White.

(17) B2W LUT (LUTBW/LUTR) (R22H)

This command builds the Look-up Table for Black-to-White.

(18) W2B LUT (LUTWB/LUTW) (R23H)

This command builds the Look-up Table for White-to-Black.

(19) B2B LUT (LUTBB / LUTB) (R24H)

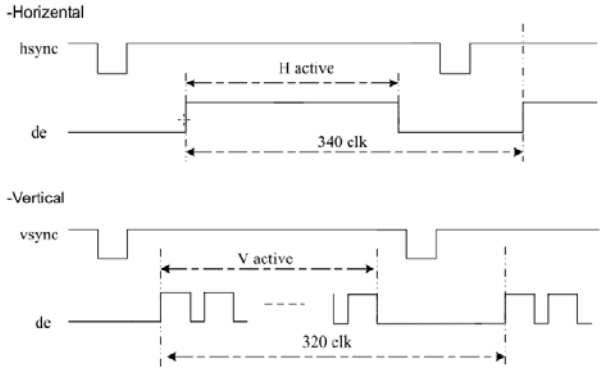
This command builds the Look-up Table for Black-to-Black.

(20) PLL Control (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	SEL_DIV[1:0]		SEL_F[4:0]				

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

SEL_F[5:0]	SEL_DIV[1:0]				SEL_F[5:0]	SEL_DIV[1:0]			
	00	01	10	11		00	01	10	11
000000	156.25	78.13	39.06	-	100000	153.49	76.75	38.37	-
000001	159.01	79.5	39.75	-	100001	150.74	75.37	37.38	-
000010	161.76	80.88	40.44	20.22	100010	147.98	73.99	36.99	-
000011	164.52	82.26	41.13	20.57	100011	145.22	72.61	36.31	-
000100	167.28	83.64	41.82	20.91	100100	142.46	71.23	35.62	-
000101	170.04	85.02	42.51	21.25	100101	139.71	69.85	34.93	-
000110	172.79	86.4	43.2	21.6	100110	136.95	68.47	34.24	-
00111	175.55	87.78	43.89	21.94	100111	134.19	67.1	33.55	-
001000	178.31	89.15	44.58	22.29	101000	131.43	65.72	32.86	-
001001	181.07	90.53	45.27	22.63	101001	128.68	64.34	32.17	-
001010	183.82	91.91	45.96	22.98	101010	125.92	62.96	31.48	-
001011	186.58	93.29	46.65	23.32	101011	123.16	61.58	30.79	-
001100	189.34	94.67	47.33	23.67	101100	120.4	60.2	30.1	-
001101	192.1	96.05	48.02	24.01	101101	117.65	58.82	29.41	-
001110	194.85	97.43	48.71	24.36	101110	114.89	57.44	28.72	-
001111	197.61	98.81	49.4	24.7	101111	112.13	56.07	28.03	-
010000	-	100.18	50.09	25.05	110000	109.38	54.69	27.34	-
010001	-	101.56	50.78	25.39	110001	106.62	53.31	26.65	-
010010	-	102.94	51.47	25.74	110010	103.86	51.93	25.97	-
010011	-	104.32	52.16	26.08	110011	101.1	50.55	25.28	-
010100	-	105.7	52.85	26.42	110100	98.35	49.17	24.59	-
010101	-	107.08	53.54	26.77	110101	95.59	47.79	23.9	-
010110	-	108.46	54.23	27.11	110110	92.83	46.42	23.21	-
010111	-	109.83	54.92	27.46	110111	90.07	45.04	22.52	-
011000	-	111.21	55.61	27.8	111000	87.32	43.66	21.83	-
011001	-	112.59	56.3	28.15	111001	84.56	42.28	21.14	-
011010	-	113.97	56.99	28.49	111010	81.8	40.9	20.45	-
011011	-	115.35	57.67	28.84	111011	79.04	39.52	-	-
011100	-	116.73	58.36	29.18	111100	76.29	38.14	-	-
011101	-	118.11	59.05	29.53	111101	73.53	36.76	-	-
011110	-	119.49	59.74	29.87	111110	70.77	35.39	-	-
011111	-	120.86	60.43	30.22	111111	68.01	34.01	-	-



(21) Temperature Sensor Calibration (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS [7:0]: When TSE (R41h) is set to 0, this command reads the internal temperature sensor value.

D [10:0]: When TSE (R41h) is set to 1, this command reads the external LM75 temperature sensor value.

(22) Temperature Sensor Calibration (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	-	-	TO[3:0]			

This command selects the Internal and External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (Default) 1: Disable; using external sensor.

TO[3:0] Temperature offset.

TO[3:0] sign bit 0b: + 1b: -

TO[2:0] offset value

TO[3:0]	Calculation	TO[3:0]	Calculation
0000 b	0	1000	-8
0001	1	1001	-7
0010	2	1010	-6
-	-	-	-
0110	6	1110	-2
0111	7	1111	-1

(23) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	0	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6] I^2C Write Byte Number

00b: 1 byte (head byte only)
01b: 2 bytes (head byte + pointer)
10b: 3 bytes (head byte + pointer + 1st parameter)
11b: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor.

WLSB[7:0]: LSByte of write-data to external temperature sensor.

This command is only active after R04H(PON) or R05H(PMES)

(24) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor.

RLSB[7:0]: LSByte read data from external temperature sensor.

This command is only active after R04H(PON) or R05H(PMES).

(25) VCOM and Data Interval Setting (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval Between VCOM and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept ($20H_{SYNC}$).

VBD[1:0]: Border data selection

B/W/Red mode (BWR=0)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1 (Default)	00	LUTB
	01	LUTR		01	LUTW
	10	LUTW		10	LUTR
	11	LUTB		11 (Default)	Floating

B/W mode (BWR=1)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1 (Default)	00	Floating
	01	LUTBW (1 → 0)		01	LUTWB (1 → 0)
	10	LUTWB (0 → 1)		10	LUTBW (0 → 1)
	11	Floating		11	Floating

DDX[1:0]: Display polarity.

DDX[1] for RED data, DDX[0] for BW data om the B/W/Red mode.

DDX[0] for B/W mode.

B/W/Red mode (BWR=0)

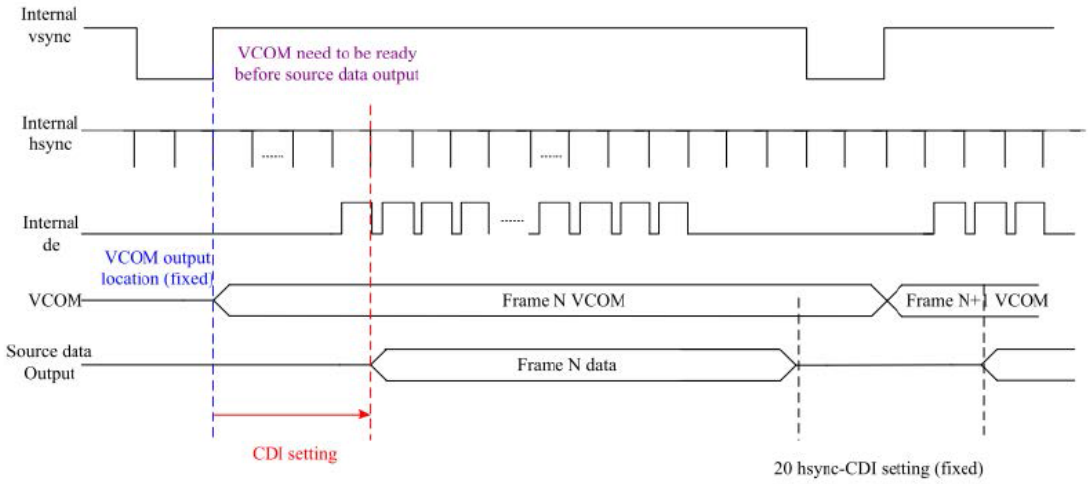
DDX[1:0]	Data {Red, B/W}	LUT	DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW	10	00	LUTR
	01	LUTB		01	LUTR
	10	LUTR		10	LUTW
	11	LUTR		11	LUTB
01 (Default)	00	LUTB	11	00	LUTR
	01	LUTW		01	LUTR
	10	LUTR		10	LUTB
	11	LUTR		11	LUTW

B/W mode (BWR=1)

DDX[0]	Data {New, Old}	LUT	DDX[0]	Data {New, Old}	LUT
00	00	LUTWW (0 → 0)	1 (Default)	00	LUTBB (0 → 0)
	01	LUTBW (1 → 0)		01	LUTWB (1 → 0)
	10	LUTWB (0 → 1)		10	LUTBW (0 → 1)
	11	LUTBB (1 → 1)		11	LUTWW (1 → 1)

CDI[3:0]: VCOM and Data Interval

CDI[3:0]	VCOM and Data Interval	CDI[3:0]	VCOM and Data Interval
0000 b	17 H_{SYNC}	0110	11
0001	16	0111	10 (Default)
0010	15	-	-
0011	14	1101	4
0100	13	1110	3
0101	12	1111	2



(26) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the condition of the battery.

LPD: Interval Low Power Detection Flag

0: Low Power Input (VDD<2.5V)

1: Normal Status (Default)

(27) TCON Setting (TCON) (R60H)

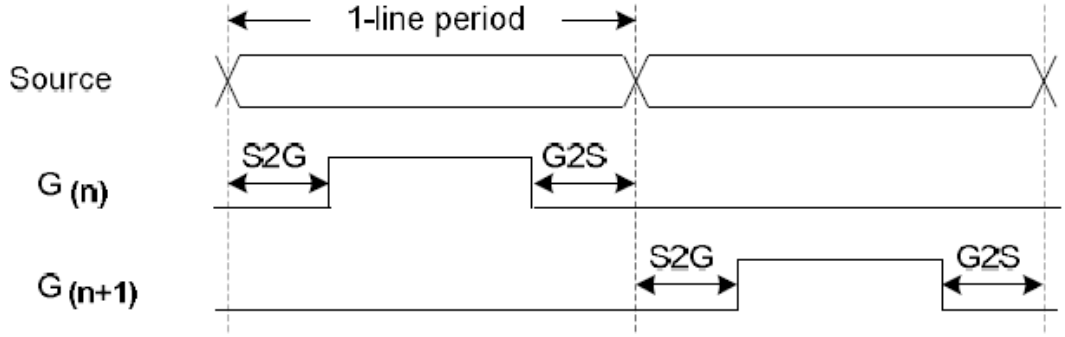
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-Overlap Period	0	0	0	1	0	1	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines the non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap Period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000 b	4		…	…
0001	8		1011	48
0010	12 (Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



(28) Resolution Setting (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution Action	0	0	0	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	-	HRES[8]
	0	1	HRES[7:1]							
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	1	VRES[7:0]							

This command defines the alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[8:1]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Channel Disable Calculation:

GD: First G active = G0; LAST active GD = first active + VRES [7:0]-1

SD: First active channel = S0; LAST active SD = first active + HRES [8:1]*2-1

(29) Source & Gate Start Setting (R62H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution Action	0	0	0	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	-	S_start[8]
	0	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	S_start[1]	S_start[0]
	0	1	-	-	-	-	-	-	-	G_start[8]
	0	1	G_start[7]	G_start[6]	G_start[5]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]

S_Start[8:0]: which source output line is the first date line

G_Start[8:0]: which gate line is the first scan line

gscan: Gate Scan Select

0: Normal Scan
1: Cascade Type 2 Scan

(30) Get Status (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	-	I^2C_ERR	I^2C_BUSY_N	Data_flag	PON	POF	BUSY_N

This command reads the IC status.

I^2C_ERR: I^2C master error status.

I^2C_BUSY_N: I^2C master BUSY_N status (low active)

Data_flag: Driver has already received all the one frame data.

PON: 0: Not in PON mode. 1: In PON mode.

POF: 0: Not in POF mode. 1: In POF mode.

BUSY_N: Driver BUSY_N status (low active)

(31) Auto Measure VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically Measure VCOM	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s 01b: 5s (Default)

10b: 8s 11b:10s

XON: All Gate PM pf AMV

0: Gate normally scans during Auto Measure VCOM period. (Default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source Output of AMV

0: Source output 0V during Auto Measure VCOM period. (Default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog Signal

0: Get VCOM value with the VV command (R18h) (Default)

1: Get VCOM value in analog signal. (external analog to digital converter)

AMVE: Auto Measure VCOM Enable (Disable)

0: Auto Measure VCOM Disable (Default)

1: Auto Measure VCOM Enable

(32) VCOM Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically Measure VCOM	0	0	1	0	0	0	0	0	0	1
	1	1	-	VV[6:0]						

This command gets the VCOM value.

VV[5:0]: VCOM Value Output

VV[5:0]	VCOM Value
000 0000b	-0.10 V
000 0001b	-0.15 V
000 0010b	-0.20 V
:	:
100 1110b	-4.00 V

(33) VCOM-DC Setting (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	VDCS[6:0]						

This command set VCOM_DC value.

VDCS[5:0]: VCOM-DC Setting

VDCS[6:0]	VCOM_DC Value
000 0000b	-0.10 V (Default)
000 0001b	-0.15 V
000 0010b	-0.20 V
:	:
100 1110b	-4.00 V

(34) Program Mode (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0
	0	1	1	0	1	0	0	1	0	1

After this command is issued, the chip will enter the program mode.

The mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(35) Active Program Mode (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

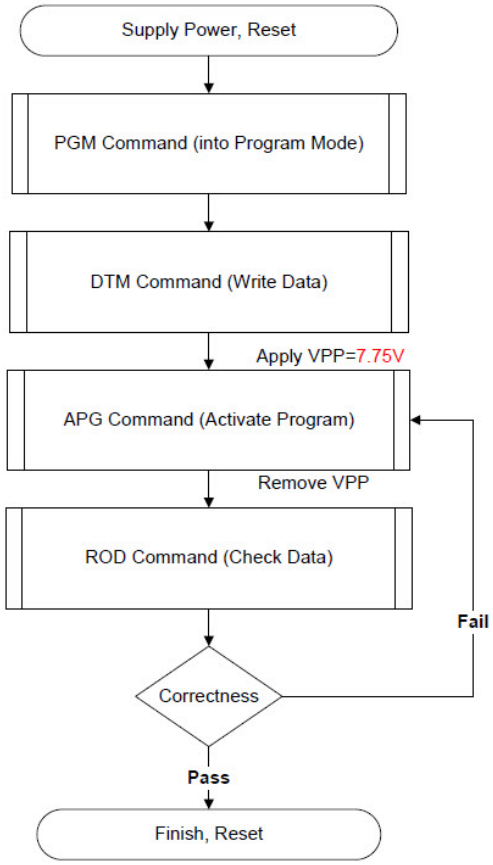
After this command is issued, the chip will enter the program mode.

(36) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP Data for Check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	..							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

This command is used for reading the content of OTP for checking the data of programming.

The value of (n) is dependent on the amount of programmed data, the max address = 0xFFF.



The Sequence of Programming OTP

7. Electrical Characteristics

7.1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to V_{CI} +2.4	V
Operating Temp. range	T_{OPR}	0 to +50	°C
Storage Temp. range	T_{STG}	-25 to +70	°C
Humidity Range	RH	40~70	%
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

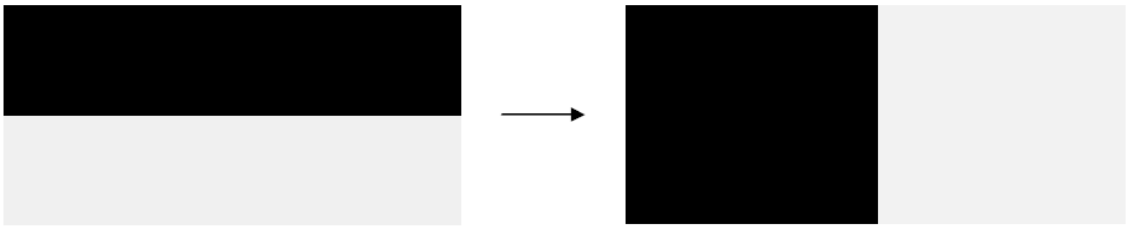
7.2. Panel DC Characteristics

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, Ta = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	V_{CI}	-	2.3	3.3	3.6	V
High Level Input Voltage	V_{IH}	Digital Input Pins	0.7V_{CI}	-	V_{CI}	V
Low Level Input Voltage	V_{IL}	Digital Input Pins	0	-	0.3V_{CI}	V
High Level Output Voltage	V_{OH}	Digital Input Pins, IOH= 400uA	V_{CI}-0.4	-	-	V
Low Level Output Voltage	V_{OL}	Digital Input Pins, IOL= -400uA	GND	-	GND+0.4	V
Operating Temperature	-	-	0	-	50	°C
Storage Temperature	-	-	-25	-	70	°C

The typical power consumption is measured with the following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern, shown below.

Note: The standby power is the consumed power when the panel controller is in standby mode. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz. V_{COM} is recommended to be set in the range of assigned value ±0.1V.



7.3. Panel AC Characteristics

7.3.1. Oscillator Frequency

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, Ta = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator Frequency	Fosc	V_{CI}=2.3 to 3.6V	-	1.625	-	MHz

7.4. MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus Interface	D1	D0	CSB	DC	RST_N
SPI4	SDA	SCL	CSB	DC	RST_N
SPI3	SDA	SCL	CSB	L	RST_N

Table 7-1: MCU Interface Assignment Under Different Bus Interface Mode

Note: L is connected to V_{SS}. H is connected to V_{CI}.

7.4.1. MCU Serial Interface (4-Wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, DC, CSB. In SPI mode, D0 acts as SCL, D1 acts as SDA.

Function	CS#	D/C#	SCL
Write Command	L	L	↑
Write Data	L	H	↑

Table 7-2: Control Pins of 4-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, … D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

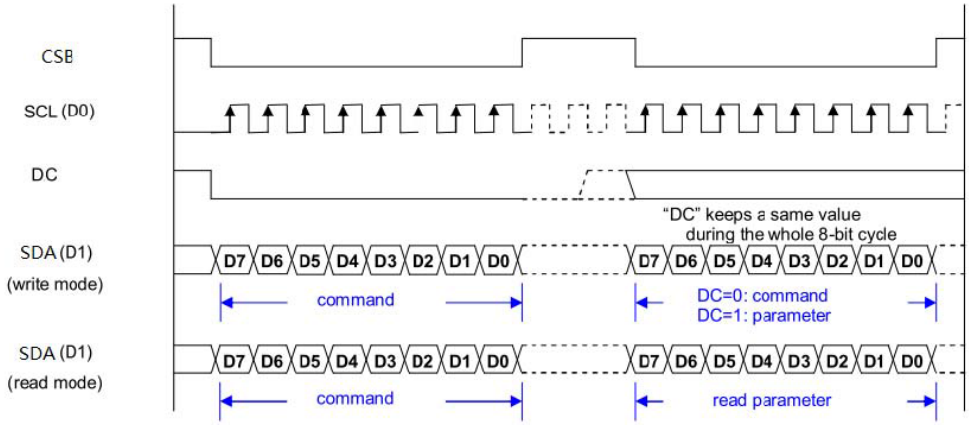


Figure 7-1: Write Procedure in 4-Wire Serial Peripheral Interface Mode

7.4.2. MCU Serial Interface (3-Wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CSB.

In 3-wire SPI mode, D0 acts as SCL, D1 acts as SDA. The pin DC can be connected to an external ground.

The operation is similar to 4-wire serial interface while DC pin is not used. There are altogether 9-bits that will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0). Under serial mode, only write operations are allowed.

Function	CSB	DC	SCL
Write Command	L	Tie LOW	↑
Write Data	L	Tie LOW	↑

Table 7-3: Control Pins of 3-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

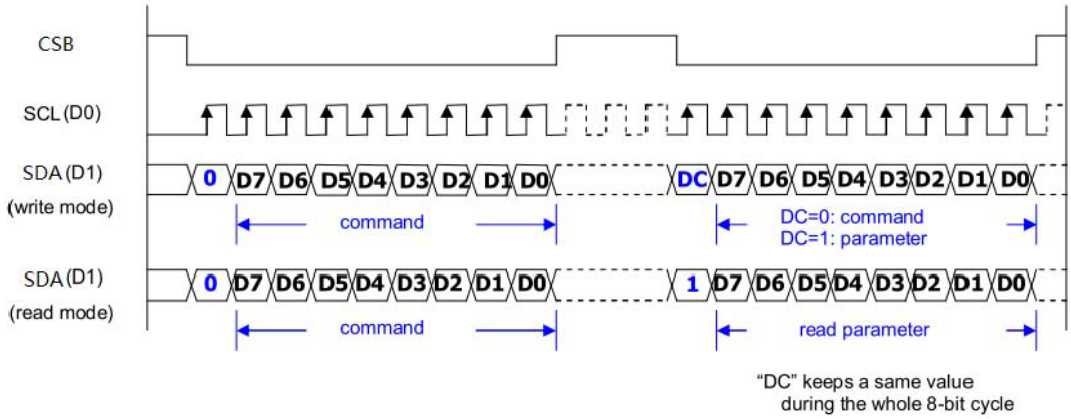
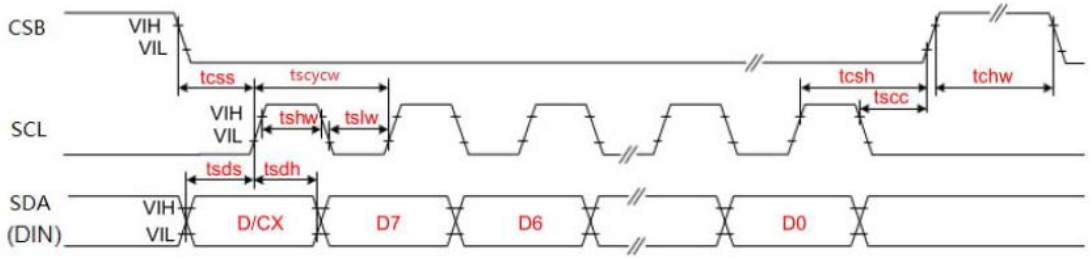
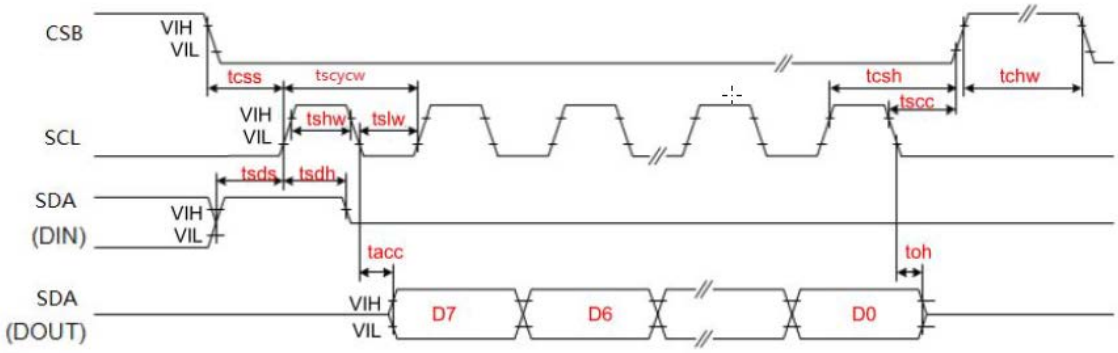


Figure 7-2: Write Procedure in 3-Wire Serial Peripheral Interface Mode

7.5. Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CSB	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCL	Serial Clock Cycle (Write)	100	-	-	ns
tshw		SCL “H” Pulse Width (Write)	35	-	-	ns
tslw		SCL “L” Pulse Width (Write)	35	-	-	ns
tscycr		Serial Clock Cycle (Read)	150	-	-	ns
tshr		SCL “H” Pulse Width (Read)	60	-	-	ns
tslr		SCL “L” Pulse Width (Read)	60	-	-	ns
tsds	SDA (DIN) (DOUT)	Data Setup Time	30	-	-	ns
tsdh		Data Hold Time	30	-	-	ns
tacc		Access Time	-	-	10	ns
toh		Output Disable Time	15	-	-	ns

7.6. Reference Circuit

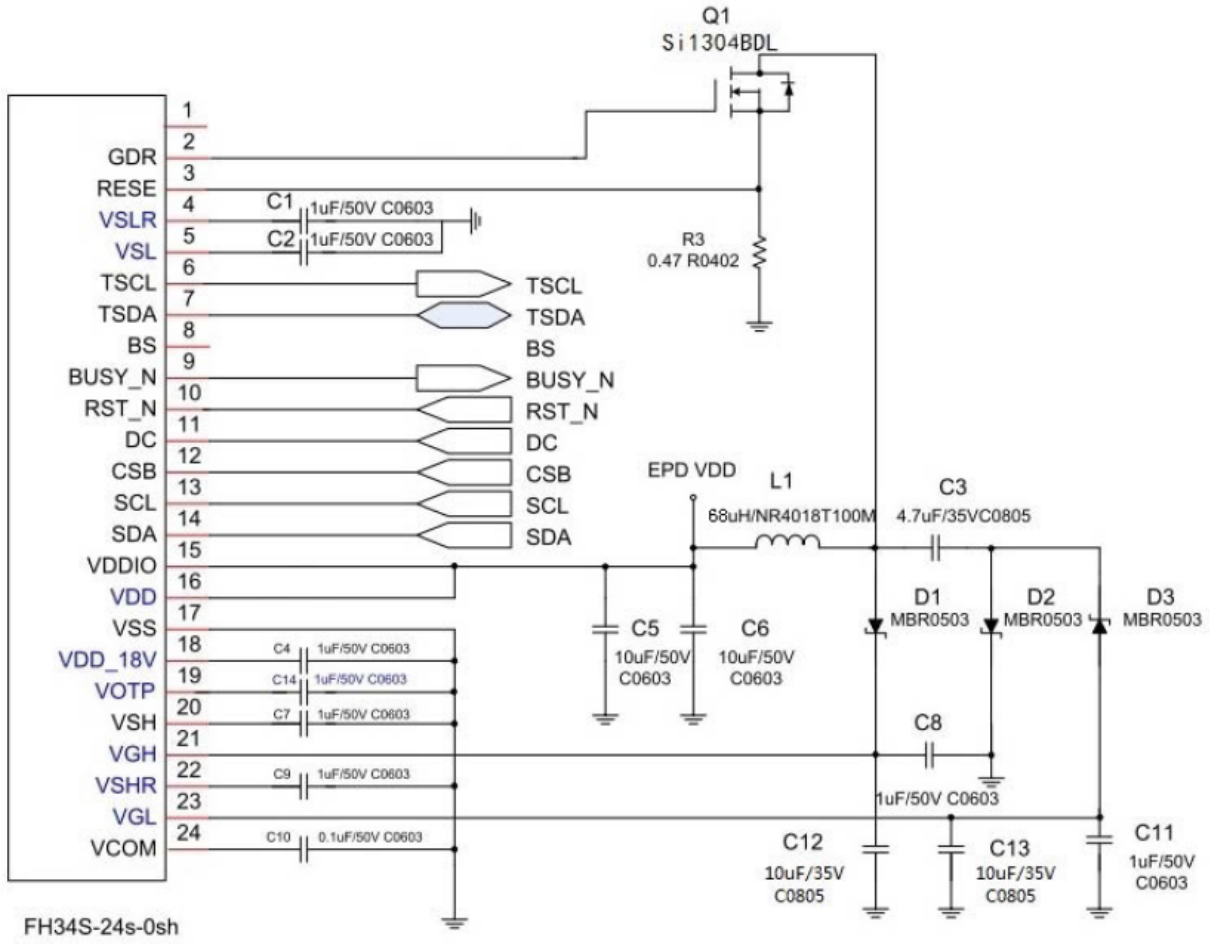
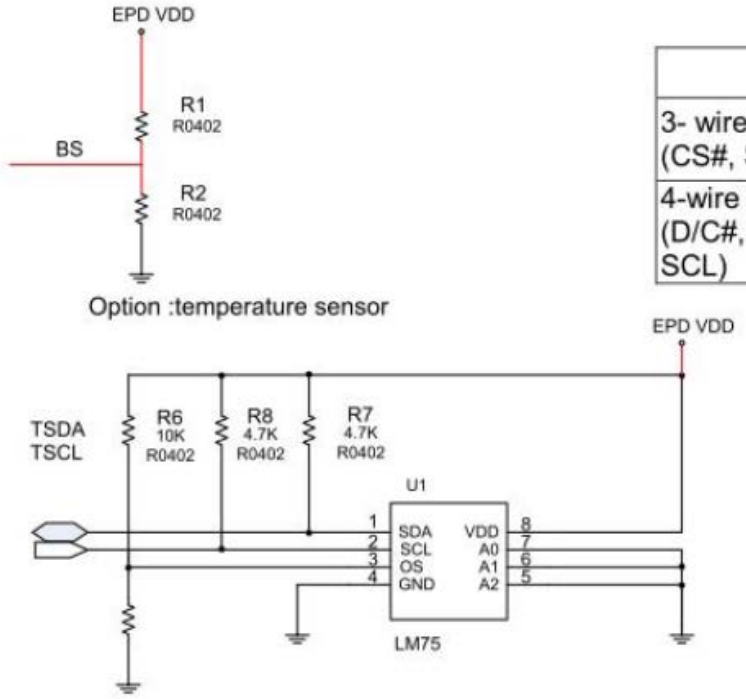


Figure 7-6 (1)



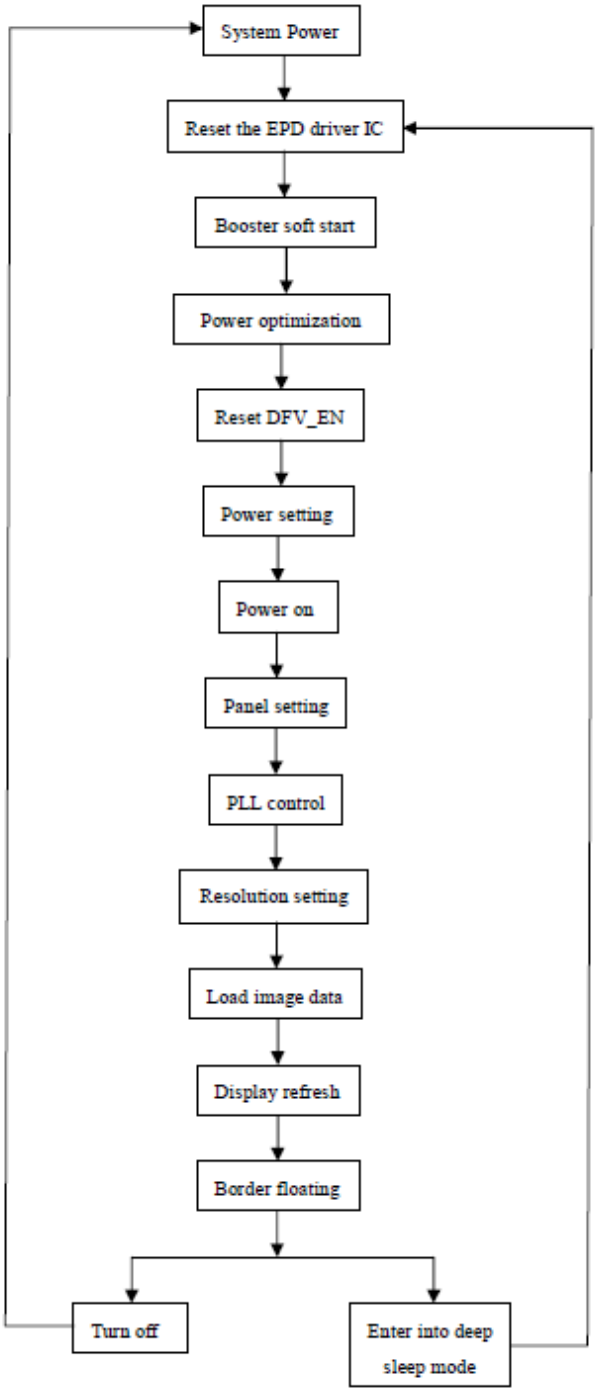
	R1	R2
3- wire SPI (CS#, SDA, SCL)	0K	NC
4-wire SPI (D/C#, CS#, SDA, SCL)	NC	0K

Figure 7-6 (2)

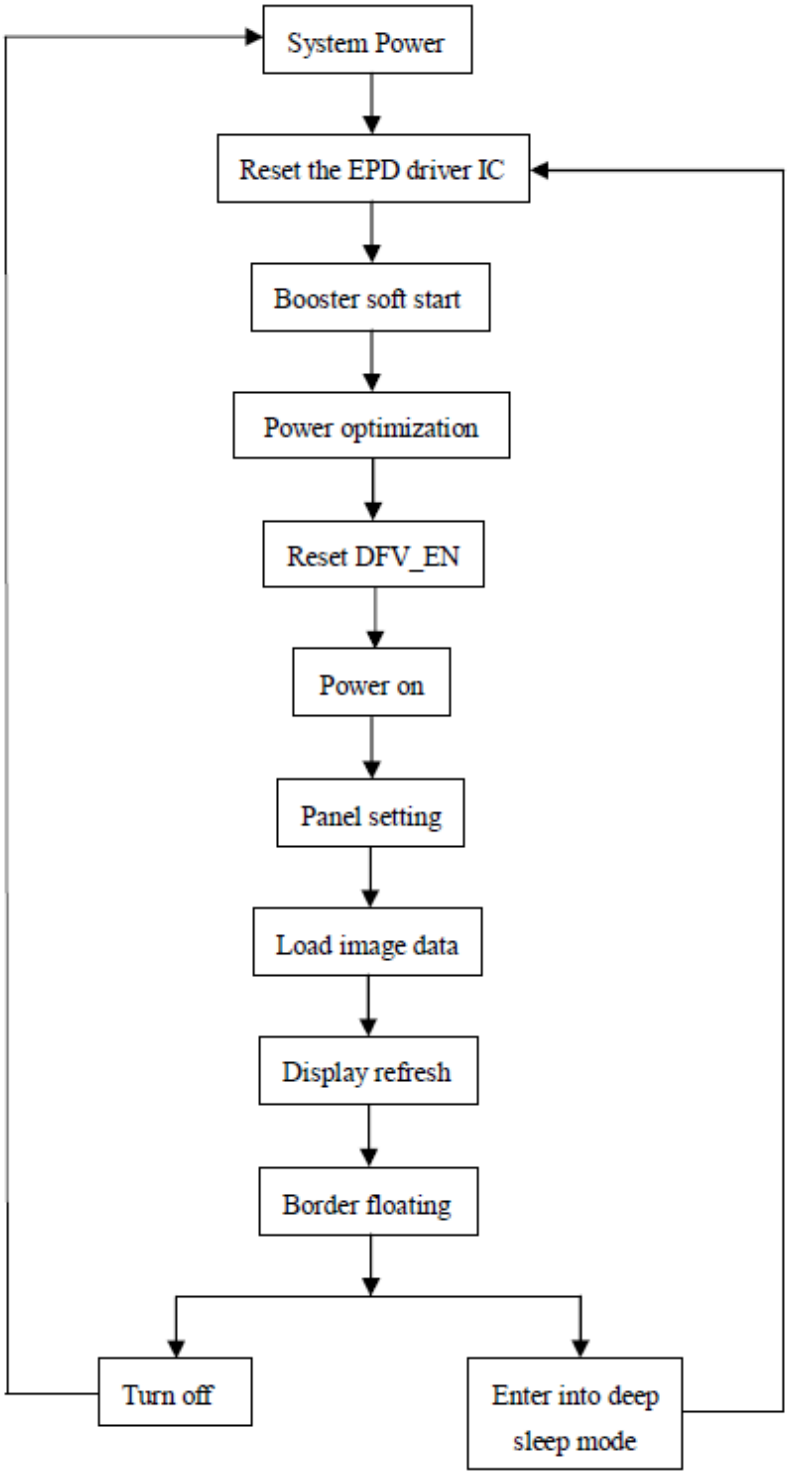
8. Typical Operating Sequence

8.1. Normal Operation Flow

8.1.1. BW Mode & LUT from Register

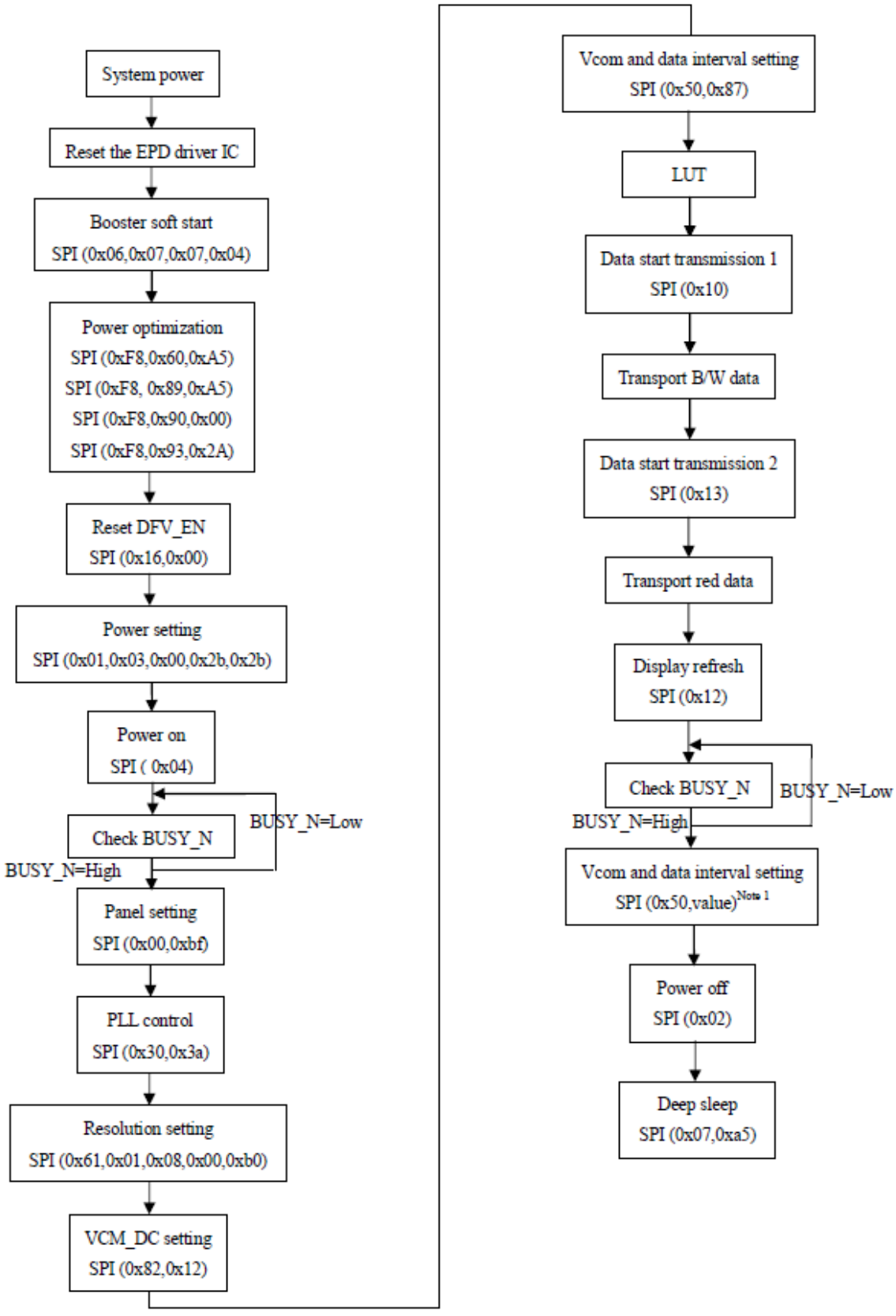


8.1.2. BW Mode & LUT from OTP



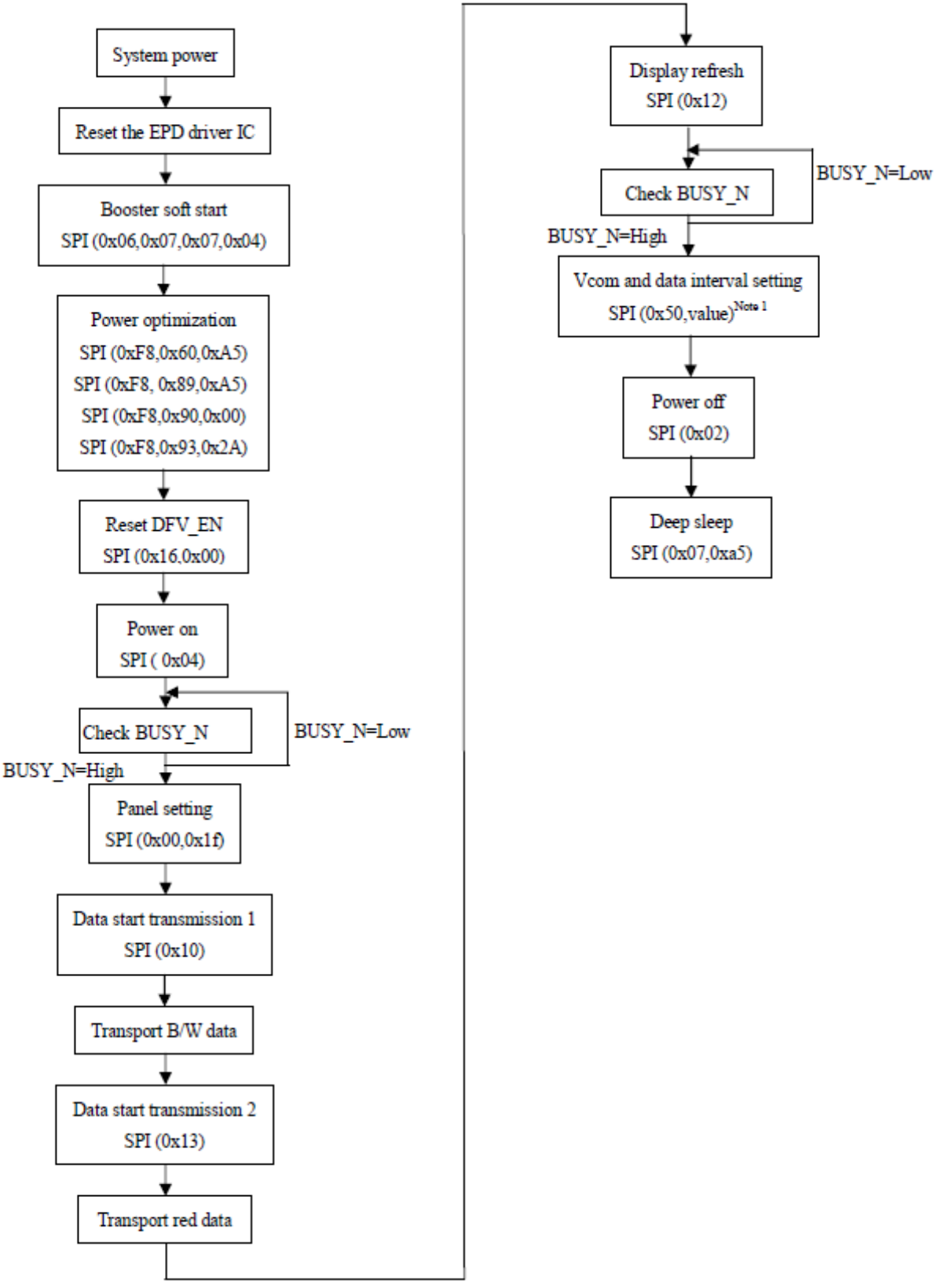
8.2. Reference Program Code

8.2.1. BW Mode & LUT from Register



Note 1: Set border to floating.

8.2.2. BW Mode & LUT from OTP



Note 1: Set border to floating.

9. Optical Characteristics

9.1. Specifications

Measurements are made with the illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Type	Max	Unit	Note
R	Reflectance	White	30	35	-	%	(1)
Gn	2Gray Level	-	-	DS＋(WS-DS) x n (m-1)	-	L*	-
CR	Contrast Ratio	Indoor	8		-	-	-
Panel's Life	-	0°C~50°C	-	1,000,000 times or 5 years	-	-	(2)

WS: White State, DS: Dark State

Gray State from Dark to White: DS, WS

m: 2

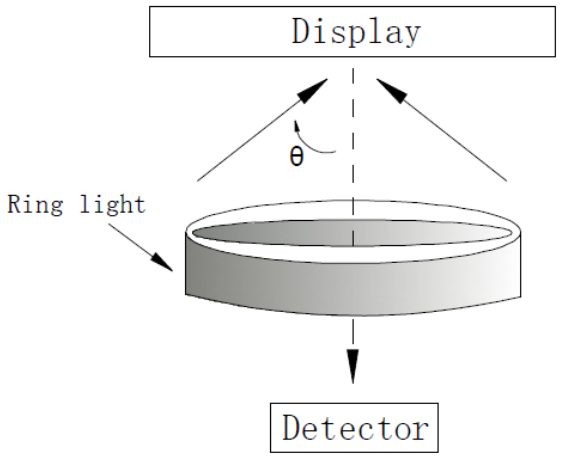
Note (1): Luminance meter: Eye – One Pro Spectrophotometer
Note (2): Panel life is not guaranteed when worked in temperatures below 0 degrees or above 50 degrees. Each update interval time should be at a minimum of 180 seconds.

9.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

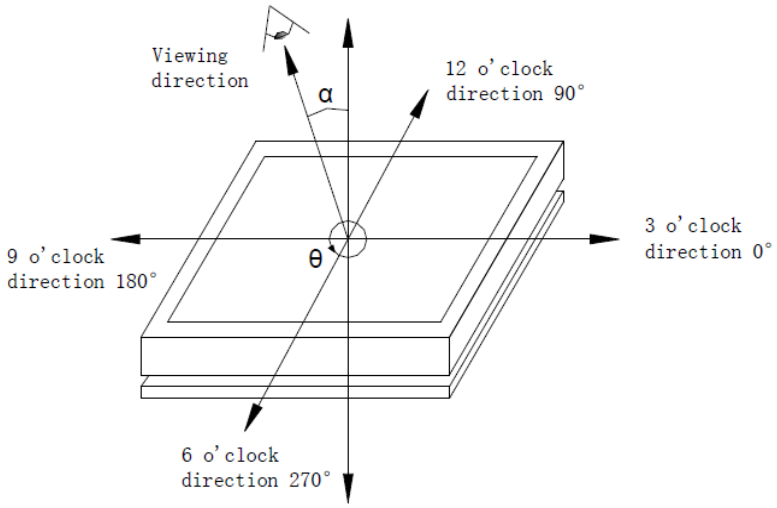


9.3. Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{WHITE\ BOARD}$ x (L_{CENTER} / $L_{WHITE\ BOARD}$)

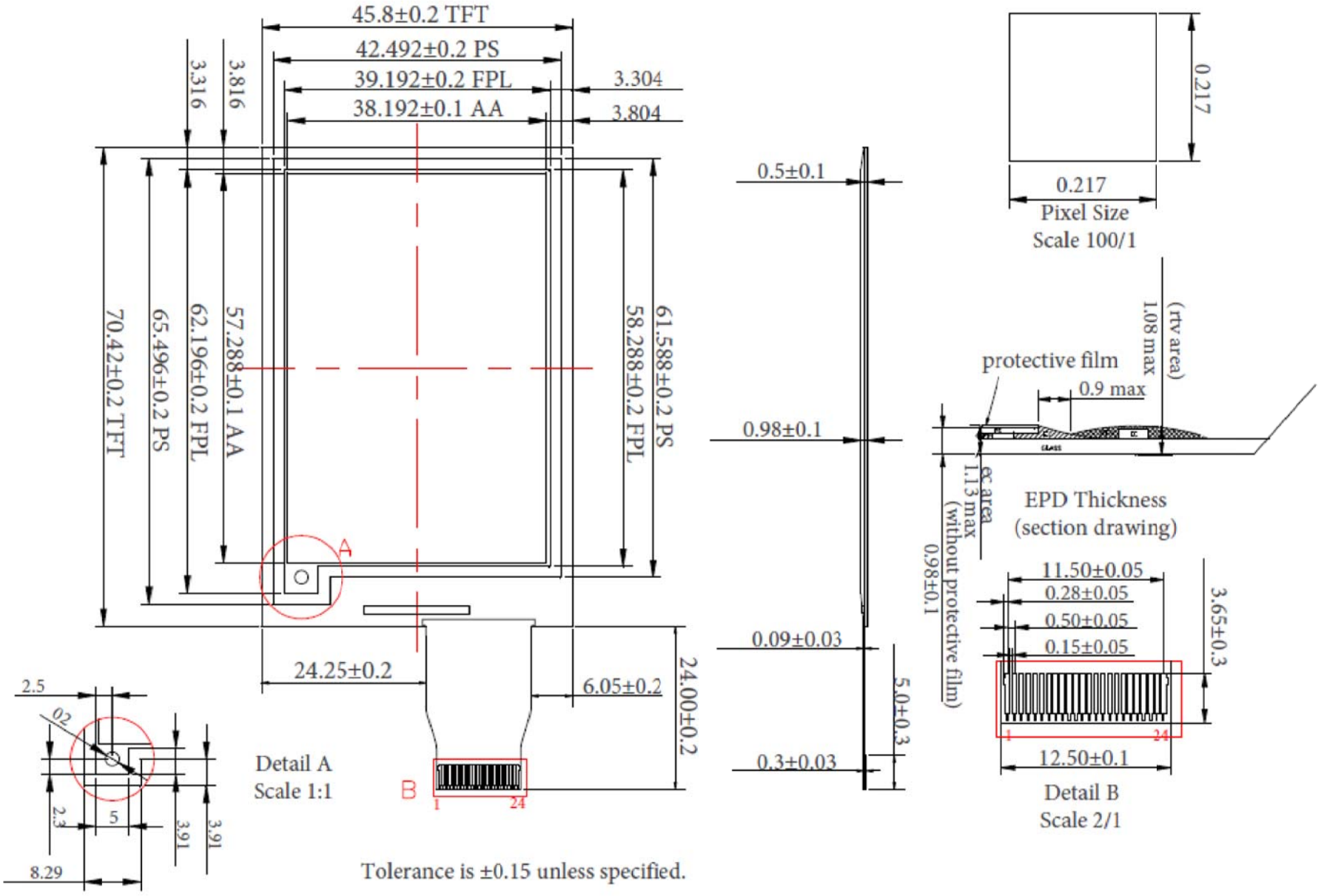
L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{WHITE\ BOARD}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



9.4. Bi-Stability

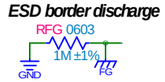
The Bi-Stability standard is as follows:

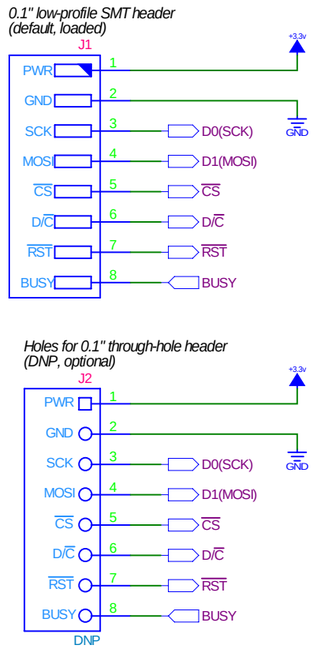
Bi-Stability	Result		
24-Hour Luminance Drift		AVG	MAX
	White state △L*	-	3
	Black state △L*	-	3

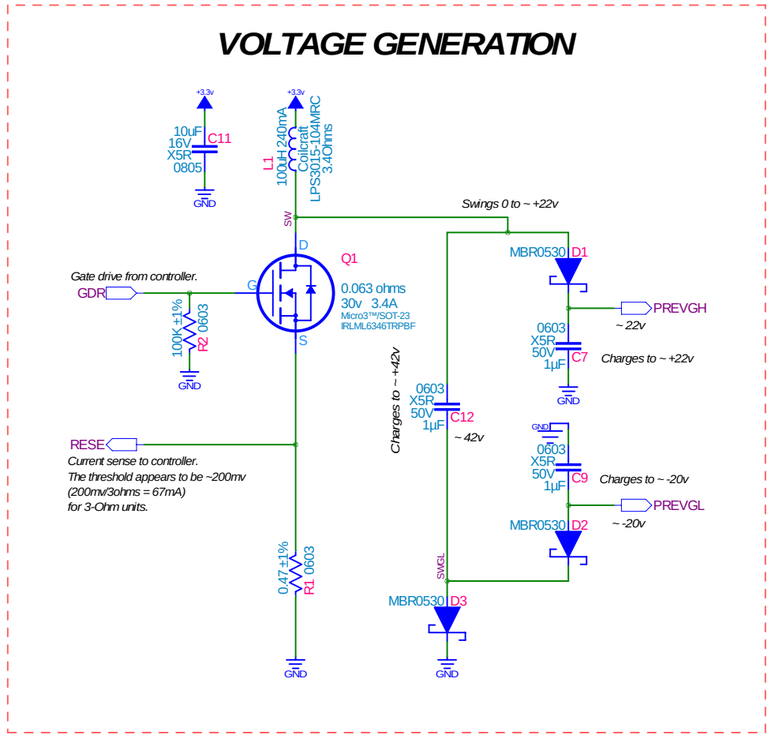


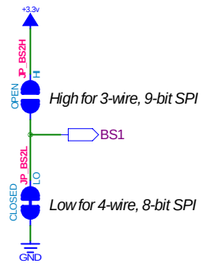
Crystalfontz	PART NUMBER(S) CFAP176264B0-0270	SCALE Not to Scale	
	DRAWING NUMBER CFAP176264B0-0270 master	UNITS Millimeters	DATE 2018-07-03

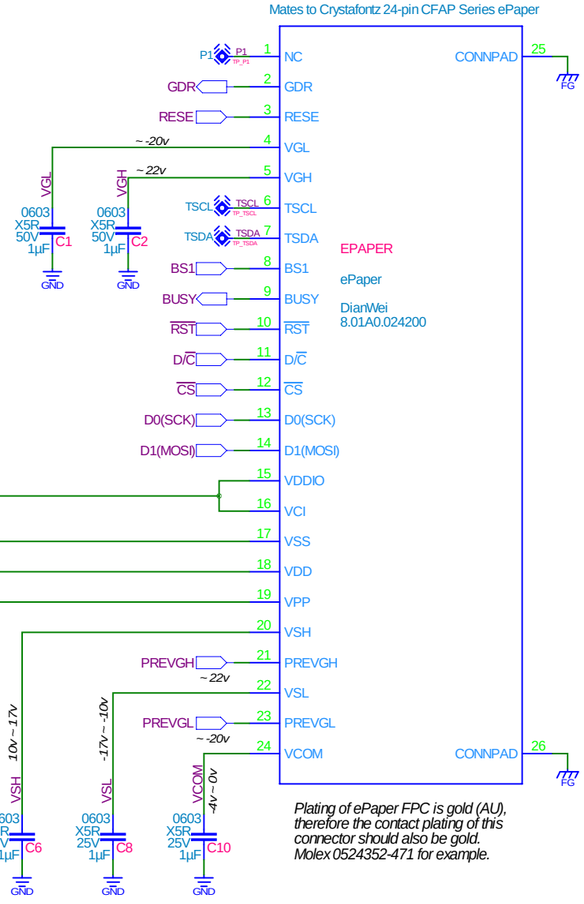
REV	ENGINEER	DATE	REMARKS
0v0	BAC	2018-04-04	Initial Creation
0v1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CN FPC
-	-	-	-
-	-	-	-
-	-	-	-











CFA-10084: ePaper Adapter Board 24-pin (0.47 ohm)

Page 1/1: Schematic

PRODUCT NAME:	PRODUCT REVISION:	PCB NUMBER:	PCB REVISION:
CFA-10084	0v1	PCB-10084	0v1