ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2018-05-29
for
CFAP104212D0-0213

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CONTENTS

1. General Information

Datasheet Revision History
Datasheet Release Date: **2018-05-29** Datasheet for the CFAP104212D0-0213 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

Disclaimer
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2. Description Overview

This ePaper display is a TFT active matrix electrophoretic flexible display with interface and a reference system design. The 2.13" active area contains 212x104 pixels and has 1-bit white/black full display capabilities. An integrated circuit contains a gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

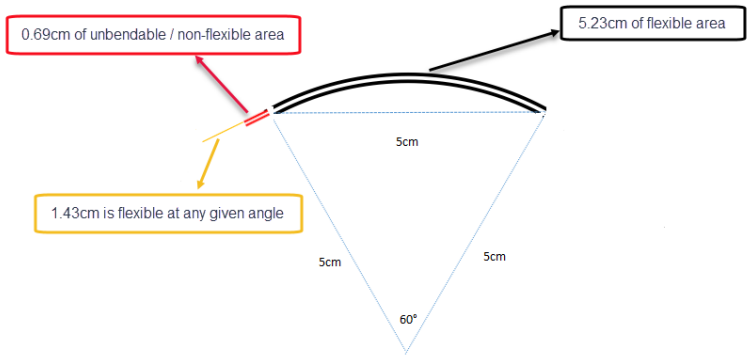
3. Features

- High Contrast
- High Reflectance
- Ultra-Wide Viewing Angle
- Ultra-Low Power Consumption
- Pure Reflective Mode
- Bi-Stable Display
- Commercial Temperature Range
- Landscape or Portrait Mode
- Antiglare Hard-Coated Front-Surface
- Low Current Deep Sleep Mode
- On-Chip Display RAM
- Waveform Stored in On-Chip OTP
- Serial Peripheral Interface Available
- On-Chip Oscillator
- On-Chip Booster and Regulator Control for Generating V_{COM}, Gate and Source Driving Voltage
- I^2C Signal Master Interface to Read External Temperature Sensor
- Available in COG Package IC Thickness 180um

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	inch	-
Display Resolution	212 (H) × 104 (W)	pixel	dpi: 111
Active Area	48.55 (H) × 23.71 (W)	mm	-
Pixel Pitch	0.229 × 0.228	mm	-
Pixel Configuration	Square	-	-
Outline Dimension	59.2 (H) × 29.2 (W) × 0.3 (D)	mm	-
Weight (typical)	0.8	g	-

5. Flexible Specifications



IMPORTANT: DO NOT TWIST. This module is bendable; it is not designed to be twisted.

6. Input/Output Terminals

6.1. Pin Out List

Pin #	Single	Description	Remark
1	NC	No Connection and Do Not Connect with Other NC Pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	VGL	Negative Gate Driving Voltage	
5	VGH	Positive Gate Driving Voltage	
6	TSCL	I^2C Interface to Digital Temperature Sensor Clock Pin	
7	TSDA	I^2C Interface to Digital Temperature Sensor Data Pin	
8	BS1	Bus Selection Pin	Note 6-5
9	BUSY	Busy State Output Pin	Note 6-4
10	RES#	Reset	Note 6-3
11	D/C#	Command / Data Control Pin	Note 6-2
12	CS#	Chip Select Input Pin	Note 6-1
13	D0	Serial Clock Pin (SPI)	
14	D1	Serial Data Pin (SPI)	
15	VDDIO	Power for Interface Logic Pins	
16	VCI	Power Supply Pin for Chip	
17	VSS	Ground	
18	VDD	Core Logic Power Pin	
19	VPP	Power Supply for OTP Programming	
20	VSH	Positive Source Driving Voltage	
21	PREVGH	Positive Supply Pin for VGH and VSH	
22	VSL	Negative Source Driving Voltage	
23	PREVGL	Power Supply Pin for VCOM, VGL, and VSL	
24	VCOM	VCOM Driving Voltage	

Note (6-1): This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note (6-2): This pin (D/C#) is the Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note (6-3): This pin (RES#) is the reset signal input. The reset is active LOW.

Note (6-4): This pin (BUSY) is the Busy state output pin. When busy is LOW, the operation of chip should not be interrupted and no commands should be issued to the module. The driver IC will put Busy pin LOW when the driver IC is working such as

- Outputting Display Waveform; or
- Programming with OTP
- Communicating with Digital Temperature Sensor

Note (6-5): This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “LOW”, 4-line SPI is selected. When it is “HIGH”, 3-line SPI (9 bits SPI) is selected. Please refer to the table below.

Table: Bus Interface Selection

BS1	MPU Interface
L	4-Lines Serial Peripheral Interface (SPI)
H	3-Lines Serial Peripheral Interface (SPI) – 9 bits SPI

7. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0:-: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD, SHL, SHD_N, RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	-	-	-	-	#	#	VDS_EN,VDG_EN	03h
		0	1	-	-	-	-	-	#	#	#	VCOM_HV, VGHL_LV[1:0]	00h
		0	1	-	-	#	#	#	#	#	#	VDH[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDL[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDHR[5:0]	03h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	17h
8	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check Code	A5h
9	Data Start Transmission 1 (DTM1, white/black data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W or OLD Pixel Data (160x296)	10h
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00h
		0	1	..	..	..	..	..	..	..	..	..	..
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00h
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-		00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17h
		1	1	1	0	1	0	0	1	0	1	Check Code	A5h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
13	VCOM LUT (LUTC) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20h
14	W2W LUT (LUTWW) (37-byte command, structure of bytes 2~7 repeated 6 times)	0	0	0	0	1	0	0	0	0	1		21h
15	B2W LUT (LUTBW / LUTR) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0		22h
16	W2B LUT (LUTWB / LUTW) (37-byte command, structure of bytes 2~7 repeated 6 times)	0	0	0	0	1	0	0	0	1	1		23h
17	B2B LUT (LUTBB / LUTB) (37-byte command, structure of bytes 2~7 repeated 6 times)	0	0	0	0	1	0	0	1	0	0		24h
18	LUT Option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2Ah
		0	1	-	-	#	#	#	#	#	#	STATE_XON[5:0]	00h
		0	1	-	-	#	#	-	#	#	#	EXS[1:0],DMS[2:0]	00h
19	PLL Control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
20	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3]/TS[7:0]	00h
		1	1	#	#	#	-	-	-	-	-	D[2:0]/-	00h
21	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	#	#	#	#	TSE,TO[3:0]	00h
22	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
23	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
24	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44h
		1	1	-	-	-	-	-	-	-	-	PSTA	00h
25	V_{COM} and Data Interval Setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[1:0],DDX[1:0],CDI[3:0]	D7h
26	Low Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	-	-	-	-	-	-	-	#	LPD	01h
27	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
28	Resolution Setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00h
		0	1	-	-	-	-	-	-	-	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
29	Gate/Source Start Setting (GSST)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00h
		0	1	-	-	-	-	-	-	-	#	VST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
30	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFh
31	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	#	#	#	#	#	#	#	PTL_FLAG, I^2C_ERR_I^2C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13h
32	Auto Measure V_{COM}	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0], XON, AMVS, AMV, AMVE	10h
33	Read V_{COM} Value (VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	-	#	#	#	#	#	#	VV[5:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
34	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00h
35	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90h
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00h
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07h
		0	1	-	-	-	-	-	-	-	#	VRST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	-	-	-	-	-	-	-	#	VRED[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	-	-	-	-	-	-	-	#	PT_SCAN	01h
36	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91h
37	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
38	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0h
39	Active Program (APG)	0	0	1	0	1	0	0	0	0	1		A1h
40	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2h
		1	1	-	-	-	-	-	-	-	-	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	..	..	..	..	..	..	..	..	..	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
41	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0h
		0	1	-	-	-	-	-	-	#	#	TSFIX_W[3:0],SD_W[3:0]	00h
42	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3h
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0],SD_W[3:0]	00h
43	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4h
		0	1	-	-	-	-	-	-	#	#	LVD_SEL[1:0]	03h
44	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5h
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00h

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N

RES [1:0]: Display Resolution setting (source x gate)

00b: 96x230 (Default) Active source channels: S0~S95. Active gate channels: G0~G229.

01b: 96x252 Active source channels: S0~S95. Active gate channels: G0~G251.

10b: 128x296 Active source channels: S0~S127. Active gate channels: G0~G295.

11b: 160x296 Active source channels: S0~S159. Active gate channels: G0~G295.

REG: LUT selection

0: LUT from OTP. (Default)

1: LUT from register

KW/R: Black / White / Red

0: Pixel with B/W/Red, KWR mode. (Default)

1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to last line: Gn-1 → Gn-2 → Gn-3 →…→ G0

1: Scan up. (Default) First line to last line: G0 → G1 → G2 →…→ Gn-1

SHL: Source Shift direction

0: Shift left. First data to last data: Sn-1 → Sn-2 → Sn-3 →…→ S0

1: Shift right. (Default) First data to last data: S0 → S1 → S2 →…→ Sn-1

SHD_N: Booster Switch

0: Booster OFF

1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) Power Setting (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]	
	0	1	-	-	VDH[5:0]					
	0	1	-	-	VDL[5:0]					
	0	1	-	-	VDHR[5:0]					

VDS_EN: Source power selection

0: External source power from VDH/VDL/VDHR pins.

1: Internal DC/DC function for generating VDH/VDL/VDHR. (Default)

VDG_EN: Gate power selection

0: External gate power from VGH/VGL pins

1: Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_HV: VCOM Voltage Level

0: VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC (Default)

1: VCOML=VGH, VCOML=VGL

VGHL_LV [1:0]: VGH / VGL Voltage Level selection

VGHL_LV	VGHL Voltage Level
00(Default)	VGH=20V, VGL= -20V
01	VGH=19V, VGL= -19V
10	VGH=18V, VGL= -18V
11	VGH=17V, VGL= -17V

VDH [5:0]: Internal VDH power selection for B/W pixel. (Default value: 100110b)

VDH	VDH_V	VDH	VDH_V
000000	6.4V	…	…
000001	6.6V	100110	14.0V
000010	6.8V	100111	14.2V
000011	7.0V	101000	14.4V
000100	7.2V	101001	14.6V
000101	7.4V	101010	14.8V
000110	7.6V	101011	15.0V
000111	7.8V	(others)	15.0V

VDL [5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V
000000	-6.4V	…	…
000001	-6.6V	100110	-14.0V
000010	-6.8V	100111	-14.2V
000011	-7.0V	101000	-14.4V
000100	-7.2V	101001	-14.6V
000101	-7.4V	101010	-14.8V
000110	-7.6V	101011	-15.0V
000111	-7.8V	(others)	-15.0V

VDHR [5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR	VDHR _V	VDHR	VDHR _V
000000	2.4V	…	…
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

(3) Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will power off following the Power Off Sequence. This command will turn off the booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD is turned OFF or Deep Sleep mode. Source/Gate/Border/VCOM will be released to floating.

(4) Power OFF Sequence Setting (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF [1:0]: Source to gate Power OFF interval time.

00b:1 frame (Default) 01b:2 frames 10b: 3 frames 11b:4 frames

(5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON following the Power ON Sequence. This command will turn on the booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling the booster. When all voltages are ready, the BUSY signal will return to high.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power ON measure	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap that will be cleared by the next POF.

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting Data Transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA [7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA [5:3]: Driving strength of phase A.

000b: strength 1 001b: strength 2 **010b: strength 3**
011b: strength4 100b: strength 5 101b: strength 6
110b: strength 7 111b: strength 8 (strongest)

BTPHA [2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB [7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB [5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3**
011b: strength4 100b: strength 5 101b: strength 6
110b: strength 7 111b: strength 8 (strongest)

BTPHB [2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC [5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3**
011b: strength4 100b: strength 5 101b: strength 6
110b: strength 7 111b: strength 8 (strongest)

BTPHC [2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting Data Transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and writes the data to SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) Data Stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping Data Transmission	0	0	0	0	0	1	0	0	0	1
	1	1	Data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10H) or “Data Stop” (R11H) commands and when data_flag=1, the refreshing of the panel starts and the BUSY signal will become “0”.

(11) Display Refresh Command (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh the display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY signal will become “0” and the refreshing of the panel starts.
The waiting interval from BUSY falling to the first FLG command must be larger than 200us.

(12) Auto Sequence (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Auto Sequence	0	0	0	0	0	1	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

This command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of the host’s control procedure. The sequence contains several operations including PON, DRF, POF, DSLP.

AUTO (0x17) + Code (0xA5) = (PON ⟶ DRF ⟶ POF)

AUTO (0x17) + Code (0xA7) = (PON ⟶ DRF ⟶ POF ⟶ DSLP)

(13) VCOM LUT (LUTC) (R20H)

This command builds the Look-up Table for VCOM.

(14) W2W LUT (LUTWW) (R21H)

This command builds the Look-up Table for White-to-White.

(15) B2W LUT (LUTBW/LUTR) (R22H)

This command builds the Look-up Table for Black-to-White.

(16) W2B LUT (LUTWB/LUTW) (R23H)

This command builds the Look-up Table for White-to-Black.

(17) B2B LUT (LUTBB / LUTB) (R24H)

This command builds the Look-up Table for Black-to-Black.

(18) LUT Option (LUTOPT) (R24H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT Option	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	STATE_XON[5:0]					
	0	1	-	-	EXS[2:0]		-	DMS[2:0]		

This command sets XON and the 2 options of KWR mode's LUT.

STATE_XON[5:0]:

All Gate ON (each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2, etc.)

00 0000b: no All-Gate-ON
00 0001b: State-1 All-Gate-ON
00 0011b: State-1 and State-2 All-Gate-ON

DMS[2:0]: Dummy state position. The option is only available when KW/R=0.
EXS[1:0]: Extra state number. This option is only available when KW/R=0.

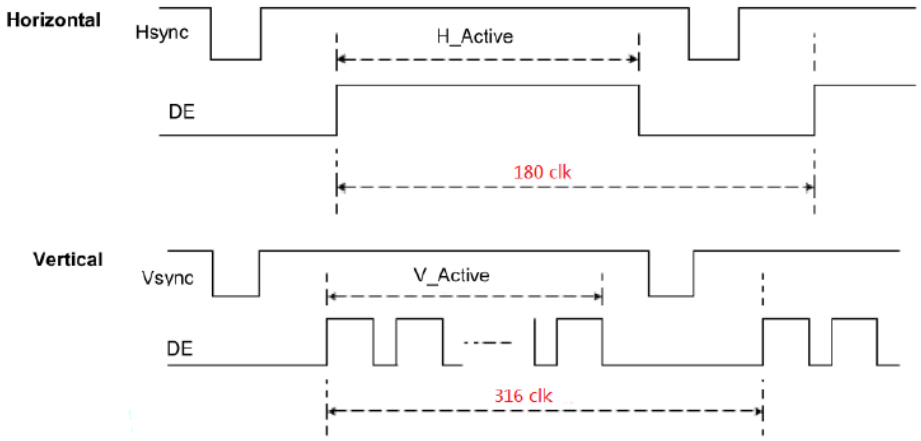
(19) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

The command controls the PLL clock frequency.

The PLL structure must support the following frame rates:

M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate
1	1	29 Hz	3	1	86 Hz	5	1	150 Hz	7	1	200 Hz
	2	14 Hz		2	43 Hz		2	72 Hz		2	100 Hz
	3	10 Hz		3	29 Hz		3	48 Hz		3	67 Hz
	4	7 Hz		4	21 Hz		4	36 Hz		4	50 Hz (Default)
	5	6 Hz		5	17 Hz		5	29 Hz		5	40 Hz
	6	5 Hz		6	14 Hz		6	24 Hz		6	33 Hz
	7	4 Hz		7	12 Hz		7	20 Hz		7	29 Hz
2	1	57 Hz	4	1	114 Hz	6	1	171 Hz			
	2	29 Hz		2	57 Hz		2	86 Hz			
	3	19 Hz		3	38 Hz		3	57 Hz			
	4	14 Hz		4	29 Hz		4	43 Hz			
	5	11 Hz		5	23 Hz		5	34 Hz			
	6	10 Hz		6	19 Hz		6	29 Hz			
	7	8 Hz		7	16 Hz		7	24 Hz			



(20) Temperature Sensor Calibration (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command enables the internal and external temperature sensor and reads the results.

TS [7:0]: When TSE (R41h) is set to 0, this command reads the internal temperature sensor value.

D [10:0]: When TSE (R41h) is set to 1, this command reads the external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)	TS[7:0]/D[10:3]	Temperature (°C)	TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

(21) Temperature Sensor Enable (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature Sensor/Offset	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	-	-	TO[3:0]			

This command selects the Internal and External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (Default)

1: Disable: using external sensor.

TO[3:0] Temperature offset.

TO[3:0]	Calculation	TO[3:0]	Calculation
0000 b	0	1000	-8
0001	1	1001	-7
0010	2	1010	-6
…	…	…	…
0110	6	1110	-2
0111	7	1111	-1

(22) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	0	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR[7:6]: I^2C Write Byte Number

00b: 1 byte (head byte only)
01b: 2 bytes (head byte + pointer)
10b: 3 bytes (head byte + pointer + 1st parameter)
11b: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)
WATTR[2:0]: Pointer setting
WMSB[7:0]: MSByte of write-data to external temperature sensor.
WLSB[7:0]: LSByte of write-data to external temperature sensor.

(23) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor.
RLSB[7:0]: LSByte read data from external temperature sensor.

(24) Panel Glass Check (PBC) (R44H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0
	1	1	-	-	-	-	-	-	-	PSTA

This command is used to enable panel check and to disable after reading the results.
PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(25) VCOM and Data Interval Setting (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 H_{SYNC}).

VBD[1:0]: Border data selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1 (Default)	00	LUTB
	01	LUTR		01	LUTW
	10	LUTW		10	LUTR
	11	LUTB		11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1 (Default)	00	Floating
	01	LUTBW (1 → 0)		01	LUTWB (1 → 0)
	10	LUTWB (0 → 1)		10	LUTBW (0 → 1)
	11	Floating		11	Floating

DDX[1:0]: Display polarity.

DDX[1] for RED data, DDX[0] for BW data om the KWR mode.

DDX[0] for KW mode.

KWR mode (KW/R=0)

DDX[1:0]	Data {Red, B/W}	LUT	DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW	10	00	LUTR
	01	LUTB		01	LUTR
	10	LUTR		10	LUTW
	11	LUTR		11	LUTB
01 (Default)	00	LUTB	11	00	LUTR
	01	LUTW		01	LUTR
	10	LUTR		10	LUTB
	11	LUTR		11	LUTW

B/W mode (BWR=1)

DDX[0]	Data {New, Old}	LUT	DDX[0]	Data {New, Old}	LUT
00	00	LUTWW (0 → 0)	1 (Default)	00	LUTBB (0 → 0)
	01	LUTBW (1 → 0)		01	LUTWB (0 → 1)
	10	LUTWB (0 → 1)		10	LUTBW (1 → 0)
	11	LUTBB (1 → 1)		11	LUTWW (1 → 1)

CDI[3:0]: VCOM and Data Interval

CDI[3:0]	VCOM and Data Interval	CDI[3:0]	VCOM and Data Interval
0000 b	17 H_{SYNC}	0110	11
0001	16	0111	10 (Default)
0010	15	…	…
0011	14	1101	4
0100	13	1110	3
0101	12	1111	2

(26) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the condition of the battery.

LPD: Interval Low Power Detection Flag

0: Low Power Input (VDD<2.5V, selected by LVD_SEL[1:0] in command LVSEL)

1: Normal Status (Default)

(27) TCON Setting (TCON) (R60H)

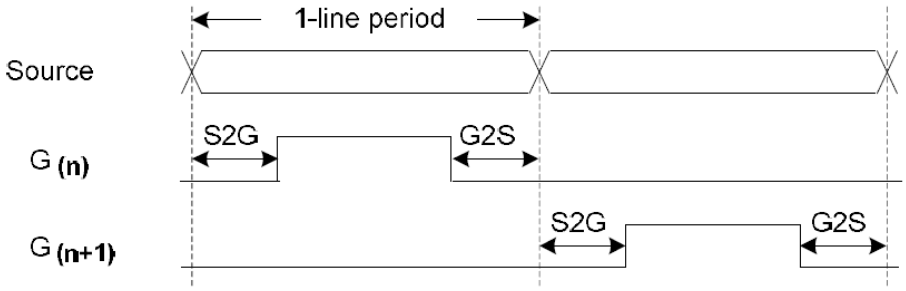
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-Overlap Period	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines the non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap Period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000 b	4		…	…
0001	8		1011	48
0010	12 (Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



(28) Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:3]					0	0	0
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	1	VRES[7:0]							

This command defines the alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution
VRES[8:0]: Vertical Display Resolution

Active Channel Calculation:
GD: First active gate = G0 (Fixed); LAST active gate = VRES[8:0]-1
SD: First active source = S0 (Fixed); LAST active source = HRES[7:3]*8-1

(29) Gate/Source Start Setting (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1
	0	1	HST[7:3]					0	0	0
	0	1	-	-	-	-	-	-	-	VST[8]
	0	1	VST[7:0]							

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)
VST[8:0]: Vertical Display Start Position (Gate)

Gate: First active gate = G32 (because HST[7:3]=4), Last active gate = G271
Source: First active source = S32 (because VST[8:0]=32), Last active source = S159

(30) Revision (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	LUT_REV							

The LUT_REV is read from OTP address = 0x0001/0x801.

(31) Get Status (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	PTL_flag	I²C_ERR	I²C_BUSY	data_flag	PON	POF	BUSY

This command reads the IC status.

PTL_FLAG: Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSY: I²C master BUSY status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY: Driver busy status (low active)

(32) Auto Measure VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically Measure VCOM	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s 01b: 5s (Default)
10b: 8s 11b:10s

XON: All Gate ON of AMV

0: Gate normally scans during Auto Measure VCOM period. (Default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source Output of AMV

0: Source output 0V during Auto Measure VCOM period. (Default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog Signal

0: Get VCOM value with the VV command (R81h) (Default)

1: Get VCOM value in analog signal. (external analog to digital converter)

AMVE: Auto Measure VCOM Enable (Disable)

0: No effect

1: Trigger Auto VCOM sensing

(33) VCOM Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically Measure VCOM	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the VCOM value.

VV[5:0]: VCOM Value Output

VV[5:0]	VCOM Value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(34) VCOM-DC Setting (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

This command set VCOM_DC value.

VDCS[5:0]: VCOM-DC Setting

VDCS[5:0]	VCOM Value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V
Others	-3.00V

(35) Partial Window (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Window	0	0	1	0	0	1	0	0	0	0
	0	1	HRST[7:3]					0	0	0
	0	1	HRED[7:3]					1	1	1
	0	1	-	-	-	-	-	-	-	VRST[8]
	0	1	VRST[7:0]							
	0	1	-	-	-	-	-	-	-	VRED[8]
	0	1	VRED[7:0]							
	0	1	-	-	-	-	-	-	-	PT_SCAN

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~13h)

HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~127h)

VRED[8:0]: Vertical end line. (value 000h~127h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (Default)

(36) Partial In (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

This command makes the display enter partial mode.

(37) Partial Out (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Out	0	0	1	0	0	1	0	0	1	0

This command makes the display enter partial mode.

(38) Program Mode (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0

After this command is issued, the chip will enter the program mode.

After the programming procedure is completed, a hardware reset is necessary to leave program mode.

(39) Active Program Mode (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

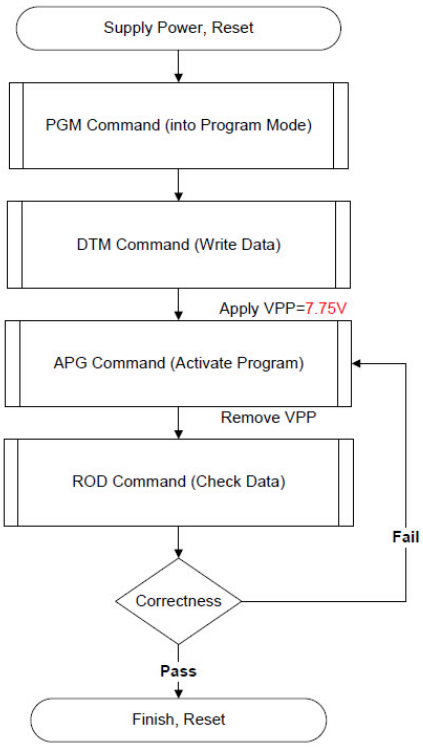
After this command is transmitted, the programming state machine will be activated. The BUSY flag will fall to 0 until the programming is completed.

(40) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP Data for Check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	-							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

This command is used for reading the content of OTP for checking the data of programming.

The value of (n) is dependent on the amount of programmed data, the max address = 0xFFF.



The Sequence of Programming OTP

(41) Cascade Setting (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Cascade Option	0	0	1	1	1	0	0	0	1	1
	0	1	-	-	-	-	-	-	TSFIX	CCEN

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (Default)

1: Output clock at CL pin for slave chip.

TSFIX: Let's the value of the slave's temperature be the same as the master's.

0: Temperature value is defined by internal temperature sensor/external LM75. (Default)

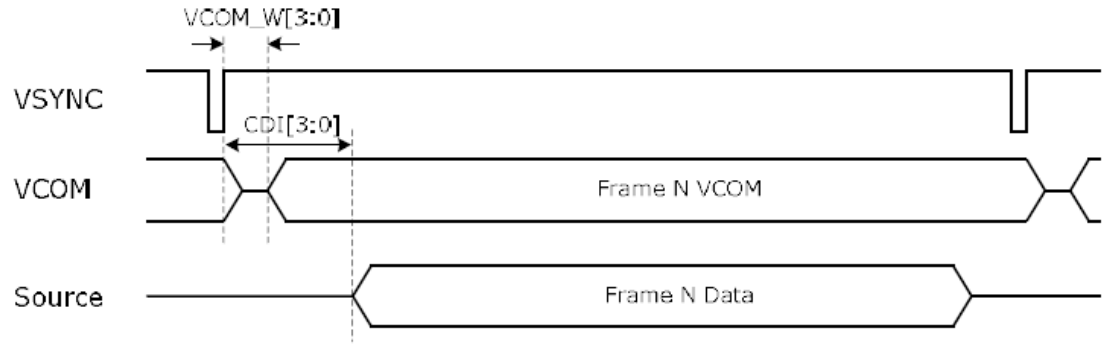
1: Temperature value is defined by TS_SET[7:0] registers.

(42) Power Saving (PWS) (RE3H)

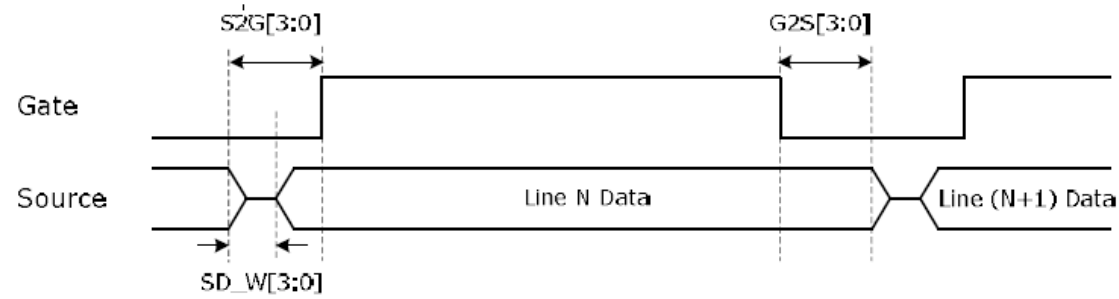
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1
	0	1	VCOM_W[3:0]				SD_W[3:0]			

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



(43) LVD Voltage Select (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]	

LVD_SEL[1:0]: Low Power Voltage Selection.

LVD_SEL[1:0]	LVD Value
00	<2.2V
01	<2.3V
10	<2.4V
11	<2.5V (Default)

(44) Force Temperature (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1
	0	1	TS_SET[7:0]							

This command is used for cascade to fix the temperature value of master and slave chip.

8. Electrical Characteristics

8.1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to V_{CI} +2.4	V
Operating Temp. range	T_{OPR}	0 to +50	°C
Storage Temp. range	T_{STG}	-25 to +70	°C
Humidity Range	RH	40~70	%
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

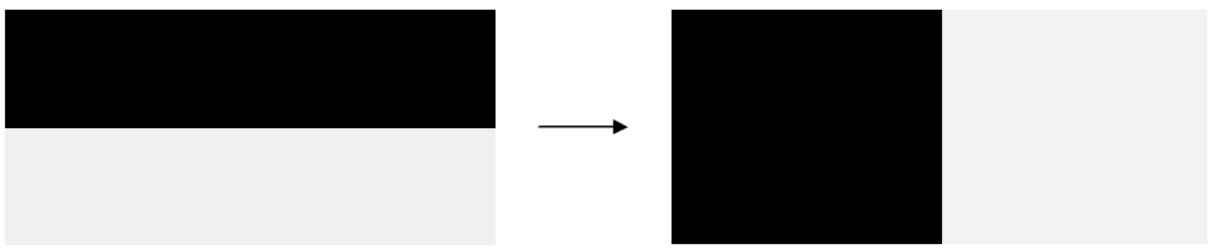
8.2. Panel DC Characteristics

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	V_{CI}	-	2.3	3.3	3.6	V
High Level Input Voltage	V_{IH}	Digital Input Pins	0.7V_{CI}	-	V_{CI}	V
Low Level Input Voltage	V_{IL}	Digital Input Pins	0	-	0.3V_{CI}	V
High Level Output Voltage	V_{OH}	Digital Input Pins, IOH= 400uA	V_{CI}-0.4	-	-	V
Low Level Output Voltage	V_{OL}	Digital Input Pins, IOL= -400uA	0	-	0.4	V
Image Update Current	I_{UPDATE}	-	-	8	10	mA
Standby Panel Current	$I_{STANDBY}$	-	-	-	5	uA
Power Panel (Update)	P_{UPDATE}	-	-	26.4	40	mW
Standby Power Panel	P_{STBY}	-	-	-	0.0165	mW
Operating Temperature	-	-	0	-	50	°C
Storage Temperature	-	-	-25	-	70	°C
Deep sleep mode current	I_{VCI}	DC/DC Off No Clock No Input Load Ram Data Not Retained	-	2	5	uA
Sleep mode current	I_{VCI}	DC/DC Off No Clock No Input Load Ram Data Retained	-	35	50	uA

The typical power consumption is measured with the following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern, shown below.

Note: The standby power is the consumed power when the panel controller is in standby mode. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz. V_{COM} is recommended to be set in the range of assigned value ±0.1V.



8.3. Panel AC Characteristics

8.3.1. Oscillator Frequency

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator Frequency	Fosc	V_{CI}=2.3 to 3.6V	-	1.625	-	MHz

8.3.2. MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus Interface	D1	D0	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 7-1: MCU Interface Assignment Under Different Bus Interface Mode

Note: L is connected to V_{SS}. H is connected to V_{CI}.

8.3.3. MCU Serial Interface (4-Wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write Data	L	H	↑

Table 7-2: Control Pins of 4-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, …D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

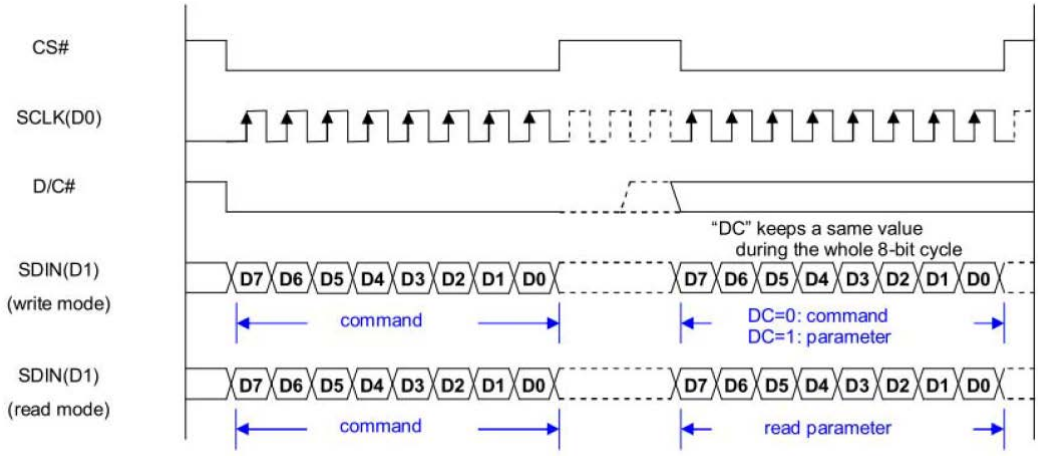


Figure 7-1: Write Procedure in 4-Wire Serial Peripheral Interface Mode

8.3.4. MCU Serial Interface (3-Wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits that will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write Data	L	Tie LOW	↑

Table 7-3: Control Pins of 3-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

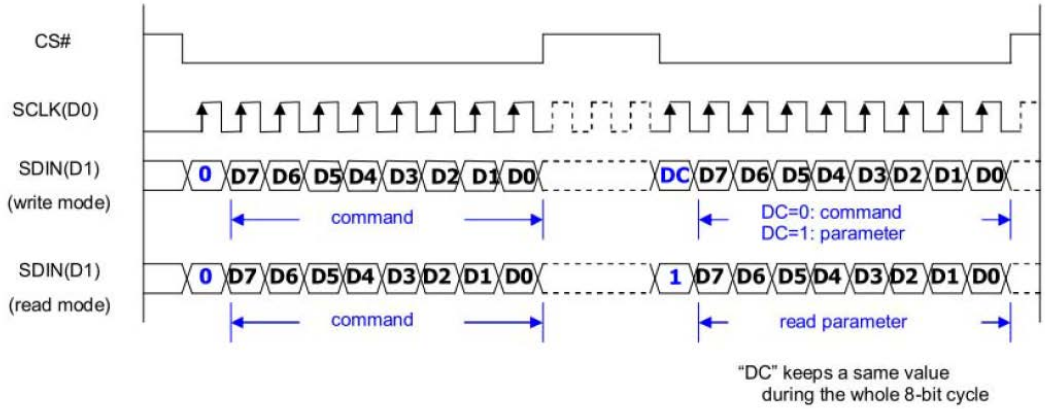
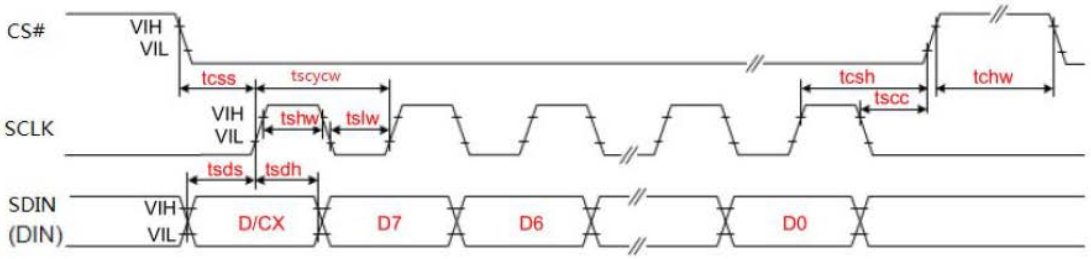
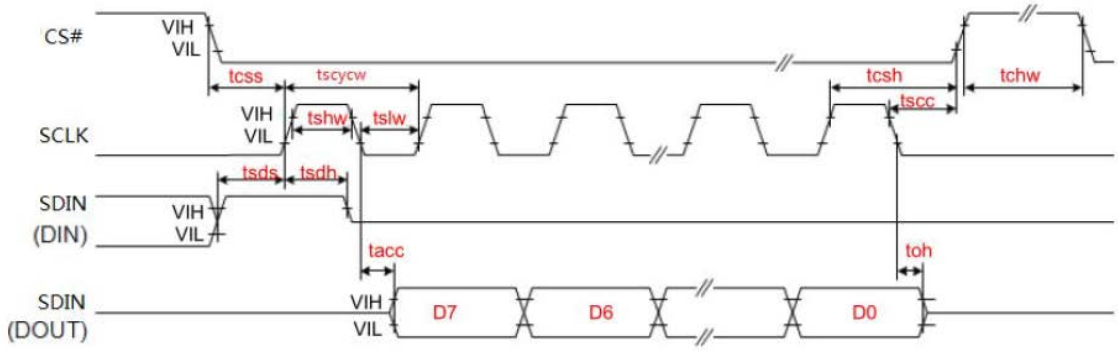


Figure 7-2: Write Procedure in 3-Wire Serial Peripheral Interface Mode

8.3.5. Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCLK	Serial Clock Cycle (Write)	100	-	-	ns
tshw		SCL “H” Pulse Width (Write)	35	-	-	ns
tslw		SCL “L” Pulse Width (Write)	35	-	-	ns
tscycr		Serial Clock Cycle (Read)	150	-	-	ns
tshr		SCL “H” Pulse Width (Read)	60	-	-	ns
tslr		SCL “L” Pulse Width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data Setup Time	30	-	-	ns
tsdh		Data Hold Time	30	-	-	ns
tacc		Access Time	-	-	10	ns
toh		Output Disable Time	15	-	-	ns

8.4. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel Power Consumption During Update	-	25°C	26.4	40	mW	-
Power Consumption in Standby Mode	-	25°C	-	0.0165	mW	-

8.5. Reference Circuit

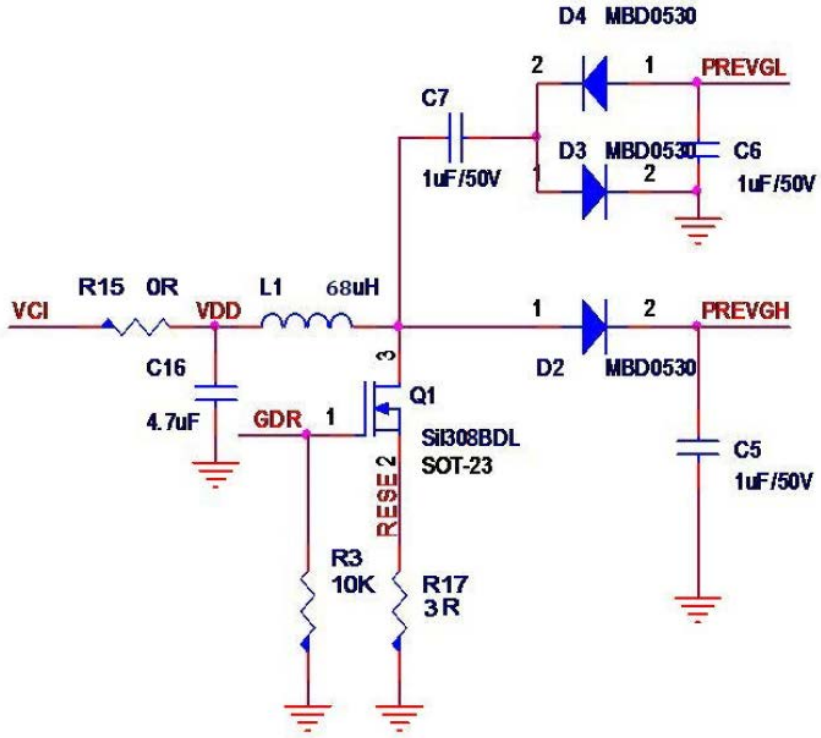


Figure 7-5 (1)

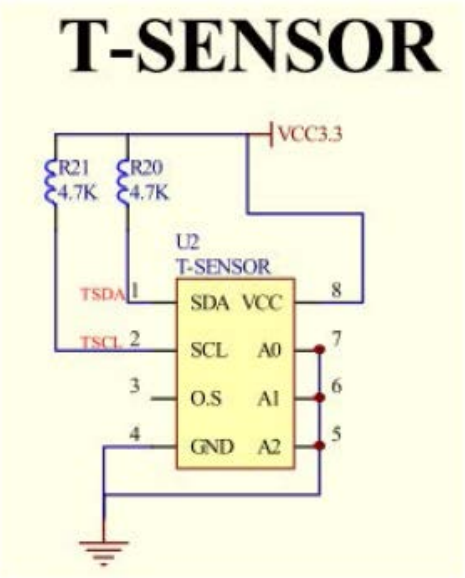
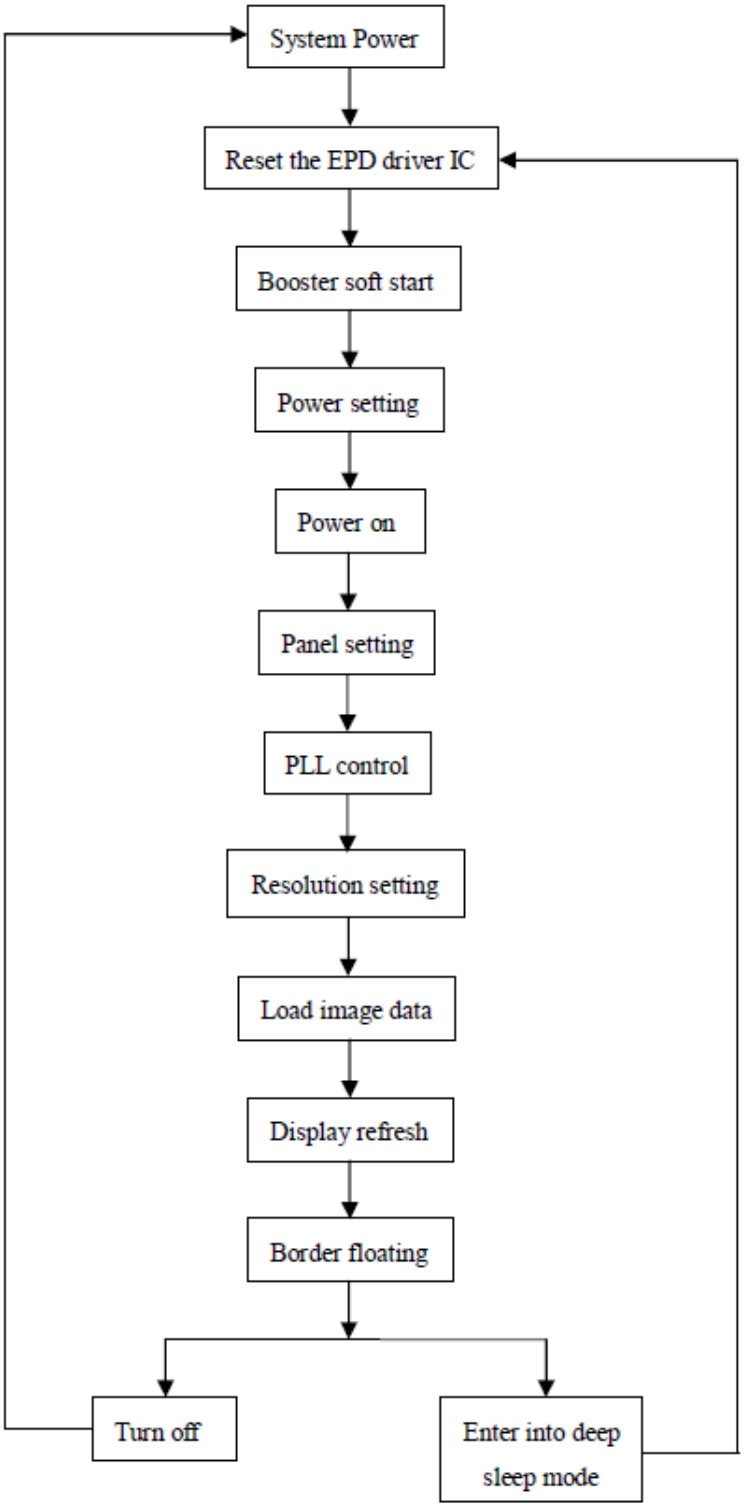


Figure 7-5 (2)

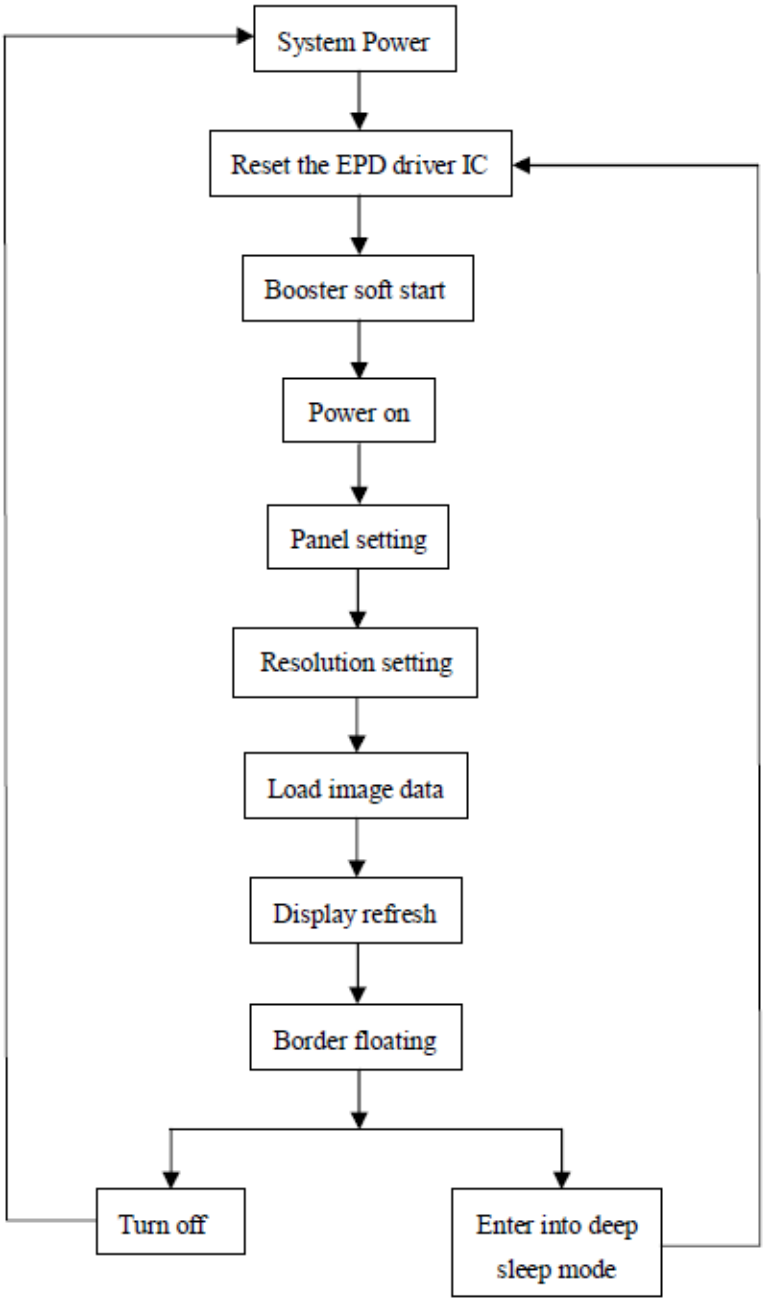
9. Typical Operating Sequence

9.1. Normal Operation Flow

9.1.1. BW Mode & LUT from Register

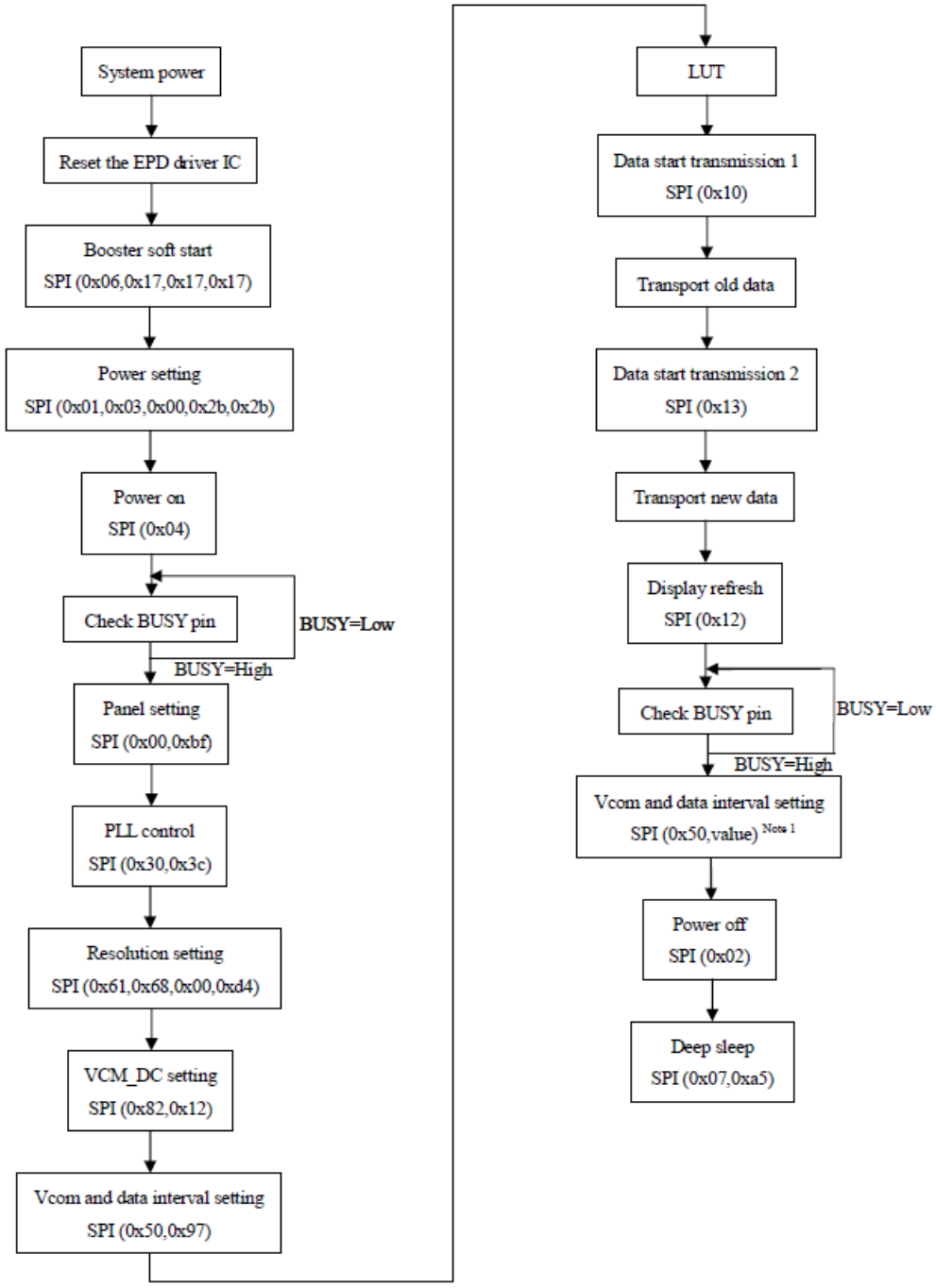


9.1.2. BW Mode & LUT from OTP



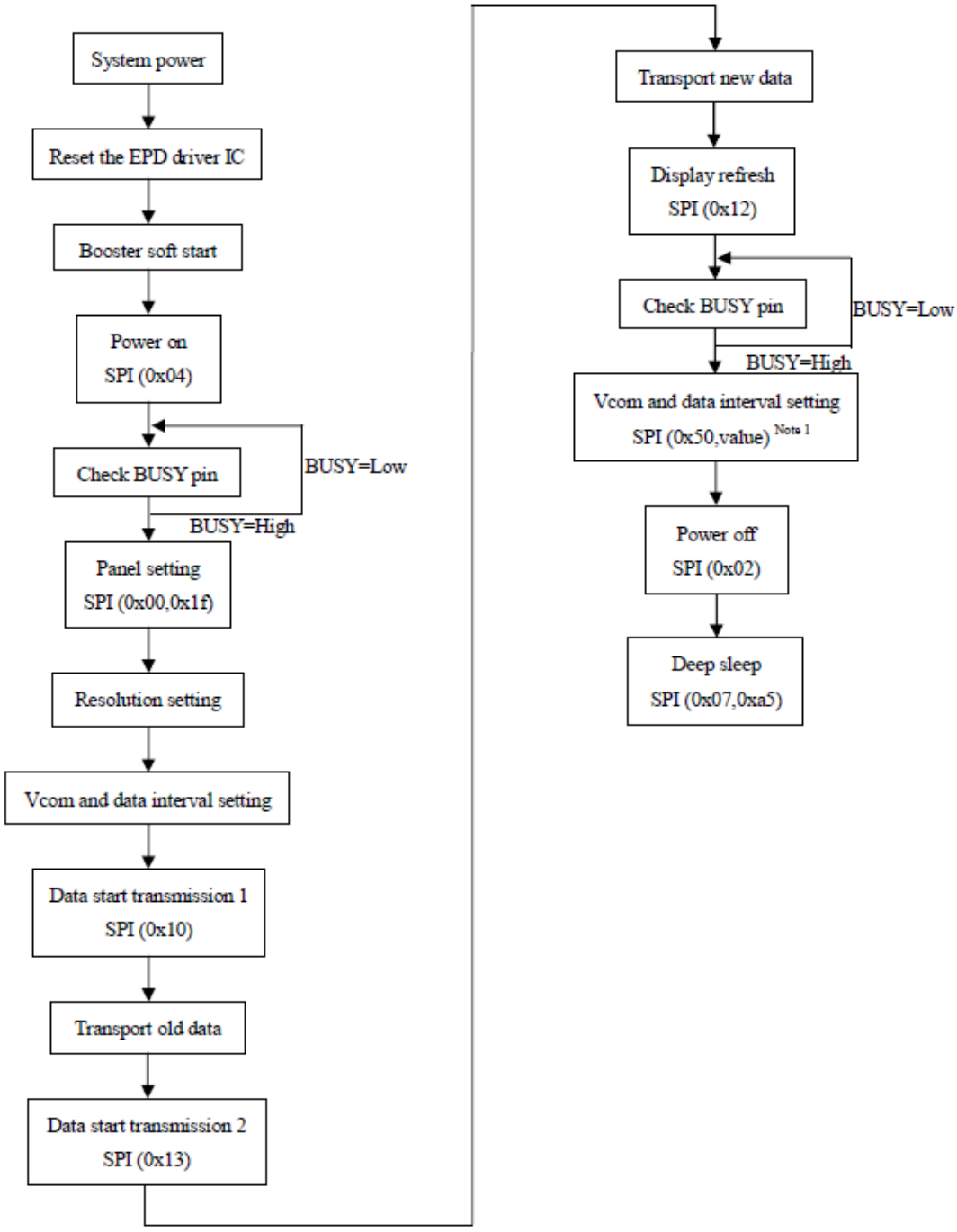
9.2. Reference Program Code

9.2.1. BW Mode & LUT from Register



Note 1: Set border to floating.

9.2.2. BW Mode & LUT from OTP



Note 1: Set border to floating.

10. Optical Characteristics

10.1. Specifications

Measurements are made with the illumination under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Type	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 10-1
Gn	2Gray Level	-	-	DS+(WS-DS) X n(m-1)	-	L*	-
CR	Contrast Ratio	Indoor	8		-	-	-
Panel's Life	-	0°C~50°C	-	1,000,000 times or 5 years	-	-	Note 10-2

WS: White State, DS: Dark State

Gray State from Dark to White: DS, WS

m: 2

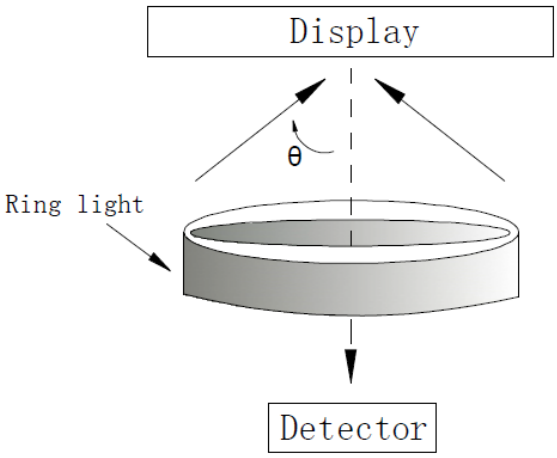
Note (10-1): Luminance meter: Eye – One Pro Spectrophotometer
Note (10-2): Panel life is not guaranteed when worked in temperatures below 0 degrees or above 50 degrees. Each update interval time should be at a minimum of 180 seconds.

10.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

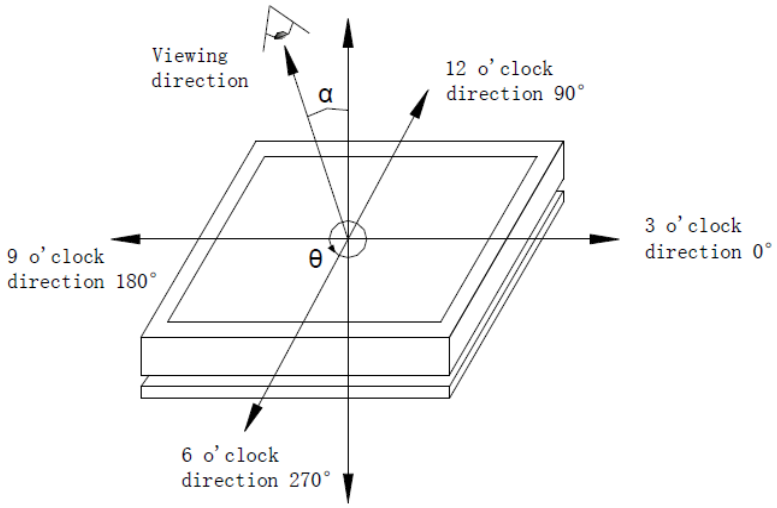


10.3. Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{CENTER} / $L_{WHITE\ BOARD}$)

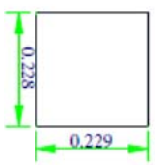
L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{WHITE\ BOARD}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



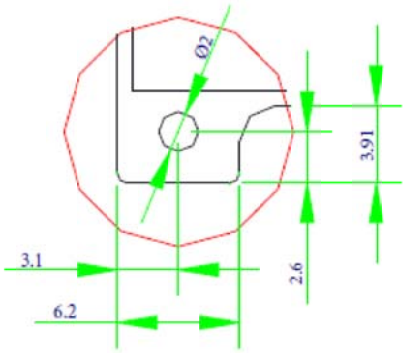
10.4. Bi-Stability

The Bi-Stability standard is as follows:

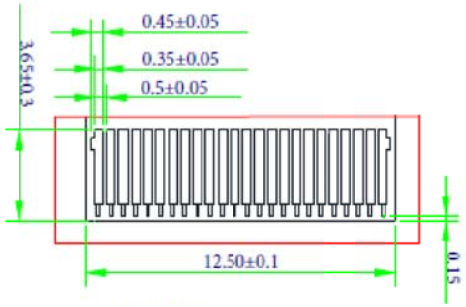
Bi-Stability	Result			
			AVG	MAX
24-Hour Luminance Drift	White state	△L*	-	3
	Black state	△L*	-	3



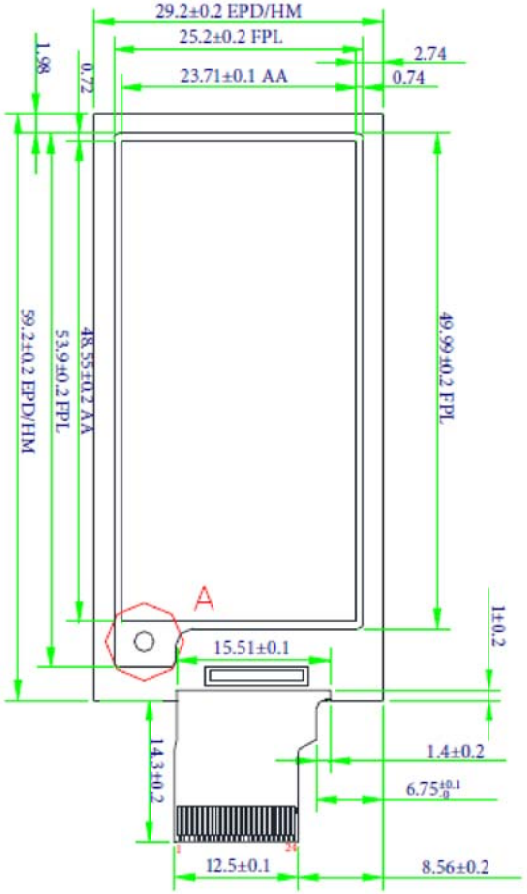
Pixel Size
Scale 50/1

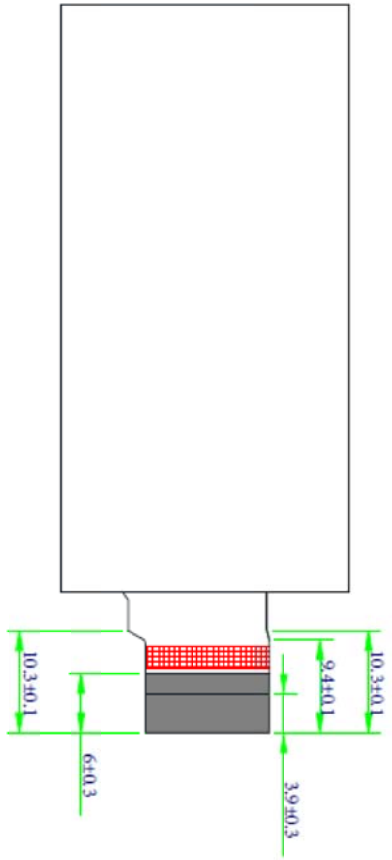


Detail A
Scale 1/1



Detail B
Scale 1/2.5



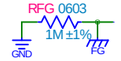


Tolerances is ±0.15mm unless specified.

Crystalfontz	PART NUMBER(S) CFAP104212D0-0213	SCALE Not to Scale	COPYRIGHT © 2018 BY CRYSTALFONTZ AMERICA, INC. WWW.CRYSTALFONTZ.COM
	DRAWING NUMBER CFAP104212D0-0213 master	UNITS Millimeters	DATE 2018-05-29

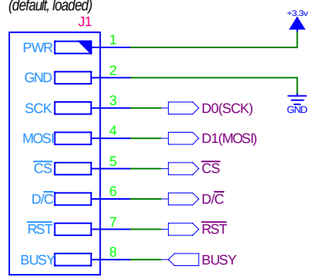
REV	ENGINEER	DATE	REMARKS
0v0	BAC	2018-04-04	Initial Creation
0v1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CN FPC
-	-	-	-
-	-	-	-
-	-	-	-

ESD border discharge

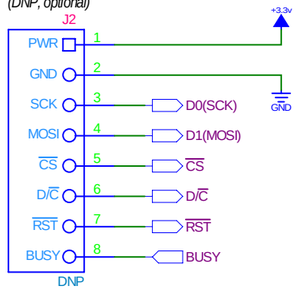


Scope Ground

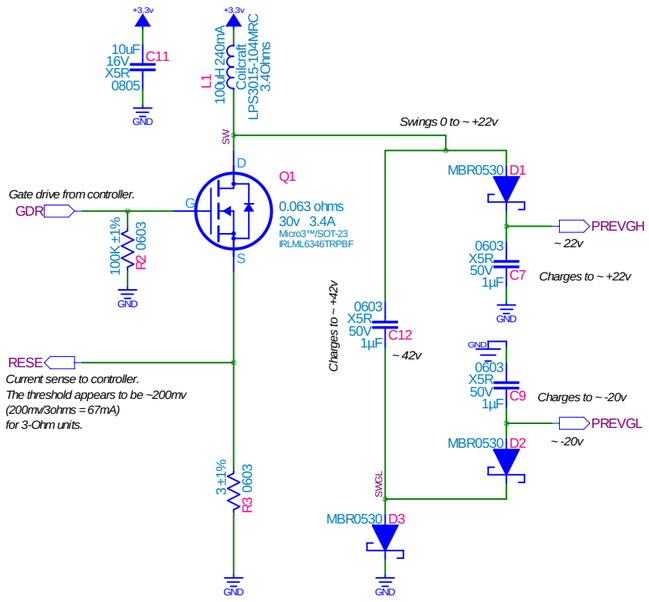
0.1" low-profile SMT header (default, loaded)

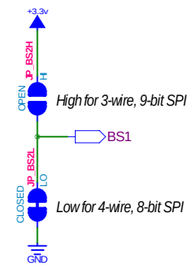


Holes for 0.1" through-hole header (DNP, optional)

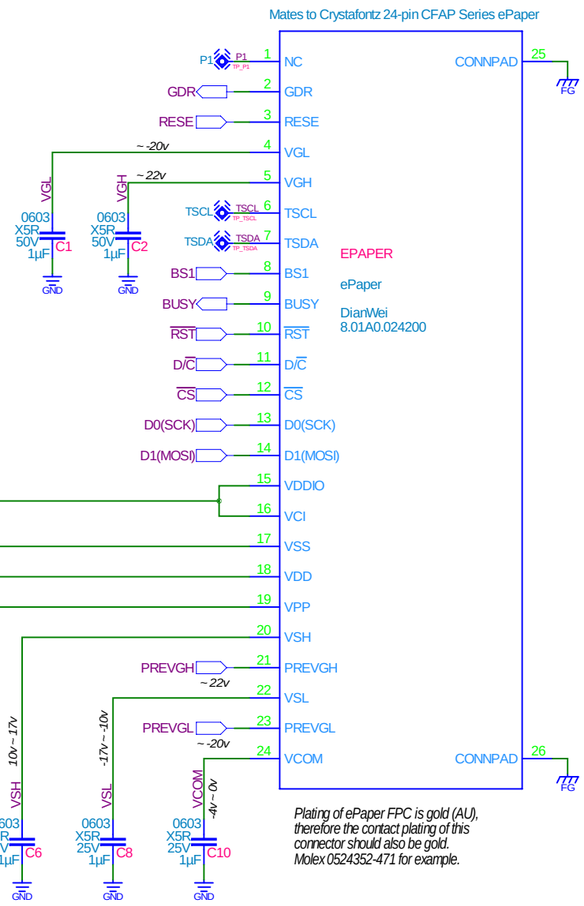


VOLTAGE GENERATION





Mates to Crystafontz 24-pin CFAP Series ePaper



CFA-10084: ePaper Adapter Board 24-pin (3-ohm)

Page 1 / 1 : Schematic

PRODUCT NAME:	PRODUCT REVISION:	PCB NUMBER:	PCB REVISION:
CFA-10084	0v1	PCB-10084	0v1