Crystalfontz America, Incorporated

GRAPHIC OLED MODULE SPECIFICATIONS

Crystalfontz Model Number	**CFAL12832C-B-B1**
Hardware Version	**Version A, November 2009**
Data Sheet Version	**Version 1.0, November 2009**
Product Pages	www.crystalfontz.com/product/CFAL12832CBB1.html

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REVISION HISTORY

HARDWARE	
2009/11/17	Current hardware version: **vA** New module.

DATA SHEET	
2009/11/17	Current Data Sheet version: **v1.0** New Data Sheet.

CONTENTS

LIST OF FIGURES

MAIN FEATURES

DEMONSTRATION AND EVALUATION PLATFORM

This module is available installed on a Crystalfontz CFA-10009 Demonstration PCB. The DMO-L12832CBB1 kit has everything you need to easily demonstrate and experiment with the module.The kit can also be used as a reference for your designs. The *CFA10009 User Guide* was added at the end of this Data Sheet.

COMPARISON TO LCD (LIQUID CRYSTAL DISPLAY) MODULE

The CFAL12832C-B-B1 is a monochrome 128 x 32 dot matrix Organic Light-Emitting Diode (OLED) display module. The small size and ultrathin form factor makes it possible to use this OLED module in applications where it would be difficult or impossible to fit a traditional monochrome LCD module. The module's small size makes it possible to use the CFAL12832C-B-B1 in space constrained applications such as a status display on a disk drive or server blade. Because of the low power requirements, the module is suitable in battery powered portable devices such as remote controls and scientific meters (for example, temperature, sound, and gas detection).

Compared to most LCD modules, this OLED module has a quicker response time and an extremely wide viewing angle. At the low end of an STN LCD's temperature range, a module's contrast will typically be poor and the response time will be very slow. Unlike an STN LCD module, contrast does not diminish and response time is good at the lower end of an OLED module's operating temperature range, allowing it to operate in cold environments without a heater.

FEATURES

- ❑ 128 x 32 module consists of an OLED LCD panel, a COG (Chip on Glass) driver IC, and an FPC (Flexible Printed Circuit) tail.
- ❑ Module Dimensions:
  - Active Area is 0.91" diagonal, 22.38 (W) x 5.58 (H) millimeters (0.88" (W) x 0.22" (H)).
  - Overall module dimension with FPC *unfolded* is 26.90 (W) x 23.50 (H) x 2.10 maximum (D) mm (1.06" (W) x 0.93" (H) x 0.083" maximum (D)).
  - Overall module dimension with FPC *folded* is 26.90 (W) x 15.26 (H) x 2.10 maximum (D) mm (1.06" (W) x 0.60" (H) x 0.083" maximum (D)).
- ❑ Requires only a single source 3v for both power supply and logic.
- ❑ 8-bit parallel (8080 or 6800) interface or SPI interface.
- ❑ Built-in Sino Wealth SH1101A or compatible controller.
- ❑ Emissive monochrome display. Display blue pixels on dark area or dark pixels on blue area (if operating with display pixels reversed/inverted).
- ❑ Extremely wide viewing angle is >160°.
- ❑ Wide temperature range for operation is -20°C to +70°C.
- ❑ RoHS compliant.

MODULE CLASSIFICATION INFORMATION

CFA ❶ L ❷ 128 ❸ 32 ❹ C ❺ - B ❻ - B1 ❼

❶	Brand	Crystalfontz America, Inc.
❷	Display Type	L – OLED
❸	Number of Pixels (Width)	128 pixels
❹	Number of Pixels (Height)	32 pixels
❺	Model Identifier	C
❻	Display Color	B – Blue
❼	Special Codes	B1 – Manufacturer's codes

ORDERING INFORMATION

PART NUMBER	COLOR
CFAL12832C-B-B1	blue 
Additional module in this series:	
CFAL12832C-W-B1	white 

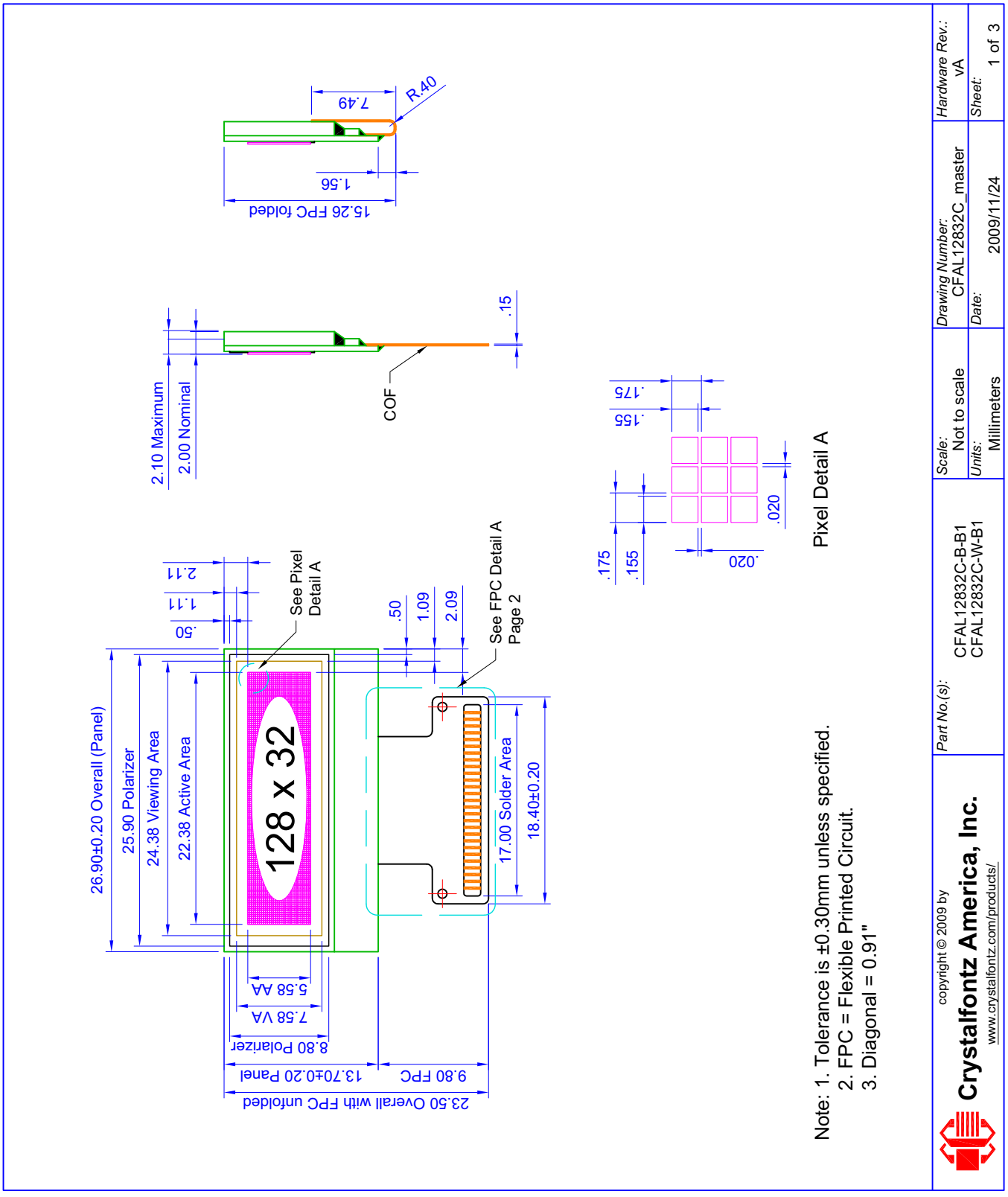
MECHANICAL SPECIFICATIONS

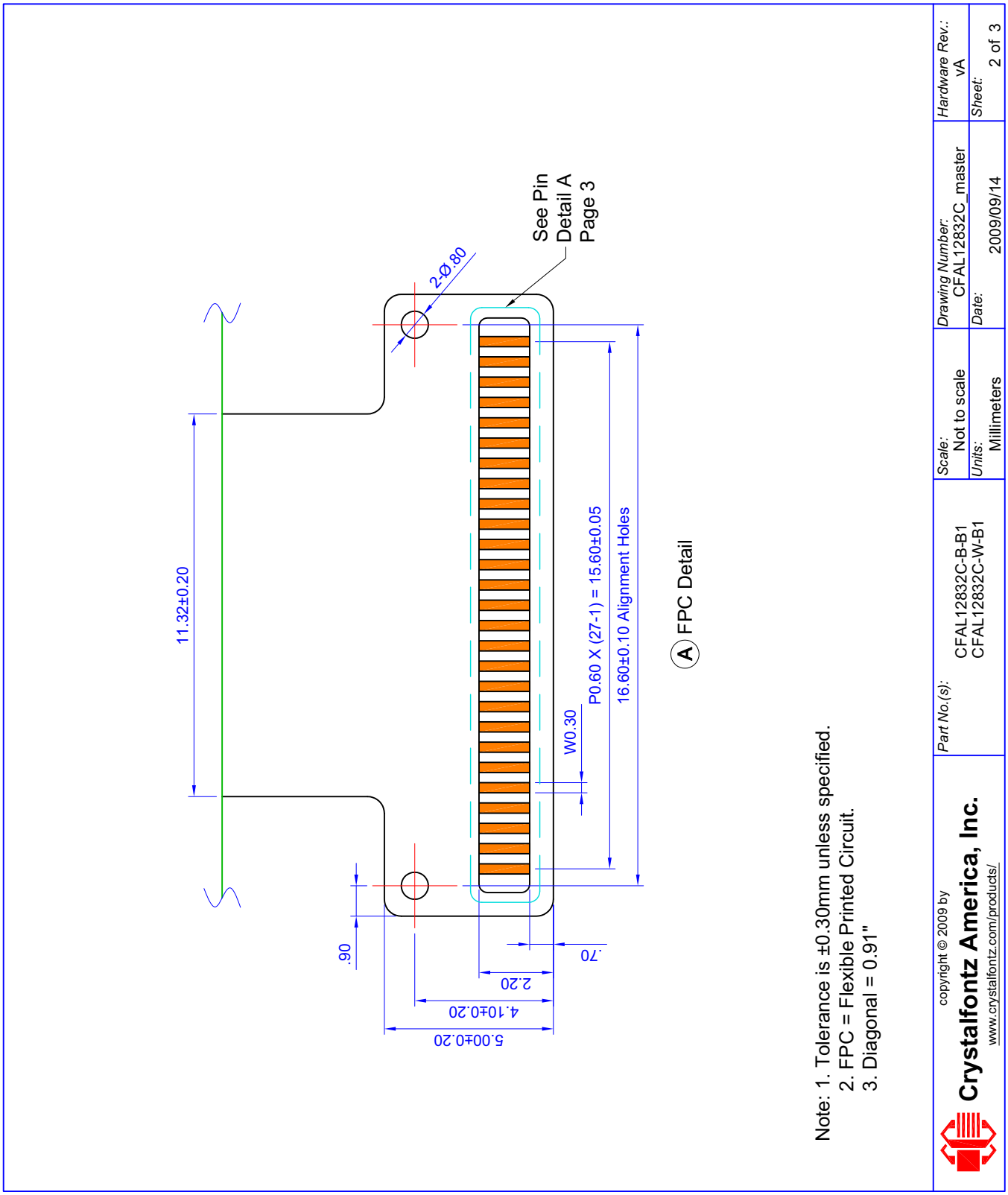
PHYSICAL CHARACTERISTICS

ITEM	SIZE
Number of Pixels	128 x 32 pixels = 4,096 pixels
Pixel Size	0.155 (W) x 0.155 (H) mm
Pixel Pitch	0.175 (W) x 0.175 (H) mm
Active Area	
Active Area Diagonal	Inches: 0.91"
Active Area Width and Height	Millimeters: 22.38 (W) x 5.58 (H) mm Inches: 0.88" (W) x 0.22" (H)
Viewing Area Width and Height	Millimeters: 24.38 (W) x 7.58 (H) mm Inches: 0.96" (W) x 0.30" (H)
Module Outline Dimensions	
Width	Millimeters: 26.90 mm Inches: 1.06"
Overall Height with FPC unfolded	Millimeters: 23.50 mm Inches: 0.93"
Overall Height with FPC folded	Millimeters: 15.26 mm Inches: 0.60"
Module Depth	Maximum: Millimeters: 2.10 mm Inches: 0.083" Nominal: Millimeters: 2.00 mm Inches: 0.079"
Module Connector Pitch	0.6 mm
FPC Bend Radius	>R.40
Aperture Rate*	76%
Weight	1.17± 10% grams (typical)
**Aperture rate is defined by dividing an effective display area with unit pixel area.*	

MODULE OUTLINE DRAWINGS

Figure 1. Module Outline Drawings (next 3 pages)




See Pin Detail A Page 3
2-Ø.80
11.32±0.20
W0.30
P0.60 X (27-1) = 15.60±0.05
16.60±0.10 Alignment Holes
.90
.70
2.20
4.10±0.20
5.00±0.20
A FPC Detail
Note: 1. Tolerance is ±0.30mm unless specified.
2. FPC = Flexible Printed Circuit.
3. Diagonal = 0.91"
Hardware Rev.: vA
Drawing Number: CFAL12832C_master
Scale: Not to scale
Date: 2009/09/14
Units: Millimeters
Sheet: 2 of 3
Part No.(s): CFAL12832C-B-B1 CFAL12832C-W-B1
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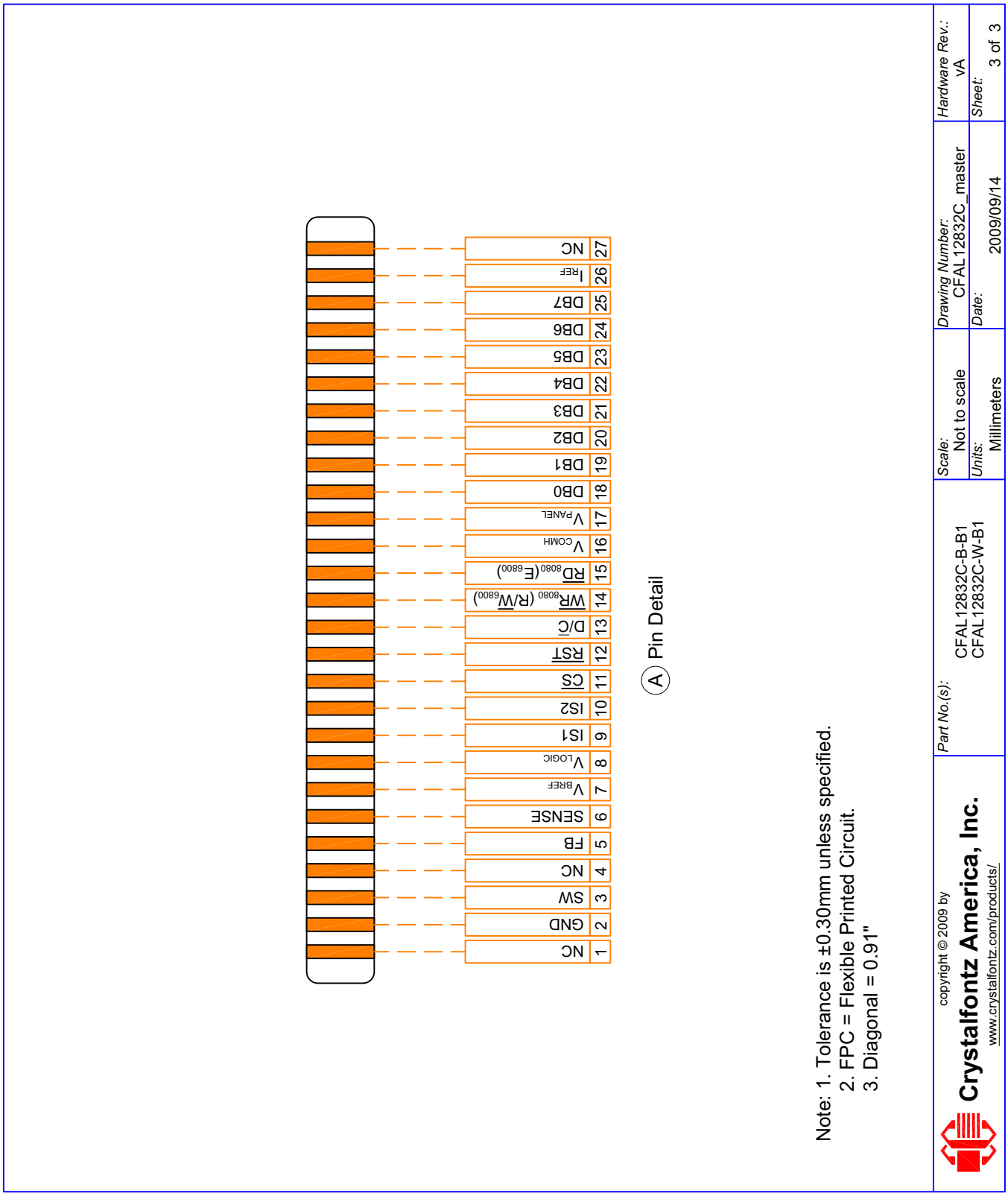
1 NC
2 GND
3 SW
4 NC
5 FB
6 SENSE
7 VBREF
8 VLOGIC
9 IS1
10 IS2
11 CS
12 RST
13 D/C
14 WR8080 (R/W6800)
15 RD8080 (E6800)
16 VCOMH
17 VPANEL
18 DB0
19 DB1
20 DB2
21 DB3
22 DB4
23 DB5
24 DB6
25 DB7
26 IREF
27 NC
A Pin Detail
Note: 1. Tolerance is ±0.30mm unless specified.
2. FPC = Flexible Printed Circuit.
3. Diagonal = 0.91"
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Crystalfontz America, Inc.
www.crystalfontz.com/products/
Part No.(s):
CFAL12832C-B-B1
CFAL12832C-W-B1
Scale: Not to scale
Units: Millimeters
Drawing Number: CFAL12832C_master
Date: 2009/09/14
Hardware Rev.: vA
Sheet: 3 of 3

ELECTRICAL SPECIFICATIONS

SYSTEM BLOCK DIAGRAM

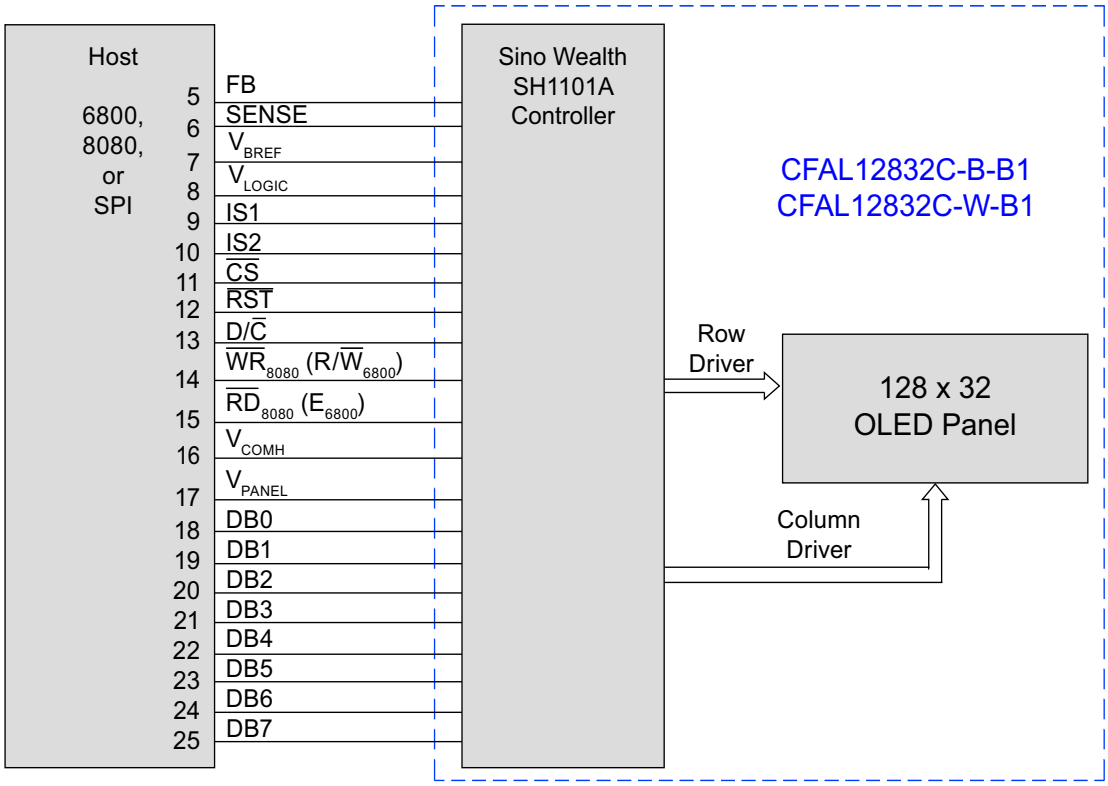


Figure 2. System Block Diagram

CIRCUIT EXAMPLE – EXTERNALLY SUPPLIED V_{PANEL}

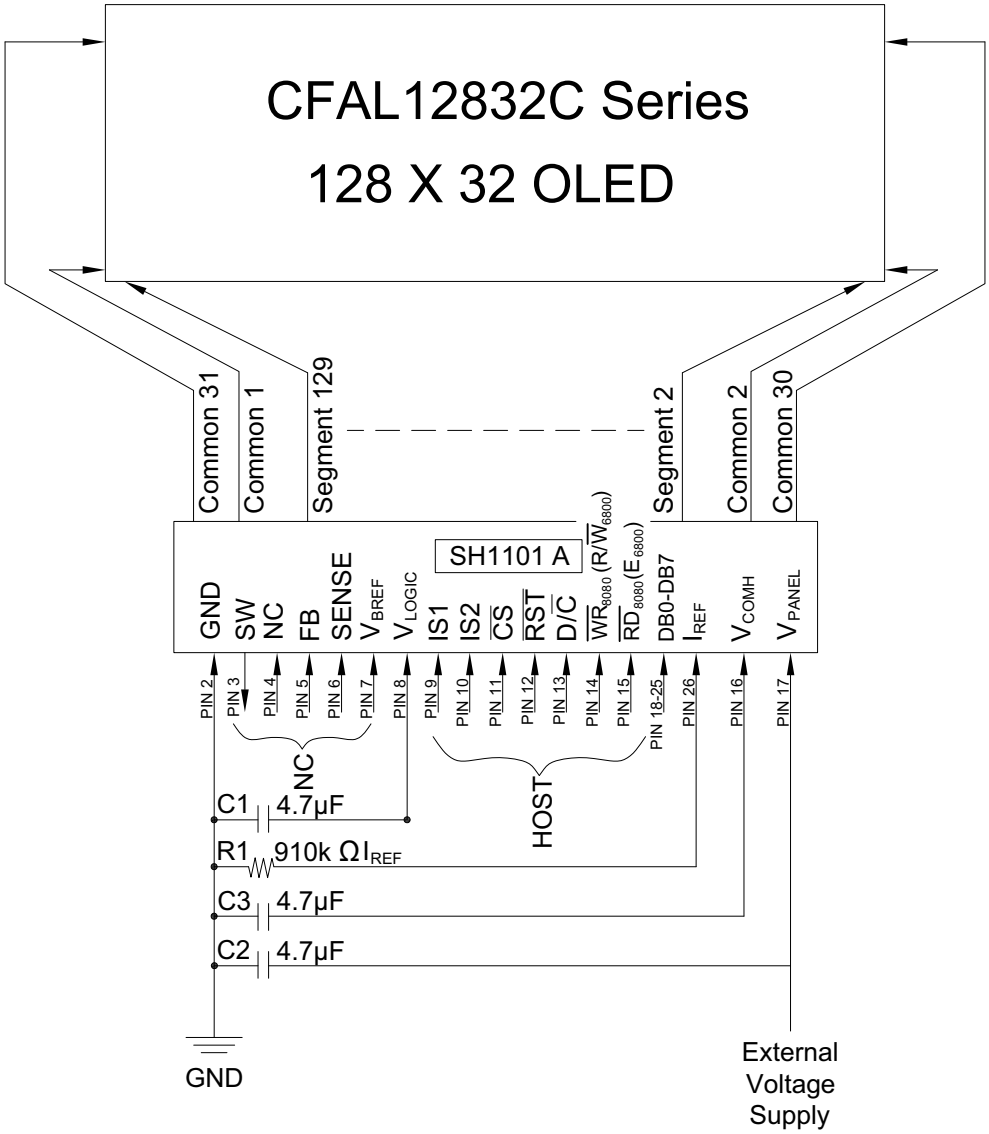


Figure 3. Externally Supplied V_{PANEL} Circuit Example

POWER UP AND POWER DOWN SEQUENCING

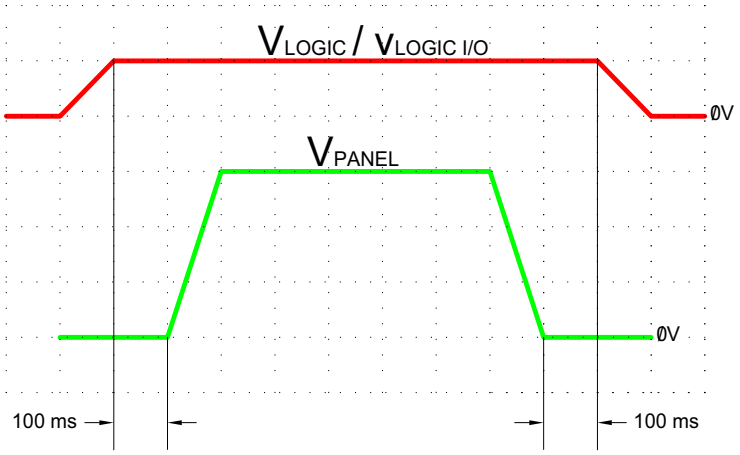


Figure 4. Power Up and Power Down Sequencing

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS	SYMBOL	MINIMUM	MAXIMUM
Operating Temperature*	T_{OP}	-20°C	+70°C
Storage Temperature*	T_{ST}	-30°C	+80°C
Humidity	RH	0%	90%
Logic Supply Voltage	V_{LOGIC}	-0.3v	+3.5v
Driver Supply Voltage	V_{PANEL}	0v	+15v
**Prolonged exposure at temperatures outside of this range may cause permanent damage to the module.*			

DC CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Logic Supply Voltage	V_{LOGIC}	T_{OP} = -20°C to +70°C	+2.4v	+3.3v	**+3.5v**[1]
OLED Driver Supply Voltage[2]	V_{PANEL}	T_{OP} = -20°C to +70°C	+7.5v	+8.0v	+9.0v
Normal Mode Power Consumption	$P_{OPERATION}$	With polarizer All pixels on Driving voltage:+8v Contrast setting: 0x28 Frame rate: 104Hz		31 mW	37 mW
Standby Mode Power Consumption	$P_{STANDBY}$	With polarizer 10% pixels on Driving voltage:+8v Contrast setting: 0x0B Frame rate: 104Hz		2.4 mW	
High Level Input Voltage	V_{IH}	I_{OUT} =0.5 mA 3.3MHz	+0.8v x V_{Logic} For V_{Logic} = +3.3v V_{IH} = +0.8v x +3.3v = +2.64v		V_{LOGIC}
Low Level Input Voltage	V_{IL}	I_{OUT} =0.5 mA 3.3MHz	0v		+0.2v x V_{Logic} For V_{Logic} = +3.3v V_{IL} = +0.2v x +3.3v = +0.66v
High Level Output Voltage	V_{OH}	I_{OUT} =0.5 mA 3.3MHz	+0.8v x V_{Logic} For V_{Logic} = +3.3v V_{IH} = +0.8v x +3.3v = +2.64v		V_{LOGIC}
High Level Output Voltage	V_{OL}	I_{OUT} =0.5 mA 3.3MHz	0v		+0.2v x V_{Logic} For V_{Logic} = +3.3v V_{IL} = +0.2v x +3.3v = +0.66v

[1] *Do not exceed 3.5v absolute maximum.*

[2] *The V_{PANEL} input must be a stable value with no ripple or noise.*

This is a summary of the module's major operating parameters. For detailed information see APPENDIX D: SINO WEALTH SH1101A CONTROLLER SPECIFICATION SHEET (Pg. 35).

DETAILS OF INTERFACE PIN FUNCTIONS

<table>
<tr><th>PIN</th><th>SIGNAL</th><th>LEVEL</th><th>DIRECTION</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>NC</td><td></td><td></td><td>No connection.</td></tr>
<tr><td>2</td><td>GND</td><td>0v</td><td></td><td>Ground. Must be connected to an external ground.</td></tr>
<tr><td>3</td><td>SW</td><td></td><td>O</td><td>Switch output drives gate of the external NMOS of the booster circuit.</td></tr>
<tr><td>4</td><td>NC</td><td></td><td></td><td>No connection.</td></tr>
<tr><td>5</td><td>FB</td><td>variable</td><td>I</td><td>Feedback resistor input for the booster circuit. Use to adjust booster output voltage level, V_{PANEL}.</td></tr>
<tr><td>6</td><td>SENSE</td><td></td><td></td><td>Source current for external NMOS of booster circuit.</td></tr>
<tr><td>7</td><td>V_{BREF}</td><td></td><td></td><td>Internal voltage reference for booster circuit. A decoupling capacitor, typically 1µF, should be connected to GND.</td></tr>
<tr><td>8</td><td>V_{LOGIC}</td><td>+2.4v
to
+3.5v</td><td>I</td><td>Power supply input. Must be connected to an external source.</td></tr>
<tr><td>9</td><td>IS1</td><td>H/L</td><td>I</td><td rowspan="2"><table><tr><th>IS1</th><th>IS2</th><th>Interface Mode</th></tr><tr><td>0</td><td>0</td><td>Serial</td></tr><tr><td>0</td><td>1</td><td>6800 Parallel</td></tr><tr><td>1</td><td>0</td><td>Not Allowed</td></tr><tr><td>1</td><td>1</td><td>8080 Parallel</td></tr></table></td></tr>
<tr><td>10</td><td>IS2</td><td>H/L</td><td>I</td></tr>
<tr><td>11</td><td>$\overline{CS}$</td><td>H/L</td><td>I</td><td>Chip select input.

Low: Controller chip is selected. Communications with the host possible.

High: Controller chip is not selected. Host interface signals are ignored by the controller.</td></tr>
<tr><td>12</td><td>$\overline{RST}$</td><td>H/L</td><td>I</td><td>Reset signal input.

Low: Display controller is reset. The $\overline{RST}$ pin should be pulsed low shortly after power is applied.

High: The $\overline{RST}$ pin should be brought high for normal operation.</td></tr>
</table>

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
13	D/$\overline{C}$	H/L	I	Data/Command control. Determines whether data bits are data or command. *1 – High:* DB0 to DB7 inputs are display data. *0 – Low:* DB0 to DB7 inputs transferred to command registers.
14	$\overline{WR}_{8080}$ (R/$\overline{W}_{6800}$)	H/L	I	Host interface input. *8080 Host*: Active low. Signal on the databus is latched at the rising edge of $\overline{WR}$ signal. *6800 Host*: read/write control signal output *R/$\overline{W}$ = High:* Read (Host←Module) *R/$\overline{W}$ = Low:* Write (Host→Module)
15	$\overline{RD}_{8080}$ (E_{6800})	H/L	I	Host interface input. Read data is output on databus when $\overline{RD}$ is low. *8080 Host*: Active low. Signal on the databus is latched at the rising edge of $\overline{RD}$ signal. *6800 Host:* Enable control signal input active high. *E = High:* Read or Write Active *E = Low:* No Read or Write Active
16	V_{COMH}		O	High level voltage output for common signals. A low ESR capacitor should be connected between this pin and GND. Do not connect external power supply directly to this pin.
17	V_{PANEL}	+7.5v to +8.5v	I	Only high voltage input on chip. Power must be supplied externally. *Note: You must observe power sequencing for this pin*. *Power Up* – Display must be powered up and initialized before power is applied to the pin. *Power Down* – Power must be removed from this pin before the display is powered off.

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
18	DB0	H/L	I/O	Bidirectional databus connects to 8-bit standard host databus. *In serial mode (IS1=0, IS2=0):* DB0 serves as the serial clock input signal (SCL) and DB1 serves as the serial data input pin (SI). DB2-DB7 are high impedance. In serial mode, data can be written to the display but not read. Pin 14 ($\overline{WR}_{8080}$ (R/$\overline{W}_{6800}$)) and pin 15 ($\overline{RD}_{8080}$ (E_{6800})) are unused and should be tied low. *In 6800 parallel mode:* Pin 14 is used as R/$\overline{W}_{6800}$. Pin 15 is used as E_{6800}. Data is input or output on DB0-DB7. *In 8080 parallel mode:* Pin 14 is used as $\overline{WR}_{8080}$. Pin 15 is used as $\overline{RD}_{8080}$. Data is input or output on DB0-DB7.
19	DB1	H/L	I/O	
20	DB2	H/L	I/O	
21	DB3	H/L	I/O	
22	DB4	H/L	I/O	
23	DB5	H/L	I/O	
24	DB6	H/L	I/O	
25	DB7	H/L	I/O	
26	I_{REF}		O	Segment output current reference for brightness adjustment. A resistor should be connected between this pin and GND. Set the current at 10µA.
27	NC			No connection.

QUICK REFERENCE FOR PIN FUNCTIONS (BACK PHOTO)

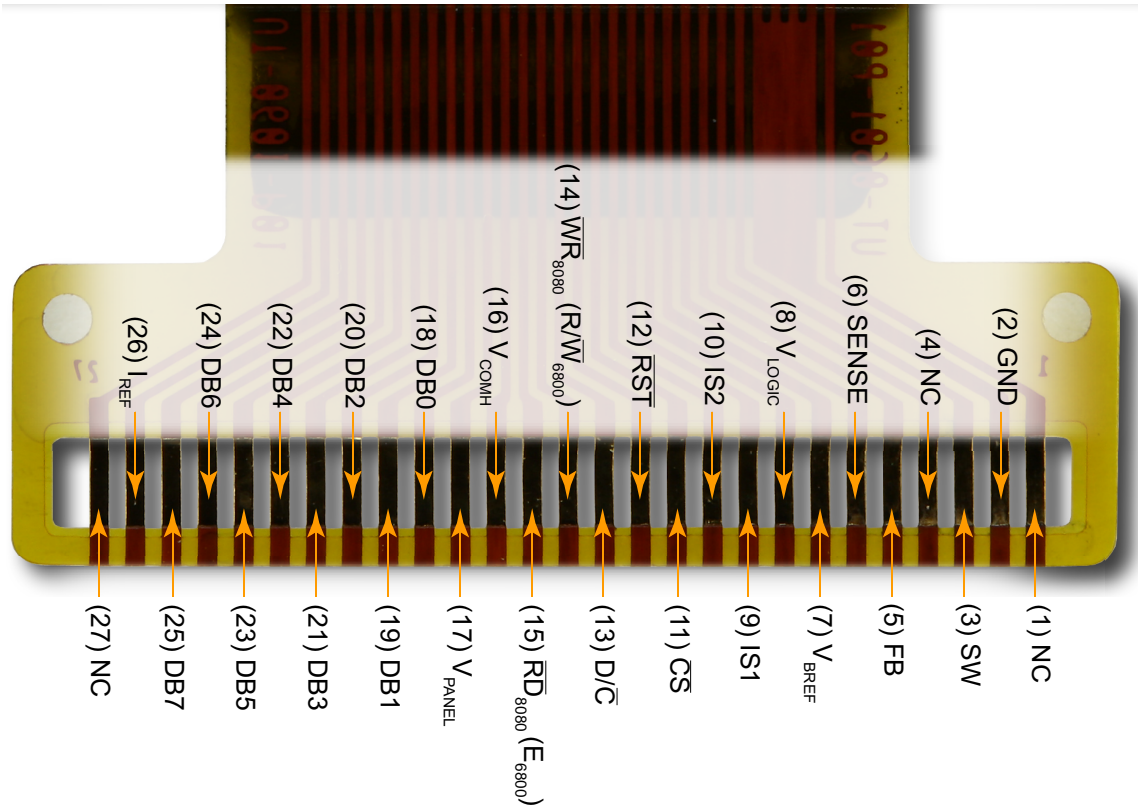


Figure 5. Back View of FPC (Labeled)

ESD (ELECTRO-STATIC DISCHARGE) SPECIFICATIONS

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. Ground your body, work surfaces, and equipment.

OPTICAL SPECIFICATIONS

OPTICAL CHARACTERISTICS

ITEM	SYMBOL	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Viewing Angle				>160°	
Dark Room Contrast Ratio[1]	CR			>100:1	
Response Time[2]				<10µs	
Luminous Intensity, Normal (IV)	$L_{BRNORMAL}$	With polarizer All pixels on Driving voltage:+8v Contrast setting: 0x28 Frame rate: 104Hz	40 cd/m^2	60 cd/m^2	
Luminous Intensity, Standby (IV)	$L_{BRSTANDBY}$	With polarizer 10% pixels on Driving voltage:+8v Contrast setting: 0x0B Frame rate: 104Hz		26 cd/m^2	
Chromaticity (CIE) for Blue	x	CIE (1931)	0.12	0.16	0.20
	y	CIE (1931)	0.22	0.26	0.30
Duty	1/32				

[1] *Contrast Ratio = (brightness with pixels light)/(brightness with pixels dark).*
[2] *Response Time: The amount of time it takes a pixel to change from active to inactive or back again.*

Definition of Viewing Angle

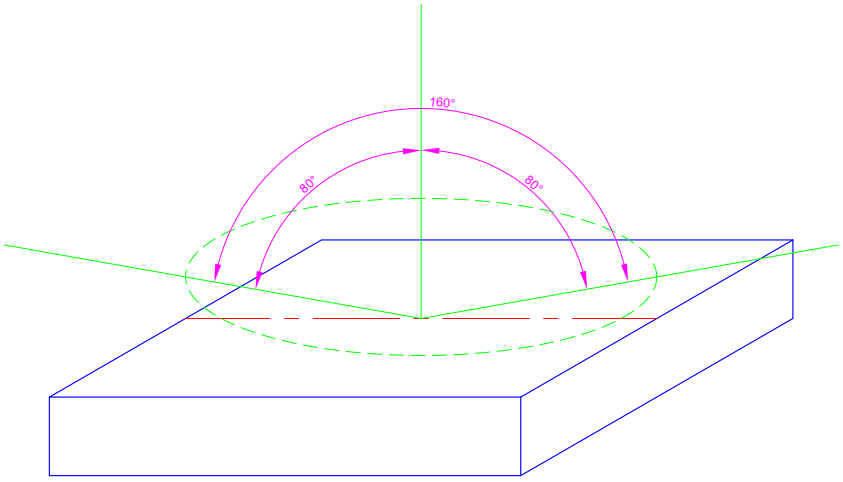


Figure 6. CFAL12832C-B-B1 has a 160° Viewing Angle

OLED CONTROLLER INTERFACE

This module uses a Sino Wealth SH1101A controller. For your reference, we added APPENDIX D: SINO WEALTH SH1101A CONTROLLER SPECIFICATION SHEET (Pg. 35) to this Data Sheet.

MODULE RELIABILITY AND LONGEVITY

MODULE RELIABILITY

ITEM	SPECIFICATION
CFAL12832C-B-B1	10,000 hours >50% of initial brightness at typical brightness for a new module.

OLED displays are an emissive technology. Each pixel is susceptible to dimming based on its individual use (burn-in). Frequently used pixels will dim more quickly than pixels that are not used as often. Please avoid using a bright, static, high-contrast image for a long time. If you want to leave the display powered on, please use scrolling text or alternating images to "wear level" the pixels. To conserve power and display lifetime, turn off or dim the display when it is not in use.

MODULE LONGEVITY (EOL / REPLACEMENT POLICY)

Crystalfontz is committed to making all of our modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life", EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.

Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's webpage as soon as possible. If interested, you can subscribe to future part change notifications.

CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions below. Excessive voltage will shorten the life of the module. You must drive the display within the specified voltage limit. See Absolute Maximum Ratings (Pg. 12).

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING

- The exposed surface of the “glass” is actually a polarizer laminated on top of the glass.To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- To protect the soft plastic polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the module, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not modify the tab of the metal holder or make connections to it.
- For prototype work, hand soldering may be acceptable. Preset soldering iron to <260°C. Do not apply heat for more than 3 to 4 seconds.
- For production soldering, please use a commercial hot bar solder station, along with the appropriate fixture.

- Solder only to the exposed terminals of the FPC connector. Please note that the FPC is quite fragile; use extreme care when soldering by hand. The use of Kapton® tape to help locate and secure the FPC may be useful.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.
- Use care to keep the exposed terminals clean. Contamination, including fingerprints may make the soldering difficult, and the reliability of the soldered connection poor.
- Sharp bends can damage the FPC. Do not crease FPC. Do not bend FPC tightly against the edge of the OLED panel.
- Do not repeatedly bend the FPC beyond its elastic region.

TAB SOLDERING

This module uses a "TAB" (tape automated bonding) or "COF" (chip on flex) style flex tail mated with a "COG" (chip on glass) display controller. The TAB is soldered directly to corresponding pads on your PCB by using a hot-bar soldering machine. High volume contract manufacturers will be familiar with this type of construction and its assembly methods.

Hot-bar soldering machines designed for prototype, rework, or repair of TAB connections are available from equipment suppliers at reasonable cost. The TAB style connection requires no separate connector so the cost is very low and the ultrathin profile of the display is maintained.

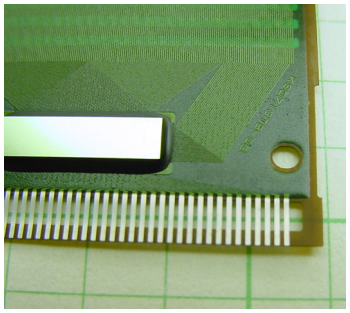


Figure 7. Typical Tab Solder Tail Construction

Hot Bar Soldering Machine

We have had good experience with the APE Bondmaster and their price is reasonable ($US4K in June 2009). Other possible solutions are:

http://www.fancort.com/hotbar/hotbar.html
https://www.manncorp.com/hot-bar-soldering/pbs-series/index.php?auto=done
http://www.cherusal.com/tm-111mkiii.htm

The process is:

1. Pads on the PCB are tinned.
2. Tail is visually aligned to the PCB or by using the alignment holes.
3. Tail is held in place relative to the PCB with Kapton® tape.
4. Bondmaster head is lowered, applying pressure between the tail and the PCB.
5. Bondmaster is "cycled", which means it heats up to the point of melting the solder and then cools down.
6. Bondmaster head is raised.

Hand Soldering

For prototype work, hand soldering may be acceptable. Preset soldering iron to <260°C. Do not apply heat for more than 3 to 4 seconds. The FPC is quite fragile; use extreme care when soldering by hand. Great care must be taken since the conductors of the tail are completely exposed in the area where they are soldered. Solder only to the exposed terminals of the FPC connector. The use of Kapton® tape to help locate and secure the FPC may be useful.

AVOID SHOCK, IMPACT, TORQUE, OR TENSION

- Do not expose the module to strong mechanical shock, impact, torque, or tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

CLEANING

- The polarizer (laminated to the glass) is soft plastic. The soft plastic is easily scratched or damaged. Be very careful when you clean the polarizer.
- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips).
- Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand “Crystal Clear Tape”). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.

OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product.” This module is not "user friendly" and connecting it to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
- Operate away from dust, moisture, and direct sunlight.

STORAGE AND RECYCLING 

- Store in an ESD-approved container away from dust, moisture, and direct sunlight, fluorescent lamps, or any ultraviolet ray.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations.
- Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated Crystalfontz modules at an approved facility.

APPENDIX A: QUALITY ASSURANCE STANDARDS

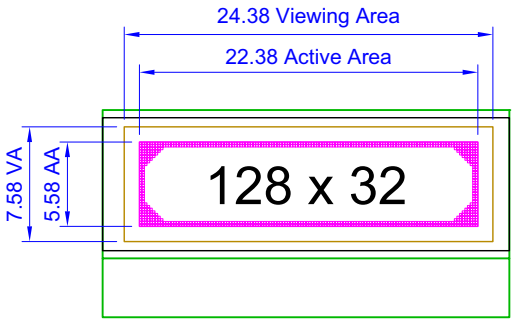
INSPECTION CONDITIONS

- Environment
  - Temperature: 25±5°C
  - Humidity: 30~85% RH (noncondensing)
- For visual inspection of active display area
  - Source lighting: two 20-Watt or one 40-Watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance: 30±5 cm (about 12 inches)
  - Viewing angle: inspect at 45° angle of vertical line right and left, top and bottom

COLOR DEFINITIONS

We try to describe the appearance of our modules as accurately as possible. For the photos, we adjust for optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.

DEFINITION OF ACTIVE AREA AND VIEWING AREA



ACCEPTANCE SAMPLING

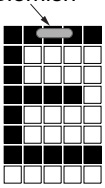
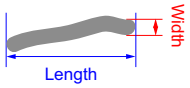
DEFECT TYPE	AQL*
Major	≤.65%
Minor	<1.0%
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

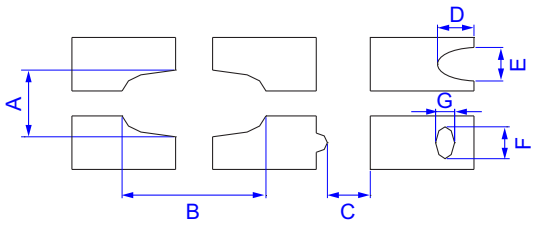
DEFECTS CLASSIFICATION

Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

ACCEPTANCE STANDARDS

#	DEFECT TYPE	CRITERIA			MAJOR / MINOR
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major
2	Viewing area defect	Viewing area does not meet specifications.			Major
3	Blemishes or foreign matter on display segments	Blemish 	*Defect Size*	*Acceptable Qty*	Minor
			≤0.30 mm	3	
			≤2 defects within 10 mm of each other		
4	Dark lines or scratches in display area 	*Defect Width*	*Defect Length*	*Acceptable Qty*	Minor
		≤0.03 mm	≤3.0 mm	3	
		0.03 to 0.05	≤2.0 mm	2	
		0.05 to 0.08	≤2.0 mm	1	
		0.08 to 0.10	≤3.0 mm	0	
		≥0.10	>3.0 mm	0	
5	Bubbles between polarizer film and glass		*Defect Size*	*Acceptable Qty*	Minor
			≤0.20 mm	Ignore	
			0.20 to 0.40 mm	3	
			0.40 to 0.60 mm	2	
			≥0.60 mm	0	

<table>
<tr><th>#</th><th>DEFECT TYPE</th><th>CRITERIA</th><th>MAJOR / MINOR</th></tr>
<tr><td rowspan="6">6</td><td rowspan="6">Display pattern defect</td><td colspan="2"> 
</td><td rowspan="6">Minor</td></tr>
<tr><td>Pixel Size</td><td>Acceptable Qty</td></tr>
<tr><td>((A+B)/2)≤0.20 mm</td><td rowspan="4">≤3 total defects
≤2 pinholes per digit</td></tr>
<tr><td>C>0 mm</td></tr>
<tr><td>((D+E)/2)≤0.25 mm</td></tr>
<tr><td>((F+G)/2)≤0.25 mm</td></tr>
<tr><td>7</td><td>PCB defects</td><td colspan="2">1. Oxidation or contamination on connectors.*
2. Wrong parts, missing parts, or parts not in specification.*
3. Jumpers set incorrectly.
4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth.
*Minor if display functions correctly. Major if the display fails.</td><td>Minor</td></tr>
<tr><td>8</td><td>Soldering defects</td><td colspan="2">1. Unmelted solder paste.
2. Cold solder joints, missing solder connections, or oxidation.*
3. Solder bridges causing short circuits.*
4. Residue or solder balls.
5. Solder flux is black or brown.
*Minor if display functions correctly. Major if the display fails.</td><td>Minor</td></tr>
</table>

APPENDIX B: SAMPLE CODE

SOURCES FOR DRIVER LIBRARIES

Graphic driver libraries may save a lot of time and help you develop a more professional product. Possible library sources are easyGUI, RAMTEX, Micrium, en.radzio.dxp.pl, and Segger emWin.

SAMPLE CODE

This code will initialize the display and then cycle between two images. You can download the complete source from this link: http://www.crystalfontz.com/products/document/2049/CFAL12832CB.zip

Note: Please observe V_{PANEL} sequencing as described in Details of Interface Pin Functions (Pg. 14). See also Power Up and Power Down Sequencing (Pg. 12).

```
#include <avr/io.h>
#include <util/delay.h>

// all on PORTC
#define OLED_CD PC7
#define OLED_RW  PC6// WR in 8080 mode
#define OLED_E    PC5   // RD in 8080 mode
#define OLED_WR  PC6// WR in 8080 mode
#define OLED_RD  PC5// RD in 8080 mode
#define OLED_CS PC3
#define OLED_RESPC2

#define CLR_CD PORTC &= ~(1<<OLED_CD);
#define SET_CD PORTC |=  (1<<OLED_CD);

#define CLR_CS PORTC &= ~(1<<OLED_CS);
#define SET_CS PORTC |=  (1<<OLED_CS);

#define CLR_RESET PORTC &= ~(1<<OLED_RES);
#define SET_RESET PORTC |=  (1<<OLED_RES);

#define CLR_WR PORTC &= ~(1 << OLED_WR);
#define SET_WR PORTC |=  (1 << OLED_WR);
#define CLR_RD PORTC &= ~(1 << OLED_RD);
#define SET_RD PORTC |=  (1 << OLED_RD);

// for bmp function
typedef uint8_t bitmap_t[8][132];

void delay(uint32_t twait)
{
        while (twait--)
                asm volatile ("nop");
}


uint8_t boot_logo[8][132] =
{
... See source code ...
};
```

```
uint8_t bitmap[8][132] =
{
... See source code ...
};


void oled_cmd(uint8_t cmd)
{

        PORTA = cmd;// set up data on bus
  CLR_CS;    // chip selected
  CLR_CD;    // command mode

  SET_RD;

        // clock WR
  CLR_WR;
  SET_WR;

  SET_CS;    // unselect chip
}

void oled_data(uint8_t dat)
{

        PORTA = dat;// set up data on bus
  SET_CD;        // data mode
  CLR_CS;        // chip selected

  SET_RD;

        // clock WR
  CLR_WR;
  SET_WR;

  SET_CS;        // unselect chip
}


void OLED_clr(uint8_t color)
{
        int i,p;

        oled_cmd(0x40);

        for (p=0;p<8;p++) // pages
        {
                oled_cmd(0xB0 + p);    // set page address
                oled_cmd(0x10);        // set high column address
                oled_cmd(0x00);        // set low column address
                for (i=0;i<132;i++)
                {
                        oled_data(color);
                }
        }
}

void bmp(bitmap_t b)
{
        unsigned char j=0;
  unsigned char page=0;

  for(page=0;page<8;page++)
  {
    oled_cmd(0xB0+page);  // set page address
```

```
              oled_cmd(0x00);       // set high column address
    oled_cmd(0x10);       // set low column address

    for(j=0;j<132;j++)
    {
      oled_data(b[page][j]);
    }
  }
}

void init_OLED()
{
        PORTD = 0;      // all off
        DDRD |= (1<<3);// VPP output

        DDRA = 0xFF;    // set PORTA for output

        PORTC = 0b11111110;
        DDRC = 0xFE;

        DDRD |= 0x06;// oled pins output

        delay(20000L);

  // reset the display
  CLR_RESET;
        delay(10000);
  SET_RESET;

        delay(20000);

        // enable VPP
        PORTD |= (1<<3);

        delay(200000L);

  oled_cmd(0xAE);    // display OFF/ON 0xAE = display off, 0xAF = display on

        oled_cmd(0xAD);    // DC-DC voltage converter OFF
        oled_cmd(0x8A);    // 0x8A = OFF, 0x8B = ON

        oled_cmd(0xA8);    // Set multiplex ratio
        oled_cmd(0x1F);    // set for 32

        oled_cmd(0xD3);    // Set display offset
        oled_cmd(0x00);    // no offset (0-63 are acceptable values)

        oled_cmd(0x40);    // Set display start line (0x40 = start at line 0)

        oled_cmd(0xA1);    // Segment mapping (0xA0 normal, 0xA1 reversed)

        oled_cmd(0xC0);    // Common output scan direction (0xC0 = (0 - COM[N-1]), 0xC8 = (COM[N-1] - 0)

        oled_cmd(0xA6);    // Set normal / reverse display (0xA6 = normal, 0xA7 = inverted/reverse)

        oled_cmd(0xA4);    // Set entire display off / on (0xA4 = off, 0xA5 = on)

        oled_cmd(0x81);    // Contrast control mode set
  oled_cmd(0x88);    // (0x00 - 0xFF valid)

        oled_cmd(0xD5);    // Set Display clock divide ratio/oscillator frequency
        oled_cmd(0x00);    // Set for -5%

        oled_cmd(0x70);    // Set lower column address (0x00 - 0x0F valid)
```

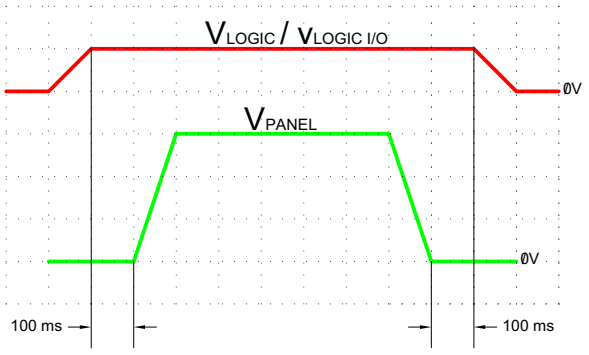
```
        oled_cmd(0xD9);    // Set discharge/precharge period
        oled_cmd(0x00);    // (A3 - A0 pre charge, A7 - A4 dis charge) period adjustment

        oled_cmd(0xAF);    // Display on

        delay(5000L);

        OLED_clr(0x00);     // clear display
}

/*****************************************************************************************/

int main()
{
  init_OLED();

        delay(20000L);

        while (1)
        {
                bmp(boot_logo);
                delay(10000000L);
                bmp(bitmap);
                delay(10000000L);
        }

        return 0;
}
```

APPENDIX C: OLED MODULE TERMS AND SYMBOLS

Crystalfontz Symbol	Equivalent	Equivalent	Equivalent	Description
C				Capacitor
cd/m^2	nit			Candela meter squared is the standard unit of measurement for luminous intensity (photometric brightness).
CIE				A color model based on human perception developed by the CIE (Commission Internationale de l'Eclairage) committee.
CLS				Clock select pin.
COF	COT	TAB		Chip On Flex. Controller is on the FPC. Similar in appearance to "TAB". The flex circuit on COF is typically much thinner than the flex of a "flex tail".
COG				Chip On Glass. Controller is on the glass panel.
COM				Common driver. Common signal output for OLED display.
CR				Contrast Ratio = (brightness with pixels light)/ (brightness with pixels dark).
$\overline{CS}$	CS#			Chip select input. *Low:* Controller chip is selected. Communications with host is possible. *High:* Controller chip is not selected. Host interface signals are ignored by the controller.
D				Diode
DB0 ~ DB*n*	D0 ~ D*n*			Bidirectional databus connects to 8-bit or 16-bit standard host databus. When SPI (serial interface) is selected, DB0 serves as the serial clock input signal (SCL or SCLK) and DB1 serves as the serial data input signal (SI or SDIN). DB2 to DB*n* are set to high impedance.
D/$\overline{C}$	RS	A0	CD or D/C#	Data/Command control. Determines whether data bits are data or command. *1 – High*: Addresses the data register. *0 – Low:* Addresses the command register.
ESD				Electro-Static Discharge. Sudden and brief electrical current that flows between two objects. ESD between a human and an OLED module can cause permanent damage.

Crystalfontz Symbol	Equivalent	Equivalent	Equivalent	Description (Continued)
FB				Feedback input for the booster circuit. Use to adjust booster output voltage level, V_{PANEL}.
FFC				Flat Flex Cable. Used for Touch Screen connection. Also called “pigtail”.
FG				Frame Ground.
FPC				Flexible Printed Circuit. Also called “flex tail”. Typically much thicker than the “flex” film of COF (Chip On Flex).
GDR				Gate Drive. Output signal drives the gate of the external NMOS of the booster circuit.
GND	V_{SS}			Ground. Must be connected to an external ground.
I_{LOGIC}	I_{DD}			Operating current for V_{LOGIC}.
$I_{LOGIC, SLEEP}$	$I_{DD, SLEEP}$			Sleep mode current for V_{LOGIC}.
I_{PANEL}	I_{CC}			Supply current for V_{PANEL}.
$I_{PANEL, SLEEP}$	$I_{CC, SLEEP}$			Sleep mode current for V_{PANEL}.
I_{REF}				Segment output current reference for brightness adjustment. A resistor should be connected between this pin and GND. Used to set the current.
I/O				Input/Output.
IS1	BS1	C86	M80	<table><tr><th>IS1</th><th>IS2</th><th>Interface Mode</th></tr><tr><td>0</td><td>0</td><td>SPI (Serial)</td></tr><tr><td>0</td><td>1</td><td>6800 Parallel</td></tr><tr><td>1</td><td>0</td><td>Not Allowed</td></tr><tr><td>1</td><td>1</td><td>8080 Parallel</td></tr></table>
IS2	BS2	P/S	$\overline{MS}$, $\overline{MS}$ or M/S#	
$L_{BRNORMAL}$	IV			Luminous Intensity Brightness, NORMAL operation.
$L_{BRSTANDBY}$	IV			Luminous Intensity Brightness, STANDBY.
mm				Millimeter or millimetre. Unit of length equal to one thousandth of a meter. 1 millimeter = 0.0394 inches.

Crystalfontz Symbol	Equivalent	Equivalent	Equivalent	Description (Continued)
mW				Milliwatt is equal to one thousandth of a Watt. Watts = Volts x Amps.
NC	nc			No Connection.
OLED				Organic light-emitting diode
$P_{OPERATION}$	P_T			Normal mode Power consumption
$P_{STANDBY}$				Standby mode Power consumption.
Q				Transistor, including FET and MOSFET.
R				Resistor
$\overline{RD}_{8080}$ (E_{6800})	$\overline{RD}$ (E)	E ($\overline{RD}$)	E	Host interface input. *8080 Host:* Active low. Signal on the databus is latched at the rising edge of $\overline{RD}$. *6800 Host:* Enable control signal input active high. E = *High:* Read or Write operation is active E = *Low:* No operation
RH	Rh			Relative Humidity.
RoHS				Restriction of Hazardous Substances Directive, an environmental standard.
$\overline{RST}$	$\overline{RES}$	RST#	RES#	Reset signal. *Low:* Display controller is reset. The $\overline{RST}$ pin should be pulsed low shortly after power is applied. *High:* The $\overline{RST}$ pin should be brought high for normal operation.
SCL	SCK			Serial Clock signal.
SEG				Segment driver. Segment signal output for OLED display.
SENSE				Source current for external NMOS of booster circuit.
SI	SDA	MOSI		Serial data Input signal.
SW				Switch output drives the gate of the external NMOS of the booster circuit.
Ta	TA			“Ambient temperature” is the temperature of the air that surrounds a component.
T_{OP}				OPerating temperature.
T_{ST}	T_{STG}			Storage Temperature.

Crystalfontz Symbol	Equivalent	Equivalent	Equivalent	Description (Continued)
V_{BREF}				Internal voltage reference for booster circuit. A decoupling capacitor, typically 1µF, should be connected to GND.
V_{COMH}				High level voltage output for common signals. A low ESR capacitor should be connected between this pin and GND. Do not connect external power supply directly to this pin.
V_{IH}	V_{ICH}			High level input voltage.
V_{IL}	V_{LCH}			Low level input voltage.
V_{LOGIC}	V_{DD}	V_{DD1}	V_{CC}	Power supply input. Must be connected to an external source.
$V_{LOGIC\ I/O}$	$V_{DD\ I/O}$	$V_{I/O}$	V_{CCIO}	Supply voltage for I/O signals.
V_{OH}	V_{OHC}			High level output voltage.
V_{OL}	V_{OLC}			Low level output voltage.
V_{PANEL}	V_{PP}	V_{CC}		Driver supply voltage. Only high voltage input on chip. Power must be supplied externally. *Note: You must observe power sequencing for this signal.* *Power Up* – Display must be powered up and initialized before power is applied to the signal. *Power Down* – Power must be removed from this signal before the display is powered off. 

Crystalfontz Symbol	Equivalent	Equivalent	Equivalent	Description (Continued)
V_{REF}				Voltage reference pin for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to V_{PANEL}.
V_{SL}				Segment voltage reference pin. This pin should be left open.
$\overline{WR}_{8080}$ ($R/\overline{W}_{6800}$)	R/$\overline{W}$ ($\overline{WR}$)	$\overline{WR}$ (R/$\overline{W}$)	R/W#	Host interface input. *8080 Host:* Active low. Signal on the databus is latched at the rising edge of $\overline{WR}$ signal. *6800 Host:* Read/Write control signal output. *R/$\overline{W}$* = High: Read (Host←Module) *R/$\overline{W}$* = Low: Write (Host→Module)

APPENDIX D: SINO WEALTH SH1101A CONTROLLER SPECIFICATION SHEET

The complete *Sino Wealth 132 x 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller* Data Sheet v2.2 (59 pages) follows.

SH1101A

132 X 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller

Features

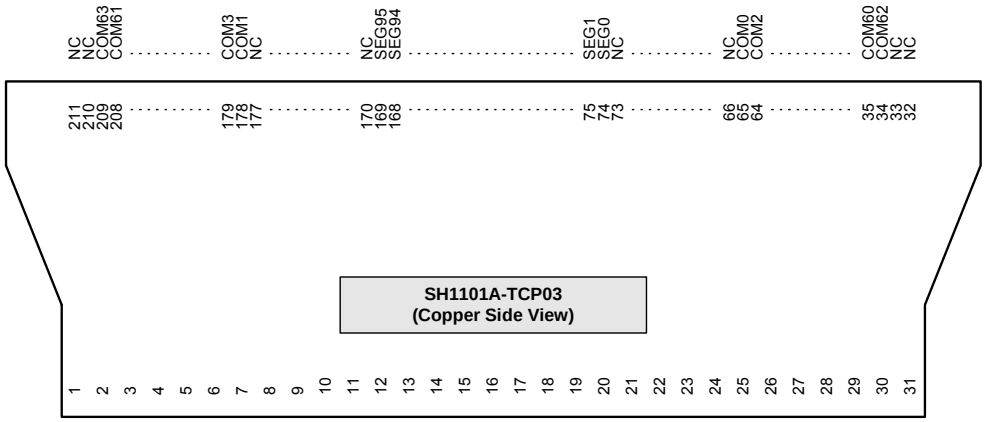
- Support maximum 132 X 64 dot matrix panel
- Embedded 132 X 64 bits SRAM
- Operating voltage: (Normal mode)
  - Logic voltage supply: V_{DD1} = 2.4V - 3.5V
  - DC-DC voltage supply: V_{DD2} = 2.4V - 3.5V
  - OLED Operating voltage supply: V_{PP} = 7.0V - 16.0V
- Operating voltage:(Low voltage mode)
  - Logic voltage supply: V_{DD1} = 1.65V - 3.5V
  - DC-DC voltage supply: V_{DD2} = 2.4V - 3.5V
  - OLED Operating voltage supply: V_{PP} = 7.0V - 9.0V
- Maximum segment output current: 320μA
- Maximum common sink current: 45mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface, serial peripheral interface
- Programmable frame frequency and multiplexing ratio
- Row re-mapping and column re-mapping (ADC)
- Vertical scrolling
- On-chip oscillator
- Available internal DC-DC converter
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
  - Sleep mode: <5μA
- Wide range of operating temperatures: -40 to +85°C
- Available in COG and TCP form

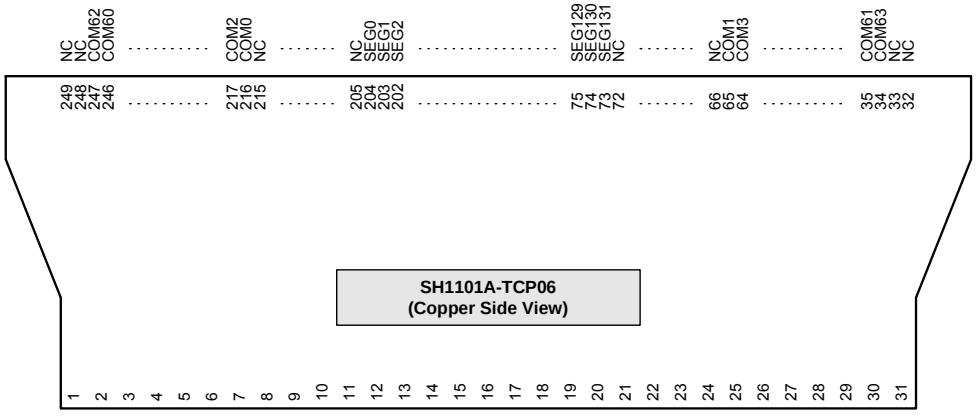
General Description

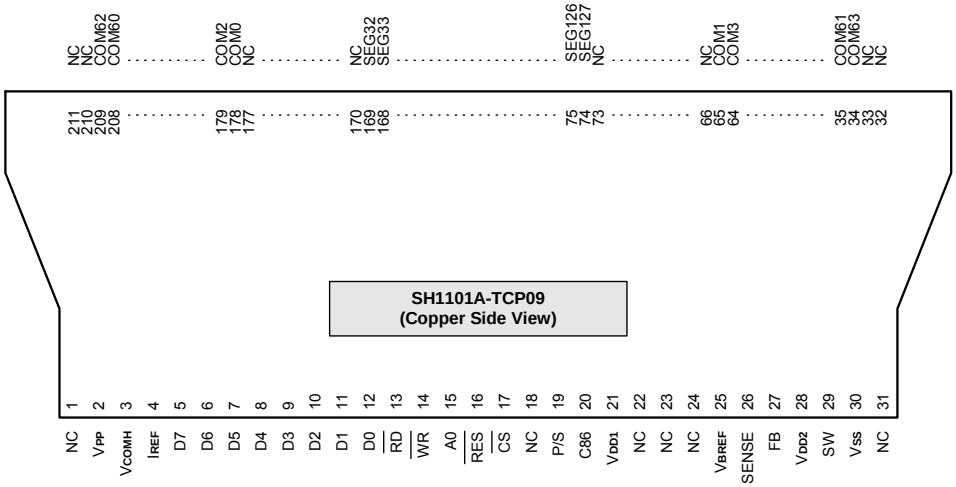
SH1101A is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. SH1101A consists of 132 segments, 64 commons that can support a maximum display resolution of 132 X 64. It is designed for Common Cathode type OLED panel.
SH1101A also support low voltage mode: V_{DD1}=1.65 - 3.5V and V_{PP} = 7.0V - 9.0V.

SH1101A embeds with contrast control, display RAM oscillator and efficient DC-DC converter, which reduces the number of external components and power consumption. SH1101A is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.

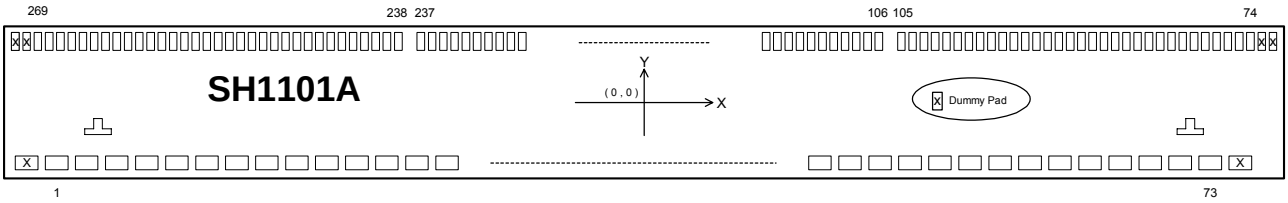
Pin Configuration



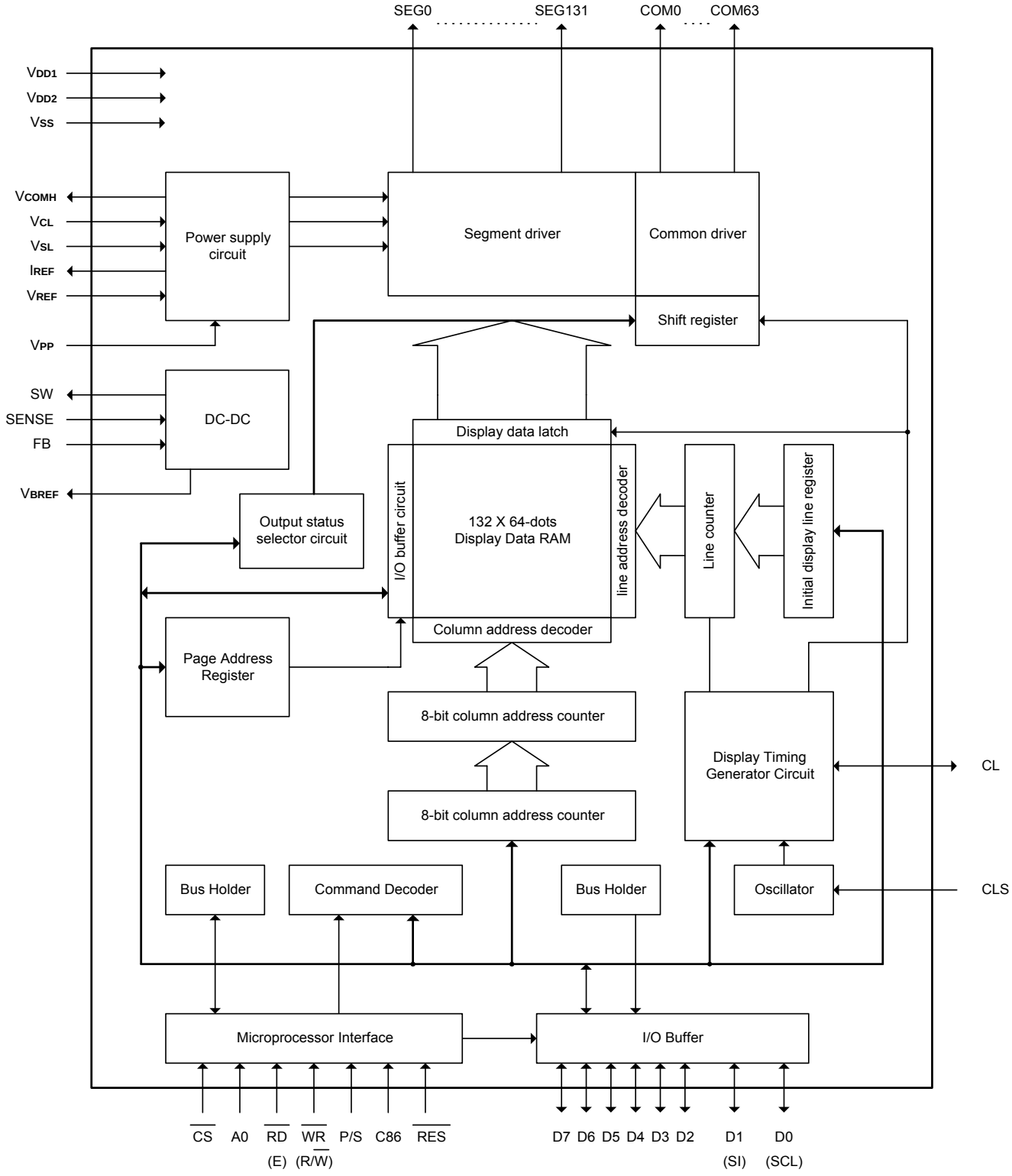




Pad Configuration



Block Diagram



Pad Description

Power Supply

Pad No.	Symbol	I/O	Description
28 - 31	V_{DD1}	Supply	Power supply input: Normal mode: 2.4 - 3.5V Low voltage mode: 1.65 - 3.5V
34, 44, 62	V_{DD1}	Supply	Power supply output for pad option: Normal mode: 2.4 - 3.5V Low voltage mode: 1.65 - 3.5V
17 - 20	V_{DD2}	Supply	2.4 - 3.5V power supply pad for the internal buffer of the DC-DC voltage converter.
7 - 13	V_{SS}	Supply	Ground.
21, 32, 36, 42, 64	V_{SS}	Supply	Ground output for pad option.
49 - 53, 71 - 73	V_{PP}	Supply	This is the most positive voltage supply pad of the chip. It should be supplied externally.
66	V_{PP}	Supply	This is the most positive voltage output for pad option, which cannot be used as the most positive voltage input.
4 - 6	V_{SL}	Supply	This is a segment voltage reference pad. This pad should be connected to Vss externally.
1 - 3	V_{CL}	Supply	This is a common voltage reference pad. This pad should be connected to Vss externally.

OLED Driver Supplies

Pad No.	Symbol	I/O	Description
70	V_{REF}	I	This is a voltage reference pad for pre-charge voltage in driving OLED device. Voltage should be set to match with the OLED driving voltage in current drive phase. It can either be supplied externally or by connecting to V_{PP}.
65	I_{REF}	O	This is a segment current reference pad. A resistor should be connected between this pad and Vss. Set the current at 10μA.
45 - 48, 67 - 69	V_{COMH}	O	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and Vss.
14 - 16	SW	O	This is an output pad driving the gate of the external NMOS of the booster circuit.
22	FB	I	This is a feedback resistor input pad for the booster circuit. It is used to adjust the booster output voltage level, V_{PP}.
23	SENSE	I	This is a source current pad of the external NMOS of the booster circuit.
24	V_{BREF}	O	This is an internal voltage reference pad for booster circuit. A stabilization capacitor, typical 1μF, should be connected to Vss.

System Bus Connection Pads

<table>
<tr><th>Pad No.</th><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>37</td><td>CL</td><td>I/O</td><td>This pad is the system clock input. When internal clock is enabled, this pad should be Left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.</td></tr>
<tr><td>63</td><td>CLS</td><td>I</td><td>This is the internal clock enable pad.
CLS = “H”: Internal oscillator circuit is enabled.
CLS = “L”: Internal oscillator circuit is disabled (requires external input).
When CLS = “L”, an external clock source must be connected to the CL pad for normal operation.</td></tr>
<tr><td>33</td><td>C86</td><td>I</td><td>This is the MPU interface switch pad.
C86 = “H”: 8080 series MPU interface.
C86 = “L”: 6800 series MPU interface.</td></tr>
<tr><td>35</td><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch pad.
P/S = “H”: Parallel data input.
P/S = “L”: Serial data input.
When P/S = “L”, D2 to D7 are HZ. D2 to D7 may be “H”, “L” or Open. $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) are fixed to either “H” or “L”. With serial data input, RAM display data reading is not supported. These are MPU interface input selection pads.
See the following table for selecting different interfaces:
<table>
<tr><th></th><th>6800-Parallel Interface</th><th>8080-Parallel Interface</th><th>Serial Interface</th></tr>
<tr><td>C86</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>P/S</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>38</td><td>$\overline{CS}$</td><td>I</td><td>This pad is the chip select input. When $\overline{CS}$ = “L”, then the chip select becomes active, and data/command I/O is enabled.</td></tr>
<tr><td>39</td><td>$\overline{RES}$</td><td>I</td><td>This is a reset signal input pad. When $\overline{RES}$ is set to “L”, the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.</td></tr>
<tr><td>40</td><td>A0</td><td>I</td><td>This is the Data/Command control pad which determines whether the data bits are data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.</td></tr>
<tr><td>41</td><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When R/$\overline{W}$ = “H”: Read.
When R/$\overline{W}$ = “L”: Write.</td></tr>
<tr><td>43</td><td>$\overline{RD}$
(E)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the SH1101A data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU , this is active HIGH. This is used as an enable clock input of the 6800 series MPU.</td></tr>
<tr><td>54 - 61
54
55</td><td>D0 - D7
(SCL)
(SI)</td><td>I/O
I
I</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance.
When the chip select is inactive, D0 to D7 are set to high impedance.</td></tr>
</table>

OLED Drive Pads

Pad No.	Symbol	I/O	Description
105 - 74, 238 - 269	COM0 - 63	O	These pads are Common signal output for OLED display.
106 - 237	SEG0 - 131	O	These pads are Segment signal output for OLED display.

Test Pads

Pad No.	Symbol	I/O	Description
25	TEST1	I	Test pads, internal pull low, no connection for user.
27	TEST2	O	Test pads, no connection for user.
26	TEST3	I	Test pads, no connection for user.
-	NC	-	NC pads, no connection for user.

Functional Description

Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface or Serial Interface (SPI) can be selected by different selections of C86, P/S as shown in Table 1.

Table. 1

	6800-Parallel Interface	8080-Parallel Interface	Serial Interface
C86	0	1	0
P/S	1	1	0

6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. When $\overline{WR}$ (R/$\overline{W}$) = "H", read operation from the display RAM or the status register occurs. When $\overline{WR}$ (R/$\overline{W}$) = "L", Write operation to display data RAM or internal command registers occurs, depending on the status of A0 input. The $\overline{RD}$ (E) input serves as data latch signal (clock) when it is "H", provided that $\overline{CS}$ = "L" as shown in Table. 2.

Table. 2

P/S	C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
1	0	6800 microprocessor bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D0 to D7

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processings are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 1 below.

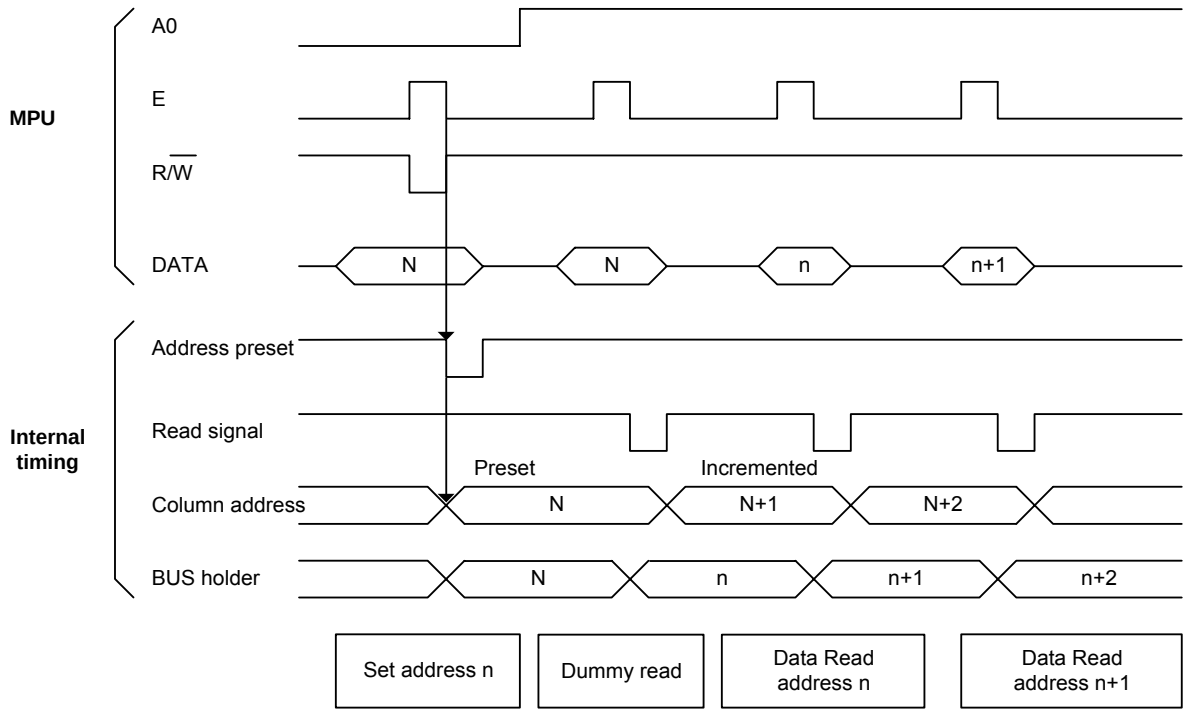


Figure. 1

8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$ (R/$\overline{W}$), $\overline{RD}$ (E), A0 and $\overline{CS}$. The $\overline{RD}$ (E) input serves as data read latch signal (clock) when it is "L" provided that $\overline{CS}$ = "L". Display data or status register read is controlled by A0 signal. The $\overline{WR}$ (R/$\overline{W}$) input serves as data write latch signal (clock) when it is "L" and provided that $\overline{CS}$ = "L". Display data or command register write is controlled by A0 as shown in Table. 3.

Table. 3

P/S	C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7
1	1	8080 microprocessor bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0 to D7

Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

Data Bus Signals

The SH1101A identifies the data bus signal according to A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals.

Table. 4

Common	6800 processor	8080 processor		Function
A0	(R / $\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM or command register in the same clock. See Figure. 2.

Table. 5

P/S	C86	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D7
0	0	Serial Interface (SPI)	$\overline{CS}$	A0	-	-	SCL	SI	(HZ)

Note: "-" Must always be HIGH or LOW.

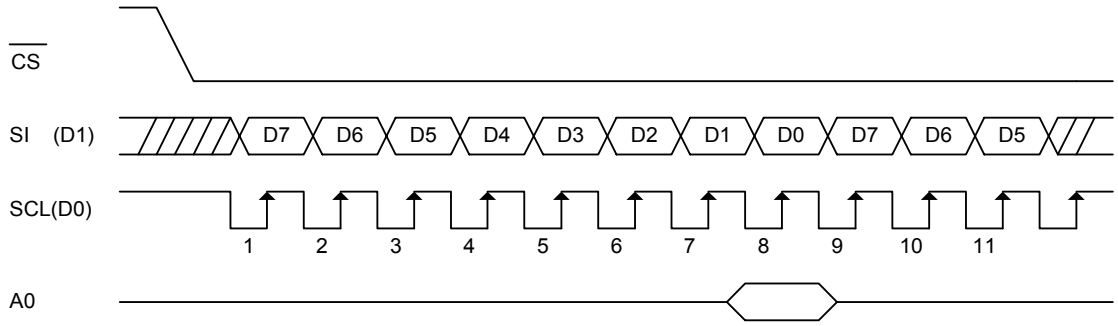


Figure. 2

- When the chip is not active, the shift registers and the counter are reset to their initial statuses.
- Read is not possible while in serial interface mode.
- Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = "H", the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = "L", the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 X 64 bits.

For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

The Page Address Circuit

As shown in Figure. 3, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

The Column Address

As shown in Figure. 3, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/ write command. This allows the MPU display data to be accessed continuously. Because the column address is independent of the page address, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to re-specify both the page address and the column address.

Furthermore, as shown in Table. 6, the Column re-mapping (ADC) command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the OLED module is assembled can be minimized.

Table. 6

Segment Output	SEG0		SEG131
ADC "0"	0 (H) →	Column Address	→ 83 (H)
ADC "1"	83 (H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Figure. 3, specifies the line address relating to the common output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for SH1101A, when the common output mode is reversed. The display area is a 64-line area for the SH1101A from the display start line address.

If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. that can be performed relationship between display data RAM and address (if initial display line is 1DH).

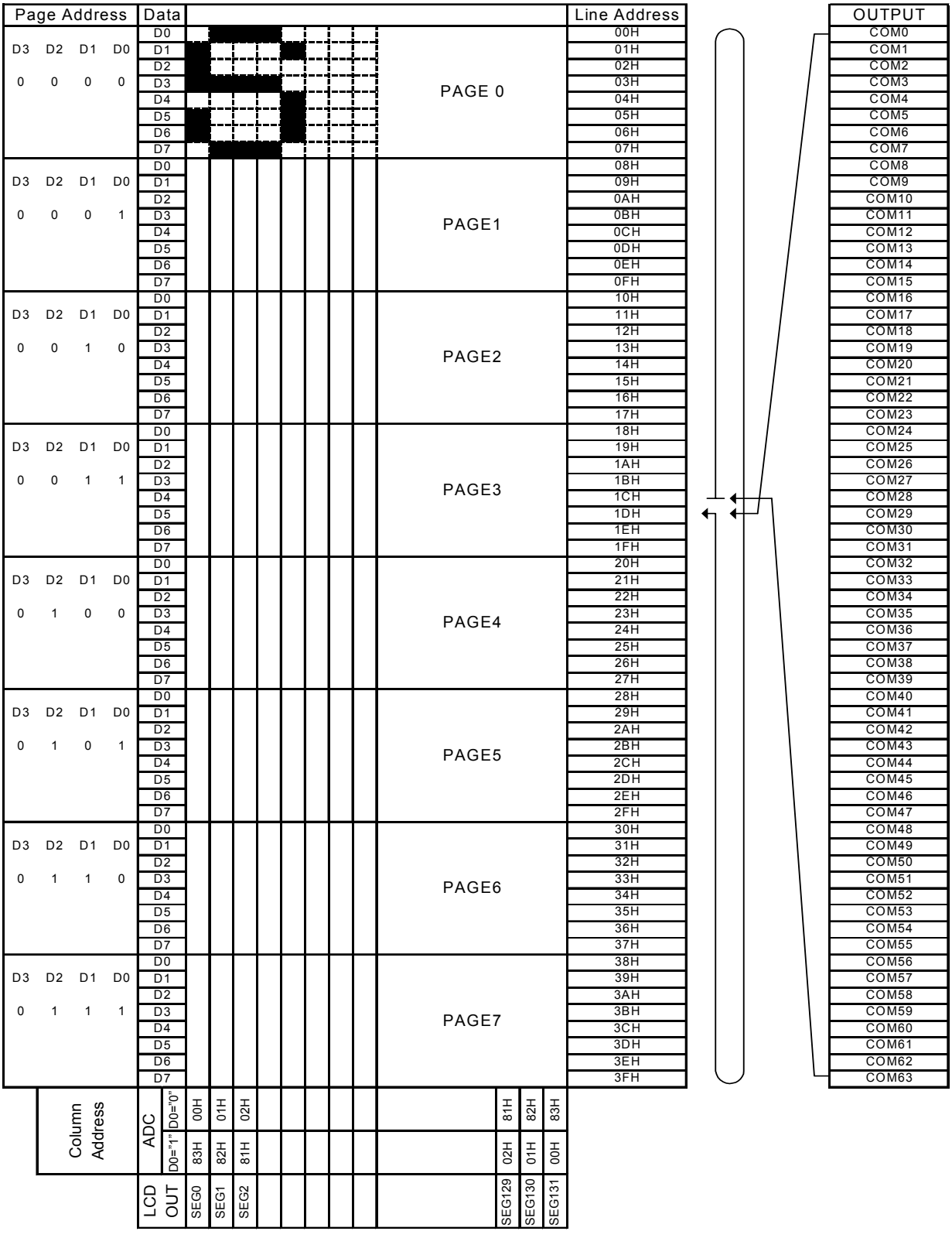


Figure 2

Appendix

The Oscillator Circuit

This is a RC type oscillator (Figure. 4) that produces the display clock. The oscillator circuit is only enabled when CLS = “H”. When CLS = “L”, the oscillation stops and the display clock is inputted through the CL terminal.

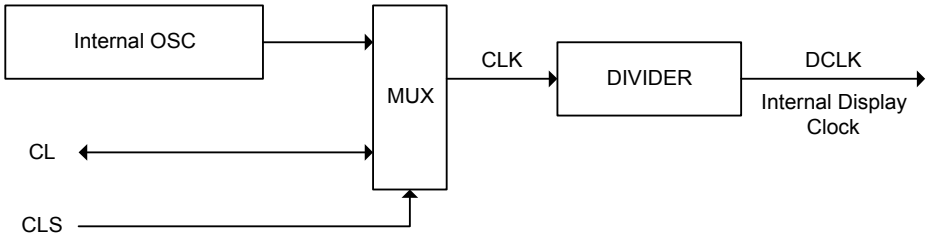


Figure. 4

DC-DC Voltage Converter

It is a switching voltage generator circuit, designed for hand held applications. In SH1101A, built-in DC-DC voltage converter accompanied with an external application circuit (shown in Figure. 5) can generate a high voltage supply V_{PP} from a low voltage supply input V_{DD2}. V_{PP} is the voltage supply to the OLED driver block.

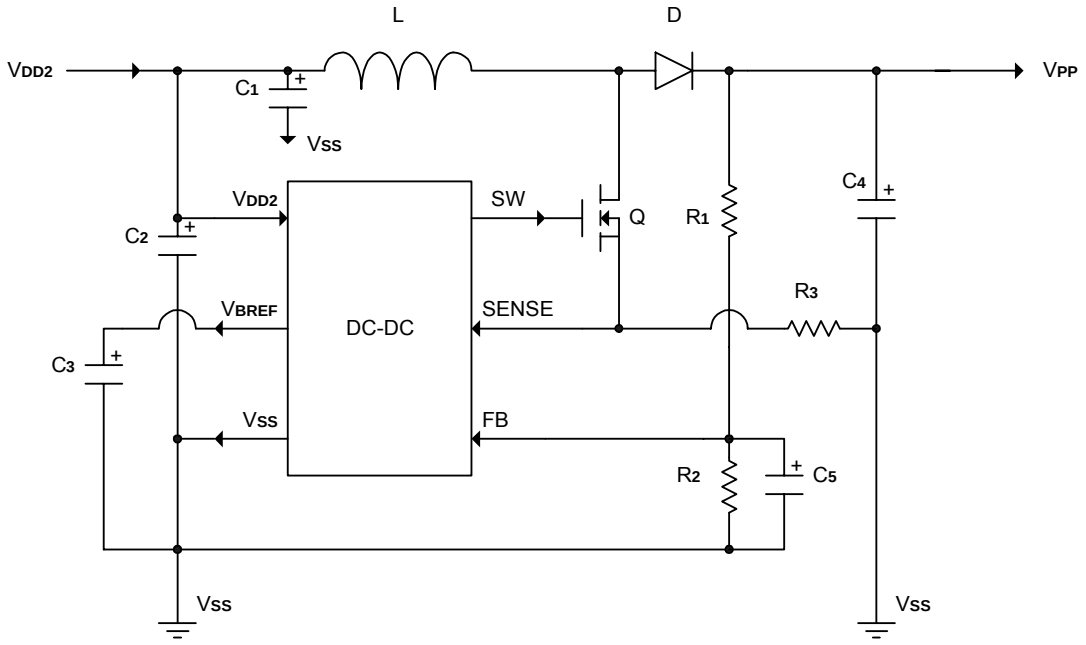


Figure. 5

$V_{PP} = (1+\frac{R1}{R2}) \times V_{BREF}$, ($R_2$: 80 - 120kΩ)

Current Control and Voltage Control

This block is used to derive the incoming power sources into different levels of internal use voltage and current. V_{PP} and V_{DD2} are external power supplies. V_{REF}, a reference voltage, which is used to derive the driving voltage for segments and commons. I_{REF} is a reference current source for segment current drivers.

Common Drivers/Segment Drivers

Segment drivers deliver 132 current sources to drive OLED panel. The driving current can be adjusted up to 320μA with 256 steps. Common drivers generate voltage scanning pulses.

Reset Circuit

When the $\overline{RES}$ input falls to "L", these reenter their default state. The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 132 X 64 Display mode.
3. Normal segment and display data column address and row address mapping (SEG0 is mapped to column address 00H and COM0 mapped to row address 00H).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM line address 00H.
6. Column address counter is set at 0.
7. Normal scanning direction of the common outputs.
8. Contrast control register is set at 80H.
9. Internal DC-DC is selected.

Commands

The SH1101A uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ ($R/\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the $R/\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.
Taking the 8080 series, microprocessor interface as an example command will explain below.
When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Set Lower Column Address: (00H - 0FH)
2. Set Higher Column Address: (10H - 1FH)

   Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

Note: Don't use any commands not mentioned above.

3 - 5. Reserved Command

These three commands are reserved for user.

6. Set Display Start Line: (40H - 7FH)

   Specifies line address (refer to Figure. 3) to determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E / $\overline{RD}$	$R/\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Appendix

7. Set Contrast Control Register: (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases.

Segment output current setting: I_{SEG} = α/256 X I_{REF} X scale factor

Where: α is contrast step; I_{REF} is reference current equals 10μA; Scale factor = 32.

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels.

When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0	I_{SEG}
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	1	0	
0	1	0	0	0	0	0	0	0	1	1	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	POR
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	
0	1	0	1	1	1	1	1	1	1	1	Large

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

8. Set Segment Re-map: (A0H - A1H)

Change the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the column address section of Figure. 3. When display data is written or read, the column address is incremented by 1 as shown in Figure. 1.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

When ADC = “L”, the right rotates (normal direction). (POR)
When ADC = “H”, the left rotates (reverse direction).

9. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = “L”, the normal display status is provided. (POR)
When D = “H”, the entire display ON status is provided.

10. Set Normal/Reverse Display: (A6H -A7H)

Reverses the display ON/OFF status without rewriting the contents of the display data RAM.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = “L”, the RAM data is high, being OLED ON potential (normal display). (POR)
When D = “H”, the RAM data is low, being OLED ON potential (reverse display)

11. Set Multiplex Ration: (Double Bytes Command)

This command switches default 64 multiplex modes to any multiplex ratio from 1 to 64. The output pads COM0-COM63 will be switched to corresponding common signal.

- Multiplex Ration Mode Set: (A8H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

- Multiplex Ration Data Set: (00H - 3FH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio
0	1	0	*	*	0	0	0	0	0	0	1
0	1	0	*	*	0	0	0	0	1	0	2
0	1	0	*	*	0	0	0	0	1	1	3
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	63
0	1	0	*	*	1	1	1	1	1	1	64 (POR)

12. Set DC-DC OFF/ON: (Double Bytes Command)

This command is to control the DC-DC voltage converter. The converter will be turned on by issuing this command then display ON command. The panel display must be off while issuing this command.

- DC-DC Control Mode Set: (ADH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1

- DC-DC ON/OFF Mode Set: (8AH - 8BH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	1	0	1	D

When D = “L”, DC-DC is disable.
When D = “H”, DC-DC will be turned on when display on. (POR)

Table. 7

DC-DC STATUS	DISPLAY ON/OFF STATUS	Description
0	0	Sleep mode
0	1	External V_{PP} must be used.
1	0	Sleep mode
1	1	Built-in DC-DC is used, Normal Display

13. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = “L”, Display OFF OLED. (POR)
When D = “H”, Display ON OLED.
When the display OFF command is executed, power saver mode will be entered.

Sleep mode:

This mode stops every operation of the OLED display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and DC-DC circuit.
(2) Stops the OLED drive and outputs HZ as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

14. Set Page Address: (B0H - B7H)

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

Note: Don’t use any commands not mentioned above for user.

15. Set Common Output Scan Direction: (C0H - C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

When D = “L”, Scan from COM0 to COM [N -1]. (POR)
When D = “H”, Scan from COM [N -1] to COM0.

16. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-63 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (64-16), so the second byte should be 100000.

- Display Offset Mode Set: (D3H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

- Display Offset Data Set: (00H~3FH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	*	*	0	0	0	0	0	0	0 (POR)
0	1	0	*	*	0	0	0	0	1	0	1
0	1	0	*	*	0	0	0	0	1	1	2
0	1	0					:				:
0	1	0	*	*	1	1	1	1	1	0	62
0	1	0	*	*	1	1	1	1	1	1	63

Note: “*” stands for “Don’t care”

17. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio (Value from 1 to 16) used to divide the oscillator frequency. POR is 1. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

■ Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

■ Divide Ratio/Oscillator Frequency Data Set: (00H - 3FH)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

A_3 - A_0 defines the divide ration of the display clocks (DCLK). Divide Ration = A[3:0]+1.

A_3	A_2	A_1	A_0	Divide Ration
0	0	0	0	1 (POR)
		:		:
1	1	1	1	16

A_7 - A_4 sets the oscillator frequency. Oscillator frequency increase with the value of A[7:4] and vice versa.

A_7	A_6	A_5	A_4	Oscillator Frequency of $f$osc
0	0	0	0	-25%
0	0	0	1	-20%
0	0	1	0	-15%
0	0	1	1	-10%
0	1	0	0	-5%
0	1	0	1	$f$osc (POR)
0	1	1	0	+5%
0	1	1	1	+10%
1	0	0	0	+15%
1	0	0	1	+20%
1	0	1	0	+25%
1	0	1	1	+30%
1	1	0	0	+35%
1	1	0	1	+40%
1	1	1	0	+45%
1	1	1	1	+50%

18. Set Dis-charge/Pre-charge Period: (Double Bytes Command)

This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. POR is 2 DCLKs.

■ Pre-charge Period Mode Set: (D9H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1

■ Dis-charge/Pre-charge Period Data Set: (00H - FFH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Pre-charge Period Adjust: (A3 - A0)

A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

Dis-charge Period Adjust: (A_7 - A_4)

A_7	A_6	A_5	A_4	Dis-charge Period
0	0	0	0	INVALID
0	0	0	1	1 DCLKs
0	0	1	0	2 DCLKs (POR)
		:		:
1	1	1	0	14 DCLKs
1	1	1	1	15 DCLKs

19. Set Common pads hardware configuration: (Double Bytes Command)

This command is to set the common signals pad configuration (sequential or alternative) to match the OLED panel hardware layout

■ Common Pads Hardware Configuration Mode Set: (DAH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	0

■ Sequential/Alternative Mode Set: (02H - 12H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	D	0	0	1	0

When D = “L”, Sequential.

COM31, 30 - 1, 0	SEG0, 1 - 130, 131	COM32, 33 - 62, 63

When D = “H”, Alternative. (POR)

COM62, 60 - 2, 0	SEG0, 1 - 130, 131	COM1, 3 - 61, 63

20. Set VCOM Deselect Level: (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

■ VCOM Deselect Level Mode Set: (DBH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

■ VCOM Deselect Level Data Set: (00H - FFH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

$V_{COM} = \beta \times V_{REF} = (0.430 + A[7:0] \times 0.006415) \times V_{REF}$

A[7:0]	β	A[7:0]	β
00H	0.430	20H	
01H		21H	
02H		22H	
03H		23H	
04H		24H	
05H		25H	
06H		26H	
07H		27H	
08H		28H	
09H		29H	
0AH		2AH	
0BH		2BH	
0CH		2CH	
0DH		2DH	
0EH		2EH	
0FH		2FH	
10H		30H	
11H		31H	
12H		32H	
13H		33H	
14H		34H	
15H		35H	0.770 (POR)
16H		36H	
17H		37H	
18H		38H	
19H		39H	
1AH		3AH	
1BH		3BH	
1CH		3CH	
1DH		3DH	
1EH		3EH	
1FH		3FH	
40H - FFH	1		

21. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. Once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

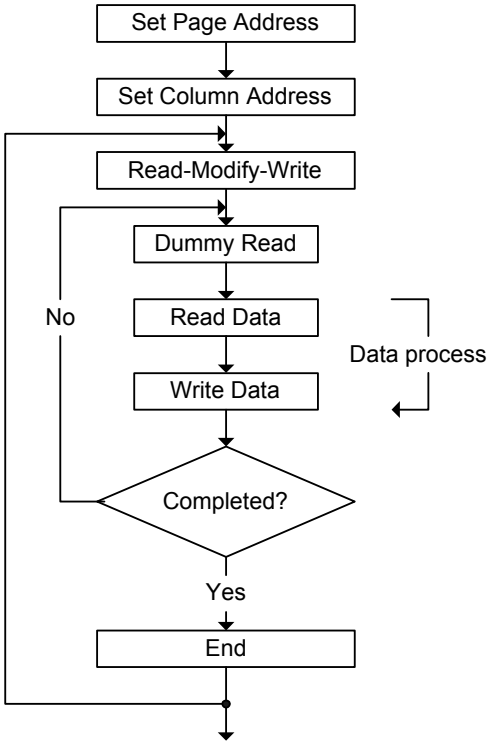


Figure. 6

22. End: (EEH)

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued.)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

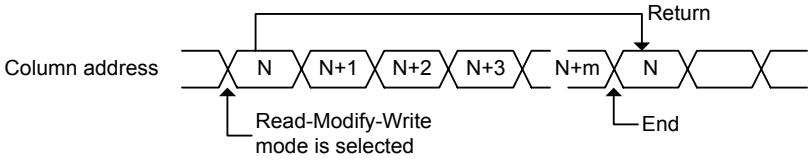


Figure. 7

Appendix

23. NOP: (E3H)

Non-Operation Command.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

24. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

25. Read Status

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	*	*	*	0	0	0

BUSY: When high, the SH1101A is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ON/OFF: Indicates whether the display is on or off. When goes low the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

26. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register. (POR = 00H)
2. Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register. (POR = 10H)
3. Reserved Command	0	1	0	0	0	1	0	0	1	0	0	Reserved
4. Reserved Command	0	1	0	0	0	1	0	0	1	1	0	Reserved
5. Reserved Command	0	1	0	0	0	1	0	1	1	1	D	Reserved
6. Set Display Start Line	0	1	0	0	1	Line address						Specifies RAM display line for COM0. (POR = 40H)
7. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (POR = 80H)
Contrast Data Register Set	0	1	0	Contrast Data								
8. Set Segment Re-map (ADC)	0	1	0	1	0	1	0	0	0	0	ADC	The right (0) or left (1) rotation. (POR = A0H)
9. Set Entire Display OFF/ON	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (POR = A4H)
10. Set Normal/ Reverse Display	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (POR = A6H)
11. Multiplex Ration Mode Set	0	1	0	1	0	1	0	1	0	0	0	This command switches default 63 multiplex mode to any multiplex ratio from 1 to 64. (POR = 3FH)
Multiplex Ration Data Set	0	1	0	*	*	Multiplex Ratio						
12. DC-DC Control Mode Set	0	1	0	1	0	1	0	1	1	0	1	This command is to control the DC-DC voltage DC-DC will be turned on when display on converter (1) or DC-DC OFF (0). (POR = 8BH)
DC-DC ON/OFF Mode Set	0	1	0	1	0	0	0	1	0	1	D	

Command Table (Continued)

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
13. Display OFF/ON	0	1	0	1	0	1	0	1	1	1	D	Turns on OLED panel (1) or turns off (0). (POR = AEH)
14. Set Page Address	0	1	0	1	0	1	1	Page Address				Specifies page address to load display RAM data to page address register. (POR = B0H)
15. Set Common Output Scan Direction	0	1	0	1	1	0	0	D	*	*	*	Scan from COM0 to COM [N - 1] (0) or Scan from COM [N -1] to COM0 (1). (POR = C0H)
16. Display Offset Mode Set	0	1	0	1	1	0	1	0	0	1	1	This is a double byte command which specifies the mapping of display start line to one of COM0-63. (POR = 00H)
Display Offset Data Set	0	1	0	*	*	COMx						
17. Set Display Divide Ratio/Oscillator Frequency Mode Set	0	1	0	1	1	0	1	0	1	0	1	This command is used to set the frequency of the internal display clocks. (POR = 50H)
Divide Ratio/Oscillator Frequency Data Set	0	1	0	Oscillator Frequency				Divide Ratio				
18. Dis-charge / Pre-charge Period Mode Set	0	1	0	1	1	0	1	1	0	0	1	This command is used to set the duration of the dis-charge and pre-charge period. (POR = 22H)
Dis-charge /Pre-charge Period Data Set	0	1	0	Dis-charge Period				Pre-charge Period				
19. Common Pads Hardware Configuration Mode Set	0	1	0	1	1	0	1	1	0	1	0	This command is to set the common signals pad configuration. (POR = 12H)
Sequential/Alternative Mode Set	0	1	0	0	0	0	D	0	0	1	0	
20. VCOM Deselect Level Mode Set	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (POR = 35H)
VCOM Deselect Level Data Set	0	1	0	VCOM (β X V_{REF})								
21. Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
22. End	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
23. NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
24. Write Display Data	1	1	0	Write RAM data								
25. Read Status	0	0	1	BUSY	ON/ OFF	*	*	*	0	0	0	
26. Read Display Data	1	0	1	Read RAM data								

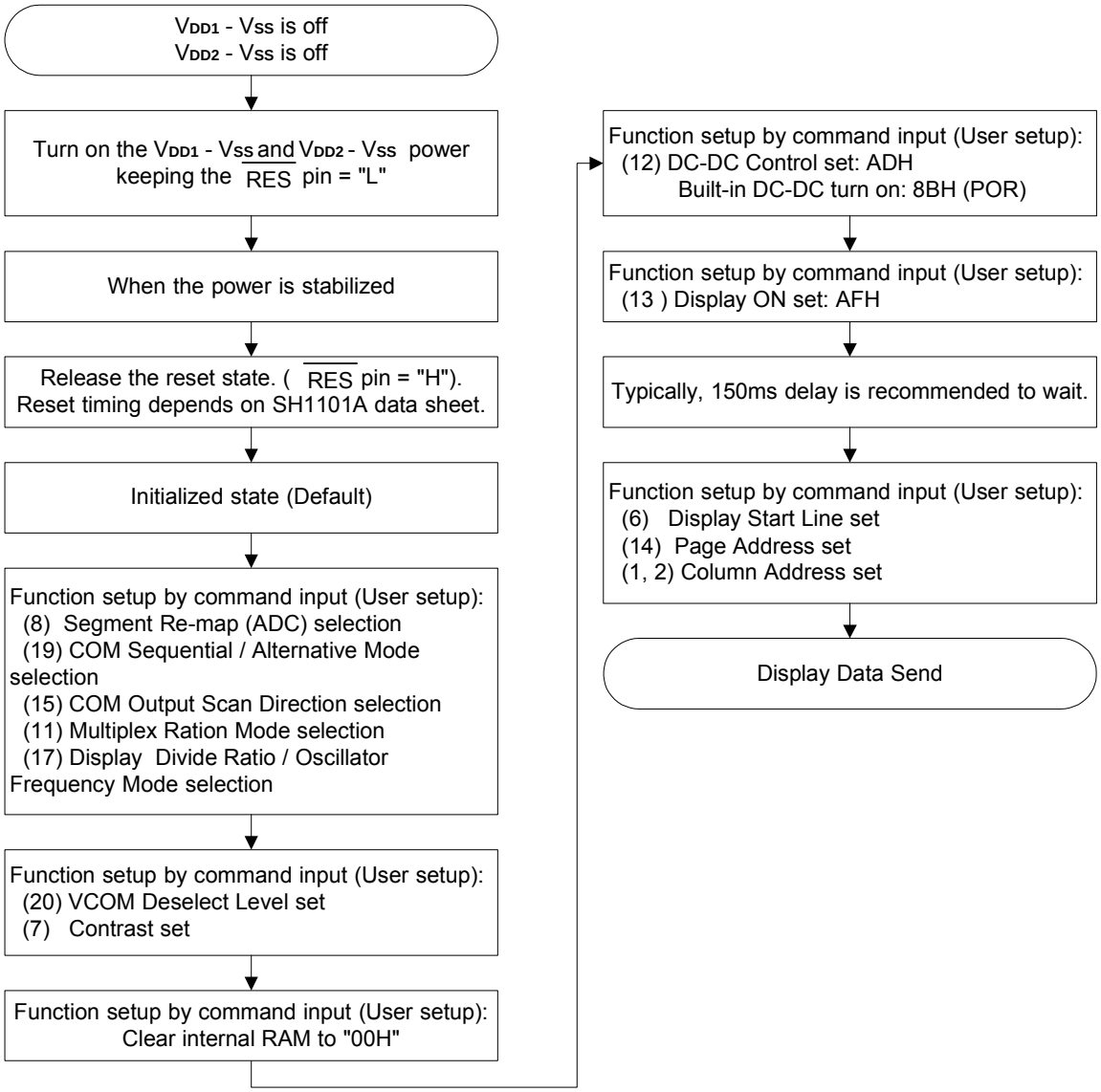
Note: Do not use any other command, or the system malfunction may result.

Command Description

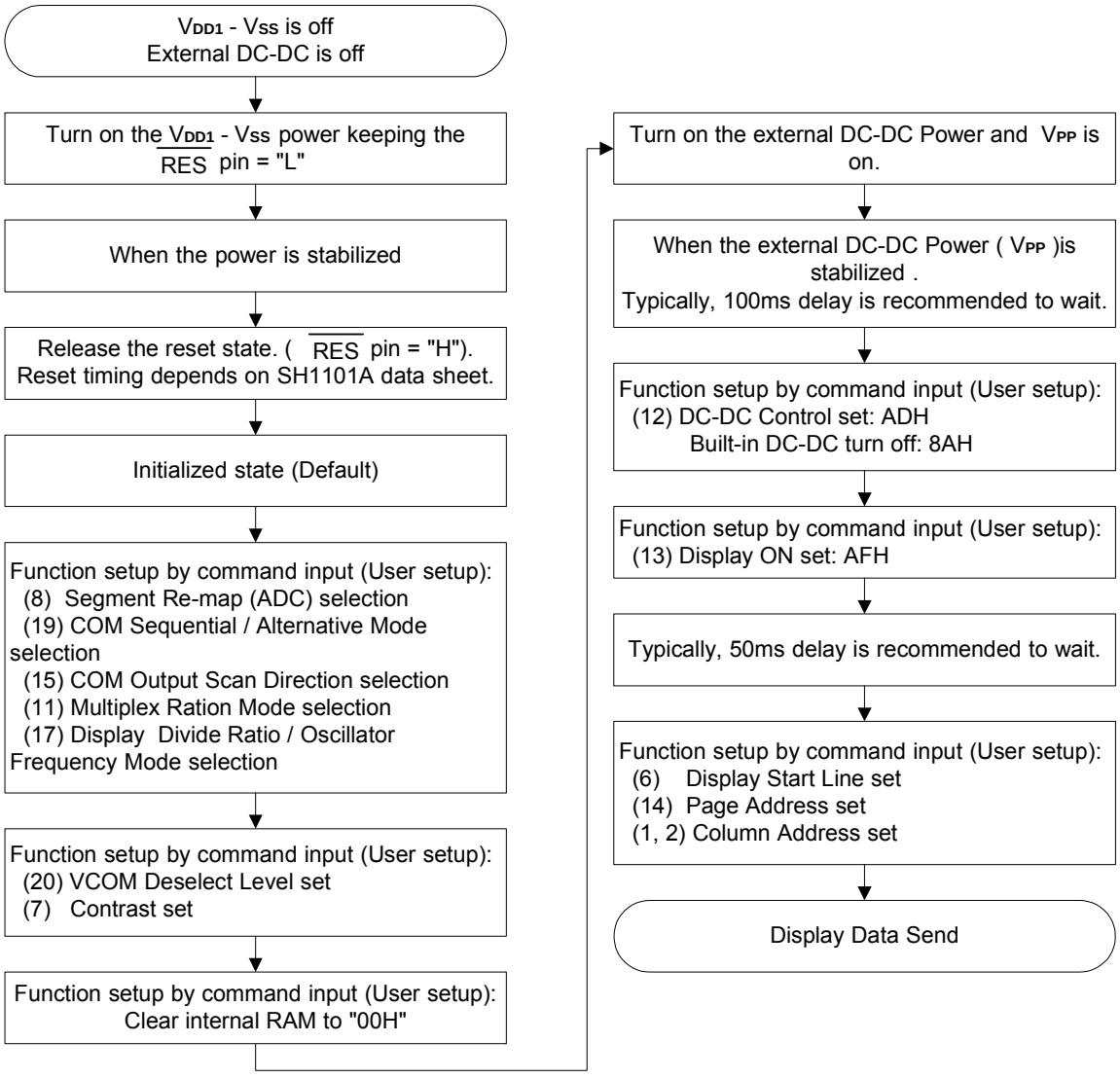
Instruction Setup: Reference

1. Power On and Initialization

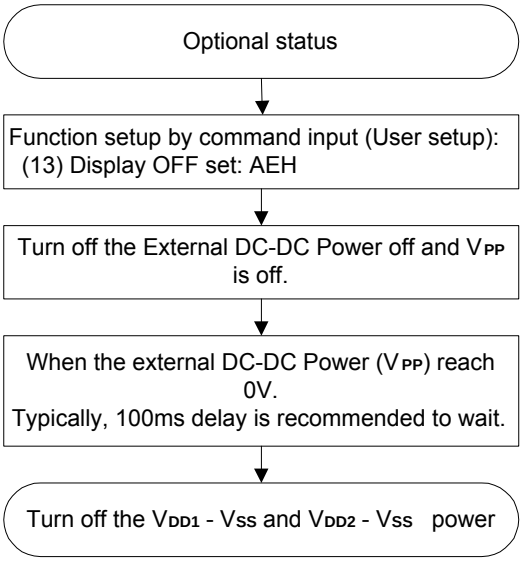
1.1. When the built-in DC-DC pump power is being used immediately after turning on the power:



1.2. When the external DC-DC pump power is being used immediately after turning on the power:



2. Power Off


Optional status
Function setup by command input (User setup):
(13) Display OFF set: AEH
Turn off the External DC-DC Power off and VPP is off.
When the external DC-DC Power (VPP) reach 0V.
Typically, 100ms delay is recommended to wait.
Turn off the VDD1 - Vss and VDD2 - Vss power

Absolute Maximum Rating*

DC Supply Voltage (V_{DD1}, V_{DD2}) . . . . . -0.3V to +3.6V

DC Supply Voltage (V_{PP}) . . . . . -0.3V to +18V

Input Voltage . . . . . -0.3V to V_{DD1} + 0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (V_{SS} = 0V, V_{DD1} = 2.4 - 3.5V T_A =+25°C, unless otherwise specified)

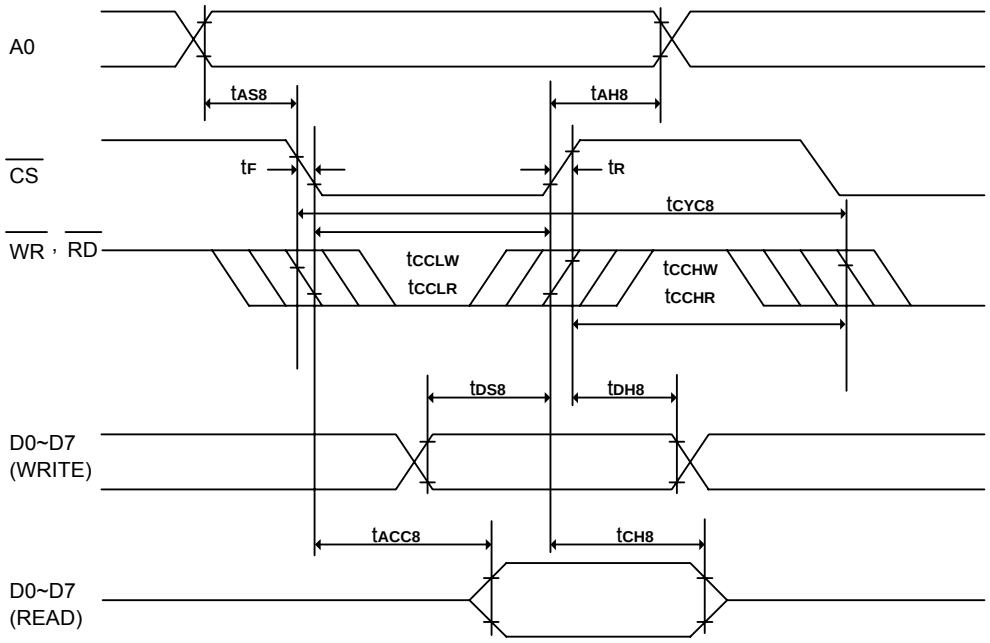
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD1}	Operating voltage	2.4	-	3.5	V	Normal mode
		1.65	-	3.5		Low voltage mode
V_{DD2}	Operating voltage	2.4	-	3.5	V	
V_{PP}	OLED Operating voltage	7.0	-	16.0	V	Normal mode
		7.0	-	9.0		Low voltage mode
V_{BREF}	Internal voltage reference	-5%	1.26*	+5%	V	With one 1μF capacitor, 1.26V is the reference value.
I_{DD1}	Dynamic current consumption 1	-	110	160	μA	V_{DD1} = 3V, V_{DD2} = 3V, I_{REF} = 10μA, Contrast α = 256, Bulid-in DC-DC OFF, Display ON, display data = All ON, No panel attached.
I_{DD2}	Dynamic current consumption 2	-	190	285	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -10μA, Contrast α = 256, Bulid-in DC-DC ON, Display ON, Display data = All ON, No panel attached.
I_{PP}	OLED dynamic current consumption	-	550	825	μA	V_{DD1} = 3V, V_{DD2} = 3V, V_{PP} = 12V, I_{REF} = -10μA, Contrast α = 256, Display ON, All ON, No panel attached.
I_{SP}	Sleep mode current consumption in V_{DD1} & V_{DD2}	-	0.01	5	μA	During sleep, T_A = +25°C, V_{DD1} = 3V, V_{DD2} = 3V.
	Sleep mode current consumption in V_{PP}	-	0.01	5	μA	During sleep, T_A = +25°C, V_{PP} = 12V.
I_{SEG}	Segment output current	-308	-320	-342	μA	V_{DD1} = 3V, V_{PP} = 12V, I_{REF} = -10μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 256.
		-	-220	-	μA	V_{DD1} = 3V, V_{PP} = 12V, I_{REF} = -10μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 176.
		-	-120	-	μA	V_{DD1} = 3V, V_{PP} = 12V, I_{REF} = -10μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 96.
		-	-20	-	μA	V_{DD1} = 3V, V_{PP} = 12V, I_{REF} = -10μA, R_{LOAD} = 20kΩ, Display ON. Contrast α = 16.
ΔI_{SEG1}	Segment output current uniformity	-	-	±3	%	ΔI_{SEG1} = (I_{SEG} - I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [0:131] at contrast α = 256.
ΔI_{SEG2}	Adjacent segment output current uniformity	-	-	±2	%	ΔI_{SEG2} = (I_{SEG} [N] - I_{SEG} [N+1])/(I_{SEG} [N] + I_{SEG} [N+1]) X 100% I_{SEG} [0:131] at contrast α = 256.

DC Characteristics (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.8 X V_{DD1}	-	V_{DD1}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, C86, P/S and $\overline{RES}$.
V_{ILC}	Low-level input voltage	Vss	-	0.2 X V_{DD1}	V	
V_{OHC}	High-level output voltage	0.8 X V_{DD1}	-	V_{DD1}	V	I_{OH} = -0.5mA (D0 - D7, and CL).
V_{OLC}	Low -level output voltage	Vss	-	0.2 X V_{DD1}	V	I_{OL} = 0.5mA (D0 - D7, and CL).
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD1} or Vss (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, C86, P/S and $\overline{RES}$).
I_{HZ}	HZ leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance.
f_{OSC}	Oscillation frequency	315	360	420	kHz	T_A = +25°C.
f_{FRM}	Frame frequency for 64 Commons	-	104	-	Hz	When f_{OSC} = 360kHz, Divide ratio = 1, common width = 54 DCLKs.

AC Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



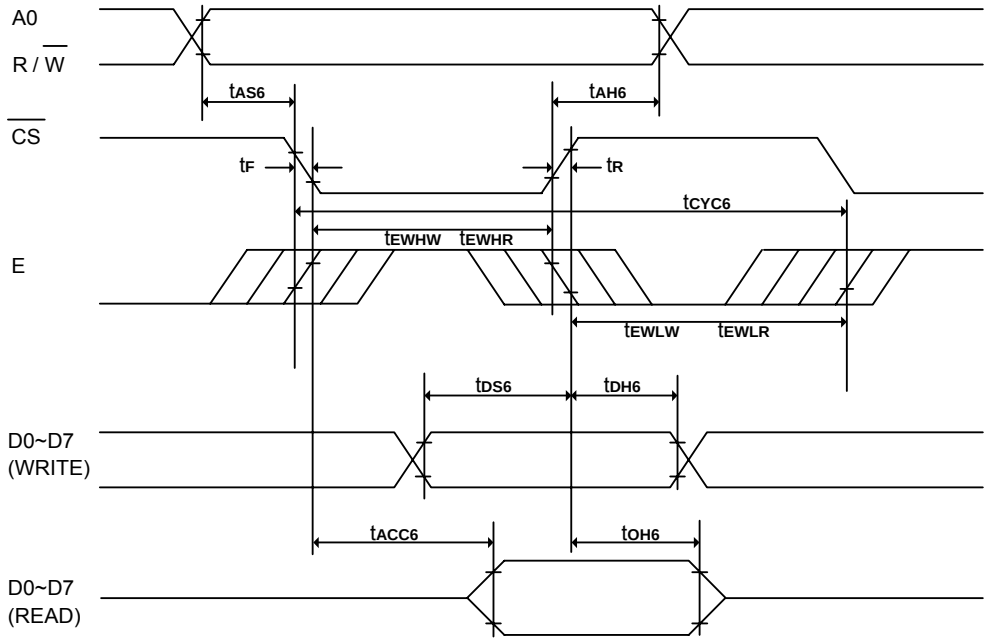
(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DH8}	Data hold time	15	-	-	ns	
t_{CH8}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	100	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	120	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	100	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(VDD1 = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	600	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	80	-	-	ns	
t_{DH8}	Data hold time	30	-	-	ns	
t_{CH8}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	280	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	200	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	240	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	200	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



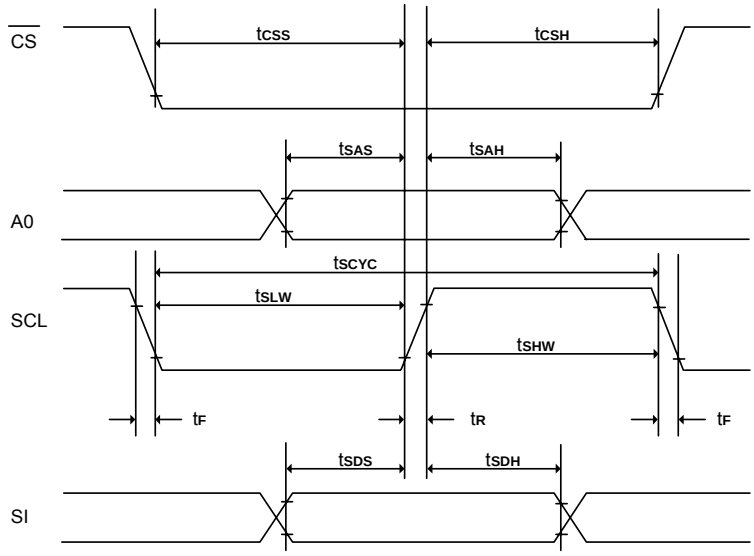
(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DH6}	Data hold time	15	-	-	ns	
t_{OH6}	Output disable time	10	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

(V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	600	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	80	-	-	ns	
t_{DH6}	Data hold time	30	-	-	ns	
t_{OH6}	Output disable time	20	-	140	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	280	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	200	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	240	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	200	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(3) System buses Write characteristics 3(For the Serial Interface MPU)



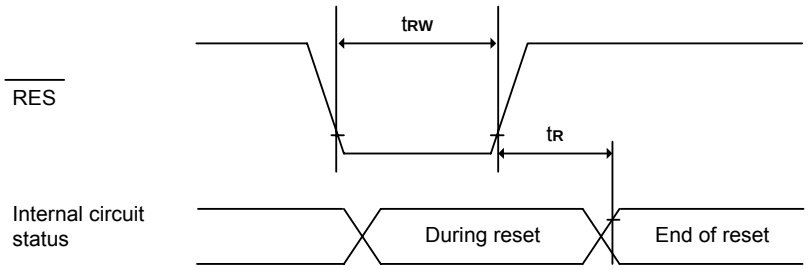
(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	250	-	-	ns	
t_{SAS}	Address setup time	150	-	-	ns	
t_{SAH}	Address hold time	150	-	-	ns	
t_{SDS}	Data setup time	100	-	-	ns	
t_{SDH}	Data hold time	100	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	120	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	60	-	-	ns	
t_{SHW}	Serial clock H pulse width	100	-	-	ns	
t_{SLW}	Serial clock L pulse width	100	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	

. (V_{DD1} = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	500	-	-	ns	
t_{SAS}	Address setup time	300	-	-	ns	
t_{SAH}	Address hold time	300	-	-	ns	
t_{SDS}	Data setup time	200	-	-	ns	
t_{SDH}	Data hold time	200	-	-	ns	
t_{CSS}	$\overline{CS}$ setup time	240	-	-	ns	
t_{CSH}	$\overline{CS}$ hold time time	120	-	-	ns	
t_{SHW}	Serial clock H pulse width	200	-	-	ns	
t_{SLW}	Serial clock L pulse width	200	-	-	ns	
t_R	Rise time	-	-	30	ns	
t_F	Fall time	-	-	30	ns	

(4) Reset Timing



(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	1.0	μs	
t_{RW}	Reset low pulse width	5.0	-	-	μs	

(V_{DD1} = 1.65 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset time	-	-	2.0	μs	
t_{RW}	Reset low pulse width	10.0	-	-	μs	

Application Circuit (for reference only)

Reference Connection to MPU:

1. 8080 series interface: (Internal oscillator, External V_{PP})

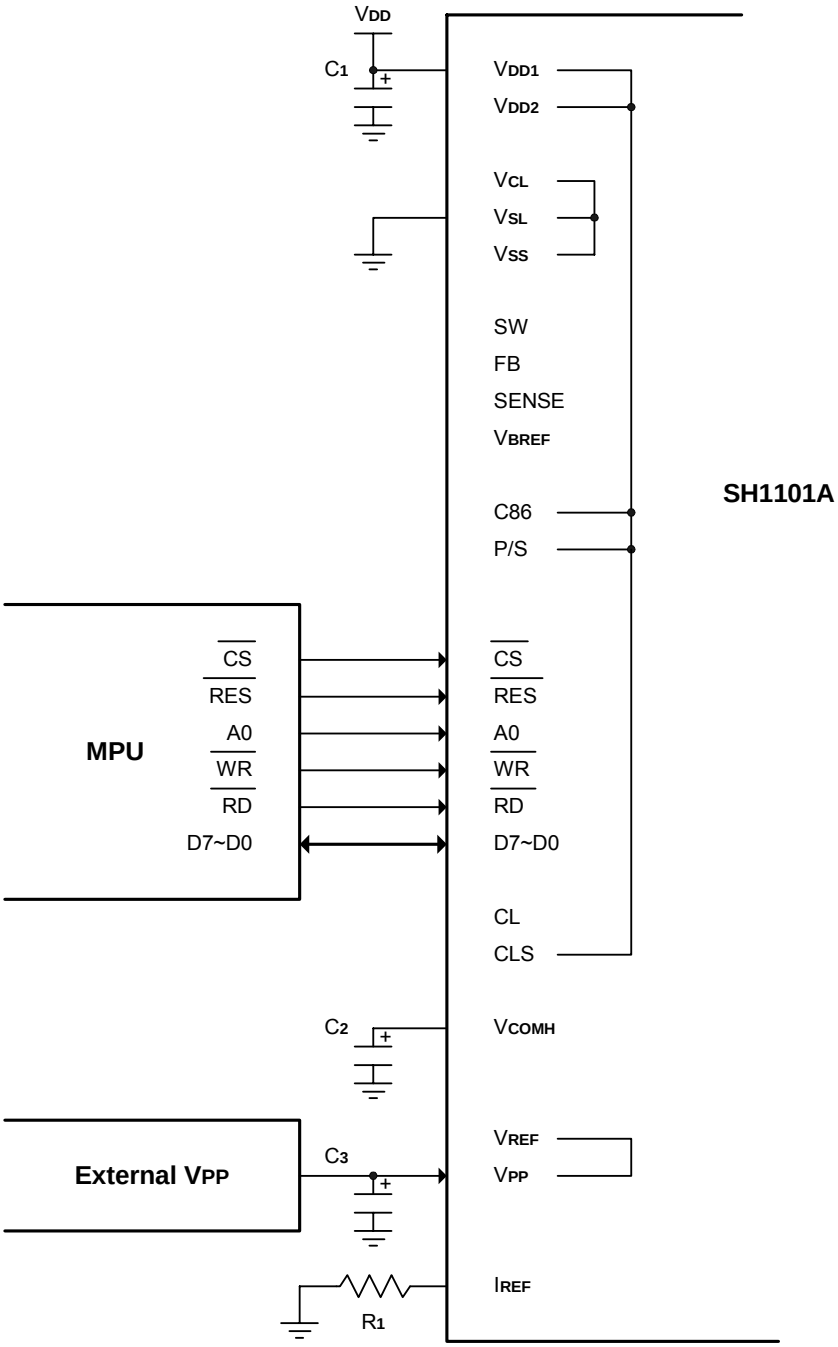


Figure. 8

Note:

C_1 - C_3: 4.7μF.

R_1: about 910kΩ, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

2. 6800 Series Interface: (Internal oscillator, Built-in DC-DC)

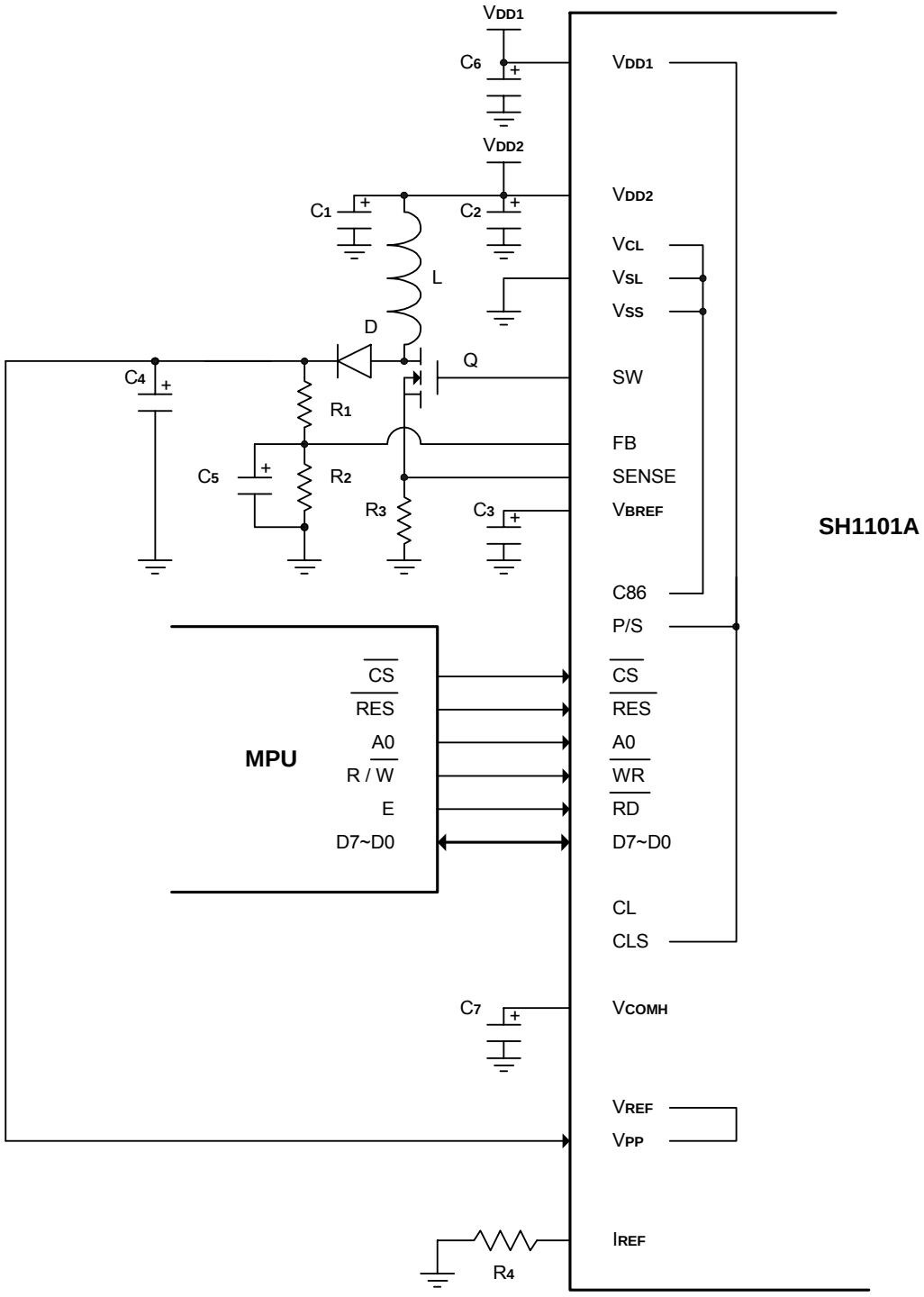


Figure. 9

Note:
L, D, Q, R1, R2, R3, C1 - C6: Please refer to following description of DC-DC module.
C6, C7: 4.7μF
R3: about 910kΩ, R4 = (Voltage at IREF - VSS)/IREF

Appendix

3. Serial Interface: (External oscillator, External V_{PP})

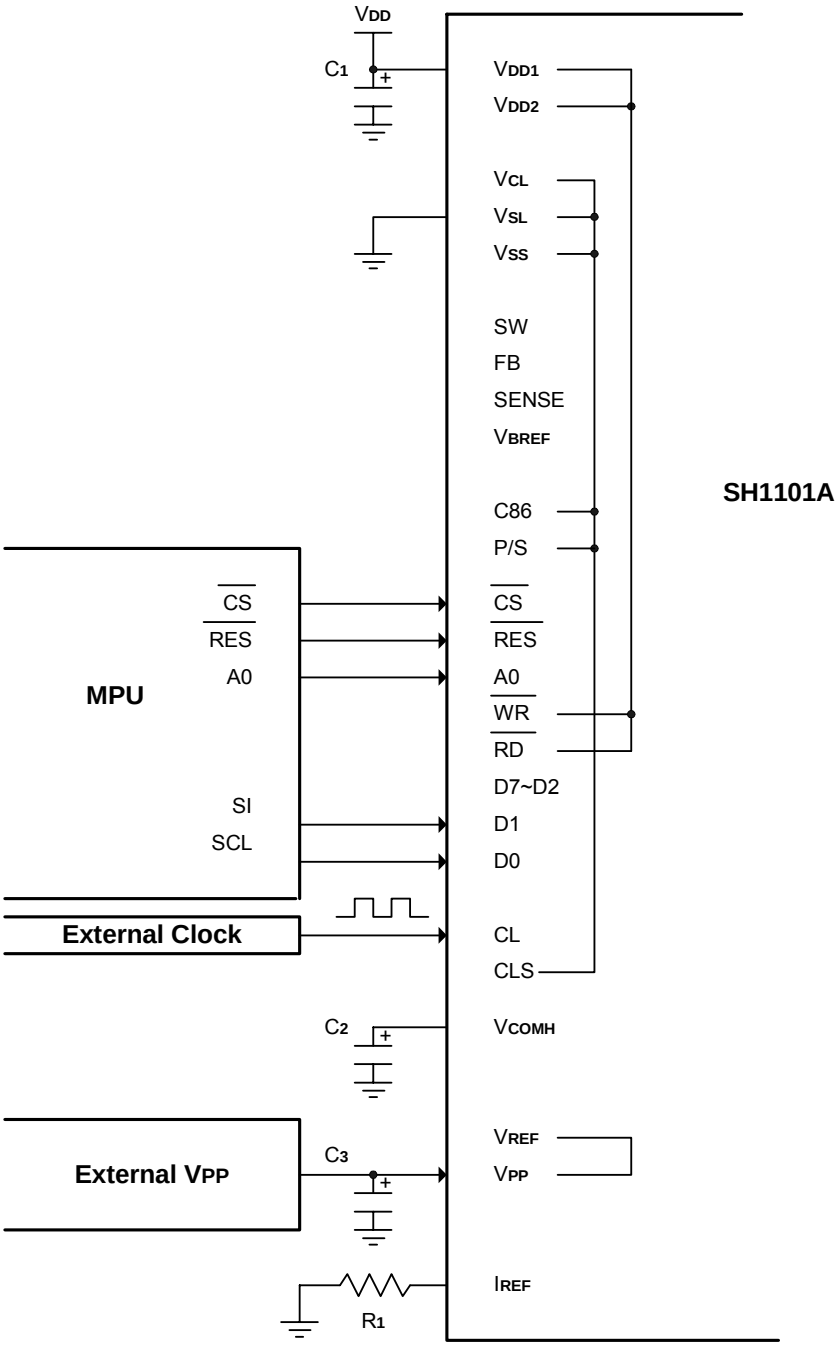


Figure. 10

Note:

C_1 - C_3: 4.7μF

R_1: about 910kΩ, R_1 = (Voltage at I_{REF} - V_{SS})/I_{REF}

DC-DC:

Below application circuit is an example for the input voltage of 3V V_{DD2} to generate V_{PP} of about 12V@10mA-25mA application.

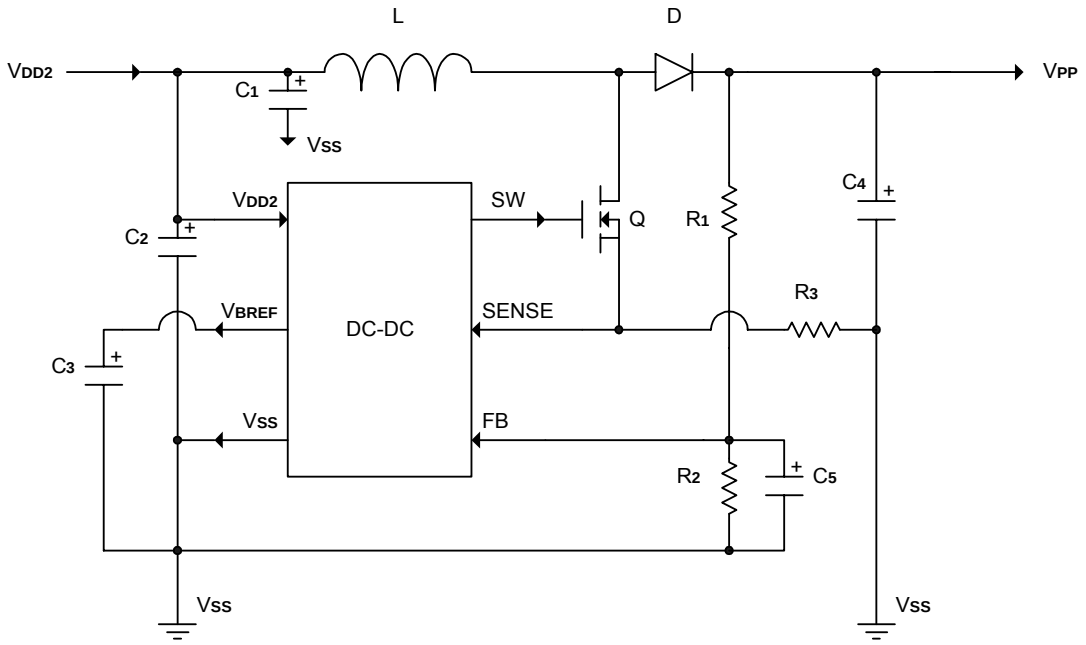
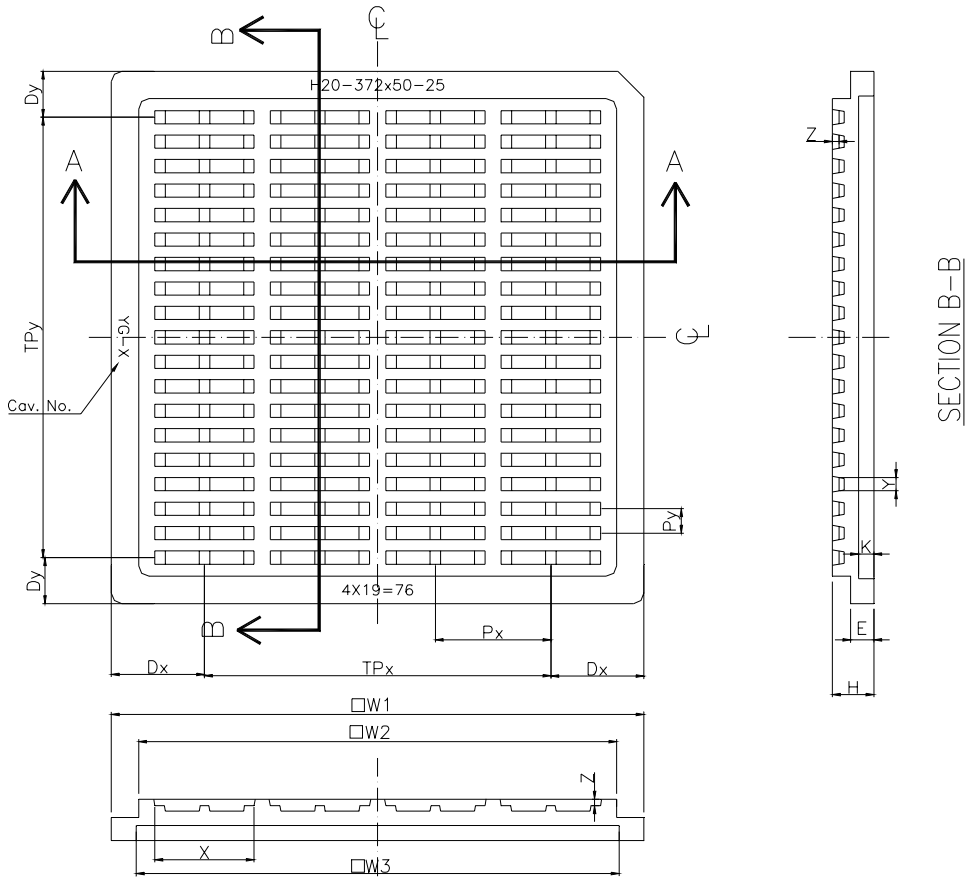


Figure. 11

Symbol	Value	Recommendation
L	10μH	LQH3C100K24
D	SCHOTTKY DIODE	20V@0.5A, MBR0520
Q	MOSFET	N-FET with low $R_{DS(ON)}$ and low V_{TH}, MGSF1N02LT1
R_1	930kΩ	1%, 1/8W
R_2	110kΩ	1%, 1/8W
R_3	0.12Ω	1%, 1/2W
C_1	1 - 10μF	Low ESR/6.3V
C_2	0.1 - 1μF	Ceramic/16V
C_3	1μF	Ceramic/16V
C_4	6.8μF	Low ESR/16V
C_5	1000pF	Ceramic/16V

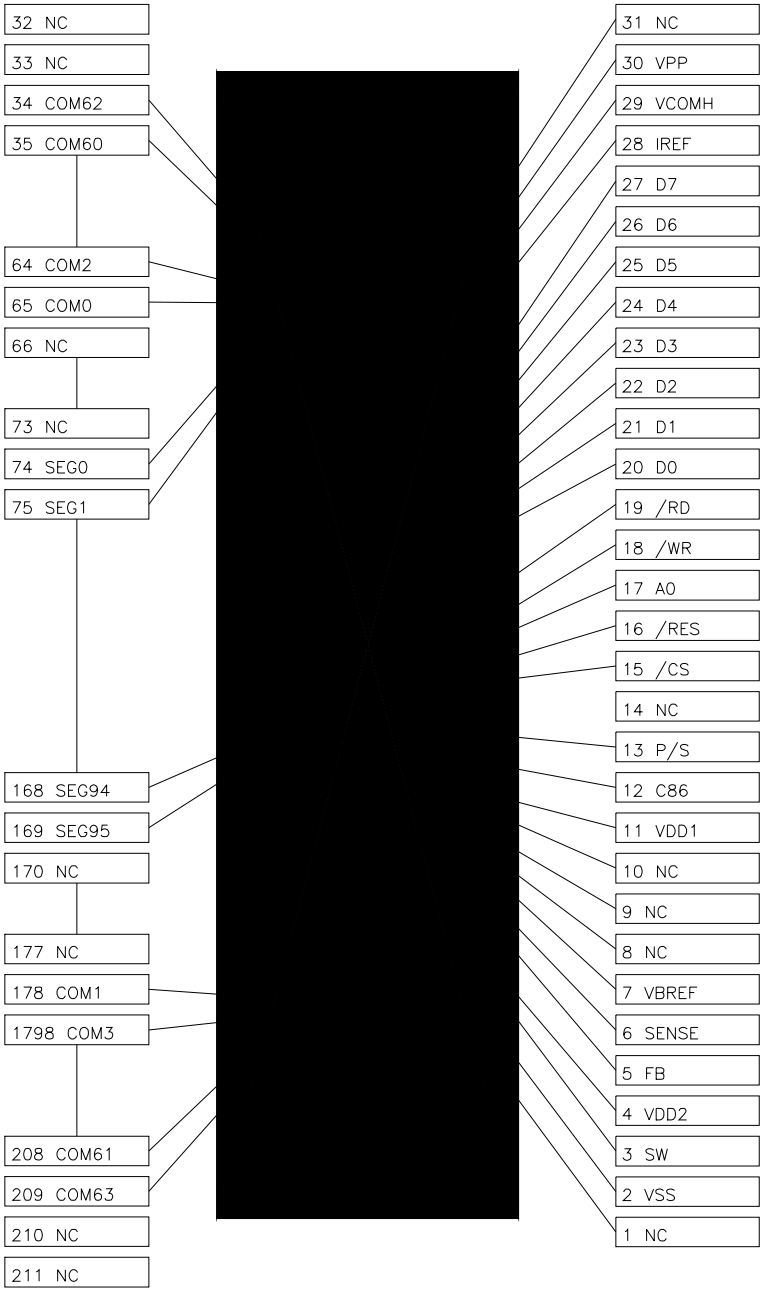
Tray Information



	Spec
	mm (mil)
W1	50.70±0.05 (1996)
W2	45.50±0.10 (1791)
W3	45.95±0.10 (1809)
H	3.95±0.05 (156)
E	2.20±0.05 (87)
K	1.45±0.10 (57)
Dx	8.87±0.05 (349)
TPx	32.97±0.10 (1298)
Dy	4.38±0.05 (172)
TPy	41.94±0.10 (1651)
Px	10.99±0.05 (433)
Py	2.33±0.05 (92)
X	9.45±0.05 (372)
Y	1.26±0.05 (50)
Z	0.63±0.05 (25)
N	76(pocket number)

Appendix

SH1101A-TCP03 TCP Pin Layout



(Copper Side View)

SH1101A-TCP03 TCP Pin Assignment (Total: 211 pins)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
1	NC	41	COM48	81	SEG7	121	SEG47
2	V_{SS}	42	COM46	82	SEG8	122	SEG48
3	SW	43	COM44	83	SEG9	123	SEG49
4	V_{DD2}	44	COM42	84	SEG10	124	SEG50
5	FB	45	COM40	85	SEG11	125	SEG51
6	SENSE	46	COM38	86	SEG12	126	SEG52
7	V_{BREF}	47	COM36	87	SEG13	127	SEG53
8	NC	48	COM34	88	SEG14	128	SEG54
9	NC	49	COM32	89	SEG15	129	SEG55
10	NC	50	COM30	90	SEG16	130	SEG56
11	V_{DD1}	51	COM28	91	SEG17	131	SEG57
12	C86	52	COM26	92	SEG18	132	SEG58
13	P/S	53	COM24	93	SEG19	133	SEG59
14	NC	54	COM22	94	SEG20	134	SEG60
15	$\overline{CS}$	55	COM20	95	SEG21	135	SEG61
16	$\overline{RES}$	56	COM18	96	SEG22	136	SEG62
17	A0	57	COM16	97	SEG23	137	SEG63
18	$\overline{WR}$	58	COM14	98	SEG24	139	SEG64
19	$\overline{RD}$	59	COM12	99	SEG25	139	SEG65
20	D0	60	COM10	100	SEG26	140	SEG66
21	D1	61	COM8	101	SEG27	141	SEG67
22	D2	62	COM6	102	SEG28	142	SEG68
23	D3	63	COM4	103	SEG29	143	SEG69
24	D4	64	COM2	104	SEG30	144	SEG70
25	D5	65	COM0	105	SEG31	145	SEG71
26	D6	66	NC	106	SEG32	146	SEG72
27	D7	67	NC	107	SEG33	147	SEG73
28	I_{REF}	68	NC	108	SEG34	148	SEG74
29	V_{COMH}	69	NC	109	SEG35	149	SEG75
30	V_{PP}	70	NC	110	SEG36	150	SEG76
31	NC	71	NC	111	SEG37	151	SEG77
32	NC	72	NC	112	SEG38	152	SEG78
33	NC	73	NC	113	SEG39	153	SEG79
34	COM62	74	SEG0	114	SEG40	154	SEG80
35	COM60	75	SEG1	115	SEG41	155	SEG81
36	COM58	76	SEG2	116	SEG42	156	SEG82
37	COM56	77	SEG3	117	SEG43	157	SEG83
38	COM54	78	SEG4	118	SEG44	158	SEG84
39	COM52	79	SEG5	119	SEG45	159	SEG85
40	COM50	80	SEG6	120	SEG46	160	SEG86

SH1101A-TCP03 TCP Pin Assignment (continued)

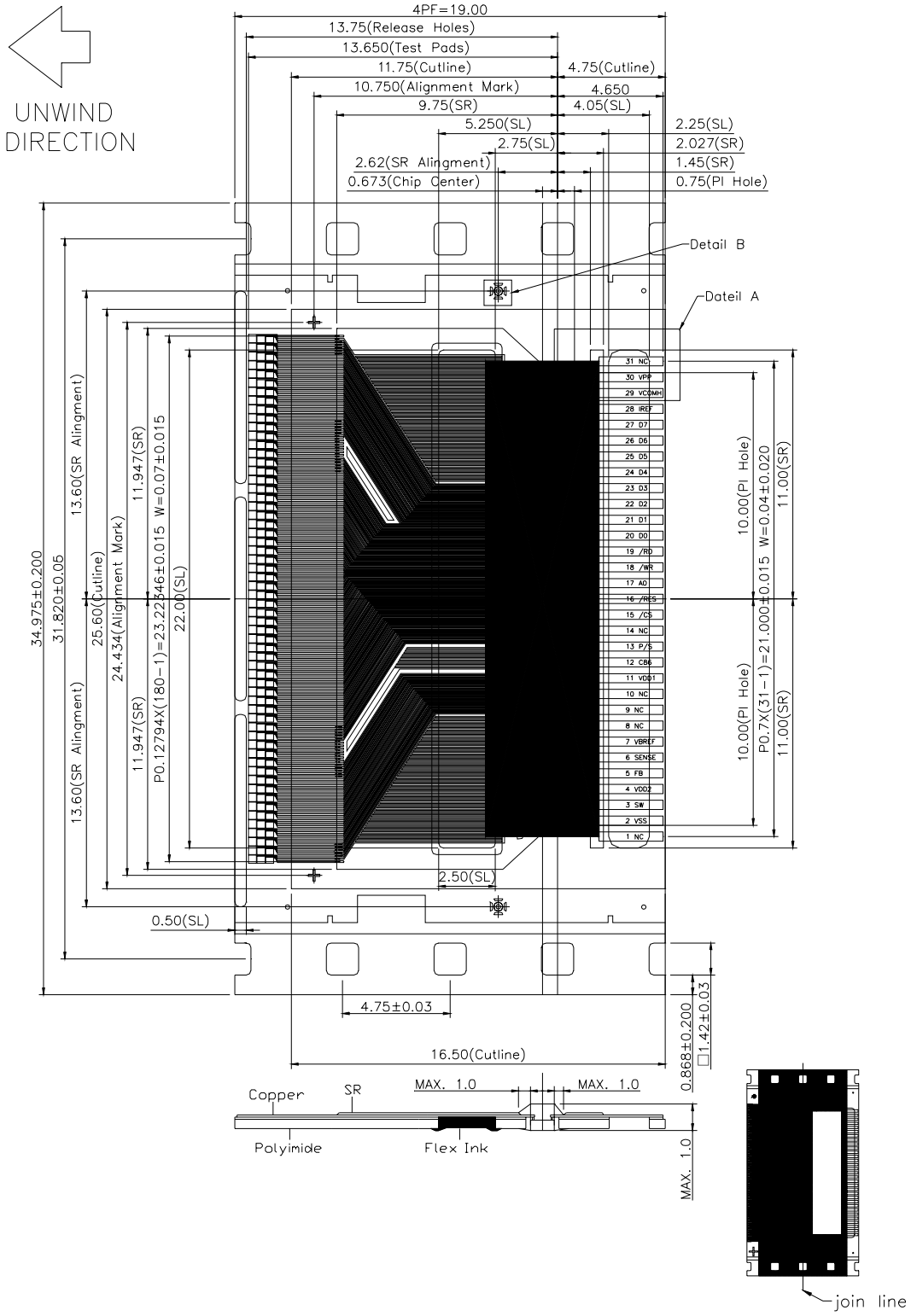
Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
161	SEG87	176	NC	191	COM27	206	COM57
162	SEG88	177	NC	192	COM29	207	COM59
163	SEG89	178	COM1	193	COM31	208	COM61
164	SEG90	179	COM3	194	COM33	209	COM63
165	SEG91	180	COM5	195	COM35	210	NC
166	SEG92	181	COM7	196	COM37	211	NC
167	SEG93	182	COM9	197	COM39		
168	SEG94	183	COM11	198	COM41		
169	SEG95	184	COM13	199	COM43		
170	NC	185	COM15	200	COM45		
171	NC	186	COM17	201	COM47		
172	NC	187	COM19	202	COM49		
173	NC	188	COM21	203	COM51		
174	NC	189	COM23	204	COM53		
175	NC	190	COM25	205	COM55		

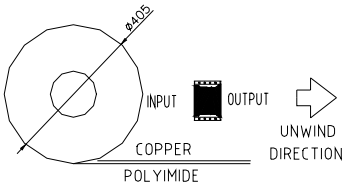
Note:

Following is the details of pad connection in SH1101A-TCP03 (TCP Form).

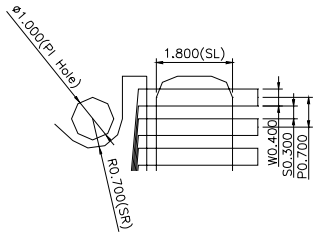
- "CLS" pad connects to "V_{DD1}" pad, Internal oscillator circuit is enabled.
- "V_{REF}" pad connects to "V_{PP}" pad.
- "V_{CL}" & "V_{SL}" pad connects to "V_{SS}" pad.
- "C86" & "P/S" pad options can be selected by user. So SH1101A-TCP03 (TCP Form) supports 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface or serial peripheral interface.
- SH1101A-TCP03 (TCP Form) supports internal DC-DC converter function.

External View of SH1101A-TCP03 TCP Pins

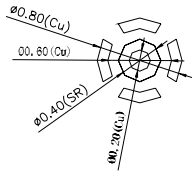




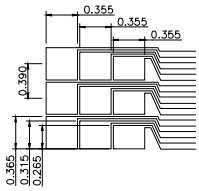
PACK DIRECTION



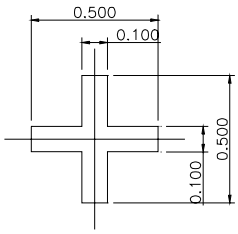
Detail A
Scale 2:1



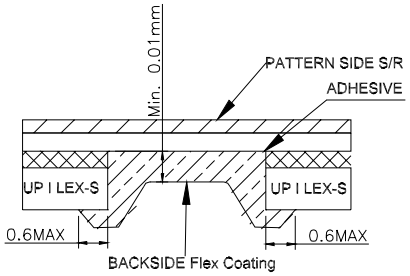
Detail B
Scale 5:1



Detail of Test Pads
Scale 5:1



Detail of Alignment Mark
Scale 10:1



NOTES:

1. All SR Dimension Tolerance ±0.200mm if not specified
2. All SL Dimension Tolerance ±0.05mm if not specified
3. Corner radiuses unless otherwise specified is 0.20mm
4. PKG Reel Size : ϕ405mm
5. Input IL total pitch from left 2nd to right 2nd
6. Output IL total pitch from left 2nd to right 2nd
7. IL Pitch=45um ; Min Pitch=45um(IL/Trace)

Cautions Concerning Storage:

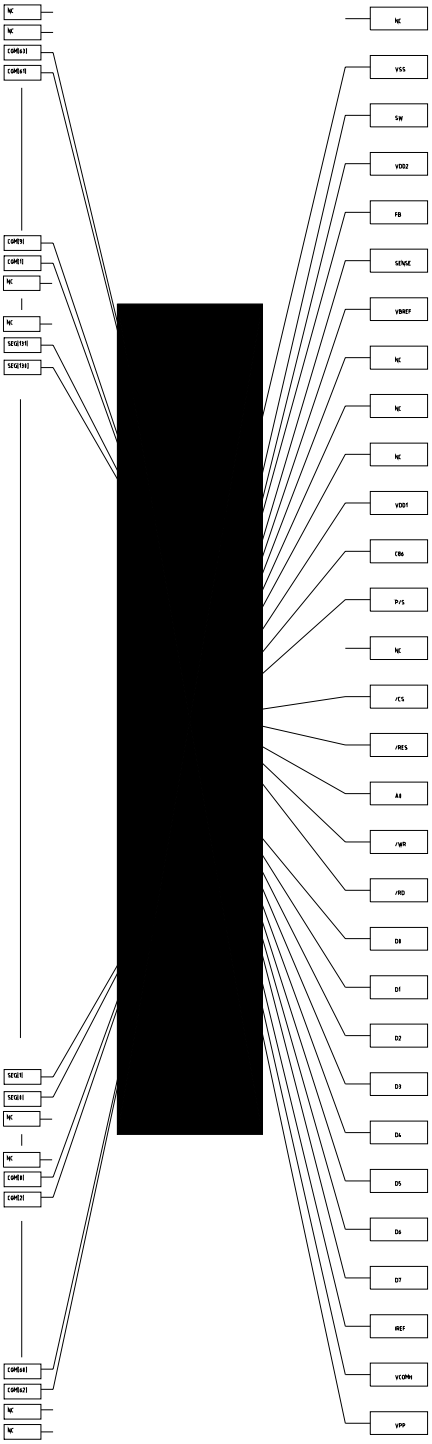
1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions:

Storage state	Storage conditions
unopened **(less than 90 days)**	Temperature: 5 to 30℃; humidity: 80%RH or less.
After seal of broken **(less than 30 days)**	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

Appendix

SH1101A-TCP06 TAB Pin Layout



(Copper Side View)

SH1101A-TCP06 TAB Pin Assignment (Total: 249 pads)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
1	NC	41	COM49	81	SEG123	121	SEG83
2	V_{PP}	42	COM47	82	SEG122	122	SEG82
3	V_{COMH}	43	COM45	83	SEG121	123	SEG81
4	I_{REF}	44	COM43	84	SEG120	124	SEG80
5	D7	45	COM41	85	SEG119	125	SEG79
6	D6	46	COM39	86	SEG118	126	SEG78
7	D5	47	COM37	87	SEG117	127	SEG77
8	D4	48	COM35	88	SEG116	128	SEG76
9	D3	49	COM33	89	SEG115	129	SEG75
10	D2	50	COM31	90	SEG114	130	SEG74
11	D1	51	COM29	91	SEG113	131	SEG73
12	D0	52	COM27	92	SEG112	132	SEG72
13	$\overline{RD}$	53	COM25	93	SEG111	133	SEG71
14	$\overline{WR}$	54	COM23	94	SEG110	134	SEG70
15	A0	55	COM21	95	SEG109	135	SEG69
16	$\overline{RES}$	56	COM19	96	SEG108	136	SEG68
17	$\overline{CS}$	57	COM17	97	SEG107	137	SEG67
18	NC	58	COM15	98	SEG106	139	SEG66
19	P/S	59	COM13	99	SEG105	139	SEG65
20	C86	60	COM11	100	SEG104	140	SEG64
21	V_{DD1}	61	COM9	101	SEG103	141	SEG63
22	NC	62	COM7	102	SEG102	142	SEG62
23	NC	63	COM5	103	SEG101	143	SEG61
24	NC	64	COM3	104	SEG100	144	SEG60
25	V_{BREF}	65	COM1	105	SEG99	145	SEG59
26	SENSE	66	NC	106	SEG98	146	SEG58
27	FB	67	NC	107	SEG97	147	SEG57
28	V_{DD2}	68	NC	108	SEG96	148	SEG56
29	SW	69	NC	109	SEG95	149	SEG55
30	V_{SS}	70	NC	110	SEG94	150	SEG54
31	NC	71	NC	111	SEG93	151	SEG53
32	NC	72	NC	112	SEG92	152	SEG52
33	NC	73	SEG131	113	SEG91	153	SEG51
34	COM63	74	SEG130	114	SEG90	154	SEG50
35	COM61	75	SEG129	115	SEG89	155	SEG49
36	COM59	76	SEG128	116	SEG88	156	SEG48
37	COM57	77	SEG127	117	SEG87	157	SEG47
38	COM55	78	SEG126	118	SEG86	158	SEG46
39	COM53	79	SEG125	119	SEG85	159	SEG45
40	COM51	80	SEG124	120	SEG84	160	SEG44

TAB Pin Assignment (continued)

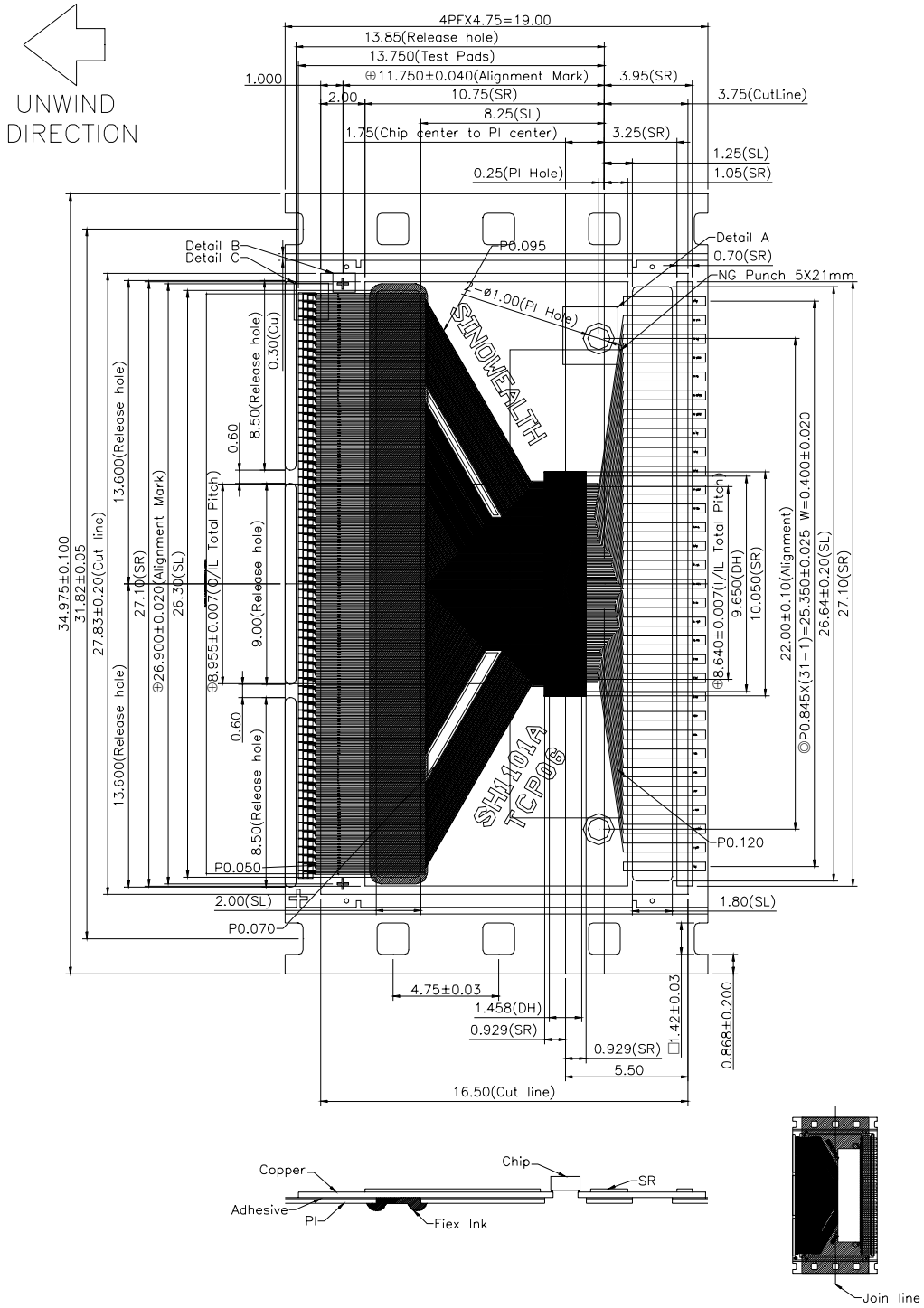
Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
161	SEG43	184	SEG20	207	NC	230	COM28
162	SEG42	185	SEG19	208	NC	231	COM30
163	SEG41	186	SEG18	209	NC	232	COM32
164	SEG40	187	SEG17	210	NC	233	COM34
165	SEG39	188	SEG16	211	NC	234	COM36
166	SEG38	189	SEG15	212	NC	235	COM38
167	SEG37	190	SEG14	213	NC	236	COM40
168	SEG36	191	SEG13	214	NC	237	COM42
169	SEG35	192	SEG12	215	NC	238	COM44
170	SEG34	193	SEG11	216	COM0	239	COM46
171	SEG33	194	SEG10	217	COM2	240	COM48
172	SEG32	195	SEG9	218	COM4	241	COM50
173	SEG31	196	SEG8	219	COM6	242	COM52
174	SEG30	197	SEG7	220	COM8	243	COM54
175	SEG29	198	SEG6	221	COM10	244	COM56
176	SEG28	199	SEG5	222	COM12	245	COM58
177	SEG27	200	SEG4	223	COM14	246	COM60
178	SEG26	201	SEG3	224	COM16	247	COM62
179	SEG25	202	SEG2	225	COM18	248	NC
180	SEG24	203	SEG1	226	COM20	249	NC
181	SEG23	204	SEG0	227	COM22		
182	SEG22	205	NC	228	COM24		
183	SEG21	206	NC	229	COM26		

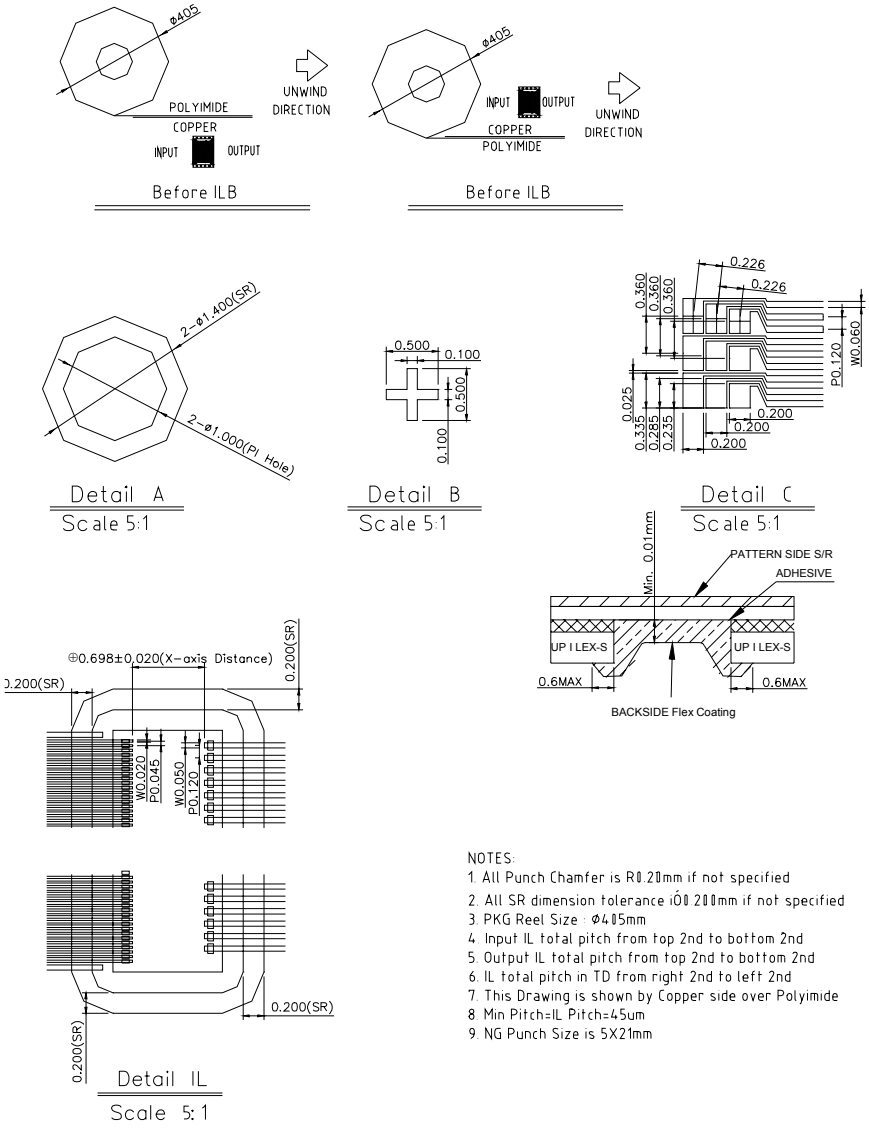
Note:

Following is the details of pad connection in SH1101A-TCP06 (TCP Form).

- "CLS" pad connects to "V_{DD1}" pad, Internal oscillator circuit is enabled.
- "V_{REF}" pad connects to "V_{PP}" pad.
- "V_{CL}" & "V_{SL}" pad connects to "Vss" pad.
- "C86" & "P/S" pad options can be selected by user. So SH1101A-TCP06 (TCP Form) supports 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface or serial peripheral interface.
- SH1101A-TCP06 (TCP Form) supports internal DC-DC converter function.

External View of SH1101A-TCP06 TAB Pins





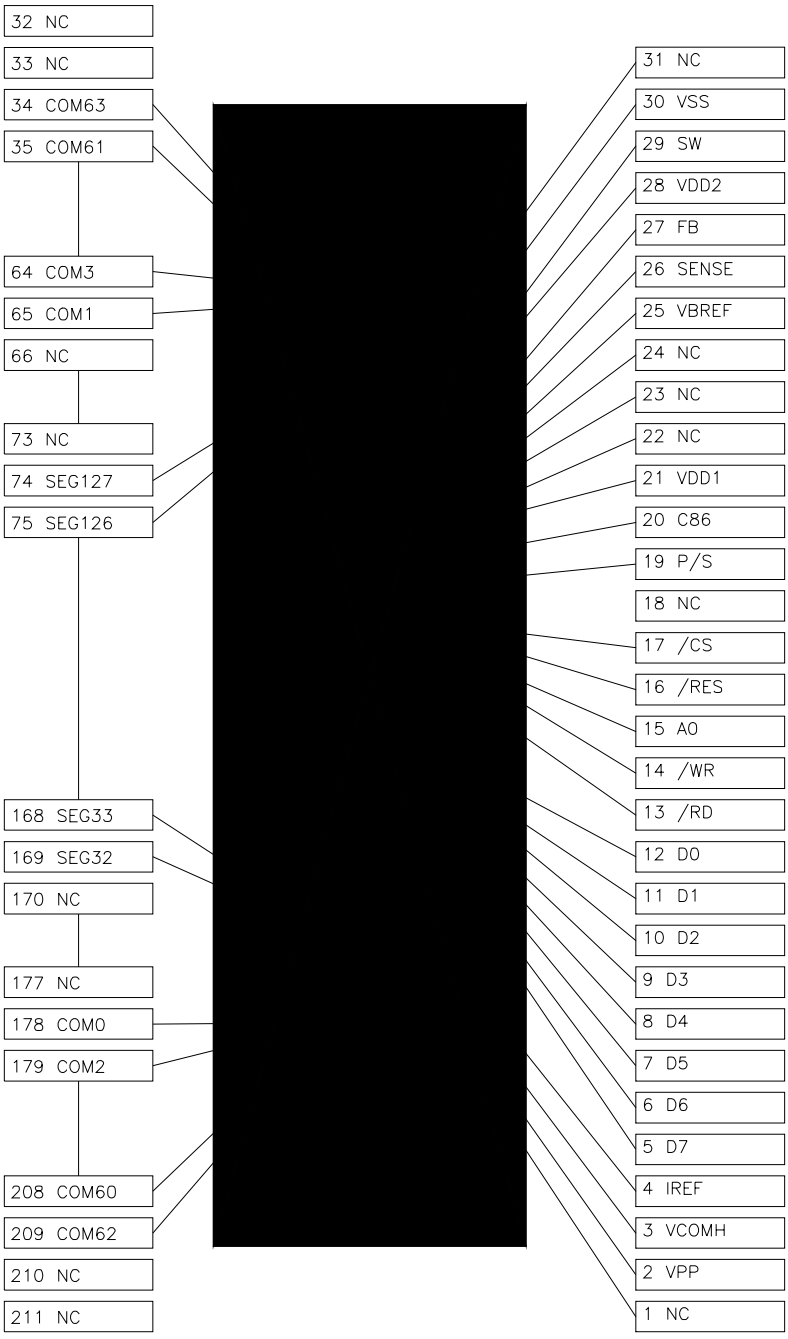
Cautions Concerning Storage:

1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions:

Storage state	Storage conditions
unopened **(less than 90 days)**	Temperature: 5 to 30℃; humidity: 80%RH or less.
After seal of broken **(less than 30 days)**	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

SH1101A-TCP09 TCP Pin Layout



(Copper Side View)

SH1101A-TCP09 TCP Pin Assignment (Total: 211 pads)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
1	NC	41	COM49	81	SEG120	121	SEG80
2	V_{PP}	42	COM47	82	SEG119	122	SEG79
3	V_{COMH}	43	COM45	83	SEG118	123	SEG78
4	I_{REF}	44	COM43	84	SEG117	124	SEG77
5	D7	45	COM41	85	SEG116	125	SEG76
6	D6	46	COM39	86	SEG115	126	SEG75
7	D5	47	COM37	87	SEG114	127	SEG74
8	D4	48	COM35	88	SEG113	128	SEG73
9	D3	49	COM33	89	SEG112	129	SEG72
10	D2	50	COM31	90	SEG111	130	SEG71
11	D1	51	COM29	91	SEG110	131	SEG70
12	D0	52	COM27	92	SEG109	132	SEG69
13	$\overline{RD}$	53	COM25	93	SEG108	133	SEG68
14	$\overline{WR}$	54	COM23	94	SEG107	134	SEG67
15	A0	55	COM21	95	SEG106	135	SEG66
16	$\overline{RES}$	56	COM19	96	SEG105	136	SEG65
17	$\overline{CS}$	57	COM17	97	SEG104	137	SEG64
18	NC	58	COM15	98	SEG103	139	SEG63
19	P/S	59	COM13	99	SEG102	139	SEG62
20	C86	60	COM11	100	SEG101	140	SEG61
21	V_{DD1}	61	COM9	101	SEG100	141	SEG80
22	NC	62	COM7	102	SEG99	142	SEG79
23	NC	63	COM5	103	SEG98	143	SEG78
24	NC	64	COM3	104	SEG97	144	SEG77
25	V_{BREF}	65	COM1	105	SEG96	145	SEG76
26	SENSE	66	NC	106	SEG95	146	SEG75
27	FB	67	NC	107	SEG94	147	SEG74
28	V_{DD2}	68	NC	108	SEG93	148	SEG73
29	SW	69	NC	109	SEG92	149	SEG72
30	V_{SS}	70	NC	110	SEG91	150	SEG71
31	NC	71	NC	111	SEG90	151	SEG70
32	NC	72	NC	112	SEG89	152	SEG69
33	NC	73	NC	113	SEG88	153	SEG68
34	COM63	74	SEG127	114	SEG87	154	SEG67
35	COM61	75	SEG126	115	SEG86	155	SEG66
36	COM59	76	SEG125	116	SEG85	156	SEG65
37	COM57	77	SEG124	117	SEG84	157	SEG64
38	COM55	78	SEG123	118	SEG83	158	SEG63
39	COM53	79	SEG122	119	SEG82	159	SEG62
40	COM51	80	SEG121	120	SEG81	160	SEG61

SH1101A-TCP09 TCP Pin Assignment (continued)

Pin No.	Designation	Pin No.	Designation	Pin No.	Designation	Pin No.	Designation
161	SEG60	176	NC	191	COM26	206	COM56
162	SEG59	177	NC	192	COM28	207	COM58
163	SEG58	178	COM0	193	COM30	208	COM60
164	SEG57	179	COM2	194	COM32	209	COM62
165	SEG56	180	COM4	195	COM34	210	NC
166	SEG55	181	COM6	196	COM36	211	NC
167	SEG54	182	COM8	197	COM38		
168	SEG53	183	COM10	198	COM40		
169	SEG52	184	COM12	199	COM42		
170	SEG51	185	COM14	200	COM44		
171	SEG50	186	COM16	201	COM46		
172	SEG49	187	COM18	202	COM48		
173	SEG48	188	COM20	203	COM50		
174	SEG47	189	COM22	204	COM52		
175	SEG46	190	COM24	205	COM54		

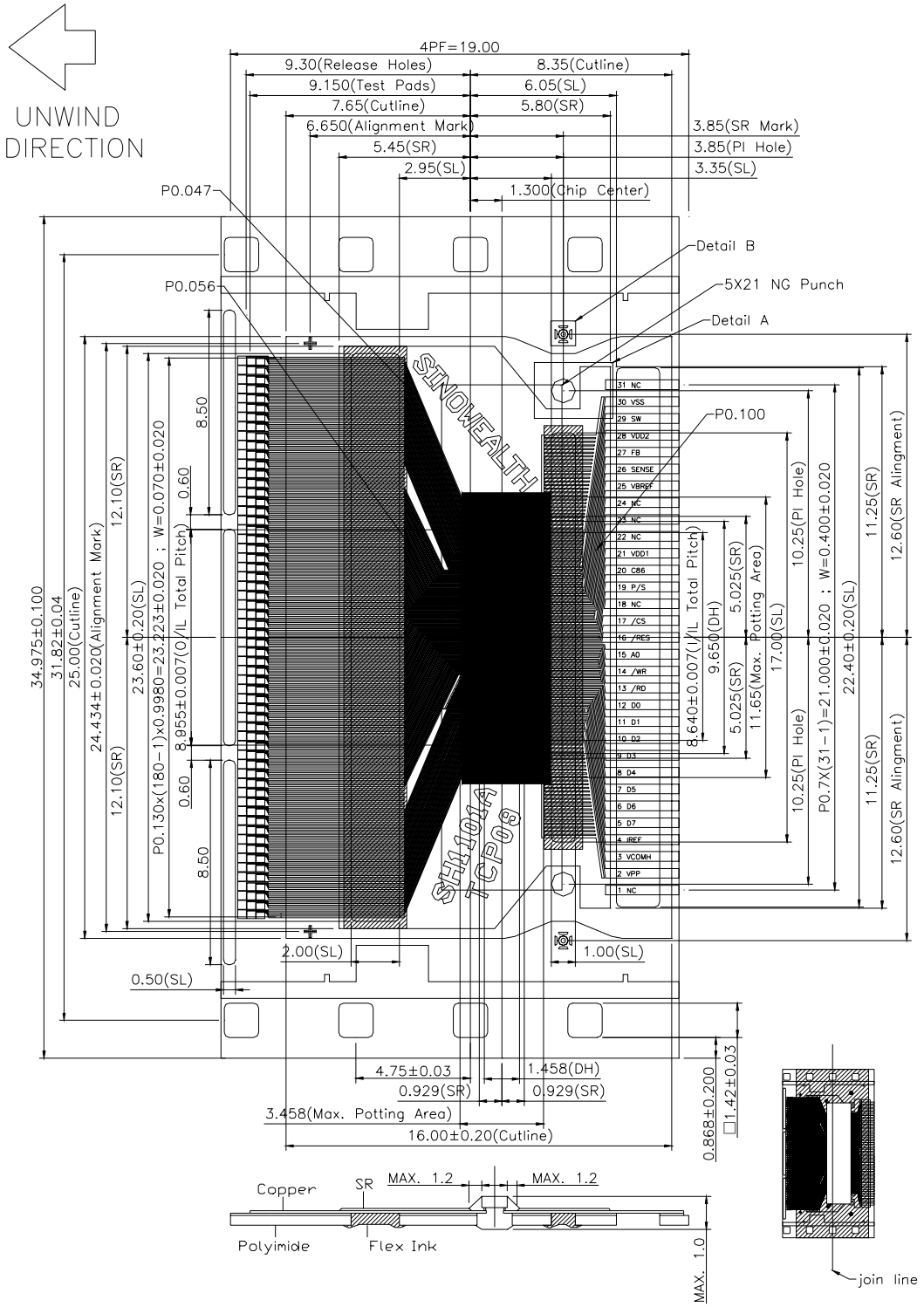
Note:

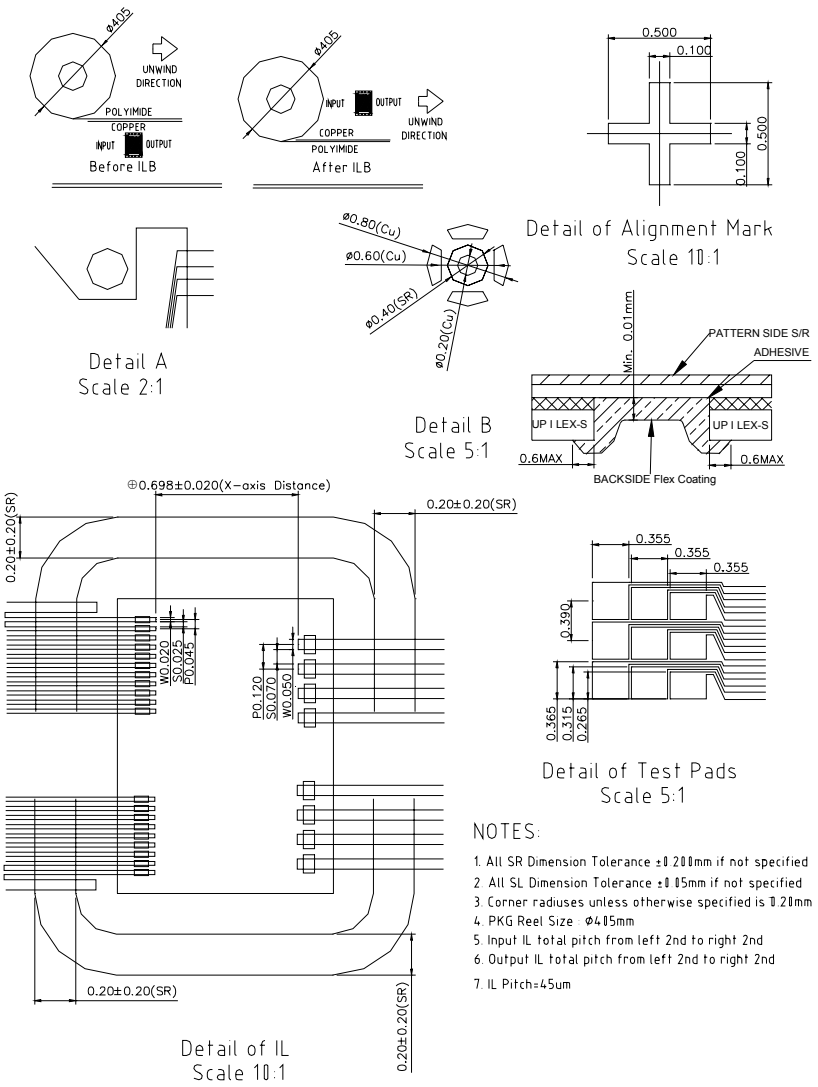
Following is the details of pad connection in SH1101A-TCP09 (TCP Form).

- "CLS" pad connects to "V_{DD1}" pad, Internal oscillator circuit is enabled.
- "V_{REF}" pad connects to "V_{PP}" pad.
- "V_{CL}" & "V_{SL}" pad connects to "Vss" pad.
- "C86" & "P/S" pad options can be selected by user. So SH1101A-TCP09 (TCP Form) supports 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface or serial peripheral interface.

SH1101A-TCP09 (TCP Form) supports internal DC-DC converter function.

External View of SH1101A-TCP09 TCP Pins





Cautions Concerning Storage:

1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions:

Storage State	Storage Conditions
unopened **(less than 90 days)**	Temperature: 5 to 30℃; humidity: 80%RH or less.
After seal of broken **(less than 30 days)**	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

Ordering Information

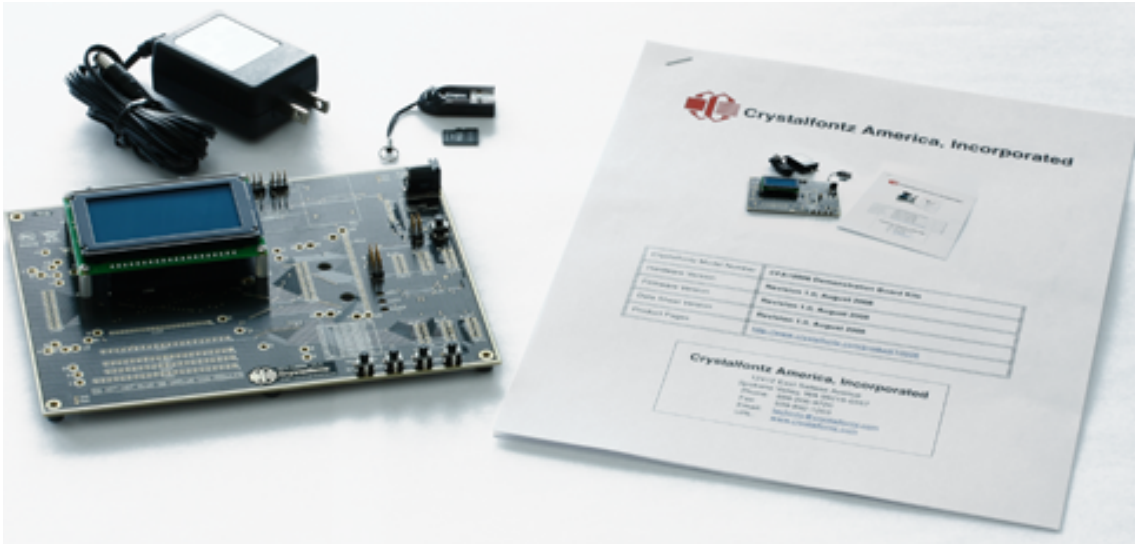
Part No.	Package
SH1101A-COG01	Gold bump on chip tray
SH1101A-TCP03	TCP Form
SH1101A-TCP06	TCP Form
SH1101A-TCP09	TCP Form

Data Sheet Revision History

Version	Content	Date
2.2	1. Change operating voltage from 1.8~3.5V to 1.65~3.5V in low voltage mode	Nov. 2006
2.1	2. Add low voltage mode 3. Add DC/AC Characteristics in low voltage mode	Aug. 2006
2.0	1. Add TCP09 Form information 2. DC Characteristics change V_{BREF} condition	Apr. 2006
1.0	Original	Nov. 2005

Crystalfontz America, Incorporated

CFA10009 Demonstration Board Kits
User Guide



Crystalfontz Model Number	**CFA10009 Demonstration Board Kits (for OLEDs)**
Hardware Version	**Revision 1.1, June 2009**
Firmware Version	**Revision 1.0, June 2009**
Data Sheet Version	**Revision 1.0, June 2009**
Product Pages	www.crystalfontz.com/product/CFA10009.html

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REVISION HISTORY

CFA10009 DEMONSTATION BOARD	
2009/06/25	Current demonstration board version: **v1.1** New demonstration board.

CFA10009 DEMONSTRATION BOARD KITS FIRMWARE	
2009/06/25	Current firmware version (series): **v1.0** Initial release.

CFA10009 DEMONSTRATION BOARD KITS USER GUIDE	
2009/06/25	Current Data Sheet version: **v1.0** New Data Sheet.

QUICK START

The CFA10009 demonstration board is shipped with a compatible OLED module of your choice installed and tested. Simply plug the power supply (included) into an AC outlet. The CFA10009 will initialize and turn on the display, then run the demonstration script from the included microSD card.

INTRODUCTION

The CFA10009 Demonstration Board Kit has everything you need to easily demonstrate and experiment with one compatible Crystalfontz OLED module.The kit can also be used as a reference for your designs that use a Crystalfontz OLED module listed in the table on the next page.

You can easily modify the miniBASIC scripts and bitmaps on the microSD card to make your own test screens, or even to model user interface functions. All that is needed is the included microSD USB reader, a text editor (Notepad will do), an image editor (MS Paint will do), and a simple, open-source format conversion utility (Image2Code) that we offer free of charge.

Beyond demonstrations, the CFA10009 allows you to easily measure current of the different portions of the circuit under operation.

The schematic, bill of materials, and even the PCB layout is available for download from our site. (As always, no registration is required.) Since the design materials are available before purchase, there is no risk of being "surprised" late in the design.

The CFA10009 is preprogrammed with a microSD boot loader. You can load our simple C example code, the miniBASIC interpreter, or build your own application for the CFA10009's versatile Atmel ATMEGA2561 microcontroller using AVR Studio and WinAVR (both free).

The board has a JTAG port for more advanced programming and debugging. All the ports are on 0.1" centers so you can connect them to anything you need. The CFA10009 is so versatile that you may want to use it as a base development platform for your projects.

CFA10009 KIT CONFIGURATIONS

FOR OLED MODULE	WITH THIS CONTROLLER	ORDER THIS DEMONSTRATION BOARD KIT	BLOCK DIAGRAM
CFAL12822A-Y-B	Solomon SSD1305	DMO-L12822AYB	Figure 2.
CFAL12822A-Y-B1	Solomon SSD1305	DMO-L12822AYB1	Figure 1.
CFAL12832C-W-B1	Sino Wealth SH1101A	DMO-L12832CWB1	Figure 1.
CFAL12864C-Y-B1	Solomon SSD1305	DMO-L12864CYB1	Figure 1.
CFAL12864L-G-B2	Solomon SSD1305	DMO-L12864LGB2	Figure 2.
CFAL12864L-Y-B2	Solomon SSD1305	DMO-L12864LYB2	Figure 2.
CFAL12864L-G-B2TS	Solomon SSD1305	DMO-L12864LGB2TS	Figure 4.
CFAL12864L-Y-B2TS	Solomon SSD1305	DMO-L12864LYB2TS	Figure 4.
CFAL12864L-G-B4	Solomon SSD1305	DMO-L12864LGB4	Figure 2.
CFAL12864L-Y-B4	Solomon SSD1305	DMO-L12864LYB4	Figure 2.
CFAL12864L-G-B6	Solomon SSD1305	DMO-L12864LGB6	Figure 2.
CFAL12864L-G- B6TS	Solomon SSD1305	DMO-L12864LGB6TS	Figure 3.
CFAL12864L-Y- B6TS	Solomon SSD1305	DMO-L12864LYB6TS	Figure 3.
CFAL12864L-W- B6TS	Solomon SSD1305	DMO-L12864LWB6TS	Figure 3.
CFAL12864N-A-B1	Sino Wealth SH1101A	DMO-L12864NAB1	Figure 1.
CFAL12864S-Y-B1	Solomon SSD1303	DMO-L12864SYB1	Figure 1.
CFAL12864U-W-B1	Solomon SSD1303	DMO-L12864UWB1	Figure 1.
CFAL12864Z-G-B2	Solomon SSD1325	DMO-L12864ZGB2	Figure 2.
CFAL12864Z-Y-B2	Solomon SSD1325	DMO-L12864ZYB2	Figure 2.
CFAL12864Z-G-B2TS	Solomon SSD1325	DMO-L12864ZGB2TS	Figure 4.
CFAL12864Z-Y-B2TS	Solomon SSD1325	DMO-L12864YB2TS	Figure 4.
CFAL12864Z-G-B4	Solomon SSD1325	DMO-L12864ZGB4	Figure 2.
CFAL12864Z-Y-B4	Solomon SSD1325	DMO-L12864ZYB4	Figure 2.
CFAL12864Z-G-B6	Solomon SSD1325	DMO-L12864ZGB6	Figure 2.
CFAL12864Z-W-B6	Solomon SSD1325	DMO-L12864ZWB6	Figure 2.
CFAL12864Z-Y-B6	Solomon SSD1325	DMO-L12864ZYB6	Figure 2.

FOR OLED MODULE	WITH THIS CONTROLLER	ORDER THIS DEMONSTRATION BOARD KIT	BLOCK DIAGRAM
CFAL12864Z-G-B6TS	Solomon SSD1325	DMO-L12864ZGB6TS	Figure 3.
CFAL12864Z-W-B6TS	Solomon SSD1325	DMO-L12864ZWB6TS	Figure 3.
CFAL12864Z-Y-B6TS	Solomon SSD1325	DMO-L12864ZYB6TS	Figure 3.
CFAL25664A-Y-B1	ST STV8105	DMO-L25664AYB1	Figure 1.
CFAL9664A-W-B1	Solomon SSD1305	DMO-L9664AWB1	Figure 1.

CONTENTS OF DEMONSTRATION BOARD KIT

- ❑ CFA10009 Demonstration Board (PCB).
- ❑ Installed OLED module of your choice. (Selected at time of ordering. See choices in the table above.)
- ❑ Power adapter.
- ❑ MicroSD memory card loaded with BASIC demonstration program and bitmap images.
- ❑ USB reader for the microSD memory card.

In addition to the kit contents, a zipped folder of hardware design and program files is available at http://www.crystalfontz.com/product/CFA10009.html. (Free download.)

HOW TO MAKE A CUSTOM DEMONSTRATION

The CFA10009 is programmed with firmware that will read a BASIC program file from the microSD memory card. The BASIC program can read bitmap image files from the microSD memory card and display them on the OLED module. The BASIC program can also read the four demonstration board buttons and change the brightness settings.

By using the USB reader, a text editor, and a graphic conversion utility (provided), you can customize the demonstration to include your own bitmap images. The large capacity of the microSD card allows you to create complex demonstrations.

For the most recent version of the graphic conversion utility, sample scripts, and sample images for customizing the demonstration, download the zipped folder at http://www.crystalfontz.com/product/CFA10009.html.

LOADING A CUSTOM HEX FILE

The CFA10009 Demonstration Board Kit is shipped with the miniBasic-AVR interpreter loaded into the microcontroller Atmel ATMEGA2561's flash memory.

If you want to load our simple demonstration or your own program, simply name the hex file "cfa10009.hex" and copy it into the root the directory of the microSD card. When the CFA10009 boots, the boot loader will program the ATMEGA2561's flash with "cfa10009.hex" and then execute it.

Acknowledgement Note: The miniBASIC-AVR is a derivative of this (see http://www.personal.leeds.ac.uk/~bgy1mm/Minibasic/MiniBasicHome.html). The miniBASIC-AVR also includes the EFSL embedded filesystems library (see http://efsl.be/.

HARDWARE DESIGN INFORMATION

BLOCK DIAGRAM

Here are block diagrams of the CFA10009 Demonstration Board with different types of installed modules:

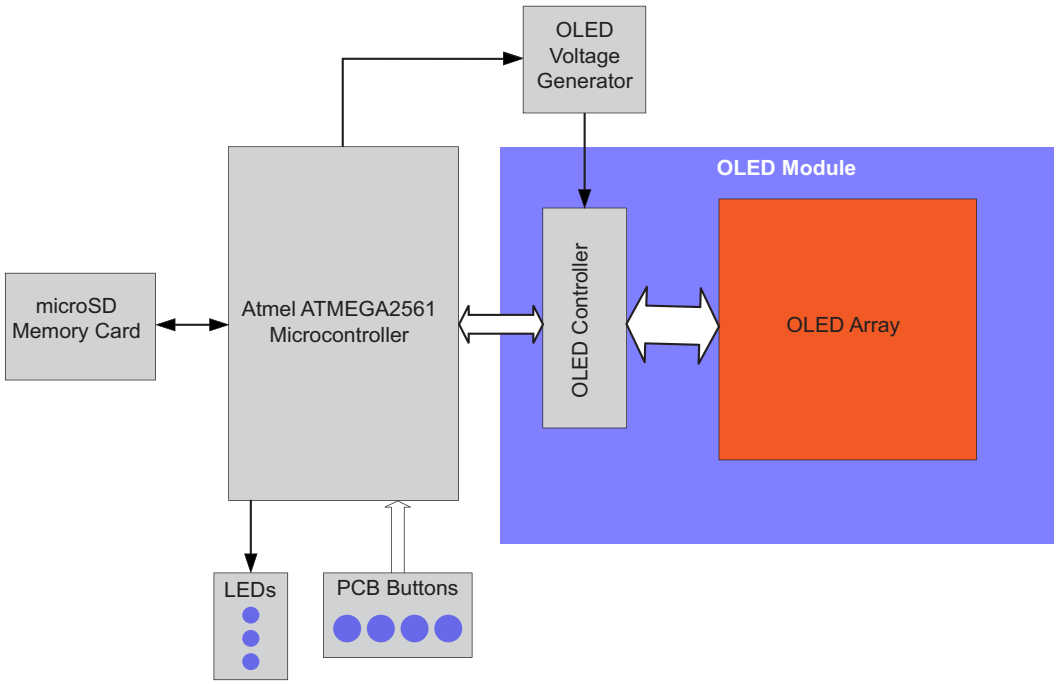

Figure 1. For kits with CFAL12822A-Y-B1,CFAL12832C-W-B1,CFAL12864C-Y-B1,CFAL12864N-A-B1, CFAL12864S-Y-B1, CFAL25664A-Y-B1, and CFAL9664A-W-B1

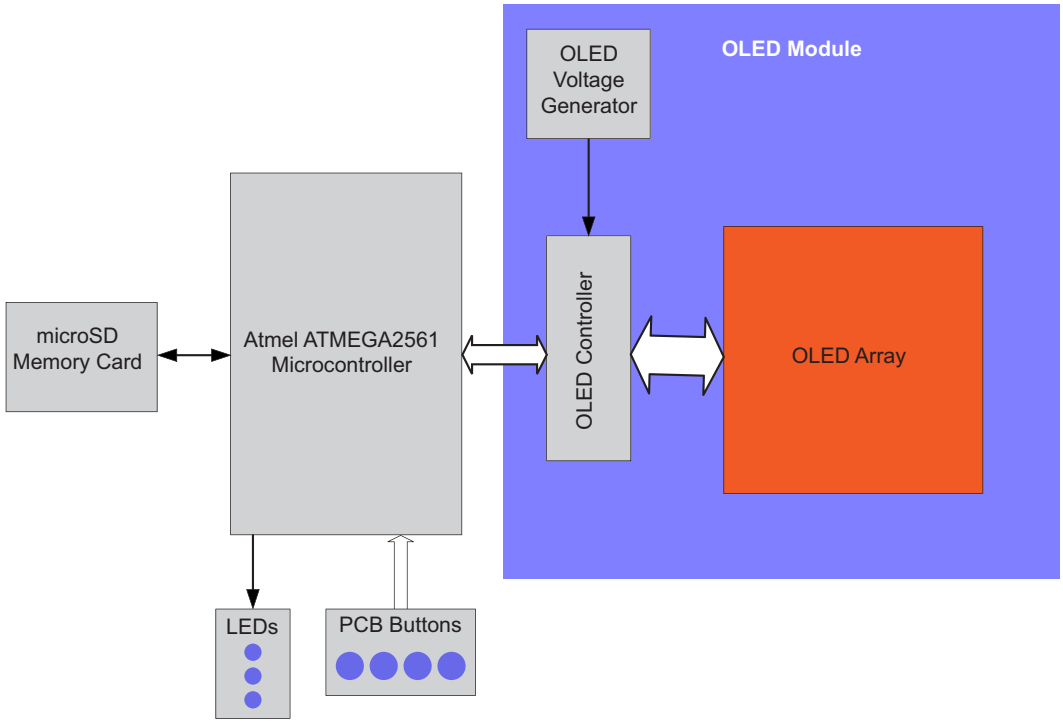

Figure 2. For kits with CFAL12822A-Y-B, CFAL12864L-G-B2, CFAL12864L-Y-B2, CFAL12864L-G-B4,CFAL12864L-Y-B4, CFAL12864L-G-B6, CFAL12864Z-G-B2, CFAL12864Z-Y-B2, CFAL12864Z-G-B4, CFAL12864Z-Y-B4, CFAL12864Z-G-B6,CFAL12864Z-W-B6, and CFAL12864Z-Y-B6

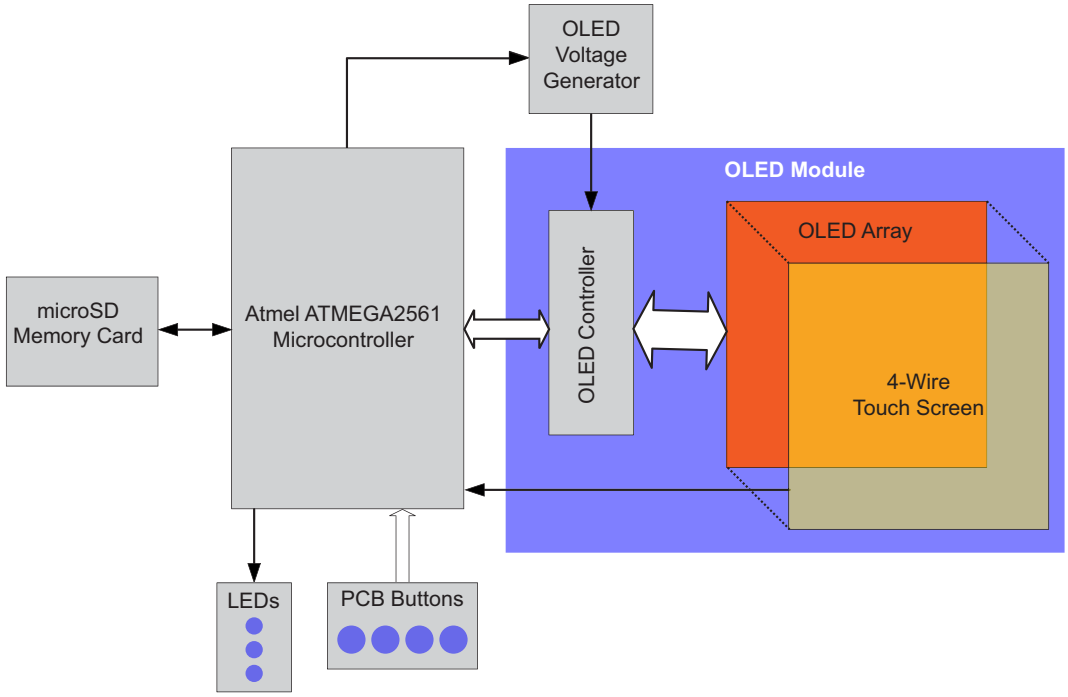

Figure 3. For kits with CFAL12864L-G- B6TS, CFAL12864L-Y- B6TS, and CFAL12864L-W- B6TS

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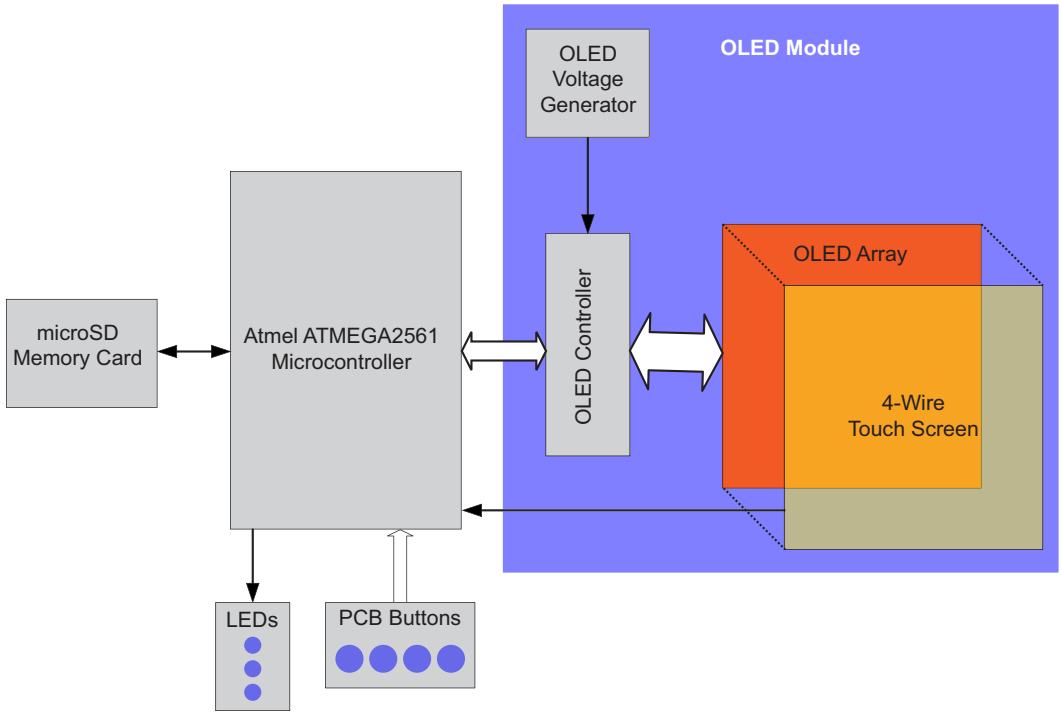

Figure 4. CFAL12864L-G-B2TS,CFAL12864L-Y-B2TS,CFAL12864L-G- B6TS, CFAL12864L-Y- B6TS, CFAL12864Z-G-B2TS, CFAL12864Z-Y-B2TS, CFAL12864Z-G-B6TS, CFAL12864Z-W-B6TS, and CFAL12864Z-Y-B6TS

CONTENTS OF HARDWARE DESIGN FOLDER

The zipped folder at http://www.crystalfontz.com/product/CFA10009.html includes the complete hardware design of the CFA10009 Demonstration Board.

- ❑ Schematic.
- ❑ PCB layout.
- ❑ Bill Of Materials (BOM) as an XLS spreadsheet.
- ❑ Simple OLED initialization code and bitmap display code.

The schematic and PCB layout were created with CadSoft EAGLE. EAGLE is a capable and low-cost electrical CAD system. You can download a freeware light edition of EAGLE from http://www.cadsoft.de/ to load, view, and print the schematic and layout files.

CARE AND HANDLING PRECAUTIONS

The kit is sold with a module mounted on it. If you attempt to modify the board to work with other modules, the warranty is void. Do not disassemble or modify the CFA10009 Demonstration Board Kit.

For optimum operation of the module and demonstration board and to prolong their life, please follow the precautions below.

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. Ground your body, work surfaces, and equipment.

AVOID SHOCK, IMPACT, TORQUE, OR TENSION

- Do not expose the demonstration board and module to strong mechanical shock, impact, torque, or tension.
- Do not drop, toss, bend, or twist the demonstration board and module.
- Do not place weight or pressure on the demonstration board and module.

OPERATION

- The module ships with a protective film over the display. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- Use only the included AC adapter to power the board.
- Observe the operating temperature limitations for the module: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
- Operate away from dust, moisture, and direct sunlight.

CLEANING

- The polarizer (laminated to the glass) is soft plastic. The soft plastic is easily scratched or damaged. Be very careful when you clean the polarizer.
- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips).
- Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand “Crystal Clear Tape”). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.

STORAGE AND RECYCLING

- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle the demonstration board and module at an approved facility.