

## **OTM3225A**

---

**720-channel 6-bit source driver and  
320-channel gate driver  
with System-On-Chip (SOC) for color  
amorphous TFT LCD**

***Preliminary***

Jan. 22, 2009

Version 0.1

## Table of Contents

	<u>PAGE</u>
<b>1. GENERAL DESCRIPTION</b> .....	<b>5</b>
<b>2. FEATURE</b> .....	<b>5</b>
<b>3. ORDERING INFORMATION</b> .....	<b>5</b>
<b>4. BLOCK DIAGRAM</b> .....	<b>6</b>
4.1. BLOCK FUNCTION .....	6
4.2. SYSTEM INTERFACE .....	7
4.2.1. Interface .....	7
4.2.2. External Display Interface .....	7
4.2.3. Address Counter (AC).....	7
4.2.4. Graphics RAM (GRAM).....	7
4.2.5. Grayscale Voltage Generating Circuit .....	7
4.2.6. Timing Controller .....	7
4.2.7. Oscillator (OSC).....	7
4.2.8. Source Driver Circuit .....	7
4.2.9. Gate Driver Circuit.....	7
4.2.10. LCD Driving Power Supply Circuit.....	7
<b>5. SIGNAL DESCRIPTIONS</b> .....	<b>8</b>
<b>6. INSTRUCTIONS</b> .....	<b>11</b>
6.1. OUTLINE.....	11
6.2. INSTRUCTION.....	13
6.2.1. Index Register (IR) .....	15
6.2.2. ID Read Register (SR) .....	15
6.2.3. Driver Output Control Register (R01h).....	15
6.2.4. LCD Driving Waveform Control (R02h).....	16
6.2.5. Entry Mode (R03h).....	16
6.2.6. Scaling Control register (R04h).....	19
6.2.7. Display Control (R07h).....	20
6.2.8. Display Control 2 (R08h).....	21
6.2.9. Display Control 3 (R09h).....	22
6.2.10. Frame Cycle Control (R0Ah).....	23
6.2.11. External Display Interface Control 1 (R0Ch).....	24
6.2.12. Frame Maker Position (R0Dh).....	25
6.2.13. External Display Interface Control 2 (R0Fh) .....	25
6.2.14. Power Control 1 (R10h).....	26
6.2.15. Power Control 2 (R11h).....	27
6.2.16. Power Control 3 (R12h).....	28
6.2.17. Power Control 4 (R13h).....	29
6.2.18. GRAM Address Set (Horizontal Address) (R20h).....	30
6.2.19. GRAM Address Set (Vertical Address) (R21h).....	30
6.2.20. Write Data to GRAM (R22h).....	31
6.2.21. Read Data Read from GRAM (R22h).....	38
6.2.22. Power Control 7 (R29h).....	39
6.2.23. Frame rate control (R2Bh).....	39

6.2.24. $\gamma$ Control (R30h to R3Dh).....	41
6.2.25. Window Horizontal RAM Address Start (R50h).....	42
6.2.26. Window Horizontal RAM Address End (R51h).....	42
6.2.27. Window Vertical RAM Address Start (R52h).....	42
6.2.28. Window Vertical RAM Address End (R53h).....	42
6.2.29. Gate Driver Scan Control (R60h).....	42
6.2.30. Driver Output Control (R61h).....	45
6.2.31. Vertical Scroll Control (R6Ah).....	45
6.2.32. Display Position – Partial Display 1 (R80h).....	46
6.2.33. RAM Address Start – Partial Display 1 (R81h).....	46
6.2.34. RAM Address End – Partial Display 1 (R82h).....	46
6.2.35. Display Position – Partial Display 2 (R83h).....	46
6.2.36. RAM Address Start – Partial Display 2 (R84h).....	46
6.2.37. RAM Address End – Partial Display 2 (R85h).....	46
6.2.38. Panel Interface Control 1 (R90h).....	47
6.2.39. Panel Interface Control 2 (R92h).....	48
6.2.40. Panel Interface control 4 (R95h).....	49
6.2.41. Panel Interface Control 5 (R97h).....	51
<b>7. GRAM.....</b>	<b>52</b>
<b>8. INTERFACES.....</b>	<b>54</b>
8.1. SYSTEM INTERFACE.....	54
8.1.1. 80-system 18-bit interface.....	55
8.1.2. 80-system 16-bit interface.....	55
8.1.3. 80-system 9-bit interface.....	56
8.1.4. 80-system 8-bit interface.....	57
8.1.5. Serial Peripheral interface (SPI).....	58
8.2. VSYNC INTERFACE.....	60
8.3. EXTERNAL DISPLAY INTERFACE.....	61
8.3.1. 6-bit RGB interface.....	63
8.3.2. 16-bit RGB interface.....	64
8.3.3. 18-bit RGB interface.....	64
8.4. SEQUENCE TO SET BETWEEN SYSTEM INTERFACE AND RGB INTERFACE:.....	65
<b>9. DISPLAY FEATURE FUNCTION:.....</b>	<b>66</b>
9.1. FMARK FUNCTION:.....	66
9.2. SCAN MODE FUNCTION:.....	67
9.3. SCALING FUNCTION:.....	68
9.4. PARTIAL DISPLAY FUNCTION:.....	70
9.5. GAMMA CORRECTION FUNCTIONS:.....	72
<b>10. POWER MANAGEMENT SYSTEM:.....</b>	<b>73</b>
<b>11. APPLICATION CIRCUITS:.....</b>	<b>76</b>
<b>12. INITIAL CODE:.....</b>	<b>77</b>
12.1. SEQUENCE TO EXIT SLEEP MODE:.....	77
<b>13. ELECTRICAL CHARACTERISTICS:.....</b>	<b>78</b>
13.1. ABSOLUTE MAXIMUM RATINGS:.....	78
13.2. DC CHARACTERISTICS.....	78

---

13.3.AC CHARACTERISTICS .....	78
13.3.1. Clock Characteristics.....	78
13.3.2. 80-System Bus Interface Timing Characteristics (18-/ 16- bit interface).....	79
13.3.3. Clock-synchronized Serial Interface Timing Characteristics .....	80
13.3.4. Reset Timing Characteristics (IOVCC=1.65~3.30V).....	81
13.3.5. RGB Interface Timing Characteristics .....	81
<b>14.CHIP INFORMATION .....</b>	<b>83</b>
14.1.PAD ASSIGNMENT .....	83
14.2.PAD DIMENSION .....	83
14.2.1. Output Pads .....	83
14.2.2. Input Pads .....	83
14.3.BUMP CHARACTERISTICS .....	84
14.4.PAD LOCATIONS .....	84
14.5.ALIGNMENT MARK.....	93
<b>15.COG PRODUCTS MANUFACTURING GUIDELINES .....</b>	<b>94</b>
<b>16.DISCLAIMER.....</b>	<b>95</b>
<b>17.REVISION HISTORY .....</b>	<b>96</b>

## 720-channel 6-bit source driver and 320-channel gate driver with System-On-Chip (SOC) for color amorphous TFT LCD

### 1. GENERAL DESCRIPTION

The OTM3225A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx320 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The OTM3225A is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

The built-in timing controller in OTM3225A can support several interfaces for the diverse request of medium or small size portable display. OTM3225A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the OTM3225A incorporates 6, 8, 16, and 18-bit RGB interfaces for picture movement display. The OTM3225A also supports a function to display eight colors and a standby mode for power control consideration.

### 2. FEATURE

- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx320, incorporating a 720-channel source driver and a 320-channel gate driver
- Outputs 64  $\gamma$ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 172800 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces

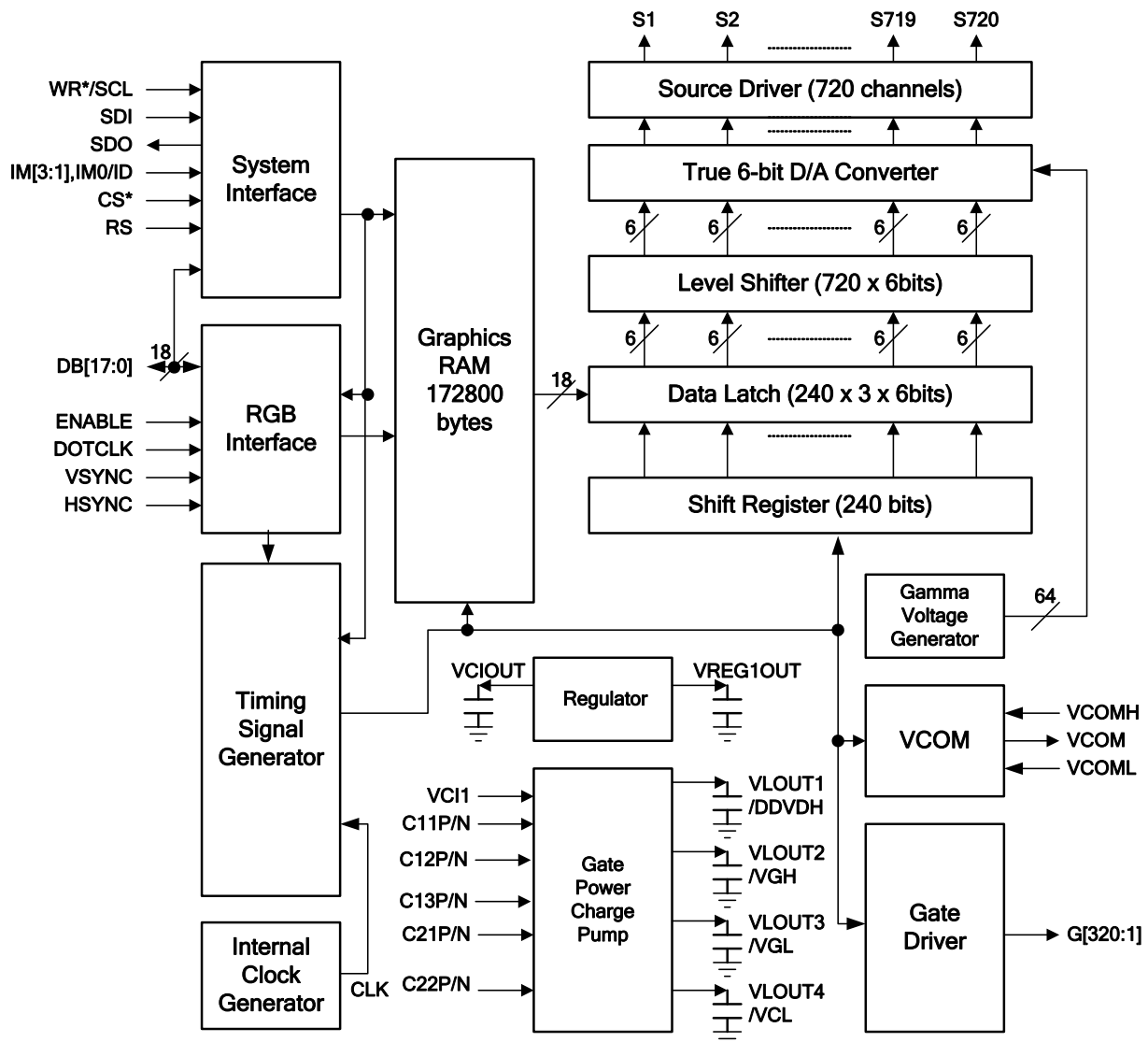
- Intel 80-system with 8-, 9-, 16-, and 18-bit parallel ports
- Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 8-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - I/O interface supply voltage (IOVCC): 1.65 ~ 3.3 V
  - Analog power supply voltage (VCI): 2.5 ~ 3.3 V
- Resize function( x 1/2, x 1/4)
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level: DDVDH-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    - VGH = 10.0V ~20.0V
    - VGL = -4.5V ~ -13.5V
    - VGH – VGL < 30.0V
  - Built-in internal oscillator and hardware reset

### 3. ORDERING INFORMATION

Product Number	Package Type
OTM3225A-C3	Chip Form with Gold Bump

## 4. BLOCK DIAGRAM

### 4.1. Block Function



## 4.2. System Interface

### 4.2.1. Interface

The OTM3225A supports two kind of system interfaces :

1. Intel 80-system interfaces with 8-, 9-, 16-, 18-bits parallel port.
2. Serial Peripheral Interface (SPI).

The OTM3225A has a 16-bit index register (IR) and two 18-bit data registers, a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM or control register.

When graphic data is written to the internal GRAM from MCU's graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the OTM3225A executes the 1<sup>st</sup> read operation. Thus, valid data can be read out after the OTM3225A executes the 2<sup>nd</sup> read operation.

### 4.2.2. External Display Interface

The OTM3225A supports external RGB interface for picture movement display.

The OTM3225A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

### 4.2.3. Address Counter (AC)

OTM3225A features an Address Counter (AC) giving an address

to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

### 4.2.4. Graphics RAM (GRAM)

OTM3225A features a 172800-byte (240 x 320 x 18 / 8) Graphic RAM (GRAM).

### 4.2.5. Grayscale Voltage Generating Circuit

OTM3225A has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the  $\gamma$ -correction register.

### 4.2.6. Timing Controller

OTM3225A has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

### 4.2.7. Oscillator (OSC)

The OTM3225A also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

### 4.2.8. Source Driver Circuit

OTM3225A consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720<sup>th</sup> bit data is input. The latched data controls the source driver and generates a drive waveform.

### 4.2.9. Gate Driver Circuit

OTM3225A consists of a 320-output gate driver circuit (G1~G320). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

### 4.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

**5. SIGNAL DESCRIPTIONS**

Signal	I/O	Connected with	Function																																																																																																																
<b>System Configuration Input Signal</b>																																																																																																																			
IM3~1, IM0/ID	I	GND/ IOVCC	Select an interface mode to MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.																																																																																																																
			<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0/ID</th> <th>Interface Mode</th> <th>DB Pin</th> <th>Colors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>80-system 16-bit interface</td> <td>DB17-10, DB8-1</td> <td>262,144 or 65,536</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>80-system 8-bit interface</td> <td>DB17-10</td> <td>262,144 or 65,536</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>*(ID)</td> <td>Clock synchronous serial interface</td> <td>-</td> <td>262,144 or 65,536</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>80-system 18-bit interface</td> <td>DB17-0</td> <td>262,144 only</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>80-system 9-bit interface</td> <td>DB17-9</td> <td>262,144 only</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin	Colors	0	0	0	0	Setting disabled	-	-	0	0	0	1	Setting disabled	-	-	0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 or 65,536	0	0	1	1	80-system 8-bit interface	DB17-10	262,144 or 65,536	0	1	0	*(ID)	Clock synchronous serial interface	-	262,144 or 65,536	0	1	1	0	Setting disabled	-	-	0	1	1	1	Setting disabled	-	-	1	0	0	0	Setting disabled	-	-	1	0	0	1	Setting disabled	-	-	1	0	1	0	80-system 18-bit interface	DB17-0	262,144 only	1	0	1	1	80-system 9-bit interface	DB17-9	262,144 only	1	1	0	0	Setting disabled	-	-	1	1	0	1	Setting disabled	-	-	1	1	1	0	Setting disabled	-	-	1	1	1	1	Setting disabled	-	-
			IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin	Colors																																																																																																										
			0	0	0	0	Setting disabled	-	-																																																																																																										
			0	0	0	1	Setting disabled	-	-																																																																																																										
			0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 or 65,536																																																																																																										
			0	0	1	1	80-system 8-bit interface	DB17-10	262,144 or 65,536																																																																																																										
			0	1	0	*(ID)	Clock synchronous serial interface	-	262,144 or 65,536																																																																																																										
			0	1	1	0	Setting disabled	-	-																																																																																																										
			0	1	1	1	Setting disabled	-	-																																																																																																										
			1	0	0	0	Setting disabled	-	-																																																																																																										
			1	0	0	1	Setting disabled	-	-																																																																																																										
			1	0	1	0	80-system 18-bit interface	DB17-0	262,144 only																																																																																																										
			1	0	1	1	80-system 9-bit interface	DB17-9	262,144 only																																																																																																										
			1	1	0	0	Setting disabled	-	-																																																																																																										
1	1	0	1	Setting disabled	-	-																																																																																																													
1	1	1	0	Setting disabled	-	-																																																																																																													
1	1	1	1	Setting disabled	-	-																																																																																																													
/RESET	I	MPU	RESET pin. This is an active low signal.																																																																																																																
<b>Interface input Signals</b>																																																																																																																			
/CS	I	MPU	Chip select signal. Low: the OTM3225A is accessible. High: the OTM3225A is not accessible. Must connect to the IOVCC level when not used.																																																																																																																
RS	I	MPU	Register select signal. Low: Index register or internal status is selected. High: Control register is selected. Must connect to the GND or IOVCC level when not used.																																																																																																																
(/WR) / (SCL)	I	MPU	(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low. (B) In SPI mode, served as a synchronizing clock signal.																																																																																																																
/RD	I	MPU	In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. Must connect to the GND or IOVCC level when not in use.																																																																																																																
SDI	I	MPU	Series Data is the input on the rising edge of the SCL signal in SPI mode. Must connect to the GND or IOVCC level when not in use.																																																																																																																
SDO	O	MPU	Series Data is the output on the rising edge of the SCL signal in SPI mode. Must keep this pin open(floating) when not used. Can not connect to the GND or IOVCC level when not in use.																																																																																																																

Signal	I/O	Connected with	Function																				
DB0-DB17	I/O	MPU	<p>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:</p> <table border="1"> <thead> <tr> <th>Mode</th> <th>Pin Assignment</th> </tr> </thead> <tbody> <tr> <td>8-bit system interface</td> <td>DB17-DB10</td> </tr> <tr> <td>9-bit system interface</td> <td>DB17-DB9</td> </tr> <tr> <td>16-bit system interface</td> <td>DB17-DB10, DB8-DB1</td> </tr> <tr> <td>18-bit system interface</td> <td>DB17-DB0</td> </tr> <tr> <td>6-bit External (RGB) interface</td> <td>DB17-DB12</td> </tr> <tr> <td>8-bit External (RGB) interface</td> <td>DB17-DB10</td> </tr> <tr> <td>16-bit External (RGB) interface</td> <td>DB17-13, DB11-DB1</td> </tr> <tr> <td>18-bit External (RGB) interface</td> <td>DB17-DB0</td> </tr> <tr> <td>Serial interface(SPI)</td> <td>Not use</td> </tr> </tbody> </table> <p>Must connect to the GND or IOVCC level when not in use.</p>	Mode	Pin Assignment	8-bit system interface	DB17-DB10	9-bit system interface	DB17-DB9	16-bit system interface	DB17-DB10, DB8-DB1	18-bit system interface	DB17-DB0	6-bit External (RGB) interface	DB17-DB12	8-bit External (RGB) interface	DB17-DB10	16-bit External (RGB) interface	DB17-13, DB11-DB1	18-bit External (RGB) interface	DB17-DB0	Serial interface(SPI)	Not use
Mode	Pin Assignment																						
8-bit system interface	DB17-DB10																						
9-bit system interface	DB17-DB9																						
16-bit system interface	DB17-DB10, DB8-DB1																						
18-bit system interface	DB17-DB0																						
6-bit External (RGB) interface	DB17-DB12																						
8-bit External (RGB) interface	DB17-DB10																						
16-bit External (RGB) interface	DB17-13, DB11-DB1																						
18-bit External (RGB) interface	DB17-DB0																						
Serial interface(SPI)	Not use																						
VSYNC	I	MPU	<p>In external RGB interface mode, served as a vertical synchronize signal input Must connect to the IOVCC or GND level when not in use.</p>																				
HSYNC	I	MPU	<p>In external RGB interface mode, served as a horizontal synchronized signal input Must connect to the IOVCC or GND level when not used.</p>																				
ENABLE	I	MPU	<p>In external RGB interface mode, polarity of ENABLE signal is synchronized with valid graphic data input. Low: Valid data on DB17-DB0 (relative to different interface modes) High: Invalid data on DB17-DB0 (relative to different interface modes) Moreover, setting EPL bit can change the polarity of the ENABLE signal. Must connect to the GND or IOVCC level when not in use.</p>																				
DOTCLK	I	MPU	<p>In external RGB interface mode, served as a dot clock signal. When DPL = "0": Input data on the rising edge of DOTCLK When DPL = "1": Input data on the falling edge of DOTCLK It is fixed to the IOVCC or GND level when not in use.</p>																				
FMARK	O	MPU	<p>Frame head pulse signal, which is used when writing data to the internal RAM. Must keep this pin open(floating) when not used. Can not connect to the GND or IOVCC level when not in use.</p>																				
<b>Charge Pump and Power Supply Signal</b>																							
C11P/N, C12P/N C13P/N C21P/N, C22P/N	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins.																				
VCI1	I/O	Stabilizing capacitor	Reference voltage of step-up circuit 1. Make sure the output voltage levels from DDVDH, VGH, and VGL do not exceed the respective setting ranges.																				
DDVDH	I	Stabilizing capacitor	Power supply for the source driver liquid crystal drive unit and VCOM drive. DDVDH = 4.5V ~ 6.0V																				
VGH	I	Stabilizing capacitor	Liquid crystal drive power supply.																				
VGL	I	Stabilizing capacitor	Liquid crystal drive power supply.																				
VCL	O	Stabilizing	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~																				

Signal	I/O	Connected with	Function
		capacitor	-3.0V
VPP2	I	Power supply or open	Power supply for OTP programming.
<b>Source/Gate Driver and VCOM Signals</b>			
G1~G320	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage is output.
VREG1OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCI or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for : (1) source driver grayscale reference voltage (2) VCOMH level reference voltage (3) VCOM amplitude reference voltage Connect to a stabilizing capacitor when in use. $VREG1OUT = 4.0V \sim (DDVDH - 0.5)V$
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). $VCOML = (VCL+0.5) V \sim 0V$ . Make sure to connect to stabilizing capacitor.
VGS	I	GND	Reference level for the grayscale voltage generating circuit.
GND	P	Power supply	Internal logic GND: $GND = 0V$ .
RGND	P	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.
IOVCC	P	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. $IOVCC = 1.65V \sim 3.3V$ . Note: Must keep $VCI \geq IOVCC$ .
AGND	P	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): $AGND = 0V$ . In case of COG, connect to GND on the FPC to prevent noise.
VCI	P	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of $2.5V \sim 3.3V$ .
<b>Misc. Signal</b>			
I0GND	I/O	Open	Test pins. Leave them open.
DUMMY1~15 DUMMY20~27	I/O	Open	Test pins. Leave them open.
TEST02~16	I/O	Open	Test pins. Leave them open.
TEST1~3	I/O	Open	Test pins. Leave them open.
TS0~8	I/O	Open	Test pins. Leave them open

## 6. INSTRUCTIONS

### 6.1. Outline

The OTM3225A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for OTM3225A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80 system and SPI). The corresponding pin assignment of different system interface are shown in Figure 6-1 to Figure 6-5

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale  $\gamma$ -correction

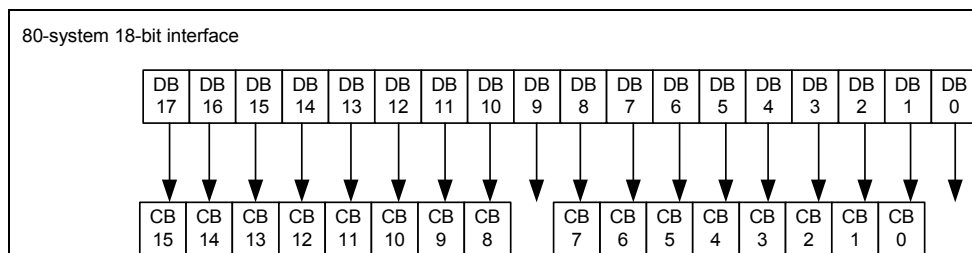


Figure 6-1 : I80-system 18bits interface data transfer format

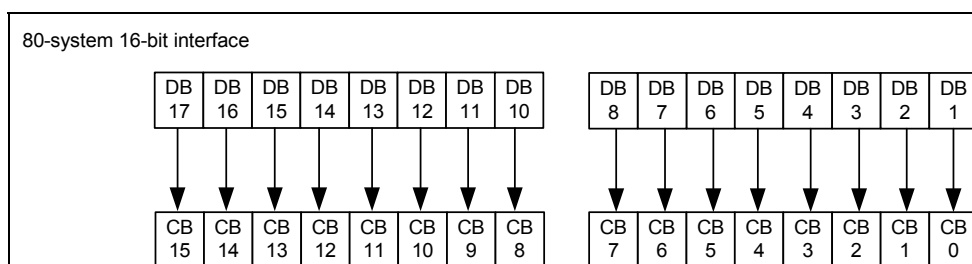


Figure 6-2 : I80-system 16bits interface data transfer format

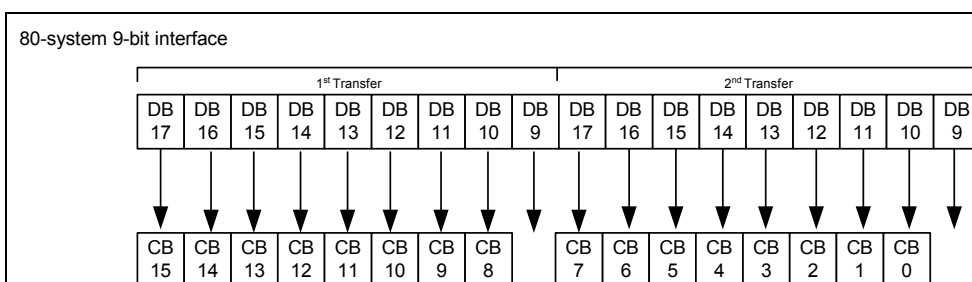


Figure 6-3 : I80-system 9bits interface data transfer format

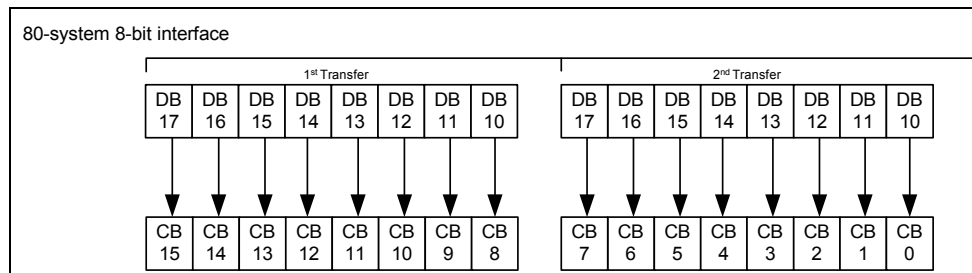
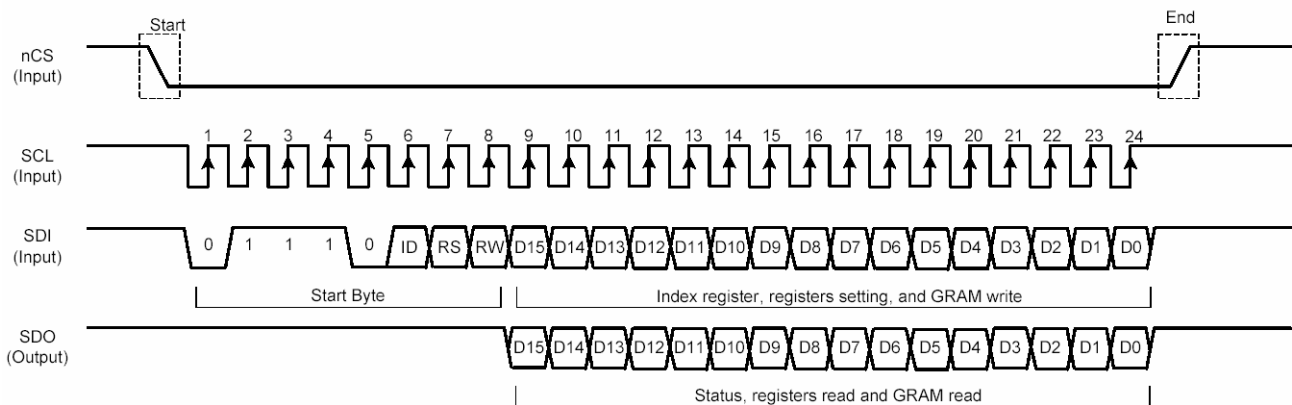


Figure 6-4 : I80 8bits interface data transfer format

(a) Basic data transmission through SPI



(b) Consecutive data transmission through SPI

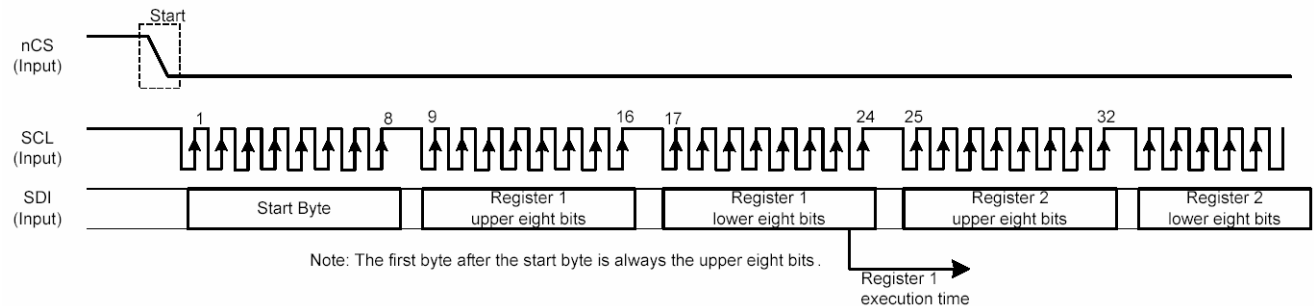


Figure 6-5 : Serial interface data transfer format

## 6.2. Instruction

**Table 6-1 Instruction List Table**

Register No	Register	Upper 8-bit								Lower 8-bit							
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
00h	ID Read	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	
01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0	
02h	LCD Drive Waveform Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	0	0	0	0	0	
03h	Entry Mode	TRIREG (0)	DFM (0)	0	BGR (0)	0	0	0	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0	
04h	Scaling Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	0	
07h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	0	GON (0)	DTE (0)	CL (0)	0	D1 (0)	
08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	
09h	Display Control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (1)	
0Ah	Frame Cycle Control	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	
0Ch	External Display interface control (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	
0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	
0Fh	External Display interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSP (0)	0	EPL (0)	
10h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	AP2 (1)	AP1 (0)	AP0 (0)	0	0	SLP (0)	
11h	Power Control (2)	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (1)	0	DC02 (1)	DC01 (1)	DC00 (1)	0	VC2 (0)	VC1 (0)	
12h	Power Control (3)	0	0	0	0	0	0	0	0	VCIRE (0)	0	0	1	VRH3 (0)	VRH2 (0)	VRH1 (0)	
13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	
20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	
21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	
22h		Write Data to GRAM Read Data from GRAM															
29h	Power Control (7)	0	0	0	0	0	0	0	0	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	
2Bh	Frame Rate Control	0	0	0	0	0	0	0	0	0	0	0	FRS3 (1)	FRS2 (0)	FRS1 (1)	FRS0 (1)	
30h	$\gamma$ Control (1)	0	0	0	0	0	KP1[2] (0)	KP1[1] (0)	KP1[0] (0)	0	0	0	0	0	KP0[2] (1)	KP0[1] (0)	
31h	$\gamma$ Control (2)	0	0	0	0	0	KP3[2] (0)	KP3[1] (1)	KP3[0] (1)	0	0	0	0	0	KP2[2] (1)	KP2[1] (1)	
32h	$\gamma$ Control (3)	0	0	0	0	0	KP5[2] (0)	KP5[1] (0)	KP5[0] (0)	0	0	0	0	0	KP4[2] (0)	KP4[1] (1)	
35h	$\gamma$ Control (4)	0	0	0	0	0	RP1[2] (0)	RP1[2] (1)	RP1[0] (1)	0	0	0	0	0	RP0[2] (1)	RP0[2] (1)	
36h	$\gamma$ Control (5)	0	0	0	VRP1[4] (0)	VRP1[3] (1)	VRP1[2] (1)	VRP1[1] (1)	VRP1[0] (0)	0	0	0	VRP0[4] (0)	VRP0[3] (0)	VRP0[2] (1)	VRP0[1] (1)	
37h	$\gamma$ Control (6)	0	0	0	0	0	KN1[2] (1)	KN1[1] (0)	KN1[0] (0)	0	0	0	0	0	KN0[2] (1)	KN0[1] (1)	
38h	$\gamma$ Control (7)	0	0	0	0	0	KN3[2] (0)	KN3[1] (1)	KN3[0] (1)	0	0	0	0	0	KN2[2] (1)	KN2[1] (1)	
39h	$\gamma$ Control (8)	0	0	0	0	0	KN5[2] (0)	KN5[1] (1)	KN5[0] (1)	0	0	0	0	0	KN4[2] (1)	KN4[1] (1)	
3Ch	$\gamma$ Control (9)	0	0	0	0	0	RN1[2] (0)	RN1[1] (1)	RN1[0] (1)	0	0	0	0	0	RN0[2] (0)	RN0[1] (1)	
3Dh	$\gamma$ Control (10)	0	0	0	VRN1[4] (0)	VRN1[3] (0)	VRN1[2] (1)	VRN1[1] (0)	VRN1[0] (0)	0	0	0	VRN0[4] (0)	VRN0[3] (1)	VRN0[2] (0)	VRN0[1] (1)	
50h	Window Horizontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	
51h	Window Horizontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	
52h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	
53h	Window Vertical RAM Address End	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	
60h	Driver Output Control	GS (0)	0	NL5 (1)	NL4 (0)	NL3 (0)	NL2 (1)	NL1 (1)	NL0 (1)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	
61h	Driver Output Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	
6Ah	Vertical Scroll Control	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	
80h	Display Position - Partial Display 1	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	
81h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	
82h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	
83h	Display Position - Partial Display 2	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	

84h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)
85h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)
90h	Panel interface Control 1	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)
92h	Panel Interface Control 2	0	0	0	0	0	NOWI2 (1)	NOWI1 (1)	NOWI0 (0)	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)
97h	Panel Interface Control 5	0	0	0	0	0	NOWE3 (1)	NOWE2 (1)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	0	0	0

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

### 6.2.1. Index Register (IR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h ~ RFFh) of a control register or RAM. The index range is from "0000\_0000" to "1111\_1111" in binary format.

### 6.2.2. ID Read Register (SR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

The IC code of OTM3225A can be accessed by read operation. The 16-bits ID Code can be read out when read ID operation is executed. The ID information can be set from 0x0000h to 0xFFFFh by IC metal option for customer's request.

### 6.2.3. Driver Output Control Register (R01h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0

**SS:** Shift direction of the source driver output selection.

When SS = "0", source driver shift from S1 to S720.

When SS = "1", source driver shift from S720 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 6-2**.

★**Note:** After changing SS bit or BGR bit, display data must be rewritten.

Table 6-2

SS=0;BGR=0;	S1	S2	S3	→	S718	S719	S720
SS=0;BGR=1;	S1	S2	S3	→	S718	S719	S720
SS=1;BGR=0;	S1	S2	S3	←	S718	S719	S720
SS=1;BGR=1;	S1	S2	S3	←	S718	S719	S720

**SM:** Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 6-3** and **Figure 6-6**.

Table 6-3

SM	GS	Gate output sequence (Begin,.....,End)
0	0	G1→G2→G3→G4→.....→G317→G318→G319→G320
0	1	G320→G319→G318→G317→.....→G4→G3→G2→G1
1	0	G1→G3→G5→.....→G317→G319→ →G2→G4→G6→.....→G318→G320
1	1	G320→G318→G316→.....→G4→G2→ →G319→G317→G315→.....→G3→G1

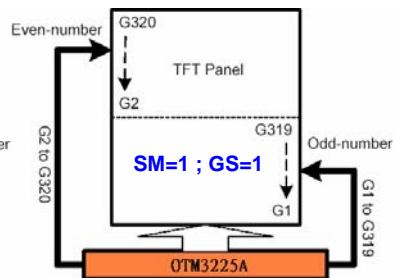
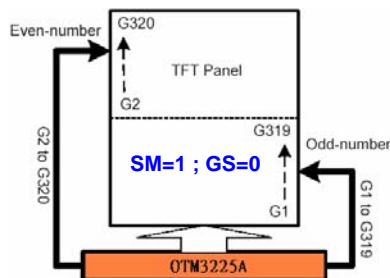
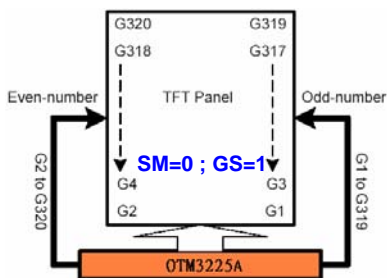
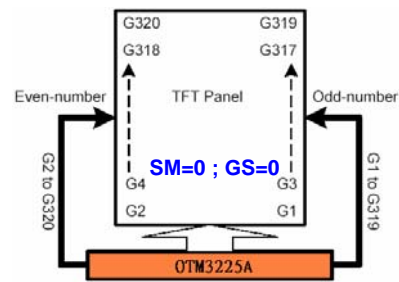


Figure 6-6 : Panel layout for SM & GS bit

### 6.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0

**BC0:** This bit can set the VCOM toggle at ever frame format or N-line inversion format.

BC0=0: Frame inversion waveform is selected.

BC0=1: Line inversion waveform is selected. (Must combine EOR=1 for Line inversion)

**EOR:** Enables Line-inversion when EOR=1 and BC0=1.

### 6.2.5. Entry Mode (R03h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0

**Table 6-4**

Operation mode	ORG	AM	I/D1	I/D0	Function
Mode 1	0	0	0	0	Replace horizontal data
Mode2	0	1	0	1	Replace vertical data
Mode3	1	0	1	0	Conditionally replace horizontal data
Mode4	1	1	1	1	Conditionally replace vertical data

★**Note:** After changing ORG;AM;I/D1 or I/D0 bit, display data must be rewritten.

**AM:** To set the update direction when writing data to GRAM.

If AM=1, data will write in vertical direction. (Address counter will automatic update in vertical direction)

If AM=0, data will write in horizontal direction. (Address counter will automatic update in horizontal direction)

When setting a window area by register R50h~R53h, the data is written only within the area based on by I/D[1:0],AM bit.

**I/D1-0:** To specify address counter(AC) automatically increment or decrement while update one pixel display data to GRAM.

I/D[0] indicates the increment or decrement in horizontal direction.

I/D[0]=0: decrement in horizontal direction automatically

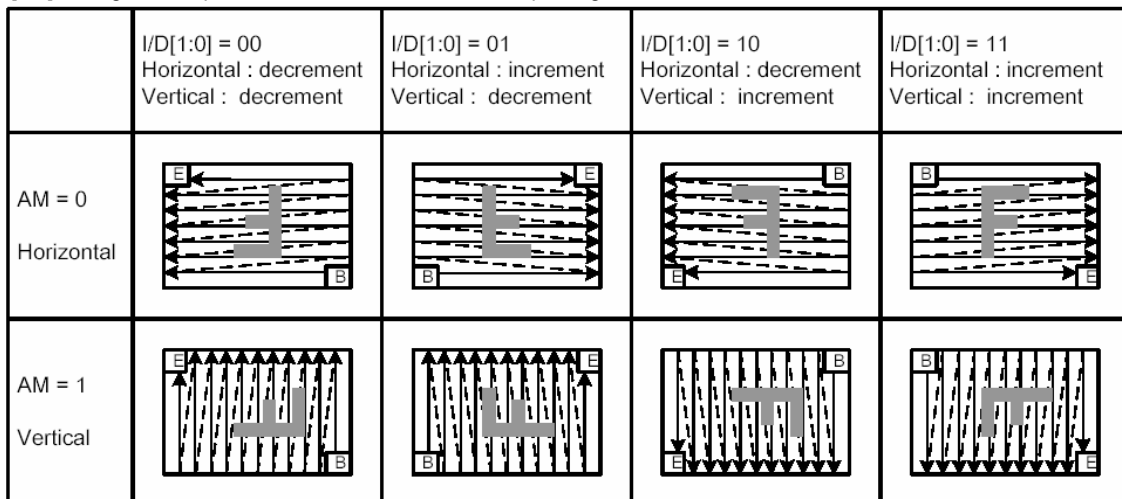
I/D[0]=1: increment in horizontal direction automatically

I/D[1] indicates the increment or decrement in vertical direction.

I/D[1]=0: decrement in vertical direction automatically

I/D[1]=1: increment in vertical direction automatically

ID[1-0] setting can cooperate with Am bit to set the data updating direction.



**Figure 6.7**

**ORG:** OTM3225A provides the option of start address definition when window function is selected.

ORG=0: RAM address setting (R20h, R21h) should set to the window start address, as normal operation case.

In this case, the origin address is not move.

ORG=1: RAM address setting (R20h, R21h) should set to (0x0000h) no matter where the window start address is.

Setting other addresses is inhibited.

In this case, the window start position is treated as (0x0000h), regardless the physical location in GRAM.

★**Note:** In GRAM read operation(R22h), make sure to set ORG=0.

★**Note:** In RGB mode with Full-Screen operation, make sure to set ORG=1.

**BGR:** To set the order of RGB sub-pixel in GRAM.

The combination of SS and BGR bit are summarized at **Table 6-2**.

BGR=0: same assignment of RGB allocation of DB17-0.																	
DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
BGR=1: inverse assignment of RGB allocation of DB17-0.																	
DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

**Figure 6.8**

**DFM:** In combination with TRI setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM=0 when not transferring data via 16-bit or 8-bit interface.

**TRI:** to set 1–3 time transfer mode for system interface. TRI bit should cooperate with DFM to meet the specific transfer mode.

For 8-bit data bus interface mode:

TRI=0: 2 time transfer mode for 16-bit GRAM data.

TRI=1: 3 time transfer mode for 18-bit GRAM data

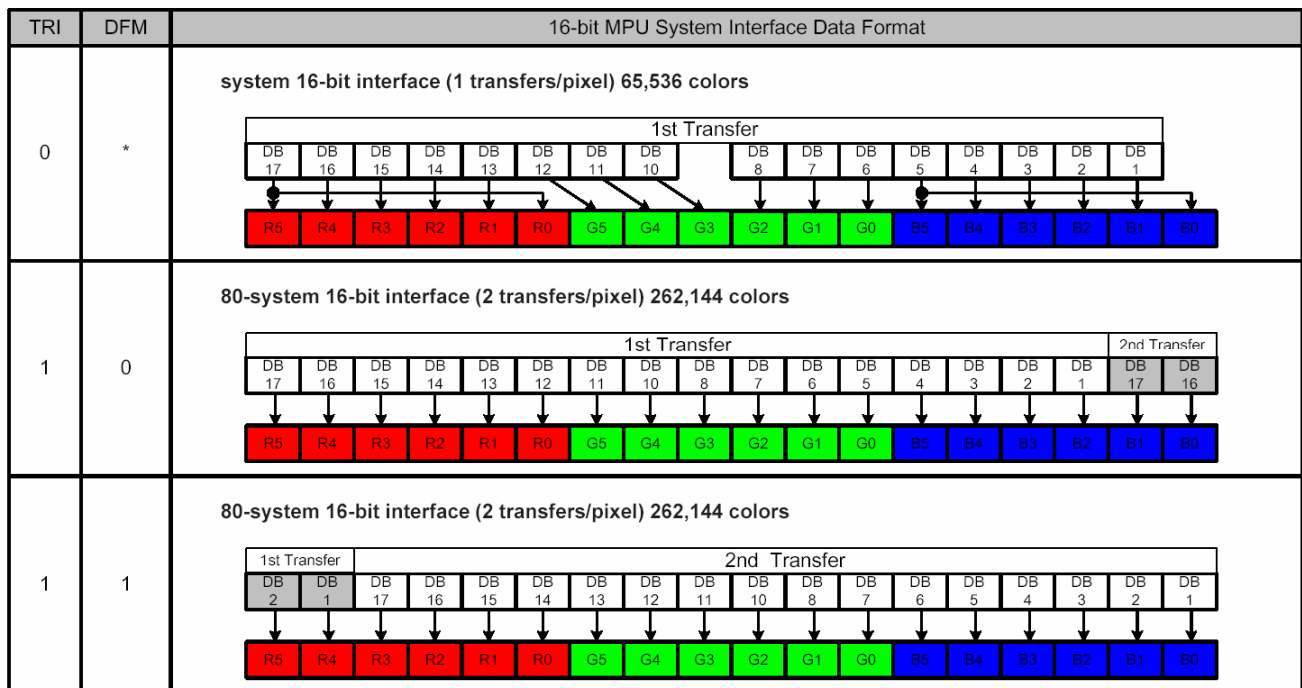
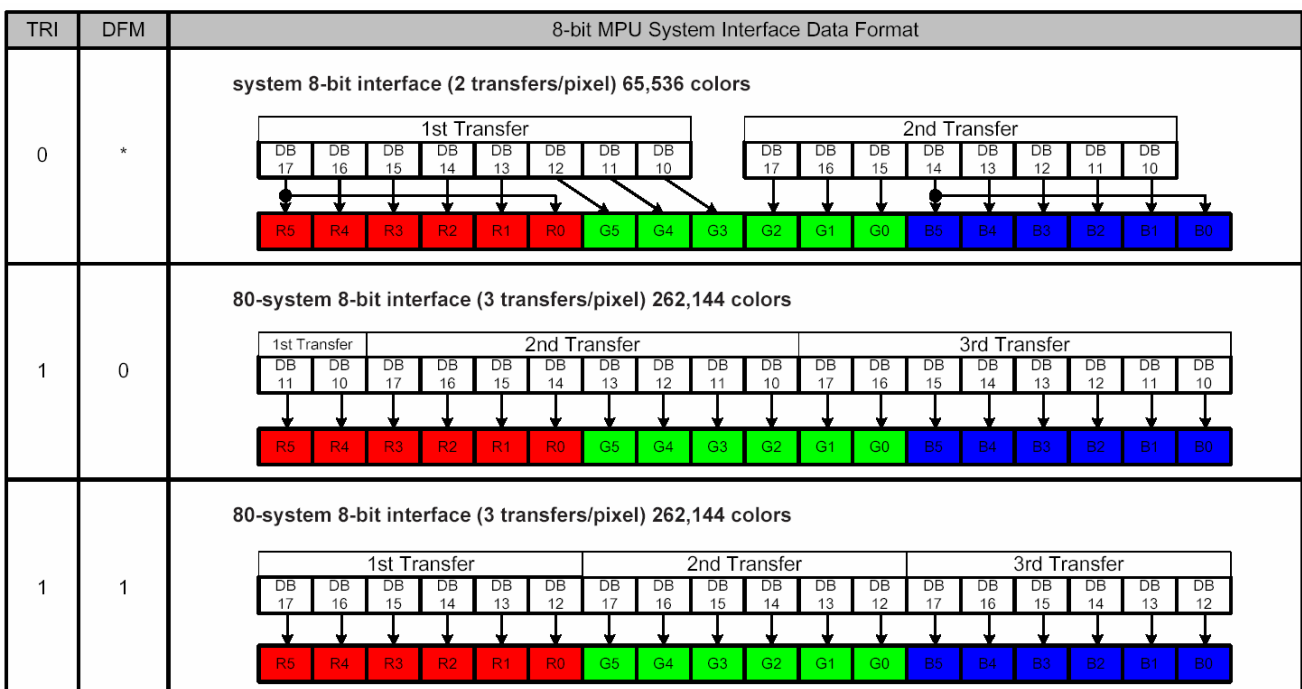
For 16-bit data bus interface mode:

TRI=0: 1 time transfer mode for 16-bit GRAM data.

TRI=1: 2 time transfer mode for 18-bit GRAM data

★**Note:** Set TRI=0, when using neither 8-bit nor 16-bit.

★**Note:** The combination of DFM and TRI bit are summarized at **Table 6-2**.


**Figure 6.9**

**Figure 6.10**

### 6.2.6. Scaling Control register (R04h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

**RSZ [1:0]:** OTM3225A provides scaling factor to give the display more flexibility to show different picture size. For detail, refer to “Scaling function”.

RSZ1	RSZ0	Scaling Factor
0	0	No Scaling
0	1	1/2 times
1	0	Setting Disable
1	1	1/4 times

**RCH [1:0]:** To set the surplus pixel number in horizontal direction when scaling mode is selected. When scaling mode is not selected, make sure RCH [1:0]= “00”

RCH1	RCH0	Surplus pixel number in Horizontal direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

**RCV [1:0]:** To set the surplus pixel number in Vertical direction when scaling mode is selected. When scaling mode is not selected, make sure RCV [1:0]= “00”

RCV1	RCV0	Surplus pixel number in Vertical direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

### 6.2.7. Display Control (R07h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	COL	0	D1	D0

**D1-0:** To set the internal operation, source driver output and VCOM output function. When D1-0=00; OTM3225A is set to standby mode. The combination of D1 and AM bit is summarized at **Table 6-5**.

**Table 6-5**

D1	BASEE	Source, VCOM output	Internal Operation	FLM
0	*	GND	Terminated	OFF
1	0	Non-lit display	Normal Operation	ON
	1	Normal display	Normal Operation	ON

**COL:** 8-color mode selection. When CL=1 OTM3225A enter to 8-color mode. When CL=0, OTM3225A is in normal operation mode.

**DTE:** Specify the high/low level of gate driver output signal. The meaning of DTE bit is summarized at **Table 6-6**

**Table 6-6**

APE	DTE	Gate Output
1	0	VGL
	1	VGH/VGL

**BASEE:** To enable Base image display

BASEE	Display
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

**PTDE1-0:** To set the partial-display enables function.

PTDE [0]: "0" Partial image 1 display "Off".

"1" Partial image 1 display "On".

PTDE [1]: "0" Partial image 2 display "Off".

"1" Partial image 2 display "On".

**6.2.8. Display Control 2 (R08h)**

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

**FP3-0:** Set the amount of blank period of front porch

**BP3-0:** Set the amount of blank period of back porch

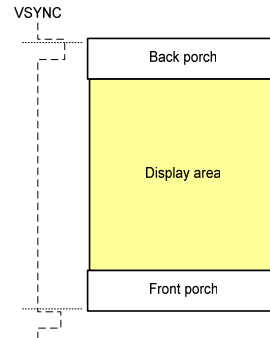
**Table 6-7** summarized the function of FP3-0/BP3-0 setting.

When setting this register, make sure that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines



**Figure 6-11** Front porch and back porch function diagram

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 6-8** summarized the setting for each interface mode.

**Table 6-7**

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	1 lines
0	0	0	1	1 lines
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	15 lines

**Table 6-8**

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

### 6.2.9. Display Control 3 (R09h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

**ISC3-0:** To set the gate driver scan cycle in non-display area.

Table 6-9 summarized the function of ISC3-0 setting

**Table 6-9**

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	0	1 Frames	16ms
0	0	0	1	1 Frames	16ms
0	0	1	0	3 Frames	50 ms
0	0	1	1	5 Frames	84 ms
0	1	0	0	7 Frames	117 ms
0	1	0	1	9 Frames	150 ms
0	1	1	0	11 Frames	184 ms
0	1	1	1	13 Frames	217 ms

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
1	0	0	0	15 Frames	251 ms
1	0	0	1	19 Frames	317 ms
1	0	1	0	21 Frames	351 ms
1	0	1	1	23 Frames	384 ms
1	1	0	0	25 Frames	418 ms
1	1	0	1	27 Frames	451 ms
1	1	1	0	29 Frames	484 ms
1	1	1	1	31 Frames	518 ms

**PTG1-0:** To set the gate driver scan mode in non-display area.

Table 6-10 summarized the function of PTG1-0 setting

**Table 6-10**

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
0	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	0	Interval scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML

**PTS2-0:** To set the source driver output level in non-display area of partial display mode. Table 6-11 summarized the function of PTS2-0 setting.

**Table 6-11**

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area	Display in non-display area (Normally White panel)
			+ polarity	- polarity		
0	0	0	V63	V0	V0~V63	White
0	0	1	V0	V63	V0~V63	Black
0	1	0	GND	GND	V0~V63	White
0	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)
1	0	0	V63	V0	V0~V63	White
1	0	1	V0	V63	V0~V63	Black
1	1	0	GND	GND	V0~V63	White
1	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)

### 6.2.10. Frame Cycle Control (R0Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARK OE	FMI2	FMI1	FMI0

**FMI [2:0]: (FMark Interval)** OTM3225A provide FMARK signal to prevent tearing effect. FMI [2:0] can set FMARK output interval.

FMI2	FMI1	FMI0	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames
1	1	1	8 frames

**FMARKOE: (FMARK Output Enable)** Set the output signal FMARK from FMARK pin.

FMARK="0": Stop to output FMARK signal.

FMARK="1": Start to output FMARK signal.

**6.2.11. External Display Interface Control 1 (R0Ch)**

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

**RIM1-0:** To set the different transfer modes of RGB interface. **Table 6-12** summarized the function of RIM1-0 setting.

**Table 6-12**

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus	Number of transfer during 1 line
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0	240x18-bits (AM bit=0) 320x18-bits (AM bit=1)
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1	240x16-bits (AM bit=0) 320x16-bits (AM bit=1)
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12	720x6-bits (AM bit=0) 960x6-bits (AM bit=1)
1	1	8-bit RGB interface (two transfers/pixel)	65K	DB17-10	480x8-bits (AM bit=0) 640x8-bits (AM bit=1)

**DM1-0:** To specify the display interface mode. DM1-0 Setting can switch the display interface among system interface, RGB interface and VSYNC interface. **Table 6-13** summarized the function of DM1-0 setting.

**Table 6-13**

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

**RM:** Select the interface to access the OTM3225A's internal GRAM. Set RM to "1" when writing display data via the RGB interface. The OTM3225A allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

**Table 6-14** summarized the function of RM bit setting.

**Table 6-14**

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

**Table 6-15**

Display State	Operation Mode	RAM access Mode(RM)	Display operation Mode (DM1-0)
Still pictures	Internal clock	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)
Low Speed moving picture	RGB interface	RGB interface (RM = 1)	Internal clock operation (DM1-0 = 00)

**Note1:** Instructions are set only via the system interface.

**Note2:** Do not make changes to the RGB-I/F mode setting (RIM-0) while the RGB I/F is in operation.

**Note3:** See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

**6.2.12. Frame Maker Position (R0Dh)**

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

**FMP 8-0:** Indicates the output position of frame cycle signal (FMARK).

A high-active pulse is output from FMARK pin and It's relate with back porch.

When FMP[8:0] =9'h000, FMARK is outputted at the start of back porch for 1line period.

When FMP[8:0] =9'h001, FMARK is outputted one line after the start of back porch.

Please reference "9.1. FMARK function" for detail description.

FMP [8:0]	FMARK Output Position
9'h000	Immediate (Delay 0 line period)
9'h001	Delay 1 line period
9'h002	Delay 2 lines period
	~
Max. Vaule	$9'h000 \leq FMP[8:0] \leq BP+NL+FP$

**6.2.13. External Display Interface Control 2 (R0Fh)**

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

**EPL:** The polarity of ENABLE signal selection in RGB interface mode.

EPL = "0": ENABLE: Low active

EPL = "1": ENABLE: High active

**DPL:** Select the data latch edge of the DOTCLK signal in RGB interface mode.

DPL = "0": rising edge of the DOTCLK.

DPL = "1": falling edge of the DOTCLK.

**VSPL:** The polarity of VSYNC signal selection in RGB interface mode.

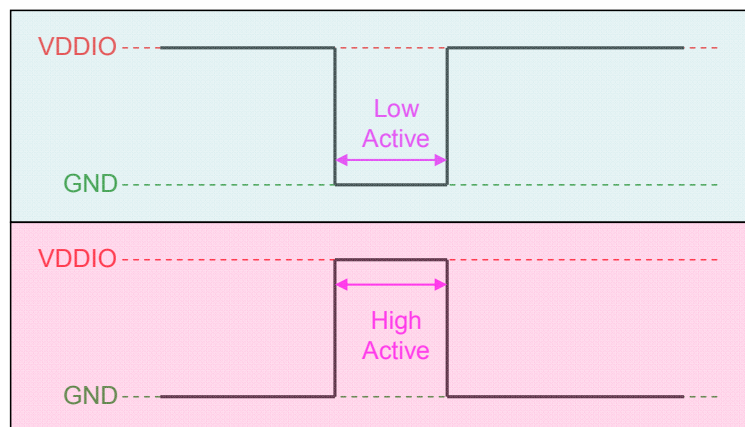
VSPL = "0": Low active.

VSPL = "1": High active.

**HSPL:** The polarity of HSYNC signal selection in RGB interface mode.

HSPL = "0": Low active.

HSPL = "1": High active.



**Figure 6.12**

**6.2.14. Power Control 1 (R10h)**

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB

**SLP:** Sleep mode selection. When SLP =1, OTM3225A set to sleep mode. In sleep mode, all internal operations are terminated except internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to "1". In sleep mode, no instruction can be accepted except R11h, R13h, bit 3-0 of R12h and R10h (except SAP2-0). Set STB=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are keep the same with these before set to SLP mode.

**STB:** Standby mode selection. When STB =1, OTM3225A set to standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set STB to "1". Set STB=0 can exit standby mode. Be sure that start oscillation following by 10ms delay should be executed before set STB to "0". Moreover, when exit from standby mode, data in GRAM and register will not lost, reset and re-sending command and data into GRAM is not necessary.

**AP2-0:** Operational amplifier DC bias current adjustment. Set AP2-0 = "000" to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during no display period.

**APE:** Enable bit for both liquid crystal power supply and gamma voltage generation circuit.

APE="0", Halt liquid crystal power supply and gamma voltage generation circuit

APE="1", Enable liquid crystal power supply and gamma voltage generation circuit.

**BT3-0:** Set the voltage level of DDVDH, VGH, VGL and VCL.

**Table 6-16** summarized the function of BT3-0 setting

BT2	BT1	BT0	DDVDH	VGH	VGL	VCL
0	0	0	VCI1 x 2	VCI1 x 6	VCI1x -5	-VCI1
0	0	1	VCI1 x 2	VCI1 x 6	VCI1x -4	-VCI1
0	1	0	VCI1 x 2	VCI1 x 6	VCI1x -3	-VCI1
0	1	1	VCI1 x 2	VCI1 x 5	VCI1x -5	-VCI1
1	0	0	VCI1 x 2	VCI1 x 5	VCI1x -4	-VCI1
1	0	1	VCI1 x 2	VCI1 x 5	VCI1x -3	-VCI1
1	1	0	VCI1 x 2	VCI1 x 4	VCI1x -4	-VCI1
1	1	1	VCI1 x 2	VCI1 x 4	VCI1x -3	-VCI1

**SAP:** Enable bit for gamma voltage generation circuit.

SAP="0", Halt gamma voltage generation circuit.

SAP="1", Enable gamma voltage generation circuit











































































































































