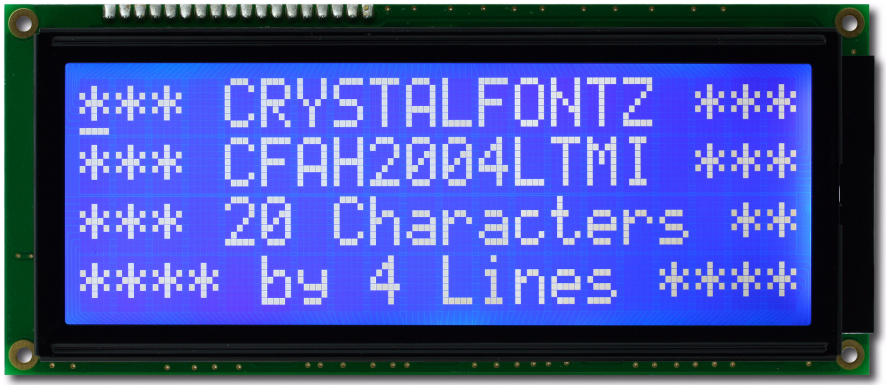
Crystalfontz America, Incorporated

CHARACTER LCD MODULE SPECIFICATIONS



Crystalfontz Model Number	**CFAH2004L-TMI-JT**
Hardware Version	**Revision D**
Data Sheet Version	**Revision 1.0, November 2008**
Product Pages	www.crystalfontz.com/product/CFAH2004L-TMI-JT.html

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REVISION HISTORY

HARDWARE	
2008/11/15	Current hardware version: **vD** This new “-JT” module replaces the discontinued “-JP” module.

DATA SHEET	
2008/11/15	Current Data Sheet version: **v1.0** New Data Sheet.

The Fine Print

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MAIN FEATURES

- 20 characters by 2 lines LCD has a large display area in a 146.0 (W) x 62.5 (H) x 13.6 (D) millimeter package (5.75" (W) x 2.46" (H) x 0.54" (D)).
- 4-bit or 8-bit parallel interface.
- Standard Hitachi HD44780 equivalent controller.
- White edge LED backlight with STN, negative, blue, transmissive mode LCD (displays light characters on blue background).
- Wide temperature operation: -20°C to +70°C.
- RoHS compliant.

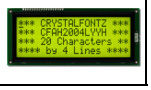
MODULE CLASSIFICATION INFORMATION

CFA H 20 04 L - T M I - J T *
❶ ❷ ❸ ❹ ❺ ❻ ❼ ❽ ❾ ❿ ⓫

❶	Brand	Crystalfontz America, Inc.
❷	Display Type	H – Character
❸	Number of Characters (Width)	20 Characters
❹	Number of Lines (Height)	4 Lines
❺	Model Identifier	L
❻	Backlight Type & Color	T – LED, white
❼	Fluid Type, Image (Positive or Negative), & LCD Glass Color	M – STN, negative, blue
❽	Polarizer Film Type, Wide (WT) Temperature Range, & Viewing Angle (O'clock)	I – Transmissive, WT, 6:00[1]
❾	Character Set (CGROM)	J – English and Japanese fonts
❿	Controller	T – Sitronix ST7066U
⓫	Special Codes	* – May have additional manufacturer's codes at this location.

[1] *Note: For more information on Viewing Angle, see Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles (Pg. 16).*

ORDERING INFORMATION

PART NUMBER	FLUID	LCD GLASS COLOR	IMAGE	POLARIZER FILM	BACKLIGHT COLOR/TYPE
CFAH2004L-TMI-JT	STN	blue	negative	transmissive	white LED
Additional variants (same form factor, different LCD mode or backlight):					
CFAH2004L-NYG-ET	STN	yellow-green	positive	reflective	no backlight
CFAH2004L-YYH-JT	STN	yellow-green	positive	transflective	yellow-green LED 

MECHANICAL SPECIFICATIONS

PHYSICAL CHARACTERISTICS

ITEM	SIZE
Number of Characters and Lines	20 Characters x 4 Lines
Module Dimensions	146.0 (W) x 62.5 (H) x 13.6 (D) mm
Viewing Area	123.5 (W) x 43.0 (H) mm
Active Area	118.84 (W) x 38.47 (H) mm
Character Size	4.84 (W) x 9.22 (H) mm
Character Pitch	6.0 (W) x 9.75 (H) mm
Dot Size	0.92 (W) x 1.1 (H) mm
Dot Pitch	0.98 (W) x 1.16 (H) mm
Weight	122 grams (typical)

MODULE OUTLINE DRAWING

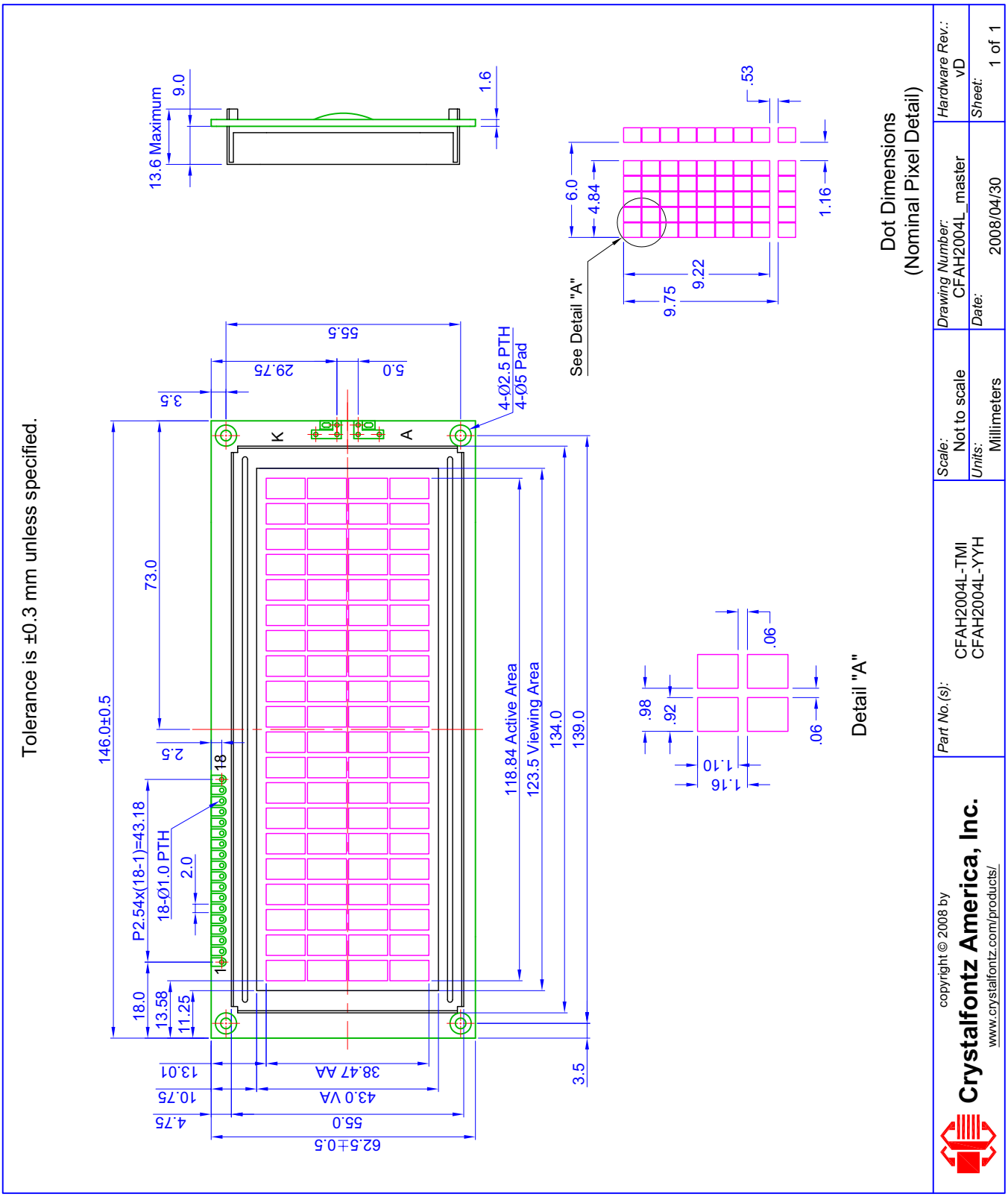


Figure 1. Module Outline Drawing

ELECTRICAL SPECIFICATIONS

SYSTEM BLOCK DIAGRAM

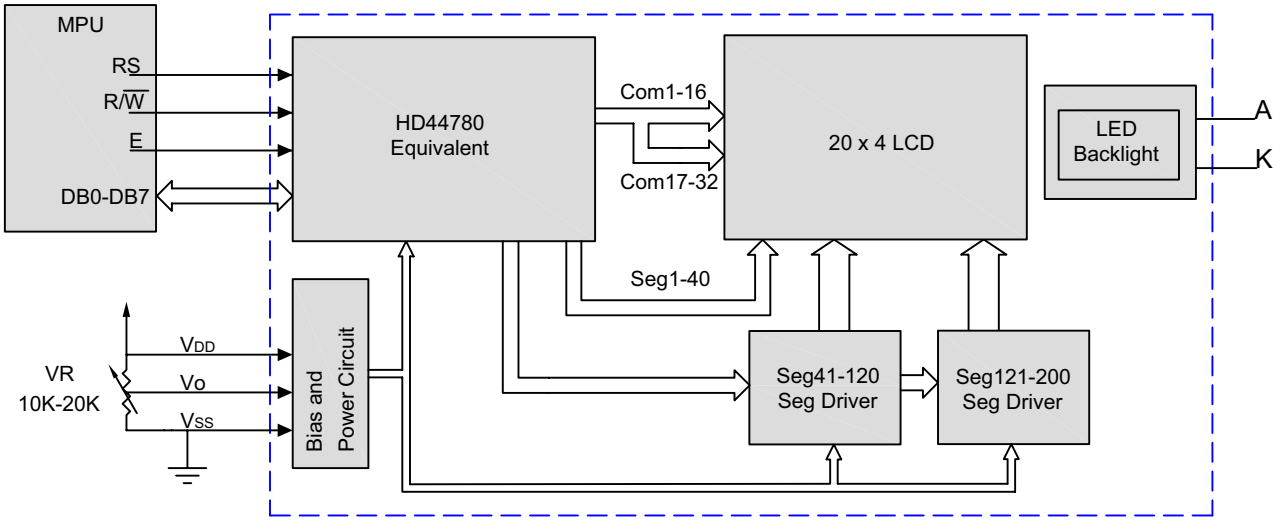


Figure 2. System Block Diagram

DRIVING METHOD

DRIVING METHOD	SPECIFICATION
Duty	1/16
Bias	1/5

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE MAXIMUM RATINGS	SYMBOL	MINIMUM	MAXIMUM
Operating Temperature*	T_{OP}	-20°C	+70°C
Storage Temperature*	T_{ST}	-30°C	+80°C
Input Voltage	V_I	V_{SS}	V_{DD}
Supply Voltage for Logic	V_{DD} - V_{SS}	-0.3v	+7v
Supply Voltage for LCD	V_{DD} - V_O	-0.3v	+13v
**Note: Prolonged exposure at temperatures outside of this range may cause permanent damage to the module.*			

DC CHARACTERISTICS (5V AND 3.3V OPERATION)

5V OPERATION							
PART	**DC CHARACTERISTICS** ***(4.5 to 5.5 volts)***	**TEST CONDITION**	**SYMBOL**	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**NOTES**
Controller and Board	Supply Voltage for Logic		V_{DD} - V_{SS}	+4.5v	+5.0v	+5.5v	
	Input High Voltage	V_{DD} = 5V	V_{IH}	+3.5v		V_{DD}	Pins: E, RS, R/$\overline{W}$, DB0 - DB7
	Input Low Voltage		V_{IL}			+0.6v	
	Output High Voltage	V_{DD} = 5V	V_{OH}	+3.7v			I_{OH} = - 0.1 mA Pins: DB0 - DB7
	Output Low Voltage		V_{OL}			+0.4v	I_{OL} = 0.1 mA Pins: DB0 - DB7
	Supply Current	without backlight	I_{DD}		1.2 mA		
LCD Glass	Supply Voltage for Driving LCD	TA = -20ºC	V_{DD} - V_O			+4.2v	
		TA = +25ºC			+3.8v		
		TA = +70ºC		+3.6v			

This is a summary of the module's major operating parameters. For detailed information, see APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET (Pg. 29).

3.3V OPERATION							
PART	**DC CHARACTERISTICS** ***(2.7 to 4.5 volts)***	**TEST CONDITION**	**SYMBOL**	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**NOTES**
Controller and Board	Supply Voltage for Logic		V_{DD} - V_{SS}	+2.7v	+3.3v	+4.5v	
	Input High Voltage	V_{DD} = 3.3V	V_{IH}	+2.3v		V_{DD}	Pins: E, RS, R/$\overline{W}$, DB0 - DB7
	Input Low Voltage		V_{IL}			+0.6v	
	Output High Voltage	V_{DD} = 3.3V	V_{OH}	+2.4v			I_{OH} = - 0.1 mA Pins: DB0 - DB7
	Output Low Voltage		V_{OL}			+0.4v	I_{OL} = 0.1 mA Pins: DB0 - DB7
	Supply Current	without backlight	I_{DD}		1.2 mA		
LCD Glass	Supply Voltage for Driving LCD	TA = -20ºC	V_{DD} - V_O			+4.2v	
		TA = +25ºC			+3.8v		
		TA = +70ºC		+3.6v			

This is a summary of the module's major operating parameters. For detailed information see *APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET (Pg. 29)*.

For more information about 3.3v operation, please see *APPENDIX B: APPLICATION NOTE FOR 3.3V OPERATION (Pg. 27)*.

DETAILS OF INTERFACE PIN FUNCTIONS

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
1	V_{SS}	0v		Ground
2	V_{DD}	+5.0v		Supply voltage for logic
3	V_O	variable		Supply voltage for driving LCD is V_O = +1v typical at V_{DD} = +5v which gives a V_{LCD} = (V_{DD} - V_O) = +4v
4	RS	H/L	I	Register selection input H: Data register (for read and write) L: Instruction code (for write)
5	R/$\overline{W}$	H/L	I	H: Read (Host←Module) L: Write (Host→Module)
6	E	H,H→L	I	Read/write enable signal H: Read data is enabled by a high level H→L: Write data is latched on the falling edge
7	DB0	H/L	I/O	Data bit 0
8	DB1	H/L	I/O	Data bit 1
9	DB2	H/L	I/O	Data bit 2
10	DB3	H/L	I/O	Data bit 3
11	DB4	H/L	I/O	Data bit 4
12	DB5	H/L	I/O	Data bit 5
13	DB6	H/L	I/O	Data bit 6
14	DB7	H/L	I/O	Data bit 7
15	A (LED +)			Supply voltage for LED. “A” (anode) or “+” of LED backlight
16	K (LED -)			Supply voltage for LED. “K” (cathode or kathode for German and original Greek spelling) or “-” of LED backlight
17	NC			No Connection
18	NC			No Connection
For backlight connections, please refer to LED Backlight Characteristics (Pg. 17).				

QUICK REFERENCE FOR PIN FUNCTIONS (FRONT & BACK PHOTOS)

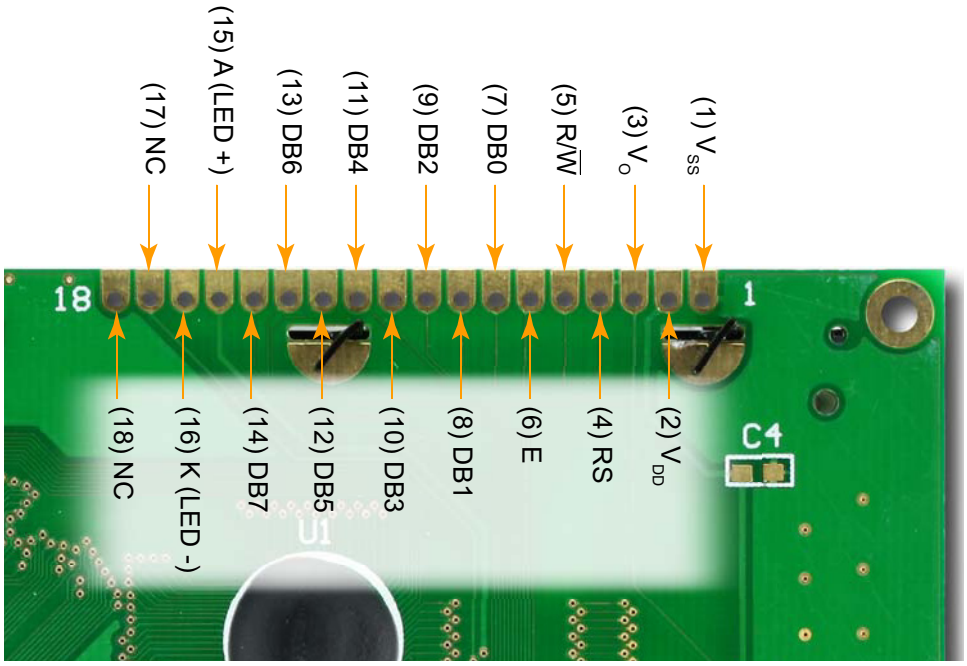


Figure 3. Back View of Pins (Labeled)

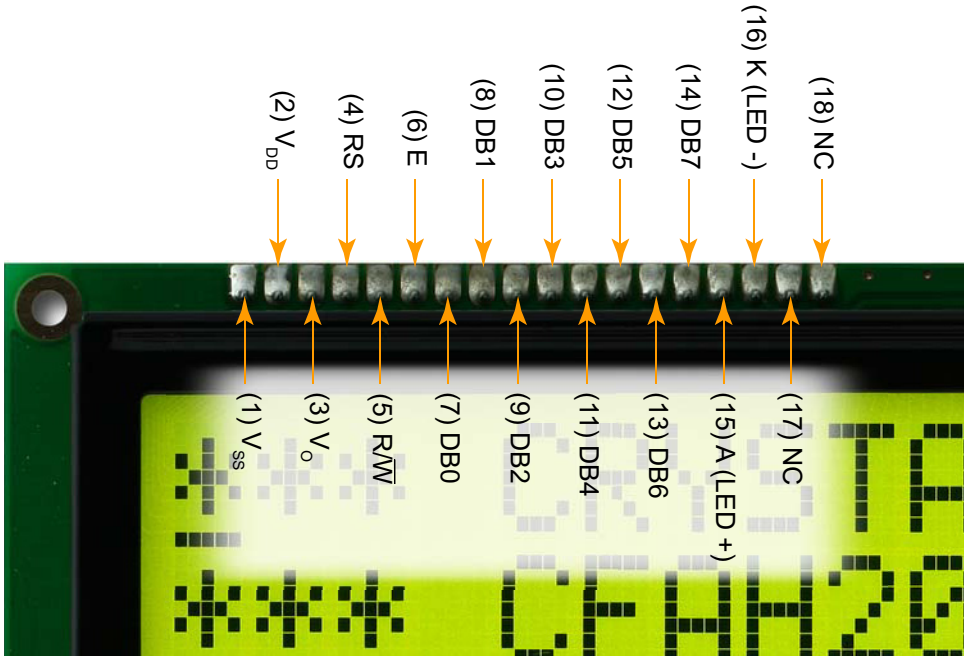


Figure 4. Front View of Pins (Labeled)

TYPICAL V_O CONNECTIONS FOR DISPLAY CONTRAST

Adjust V_O to +1v (V_{LCD} = +4v) as an initial setting. When the module is operational, readjust V_O for optimal display appearance.

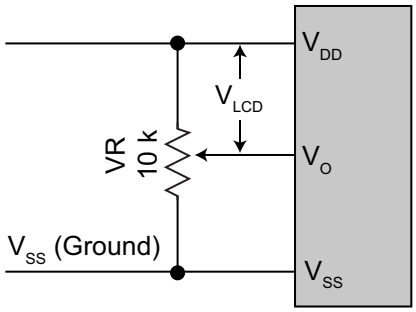


Figure 5. Typical V_O Connections

We recommend allowing field adjustment of V_O for all designs. The optimal value for V_O will change with temperature, variations in V_{DD}, and viewing angle. V_O will also vary module-to-module and batch-to-batch due to normal manufacturing variations.

Ideally, adjustments to V_O should be available to the end user so each user can adjust the display to the optimal contrast for their required viewing conditions. At a minimum, your design should allow V_O to be adjusted as part of your product's final test.

Although a potentiometer is shown as a typical connection, V_O can be driven by your microcontroller, either by using a DAC or a filtered PWM. Displays that require V_O to be negative may need a level-shifting circuit. Please do not hesitate to contact Crystalfontz application support for design assistance on your application.

ESD (ELECTRO-STATIC DISCHARGE) SPECIFICATIONS

This circuitry is industry standard CMOS logic and is susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. For more information, see CARE AND HANDLING PRECAUTIONS (Pg. 22).

OPTICAL SPECIFICATIONS

OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MINIMUM	TYPICAL	MAXIMUM
Viewing Angle (6 o'clock) (Vertical, Horizontal)	(V)θ	CR≥2	20°		40°
	(H)φ	CR≥2	-30°		30°
Contrast Ratio	CR			3	
LCD Response Time*	T rise	Ta = 25°C		150 ms	200 ms
	T fall	Ta = 25°C		150 ms	200 ms
**Response Time: The amount of time it takes a liquid crystal cell to go from active to inactive or back again.*					

OPTICAL DEFINITIONS

- Operating Voltage (V_{LCD}): V_{OP}
- Viewing Angle
  - Vertical (V)θ: 0°
  - Horizontal (H)φ: 0°
- Frame Frequency: 64 Hz
- Driving Waveform: 1/16 Duty, 1/5 Bias
- Ambient Temperature (Ta): 25°C

Definition of Operation Voltage (Vop)

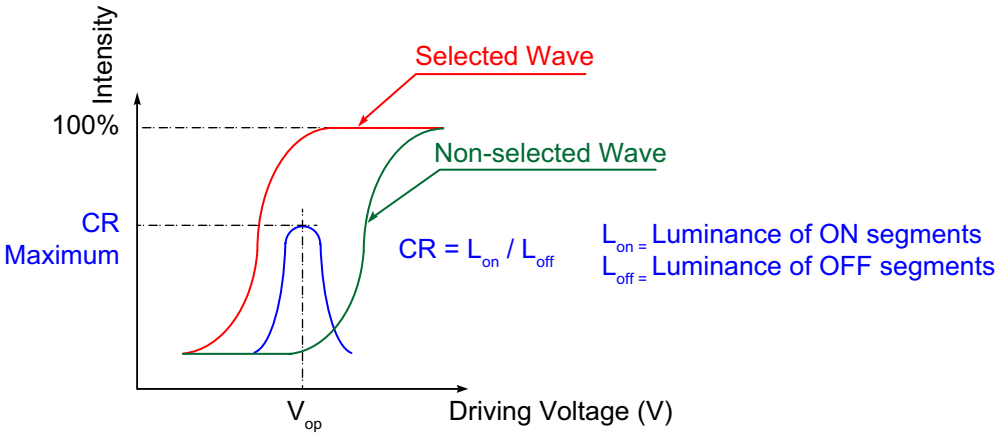


Figure 6. Definition of Operation Voltage (V_{OP}) (Negative)

Definition of Response Time (Tr, Tf)

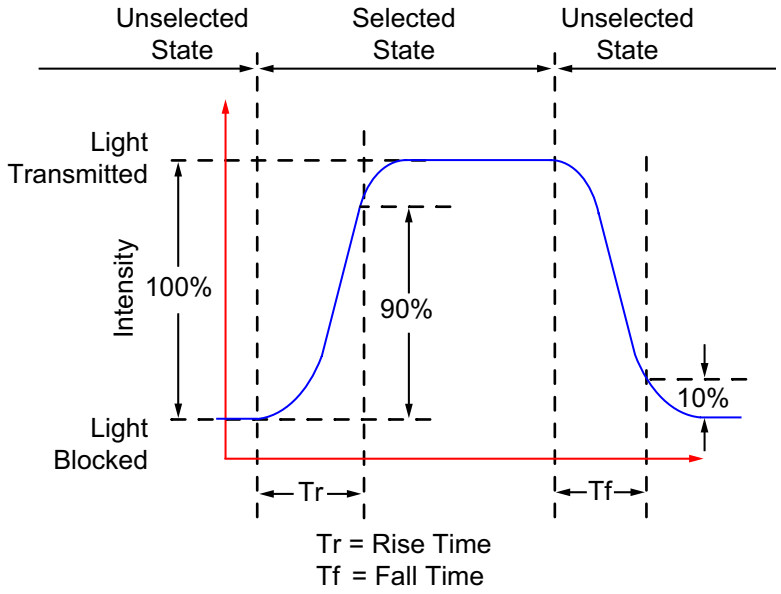


Figure 7. Definition of Response Time (Tr, Tf) (Negative)

Definition of Vertical and Horizontal Viewing Angles (CR≥2)

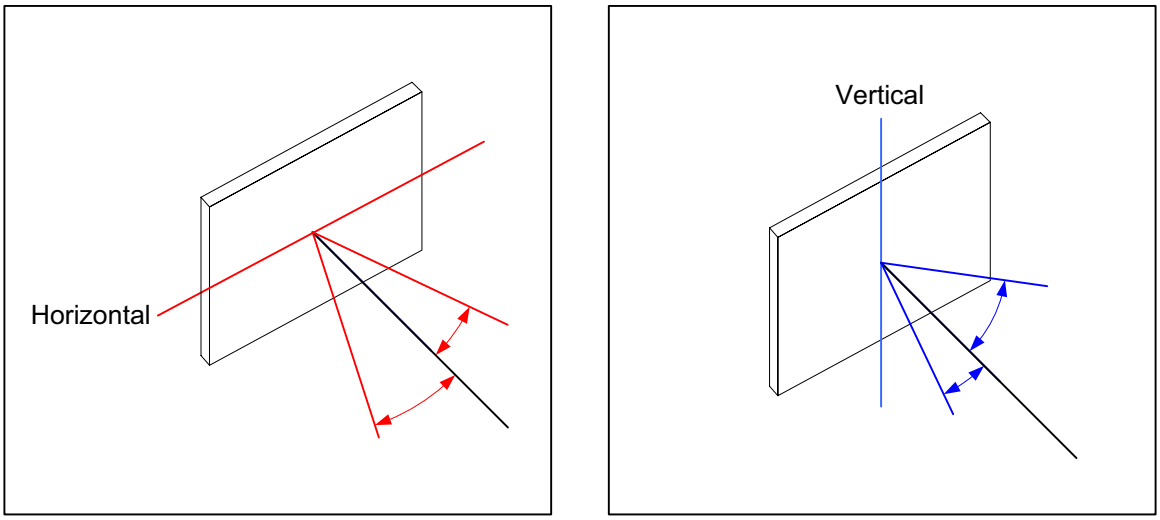


Figure 8. Definition of Horizontal and Vertical Viewing Angles (CR>2)

Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles

This module has a 6:00 o'clock viewing angle. A 6:00 o'clock viewing angle is a bottom viewing angle like what you would see when you look at a cell phone or calculator. A 12:00 o'clock viewing angle is a top viewing angle like what you would see when you look at the gauges in a golf cart or airplane.

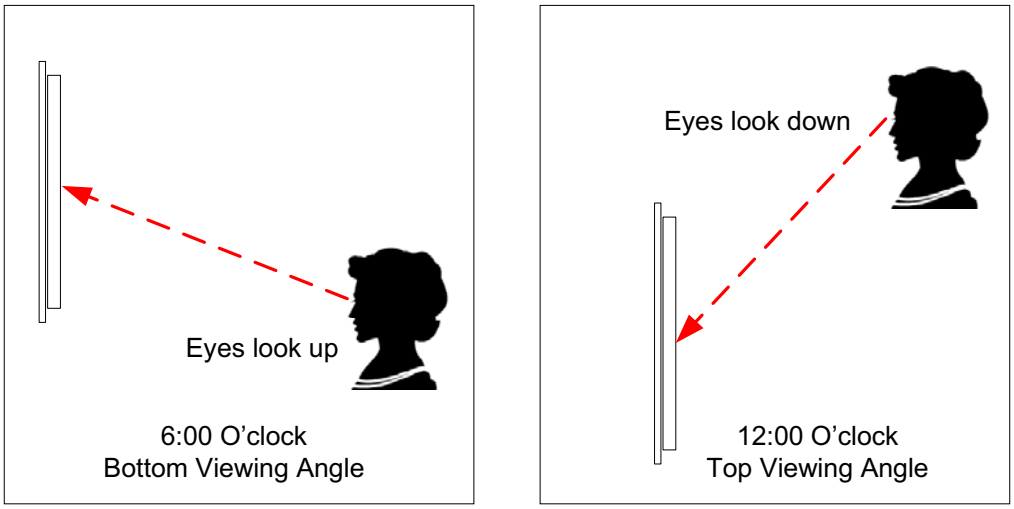


Figure 9. Definition of 6:00 O'Clock and 12:00 O'Clock Viewing Angles

LED BACKLIGHT CHARACTERISTICS

The CFAH2004L-TMI-JT uses an LED backlight. LED backlights are easy to use, but they are also easily damaged by abuse.

> **NOTE**
> Do not connect +5v directly to the backlight terminals. This will ruin the backlight.

LEDs are “current” devices. The important aspect of driving an LED is the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor in line from a voltage source will work well in most applications and is much less complex than a current source.

You need to know what the forward voltage of the LEDs is so you can calculate the current limiting resistor (R_{LIMIT}). The forward voltage will vary slightly from display to display.

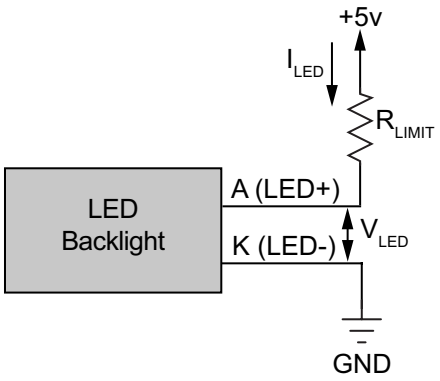


Figure 10. Typical LED Backlight Connections for “Always On”

The equation to calculate R_{LIMIT} is:

$$R_{LIMIT}\ (\text{minimum}) = \frac{V_{DD}\ (\text{Supply Voltage}) - V_{LED}\ (\text{Typical LED Forward Voltage})}{I_{LED}\ (\text{Typical LED Forward Current})}$$

The specific R_{LIMIT} calculation for the CFAH2004L-TMI-JT at V_{DD} = +5v is:

$$R_{LIMIT} = \frac{5v - 3.5v}{0.08\ A} = 18.75\Omega\ (\text{minimum})$$

The backlight may be dimmed by PWM (Pulse Width Modulation). The typical range for the PWM frequency is from 100 to 300 Hz.

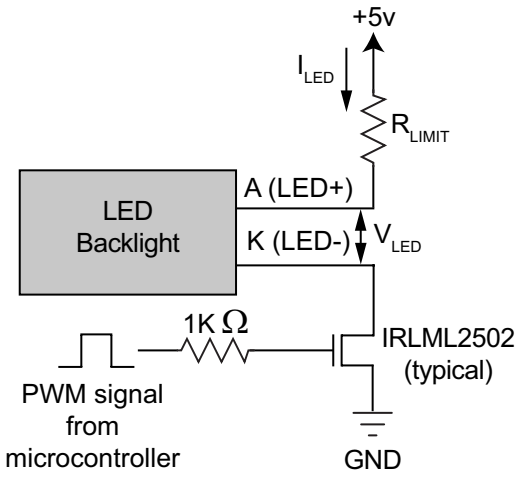


Figure 11. Example of LED Backlight Connections for PWM Dimming

Backlight Characteristics ***light dots on blue background***			
PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**
Forward Current (I_{LED}) V = 3.5v	72 mA	80 mA	125 mA
Forward Voltage (V_{LED})	+3.4v	+3.5v	+3.6v
Reverse Voltage (V_R)			+5v
Luminous Intensity* (I_V) I_{LED} = 80 mA	232 cd/m^2	290 cd/m^2	
**Direct measurement of backlight–the backlight is not measured through the LCD.*			

LCD CONTROLLER INTERFACE

This module uses a Sitronix ST7066U controller. The Sitronix ST7066U is compatible with the industry standard Hitachi HD44780 controller. Software written for modules that use the HD44780 should work without modification.

For your reference, we added APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET (Pg. 29) to this Data Sheet.

DISPLAY POSITION DDRAM ADDRESS

The following table shows the relationship between the controller's addresses and the corresponding character location on the module.

		COLUMN																			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ROW	0	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0xA	0xB	0xC	0xD	0xE	0xF	0x10	0x11	0x12	0x13
	1	0x40	0x41	0x42	0x43	0x44	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C	0x4D	0x4E	0x4F	0x50	0x51	0x52	0x53
	2	0x14	0x15	0x16	0x17	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
	3	0x54	0x55	0x56	0x57	0x58	0x59	0x5A	0x5B	0x5C	0x5D	0x5E	0x5F	0x60	0x61	0x62	0x63	0x64	0x65	0x66	0x67

CHARACTER GENERATOR ROM (CGROM)

To find the code for a given character, add the two numbers that are shown in bold for its row and column. For example, the lowercase “h” is in the column labeled “96_{10}” and in the row labeled “8_{10}”. So you would add 96 + 8 to get 104. When you send a byte with the value of 104 to the display, then a lowercase “h” will be shown. (See APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET (Pg. 29).

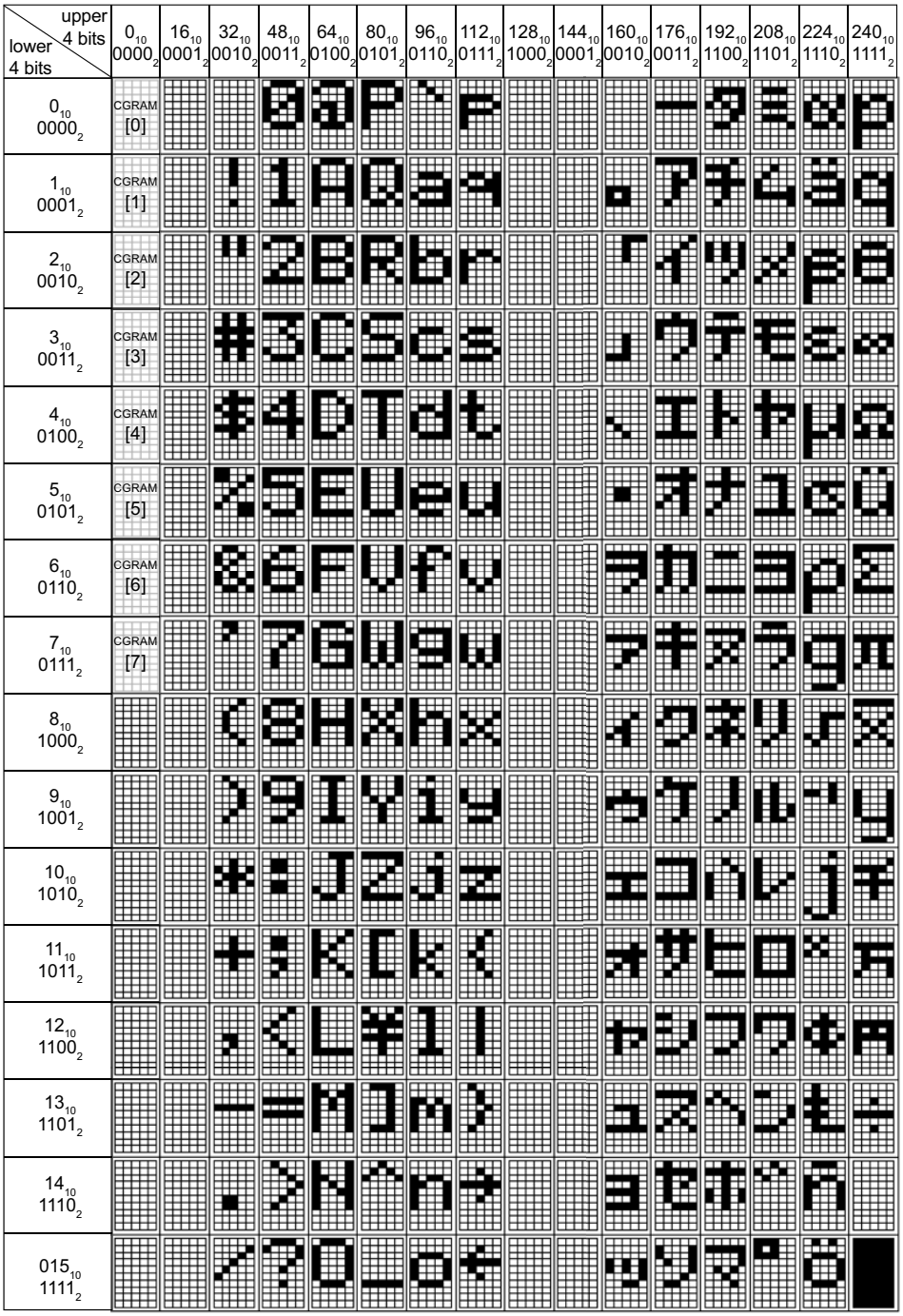


Figure 12. Character Generator ROM (CGROM)

MODULE RELIABILITY AND LONGEVITY

MODULE RELIABILITY

ITEM	SPECIFICATION	
LCD excluding backlight	50,000 to 100,000 hours (typical)	
White LED Backlight (I_{LED} < 80 mA)* * *We recommend that the backlight of the white LED backlit modules be dimmed or turned off during periods of inactivity to conserve the white LED backlight life-time.*	*Power-On Hours*	*% of Initial Brightness (New Module)*
	<7,500	>90%
	<35,000	>50%

We list the lifetime of this white LED at 7,500 hours to emphasize that white LEDs do not have the extremely long lifetime typical of red or green LEDs. The white LEDs dim over time, especially if driven with high currents. The dimming may not be noticeable when a single display is installed. However, if a new display is installed next to a display that has been on continuously for a very long time, you will see the difference. To preserve the lifetime of white LEDs, we recommend that white LED backlights are dimmed or turned off when not needed. Also, please do not use more current than you need to achieve your brightness requirements.

MODULE LONGEVITY (EOL / REPLACEMENT POLICY)

Crystalfontz is committed to making all of our LCD modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life", EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module it replaces. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *LCD fluid, polarizers, or the LCD manufacturing process.* These items may change the appearance of the display, requiring an adjustment to V_O (See Typical V_O Connections for Display Contrast (Pg. 13)).
- *Backlight LEDs.* Brightness may be affected (perhaps the new LEDs have better efficiency) or the current they draw may change (new LEDs may have a different VF).
- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.

Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's webpage as soon as possible. If interested, you can subscribe to future part change notifications.

CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions below.

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other PCB such as expansion cards or motherboards. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING

- The exposed surface of the LCD “glass” is actually a polarizer laminated on top of the glass.To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- To protect the soft plastic polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the module, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not modify the tab of the metal holder or make connections to it.
- Solder only to the I/O terminals. Use care when removing solder—it is possible to damage the PCB.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.

AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the module to strong mechanical shock, impact, torque, and tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

IF LCD PANEL BREAKS

- If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or eyes.
- If the liquid crystal fluid touches your skin, clothes, or work surface, wash it off immediately using soap and plenty of water.
- Do not eat the LCD panel.

CLEANING

The polarizer (laminated to the glass) is soft plastic. The soft plastic is easily scratched or damaged. Be very careful when you clean the polarizer.

- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips).
- Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand “Crystal Clear Tape”). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.

OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product.” This module is not "user friendly" and connecting them to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
  - At lower temperatures of this range, response time is delayed.
  - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

STORAGE AND RECYCLING

- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated Crystalfontz LCD modules at an approved facility.

APPENDIX A: QUALITY ASSURANCE STANDARDS

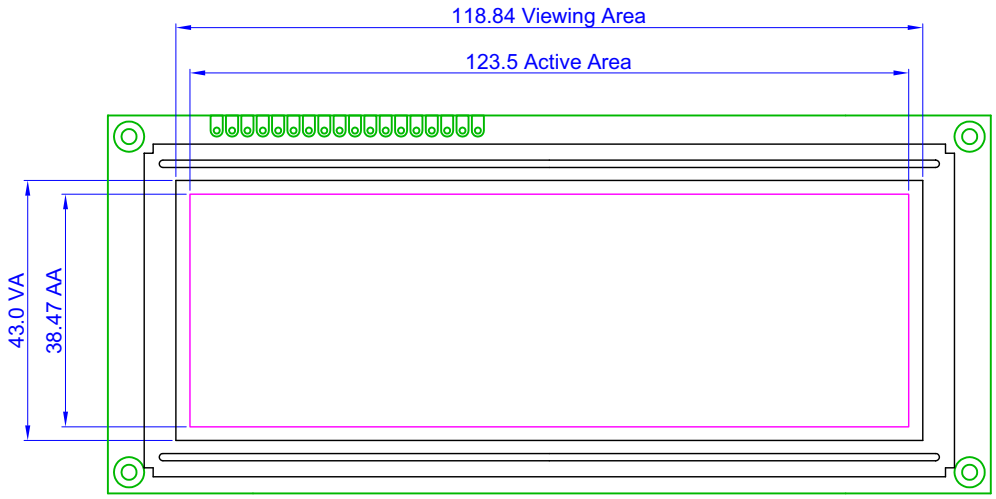
INSPECTION CONDITIONS

- Environment
  - Temperature: 25±5°C
  - Humidity: 30~85% RH (noncondensing)
- For visual inspection of active display area
  - Source lighting: two 20-Watt or one 40-Watt fluorescent light
  - Display adjusted for best contrast
  - Viewing distance: 30±5 cm (about 12 inches)
  - Viewing angle: inspect at 45° angle of vertical line right and left, top and bottom

COLOR DEFINITIONS

We try to describe the appearance of our LCD modules as accurately as possible. For the photos, we adjust the backlight (if any) and contrast for optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.

DEFINITION OF ACTIVE AREA AND VIEWING AREA



ACCEPTANCE SAMPLING

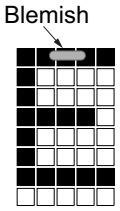
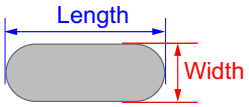
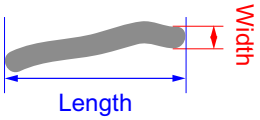
DEFECT TYPE	AQL*
Major	≤.65%
Minor	<1.0%
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

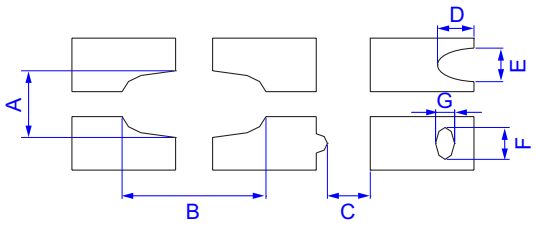
DEFECTS CLASSIFICATION

Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

ACCEPTANCE STANDARDS

#	DEFECT TYPE	CRITERIA			MAJOR / MINOR
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major
2	Viewing area defect	Viewing area does not meet specifications.			Major
3	Contrast adjustment defect	Contrast adjustment fails or malfunctions.			Major
4	Blemishes or foreign matter on display segments		*Defect Size*	*Acceptable Qty*	Minor
			≤0.30 mm	3	
			≤2 defects within 10 mm of each other		
5	Blemishes or foreign matter outside of display segments	Defect Size = (Width + Length)/2 	*Defect Size*	*Acceptable Qty*	Minor
			≤0.15 mm	Ignore	
			0.15 to 0.20 mm	3	
			0.20 to 0.25 mm	2	
			> 0.30 mm	1	
6	Dark lines or scratches in display area 	*Defect Width*	*Defect Length*	*Acceptable Qty*	Minor
		≤0.03 mm	≤3.0 mm	3	
		0.03 to 0.05	≤2.0 mm	2	
		0.05 to 0.08	≤2.0 mm	1	
		0.08 to 0.10	≤3.0 mm	0	
		≥0.10	>3.0 mm	0	

<table>
<tr><th>#</th><th>DEFECT TYPE</th><th colspan="3">CRITERIA</th><th>MAJOR / MINOR</th></tr>
<tr><td rowspan="5">7</td><td rowspan="5">Bubbles between polarizer film and glass</td><td colspan="2">Defect Size</td><td>Acceptable Qty</td><td rowspan="5">Minor</td></tr>
<tr><td colspan="2">≤0.20 mm</td><td>Ignore</td></tr>
<tr><td colspan="2">0.20 to 0.40 mm</td><td>3</td></tr>
<tr><td colspan="2">0.40 to 0.60 mm</td><td>2</td></tr>
<tr><td colspan="2">≥0.60 mm</td><td>0</td></tr>
<tr><td rowspan="6">8</td><td rowspan="6">Display pattern defect</td><td colspan="3"> 
</td><td rowspan="6">Minor</td></tr>
<tr><td>Dot Size</td><td colspan="2">Acceptable Qty</td></tr>
<tr><td>((A+B)/2)≤0.20 mm</td><td colspan="2" rowspan="4">≤3 total defects
≤2 pinholes per digit</td></tr>
<tr><td>C>0 mm</td></tr>
<tr><td>((D+E)/2)≤0.25 mm</td></tr>
<tr><td>((F+G)/2)≤0.25 mm</td></tr>
<tr><td>9</td><td>Backlight defects</td><td colspan="3">1. Light fails or flickers. (Major)
2. Color and luminance do not correspond to specifications. (Major)
3. Exceeds standards for display's blemishes, foreign matter, dark lines or scratches. (Minor)</td><td>See list ←</td></tr>
<tr><td>10</td><td>PCB defects</td><td colspan="3">1. Oxidation or contamination on connectors.*
2. Wrong parts, missing parts, or parts not in specification.*
3. Jumpers set incorrectly. (Minor)
4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth. (Minor)
*Minor if display functions correctly. Major if the display fails.</td><td>See list ←</td></tr>
<tr><td>11</td><td>Soldering defects</td><td colspan="3">1. Unmelted solder paste.
2. Cold solder joints, missing solder connections, or oxidation.*
3. Solder bridges causing short circuits.*
4. Residue or solder balls.
5. Solder flux is black or brown.
*Minor if display functions correctly. Major if the display fails.</td><td>Minor</td></tr>
</table>

APPENDIX B: APPLICATION NOTE FOR 3.3V OPERATION

This module can be used with a 3.3v power supply. In order to meet the requirements of V_{LCD}, you must provide a negative voltage source for V_O (pin 3, see Details of Interface Pin Functions (Pg. 11)). You need to drive V_O to below ground (typically -1v or -2v) until the V_{LCD} is met, making display contrast acceptable.

You can supply the negative voltage by one of the following methods:

1. Use an available source for the negative voltage.

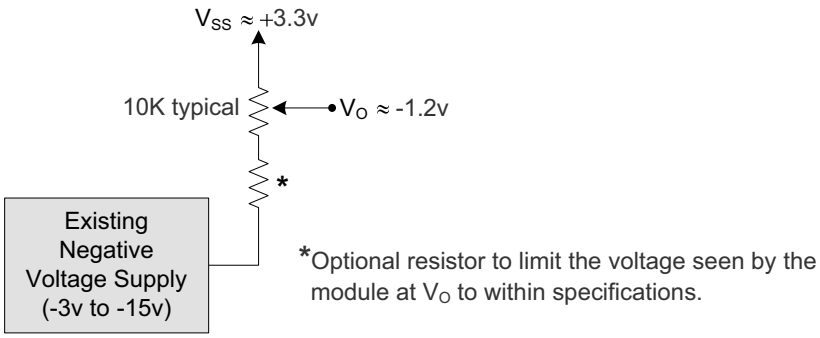


Figure 1. Use Existing Negative Voltage Supply

2. Use a “7660” CMOS switched-capacitor voltage converter or one of the many other available solutions for creating a negative voltage from a positive supply.

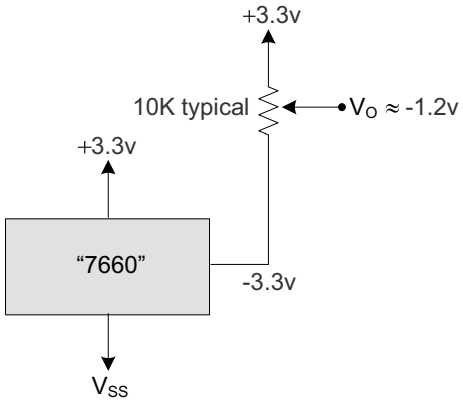


Figure 2. “7660” Switched-Capacitor Voltage Converter

3. Use the circuit in the figure below to create the voltage for V_O by using a PWM (Pulse Width Modulation) output of your microcontroller. This circuit allows the contrast to be adjusted under software control.

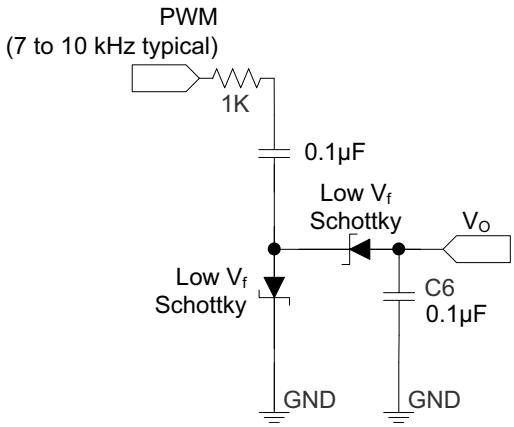


Figure 3. V_O Driving Circuit

Since V_O is pulled up internally by the LCD controller, this circuit will produce positive (≈+1v) V_{LCD} (V_{LCD} = small, contrast is light) for low (≈10%) or high (90%) duty cycles. For duty cycles near 50%, this circuit will produce negative (≈-2v) levels of V_O (V_{LCD} = big, contrast is dark).

4. Replace this module with the module in this series that has an on-board negative voltage generator. (The part number has a "V" at the end of it.)

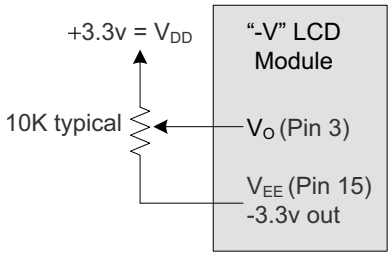


Figure 4. On-Board Negative Voltage Generator

APPENDIX C: SITRONIX ST7066U CONTROLLER SPECIFICATION SHEET

The complete *Sitronix ST7066U Dot Matrix LCD Controller/Driver* specifications (42 pages) follows.

Sitronix

ST7066U

Dot Matrix LCD Controller/Driver

■ Features

- **5 x 8 and 5 x 11 dot matrix possible**
- **Low power operation support:**
  -- 2.7 to 5.5V
- **Wide range of LCD driver power**
  -- 3.0 to 10V
- **Correspond to high speed MPU bus interface**
  -- 2 MHz (when V_{CC} = 5V)
- **4-bit or 8-bit MPU interface enabled**
- **80 x 8-bit display RAM (80 characters max.)**
- **13,200-bit character generator ROM for a total of 240 character fonts(5 x 8 dot or 5 x 11 dot)**
- **64 x 8-bit character generator RAM**
  -- 8 character fonts (5 x 8 dot)
  -- 4 character fonts (5 x 11 dot)
- **16-common x 40-segment liquid crystal display driver**
- **Programmable duty cycles**
  -- 1/8 for one line of 5 x 8 dots with cursor
  -- 1/11 for one line of 5 x 11 dots & cursor
  -- 1/16 for two lines of 5 x 8 dots & cursor
- **Wide range of instruction functions:**
  Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- **Automatic reset circuit that initializes the controller/driver after power on**
- **Internal oscillator with external resistors**
- **Low power consumption**
- **QFP80 and Bare Chip available**

■ Description

The ST7066U dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

The ST7066U character generator ROM is extended to generate 240 5x8(5x11) dot character fonts for a total of 240 different character fonts. The low power supply (2.7V to 5.5V) of the ST7066U is suitable for any portable battery-driven product requiring low power dissipation.

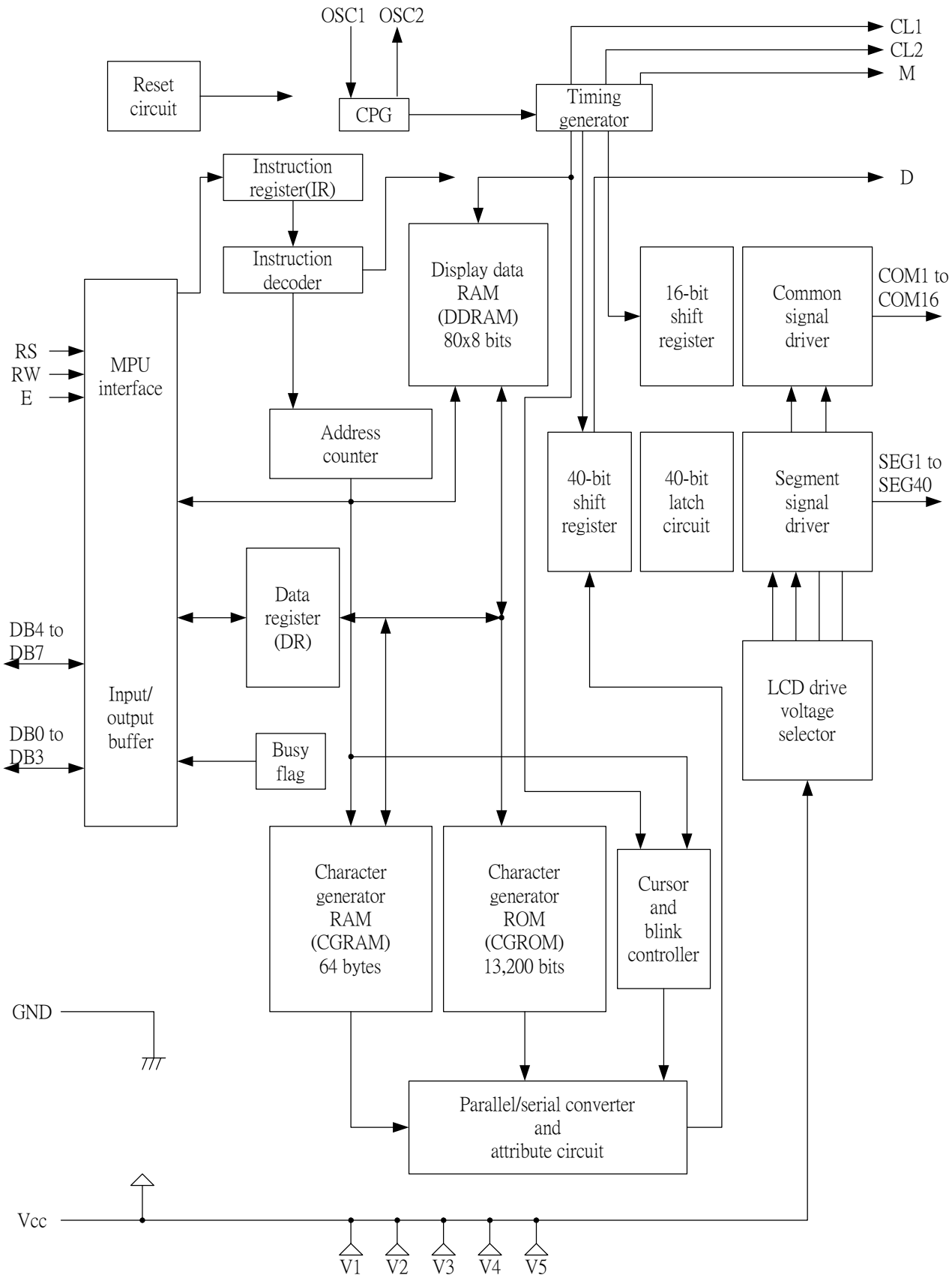
The ST7066U LCD driver consists of 16 common signal drivers and 40 segment signal drivers which can extend display size by cascading segment driver ST7065 or ST7063. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single ST7066U can display up to one 8-character line or two 8-character lines.

Product Name	Support Character
ST7066U-0A	English / Japan
ST7066U-0B	English / European
ST7066U-0E	English / European

Appendix

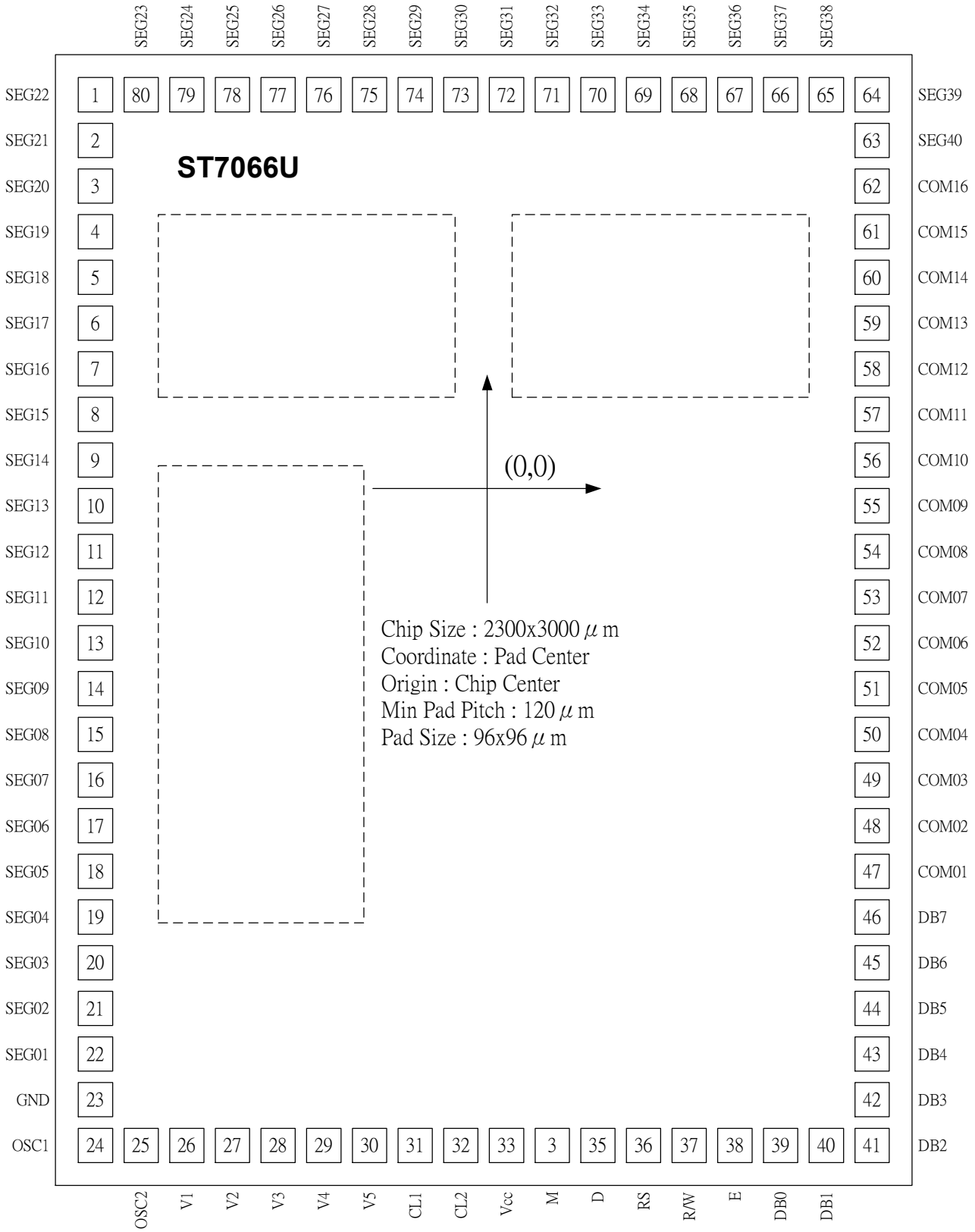
ST7066 Serial Specification Revision History		
Version	**Date**	**Description**
1.7	2000/10/31	1. Added 8051 Example Program Code(Page 21,23) 2. Added Annotated Flow Chart : "BF cannot be checked before this instruction" 3. Changed Maximum Ratings Power Supply Voltage:+5.5V →+7.0V(Page 28)
1.8	2000/11/14	Added QFP Pad Configuration(Page 5)
1.8a	2000/11/30	1. Moved QFP Package Dimensions(Page 39) to Page 5 2. Changed DC Characteristics Ratings(Page 32,33)
2.0	2001/03/01	Transition to ST7066U
2.1	2006/04/10	1. Add Power Supply Conditions (Page 31); 2. Modify reset description on Page 22.
2.2	2006/05/11	Emphasis checking BF procedure (Page 9, 27, 28).

■ Block Diagram



Appendix

■ Pad Arrangement

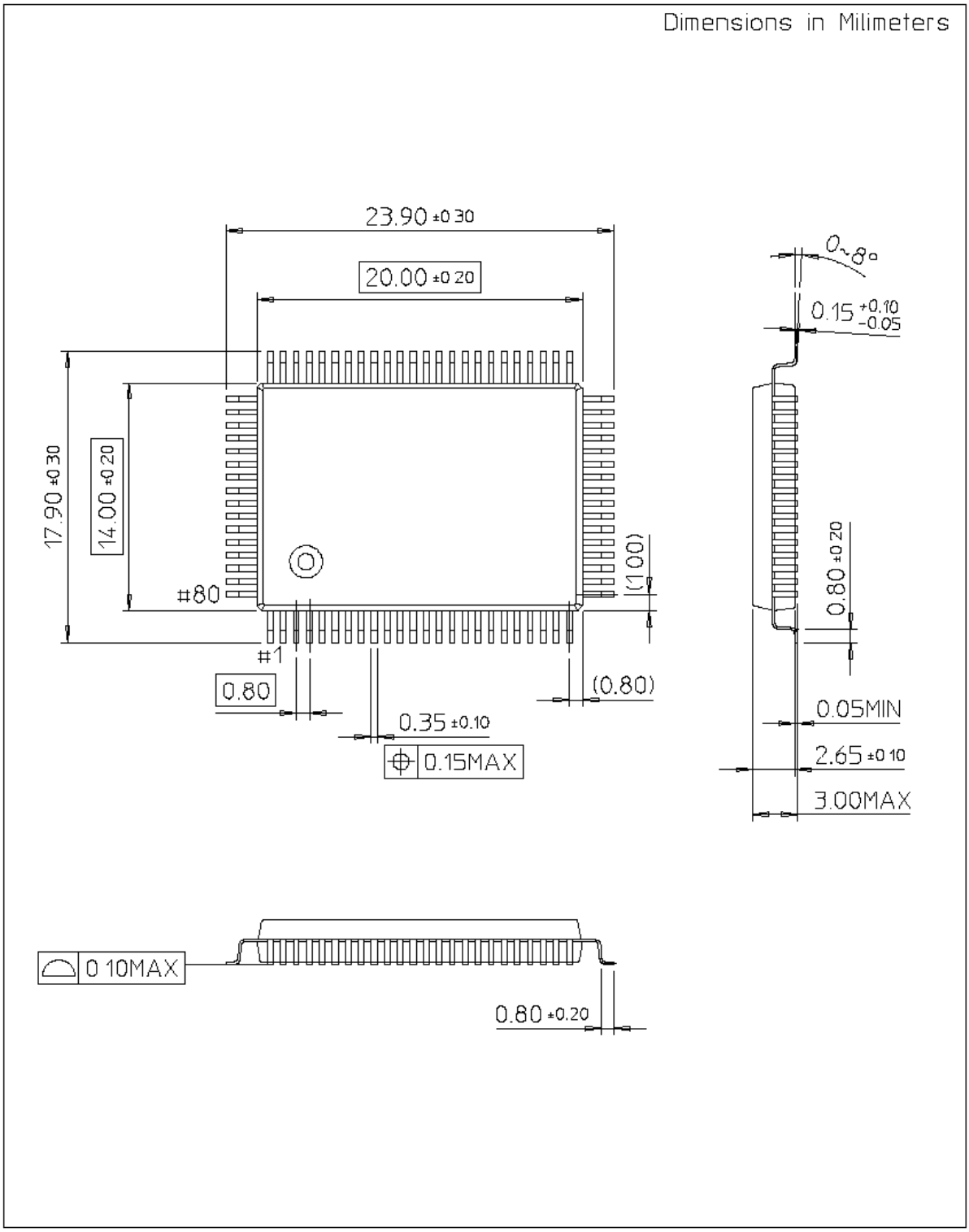


Substrate Connect to VDD.

Appendix

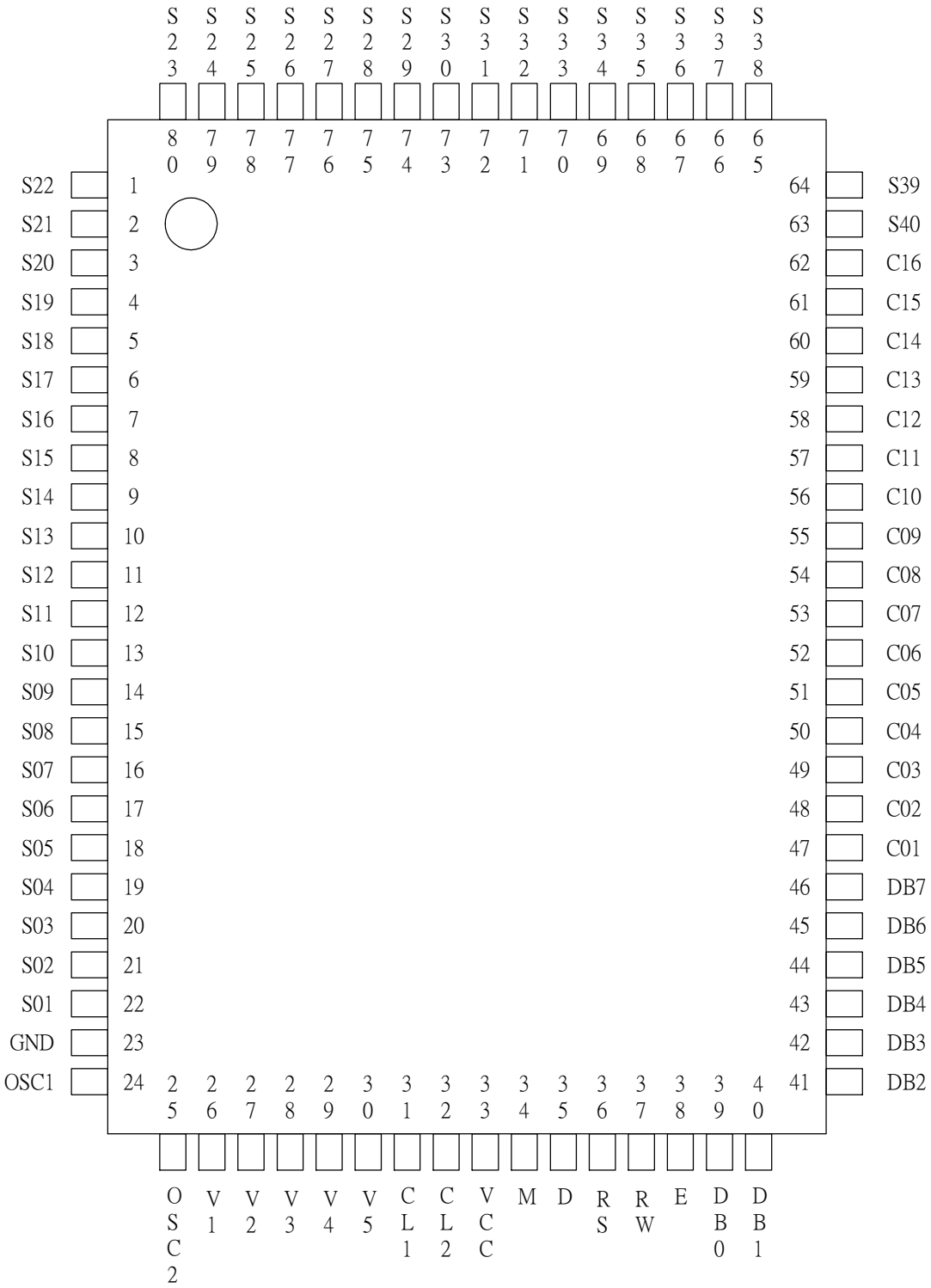
■ Package Dimensions

80-QFP-1420C



Appendix

■ Pad Configuration(80 QFP)



Appendix

■ Pad Location Coordinates

Pad No.	Function	X	Y
1	SEG22	-1040	1400
2	SEG21	-1040	1270
3	SEG20	-1040	1140
4	SEG19	-1040	1020
5	SEG18	-1040	900
6	SEG17	-1040	780
7	SEG16	-1040	660
8	SEG15	-1040	540
9	SEG14	-1040	420
10	SEG13	-1040	300
11	SEG12	-1040	180
12	SEG11	-1040	60
13	SEG10	-1040	-60
14	SEG9	-1040	-180
15	SEG8	-1040	-300
16	SEG7	-1040	-420
17	SEG6	-1040	-540
18	SEG5	-1040	-660
19	SEG4	-1040	-780
20	SEG3	-1040	-900
21	SEG2	-1040	-1020
22	SEG1	-1040	-1140
23	GND	-1040	-1270
24	OSC1	-1040	-1400
25	OSC2	-910	-1400
26	V1	-780	-1400
27	V2	-660	-1400
28	V3	-540	-1400
29	V4	-420	-1400
30	V5	-300	-1400
31	CL1	-180	-1400
32	CL2	-60	-1400
33	Vcc	60	-1400
34	M	180	-1400
35	D	300	-1400
36	RS	420	-1400
37	RW	540	-1400
38	E	660	-1400
39	DB0	780	-1400
40	DB1	910	-1400

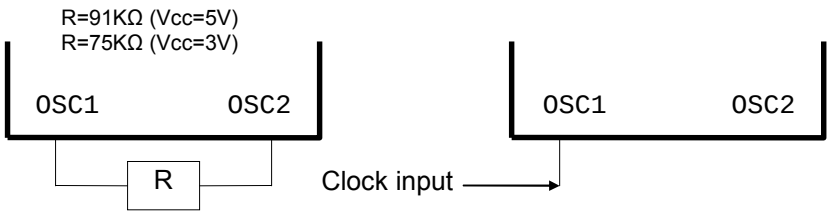
Pad No.	Function	X	Y
41	DB2	1040	-1400
42	DB3	1040	-1270
43	DB4	1040	-1140
44	DB5	1040	-1020
45	DB6	1040	-900
46	DB7	1040	-780
47	COM1	1040	-660
48	COM2	1040	-540
49	COM3	1040	-420
50	COM4	1040	-300
51	COM5	1040	-180
52	COM6	1040	-60
53	COM7	1040	60
54	COM8	1040	180
55	COM9	1040	300
56	COM10	1040	420
57	COM11	1040	540
58	COM12	1040	660
59	COM13	1040	780
60	COM14	1040	900
61	COM15	1040	1020
62	COM16	1040	1140
63	SEG40	1040	1270
64	SEG39	1040	1400
65	SEG38	910	1400
66	SEG37	780	1400
67	SEG36	660	1400
68	SEG35	540	1400
69	SEG34	420	1400
70	SEG33	300	1400
71	SEG32	180	1400
72	SEG31	60	1400
73	SEG30	-60	1400
74	SEG29	-180	1400
75	SEG28	-300	1400
76	SEG27	-420	1400
77	SEG26	-540	1400
78	SEG25	-660	1400
79	SEG24	-780	1400
80	SEG23	-910	1400

Appendix

■ Pin Function

Name	Number	I/O	Interfaced with	Function
RS	1	I	MPU	Select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read)
R/W	1	I	MPU	Select read or write. 0: Write 1: Read
E	1	I	MPU	Starts data read/write.
DB4 to DB7	4	I/O	MPU	Four high order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. DB7 can be used as a busy flag.
DB0 to DB3	4	I/O	MPU	Four low order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. These pins are not used during 4-bit operation.
CL1	1	O	Extension driver	Clock to latch serial data D sent to the extension driver
CL2	1	O	Extension driver	Clock to shift serial data D
M	1	O	Extension driver	Switch signal for converting the liquid crystal drive waveform to AC
D	1	O	Extension driver	Character pattern data corresponding to each segment signal
COM1 to COM16	16	O	LCD	Common signals that are not used are changed to non-selection waveform. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor.
SEG1 to SEG40	40	O	LCD	Segment signals
V1 to V5	5	-	Power supply	Power supply for LCD drive V_{cc} - V5 = 10 V (Max)
V_{cc}, GND	2	-	Power supply	V_{cc}: 2.7V to 5.5V, GND: 0V
OSC1, OSC2	2		Oscillation resistor clock	When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1.

Note:
1. Vcc>=V1>=V2>=V3>=V4>=V5 must be maintained
2. Two clock options:



Appendix

■ Function Description

- **System Interface**

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag(DB7) and address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

Table 1. Various kinds of operations according to RS and R/W bits.

- **Busy Flag (BF)**

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High. **Before checking BF, be sure to wait at least 80us. Please refer to Page 27 for the example. Do NOT keep "E" always "High" for checking BF.**

- **Address Counter (AC)**

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

- **Display Data RAM (DDRAM)**

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

➢ **1-line display (N = 0) (Figure 2)**

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the ST7066U, 8 characters are displayed. See Figure 3.
When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

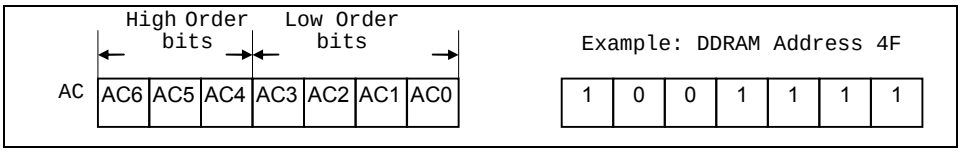


Figure 1 DDRAM Address

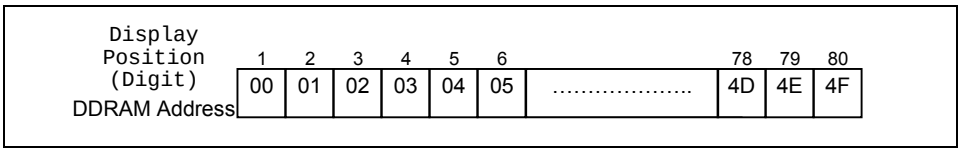


Figure 2 1-Line Display

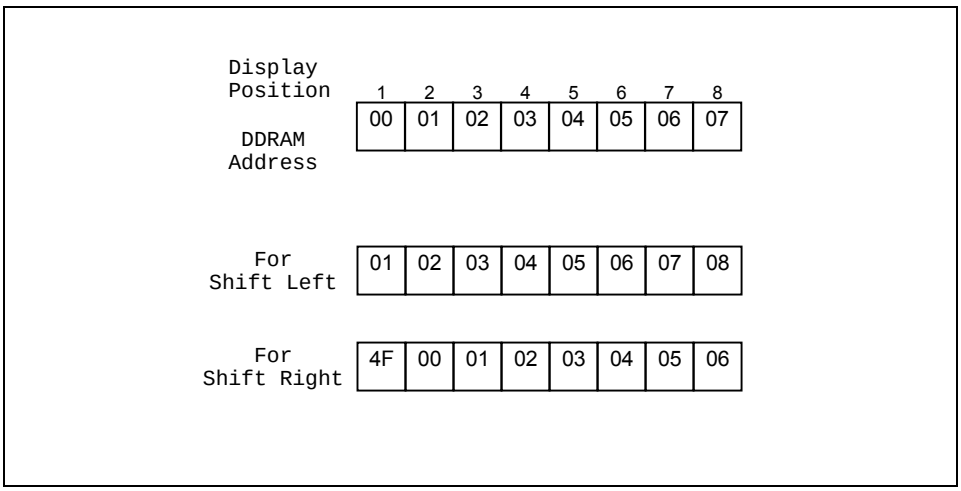


Figure 3 1-Line by 8-Character Display Example

➢ **2-line display (N = 1) (Figure 4)**

Case 1: When the number of display characters is less than 40 × 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the ST7066U is used, 8 characters × 2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

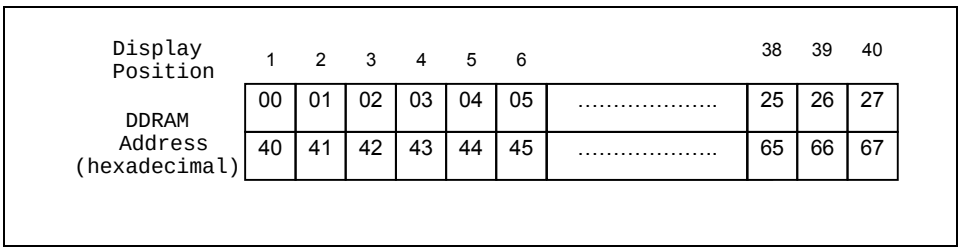


Figure 4 2-Line Display

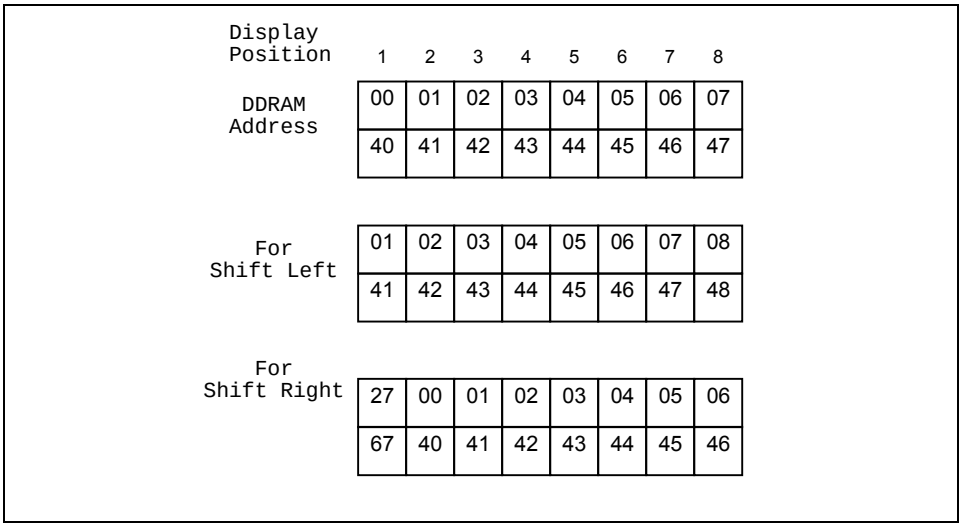


Figure 5 2-Line by 8-Character Display Example

Case 2: For a 16-character × 2-line display, the ST7066U can be extended using one 40-output extension driver. See Figure 6.
When display shift operation is performed, the DDRAM address shifts. See Figure 6.

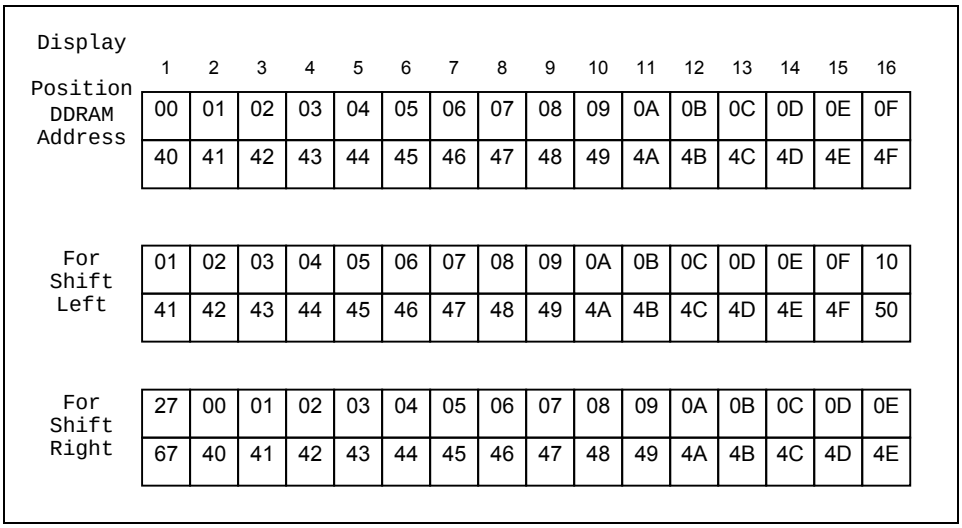


Figure 6 2-Line by 16-Character Display Example

Appendix

- **Character Generator ROM (CGROM)**

The character generator ROM generates 5 x 8 dot or 5 x 11 dot character patterns from 8-bit character codes. It can generate 240 5 x 8 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

- **Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written, and for 5 x 11 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

- **Timing Generation Circuit**

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

- **LCD Driver Circuit**

LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch. In case of 1-line display mode, COM1 ~ COM8 have 1/8 duty or COM1 ~ COM11 have 1/11duty , and in 2-line mode, COM1 ~ COM16 have 1/16 duty ratio.

- **Cursor/Blink Control Circuit**

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

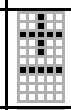
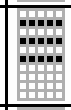
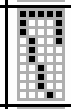
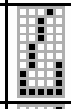
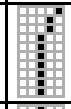
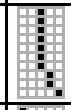
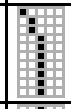
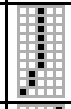
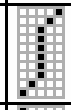
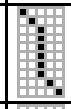
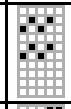
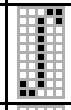
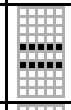
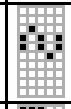
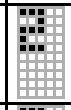
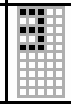
Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: 0A)

NO.7066-0A

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Table 4(Cont.) (ROM Code: 0B)

NO.7066-0B

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Appendix

Table 4(Cont.) (ROM Code: 0E)

NO.7066-0E

Appendix

Character Code (DDRAM Data)								CGRAM Address						Character Patterns (CGRAM Data)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
					0	0	0				0	0	1				0	0	1	0	0
					0	0	0				0	1	0				0	0	1	0	0
					0	0	0				0	1	1				0	0	1	0	0
					0	0	0				1	0	0				0	0	1	0	0
					0	0	0				1	0	1				0	0	1	0	0
					0	0	0				1	1	0				0	0	1	0	0
					0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
					0	0	1				0	0	1				1	0	0	0	1
					0	0	1				0	1	0				1	0	0	0	1
					0	0	1				0	1	1				1	1	1	1	0
					0	0	1				1	0	0				1	0	1	0	0
					0	0	1				1	0	1				1	0	0	1	0
					0	0	1				1	1	0				1	0	0	0	1
					0	0	1				1	1	1				0	0	0	0	0

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:
1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
"-": Indicates no effect.

■ Instructions

There are four categories of instructions that:

- **Designate ST7066U functions, such as display format, data length, etc.**
- **Set internal RAM addresses**
- **Perform data transfer with internal RAM**
- **Others**

Instruction Table:

Instruction	Instruction Code										Description	Description Time (270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.52 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	37 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	37 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37 us
Function Set	0	0	0	0	1	DL	N	F	x	x	DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8	37 us
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	37 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	37 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 us
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	37 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	37 us

Note:
Be sure the ST7066U is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7066U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

Appendix

■ Instruction Description

- **Clear Display**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	x

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

- **Entry Mode Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

➢ **I/D : Increment / decrement of DDRAM address (cursor or blink)**
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

➢ **S: Shift of entire display**
When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

Appendix

- **Display ON/OFF**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**
  When D = "High", entire display is turned on.
  When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**
  When C = "High", cursor is turned on.
  When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**
  When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
  When B = "Low", blink is off.

- **Cursor or Display Shift**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	x	x

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

- **Function Set**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	x	x

- **DL : Interface data length control bit**
  When DL = "High", it means 8-bit bus mode with MPU.
  When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
  When 4-bit bus mode, it needs to transfer 4-bit data by two times.
- **N : Display line number control bit**
  When N = "Low", it means 1-line display mode.
  When N = "High", 2-line display mode is set.
- **F : Display font type control bit**
  When F = "Low", it means 5 x 8 dots format display mode
  When F = "High", 5 x11 dots format display mode.

N	F	No. of Display Lines	Character Font	Duty Factor
L	L	1	5x8	1/8
L	H	1	5x11	1/11
H	x	2	5x8	1/16

- **Set CGRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

- **Set DDRAM Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

- **Read Busy Flag and Address**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

When BF = “High”, indicates that the internal operation is being processed.So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

- **Write Data to CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from CGRAM or DDRAM**

	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

■ Reset Function

Initializing by Internal Reset Circuit

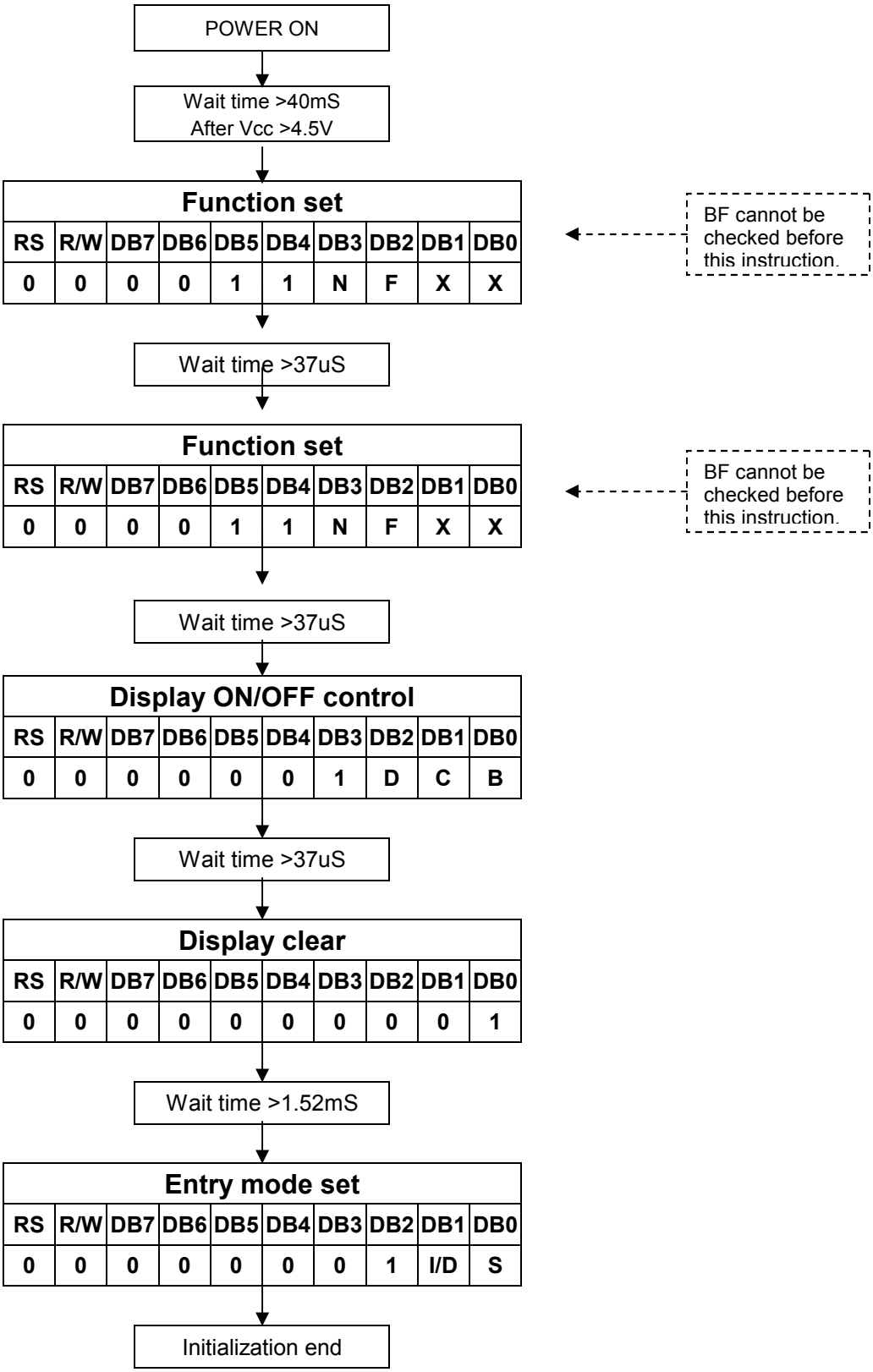
An internal reset circuit automatically initializes the ST7066U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

1. Display clear
2. Function set:
   DL = 1; 8-bit interface data
   N = 0; 1-line display
   F = 0; 5x8 dot character font
3. Display on/off control:
   D = 0; Display off
   C = 0; Cursor off
   B = 0; Blinking off
4. Entry mode set:
   I/D = 1; Increment by 1
   S = 0; No shift

Note:
If the electrical characteristics conditions listed in the table Power Supply Conditions (Page 31) are not met, the internal reset circuit will not operate normally and will fail to initialize the ST7066U. For such a case, initialization must be performed by the MPU as explain by the following figures.

■ Initializing by Instruction

● **8-bit Interface (fosc=270KHz)**

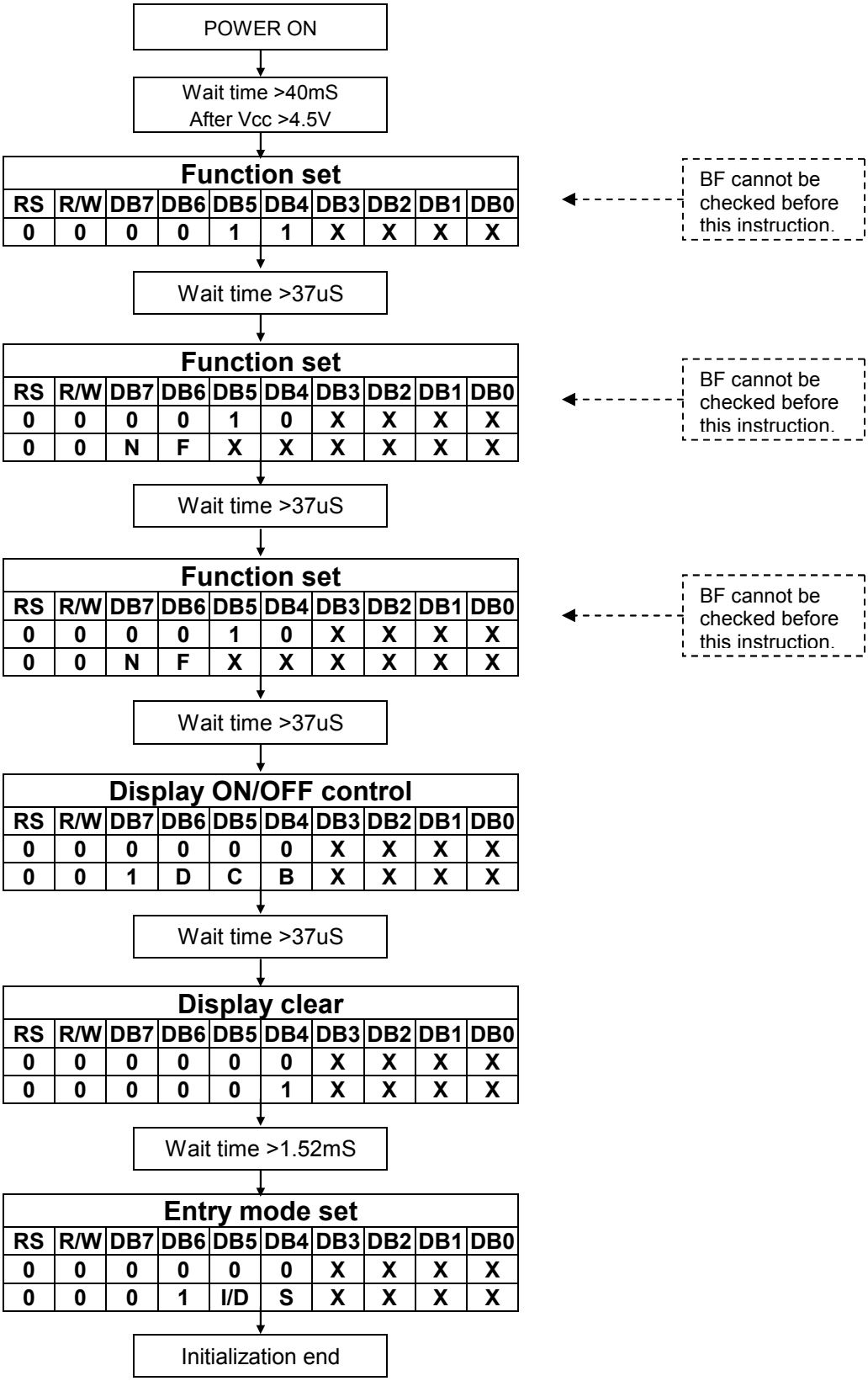


Appendix

➢ **Initial Program Code Example For 8051 MPU(8 Bit Interface):**

```
;-------------------------------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK       ;CURSOR MOVES TO RIGHT
        CALL    DELAY37uS
;-------------------------------------------------------------------------------
MAIN_START:

        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
          .
          .
;-------------------------------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        CLR     RS                      ;EX:Port 3.0
        CLR     RW                      ;EX:Port 3.1
        SETB    E                       ;EX:Port 3.2
        MOV     P1,A                    ;EX:Port 1=Data Bus
        CLR     E
        MOV     P1,#FFH                 ;For Check Busy Flag
        RET
;-------------------------------------------------------------------------------
CHK_BUSY:                               ;Check Busy Flag
        CLR     RS
        SETB    RW
        SETB    E
        JB      P1.7,$
        CLR     E
        RET
```

- **4-bit Interface (fosc=270KHz)**



Appendix

➢ **Initial Program Code Example For 8051 MPU(4 Bit Interface):**

```
;---------------------------------------------------------------
INITIAL_START:
        CALL    DELAY40mS

        MOV     A,#38H          ;FUNCTION SET
        CALL    WRINS_ONCE      ;8 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#28H          ;FUNCTION SET
        CALL    WRINS_NOCHK     ;4 bit,N=1,5*7dot
        CALL    DELAY37uS

        MOV     A,#0FH          ;DISPLAY ON
        CALL    WRINS_CHK
        CALL    DELAY37uS

        MOV     A,#01H          ;CLEAR DISPLAY
        CALL    WRINS_CHK
        CALL    DELAY1.52mS

        MOV     A,#06H          ;ENTRY MODE SET
        CALL    WRINS_CHK
        CALL    DELAY37uS
;---------------------------------------------------------------
MAIN_START:
        XXXX
        XXXX
        XXXX
        XXXX
          .
          .
          .
          .
          .
          .
          .
          .
          .
          .
          .
          .
```

```
;---------------------------------------------------------------
WRINS_CHK:
        CALL    CHK_BUSY
WRINS_NOCHK:
        PUSH    A
        ANL     A,#F0H
        CLR     RS              ;EX:Port 3.0
        CLR     RW              ;EX:Port 3.1
        SETB    E               ;EX:Port 3.2
        MOV     P1,A            ;EX:Port1=Data Bus
        CLR     E
        POP     A
        SWAP    A
WRINS_ONCE:
        ANL     A,#F0H
        CLR     RS
        CLR     RW
        SETB    E
        MOV     P1,A
        CLR     E
        MOV     P1,#FFH         ;For Check Bus Flag
        RET
;---------------------------------------------------------------
CHK_BUSY:                       ;Check Busy Flag
        PUSH    A
        MOV     P1,#FFH
$1
        CLR     RS
        SETB    RW
        SETB    E
        MOV     A,P1
        CLR     E
        MOV     P1,#FFH
        CLR     RS
        SETB    RW
        SETB    E
        NOP
        CLR     E
        JB      A.7,$1
        POP     A
        RET
```

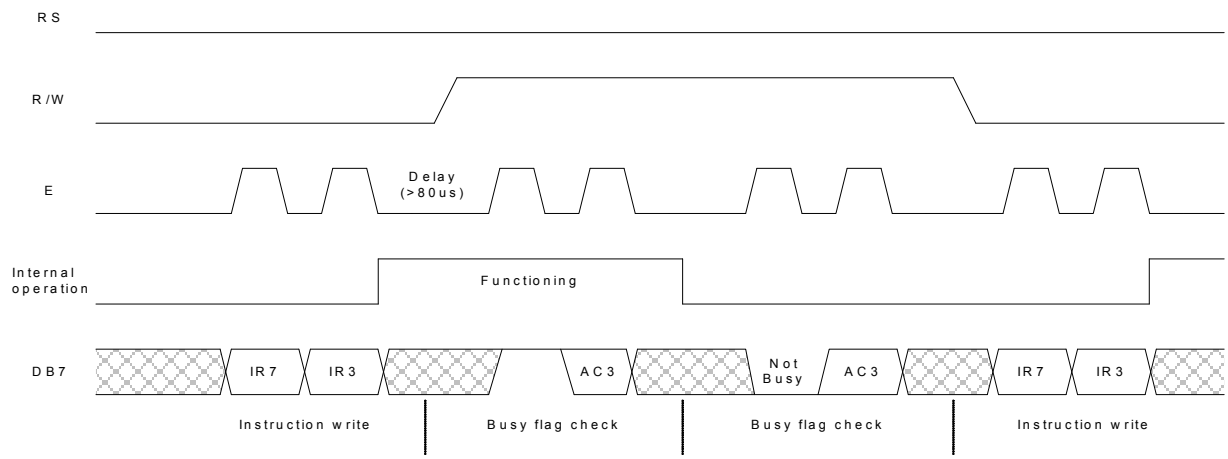
Appendix

■ Interfacing to the MPU

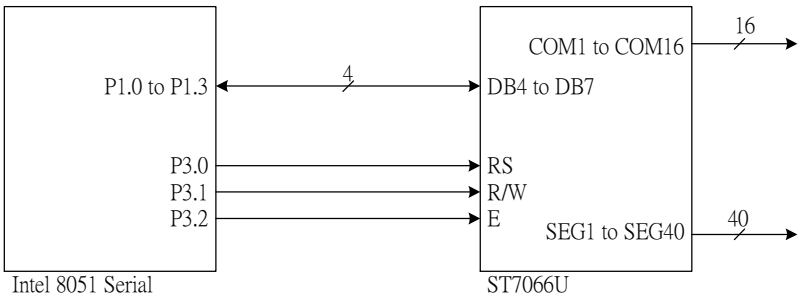
The ST7066U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPU.

- **For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer.** Bus lines DB0 to DB3 are disabled. The data transfer between the ST7066U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

➢ **Example of busy flag check timing sequence**



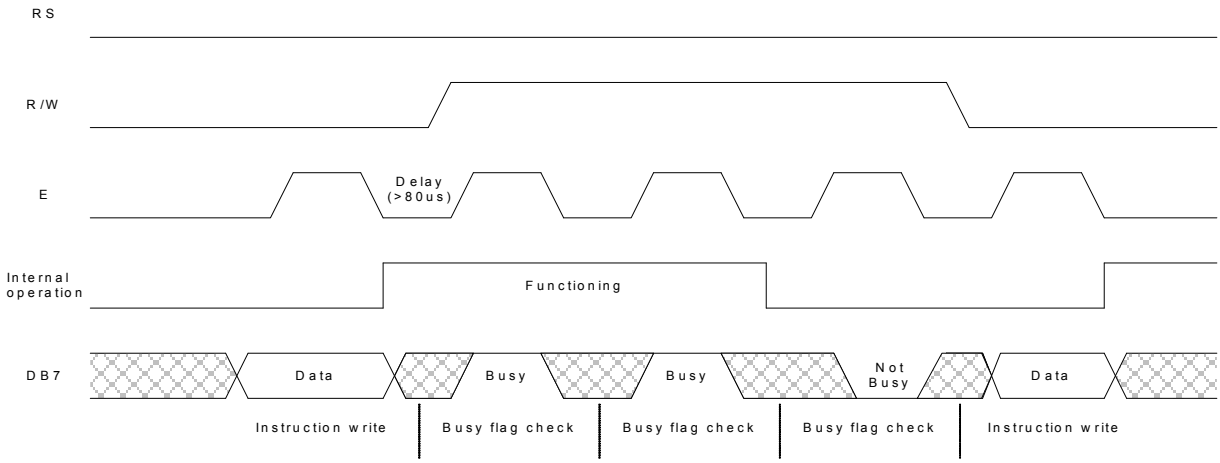
➢ **Intel 8051 interface**



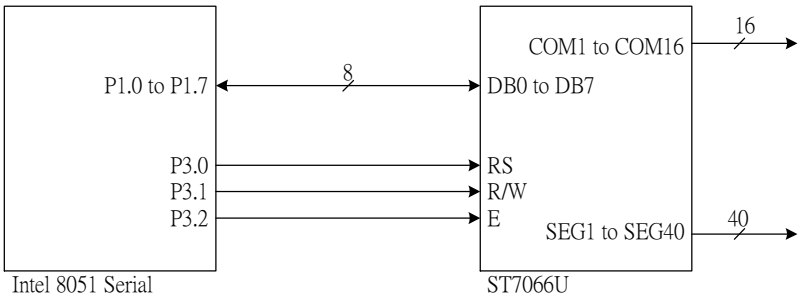
Appendix

- **For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.**

➢ **Example of busy flag check timing sequence**



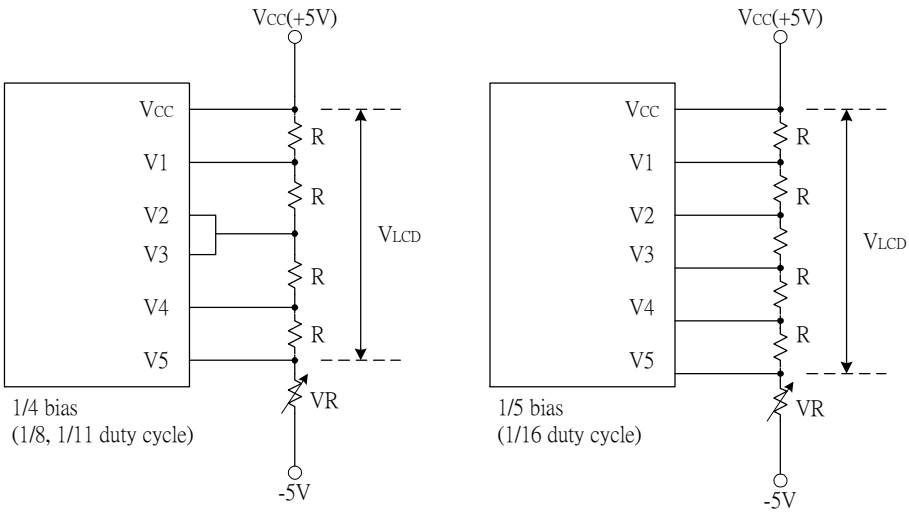
➢ **Intel 8051 interface**



■ Supply Voltage for LCD Drive

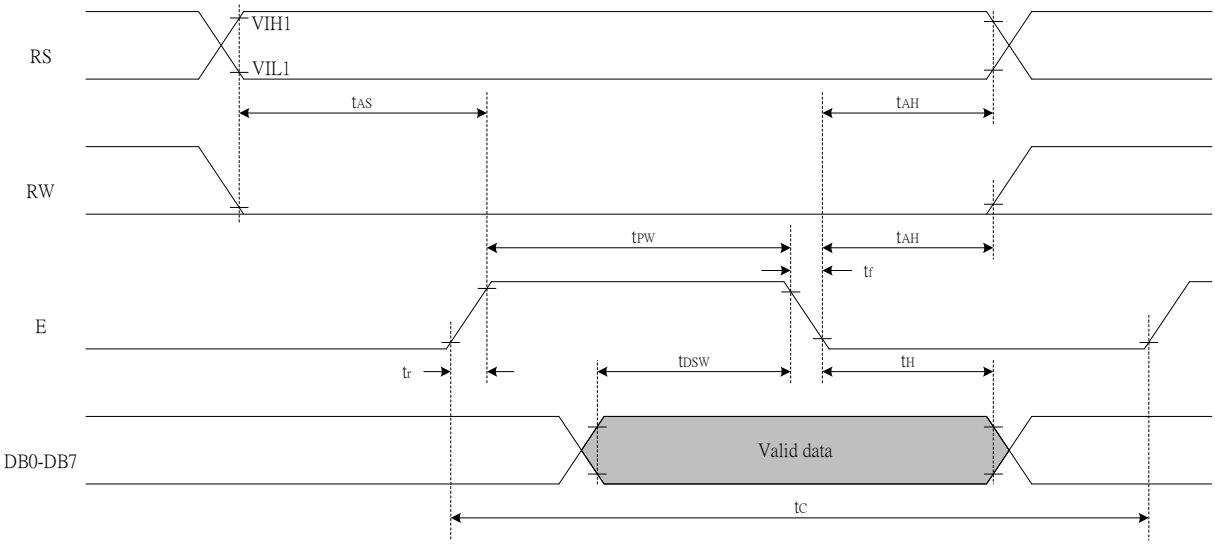
There are different voltages that supply to ST7066U's pin (V1 - V5) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as below:

	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Supply Voltage	1/4	1/5
V1	Vcc - 1/4VLCD	Vcc - 1/5VLCD
V2	Vcc - 1/2VLCD	Vcc - 2/5VLCD
V3	Vcc - 1/2VLCD	Vcc - 3/5VLCD
V4	Vcc - 3/4VLCD	Vcc - 4/5VLCD
V5	Vcc - VLCD	Vcc- VLCD

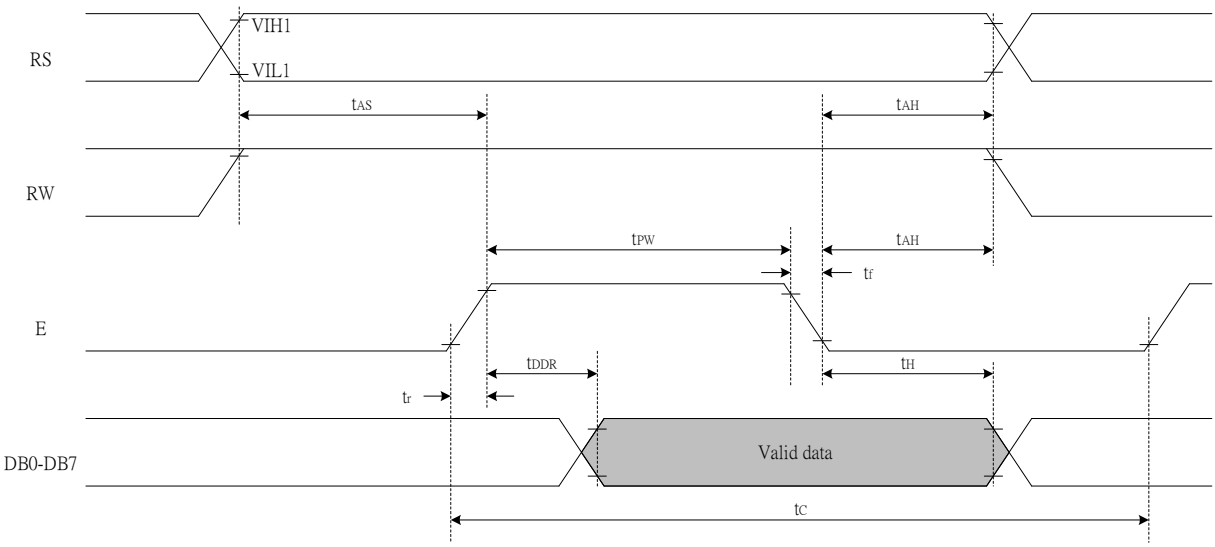


■ Timing Characteristics

- **Writing data from MPU to ST7066U**

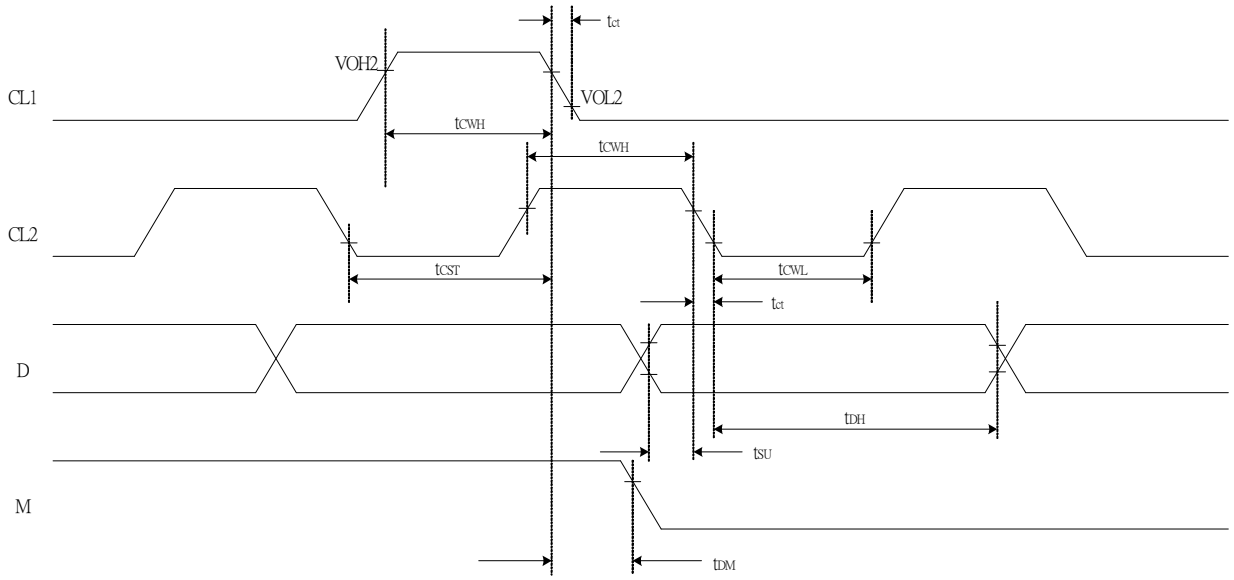


- **Reading data from ST7066U to MPU**

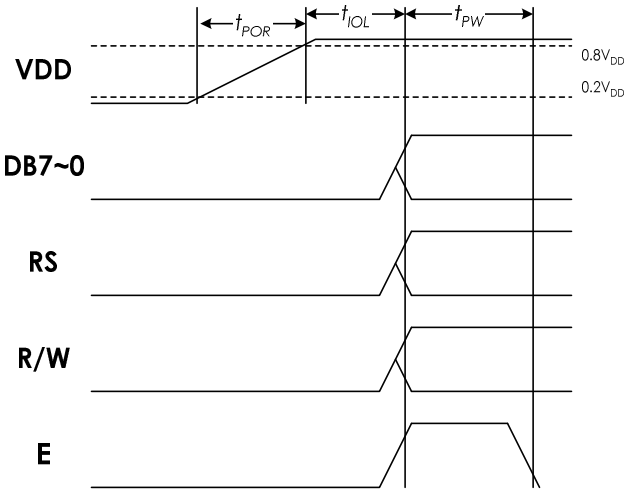


Appendix

- **Interface Timing with External Driver**



■ Power Supply Conditions



Symbol	Characteristics	Description	Min.	Typ.	Max.	Unit
tPOR	Power rise time	Power rise time that will trigger internal power on reset circuit	0.1		100	ms
tIOL	I/O Low time	The period that I/O is kept low.	40			ms
tPW	Enable pulse width	**Please refer to the following tables.**				

1. **During tPOR, VDD noise should be reduced (especially close to 2.0V). Otherwise the Power-ON-Reset function might be triggered several times and maybe cause unexpected result.**
2. **During tIOL, the I/O ports of the interface (control and data signals) should be kept at "Low".**

Appendix

■ AC Characteristics

(TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 75KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7066U)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	460	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	80	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from ST7066U to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	480	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	320	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Interface Mode with LCD Driver(ST7065)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

Appendix

■ AC Characteristics

(TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	R = 91KΩ	190	270	350	KHz
External Clock Operation						
f_{EX}	External Frequency	-	125	270	410	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	μs
Write Mode (Writing data from MPU to ST7066U)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from ST7066U to MPU)						
T_C	Enable Cycle Time	Pin E	1200	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	140	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	0	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	100	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Interface Mode with LCD Driver(ST7065)						
T_{CWH}	Clock Pulse with High	Pins: CL1, CL2	800	-	-	ns
T_{CWL}	Clock Pulse with Low	Pins: CL1, CL2	800	-	-	ns
T_{CST}	Clock Setup Time	Pins: CL1, CL2	500	-	-	ns
T_{SU}	Data Setup Time	Pin: D	300	-	-	ns
T_{DH}	Data Hold Time	Pin: D	300	-	-	ns
T_{DM}	M Delay Time	Pin: M	0	-	2000	ns

Appendix

■ Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{CC}	-0.3 to +7.0
LCD Driver Voltage	V_{LCD}	Vcc-10.0 to Vcc+0.3
Input Voltage	V_{IN}	-0.3 to V_{CC}+0.3
Operating Temperature	T_A	-40°C to + 90°C
Storage Temperature	T_{STO}	-55°C to + 125°C

■ DC Characteristics

(TA = 25℃ , VCC = 2.7 V – 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	2.7	-	4.5	V
V_{LCD}	LCD Voltage	V_{CC}-V5	3.0	-	10.0	V
I_{CC}	Power Supply Current	f_{OSC} = 270KHz V_{CC}=3.0V	-	0.1	0.25	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2Vcc	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.75 Vcc	-	-	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.2Vcc	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{CC}	-	V_{CC}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2V_{CC}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	V_{CC} = 3V	-10	-50	-120	μA

Appendix

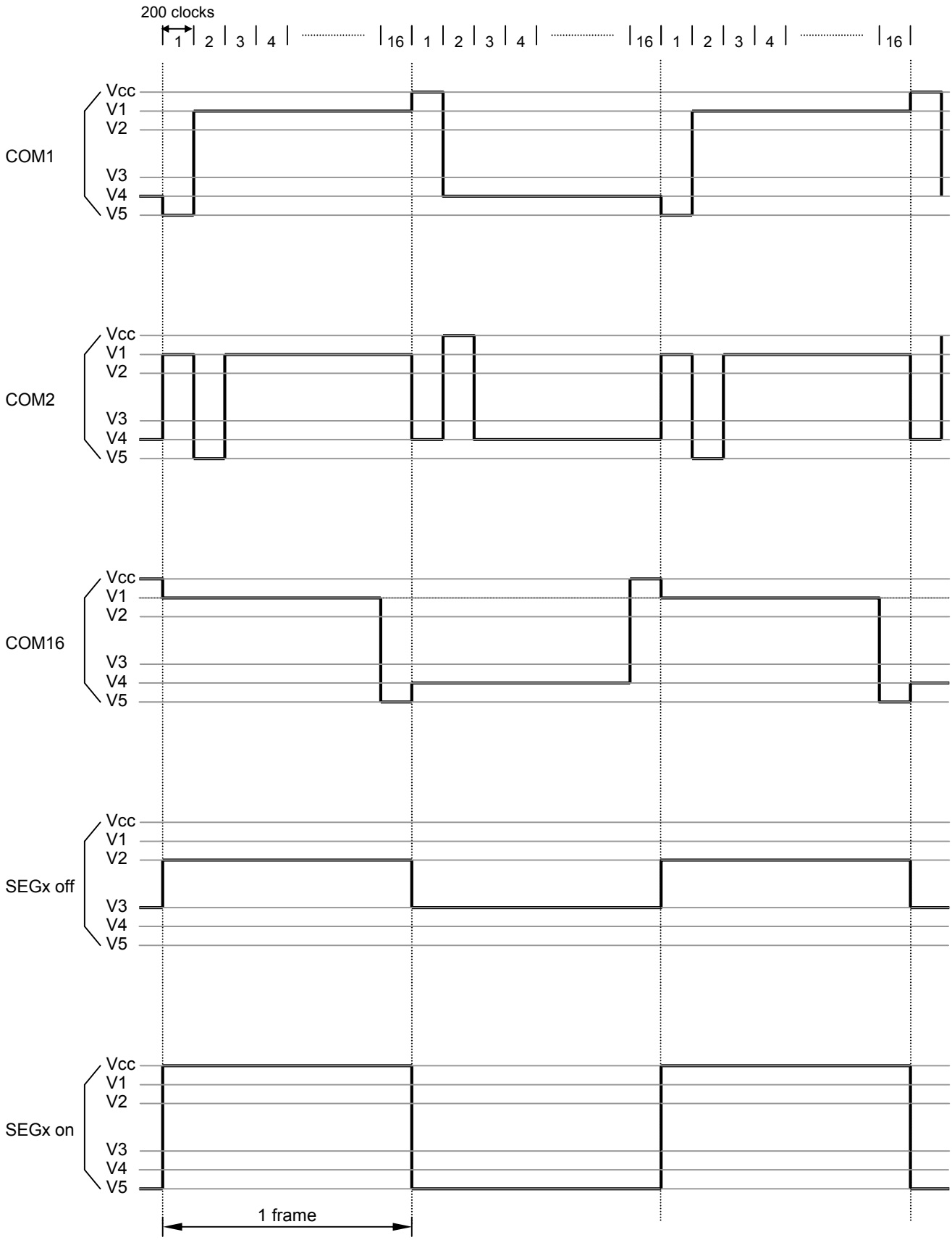
■ DC Characteristics

(TA = 25℃, V_{CC} = 4.5 V - 5.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	4.5	-	5.5	V
V_{LCD}	LCD Voltage	V_{CC}-V5	3.0	-	10.0	V
I_{CC}	Power Supply Current	f_{OSC} = 270KHz V_{CC}=5.0V	-	0.2	0.5	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7Vcc	-	V_{CC}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	-0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	V_{CC}-1	-	V_{CC}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	1.0	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	3.9	-	V_{CC}	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.4	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.9V_{CC}	-	V_{CC}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.1V_{CC}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{CC}	-1	-	1	μA
I_{PUP}	Pull Up MOS Current	V_{CC} = 5V	-50	-110	-180	μA

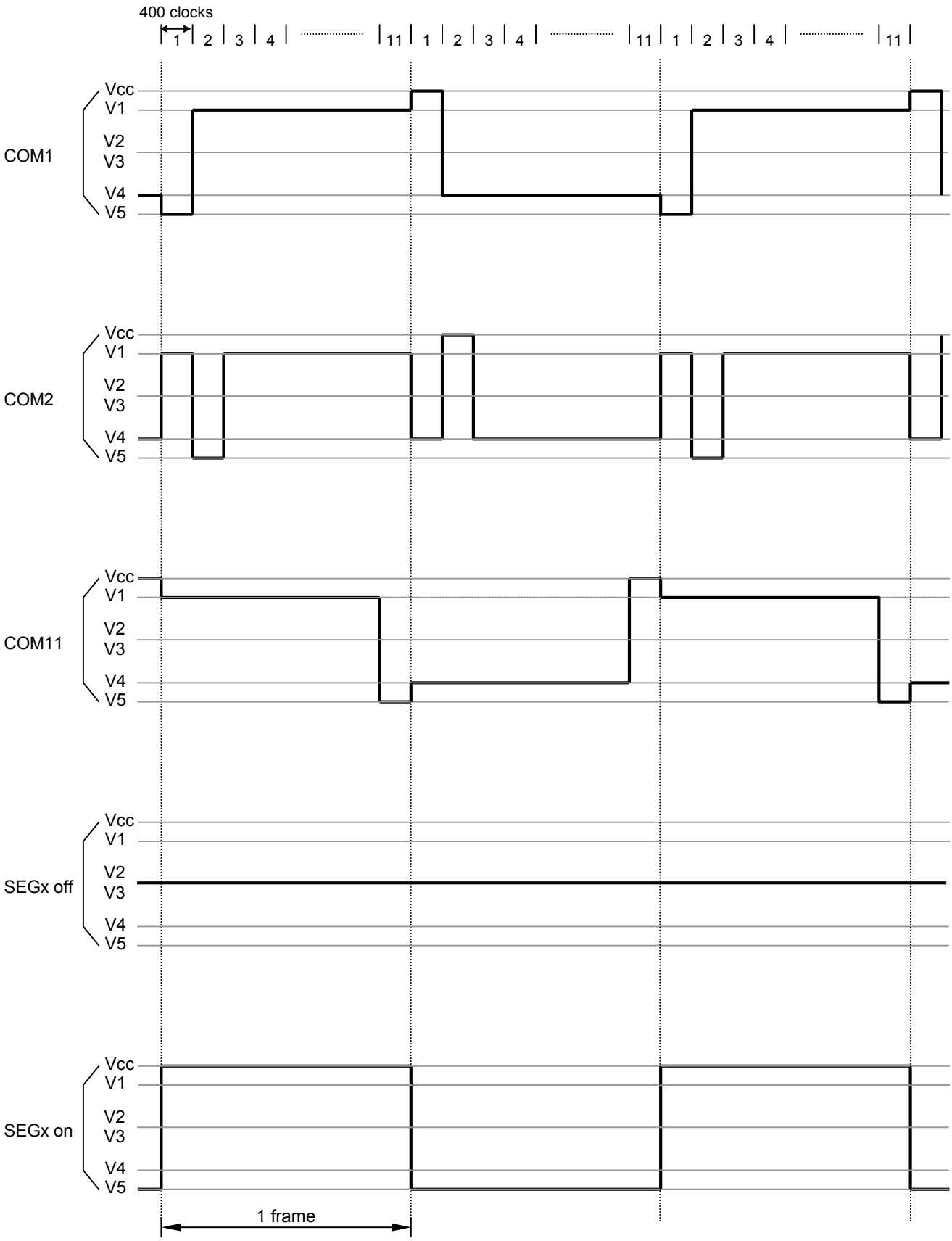
■ LCD Frame Frequency

- **Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/16 duty; 1/5 bias,1 frame = 3.7us x 200 x 16 = 11840us=11.8ms(84.7Hz)**



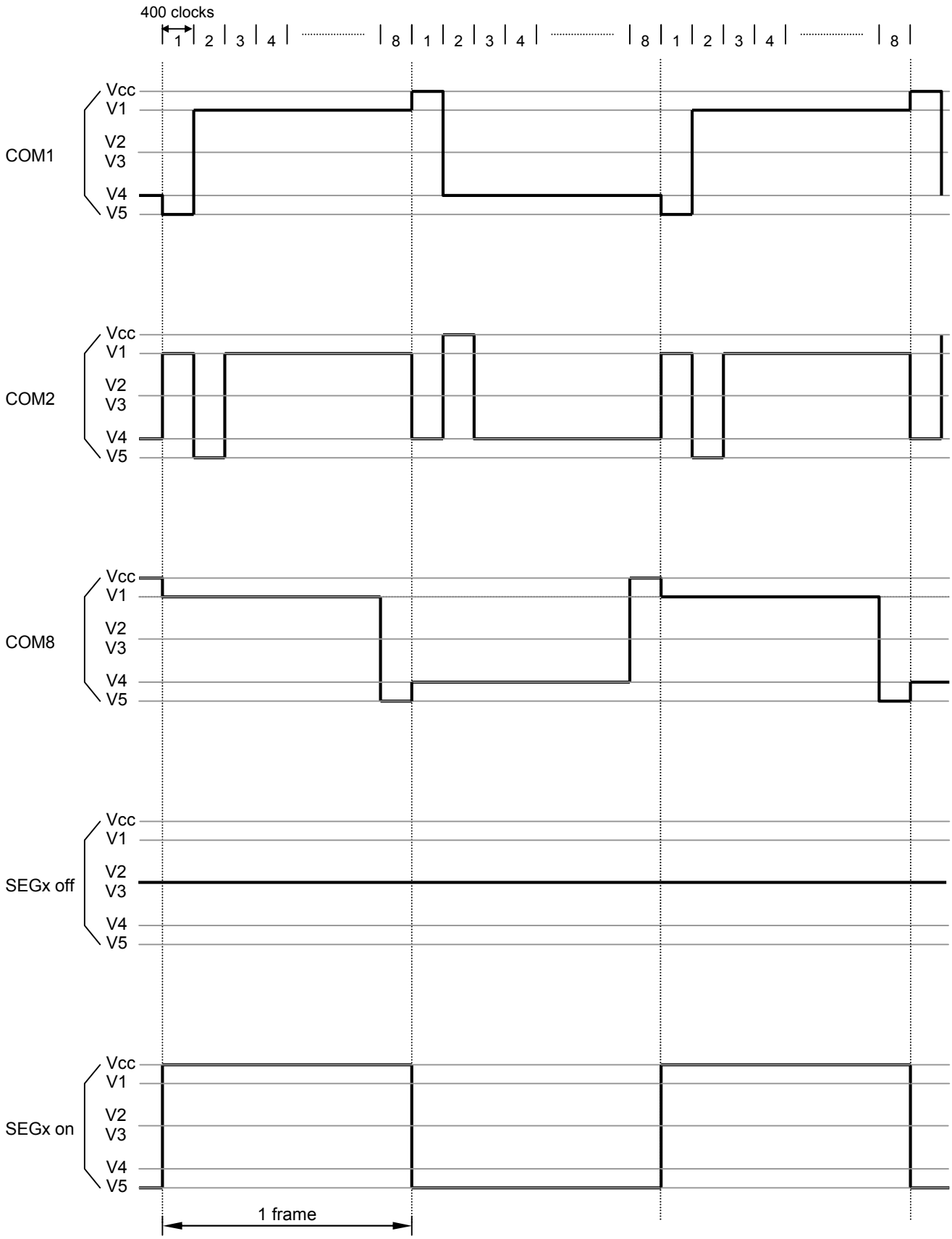
Appendix

- **Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/11 duty; 1/4 bias,1 frame = 3.7us x 400 x 11 = 16280us=16.3ms (61.3Hz)**



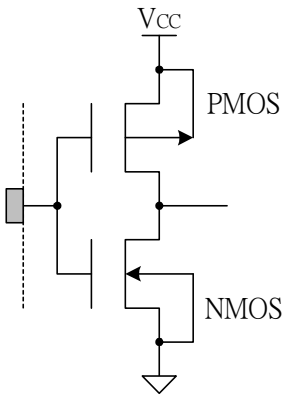
Appendix

- **Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/8 duty; 1/4 bias,1 frame = 3.7us x 400 x 8 = 11840us=11.8ms (84.7Hz)**

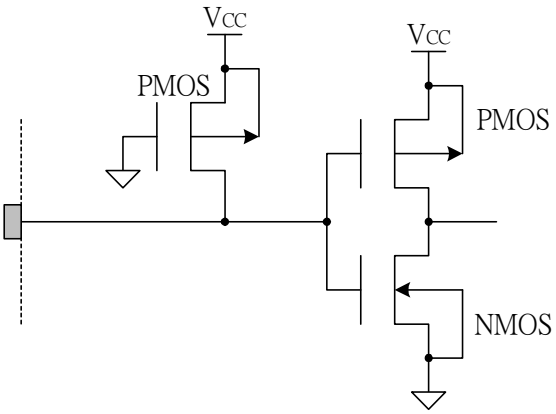


Appendix

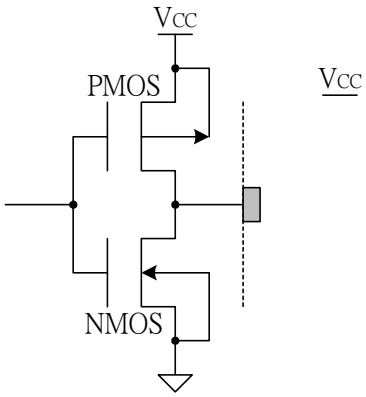
■ I/O Pad Configuration



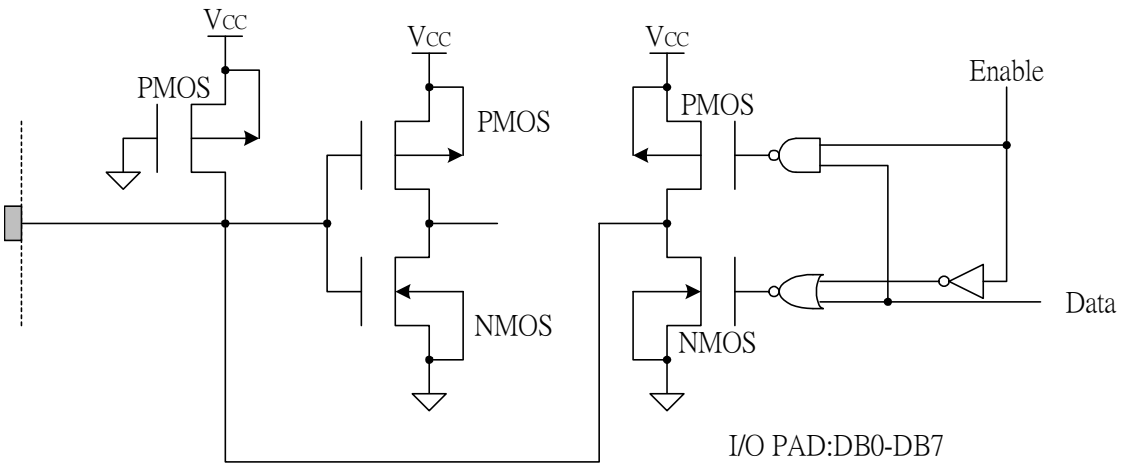
Input PAD:E(No Pull up)



Input PAD:RS,R/W(With Pull up)



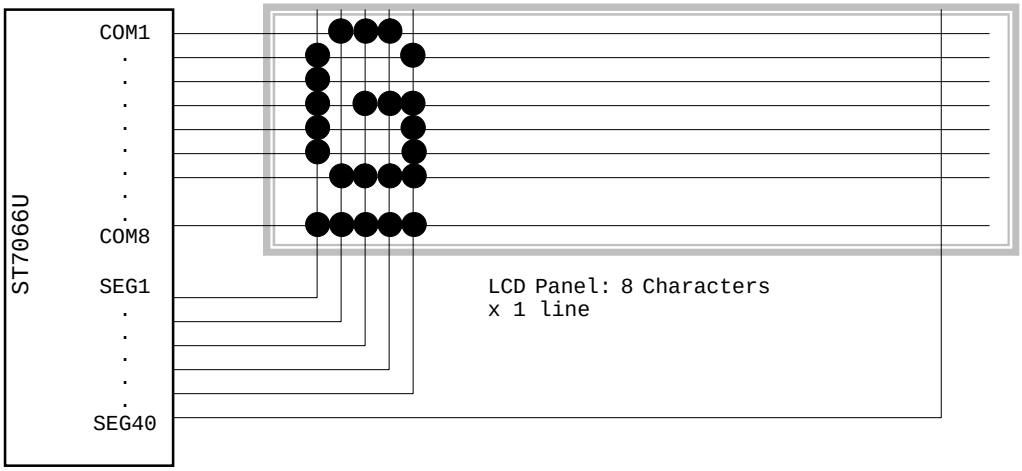
Output PAD:CL1,CL2,M,D



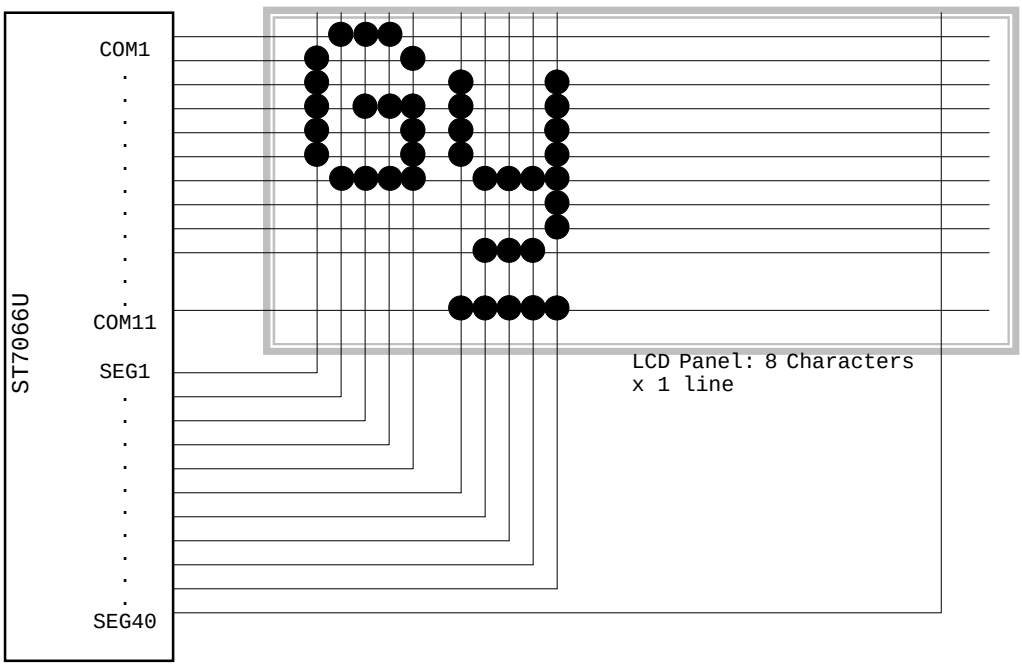
I/O PAD:DB0-DB7

■ LCD and ST7066U Connection

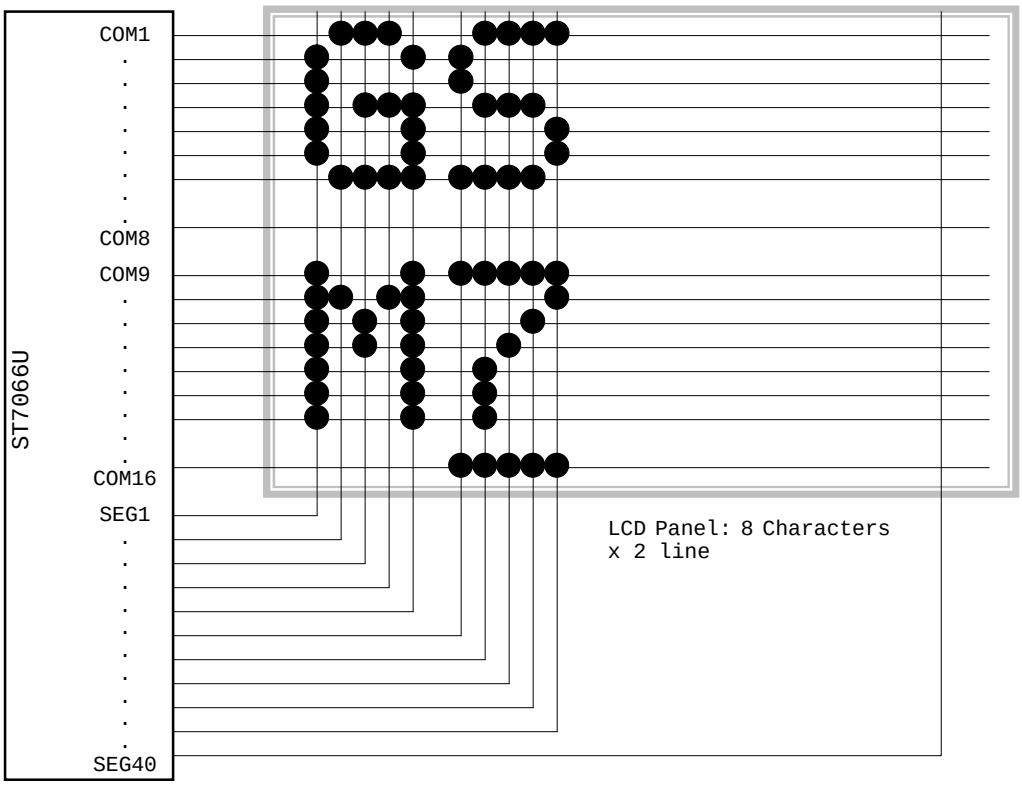
1. 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



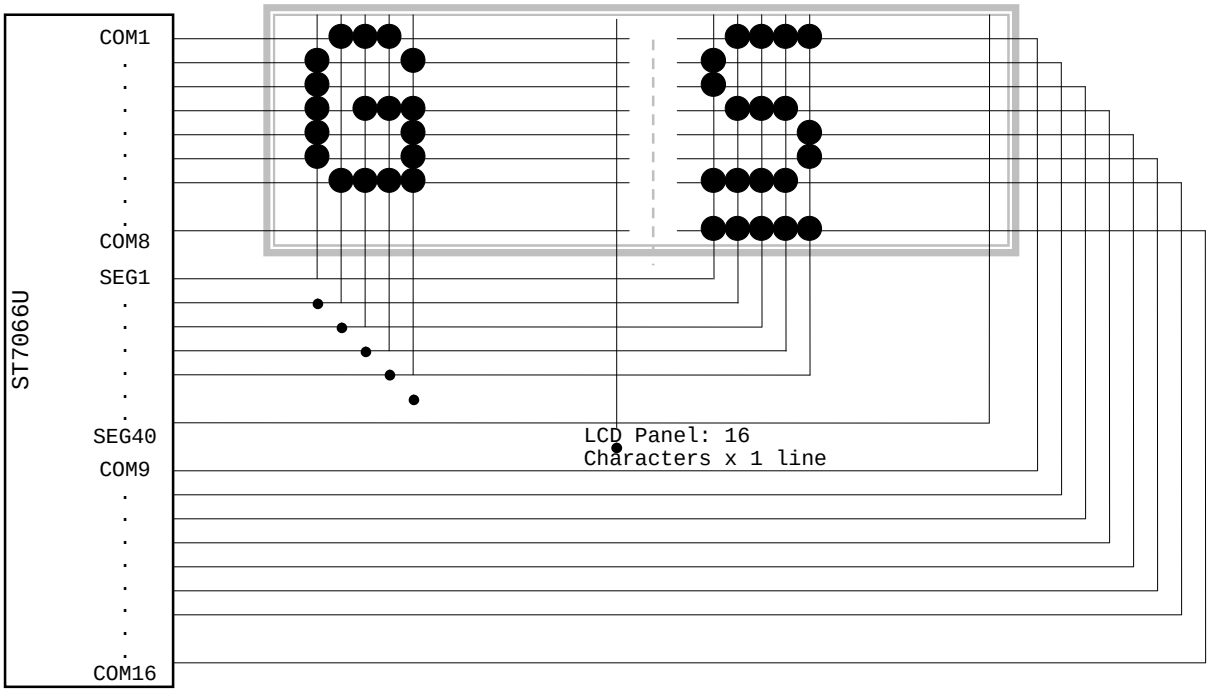
2. 5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)



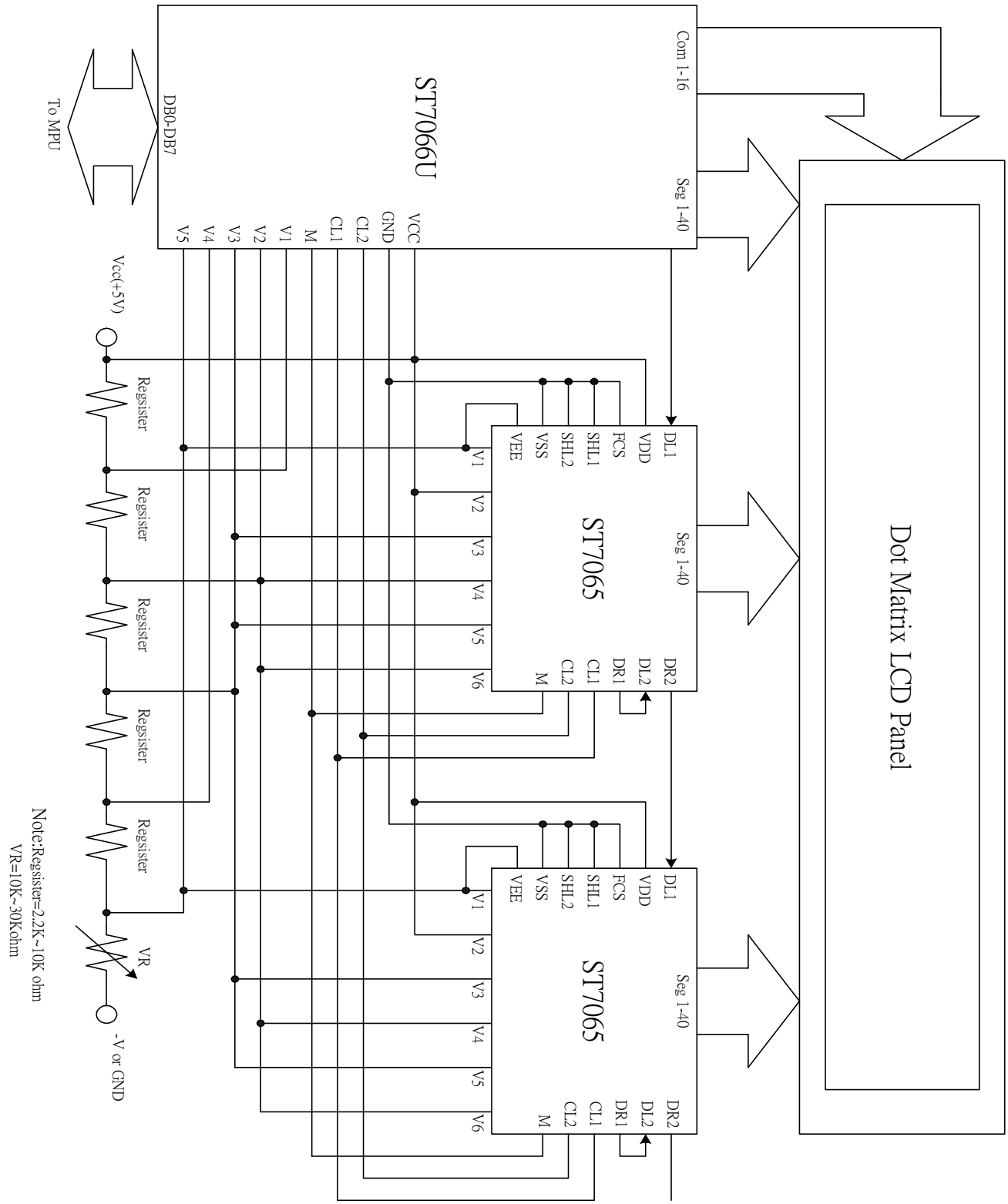
3. 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



4. 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)



■ Application Circuit



Appendix