

Crystalfontz America, Inc.

CUSTOMER : _____

MODULE NO.: CFAL12864S-Y-B1

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY
ISSUED DATE:			

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1.Module Classification Information

CFA L 12864 S—Y— B1
① ② ③ ④ ⑤ ⑥

①Brand :	CRYSTALFONTZ AMERICA, INCORPORATED		
②Display Type :	H→Character Type, G→Graphic Type , L→ OLED		
③Display's Logical Dimensions :	128 columns by 64 rows.		
④Model Variant:	S		
⑤Color :	Y→Yellow		
⑥Special Code	B1→TAB/COF		

2.Precautions in use of OLED Modules

- (1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2)Don't make extra holes on the printed circuit board, modify its shape or change the components of OLED module.
- (3)Don't disassemble the OLED.
- (4)Don't operate it above the absolute maximum rating.
- (5)Don't drop, bend or twist OLED.
- (6)Soldering: only to the I/O terminals.
- (7)Storage: please storage in anti-static electricity container and clean environment.

3.General Specification

Item	Dimension	Unit
Number of Characters	128 columns x 64 Rows	—
Module dimension	60.5 x 56.6 x 2.01 (MAX)	mm
View area	57.01 x 29.49	mm
Active area	55.01 x 27.49	mm
Dot size	0.40 x 0.40	mm
Dot pitch	0.43 x 0.43	mm
LCD type	OLED , Yellow	
Duty	1/64	

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _{OP}	-20	—	+70	°C
Storage Temperature	T _{ST}	-30	—	+80	°C
OLED Operating Voltage	V _{CC}	8	—	16	V
Input Voltage	V _I	0	—	V _{DD}	V
Supply Voltage	V _{DD} -V _{SS}	2.4	3.0	3.5	V

5.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}	—	2.4	2.7	3.5	V
OLED Driver Supply Voltage	V_{CC}	—	2.4	2.7	3.5	V
Operating Current for V_{DD}	I_{DD}	Contrast = FF	—	190	300	μA
Operating Current for V_{PP}	I_{CC}	Contrast=FF	—	550	1000	μA
Input High Volt.	V_{IH}	—	$0.8 * V_{DDI}$	—	—	V
Input Low Volt.	V_{IL}	—	—	—	$0.2 * V_{DDI}$	V
Output High Volt.	V_{OH}	—	$0.9 * V_{DDI}$	—	—	V
Output Low Volt.	V_{OL}	—	—	—	$0.1 * V_{DDI}$	V
Normal mode Power consumption	P_T	All pixels on	—	—	400	mW

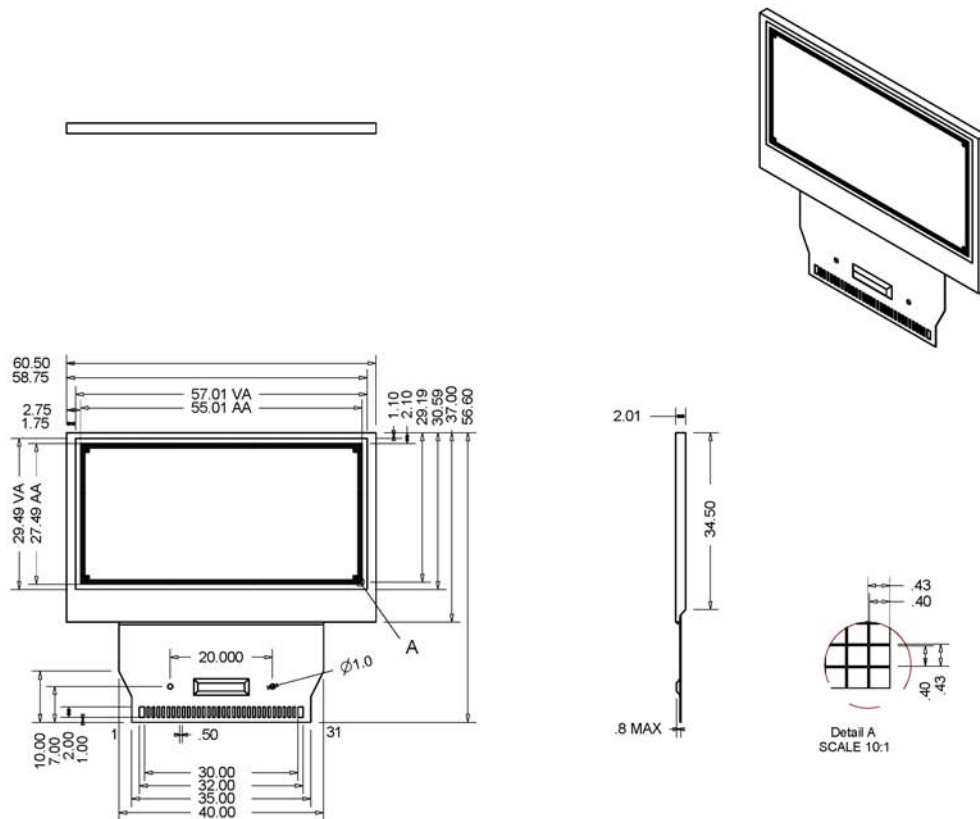
6.Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) θ			160		deg
	(H) ϕ			160		deg
Contrast Ratio (Dark Room)	CR	80cd/m ²	—	200:1	—	—
Brightness		With polarizer		80		cd/m ²

7.Interface Pin Function

PIN NO	PIN NAME	DESCRIPTION															
1	NC	No Connection															
2	VCC	OLED drive voltage, It should be supplied externally.															
3	VCOMH	This is an input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.															
4	IREF	This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.															
5-12	D7-D0	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input, SDIN, and D0 will be the serial clock input, SCLK.															
13	E(RD#)	This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#) signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW.															
14	R/W(WR#)	This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode. When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.															
15	D/C#	Data/Command Select. This is the Data/Command control pin. When it is pulled HIGH, the input at D7-D0 is treated as display data. When it is pulled LOW, the input at D7-D0 is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
16	RES#	Reset, active low															
17	CS#	Chip Select, active low															
18	NC	No Connection															
19	BS2	<div>These are MCU interface input selection pins. See the following table for selecting different interfaces:</div> <table><tr><th>Pin Name</th><th>I2C Inter face</th><th>6800-parallel Interface</th><th>8080-parallel interface</th><th>Serial interface</th></tr><tr><td>BS1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>BS2</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>	Pin Name	I2C Inter face	6800-parallel Interface	8080-parallel interface	Serial interface	BS1	1	0	1	0	BS2	0	1	1	0
Pin Name	I2C Inter face		6800-parallel Interface	8080-parallel interface	Serial interface												
BS1	1		0	1	0												
BS2	0	1	1	0													
20	BS1																
21	VDD	Power supply for interface logic level. It should be match with MCU interface voltage level. VDDIO must always be equal or lower than VDD.															
22	NC	No connection															
23	NC																
24	NC																
25	Test4	Reserved pin; No connection and left float.															
26	Test3																
27	Test2																
28	Test1																
29	Test0																
30	VSS	Ground															
31	NC	No Connection															

8. Contour Drawing & Block Diagram



 CrystalFontz America, Incorporated

Part No.(s): CFAL12864Z-Y-B1

SCALE:
1:1

UNITS:

UNITS:
MILLIMETERS

DRAWN BY:	
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BRIAN

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DRAWING NUMBER:	
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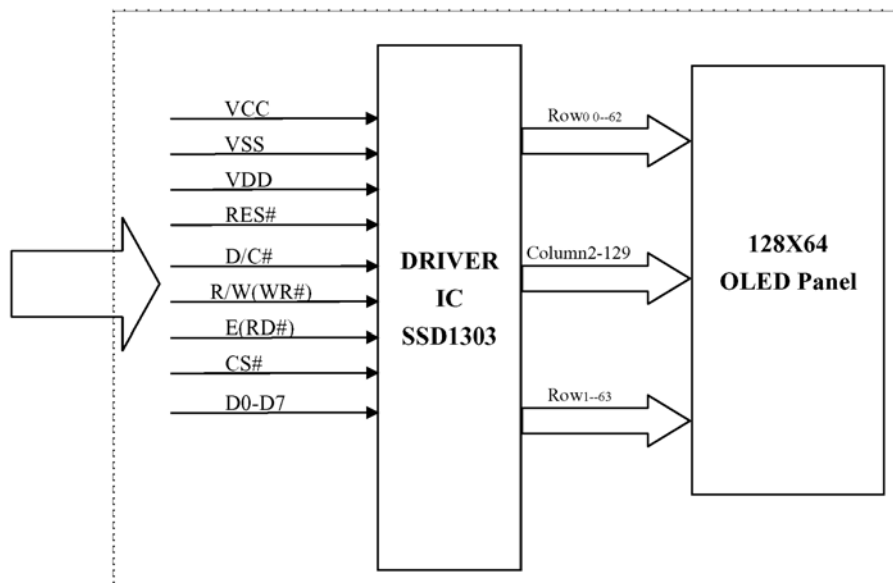
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DATE: 2008/09/23

HARDWARE REV:

1.0

SHEET:
1 of 1

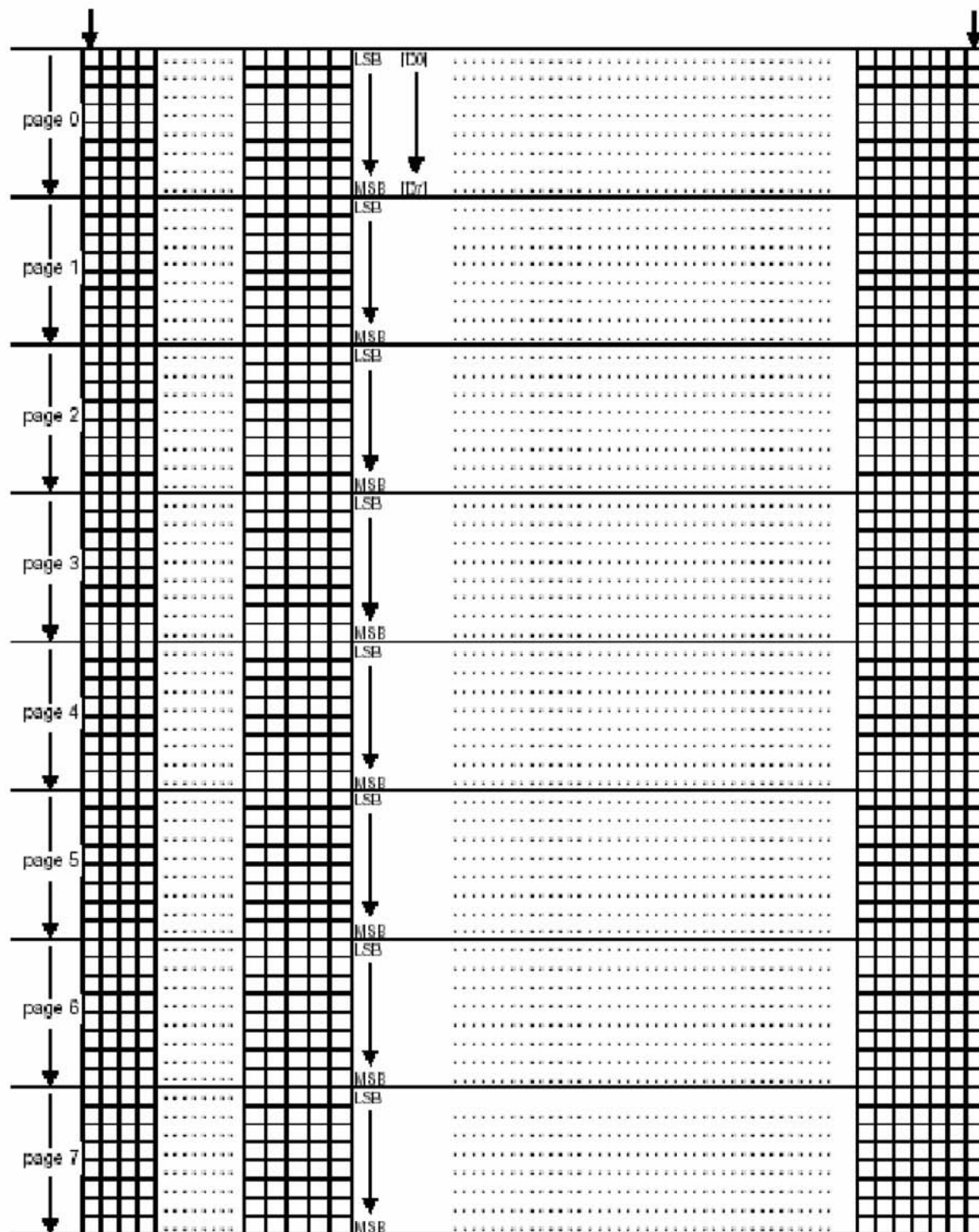


NOTE: Some pins omitted

9. Graphic Display DDRAM Map

Column address 00H

Column address 7FH



10. Instruction Table

Command table (D/C =0, R/W (WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Address **	Set the lower nibble of the column address register using X ₃ X ₂ X ₁ X ₀ as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Address **	Set the higher nibble of the column address register using X ₃ X ₂ X ₁ X ₀ as data bits. The initial display line register is reset to 0000b after RESET.
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[2:0] Set the number of column scroll per step Valid value: 001b, 010b, 011b, 100b
0	A[2:0]	*	*	*	*	*	A ₂	A ₁	A ₀		B[2:0] Define start page address
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	B ₀		C[1:0] Set time interval between each scroll step in terms of frame frequency
0	C[1:0]	*	*	*	*	*	*	C ₁	C ₀		
0	D[2:0]	*	*	*	*	*	D ₂	D ₁	D ₀		00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40-7F	0	1	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₅ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000 during RESET
0	81	1	0	0	0	0	0	0	1	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	82	1	0	0	0	0	0	1	0	Brightness for color banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT)	Set current drive pulse width of Bank 0, Color A, B and C.
0	X[5:0]	*	*	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀		Bank 0: X[5:0] = 31... 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b)
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		Color A: A[5:0] same as above (RESET = 111111b)
0	B[5:0]	*	*	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		Color B: B[5:0] same as above (RESET = 111111b)
0	C[5:0]	*	*	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		Color C: C[5:0] same as above (RESET = 111111b)
											Note: color D pulse width is fixed at 64 clocks pulse.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank color of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 1
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 2
0	B[7:0]	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		:
0	C[7:0]	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		:
0	D[7:0]	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:6] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank color of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 17
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 18
0	B[7:0]	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		:
0	C[7:0]	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		:
0	D[7:0]	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:6] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 32
0	A0~ A1	1	0	1	0	0	0	0	X ₀	Set Segment Re-map **	X ₀ =0: column address 0 is mapped to SEG0 (RESET) X ₀ =1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X ₀	Set Entire Display ON/OFF **	X ₀ =0: normal display (RESET) X ₀ =1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X ₀	Set Normal/Inverse Display **	X ₀ =0: normal display (RESET) X ₀ =1: inverse display
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, RESET= 64MUX
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0	AD	1	0	1	0	1	1	0	1	Set DC-DC on/off	X ₀ : 1 DC-DC will be turned on when display on (RESET) 0 DC-DC is disable
0		1	0	0	0	1	0	1	X ₀		
0	AE~AF	1	0	1	0	1	1	1	X ₀	Set Display ON/OFF **	X ₀ =0: turns OFF OLED panel (RESET) X ₀ =1: turns ON OLED panel
0	B0~BF	1	0	1	1	X ₃	X ₂	X ₁	X ₀	Set Page Address **	Set GDDRAM Page Address (0~7) for read/write using X ₃ X ₂ X ₁ X ₀
0	C0/C8	1	1	0	0	X ₃	*	*	*	Set COM Output Scan Direction **	X ₃ =0: normal mode (RESET) Scan from COM 0 to COM [N-1] X ₃ =1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X ₀	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	D3 A[5:0]	1 *	1 *	0 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Display Offset **	Set vertical scroll by COM from 0-63. The value is reset to 00H after RESET.
0 0	D5 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] Define the divide ratio of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] Set the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b
0 0	D8	1 0	1 0	0 X ₅	1 X ₄	1 0	0 X ₂	0 0	0 X ₀	Set area color mode on/off & low power display mode	X ₅ X ₄ = 00 (RESET) : mono mode X ₅ X ₄ = 11 Area Color enable X ₂ =0 and X ₀ =0: Normal (RESET) power mode X ₂ =1 and X ₀ =1: Set low power save mode
0 0	D9 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Pre-charge period**	A[3:0] Phase 1 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry A[7:4] Phase 2 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry
0 0	DA	1 0	1 0	0 0	1 X ₄	1 0	0 0	1 1	0 0	Set COM pins hardware configuration	X ₄ =0, Sequential COM pin configuration (i.e. COM31, 30, 29....0 ; SEG0-132; COM31,32....62,63) X ₄ =1(RESET), Alternative COM pin configuration (i.e. COM62,60,58,...2,0; SEG0-132; COM1,3,5...61,63)
0 0	DB A[6:0]	1 *	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	1 A ₁	1 A ₀	Set VCOM Deselect Level	A[6:0] 0000000 low VCOM deselect level (~ 0.43 Vref) 0110101 normal VCOM deselect level (~ 0.77*Vref (RESET)) 1111111 high VCOM deselect level (equal Vref)
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Status Register Read *	D ₇ : Reserve D ₆ : "1" for display OFF / "0" for display ON D ₅ : Reserve D ₄ : Reserve D ₃ : Reserve D ₂ : Reserve D ₁ : Reserve D ₀ : Reserve

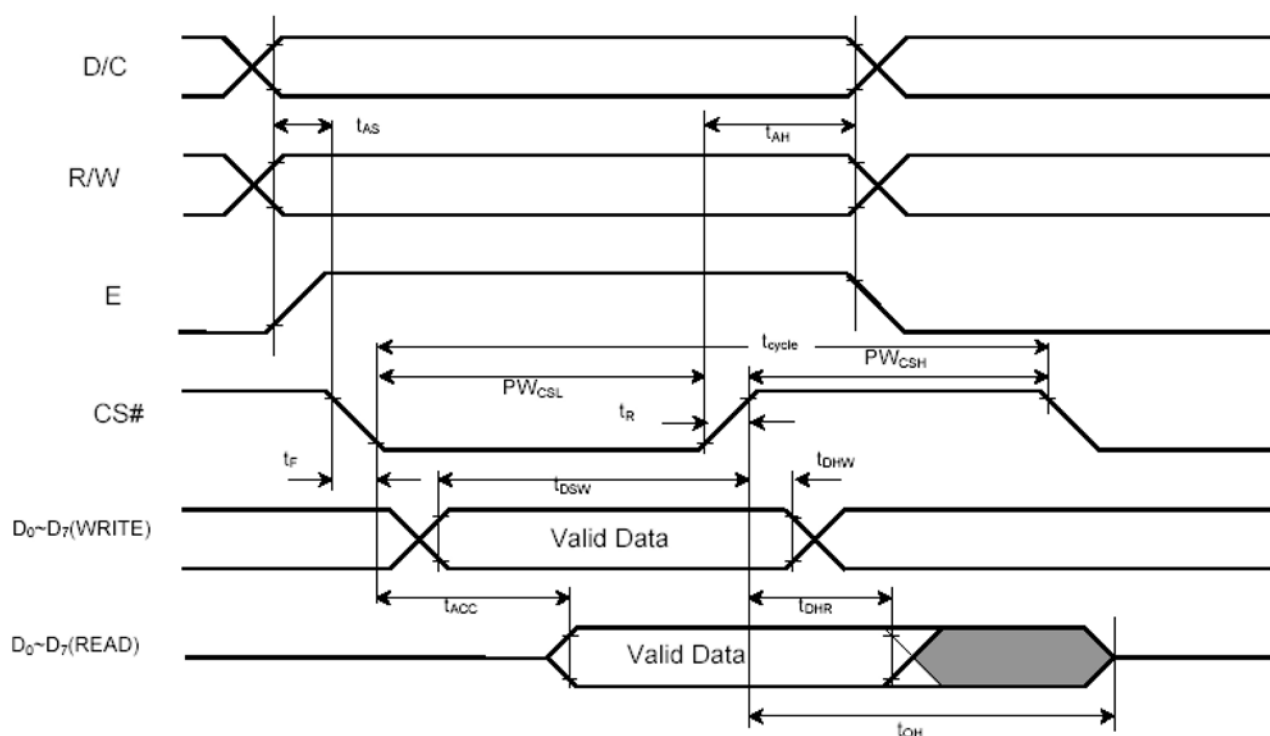
Note: Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

11. Timing Characteristics

6800-Series MPU Parallel Interface Timing Characteristics

(TA=25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

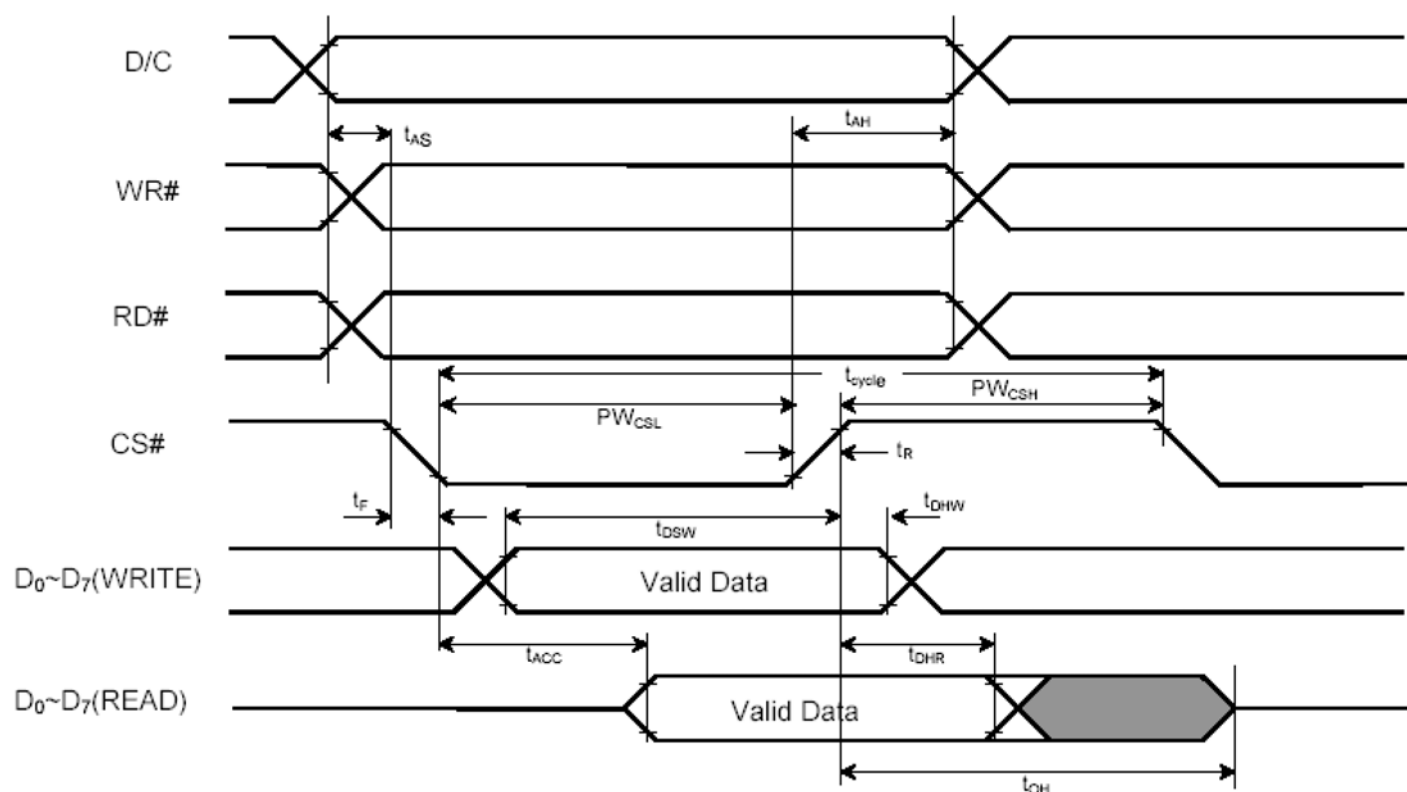


6800-series MPU parallel interface characteristics

8080-Series MPU Parallel Interface Timing Characteristics

(TA =25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

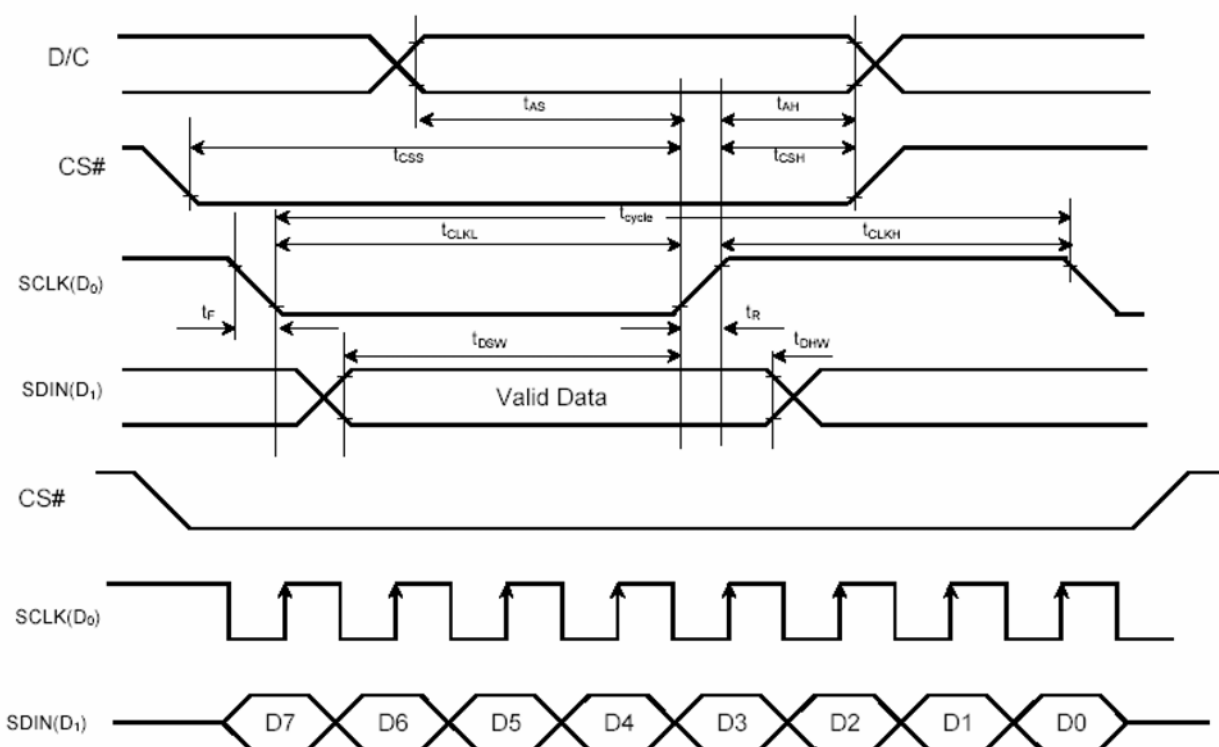


8080-series MPU parallel interface characteristics

Serial Interface Timing Characteristics

(TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



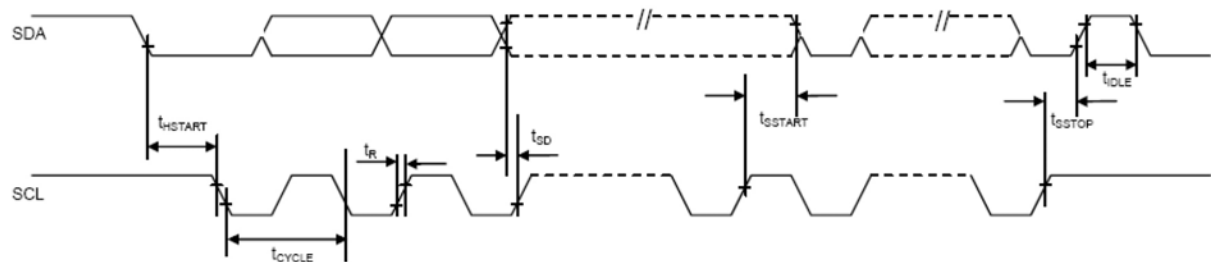
Serial interface characteristics

I²C Interface Timing Characteristics

(TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_{R}	Rise Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I²C Interface Timing Characteristics



12. OLED Lifetime

Conditions :

Temperature : 25°C

Brightness decay to 50% of original value

Panel lifetime is a function of the brightness as follows :

Average Brightness (cd/m²)	Lifetime (Hours)
80	10,000
40	20,000