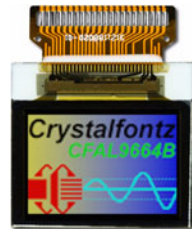




# CrystalFontz America, Incorporated

## GRAPHIC OLED MODULE SPECIFICATIONS



Shown actual size.

CrystalFontz Model Number	<b>CFAL9664B-F-B1</b>
Hardware Version	<b>Revision A</b>
Data Sheet Version	<b>Revision 1.1 July 2009</b>
Product Pages	<a href="http://www.crystalfontz.com/product/CFAL9664BFB1.html">http://www.crystalfontz.com/product/CFAL9664BFB1.html</a>

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## MAIN FEATURES

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### COMPARISON TO LCD (LIQUID CRYSTAL DISPLAY) MODULE

The CFAL9664B-F-B1 is a full color 96 x 64 dot matrix Organic Light-Emitting Diode (OLED) display module. The small size, ultra-thin form factor, and full color capability of the CFAL9664B-F-B1 makes it possible to use this OLED module in applications where it would be difficult or impossible to fit a traditional monochrome LCD module. The module's small size makes it possible to use the CFAL9664B-F-B1 in space constrained applications such as a status display on a disk drive or server blade. Because of the low power requirements, the CFAL9664B-F-B1 is suitable in battery powered portable devices such as remote controls and scientific meters (for example, temperature, sound, and gas detection). Full color allows information to be quickly perceived. For example, use red to indicate a fault and green to indicate normal operation.

Compared to most LCD modules, this OLED module has a quicker response time and an extremely wide viewing angle. At the low end of an STN LCD's temperature range, a module's contrast will typically be poor and the response time will be very slow. Unlike an STN LCD module, contrast does not diminish and response time is good at the lower end of an OLED module's operating temperature range, allowing it to operate in cold environments without a heater.

### FEATURES

- 96 (wide) x 3 (RGB) x 64 (high) OLED COG (Chip on Glass) with an FPC tail (Flexible Printed Circuit).
  - Panel is 24.8 (W) x 22.42 (H) x 1.42 (D) millimeters (.98" (W) x .88" (H) x .06" (D) inches).
  - Overall height (panel + FPC) is 30.42 millimeters (1.20").
- 8-bit parallel (8080 or 6800) or SPI Interface.
- Built-in Solomon Systech [SSD1332](#) Controller.
- 65K full color emissive display.
- Extremely wide viewing angle is >160°.
- Wide temperature range for operation is -20°C to +70°C.
- RoHS compliant.



## MODULE CLASSIFICATION INFORMATION

CFA L 96 64 B - F - B1  
 ① ② ③ ④ ⑤ ⑥ ⑦

①	Brand	CrystalFontz America, Inc.
②	Display Type	L – OLED
③	Number of Pixels (Width)	96 pixels
④	Number of Pixels (Height)	64 pixels
⑤	Model Identifier	B
⑥	Display Color	F – Full color
⑦	Special Code 1	B1 – Manufacturer’s codes

## MECHANICAL SPECIFICATIONS

---

### PHYSICAL CHARACTERISTICS

ITEM	SIZE
Number of pixels	96 (W) x 3 (RGB) x 64 pixels (H)
Panel Dimensions (excludes FPC Tail)	24.8 (W) x 22.42 (H) x 1.42 (D) mm
Overall Height Dimension (Panel + FPC Tail)	30.42 mm
Viewing Area	22.14 (W) x 15.42 (H) mm
Active Area	20.14 (W) x 13.42 (H) mm
Pixel Size	0.05 (W) x 0.19 (H) mm
Pixel Pitch	0.07 (W) x 0.21 (H) mm
Aperture Rate*	65%
Weight	1 gram (typical)
*Aperture rate is defined by dividing the effective display area with unit pixel area.	

























































## APPENDIX D: SOLOMON SYSTECH SSD1332 CONTROLLER SPECIFICATION SHEET

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The complete *Solomon Systech 96RGB x 64 Dot Matrix OLED/PLED Segment/Common Driver with Controller Data Sheet* (56 pages) follows.

**SSD1332**

***Advance Information***

**96RGB x 64 Dot Matrix  
OLED/PLED Segment/Common Driver with Controller**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

<http://www.solomon-systech.com>

**SSD1332**

Rev 2.3

P 1/56

Mar 2006

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## 1 GERENAL INFORMATIOM

The SSD1332 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 288 segments (96RGB) and 64 commons. This IC is designed for Common Cathode type OLED panel.

The SSD1332 displays data directly from its internal 96x64x16 bits Graphic Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800/8000 series compatible Parallel Interface or Serial Peripheral Interface. It has a 256 steps contrast control and 65K color control.

## 2 FEATURES

- Support max. 96RGB x 64 matrix panel
- Power supply:  $V_{DD} = 2.4V - 3.5V$   
 $V_{CC} = 7.0V - 18.0V$
- OLED driving output voltage, 16V maximum
- DC-DC voltage converter
- Segment maximum source current: 200uA
- Common maximum sink current: 50mA
- Embedded 96x64x16 bit SRAM display buffer
- 16 step master current control, and 256 step current control for the three color components
- Programmable Frame Rate
- Graphic Acceleration Command Set (GAC)
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature: -40 to 85 °C

## 3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1332U1R1	96RGB	64	COF	Page 47	<ul style="list-style-type: none"> <li>• 35mm film</li> <li>• 5 sprocket hole</li> <li>• 80 / 68 / SPI interface</li> <li>• SEG lead pitch 0.06mm</li> <li>• COM lead pitch 0.09mm</li> </ul>
SSD1332T1R1	96RGB	64	TAB	Page 51	<ul style="list-style-type: none"> <li>• 35mm film</li> <li>• 5 sprocket hole</li> <li>• Folding TAB</li> <li>• 80 / 68 / SPI interface</li> <li>• SEG lead pitch 0.06mm</li> <li>• COM lead pitch 0.09mm</li> </ul>
SSD1332Z	96RGB	64	COG	Page 8, 55	<ul style="list-style-type: none"> <li>• Min SEG pad pitch: 41.2 <math>\mu</math>m</li> <li>• Min COM pad pitch: 41.2 <math>\mu</math>m</li> </ul>

## 4 BLOCK DIAGRAM

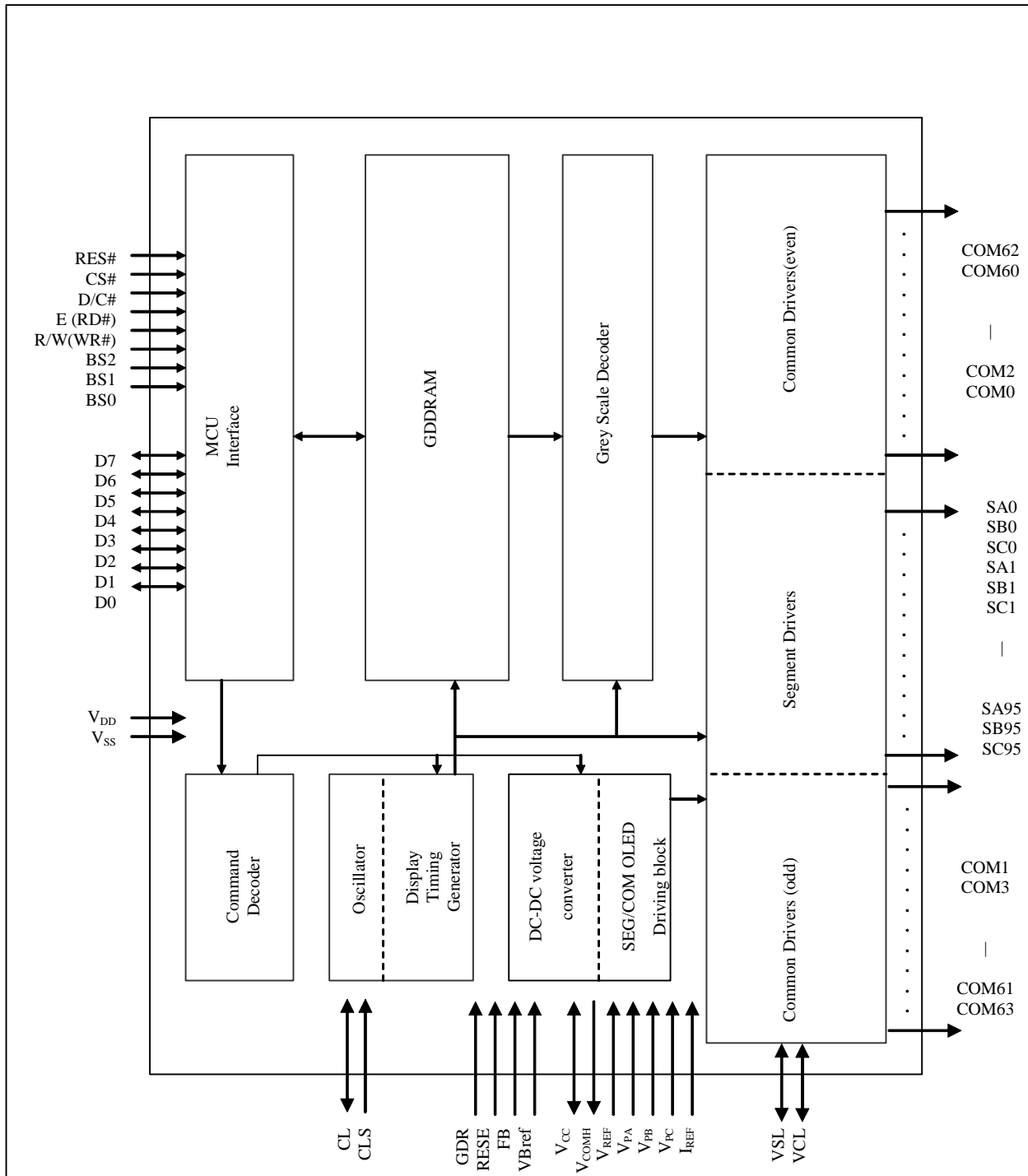
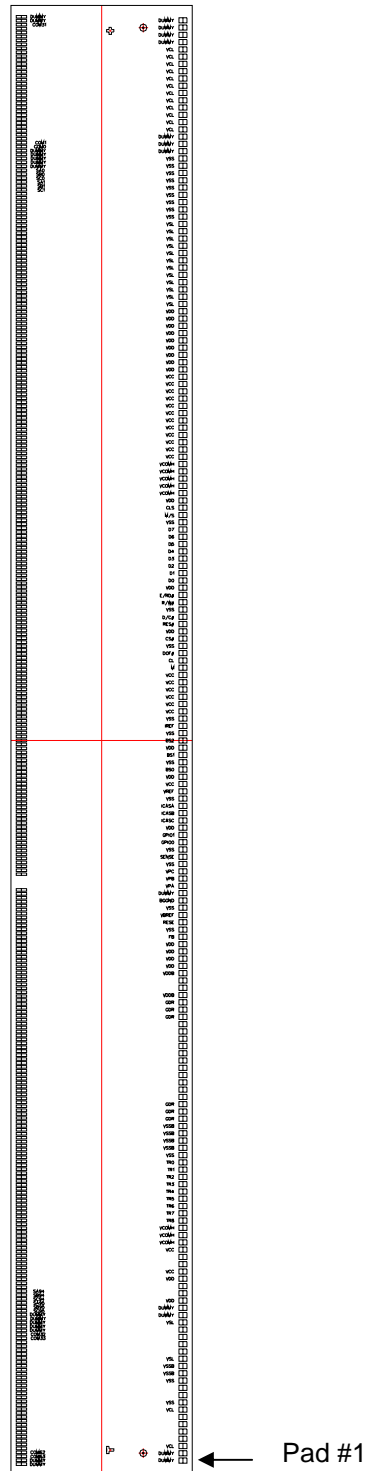


Figure 1 - Block Diagram

## 5 SSD1332Z GOLD BUMP DIE PAD ASSIGNMENT

Figure 2 – SSD1332Z Pin Assignment



+ represents the centre of the alignment mark

	X-pos ( $\mu\text{m}$ )	Y-pos ( $\mu\text{m}$ )
	-7433.6	-90.5
	7433.6	-90.5
	-7465.9	-437.4
	7465.9	-437.4

All alignment keys have size  
75  $\mu\text{m}$  x 75  $\mu\text{m}$

Die Size: 15.4mm x 1.9mm  
Die Thickness: 457 +/- 25  $\mu\text{m}$   
Min I/O pad pitch: 76.2  $\mu\text{m}$   
Min SEG pad pitch: 41.2  $\mu\text{m}$   
Min COM pad pitch: 41.2  $\mu\text{m}$   
Bump Height: Nominal 15  $\mu\text{m}$

**Table 2 - SSD1332Z Die Pad Coordinates**

Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis	Pad #	Pad Name	X-Axis	Y-Axis
1	DUMMY	-7543.8	-853	61	GDR	-2971.8	-853	121	VDD	1600.2	-853	181	DUMMY	6172.2	-853
2	DUMMY	-7467.6	-853	62	GDR	-2895.6	-853	122	D0	1676.4	-853	182	DUMMY	6248.4	-853
3	VCL	-7391.4	-853	63	GDR	-2819.4	-853	123	D1	1752.6	-853	183	DUMMY	6324.6	-853
4	VCL	-7315.2	-853	64	GDR	-2743.2	-853	124	D2	1828.8	-853	184	VCL	6400.8	-853
5	VCL	-7239	-853	65	VDD	-2667	-853	125	D3	1905	-853	185	VCL	6477	-853
6	VCL	-7162.8	-853	66	VDD	-2590.8	-853	126	D4	1981.2	-853	186	VCL	6553.2	-853
7	VCL	-7086.6	-853	67	VDD	-2514.6	-853	127	D5	2057.4	-853	187	VCL	6629.4	-853
8	VCL	-7010.4	-853	68	VDD	-2438.4	-853	128	D6	2133.6	-853	188	VCL	6705.6	-853
9	VSS	-6934.2	-853	69	VDD	-2362.2	-853	129	D7	2209.8	-853	189	VCL	6781.8	-853
10	VSS	-6858	-853	70	VDD	-2286	-853	130	VSS	2286	-853	190	VCL	6858	-853
11	VSS	-6781.8	-853	71	VDD	-2209.8	-853	131	M/S	2362.2	-853	191	VCL	6934.2	-853
12	VSS	-6705.6	-853	72	VDD	-2133.6	-853	132	CLS	2438.4	-853	192	VCL	7010.4	-853
13	VSSB	-6629.4	-853	73	FB	-2057.4	-853	133	VDD	2514.6	-853	193	VCL	7086.6	-853
14	VSSB	-6553.2	-853	74	VSS	-1981.2	-853	134	VCOMH	2590.8	-853	194	VCL	7162.8	-853
15	VSL	-6477	-853	75	RESE	-1905	-853	135	VCOMH	2667	-853	195	VCL	7239	-853
16	VSL	-6400.8	-853	76	VBREF	-1828.8	-853	136	VCOMH	2743.2	-853	196	DUMMY	7315.2	-853
17	VSL	-6324.6	-853	77	VSS	-1752.6	-853	137	VCOMH	2819.4	-853	197	DUMMY	7391.4	-853
18	VSL	-6248.4	-853	78	BGGND	-1676.4	-853	138	VCOMH	2895.6	-853	198	DUMMY	7467.6	-853
19	VSL	-6172.2	-853	79	DUMMY	-1600.2	-853	139	VCC	2971.8	-853	199	DUMMY	7543.8	-853
20	VSL	-6096	-853	80	VPA	-1524	-853	140	VCC	3048	-853	200	DUMMY	7580.8	840
21	DUMMY	-6019.8	-853	81	VPB	-1447.8	-853	141	VCC	3124.2	-853	201	DUMMY	7539.6	840
22	DUMMY	-5943.6	-853	82	VPC	-1371.6	-853	142	VCC	3200.4	-853	202	COM31	7498.4	840
23	VDD	-5867.4	-853	83	VSS	-1295.4	-853	143	VCC	3276.6	-853	203	COM30	7457.2	840
24	VDD	-5791.2	-853	84	SENSE	-1219.2	-853	144	VCC	3352.8	-853	204	COM29	7416	840
25	VDD	-5715	-853	85	VSS	-1143	-853	145	VCC	3429	-853	205	COM28	7374.8	840
26	VDD	-5638.8	-853	86	GPIO0	-1066.8	-853	146	VCC	3505.2	-853	206	COM27	7333.6	840
27	VCC	-5562.6	-853	87	GPIO1	-990.6	-853	147	VCC	3581.4	-853	207	COM26	7292.4	840
28	VCC	-5486.4	-853	88	VDD	-914.4	-853	148	VCC	3657.6	-853	208	COM25	7251.2	840
29	VCC	-5410.2	-853	89	ICASC	-838.2	-853	149	VCC	3733.8	-853	209	COM24	7210	840
30	VCC	-5334	-853	90	ICASB	-762	-853	150	VCC	3810	-853	210	COM23	7168.8	840
31	VCOMH	-5257.8	-853	91	ICASA	-685.8	-853	151	VDD	3886.2	-853	211	COM22	7127.6	840
32	VCOMH	-5181.6	-853	92	VSS	-609.6	-853	152	VDD	3962.4	-853	212	COM21	7086.4	840
33	VCOMH	-5105.4	-853	93	VREF	-533.4	-853	153	VDD	4038.6	-853	213	COM20	7045.2	840
34	TR8	-5029.2	-853	94	VCC	-457.2	-853	154	VDD	4114.8	-853	214	COM19	7004	840
35	TR7	-4953	-853	95	VDD	-381	-853	155	VDD	4191	-853	215	COM18	6962.8	840
36	TR6	-4876.8	-853	96	BS0	-304.8	-853	156	VDD	4267.2	-853	216	COM17	6921.6	840
37	TR5	-4800.6	-853	97	VSS	-228.6	-853	157	VDD	4343.4	-853	217	COM16	6880.4	840
38	TR4	-4724.4	-853	98	BS1	-152.4	-853	158	VDD	4419.6	-853	218	COM15	6839.2	840
39	TR3	-4648.2	-853	99	VDD	-76.2	-853	159	VDD	4495.8	-853	219	COM14	6798	840
40	TR2	-4572	-853	100	BS2	0	-853	160	VSL	4572	-853	220	COM13	6756.8	840
41	TR1	-4495.8	-853	101	VSS	76.2	-853	161	VSL	4648.2	-853	221	COM12	6715.6	840
42	TR0	-4419.6	-853	102	IREF	152.4	-853	162	VSL	4724.4	-853	222	COM11	6674.4	840
43	VSS	-4343.4	-853	103	VSS	228.6	-853	163	VSL	4800.6	-853	223	COM10	6633.2	840
44	VSSB	-4267.2	-853	104	VCC	304.8	-853	164	VSL	4876.8	-853	224	COM9	6592	840
45	VSSB	-4191	-853	105	VCC	381	-853	165	VSL	4953	-853	225	COM8	6550.8	840
46	VSSB	-4114.8	-853	106	VCC	457.2	-853	166	VSL	5029.2	-853	226	COM7	6509.6	840
47	VSSB	-4038.6	-853	107	VCC	533.4	-853	167	VSL	5105.4	-853	227	COM6	6468.4	840
48	GDR	-3962.4	-853	108	VCC	609.6	-853	168	VSL	5181.6	-853	228	COM5	6427.2	840
49	GDR	-3886.2	-853	109	VCC	685.8	-853	169	VSL	5257.8	-853	229	COM4	6386	840
50	GDR	-3810	-853	110	M	762	-853	170	VSL	5334	-853	230	COM3	6344.8	840
51	GDR	-3733.8	-853	111	CL	838.2	-853	171	VSL	5410.2	-853	231	COM2	6303.6	840
52	GDR	-3657.6	-853	112	DOF#	914.4	-853	172	VSS	5486.4	-853	232	COM1	6262.4	840
53	GDR	-3581.4	-853	113	VSS	990.6	-853	173	VSS	5562.6	-853	233	COM0	6221.2	840
54	GDR	-3505.2	-853	114	CS#	1066.8	-853	174	VSS	5638.8	-853	234	DUMMY	6180	840
55	GDR	-3429	-853	115	VDD	1143	-853	175	VSS	5715	-853	235	DUMMY	6138.8	840
56	GDR	-3352.8	-853	116	RES#	1219.2	-853	176	VSS	5791.2	-853	236	DUMMY	6097.6	840
57	GDR	-3276.6	-853	117	D/C#	1295.4	-853	177	VSS	5867.4	-853	237	DUMMY	6056.4	840
58	GDR	-3200.4	-853	118	VSS	1371.6	-853	178	VSS	5943.6	-853	238	DUMMY	6015.2	840
59	GDR	-3124.2	-853	119	R/W#	1447.8	-853	179	VSS	6019.8	-853	239	SA0	5974	840
60	GDR	-3048	-853	120	E/RD#	1524	-853	180	VSS	6096	-853	240	SB0	5932.8	840

Pad #	Pad Name	X-Axis	Y-Axis
241	SC0	5891.6	840
242	SA1	5850.4	840
243	SB1	5809.2	840
244	SC1	5768	840
245	SA2	5726.8	840
246	SB2	5685.6	840
247	SC2	5644.4	840
248	SA3	5603.2	840
249	SB3	5562	840
250	SC3	5520.8	840
251	SA4	5479.6	840
252	SB4	5438.4	840
253	SC4	5397.2	840
254	SA5	5356	840
255	SB5	5314.8	840
256	SC5	5273.6	840
257	SA6	5232.4	840
258	SB6	5191.2	840
259	SC6	5150	840
260	SA7	5108.8	840
261	SB7	5067.6	840
262	SC7	5026.4	840
263	SA8	4985.2	840
264	SB8	4944	840
265	SC8	4902.8	840
266	SA9	4861.6	840
267	SB9	4820.4	840
268	SC9	4779.2	840
269	SA10	4738	840
270	SB10	4696.8	840
271	SC10	4655.6	840
272	SA11	4614.4	840
273	SB11	4573.2	840
274	SC11	4532	840
275	SA12	4490.8	840
276	SB12	4449.6	840
277	SC12	4408.4	840
278	SA13	4367.2	840
279	SB13	4326	840
280	SC13	4284.8	840
281	SA14	4243.6	840
282	SB14	4202.4	840
283	SC14	4161.2	840
284	SA15	4120	840
285	SB15	4078.8	840
286	SC15	4037.6	840
287	SA16	3996.4	840
288	SB16	3955.2	840
289	SC16	3914	840
290	SA17	3872.8	840
291	SB17	3831.6	840
292	SC17	3790.4	840
293	SA18	3749.2	840
294	SB18	3708	840
295	SC18	3666.8	840
296	SA19	3625.6	840
297	SB19	3584.4	840
298	SC19	3543.2	840
299	SA20	3502	840
300	SB20	3460.8	840

Pad #	Pad Name	X-Axis	Y-Axis
301	SC20	3419.6	840
302	SA21	3378.4	840
303	SB21	3337.2	840
304	SC21	3296	840
305	SA22	3254.8	840
306	SB22	3213.6	840
307	SC22	3172.4	840
308	SA23	3131.2	840
309	SB23	3090	840
310	SC23	3048.8	840
311	SA24	3007.6	840
312	SB24	2966.4	840
313	SC24	2925.2	840
314	SA25	2884	840
315	SB25	2842.8	840
316	SC25	2801.6	840
317	SA26	2760.4	840
318	SB26	2719.2	840
319	SC26	2678	840
320	SA27	2636.8	840
321	SB27	2595.6	840
322	SC27	2554.4	840
323	SA28	2513.2	840
324	SB28	2472	840
325	SC28	2430.8	840
326	SA29	2389.6	840
327	SB29	2348.4	840
328	SC29	2307.2	840
329	SA30	2266	840
330	SB30	2224.8	840
331	SC30	2183.6	840
332	SA31	2142.4	840
333	SB31	2101.2	840
334	SC31	2060	840
335	SA32	2018.8	840
336	SB32	1977.6	840
337	SC32	1936.4	840
338	SA33	1895.2	840
339	SB33	1854	840
340	SC33	1812.8	840
341	SA34	1771.6	840
342	SB34	1730.4	840
343	SC34	1689.2	840
344	SA35	1648	840
345	SB35	1606.8	840
346	SC35	1565.6	840
347	SA36	1524.4	840
348	SB36	1483.2	840
349	SC36	1442	840
350	SA37	1400.8	840
351	SB37	1359.6	840
352	SC37	1318.4	840
353	SA38	1277.2	840
354	SB38	1236	840
355	SC38	1194.8	840
356	SA39	1153.6	840
357	SB39	1112.4	840
358	SC39	1071.2	840
359	SA40	1030	840
360	SB40	988.8	840

Pad #	Pad Name	X-Axis	Y-Axis
361	SC40	947.6	840
362	SA41	906.4	840
363	SB41	865.2	840
364	SC41	824	840
365	SA42	782.8	840
366	SB42	741.6	840
367	SC42	700.4	840
368	SA43	659.2	840
369	SB43	618	840
370	SC43	576.8	840
371	SA44	535.6	840
372	SB44	494.4	840
373	SC44	453.2	840
374	SA45	412	840
375	SB45	370.8	840
376	SC45	329.6	840
377	SA46	288.4	840
378	SB46	247.2	840
379	SC46	206	840
380	SA47	164.8	840
381	SB47	123.6	840
382	SC47	82.4	840
383	SA48	41.2	840
384	SB48	0	840
385	SC48	-41.2	840
386	SA49	-82.4	840
387	SB49	-123.6	840
388	SC49	-164.8	840
389	SA50	-206	840
390	SB50	-247.2	840
391	SC50	-288.4	840
392	SA51	-329.6	840
393	SB51	-370.8	840
394	SC51	-412	840
395	SA52	-453.2	840
396	SB52	-494.4	840
397	SC52	-535.6	840
398	SA53	-576.8	840
399	SB53	-618	840
400	SC53	-659.2	840
401	SA54	-700.4	840
402	SB54	-741.6	840
403	SC54	-782.8	840
404	SA55	-824	840
405	SB55	-865.2	840
406	SC55	-906.4	840
407	SA56	-947.6	840
408	SB56	-988.8	840
409	SC56	-1030	840
410	SA57	-1071.2	840
411	SB57	-1112.4	840
412	SC57	-1153.6	840
413	SA58	-1194.8	840
414	SB58	-1236	840
415	SC58	-1277.2	840
416	SA59	-1318.4	840
417	SB59	-1359.6	840
418	SC59	-1400.8	840
419	SA60	-1565.6	840
420	SB60	-1606.8	840

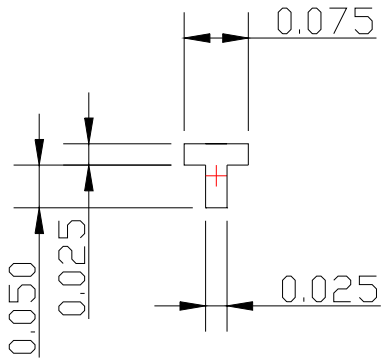
Pad #	Pad Name	X-Axis	Y-Axis
421	SC60	-1648	840
422	SA61	-1689.2	840
423	SB61	-1730.4	840
424	SC61	-1771.6	840
425	SA62	-1812.8	840
426	SB62	-1854	840
427	SC62	-1895.2	840
428	SA63	-1936.4	840
429	SB63	-1977.6	840
430	SC63	-2018.8	840
431	SA64	-2060	840
432	SB64	-2101.2	840
433	SC64	-2142.4	840
434	SA65	-2183.6	840
435	SB65	-2224.8	840
436	SC65	-2266	840
437	SA66	-2307.2	840
438	SB66	-2348.4	840
439	SC66	-2389.6	840
440	SA67	-2430.8	840
441	SB67	-2472	840
442	SC67	-2513.2	840
443	SA68	-2554.4	840
444	SB68	-2595.6	840
445	SC68	-2636.8	840
446	SA69	-2678	840
447	SB69	-2719.2	840
448	SC69	-2760.4	840
449	SA70	-2801.6	840
450	SB70	-2842.8	840
451	SC70	-2884	840
452	SA71	-2925.2	840
453	SB71	-2966.4	840
454	SC71	-3007.6	840
455	SA72	-3048.8	840
456	SB72	-3090	840
457	SC72	-3131.2	840
458	SA73	-3172.4	840
459	SB73	-3213.6	840
460	SC73	-3254.8	840
461	SA74	-3296	840
462	SB74	-3337.2	840
463	SC74	-3378.4	840
464	SA75	-3419.6	840
465	SB75	-3460.8	840
466	SC75	-3502	840
467	SA76	-3543.2	840
468	SB76	-3584.4	840
469	SC76	-3625.6	840
470	SA77	-3666.8	840
471	SB77	-3708	840
472	SC77	-3749.2	840
473	SA78	-3790.4	840
474	SB78	-3831.6	840
475	SC78	-3872.8	840
476	SA79	-3914	840
477	SB79	-3955.2	840
478	SC79	-3996.4	840
479	SA80	-4037.6	840
480	SB80	-4078.8	840

Pad #	Pad Name	X-Axis	Y-Axis
481	SC80	-4120	840
482	SA81	-4161.2	840
483	SB81	-4202.4	840
484	SC81	-4243.6	840
485	SA82	-4284.8	840
486	SB82	-4326	840
487	SC82	-4367.2	840
488	SA83	-4408.4	840
489	SB83	-4449.6	840
490	SC83	-4490.8	840
491	SA84	-4532	840
492	SB84	-4573.2	840
493	SC84	-4614.4	840
494	SA85	-4655.6	840
495	SB85	-4696.8	840
496	SC85	-4738	840
497	SA86	-4779.2	840
498	SB86	-4820.4	840
499	SC86	-4861.6	840
500	SA87	-4902.8	840
501	SB87	-4944	840
502	SC87	-4985.2	840
503	SA88	-5026.4	840
504	SB88	-5067.6	840
505	SC88	-5108.8	840
506	SA89	-5150	840
507	SB89	-5191.2	840
508	SC89	-5232.4	840
509	SA90	-5273.6	840
510	SB90	-5314.8	840
511	SC90	-5356	840
512	SA91	-5397.2	840
513	SB91	-5438.4	840
514	SC91	-5479.6	840
515	SA92	-5520.8	840
516	SB92	-5562	840
517	SC92	-5603.2	840
518	SA93	-5644.4	840
519	SB93	-5685.6	840
520	SC93	-5726.8	840
521	SA94	-5768	840
522	SB94	-5809.2	840
523	SC94	-5850.4	840
524	SA95	-5891.6	840
525	SB95	-5932.8	840
526	SC95	-5974	840
527	DUMMY	-6015.2	840
528	DUMMY	-6056.4	840
529	DUMMY	-6097.6	840
530	DUMMY	-6138.8	840
531	DUMMY	-6180	840
532	COM32	-6221.2	840
533	COM33	-6262.4	840
534	COM34	-6303.6	840
535	COM35	-6344.8	840
536	COM36	-6386	840
537	COM37	-6427.2	840
538	COM38	-6468.4	840
539	COM39	-6509.6	840
540	COM40	-6550.8	840

Pad #	Pad Name	X-Axis	Y-Axis
541	COM41	-6592	840
542	COM42	-6633.2	840
543	COM43	-6674.4	840
544	COM44	-6715.6	840
545	COM45	-6756.8	840
546	COM46	-6798	840
547	COM47	-6839.2	840
548	COM48	-6880.4	840
549	COM49	-6921.6	840
550	COM50	-6962.8	840
551	COM51	-7004	840
552	COM52	-7045.2	840
553	COM53	-7086.4	840
554	COM54	-7127.6	840
555	COM55	-7168.8	840
556	COM56	-7210	840
557	COM57	-7251.2	840
558	COM58	-7292.4	840
559	COM59	-7333.6	840
560	COM60	-7374.8	840
561	COM61	-7416	840
562	COM62	-7457.2	840
563	COM63	-7498.4	840
564	DUMMY	-7539.6	840
565	DUMMY	-7580.8	840

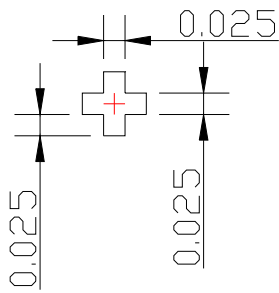
	Width (um)	Length (um)
Die Size (after saw)	15400	1900
Top Side	27	110
Bottom side	54	84

Figure 3 - SSD1332Z Alignment mark dimensions



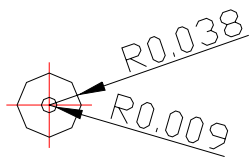
T shape

Detail T



+ shape

Detail +



Circle

Detail □

Scale: 10:1

Unit in um

## 6 PIN DESCRIPTION

### BS0, BS1, BS2

These input pins are used to configure MCU interface selection by appropriate logic setting, which is described in the following table:

**Table 3 – MCU Interface Selection Setting**

	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS0	0	0	0
BS1	0	1	0
BS2	1	1	0

### CS#

This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.

### RES#

This pin is reset signal input. When the pin is low, initialization of the chip is executed.

### D/C

This pin is Data/Command control pin. When the pin is pulled high, the data at D<sub>7</sub>-D<sub>0</sub> is treated as display data. When the pin is pulled low, the data at D<sub>7</sub>-D<sub>0</sub> will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.

### R/W(WR#)

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the chip is selected.

When serial interface is selected, this pin E(RD#) must be connected to VSS.

### E (RD#)

This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the chip is selected.

When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and the chip is selected.

When serial interface is selected, this pin E(RD#) must be connected to VSS.

### D<sub>7</sub>-D<sub>0</sub>

These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.

### V<sub>DD</sub>

Power Supply pin for logic operation of the driver. It must be connected to external source.

**V<sub>SS</sub>**

Ground pin. It must be connected to external ground.

**V<sub>CC</sub>**

This is the most positive voltage supply pin of the chip. It is supplied either by external high voltage source or internal booster

**V<sub>REF</sub>**

This pin is the reference for OLED driving voltages like V<sub>PA</sub>, V<sub>PB</sub>, V<sub>PC</sub> and V<sub>COMH</sub>. The relation between V<sub>REF</sub> and those driving voltages can be programmed and please refer to section "Command Table" for details. V<sub>REF</sub> can be either supplied externally or connected to V<sub>CC</sub>.

**V<sub>PA</sub>, V<sub>PB</sub>, V<sub>PC</sub>**

These pins are the pre-charge driving voltages for OLED driving segment pins SA0-SA95, SB0-SB95 and SC0-SC95 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, V<sub>PA</sub>, V<sub>PB</sub>, V<sub>PC</sub> pins should be left open.

**I<sub>REF</sub>**

This pin is the segment output current reference pin. I<sub>SEG</sub> is derived from I<sub>REF</sub>

$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor},$$

in which the contrast is set by command and the scale factor = 1 ~ 16.

A resistor should be connected between this pin and V<sub>SS</sub> to maintain the current around 10uA. Please refer to section 6 "Current and Voltage Supply" for the formula of resistor value from I<sub>REF</sub>.

**V<sub>COMH</sub>**

A capacitor, with recommended value 4.7uF, should be connected between this pin and V<sub>SS</sub>. No external power supply is allowed to connect to this pin.

**V<sub>DDB</sub>**

This is the power supply pin for the internal buffer of the DC-DC voltage converter.  $3.5V \geq V_{DDB} \geq V_{DD}$ .

**V<sub>SSB</sub>**

This is the GND pin for the internal buffer of the DC-DC voltage converter. It must be connected to V<sub>SS</sub>.

**GDR**

This output pin drives the gate of the external NMOS of the booster circuit. Please refer to the DC-DC voltage converter section for connection details.

**RESE**

This pin connects to the source current pin of the external NMOS of the booster circuit. Please refer to the DC-DC voltage converter section for connection details.

**V<sub>BREF</sub>**

This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typically 1uF, should be connected between V<sub>BREF</sub> and V<sub>SS</sub>.

**FB**

This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level ( $V_{cc}$ ). Please refer to the DC-DC voltage converter section for connection details.

#### **VSL**

This is segment voltage reference pin. This pin should be left open.

#### **VCL**

This is common voltage reference pin. This pin should be connected to VSS externally.

#### **TR0-TR8**

These are testing reserved pins. Keep NC.

#### **COM0-COM63**

These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is off.

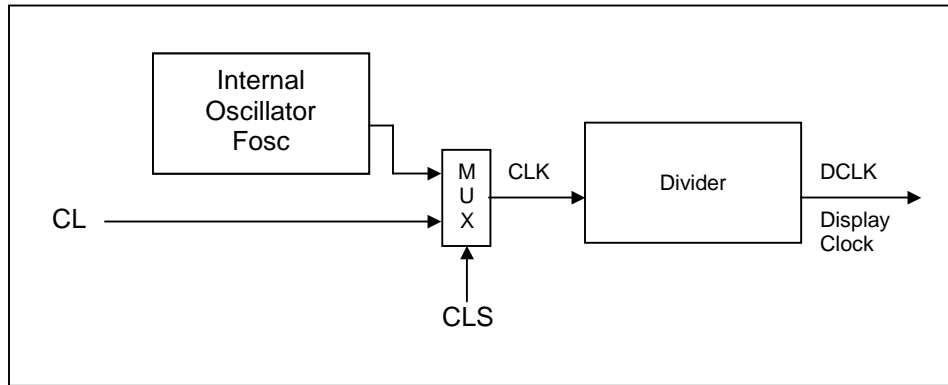
#### **SA0-SA95, SB0-SB95, SC0-SC95**

These pins provide the OLED segment driving signals. These pins are in high impedance state when display is off.

The 288 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.

## 7 FUNCTIONAL BLOCK DESCRIPTIONS

### Oscillator Circuit and Display Time Generator



**Figure 4 - Oscillator Circuit**

This module is an On-Chip low power RC oscillator circuitry (Figure 4). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is high, internal oscillator is selected. If CLS pin is low, external clock from CL pin will be used for CLK. The frequency of internal oscillator Fosc can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor can be programmed from 1 to 16 by command B3h.

#### Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 64 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Master contrast control register is set at 0Fh
9. Individual contrast control registers of color A, B, and C are set at 80h

#### Command Decoder and Command Interface

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is high, data is written to Graphic Display Data RAM (GDDRAM). If it is low, the input at D<sub>0</sub>-D<sub>7</sub> is interpreted as a Command and it will be decoded and be written to the corresponding command register.

## Current and Voltage Supply

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

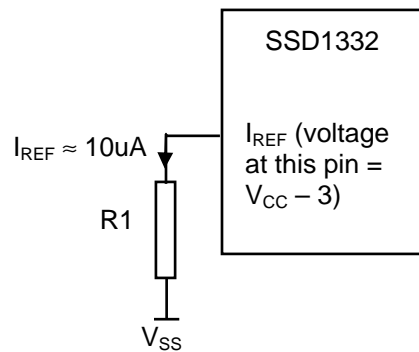
- $V_{CC}$  are most positive voltage supply. It can be supplied externally or from internal DC-DC converter.
- $V_{DD}$  are external power supply for logic operation of the driver.
- $V_{REF}$  is reference voltage, which is used to derive driving voltage for segments and commons like  $V_{PA}$ ,  $V_{PB}$ ,  $V_{PC}$  and  $V_{COMH}$ . Normally,  $V_{REF}$  is connected to  $V_{CC}$ . Please refer to the command table for the relationships of  $V_{REF}$  to the segments and commons voltages.
- $I_{REF}$  is a reference current source for segment current drivers  $I_{SEG}$ . The relationship between reference current and segment current of a color is:

$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor}$$

in which the contrast (0~255) is set by Set Contrast command,  
and the scale factor (1 ~ 16) is set by Master Current Control command.

For example, in order to achieve  $I_{SEG} = 160\mu\text{A}$  at maximum contrast 255,  $I_{REF}$  is set to around  $10\mu\text{A}$ . This current value is obtained by connecting an appropriate resistor from  $I_{REF}$  pin to  $V_{SS}$  as shown in Figure 5.

Recommended range for  $I_{REF} = 8 - 12\mu\text{A}$



**Figure 5 –  $I_{REF}$  Current Setting by Resistor Value**

Since the voltage at  $I_{REF}$  pin is  $V_{CC} - 3\text{V}$ , the value of resistor  $R1$  can be found as below.  
 $R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} = (V_{CC} - 3) / 10\mu\text{A} \approx 910\text{k}\Omega$  for  $V_{CC} = 12\text{V}$ .

### Segment Drivers/Common Drivers

Segment drivers consists of 288 (96 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps by contrast setting command. Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

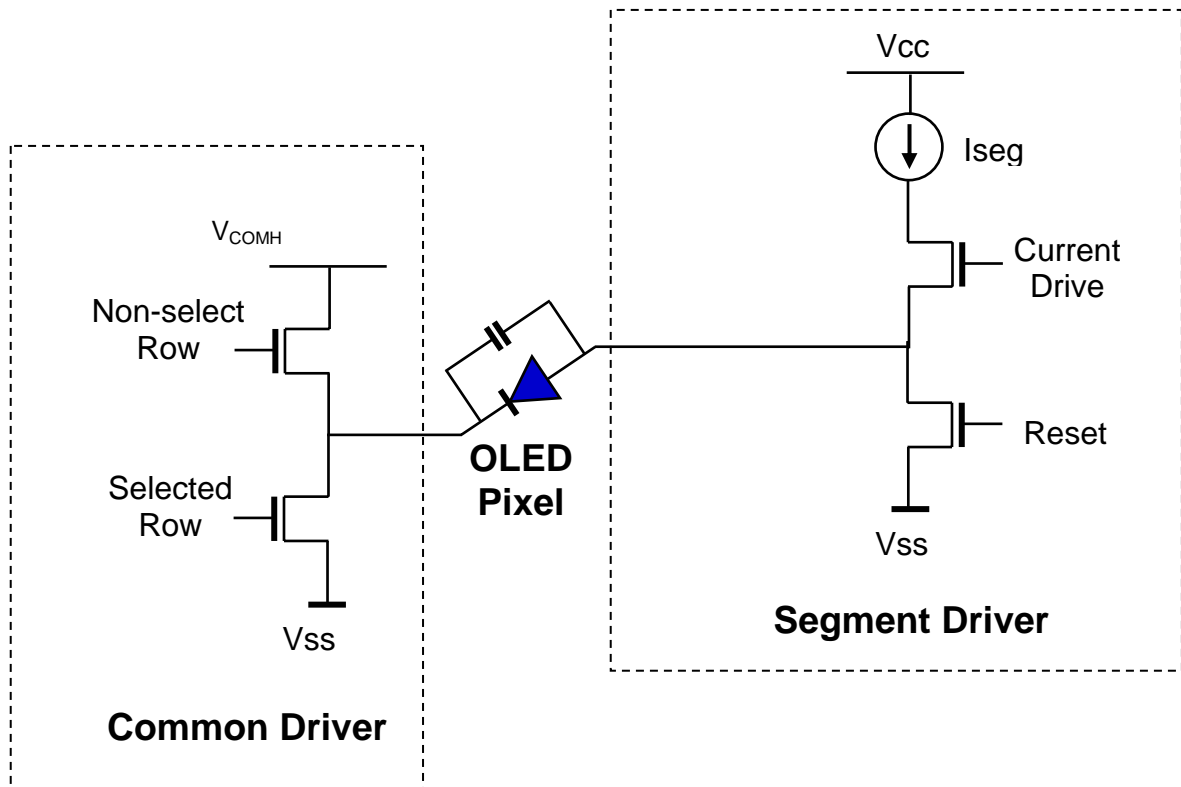


Figure 6 – Segment and Common Driver Block Diagram

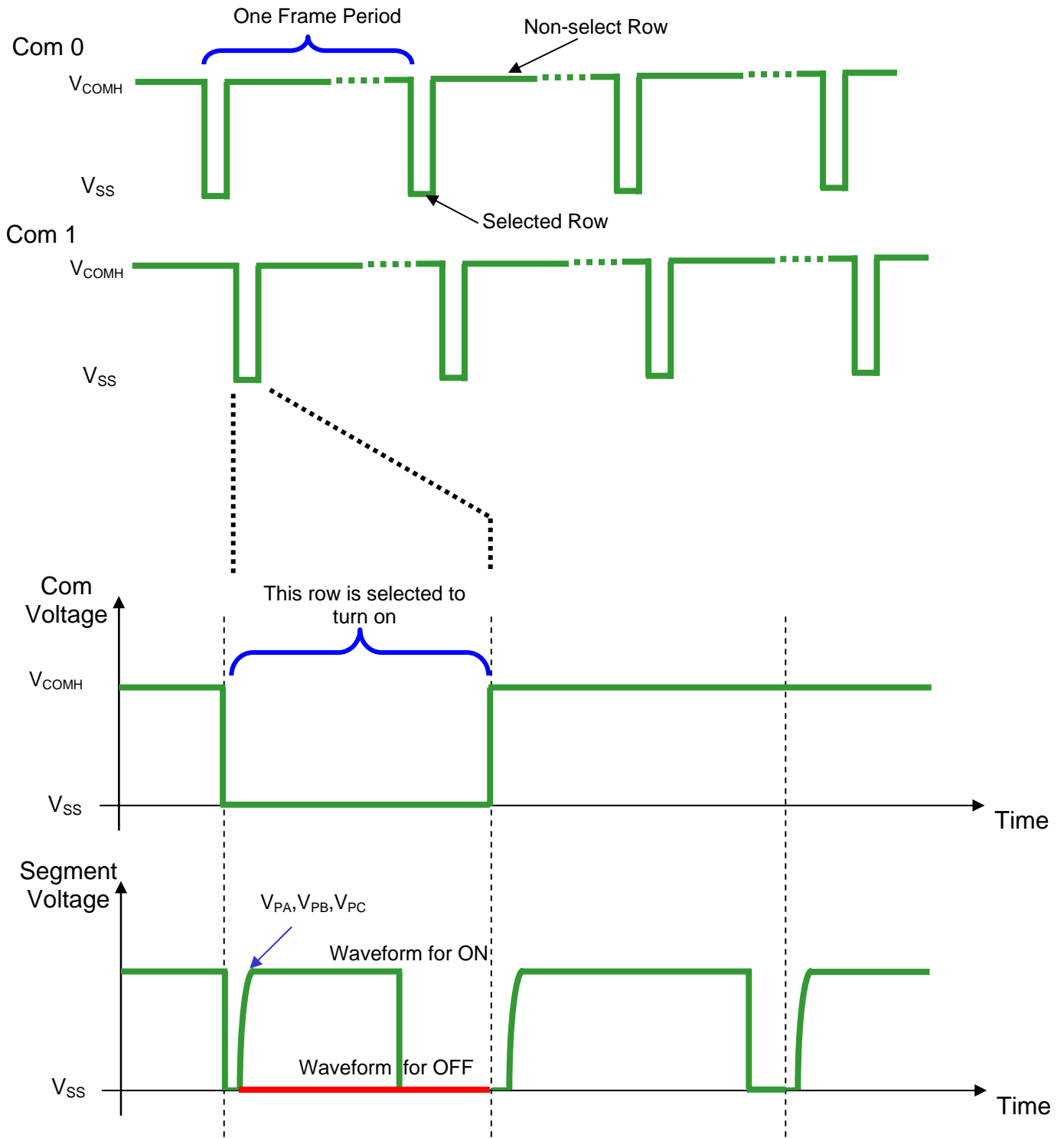


Figure 7 – Segment and Common Driver Signal Waveform

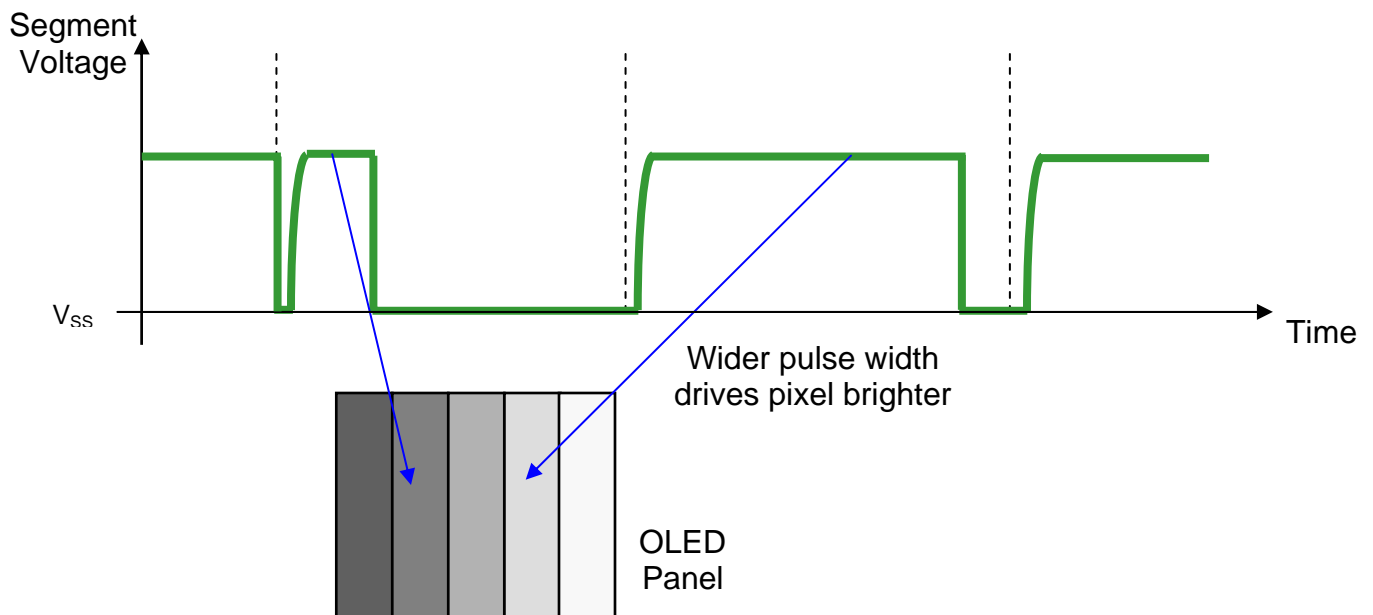
The commons are scanned sequentially one by one row. If the row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage  $V_{COMH}$ .

In the scanned row, the pixels on the row will be turned on or off by sending the corresponding data signal to the segment pins. If the pixel is turned off, the segment current is kept at 0. On the other hand, the segment drives to  $I_{SEG}$  when the pixel is turned on.

There are three phases to driving a OLED a pixel. In phase 1, the pixel is reset by the segment driver to  $V_{SS}$  in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, the pixel is charged up by the segment driver to the desired voltage levels  $V_{PA}$ ,  $V_{PB}$  or  $V_{PC}$  for color A, B or C respectively. The period of phase 2 can be programmed by command B1h from 1 to 16 DCLK. An OLED panel with larger capacitance requires a longer period for charging up.

Last phase is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The wider pulse widths in the current drive stage results in brighter pixels and vice versa. This is shown in the following figure.



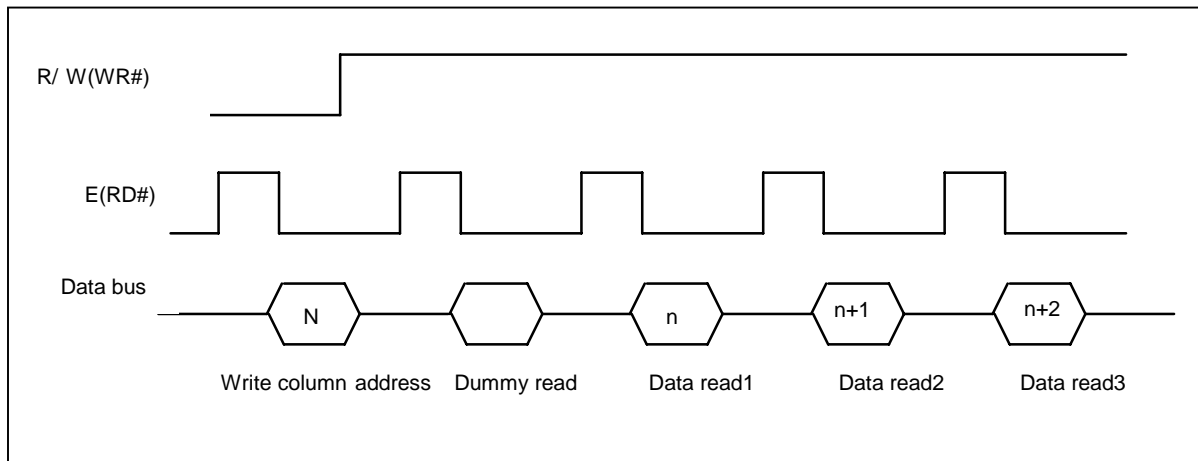
**Figure 8 – Gray Scale Control by PWM in Segment**

The pulse width in current drive stage to control brightness can be programmed through “Set Gray Scale Table” command. It is described in more detailed in “Command Descriptions” section.

### MPU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins ( $D_0$ - $D_7$ ), R/W(WR#), D/C, E (RD#) and CS#. R/W(WR#) High Input indicates a read operation from the Graphic Display Data RAM (GDDRAM) or the status register. R/W(WR#) Low Input indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/C input. The E(RD#) input serves as data latch signal (clock) when high provided that CS# is low. Refer to Figure 27 of parallel timing characteristics for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 9 below.



**Figure 9 - Display data read back procedure - insertion of dummy read**

### MPU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins ( $D_0$ - $D_7$ ), E (RD#), R/W(WR#), D/C and CS#. The E(RD#) input serves as data read latch signal (clock) when low, provided that CS# is low. Display data RAM or status register read is controlled by D/C#.

R/W(WR#) input serves as data write latch signal (clock) when low provided that CS# is low, or CS# input serves as data write latch signal at rising edge when R/W(WR#) is low. Display data RAM or command register write is controlled by D/C. Refer to Figure 28 of parallel timing characteristics for Parallel Interface Timing Diagram of 8080-series microprocessor. Similar to 6800-series interface, a dummy read is also required before the first actual display data read.

### MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. D3 to D7, E and R/W pins can be connected to external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM or command register in the same clock.

### Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The size of the RAM is 96 x 64 x 16bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 16-bit data. Three sub-pixels for color A, B and C have 6 bits, 5 bits and 6 bits respectively. The arrangement of data pixel in graphic display data RAM is shown below.

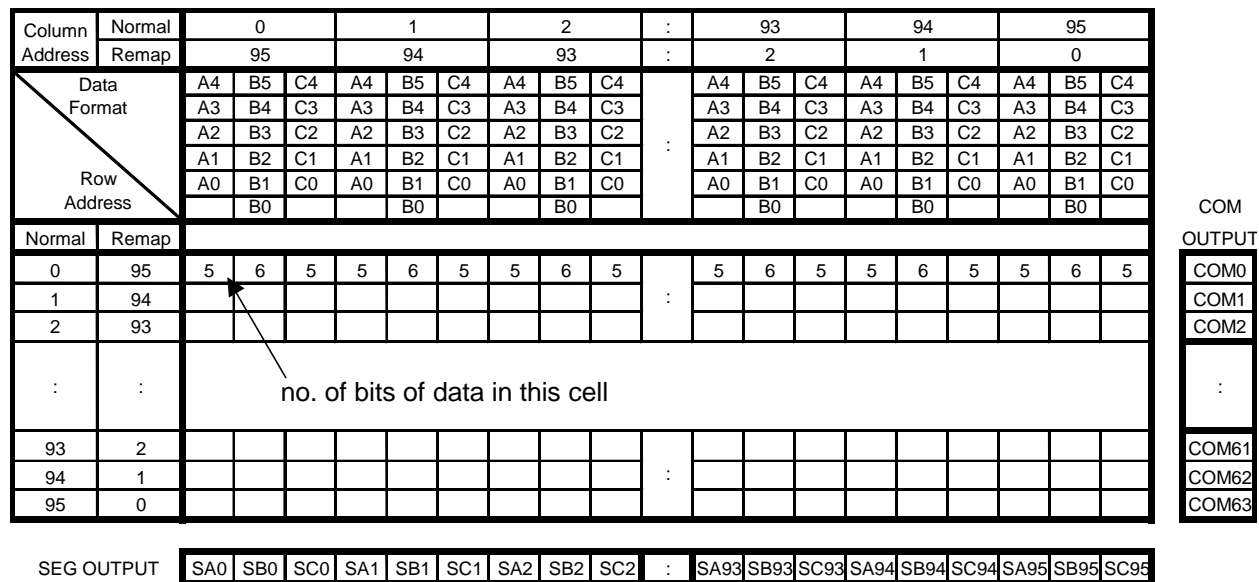


Figure 10 – 65k Color Depth Graphic Display Data RAM Structure

The sequence of sending one pixel of 16-bit data is divided into two 8-bit sessions as shown below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 <sup>st</sup> byte	C4	C3	C2	C1	C0	B5	B4	B3
2 <sup>nd</sup> byte	B2	B1	B0	A4	A3	A2	A1	A0

Figure 11 – 65k Color Depth Graphic Display Data Writing Sequence

In 256-color mode, each pixel is composed of 8-bit. Color A uses 2-bit while color B and color C each is represented by 3-bit. Although only 8 bits are required to represent one pixel, each pixel occupies 16-bit space inside graphic display data RAM with format as follows.

For 256-color mode, one pixel data is sent in a 8-bit session like below.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 <sup>st</sup> byte	C2	C1	C0	B2	B1	B0	A1	A0

Figure 11 – 256 Color Depth Graphic Display Data Writing Sequence

Color C (3 bits)	RAM Content (5 bits)	Color B (3 bits)	RAM Content (6 bits)	Color A (2 bits)	RAM Content (5 bits)
000	00000	000	000000	00	00000
001	00100	001	001000	01	01000
010	01000	010	010000	10	10100
011	01100	011	011000	11	11100
100	10010	100	100100		
101	10110	101	101100		
110	11010	110	110100		
111	11110	111	111100		

**Figure 12 – 256 Color Depth Graphic Display Data RAM Structure for One Pixel**

### Gray Scale and Gray Scale Table

The gray scale display is produced by controlling the current pulse widths from the segment driver in the current drive phase. The gray scale table stores the corresponding pulse widths (PW0 ~ PW63) of the 64 gray scale levels (GS0~GS63). The wider the pulse width, the brighter the pixel will be. This single gray scale table supports all the three colors A, B and C. The pulse widths are entered by software commands.

As shown in figure 13, color B sub-pixel RAM data has 6 bits, represent the 64 gray scale levels from GS0 to GS63. color A and color C sub-pixel RAM data has only 5 bits, represent 32 gray scale levels from GS0, GS2, ..., GS62.

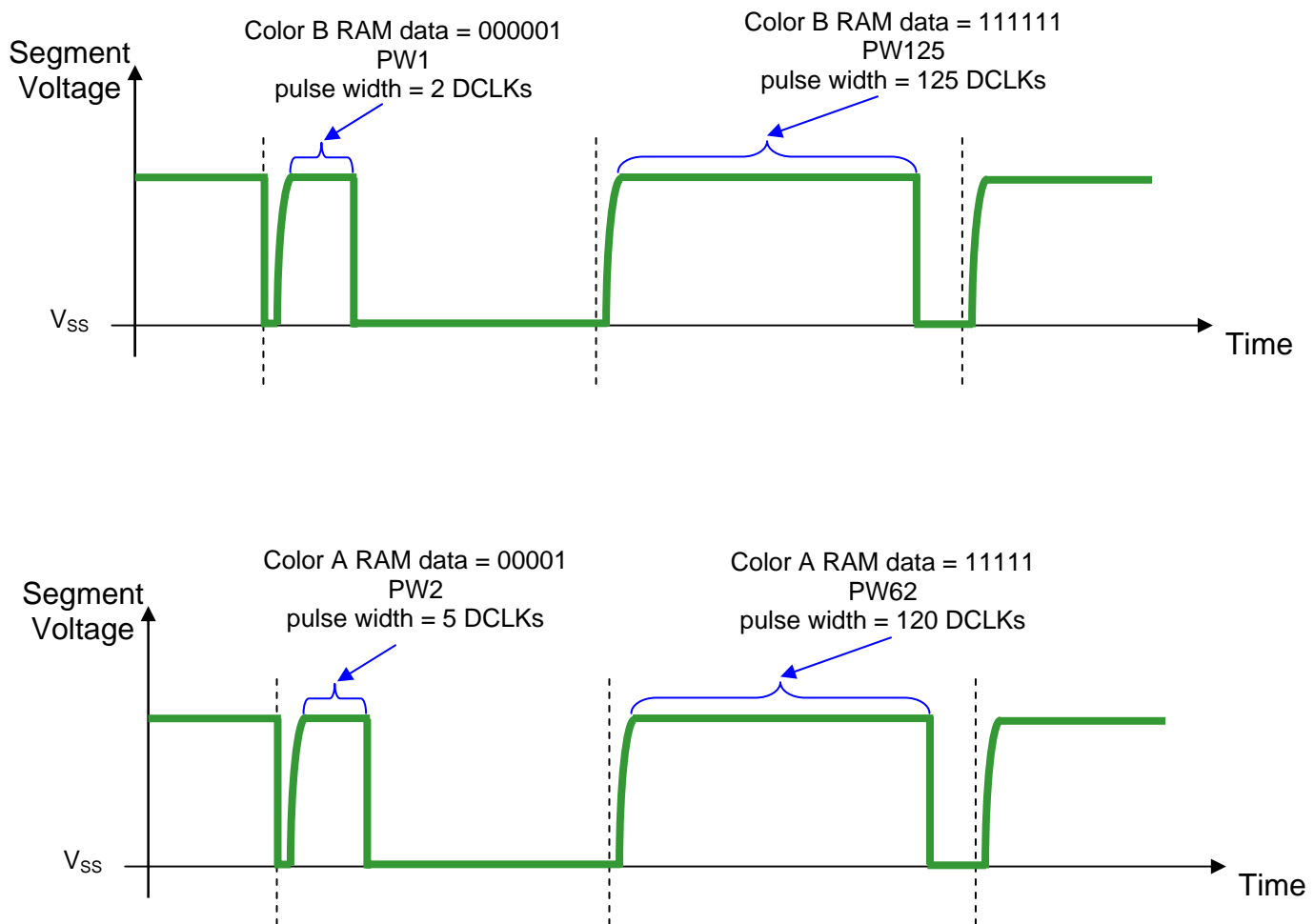
Color A, C RAM data (5 bits)	Color B RAM data (6 bits)	Gray Scale
0	0	GS0
-	1	GS 1
1	2	GS 2
-	3	GS 3
2	4	GS 4
:	:	:
:	:	:
:	:	:
30	60	GS 60
-	61	GS 61
31	62	GS 62
-	63	GS 63

**Figure 13 – Relation between graphic data RAM value and gray scale table entry for three colors in 65K color mode**

The meaning of values inside data RAM with respect to the gray scale level is best to be illustrated in an example below.

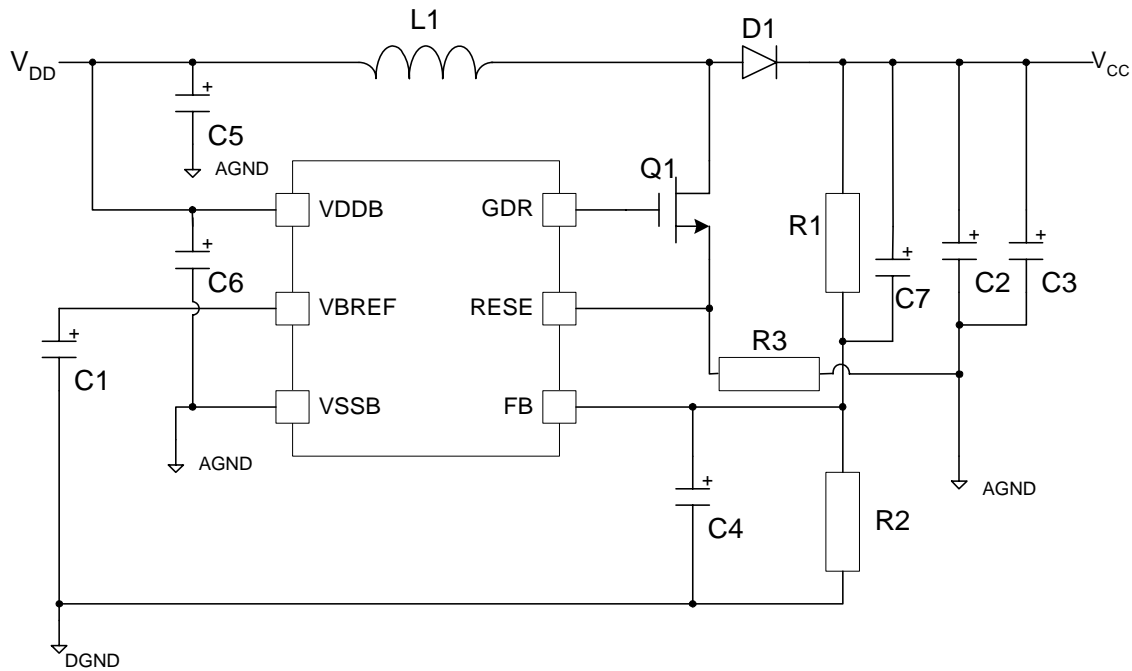
Gray Scale (Pulse Width)	Value/DCLKs
PW0	0
PW1	2
PW2	5
:	:
PW62	120
PW63	125

**Gray Scale Table**



**Figure 14 – illustration of relation between graphic display RAM value and gray scale control**

## DC-DC Voltage Converter



**Figure 15 – DC-DC Converter Application Circuit Diagram**

It is a switching voltage generator circuit, designed for handheld applications. In SSD1332, internal DC-DC voltage converter accompanying with an external application circuit (shown in Figure 15) can generate a high voltage supply  $V_{CC}$  from a low voltage supply input  $V_{DD}$ .  $V_{CC}$  is the voltage supply to the OLED driver block. The application circuit above is an example for the input voltage of 3V  $V_{DD}$  to generate  $V_{CC}$  of 12V @20mA ~ 30mA application.

\*ALL PATHS TO AGND SHOULD BE CONNECTED AS SHORT AS POSSIBLE

Passive components selection:

**Table 4 – Components Selection for DC-DC Converter**

Components	Typical Value	Remark
L1	Inductor, 22 $\mu$ H	2A
D1	Schottky diode	2A, 25V e.g. 1N5822
Q1	MOSFET	N-FET with low $R_{DS(on)}$ and low $V_{th}$ voltage. e.g. MGSF1N02LT1 [ON SEMICONDUCTOR]
R1, R2	Resistor	1%, 1/10W
R3	Resistor, 1.2 $\Omega$	1%, 1/2W
C1	Capacitor, 1 $\mu$ F	16V
C2	Capacitor, 22 $\mu$ F	Low ESR, 25V
C3	Capacitor, 1 $\mu$ F	16V
C4	Capacitor, 10nF	16V
C5	Capacitor, 1 ~ 10 $\mu$ F	16V
C6	Capacitor, 0.1 ~ 1 $\mu$ F	16V
C7	Capacitor, 15nF	16V

The  $V_{CC}$  output voltage level can be adjusted by R1 and R2, the reference formula is:

$$V_{CC} = 1.2 \times (R1+R2) / R2$$

## 8 COMMAND TABLE

**Table 5 – Configuration Command Table**

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#) = 0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0	15 A[6:0] B[6:0]	0 * *	0 A <sub>6</sub> B <sub>6</sub>	0 A <sub>5</sub> B <sub>5</sub>	1 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Column Address	A[6:0] sets the column start address from 0-95, RESET=00d. B[6:0] sets the column end address from 0-95 RESET=95d.
0 0 0	75 A[5:0] B[5:0]	0 * *	1 * *	1 A <sub>5</sub> B <sub>5</sub>	1 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	1 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Row Address	A[5:0] sets the row start address from 0-63, RESET=00d. B[5:0] sets the row end address from 0-63, RESET=63d.
0 0	81 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast for Color A (Segment Pins :SA0 – SA95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. RESET = 80h
0 0	82 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Contrast for Color B (Segment Pins :SB0 – SB95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. RESET = 80h
0 0	83 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast for Color C (Segment Pins :SC0 – SC95)	Double byte command to select 1 out of 256 contrast steps. Contrast increases as level increases. RESET = 80h
0 0	87 A[3:0]	1 *	0 *	0 *	0 *	0 A <sub>3</sub>	1 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Master Current Control	Set A[3:0] from 0000, 0001... to 1111 to adjust the master current attenuation factor from 1/16, 2/16... to 16/16. RESET =1111b, for no attenuation.
0 0	A0 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 A <sub>5</sub>	0 A <sub>4</sub>	0 *	0 *	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Re-map & Data Format	A[0]=0, Horizontal address increment (RESET) A[0]=1, Vertical address increment  A[1]=0, Column address 0 is mapped to SEG0 (RESET) A[1]=1, Column address 95 is mapped to SEG0  A[4]=0, Scan from COM 0 to COM [N –1] A[4]=1, Scan from COM [N-1] to COM0. Where N is the Multiplex ratio.  A[5]=0, Disable COM Split Odd Even (RESET) A[5]=1, Enable COM Split Odd Even  A[7:6]=00; 256 color format = 01; 65k color format(RESET)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	A1 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Start Line	Set display RAM display start line register from 0-63. Display start line register is reset to 00h after RESET.
0 0	A2 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	0 A <sub>0</sub>	Set Display Offset	Set vertical scroll by COM from 0-63. The value is reset to 00H after RESET.
0	A4~A7	1	0	1	0	0	1	X <sub>1</sub>	X <sub>0</sub>	Set Display Mode	A4h=Normal Display (RESET) A5h=Entire Display On, all pixels turn on at GS level 63 A6h=Entire Display Off, all pixels turn off A7h=Inverse Display
0 0	A8 A[5:0]	1 *	0 *	1 A <sub>5</sub>	0 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-64MUX, RESET=63d (64MUX) A[5:0]=0-14d (invalid entry)
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	0 A <sub>2</sub>	0 1	0 A <sub>0</sub>	Set Master Configuration	A[0]=0, Select external V <sub>CC</sub> supply at Display ON A[0]=1, Select internal booster at Display ON (RESET)  A[2]=0, Select External V <sub>P</sub> voltage supply A[2]=1, Select Internal V <sub>P</sub> (RESET)
0	AE~AF	1	0	1	0	X <sub>3</sub>	1	1	1	Set Display On/Off	A <sub>E</sub> h=Display off (RESET)  A <sub>F</sub> h=Display on
0 0	B0 A[7:0]	1 0	0 0	1 0	1 A <sub>4</sub>	0 0	0 0	0 A <sub>1</sub>	0 0	Set Power Save	A[7:0]=00 (RESET)  A[7:0]=12, power saving mode
0 0	B1 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Phase 1 and 2 period adjustment	A[3:0] Phase 1 period in 1~16 DCLK clocks [RESET=4h] A[7:4] Phase 2 period in 1~16 DCLK clocks [RESET=7h]
0 0	B3 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	1 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	1 A <sub>1</sub>	1 A <sub>0</sub>	Display Clock Divider / Oscillator Frequency	A[3:0] [DIVIDER, RESET=0] DCLK is generated from CLK divided by DIVIDER +1 (i.e., 1 to 16) A[7:4] Fosc frequency, RESET=D0H Frequency increases as level increases

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 32 bytes of command set the current drive pulse width of gray scale level GS1, GS3, GS5 ...GS63 as below:  A[7:0]=PW1, RESET=1, it equals 1 DCLK clock  B[7:0]=PW3, RESET=5, it equals 3 DCLK clocks  C[7:0]=PW5, RESET= 9  : : : :  AE[7:0]=PW61, RESET=121  AF[7:0]=PW63, RESET=125, it equals 125 DCLK clocks  Note: GS0 has no pre-charge and current drive stages. For GS2 GS4...GS62, they are derived by driver itself with: $PW_n = (PW_{n-1} + PW_{n+1}) / 2$ Max pulse width is 125
0	A[7:0]--PW1	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	B[7:0]--PW3	B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	C[7:0]--PW5	C <sub>7</sub>	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	:										
0	:										
0	:										
0	AE[7:0]--PW61	AE <sub>7</sub>	AE <sub>6</sub>	AE <sub>5</sub>	AE <sub>4</sub>	AE <sub>3</sub>	AE <sub>2</sub>	AE <sub>1</sub>	AE <sub>0</sub>		
0	AF[7:0]--PW63	AF <sub>7</sub>	AF <sub>6</sub>	AF <sub>5</sub>	AF <sub>4</sub>	AF <sub>3</sub>	AF <sub>2</sub>	AF <sub>1</sub>	AF <sub>0</sub>		
0	B9	1	0	1	1	1	0	0	1		Enable Linear Gray Scale Table  PW1=1,PW2=3,PW3=5  ...  PW61=121,PW62=123,PW63=125
0	BB ~ BD	1	0	1	1	1	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	V <sub>PA</sub> , V <sub>PB</sub> , V <sub>PC</sub> level setting for Color A,B,C	011b for Color A, 100b for Color B, 101b for Color C  A[7:0] 00000000 0.43*V <sub>REF</sub> 00111111 0.83* V <sub>REF</sub> 01111111 1.0* V <sub>REF</sub> 1xxxxxxx connects to V <sub>COMH</sub> (RESET)
0	A[7:0]	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	BE	1	0	1	1	1	1	1	0	Set V <sub>COMH</sub>	A[5:0] 000000 0.43* V <sub>REF</sub> 111111 0.83* V <sub>REF</sub> (RESET)
0	A[5:0]	0	0	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

**Table 6 – Graphic Acceleration Command Set Table**

(To write commands to command registers, the MCU interface pins are set as: D/C = 0, R/W(WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	21	0	0	1	0	0	0	0	1	Draw Line	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End E[5:1] : Color C of the line F[5:0] : Color B of the line G[5:1] : Color A of the line
0	A[6:0]	*	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	B[5:0]	*	*	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	C[6:0]	*	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	D[5:0]	*	*	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
0	E[5:1]	*	*	E <sub>5</sub>	E <sub>4</sub>	E <sub>3</sub>	E <sub>2</sub>	E <sub>1</sub>	*		
0	F[5:0]	*	*	F <sub>5</sub>	F <sub>4</sub>	F <sub>3</sub>	F <sub>2</sub>	F <sub>1</sub>	F <sub>0</sub>		
0	G[5:1]	*	*	G <sub>5</sub>	G <sub>4</sub>	G <sub>3</sub>	G <sub>2</sub>	G <sub>1</sub>	*		
0	22	0	0	1	0	0	0	1	0		Drawing Rectangle
0	A[6:0]	*	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	B[5:0]	*	*	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	C[6:0]	*	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	D[5:0]	*	*	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
0	E[5:1]	*	*	E <sub>5</sub>	E <sub>4</sub>	E <sub>3</sub>	E <sub>2</sub>	E <sub>1</sub>	*		
0	F[5:0]	*	*	F <sub>5</sub>	F <sub>4</sub>	F <sub>3</sub>	F <sub>2</sub>	F <sub>1</sub>	F <sub>0</sub>		
0	G[5:1]	*	*	G <sub>5</sub>	G <sub>4</sub>	G <sub>3</sub>	G <sub>2</sub>	G <sub>1</sub>	*		
0	H[5:1]	*	*	H <sub>5</sub>	H <sub>4</sub>	H <sub>3</sub>	H <sub>2</sub>	H <sub>1</sub>	*		
0	I[5:0]	*	*	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>		
0	J[5:1]	*	*	J <sub>5</sub>	J <sub>4</sub>	J <sub>3</sub>	J <sub>2</sub>	J <sub>1</sub>	*		
0	23	0	0	1	0	0	0	1	1	Copy	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End E[6:0] : Column Address of New Start F[5:0] : Row Address of New Start
0	A[6:0]	*	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	B[5:0]	*	*	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	C[6:0]	*	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	D[5:0]	*	*	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
0	E[6:0]	*	E <sub>6</sub>	E <sub>5</sub>	E <sub>4</sub>	E <sub>3</sub>	E <sub>2</sub>	E <sub>1</sub>	E <sub>0</sub>		
0	F[5:0]	*	*	F <sub>5</sub>	F <sub>4</sub>	F <sub>3</sub>	F <sub>2</sub>	F <sub>1</sub>	F <sub>0</sub>		
0	24	0	0	1	0	0	1	0	0	Dim Window	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End The effect of dim window: GS15~GS0 no change GS19~GS16 become GS4 GS23~GS20 become GS5 ... GS63~GS60 become GS15
0	A[6:0]	*	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	B[5:0]	*	*	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	C[6:0]	*	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	D[5:0]	*	*	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		
0	25	0	0	1	0	0	1	0	1	Clear Window	A[6:0] : Column Address of Start B[5:0] : Row Address of Start C[6:0] : Column Address of End D[5:0] : Row Address of End
0	A[6:0]	*	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	B[5:0]	*	*	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
0	C[6:0]	*	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>		
0	D[5:0]	*	*	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26	0	0	1	0	0	1	1	0	Fill Enable / Disable	A0 0 : Disable Fill for Draw Rectangle Command (RESET) 1 : Enable Fill for Draw Rectangle Command
0	A[4:0]	*	*	*	A <sub>4</sub>	0	0	0	A <sub>0</sub>		A[3:1] 000 : Reserved values A4 0 : Disable reverse copy (RESET) 1 : Enable reverse during copy command.

**Table 7 - Read Command Table**

(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
D <sub>7</sub> D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> D <sub>0</sub>	Status Register Read *	D <sub>7</sub> : "1" for Command lock D <sub>6</sub> : "1" for display OFF / "0" for display ON D <sub>5</sub> : Reserve D <sub>4</sub> : Reserve D <sub>3</sub> : Reserve D <sub>2</sub> : Reserve D <sub>1</sub> : Reserve D <sub>0</sub> : Reserve

Note: Patterns other than that given in Command Table are prohibited to enter to the chip as a command; otherwise, unexpected result will occur.

**Data Read / Write**

To read data from the GDDRAM, input HIGH to R/W (WR#) pin and D/C pin for 6800-series parallel mode, LOW to E (RD#) pin and HIGH to D/C pin for 8080-series parallel mode. No data read is provided in serial mode operation.

In normal data read mode, GDDRAM column address pointer will be increased by one automatically after each data read.

Also, a dummy read is required before the first data read. See Figure 5 in Functional Block Description.

To write data to the GDDRAM, input LOW to R/W (WR#) pin and HIGH to D/C pin for 6800-series parallel mode AND 8080-series parallel mode. For serial interface mode, it is always in write mode. GDDRAM column address pointer will be increased by one automatically after each data write.

**Table 8 - Address increment table (Automatic)**

D/C	R/W (WR#)	Comment	Address Increment
0	0	Write Command	No
0	1	Read Status	No
1	0	Write Data	Yes
1	1	Read Data	Yes

## 9 COMMAND DESCRIPTIONS

### Set Column Address (15h)

This command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address.

### Set Row Address (75h)

This command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 93, row start address is set to 1 and row end address is set to 62. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 93 and from row 1 to row 62 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation. Whenever the column address pointer finishes accessing the end column 93, it is reset back to column 2 and row address is automatically increased by 1. While the end row 62 and end column 93 RAM location is accessed, the row address is reset back to 1. The diagram below shows the way of column and row address pointer movement for this example.

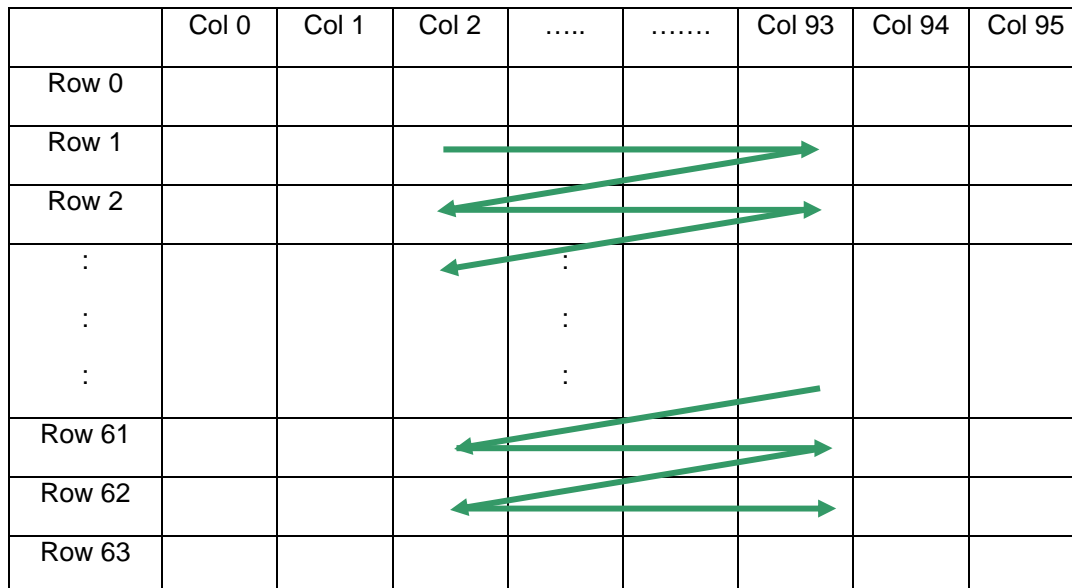


Figure 16 – Example of Column and Row Address Pointer Movement

















































