

# *Crystalfontz America, Inc.*

**CUSTOMER :** \_\_\_\_\_  
**MODULE NO.:** **CFAG12232D-YYH-VA** (preliminary)

<b>SALES BY</b>	<b>APPROVED BY</b>	<b>CHECKED BY</b>	<b>PREPARED BY</b>
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# 1.Module Classification Information

CFA G 1 2 2 3 2 D Y Y H VA  
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧

①	Brand □ CRYSTALFONTZ AMERICA, INCORPORATED	
②	Display Type □ H → Character Type, <b>G → Graphic Type</b>	
③	Display's logical dimensions: <b>122</b> pixels by <b>32</b> pixels	
④	PCB Variant: <b>D</b>	
⑤	Backlight Type	N → Without backlight B → EL, Blue green D → EL, Green W → EL, White F → CCFL, White <b>Y → LED, Yellow Green</b> A → LED, Amber R → LED, Red O → LED, Orange G → LED, Green
⑥	LCD Mode	B → TN Positive, Gray      T → FSTN Negative N → TN Negative, G → STN Positive, Gray <b>Y → STN Positive, Yellow Green</b> M → STN Negative, Blue F → FSTN Positive
⑦	LCD Polarize Type/ Temperature range/ View direction	A → Reflective, N.T, 6:00 <b>H → Transflective, W.T,6:00</b> D → Reflective, N.T, 12:00      K → Transflective, W.T,12:00 G → Reflective, W. T, 6:00      C → Transmissive, N.T,6:00 J → Reflective, W. T, 12:00      F → Transmissive, N.T,12:00 B → Transflective, N.T,6:00      I → Transmissive, W. T, 6:00 E → Transflective, N.T.12:00      L → Transmissive, W.T,12:00
⑧	Special Code	<b>V → negative voltage generator on board; A → Avant IC</b>

## **2.Precautions in use of LCD Modules**

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

## **3.General Specification**

<b>Item</b>	<b>Dimension</b>	<b>Unit</b>
Number of Characters	122 x 32	
Module dimension	59.0 x 29.3 x 5.5(MAX)	mm
View area	52.0 x 15.0	mm
Active area	45.72 x 11.97	mm
Dot size	0.345 x 0.345	mm
Dot pitch	0.375 x 0.375	mm
LCD type	STN, Positive, Transflective , Yellow Green	
Duty	1/32	
View direction	6 o'clock	
Backlight Type	Led Edge ,Yellow Green(Internal Power)	

## 4. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	$T_{OP}$	-20		+70	°C
Storage Temperature	$T_{ST}$	-30		+80	°C
Input Voltage	$V_I$	0		$V_{DD}$	V
Supply Voltage For Logic	$V_{DD}$	0		6.7	V
Supply Voltage For LCD	$V_{DD}-V_{LCD}$	0		-10	V
Supply Voltage For LCD	VEE	0		-10	V

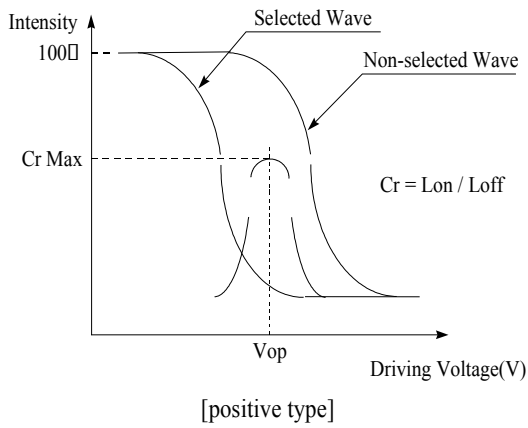
## 5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$		4.75	5.0	5.25	V
Supply Voltage For LCD	$V_{DD}-V_O$	$T_a=-20^{\circ}\text{C}$ $T_a=25^{\circ}\text{C}$ $T_a=+70^{\circ}\text{C}$	3.9	4.7	5.8	V V V
Input High Volt.	$V_{IH}$		2.0		$V_{DD}$	V
Input Low Volt.	$V_{IL}$		0		0.8	V
Output High Volt.	$V_{OH}$		2.7		$V_{DD}$	V
Output Low Volt.	$V_{OL}$		0		0.4	V
Supply Current	$I_{DD}$		0.6	0.8	1.2	mA

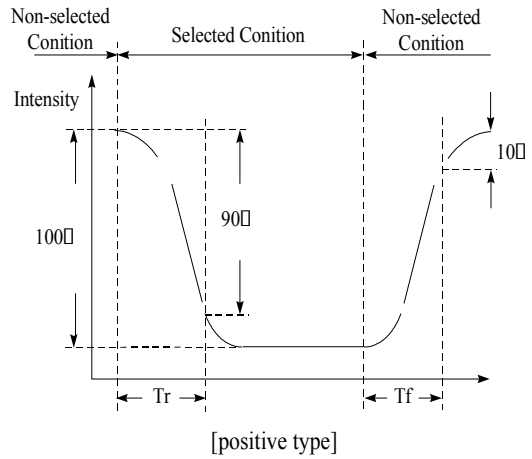
# 6. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) $\theta$	$CR \geq 2$	20	-	40	deg
	(H) $\phi$	$CR \geq 2$	-30	-	30	deg
Contrast Ratio	CR	-		3	-	-
Response Time	T rise	-	-	100	150	ms
	T fall	-	-	100	150	ms

## Definition of Operation Voltage (Vop)



## Definition of Response Time (Tr, Tf)



### Conditions :

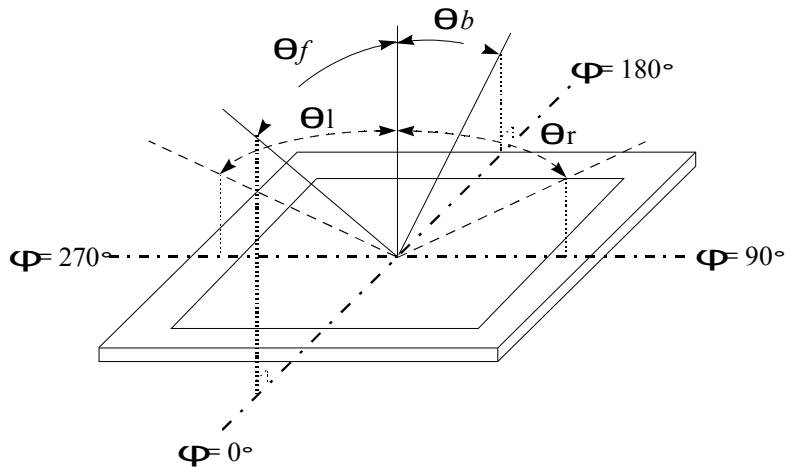
Operating Voltage : Vop

Viewing Angle( $\theta$   $\phi$ ) :  $0^\circ \leq \theta \leq 0^\circ$

Frame Frequency : 64 HZ

Driving Waveform : 1/N duty , 1/a bias

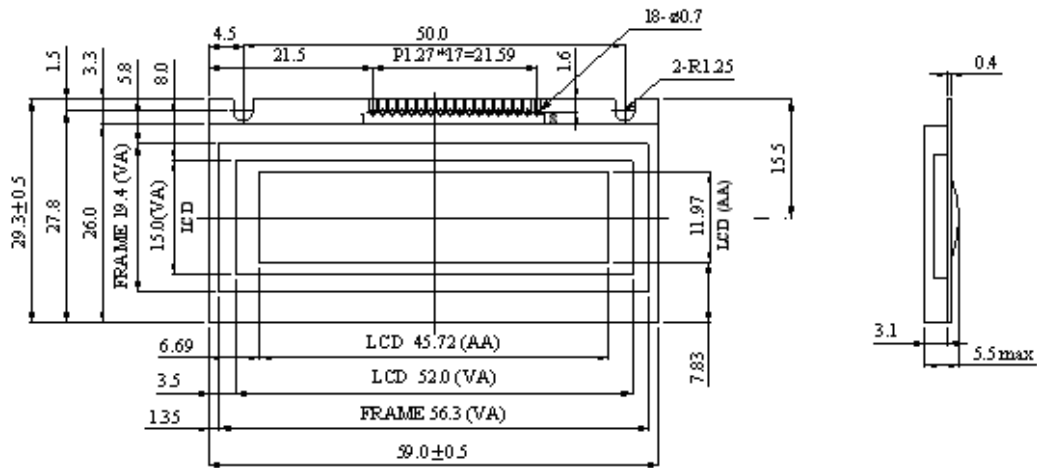
## Definition of viewing angle(CR $\geq$ 2)



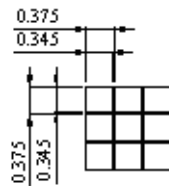
## **7.Interface Description**

<b>Pin No.</b>	<b>Symbol</b>	<b>Level</b>	<b>Description</b>
1	/VLED	0V	B/L Selected
2	V <sub>ss</sub>	0V	Ground
3	V <sub>dd</sub>	5V	Power supply for logic
4	Vo	(Variable)	Operating voltage for LCD
5	A0	H/L	H : Data L : Instruction
6	E1	H/L	Chip select signal for IC1 ( left 61*32 dots ) active "H"
7	E2	H/L	Chip select signal for IC2 ( right 61*32 dots ) active "H"
8	DB0	H/L	Data bus line
9	DB1	H/L	Data bus line
10	DB2	H/L	Data bus line
11	DB3	H/L	Data bus line
12	DB4	H/L	Data bus line
13	DB5	H/L	Data bus line
14	DB6	H/L	Data bus line
15	DB7	H/L	Data bus line
16	R/W	H/L	H : Read ; L : Write
17	VEE		Negative Voltage output
18	NC		NC

# 8. Contour Drawing & Block Diagram

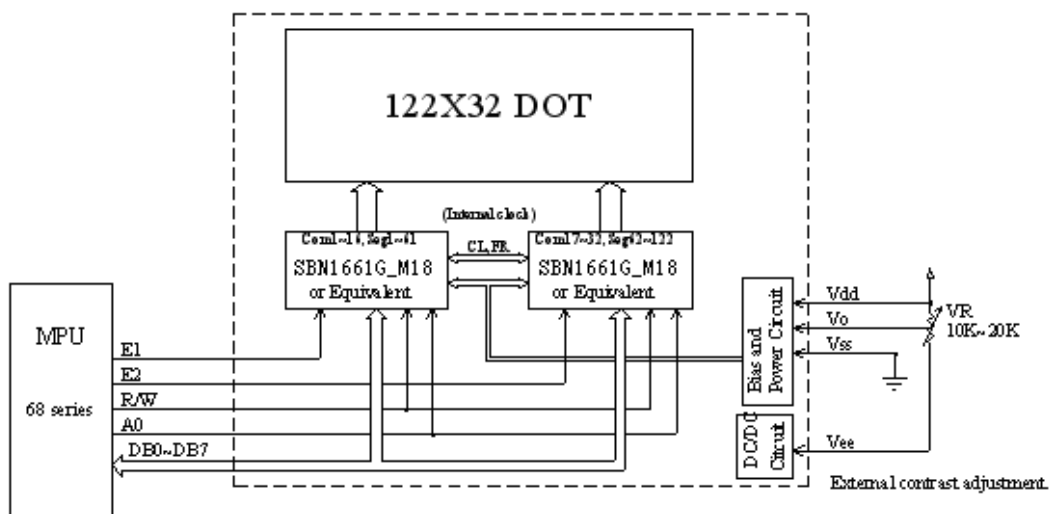


Pin No.	Symbol
1	VLED
2	VSS
3	VDD
4	VO
5	AO
6	E1
7	E2
8	DB0
9	DB1
10	DB2
11	DB3
12	DB4
13	DB5
14	DB6
15	DB7
16	R/W
17	VEE
18	NC



DOT SIZE  
SCALE 15/1

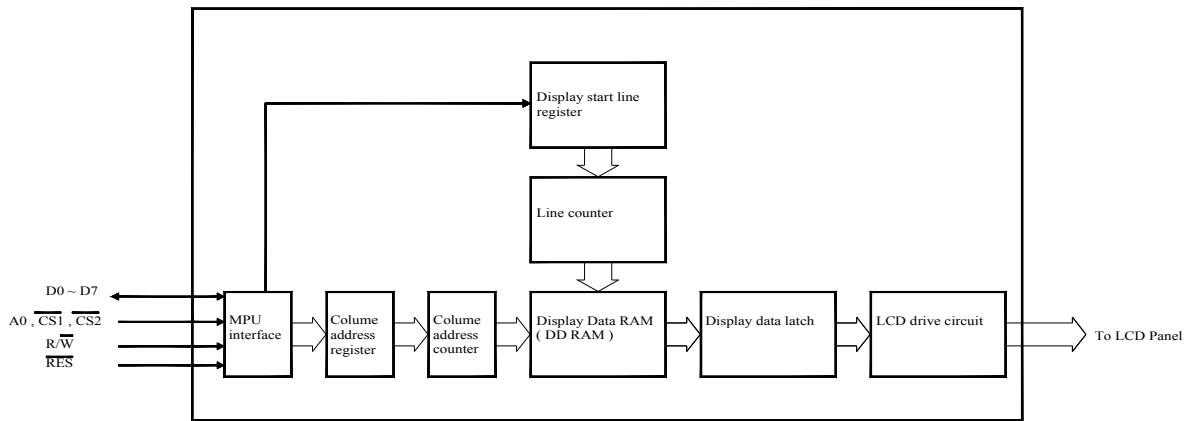
The non-specified tolerance of dimension is? 0.3 mm.



# 9. Function Description

## Block Diagram

This 122×32 dots LCD Module built in two SBN1661G\_M18-D LSI controller.



## MPU interface

The SBN1661G\_M18-D controller transfers data via 8-bit bidirectional data buses (D0 to D7), it can fit any MPU if it corresponds to SBN1661G\_M18-D Read and Write Timing Characteristics.

## Data transfer

The SBN1661G\_M18-D driver uses the A0, E and R/W signals to transfer data between the system MPU and internal registers, The combinations used are given in the table below.

A0	R/W	Function
1	1	Read display data
1	0	Write display data
0	1	Read status
0	0	Write to internal register (command)

**Busy flag**

When the Busy flag is logical 1, the SBN1661G\_M18-D series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time ( $t_{CYC}$ ) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

**Display Start Line and Line Count Registers**

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command.

**Column Address Counter**

The column address counter is a 7-bit presentable counter that supplies the column address for MPU access to the display data RAM. See Figure 1. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

**Display Data RAM**

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relationship between display data, display address and the display is shown in Figure 1

**Page Register**

The page register is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 1. The contents of the page register are set by the Set Page Register command.

**Figure 1.**

# Display Data RAM Address

Page address	DATA	Line address	Common output			
D1,D2=0,0	D0	00H	COM 0			
	D1	01H	COM 1			
	D2	02H	COM 2			
	D3	03H	COM 3			
	D4	04H	COM 4			
	D5	05H	COM 5			
	D6	06H	COM 6			
	D7	07H	COM 7			
0,1	D0	08H	COM 8			
	D1	09H	COM 9			
	D2	0AH	COM 10			
	D3	0BH	COM 11			
	D4	0CH	COM 12			
	D5	0DH	COM 13			
	D6	0EH	COM 14			
	D7	0FH	COM 15			
1,0	D0	10H	COM 16			
	D1	11H	COM 17			
	D2	12H	COM 18			
	D3	13H	COM 19			
	D4	14H	COM 20			
	D5	15H	COM 21			
	D6	16H	COM 22			
	D7	17H	COM 23			
1,1	D0	18H	COM 24			
	D1	19H	COM 25			
	D2	1AH	COM 26			
	D3	1BH	COM 27			
	D4	1CH	COM 28			
	D5	1DH	COM 29			
	D6	1EH	COM 30			
	D7	1FH	COM 31			
Column address	ADC	D0=0	4FH	00H	80	
		D0=1	4EH	01H	79	
		00H	4FH	4EH	02H	78
		01H	4EH	4DH	03H	77
		02H	4DH	4CH	04H	76
		03H	4CH	4BH	05H	75
		04H	4BH	4AH	06H	74
		05H	4AH	49H	07H	73
		06H	49H	48H	08H	72
		07H	48H	47H	09H	71
		08H	47H	46H	0AH	70
		09H	46H	45H	0BH	69
		0AH	45H	44H	0CH	68
		0BH	44H	43H	0DH	67
		0CH	43H	42H	0EH	66
		0DH	42H	41H	0FH	65
		0EH	41H	40H	10H	64
		0FH	40H	3FH	11H	63
		10H	3FH	3EH	12H	62
		11H	3EH	3DH	13H	61
		12H	3DH	3CH	14H	60
		13H	3CH	3BH	15H	59
		14H	3BH	3AH	16H	58
		15H	3AH	39H	17H	57
		16H	39H	38H	18H	56
		17H	38H	37H	19H	55
		18H	37H	36H	20H	54
		19H	36H	35H	21H	53
		20H	35H	34H	22H	52
		21H	34H	33H	23H	51
		22H	33H	32H	24H	50
		23H	32H	31H	25H	49
		24H	31H	30H	26H	48
		25H	30H	29H	27H	47
		26H	29H	28H	28H	46
		27H	28H	27H	29H	45
		28H	27H	26H	30H	44
		29H	26H	25H	31H	43
		30H	25H	24H	32H	42
		31H	24H	23H	33H	41
		32H	23H	22H	34H	40
		33H	22H	21H	35H	39
		34H	21H	20H	36H	38
		35H	20H	19H	37H	37
		36H	19H	18H	38H	36
		37H	18H	17H	39H	35
		38H	17H	16H	40H	34
		39H	16H	15H	41H	33
		40H	15H	14H	42H	32
		41H	14H	13H	43H	31
		42H	13H	12H	44H	30
		43H	12H	11H	45H	29
		44H	11H	10H	46H	28
		45H	10H	09H	47H	27
		46H	09H	08H	48H	26
		47H	08H	07H	49H	25
		48H	07H	06H	50H	24
		49H	06H	05H	51H	23
		50H	05H	04H	52H	22
		51H	04H	03H	53H	21
		52H	03H	02H	54H	20
		53H	02H	01H	55H	19
		54H	01H	00H	56H	18
		55H	00H		57H	17
		56H			58H	16
		57H			59H	15
		58H			60H	14
		59H			61H	13
		60H			62H	12
		61H			63H	11
		62H			64H	10
		63H			65H	09
		64H			66H	08
		65H			67H	07
		66H			68H	06
		67H			69H	05
		68H			70H	04
		69H			71H	03
		70H			72H	02
		71H			73H	01
		72H			74H	00
		73H			75H	
		74H			76H	
		75H			77H	
		76H			78H	
		77H			79H	
		78H			80H	
		79H				
		80H				

SED1520: 00H to 39H

SED1521: 00H to 61H

The 122\*32 dots display area is consisted 2 61\*32, The interface pin CS1 enable the left 61\*32, CS2 enable the right 61\*32 dots.

# 10. Commands Descriptions

The host microcontroller can issue commands to the SBN1661G\_X. Table 27 lists all the commands. When issuing a command, the host microcontroller should put the command code on the data bus. The host microcontroller should also give the control bus C/D, E(RD), and R/W(WR) proper value and timing.

## Commands

COMMAND	COMMAND CODE								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
Write Display Data	Data to be written into the Display Data Memory.								Write a byte of data to the Display Data Memory.
Read Display Data	Data read from the Display Data Memory.								Read a byte of data from the Display Data Memory.
Read-Modify-Write	1	1	1	0	0	0	0	0	Start Read-Modify-Write operation.
END	1	1	1	0	1	1	1	0	Stop Read-Modify-Write operation.
Software Reset	1	1	1	0	0	0	1	0	Software Reset.

## Write Display Data

The Write Display Data command writes a byte (8 bits) of data to the Display Data Memory. Data is put on the data bus by the host microcontroller. The location which accepts this byte of data is pointed to by the Page Address Register and the Column Address Register. At the end of the command operation, the content of the Column Address Register is automatically incremented by 1.

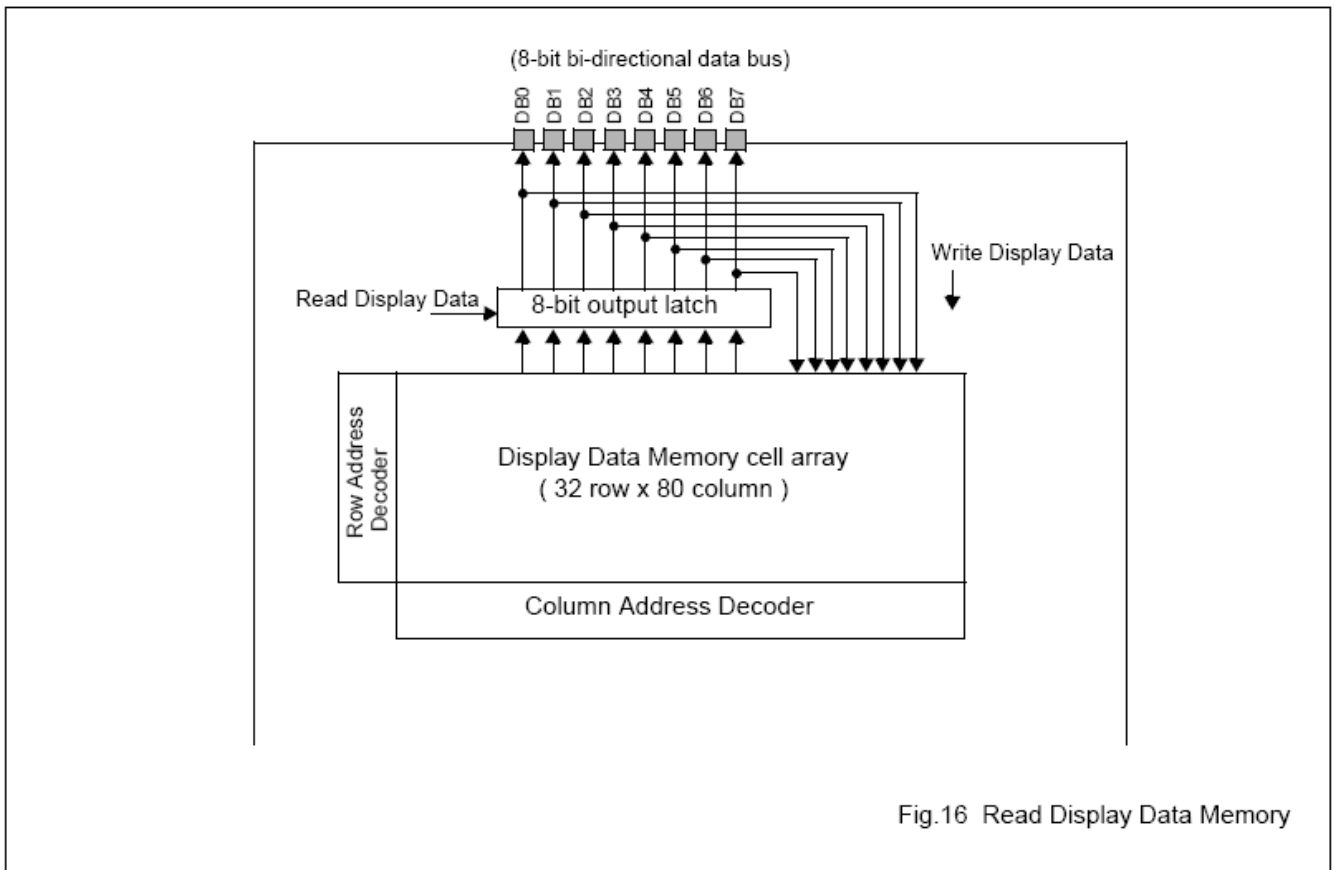
### The setting of the control bus for issuing Write Display Data command

$\overline{C/D}$	$E/(\overline{RD})$	$R/\overline{W}(\overline{WR})$
1	1	0

## Read Display Data

The Read Display Data command starts a 3-step operation.

1. First, the current data of the internal 8-bit output latch of the Display Data Memory is read by the microcontroller, via the 8-bit data bus DB0~DB7.
2. Then, a byte of data of the Display Data Memory is transferred to the 8-bit output latch from a location specified by the Page Address Register and the Column Address Register,
3. Finally, the content of the Column Address Register is automatically incremented by one. Fig. 16 shows the internal 8-bit output latch located between the 8-bit I/O data bus and the Display Data Memory cell array. Because of this internal 8-bit output latch, a dummy read is needed to obtain correct data from the Display Data Memory. For Display Data Write operation, a dummy write is **not** needed, because data can be directly written from the data bus to internal memory cells.



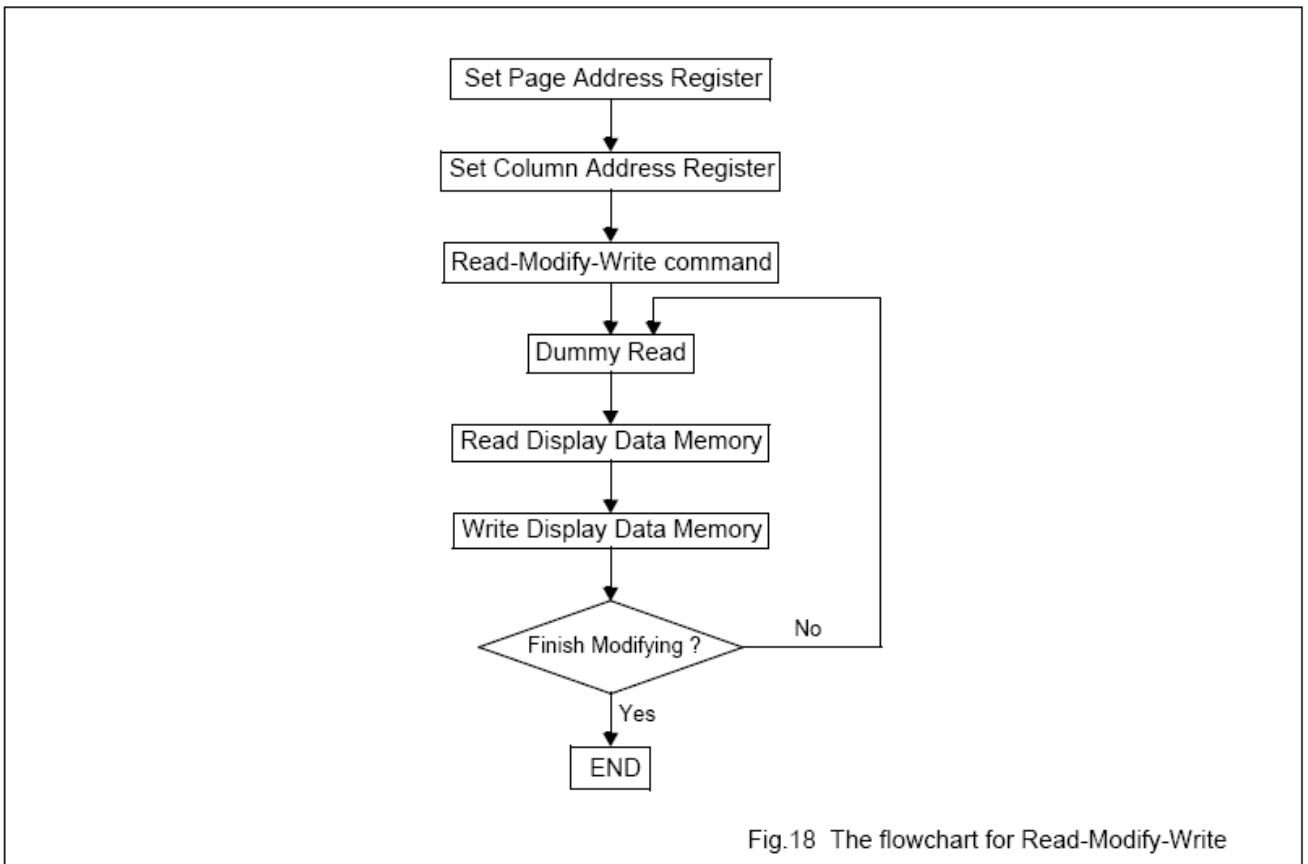
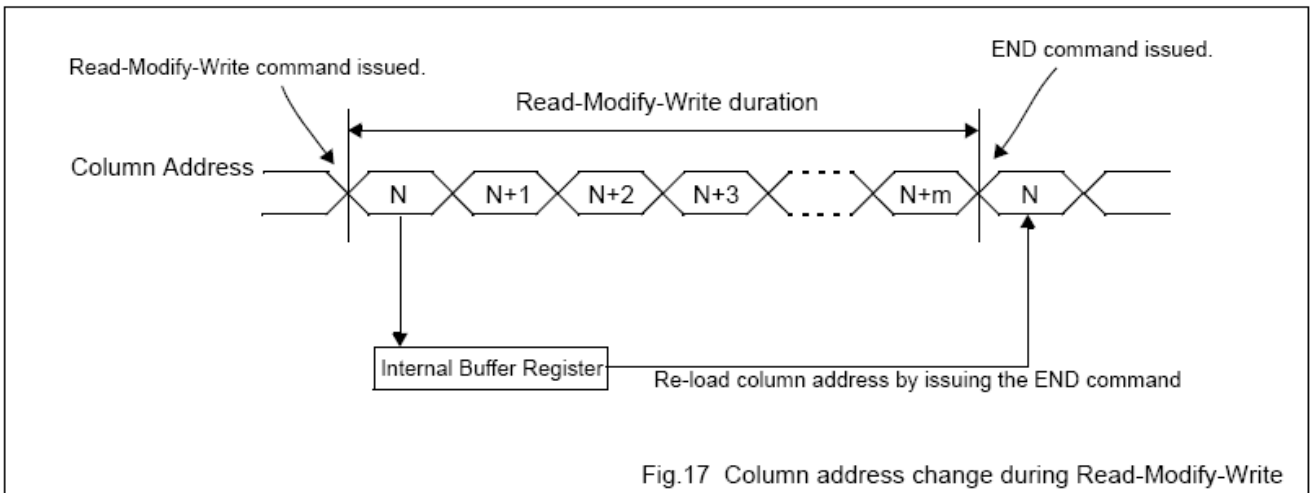
**The setting of the control bus for issuing Read Display Data command**

$\overline{C/D}$	$E/(\overline{RD})$	$R/\overline{W}(\overline{WR})$
1	0	1

**Read-Modify-Write**

When the Read-Modify-Write command is issued, the SBN1661G\_X enters into Read-Modify-Write mode. In normal operation, when a Read Display Data command or a Write Display Data command is issued, the content of the Column Address Register is automatically incremented by one after the command operation is finished. However, during Read-Modify-Write mode, the content of the Column Address Register is not incremented by one after a Read Display Data command is finished; only the Write Display Data command can make the content of the Column Address Register automatically incremented by one after the command operation is finished. During Read-Modify-Write mode, any other registers, except the Column Address Register, can be modified. This command is useful when a block of the Display Data Memory needs to be repeatedly read and updated.

Fig. 17 gives the change sequence of the Column Address Register during Read-Modify-Write mode. Figure 18 gives the flow chart for Read-Modify-Write command.



**The setting of the control bus for the Read-Modify-Write command**

$\bar{C}/D$	$E/(\bar{RD})$	$R/\bar{W}(\bar{WR})$
0	1	0

**The setting of the data bus for the Read-Modify-Write command**

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	0	0	0	0

**The END command**

The END command releases the Read-Modify-Write mode and re-loads the Column Address Register with the value previously stored in the internal buffer (refer to Fig. 17) when the Read-Modify-Write command was issued.

### The setting of the control bus for the END command

$\overline{C}/D$	$E/(\overline{RD})$	$R/\overline{W}(\overline{WR})$
0	1	0

### The setting of the data bus for the END command

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	1	1	1	0

The command code is EE Hex.

### Software RESET command

The Software Reset command is different from the hardware reset and can not be used to replace hardware reset.

When Software Reset is issued by the host microcontroller,

- the content of the Display Start Line Register is cleared to zero(A4~A0=00000),
- the Page Address Register is set to 3 (A1 A0 = 11),
- the content of the Display Data Memory remains unchanged.
- the content of all other registers remains unchanged.

### The setting of the control bus for Software RESET

$\overline{C}/D$	$E/(\overline{RD})$	$R/\overline{W}(\overline{WR})$
0	1	0

The setting of the data bus for Software RESET

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	0	0	1	0

The command code is E2 Hex.

# 11. Timing Characteristics

## CL and FR timing

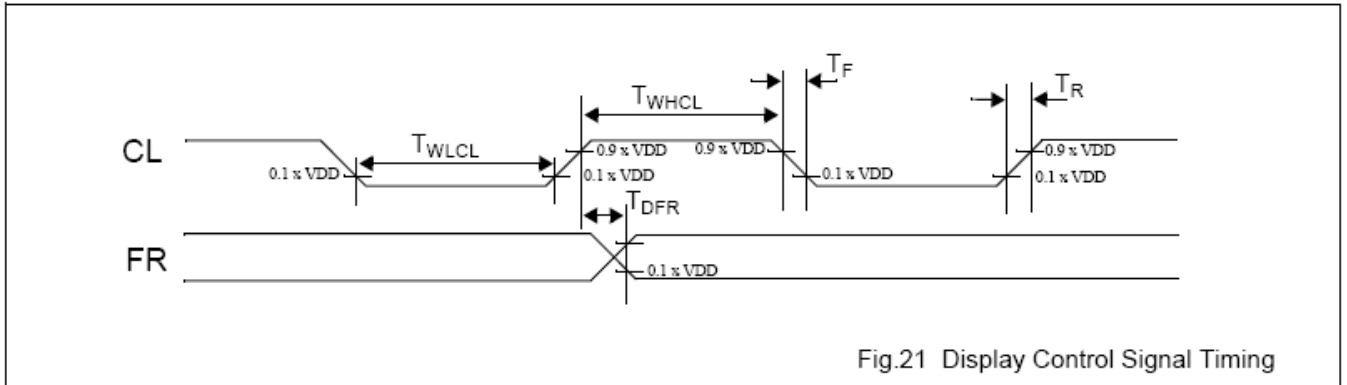


Fig.21 Display Control Signal Timing

CL and FR timing characteristics at VDD=5 volts

VDD = 5 V ±10%; VSS = 0 V; all voltages with respect to VSS unless otherwise specified; Tamb = -20 to +75 °C.

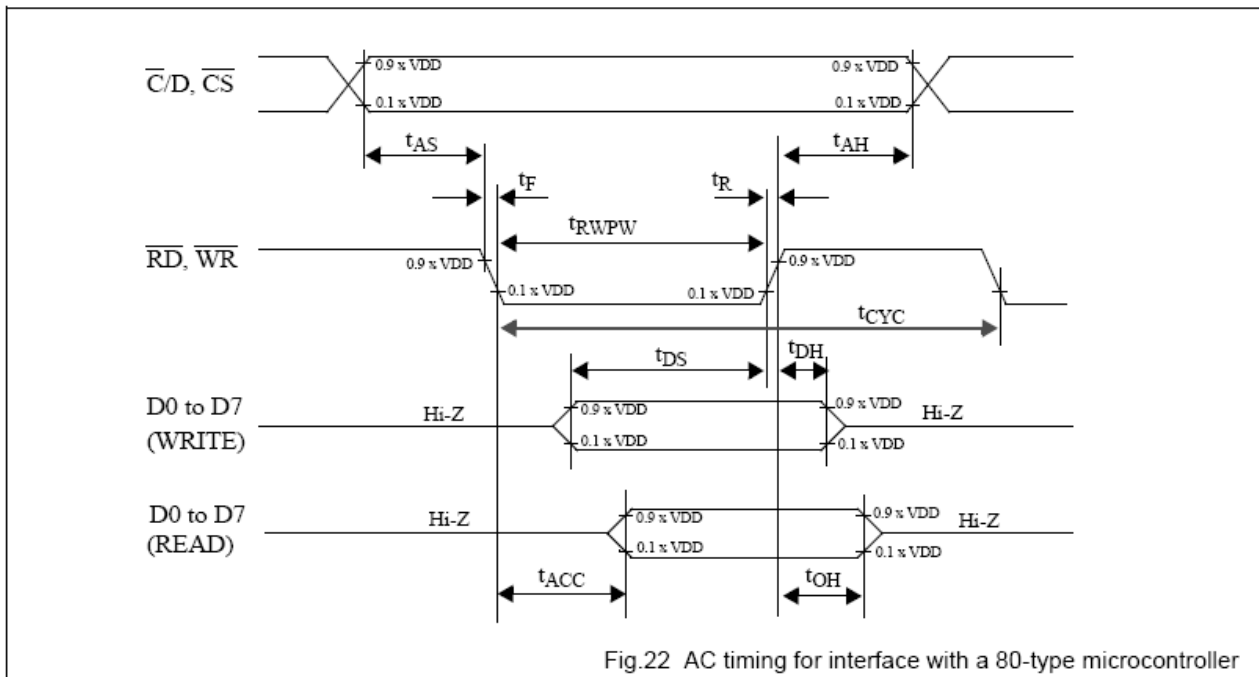
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNI
$T_{WHCL}$	CL clock high pulse width		33			μS
$T_{WLCL}$	CL clock low pulse width		33			μS
$T_R$	CL clock rise time			28	120	ns
$T_F$	CL clock fall time			28	120	ns
$T_{DFR(input)}$	FR delay time (input)	When used as input in Slave Mode application	-2.0	0.2	1.6	μS
$T_{DFR(output)}$	FR delay time (output)	When used as output in Master Mode application, with CL= 100 pF.		0.2	0.36	μS

CL and FR timing characteristics at VDD=3 volts

VDD = 3 V ±10%; VSS = 0 V; all voltages with respect to VSS unless otherwise specified; Tamb = -20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$T_{WHCL}$	CL clock high pulse width		65			$\mu\text{s}$
$T_{WLCL}$	CL clock low pulse width		65			$\mu\text{s}$
$T_R$	CL clock rise time			50	220	ns
$T_F$	CL clock fall time			50	220	ns
$T_{DFR(\text{input})}$	FR delay time (input)	When used as input in Slave Mode application	-3.6	0.36	3.6	$\mu\text{s}$
$T_{DFR(\text{output})}$	FR delay time (output)	When used as output in Master Mode application, with $C_L = 100 \text{ pF}$ .		0.32	0.6	$\mu\text{s}$

### AC timing for interface with an 80-type microcontroller



AC timing for interface with a 80-type microcontorlller at  $V_{DD} = 5 \text{ volts}$   $V_{DD} = 5 \text{ V} \pm 10\%$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -20 \text{ }^\circ\text{C}$  to  $+75 \text{ }^\circ\text{C}$ .

symbol	parameter	min.	max.	test conditons	unit
$t_{AS}$	Address set-up time	20			ns
$t_{AH}$	Address hold time	10			ns
$t_F, t_R$	Read/Write pulse falling/rising time		15		ns
$t_{RWPW}$	Read/Write pulse width	200			ns
$t_{CYC}$	System cycle time	1000			ns
$t_{DS}$	Data setup time	80			ns
$t_{DH}$	Data hold time	10			ns
$t_{ACC}$	Data READ access time		90	$C_L = 100 \text{ pF}$ .	ns
$t_{OH}$	Data READ output hold time	10	60	Refer to Fig. 23.	ns

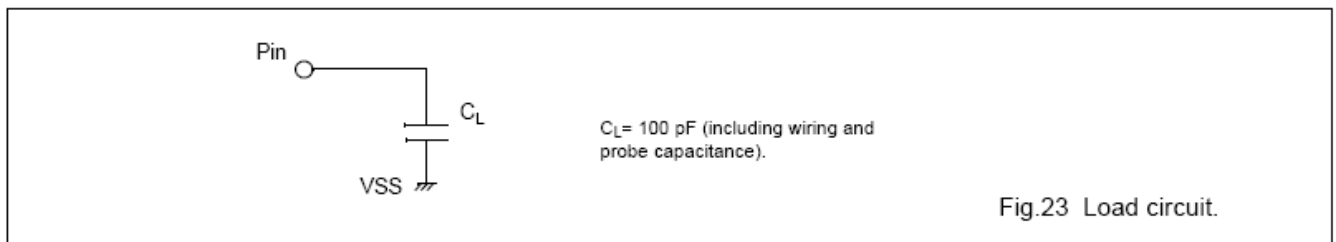
AC timing for interface with an 80-type microcontorlller at  $V_{DD} = 3 \text{ volts}$   $V_{DD} = 3 \text{ V} \pm 10\%$ ;  $V_{SS} = 0 \text{ V}$ ;  $T_{amb} = -20 \text{ }^\circ\text{C}$  to  $+75 \text{ }^\circ\text{C}$ .

symbol	parameter	min.	max.	test conditons	unit
t <sub>AS</sub>	Address set-up time	40			ns
t <sub>AH</sub>	Address hold time	20			ns
t <sub>F</sub> , t <sub>R</sub>	Read/Write pulse falling/rising time		15		ns
t <sub>RWPW</sub>	Read/Write pulse width	400			ns
t <sub>CYC</sub>	System cycle time	2000			ns
t <sub>DS</sub>	Data setup time	160			ns

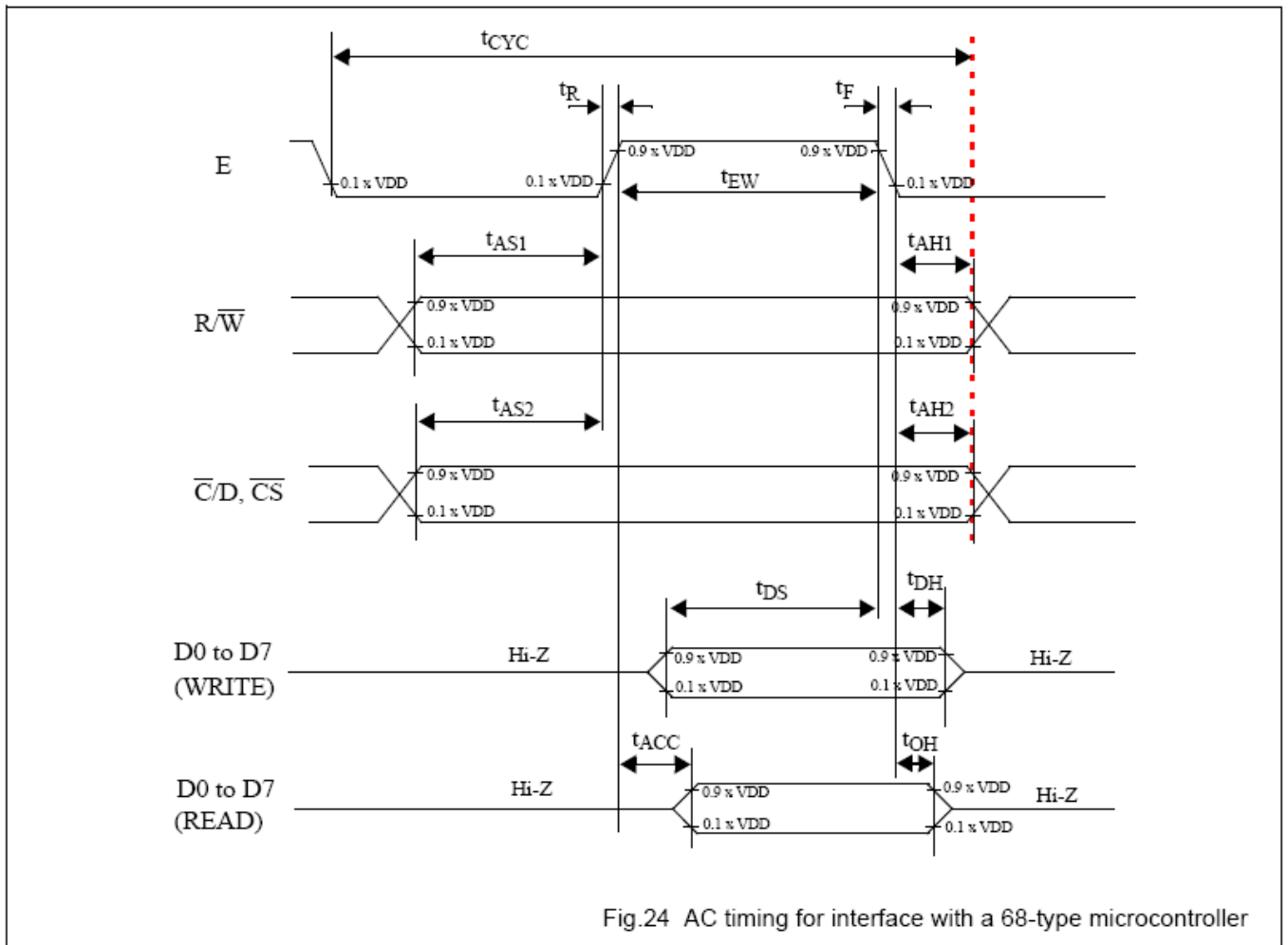
symbol	parameter	min.	max.	test conditons	unit
t <sub>DH</sub>	Data hold time	20			ns
t <sub>ACC</sub>	Data READ access time		180	CL= 100 pF,	ns
t <sub>OH</sub>	Data READ output hold time	20	120	Refer to 23.	ns

**Note:**

The measurement is with the load circuit connected. The load circuit is shown in Fig. 23.



**AC timing for interface with a 68-type microcontroller**



AC timing for interface with a 68-type microcontroller at VDD=5 volts VDD = 5 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t <sub>AS1</sub>	Address set-up time with respect to R/W	20			ns
t <sub>AS2</sub>	Address set-up time with respect to C/D, CS	20			ns
t <sub>AH1</sub>	Address hold time with respect to R/W	10			ns
t <sub>AH2</sub>	Address hold time respect with to C/D, CS	10			ns
t <sub>F</sub> , t <sub>R</sub>	Enable (E) pulse falling/rising time		15		ns
t <sub>CYC</sub>	System cycle time	1000		Note 1	ns
t <sub>EW</sub>	Enable pulse width for READ	100			ns
t <sub>EW</sub>	Enable pulse width for WRITE	80			ns
t <sub>DS</sub>	Data setup time	80			ns
t <sub>DH</sub>	Data hold time	10			ns
t <sub>ACC</sub>	Data access time		90	CL= 100 pF.	ns
t <sub>OH</sub>	Data output hold time	10	60	Refer to Fig. 23.	ns

AC timing for interface with a 68-type microcontroller at VDD=3 volts VDD = 3 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
$t_{AS1}$	Address set-up time with respect to $\overline{R/W}$	40			ns
$t_{AS2}$	Address set-up time with respect to $\overline{C/D}, \overline{CS}$	40			ns
$t_{AH1}$	Address hold time with respect to $\overline{R/W}$	20			ns
$t_{AH2}$	Address hold time respect with to $\overline{C/D}, \overline{CS}$	20			ns
$t_F, t_R$	Enable (E) pulse falling/rising time		15		ns
$t_{CYC}$	System cycle time	2000		Note 1	ns
$t_{EWR}$	Enable pulse width for READ	200			ns
$t_{EWW}$	Enable pulse width for WRITE	160			ns
$t_{DS}$	Data setup time	160			ns
$t_{DH}$	Data hold time	20			ns
$t_{ACC}$	Data access time		180	CL= 100 pF.	ns
$t_{OH}$	Data output hold time	20	120	Refer to Fig. 23.	ns

**Note:**

1. The system cycle time( $t_{CYC}$ ) is the time duration from the time when Chip Enable is enabled to the time when Chip Select is released.

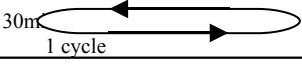
# 12. Quality Assurance

## Screen Cosmetic Criteria

No.	Defect	Judgment Criterion	Partition																				
1	Spots	<p>A)Clear</p> <table border="0"> <tr> <td><u>Size: d mm</u></td> <td><u>Acceptable Qty in active area</u></td> </tr> <tr> <td><math>d \leq 0.1</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.1 &lt; d \leq 0.2</math></td> <td>6</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.3</math></td> <td>2</td> </tr> <tr> <td><math>0.3 &lt; d</math></td> <td>0</td> </tr> </table> <p>Note: Including pin holes and defective dots which must be within one pixel size.</p> <p>B)Unclear</p> <table border="0"> <tr> <td><u>Size: d mm</u></td> <td><u>Acceptable Qty in active area</u></td> </tr> <tr> <td><math>d \leq 0.2</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.2 &lt; d \leq 0.5</math></td> <td>6</td> </tr> <tr> <td><math>0.5 &lt; d \leq 0.7</math></td> <td>2</td> </tr> <tr> <td><math>0.7 &lt; d</math></td> <td>0</td> </tr> </table>	<u>Size: d mm</u>	<u>Acceptable Qty in active area</u>	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	6	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	<u>Size: d mm</u>	<u>Acceptable Qty in active area</u>	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
<u>Size: d mm</u>	<u>Acceptable Qty in active area</u>																						
$d \leq 0.1$	Disregard																						
$0.1 < d \leq 0.2$	6																						
$0.2 < d \leq 0.3$	2																						
$0.3 < d$	0																						
<u>Size: d mm</u>	<u>Acceptable Qty in active area</u>																						
$d \leq 0.2$	Disregard																						
$0.2 < d \leq 0.5$	6																						
$0.5 < d \leq 0.7$	2																						
$0.7 < d$	0																						
2	Bubbles in Polarize	<table border="0"> <tr> <td><u>Size: d mm</u></td> <td><u>Acceptable Qty in active area</u></td> </tr> <tr> <td><math>d \leq 0.3</math></td> <td>Disregard</td> </tr> <tr> <td><math>0.3 &lt; d \leq 1.0</math></td> <td>3</td> </tr> <tr> <td><math>1.0 &lt; d \leq 1.5</math></td> <td>1</td> </tr> <tr> <td><math>1.5 &lt; d</math></td> <td>0</td> </tr> </table>	<u>Size: d mm</u>	<u>Acceptable Qty in active area</u>	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor										
<u>Size: d mm</u>	<u>Acceptable Qty in active area</u>																						
$d \leq 0.3$	Disregard																						
$0.3 < d \leq 1.0$	3																						
$1.0 < d \leq 1.5$	1																						
$1.5 < d$	0																						
3	Scratch	In accordance with spots cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor																				
4	Allowable Density	Above defects should be separated more than 30mm each other.	Minor																				
5	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-light type should be judged with back-light on state only.	Minor																				

# 13. Reliability

## Content of Reliability Test

Environmental Test			
Test Item	Content of Test	Test Condition	Applicable Standard
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	---
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	---
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	---
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	---
High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	80°C,90%RH 96hrs	---
High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	70°C,90%RH 96hrs	---
Temperature Cycle	Endurance test applying the low and high temperature cycle. -30°C                  25°C                  80°C 	-30°C/ 80°C 10 cycles	---
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~55Hz→1.5mmp-p x, y, z Total 1.5hrs	---
Others			
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	---

\*\*\*Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25°C

# 14.Backlight Information

## Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	I <sub>LED</sub>	32	40	60	mA	V=4.2V
Supply Voltage	V	4.0	4.2	4.4	V	
Reverse Voltage	V <sub>R</sub>	-	-	8	V	
Luminous Intensity	I <sub>V</sub>	-	15	-	CD/M <sup>2</sup>	I <sub>LED</sub> =40mA
Wave Length	λ <sub>p</sub>		571		nm	I <sub>LED</sub> =40mA
Life Time	-	-	100K	-	Hr.	I <sub>LED</sub> =40mA
Color	Yellow Green					

**Note: The LED of B/L is drive by current only, drive voltage is for reference only. drive voltage can make driving current under safety area (current between minimum and maximum).**

