SPECIFICATION
FOR
LCD Module
2BM-20050(-TS)

MODULE:	**2BM-20050(-TS)**
CUSTOMER:	

REV	DESCRIPTION	DATE
1	FIRST ISSUE	2011.07.22

	INITIAL	DATE
PREPARED BY		
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Revision History

Data	Rev. No.	Page	Summary
2011.07.22	1.0		FIRST ISSUE

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General Description

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 5.0" TFT-LCD contains 800 x 480 pixels, and can display up to 262K colors.

* Features

-Low Input Voltage: VDD: 5.0V
-Display Colors of TFT LCD: 262K colors
-CPU Interface: 8080 parallel 16 bit
-Internal Power Supply Circuit.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	108.0(H) *64.8(V) (5.0 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	262K	colors	-
Number of pixels	800(RGB) *480	dots	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.198 (H) x 0.198 (V)	mm	-
Viewing angle	6：00	o'clock	-
Controller IC	KD45789	-	-
Display mode	Transmissive/ Normally White	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		121		mm	-
	Vertical(V)		76		mm	-
	Depth(D)		15.2		mm	-
Weight			TBD		g	-

1. Optical Characteristics

1.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Threshold voltage		Vsat		—	2.4	—		(6)
		Vth		—	1.4	—		(6)
Transmittance (With PZ)		T		—	6.78	—		
Contrast		CR	Θ=0 Normal viewing angle	480	600	—		(1)(2)
Response time	Rising	T_R		—	3	6	msec	(1)(3)
	Falling	T_F		—	7	14		
Color gamut		S		—	50	—	%	C light
Color chromaticity (CIE1931)	White	W_x		0.292	0.307	0.322		(1)(4) CF Glass C light
		W_y		0.333	0.348	0.363		
	Red	Rx		0.616	0.631	0.646		
		Ry		0.327	0.342	0.357		
	Green	Gx		0.306	0.321	0.336		
		Gy		0.538	0.553	0.568		
	Blue	Bx		0.134	0.149	0.164		
		By		0.168	0.183	0.198		
Viewing angle	Hor.	Θ_L	CR>10	65	75	—		
		Θ_R		65	75	—		
	Ver.	Θ_U		50	60	—		
		Θ_D		60	70	—		
Optima View Direction		6 O' clock						(5)

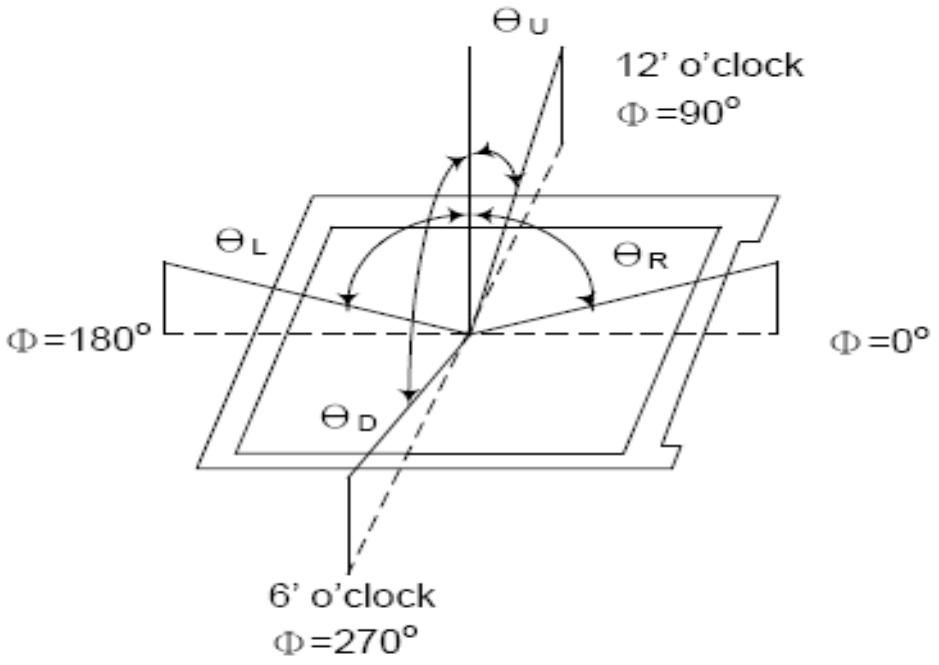
1.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: 25±2oC
- 15min. warm-up time.

1.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.
- Measuring spot size: 20 ~ 21 mm

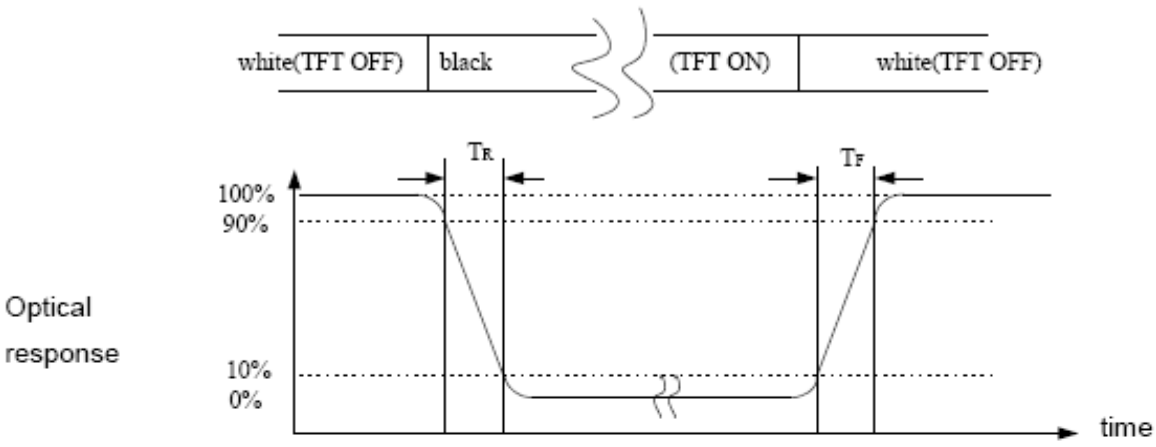
Note (1) Definition of Viewing Angle:



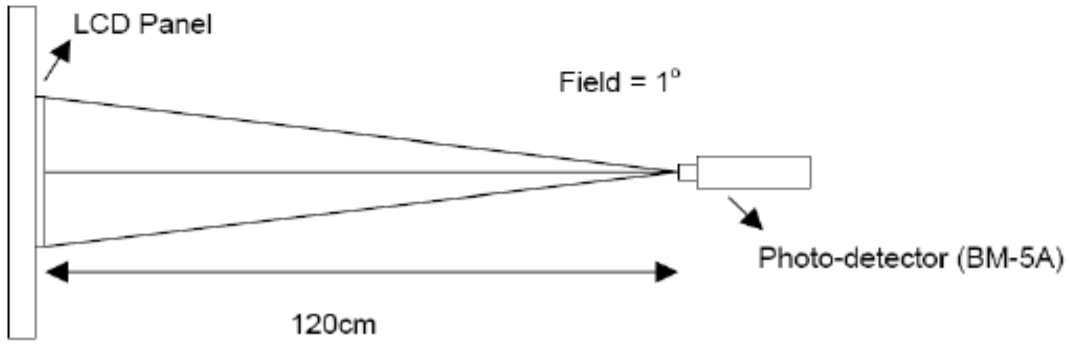
Note (2) Definition of Contrast Ratio (CR):
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time: Sum of T_R and T_F

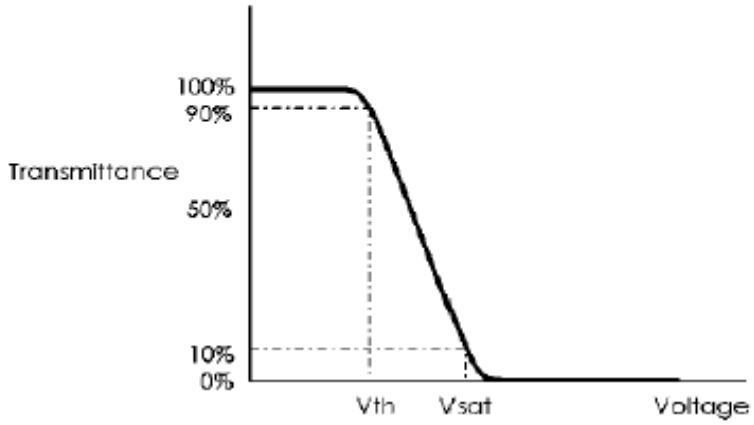


Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optimal view direction.

Note (6) Definition of Vsat and Vth (at 20^{0}C)



2. Electrical Characteristics

2.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
LCD Interface power supply	V_{DD_LCD}	-0.5	-	6	V	
I/O power supply	V_{DDDIO}	-0.5	-	6	V	
Input Voltage	V_{IN}	-0.5	-	6		
Output Voltage	V_{OUT}	-0.5		46		
Operating temperature	T_{OP}	−20		+70	℃	
Storage temperature	T_{ST}	−30		+80	℃	

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VIN and VOUT be constrained to the range VSS < (VIN or VOUT) < VDDIO. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

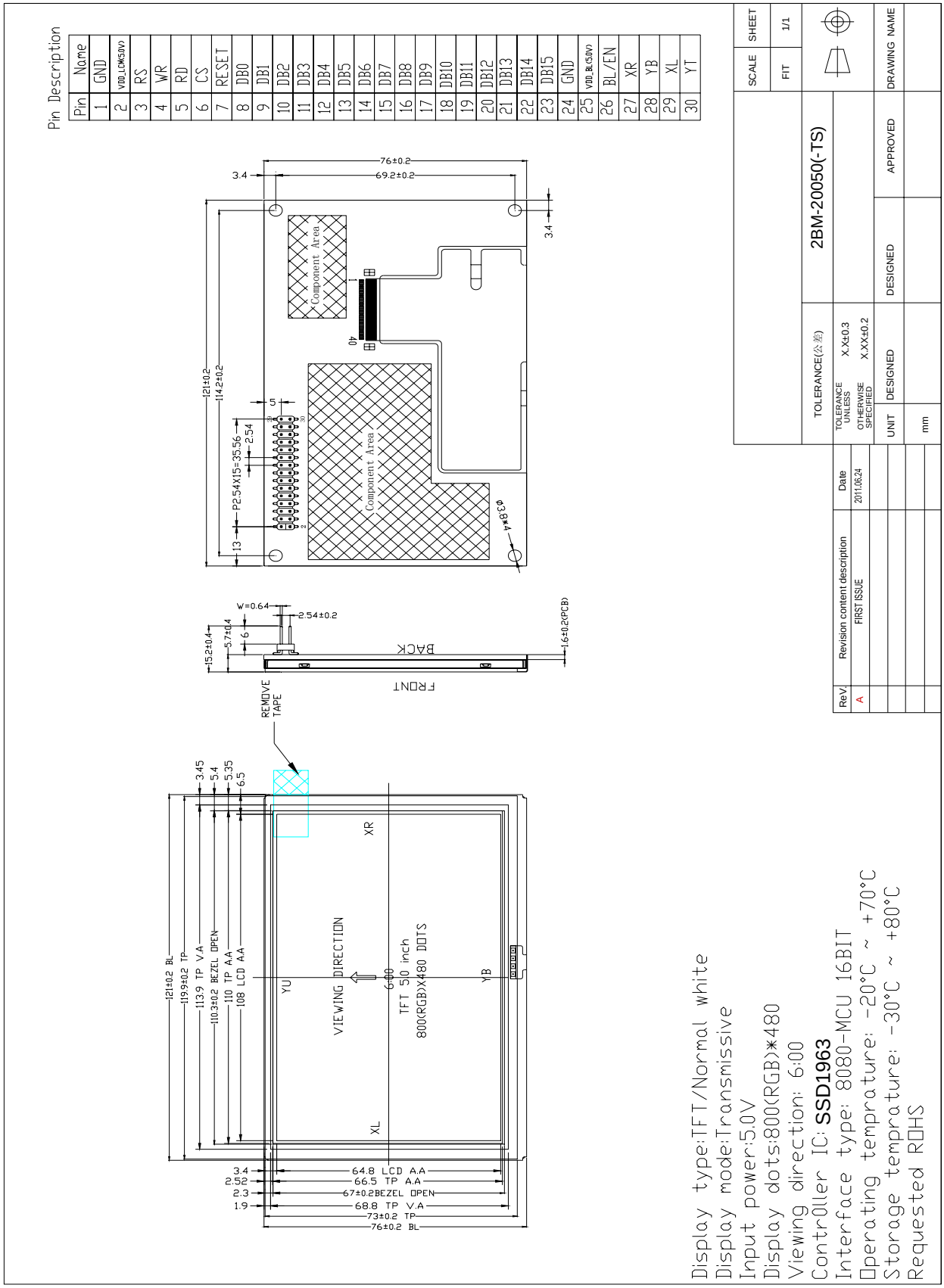
2.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
System voltage	Vcc	4.5	5.0	5.5	V	
Normal mode Current consumption	Vcc_I		350		mA	
Level input voltage	V_{IH}	0.8V_{DDIO}		–	V	
	V_{IL}	–		0.2V_{DDIO}	V	
Level output voltage	V_{OH}	0.8V_{DDIO}		–	V	
	V_{OL}	–		0.2V_{DDIO}	V	

2.3 LED Backlight Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LCM Luminance	L_V		250	–	cd/m2	
Uniformity	AVg	80	–	–	%	–

3. Outline dimension



4. Input terminal Pin Assignment

Pin NO.	Symbol	Typ	Function
1	GND	P	Ground.
2	VDD_LCM	P	Power supply for LCM +5v
3	RS	I	Data/Command select.
4	WR	I	write strobe signal.
5	RD	I	read strobe signal.
6	CS	I	Chip select.
7	RESET	I	Master synchronize reset.
8-23	DB0-DB15	I/O	Data bus. Pins not used should be floating.
24	GND		Ground.
25	VDD_BL		Power supply for BL +5v
26	BL/EN	I	Backlight Enable Control Input.
27	XR		Touch panel coordinate(Right)
28	YB		Touch panel coordinate(Down)
29	XL		Touch panel coordinate(Left)
30	YT		Touch panel coordinate(Up)

5. Operating Principle & Methods

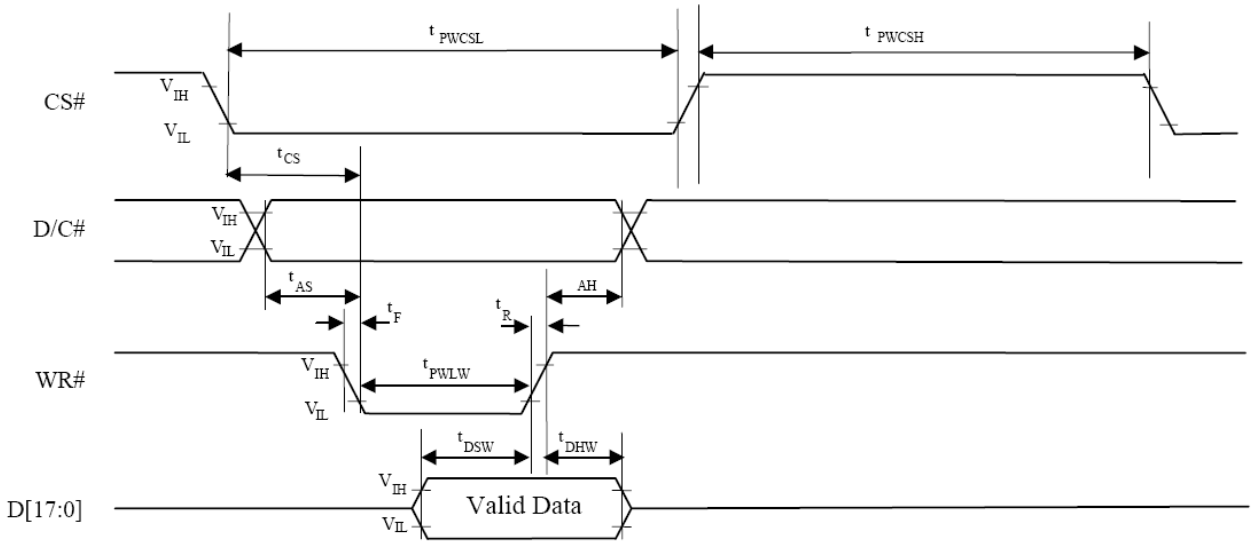
Please refer to SSD1963 datasheet for more details.80-System Bus operation Interface Timing Characteristics .

5.1 Parallel 8080-series Interface Timing Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
f_{MCLK}	System Clock Frequency*		1	-	110	MHz
t_{MCLK}	System Clock Period*		$1/f_{MCLK}$	-	-	ns
t_{PWCSL}	Control Pulse High Width	Write Read	13 30	$1.5* t_{MCLK}$ $3.5* t_{MCLK}$	-	ns
t_{PWCSH}	Control Pulse Low Width	Write (next write cycle) Write (next read cycle) Read	13 80 80	$1.5* t_{MCLK}$ $9* t_{MCLK}$ $9* t_{MCLK}$	-	ns
t_{AS}	Address Setup Time		1	-	-	ns
t_{AH}	Address Hold Time		2	-	-	ns
t_{DSW}	Write Data Setup Time		4	-	-	ns
t_{DHW}	Write Data Hold Time		1	-	-	ns
t_{PWLW}	Write Low Time		12	-	-	ns
t_{DHR}	Read Data Hold Time		1	-	-	ns
t_{ACC}	Access Time		32	-	-	ns
t_{PWLR}	Read Low Time		36	-	-	ns
t_R	Rise Time		-	-	0.5	ns
t_F	Fall Time		-	-	0.5	ns
t_{CS}	Chip select setup time		2	-	-	ns
t_{CSH}	Chip select hold time to read signal		3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

5.2 Parallel 8080-series Interface Timing Diagram (Write Cycle)



5.3 Parallel 8080-series Interface Timing Diagram (Read Cycle)