Crystalfontz America, Inc.

CUSTOMER		
MODEL	**CFAX12864A-NFH**	
APPROVAL	**BY:**	**DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

Crystalfontz America, Inc.
12412 East Saltese Avenue
Spokane Valley, WA 99216-0357

Phone: (888) 206-9720
Fax: (509) 892-1203
Email: techinfo@crystalfontz.com
URL: www.crystalfontz.com

Contents

1.Module Classification Information

CFA X 1 2 8 6 4 A - N F H

① ② ③ ④ ⑤⑥ ⑦

①	Brand：CRYSTALFONTZ AMERICA, INCORPORATED		
②	Display Type：H→Character Type, G→Graphic Type, **X→TAB**		
③	Display's logical dimensions: **128** pixels by **64** pixels		
④	Model serials no.		
⑤	Backlight Type：	**N→Without backlight** B→EL, Blue green D→EL, Green W→EL, White F→CCFL, White Y→LED, Yellow Green	 A→LED, Amber R→LED, Red O→LED, Orange G→LED, Green
⑥	LCD Mode：	B→TN Positive, Gray N→TN Negative, G→STN Positive, Gray Y→STN Positive, Yellow Green M→STN Negative, Blue **F→FSTN Positive**	T→FSTN Negative
⑦	LCD Polarizer Type/ Temperature range/ View direction	A→Reflective, N.T, 6:00 D→Reflective, N.T, 12:00 G→Reflective, W. T, 6:00 J→Reflective, W. T, 12:00 B→Transflective, N.T,6:00 E→Transflective, N.T.12:00	**H→Transflective, W.T,6:00** K→Transflective, W.T,12:00 C→Transmissive, N.T,6:00 F→Transmissive, N.T,12:00 I→Transmissive, W. T, 6:00 L→Transmissive, W.T,12:00
⑧	Special Code		

2.Precautions in use of LCD Modules

(1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
(2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
(3) Don't disassemble the LCM.
(4) Don't operate it above the absolute maximum rating.
(5) Don't drop, bend or twist LCM.
(6) Soldering: only to the I/O terminals.
(7) Storage: please storage in anti-static electricity container and clean environment.

3.General Specification

Item	Dimension	Unit
Number of Dots	128*64	
Module dimension(w/o TAB)	34.0x 24.22x 1.8(max)	mm
View area	29.58x 17.98	mm
Active area	25.58x 15.98	mm
Dot size	0.18x 0.23	mm
Dot pitch	0.20x 0.25	mm
LCD type	FSTN, positive, transflective	
Duty	1/64	
View direction	6 o'clock	

4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	-	+70	℃
Storage Temperature	T_{ST}	-30	-	+80	℃
Input Voltage	V_I	V_{SS}	-	V_{DD}	V
Supply Voltage For Logic	V_{DD}-V_{SS}	2.4	-	5.5	V
Supply Voltage For LCD	V_O-V_{SS}	4.0	-	15.0	V

5.Electrical Characteristics

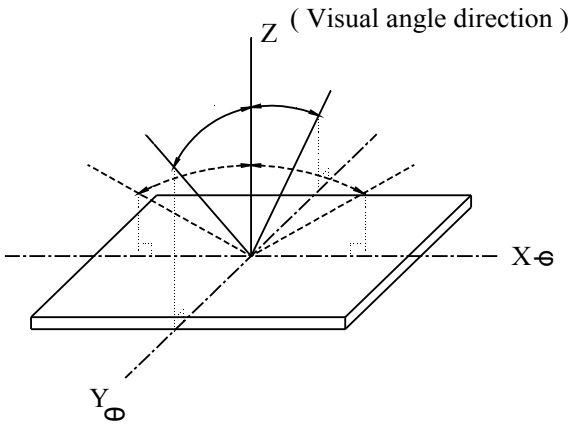
Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	-	2.4	-	5.5	V
Supply Voltage For LCD	V_{DD}-V_0	Ta=-20℃	-	-	9.2	V
		Ta=25℃				V
		Ta=70℃		8.2	-	V
			-			
			7.2	-	-	
Input High Volt.	V_{IH}	-	0.8 V_{DD}	-	V_{DD}	V
Input Low Volt.	V_{IL}	-	-	-	0.2 V_{DD}	V
Output High Volt.	V_{OH}	-	V_{DD} -0.4	-	-	V
Output Low Volt.	V_{OL}	-	-	-	0.4	V
Supply Current	I_{DD}	V_{DD}=5V	-	1.5	-	mA

6.Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V)θ	CR≧2	10	-	40	deg
	(H)φ	CR≧2	-30	-	30	deg
Contrast Ratio	CR	-	-	5	-	-
Response Time	T rise	-	-	110	220	ms
	T fall	-	-	260	520	ms

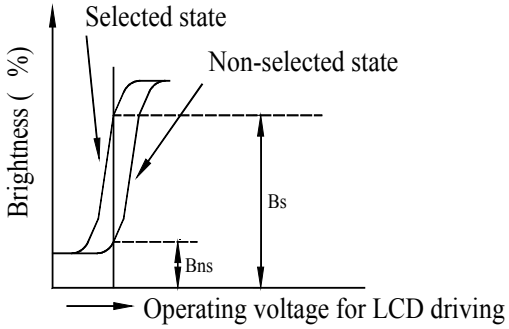
6.1 Definitions

■View Angles



■Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



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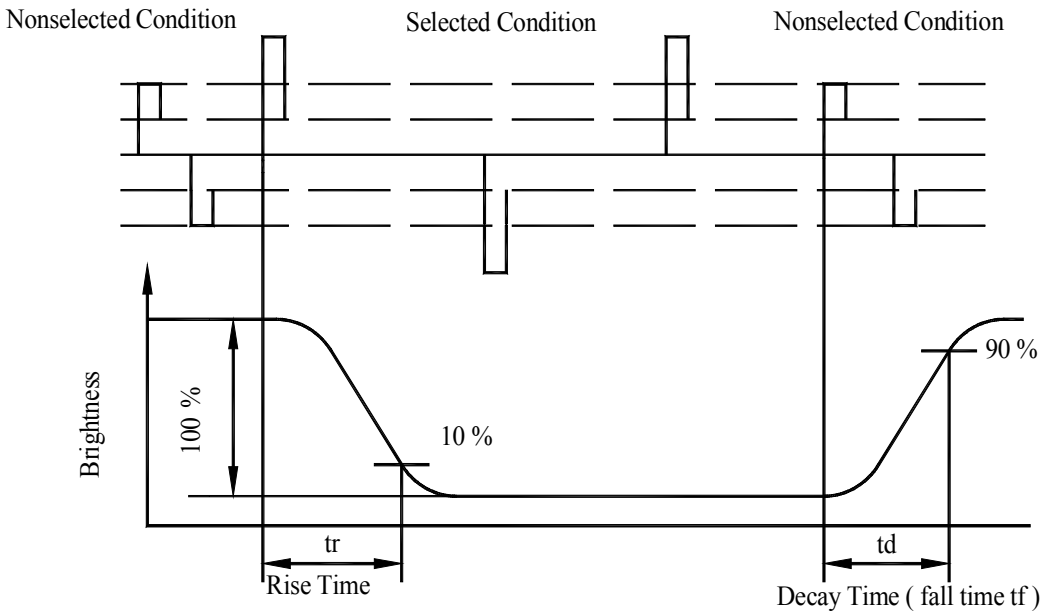
■ Response Time



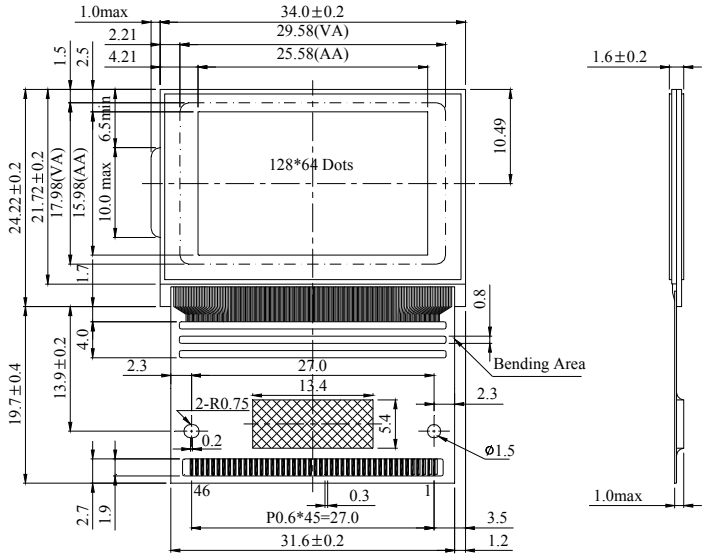
7.Interface Description

Pin No.	Symbol	I/O	Description
1	NC	-	No connection
2	TEMPS	I	Selects temperature coefficient of the reference voltage TEMPS="L": -0.05%℃, TEMPS="H": -0.2%℃
4	HPM	I	Power control pin of the power supply circuit for LCD driver. HPM="H": high power mode HPM="L": normal power mode This pin is valid in master operation.
5	DCDC5B	I	5times boosting circuit enable input pin. When this pin is low in 4 times boosting circuit, the 5-time boosting voltage appears at VOUT.
6	BSTS	I	Select input voltage of the built-in voltage converter. Voltage converter input BSTS="L": 4V (VDD>4V) BSTS="H": VDD (2.4V≦VDD≦3.6V) When BSTS pin is "L", VDD must be higher than 4V in four times boosting. NOTE: Because the maximum voltage of VDD has been changed to 3.6V, we strongly recommend that BSTS pin should be fixed to " H" .
7~11	V0~V4	I/O	LCD driver supply voltages. The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relational; V0≧V1≧V2≧V3≧V4≧VSS
12	VR	I	V0 voltage adjustment pin. It is valid only when on-chip resistors are not used(INTRS="L")
13	C2-	O	Capacitor 2 negative connection pin for voltage converter.
14	C2+	O	Capacitor 2 positive connection pin for voltage converter.
15	C1-	O	Capacitor 1 negative connection pin for voltage converter.
16	C1+	O	Capacitor 1 positive connection pin for voltage converter.
17	C3-	O	Capacitor 1 negative connection pin for voltage converter.
18	C3+	O	Capacitor 1 positive connection pin for voltage converter.
19	VOUT	I/O	Voltage converter input/output pin.
20	VDD	-	Power supply pin for logic.
21	VSS	-	Ground pin, connected to 0V

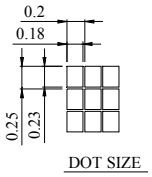
22	PS	I	Parallel/Serial data input select pin. Interface Data Read/Write Serial clock PS="H": Parallel DB0~DB7 E_RD,RW_WR - PS="L": Serial SID(DB7) Write only SCLK(DB6) In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either "H" or "L".
23	MI	I	Microprocessor interface selects pin. MI="H": 6800-series MPU interface MI="L": 8080-series MPU interface
24	CLS	I	Built-in oscillator circuit enable/disable select pin. CLS="H": enable CLS="L": disable(external display clock input from CL pin)
25	MS	I	Master or Slave mode operation select pin. MS="H" : master operation MS="L" : slave operation
26 27	DUTY1 DUTY0	I	The LCD driver duty ratio depends on the following table DUTY1 DUTY0 Duty ratio L L 1/33 L H 1/49 H L 1/65
28~35	DB7~DB0	I/O	8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected(PS="L") DB0~DB5: high impedance DB6: serial input clock (SCLK) DB7: serial input data (SID) When chip select is not active, DB0~DB7 may be high impedance.
36	E_RD	I	When connected to 80-family MPU: Read enable clock input pin. When /RD is "L", DB0~DB7 are in an output status When connected to 68-family MPU: RW = "H": When E is "H", DB0~DB7 are in an output status RW = "L": The data on DB0~DB7 are latched at the falling edge of the E signal
37	RW_WR	I	When connected to 80-family MPU: Write enable clock input pin. The data ON DB0~DB7 are latched at the rising edge of the /WR signal. When connected to 68-family MPU: RW = "H": read RW = "L": write
38	RS	I	Register select pin RS="H": DB0~DB7 are display data RS="L": DB0~DB7 are control data
39	RESETB	I	Reset input pin When RESETB is "L", initialization is executed.
40 41	CS2 CS1B	I	Chip select input pins Data/instruction I/O enable only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0~DB7 may be high impedance.

42	DISP	I/O	LCD display blanking control input /output When KS0713 is used in master/slave mode (multi-chip), the DISP pins must be connected each other. MS=”H”: output MS=”L”: input
43	CL	I/O	Display clock input/output pin When the KS0713 is used in master/slave mode (multi-chip), the CL pins must be connected each other.
44	M	I/O	LCD AC signal input /output pin When KS0713 is used in master/slave mode (multi-chip), the M pins must be connected each other. MS=”H”: output MS=”L”: input
45	FRS	O	Static driver segment output pin This pin is used together with the M pin.
46	NC	-	No connection.

8.Contour Drawing & Block Diagram



42	DISP	21	Vss	PIN NO.	SYMBOL
43	CL	22	PS	1	NC
44	M	23	MI	2	TEMPS
45	FRS	24	CLS	3	INTRS
46	NC	25	MS	4	HPM
		26	DUTY1	5	DCDC5B
		27	DUTY0	6	BSTS
		28	DB7	7	V4
		29	DB6	8	V3
		30	DB5	9	V2
		31	DB4	10	V1
		32	DB3	11	V0
		33	DB2	12	VR
		34	DB1	13	C2-
		35	DB0	14	C2+
		36	E_RD	15	C1-
		37	RW_WR	16	C1+
		38	RS	17	C3-
		39	RESETB	18	C3+
		40	CS2	19	Vout
		41	CS1B	20	Vdd



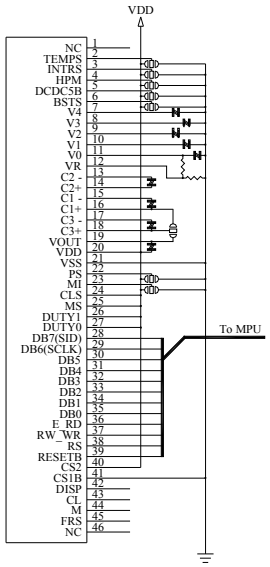
DOT SIZE

The non-specified tolerance of diemnsion is ±0.15mm.

Display Data RAM

Page Address P3,P2,P1,P0	Data	RAM address	Line Address (HEX)	Com Output
0,0,0,0	DB0		00	COM1
	DB1		01	COM2
	DB2		02	COM3
	DB3		03	COM4
	DB4		04	COM5
	DB5		05	COM6
	DB6		06	COM7
	DB7		07	COM8
≀			≀	≀
0,1,1,1	DB0		38	COM57
	DB1		39	COM58
	DB2		3A	COM59
	DB3		3B	COM60
	DB4		3C	COM61
	DB5		3D	COM62
	DB6		3E	COM63
	DB7		3F	COM64
0,1,1,1	DB0		40	COM65

Column Address	ADC=0	83	82	81	80	7F	7E	7D	7C	7B	7A	≀	5	4	3	2	1	0
	ADC=1	0	1	2	3	4	5	6	7	8	9	≀	7E	7F	80	81	82	83
Segment Output		132	131	130	129	128	127	126	125	124	123	≀	6	5	4	3	2	1



Application Circuit

Boosting Circuit