ePAPER DISPLAY MODULE DATASHEET

Datasheet Release 2017-08-16
for
CFAP200200A0-0154

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1. General Information

Datasheet Revision History
Datasheet Release Date: **2017-08-16** Datasheet for the CFAP200200A0-0154 ePaper display module.

Product Change Notifications
You can check for or subscribe to Part Change Notices for this display module on our website.

Variations
Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility
This display module has volatile memory.

Disclaimer
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2. Description Overview

This ePaper display is a TFT active matrix electrophoretic display with interface and a reference system design. The 1.54" active area contains 200×200 pixels and has 1-bit full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

3. Features

- High contrast
- High reflectance
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-Stable Display
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On-chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating V_{COM}, Gate and source driving voltage
- Available in COG package IC thickness 300um

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.54	inch	
Display Resolution	200 × 200	pixel	dpi: 184
Active Area	27.6 × 27.6	mm	
Pixel Pitch	0.138 × 0.138	mm	
Pixel Configuration	Square	-	
Outline Dimension	37.32 (H) x 31.8 (W) x 1.05 (D)	mm	
Weight (Typical)	4±0.5	g	

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Type	Single	Description	Remark
1		NC	No Connection and Do Not Connect with Other NC Pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate Driving Voltage	
5	C	VGH	Positive Gate Driving Voltage	
6	-	NC	Keep Open	
7	O	NC	Keep Open	
8	I	BS1	Bus Selection Pin	Note 5-5
9	O	BUSY	Busy State Output Pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command Control Pin	Note 5-2
12	I	CS #	Chip Select Input Pin	Note 5-1
13	I/O	D0	Serial Clock Pin (SPI)	
14	I/O	D1	Serial Data Pin (SPI)	
15	I	VDDIO	Power for Interface Logic Pins	
16	I	VCI	Power Supply Pin for the Chip	
17		VSS	Ground	
18	C	VDD	Core Logic Power Pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source Driving Voltage	
21	C	PREVGH	Power Supply Pin for VGH and VSH	
22	C	VSL	Negative Source Driving Voltage	
23	C	PREVGL	Power Supply Pin for VCOM, VGL, and VSL	
24	C	VCOM	VCOM Driving Voltage	

Note (5-1): This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note (5-2): This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note (5-3): This pin (RES#) is reset signal input. The Reset is active Low.

Note (5-4): This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting Display Waveform; or
- Programming with OTP
- Communicating with Digital Temperature Sensor

Note (5-5): This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to table below.

Bus Interface Selection

BS1	MPU Interface
L	4-Lines Serial Peripheral Interface (SPI)
H	3-Lines Serial Peripheral Interface (SPI) – 9 bits SPI

6. Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output Control	Gate Setting: A[8:0]: MUX setting as A[8:0] + 1 POR = 12Bh + 1 MUX B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…G299 (left and right gate interlaced) SM=1, G0, G2, G4, …G178, G1, G3, …G299 B[0]: TB TB = 0 [POR], scan from G0 to G299 TB = 1, scan from G299 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft Start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current setting. A[7:0] -> Soft start setting for Phase1 = 87h [POR] B[7:0] -> Soft start setting for Phase2 = 86h [POR] C[7:0] -> Soft start setting for Phase3 = 85h [POR]
0	1		1	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		1	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		1	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	0	0F	0	0	0	0	1	1	1	1	Gate Scan Start Position	Set the scanning start position of the gate driver. The valid range is from 0 to 299. When TB=0: SCN [8:0] = A[8:0] A[8:0] = 000h [POR] When TB=1: SCN [8:0] = 299 - A[8:0] A[8:0] = 000h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep Mode	Deep Sleep Mode Control A[0]: Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	1		0	0	0	0	0	0	0	A_0		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	11	0	0	0	1	0	0	0	1	Data Entry Mode Setting	Define data entry sequence. A[1:0] = ID[1:0] Address automatic increment / decrement setting. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 Y decrement, X decrement, 01 Y decrement, X increment, 10 Y increment, X decrement, 11 Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data is written to the RAM. When AM= 0, the address counter is updated in the X direction. [POR] When AM = 1, the address counter is updated in the Y direction.
0	1	-	0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to Temperature Register)	Write to Temperature Register. A[7:0] MSByte 01111111[POR] B[7:0] LSByte 11110000[POR]
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	-	B_7	B_6	B_5	B_4	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence. The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Display Update Control 1</td><td>Option for Display Update
Bypass Option used for Pattern Display, which is used for display the RAM content into the Display.

OLD RAM Bypass option
A[7]
A[7] = 1: Enable bypass
A[7] = 0: Disable bypass [POR]

A[4] value will be used as New RAM for bypass.
A[4] = 0 [POR]

A[1:0] Initial Update Option - Source Control

<table><tr><td>A[1:0]</td><td>GSA</td><td>GSB</td></tr><tr><td>01[POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A_7</td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update Control 2</td><td>Display Update Sequence Option:
Enable the stage for Master Activation
Remarks:

<table><tr><td></td><td>Parameter (in Hex)</td></tr><tr><td>Enable Clock Signal,
Then Enable CP
Then Load Temperature Value
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable CP
Then Disable OSC</td><td>FF [POR]</td></tr><tr><td>To Enable Clock Signal (CLKEN=1)</td><td>80</td></tr><tr><td>To Enable Clock Signal, then Enable CP (CLKEN=1, CPEN=1)</td><td>C0</td></tr><tr><td>To INITIAL DISPLAY + PATTERN DISPLAY</td><td>0C</td></tr><tr><td>To INITIAL DISPLAY</td><td>08</td></tr><tr><td>To DISPLAY PATTERN</td><td>04</td></tr><tr><td>To Disable CP, then Disable Clock Signal (CLKEN=1)</td><td>03</td></tr><tr><td>To Disable Clock Signal (CLKEN=1)</td><td>01</td></tr></table>
CLKEN = 1:
If CLS=VDDIO then Enable OSC
If CLS=VSS then Enable External Clock
CLKEN=0:
If CLS=VDDIO then Disable OSC AND INTERNAL CLOCK Signal = VSS</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td></td><td></td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
0	0	2C	0	0	1	0	1	0	1	1	Write VCOM Register	Write VCOM Register from MCU Interface
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT Register	Write LUT register from MCU [240 bits], (excluding the VSH/VSL and Dummy bit).
0	1	LUT [30 bytes]										
0	1											
0	1											
…	…											
0	1											
0	1											
0	0	3A	0	0	1	1	1	0	1	0	Set Dummy Line Period	Set number of dummy line period. A[6:0]: Number of dummy line period in terms of TGate A[6:0] =16h [POR] Available setting 0 to 127.
0	1	-	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7] Follow Source at Initial Update Display A[7]=0: [POR] A[7]=1: Follow Source at Initial Update Display for VBD, A [6:0] settings are being overridden at Initial Display STAGE. A[6] Select GS Transition/ Fix Level for VBD A[6]=0: Select GS Transition A[3:0] for VBD A[6]=1: Select FIX level Setting A[5:4] for VBD [POR] A[5:4] Fix Level Setting for VBD A[5:4] / VBD level 00 / VSS 01 / VSH 10 / VSL 11[POR] / HiZ A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) A[1:0] / GSA / GSB 01[POR] / GS0 / GS1
0	1	-	A_7	A_6	A_5	A_4	0	0	A_1	A_0		

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - Address Start / End Position	Specify the start/end positions of the window address in the X direction by an address unit. A[4:0]: XSA[4:0], XStart, POR = 00h B[4:0]: XEA[4:0], XEnd, POR = 18h
0	1	-	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1	-	0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- Address Start / End Position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 12Bh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X - Address Counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h
0	1	-	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y - Address Counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: XAD[8:0], POR is 000h
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	-	0	0	0	0	0	0	0	A_8		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read Commands.

7. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.5 to +3.6	V
Logic Input Voltage	V_{IN}	-0.5 to V_{CI}+0.5	V
Logic Output Voltage	V_{OUT}	-0.5 to V_{CI}+0.5	V
Operation Temperature Range	T_{OPR}	0 to +50	°C
Storage Temperature Range	T_{STG}	-25 to +70	°C
Humidity Range	RH	40~70	%
IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.			

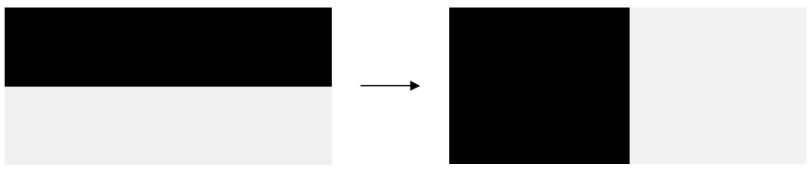
8. Panel DC Characteristics

The following specifications apply for V_{SS}=0V, V_{CI}=3.0V, T_a=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Single Ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	V_{CI}	-	2.4	3.3	3.7	V
High Level Input Voltage	V_{IH}	-	0.8V_{CI}	-	-	V
Low Level Input Voltage	V_{IL}	-	-	-	0.2V_{CI}	V
High Level Output Voltage	V_{OH}	I_{OH}= -100uA	0.9V_{CI}	-	-	V
Low Level Output Voltage	V_{OL}	I_{OH}= 100uA	-	-	0.1V_{CI}	V
Image Update Current	I_{UPDATE}	-	-	8	10	mA
Standby Panel Current	$I_{STANDBY}$	-	-	-	5	uA
Power Panel（Update）	P_{UPDATE}	-	-	26.4	-	mW
Standby Power Panel	P_{STBY}	-	-	-	0.0165	mW
Operating Temperature	-	-	0	-	50	°C
Storage Temperature	-	-	-25	-	70	°C
Image Update Time at 25°C	-	-	-	680	-	ms
Partial Image Update Time at 25°C	-	-	-	280	-	ms
Deep Sleep Mode Current	V_{CI}	DC/DC Off No Clock No Input Load Ram Data Not Retained	-	2	5	uA
Sleep Mode Current	V_{CI}	DC/DC Off No Clock No Input Load Ram Data Retained	-	35	50	uA

The typical power consumption is measured with the following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern, shown below.

Note: The standby power is the consumed power when the panel controller is in standby mode. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz. VCOM is recommended to be set in the range of the assigned value: ± 0.1V.



9. Panel AC Characteristics

9.1. Oscillator Frequency

The following specifications apply for V_{SS}=0V, V_{CI}=3.0V, T_a=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Internal Oscillator Frequency	F_{OSC}	V_{CI}=2.4 to 3.7V	0.95	1	1.05	MHz

9.2. MCU Interface Selection

In this module, there is 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI), is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus Interface	D1	D0	CS#	D/C#	RES#
SPI 4	SD_{IN}	SCLK	CS#	D/C#	RES#
SPI 3	SD_{IN}	SCLK	CS#	L	RES#

Note: L is connected to V_{SS}. H is connected to V_{CI}.

9.3. MCU Serial Interface (4-Wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SD_{IN}.

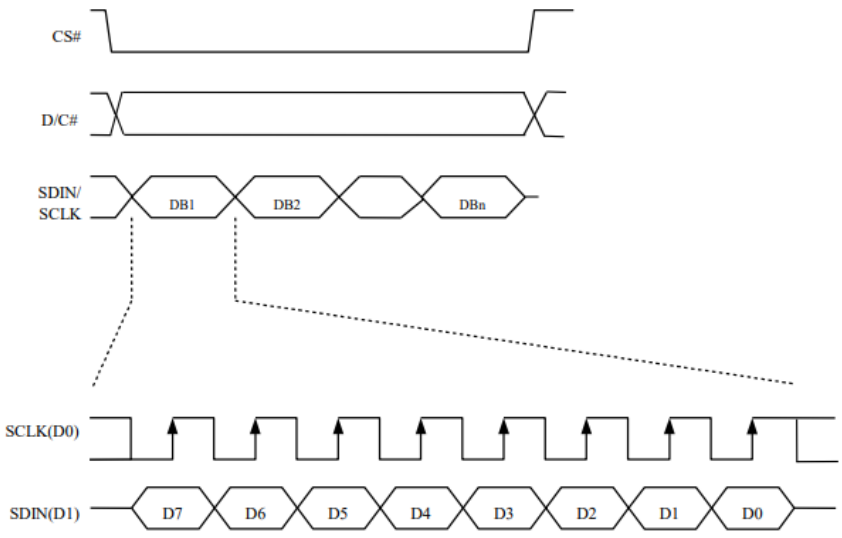
Control Pins of 4-Wire Serial Peripheral Interface:

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write Data	L	H	↑

Note: “ ↑ ” stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Write Procedure in 4-Wire Serial Peripheral Interface Mode:



9.4. MCU Serial Interface (3-Wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SD_{IN}. The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. Altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data), will determine the following data byte when shift register is written to the Display Data RAM (D/C# bit = 1), or the command register (D/C# bit = 0). Only write operations are allowed under serial mode.

Control Pins of 3-Wire Serial Peripheral Interface:

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write Data	L	Tie LOW	↑

Note: " ↑ " stands for rising edge of signal

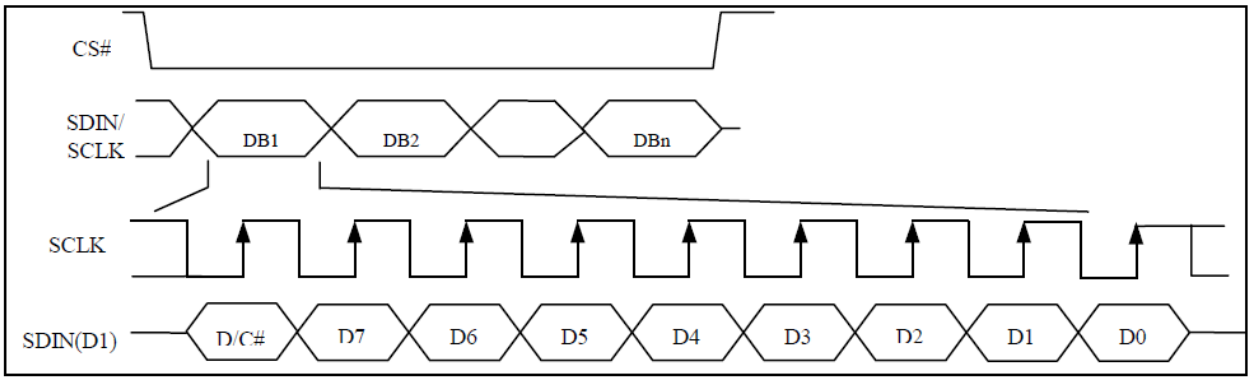


Figure 9-1: Write Procedure in 3-Wire Serial Peripheral Interface Mode

10. Timing Characteristics of Series Interface

(V_{CI}-V_{SS}=1.8V to 2.0V, T_a=25℃, CL=20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Clock Cycle Time	t_{cycle}	250	-	-	ns
Address Setup Time	t_{AS}	150	-	-	ns
Address Hold Time	t_{AH}	150	-	-	ns
Chip Select Setup Time	t_{CSS}	120	-	-	ns
Chip Select Hold Time	t_{CSH}	60	-	-	ns
Write Data Setup Time	t_{DSW}	50	-	-	ns
Write Data Hold Time	t_{DHW}	15	-	-	ns
Clock Low Time	t_{CLKL}	100	-	-	ns
Clock High Time	t_{CLKH}	100	-	-	ns
Rise Time (20%~80%)	t_R	-	-	15	ns
Fall Time (20%~80%)	t_F	-	-	15	ns

Table 10-1: Serial Peripheral Interface Timing Characteristics

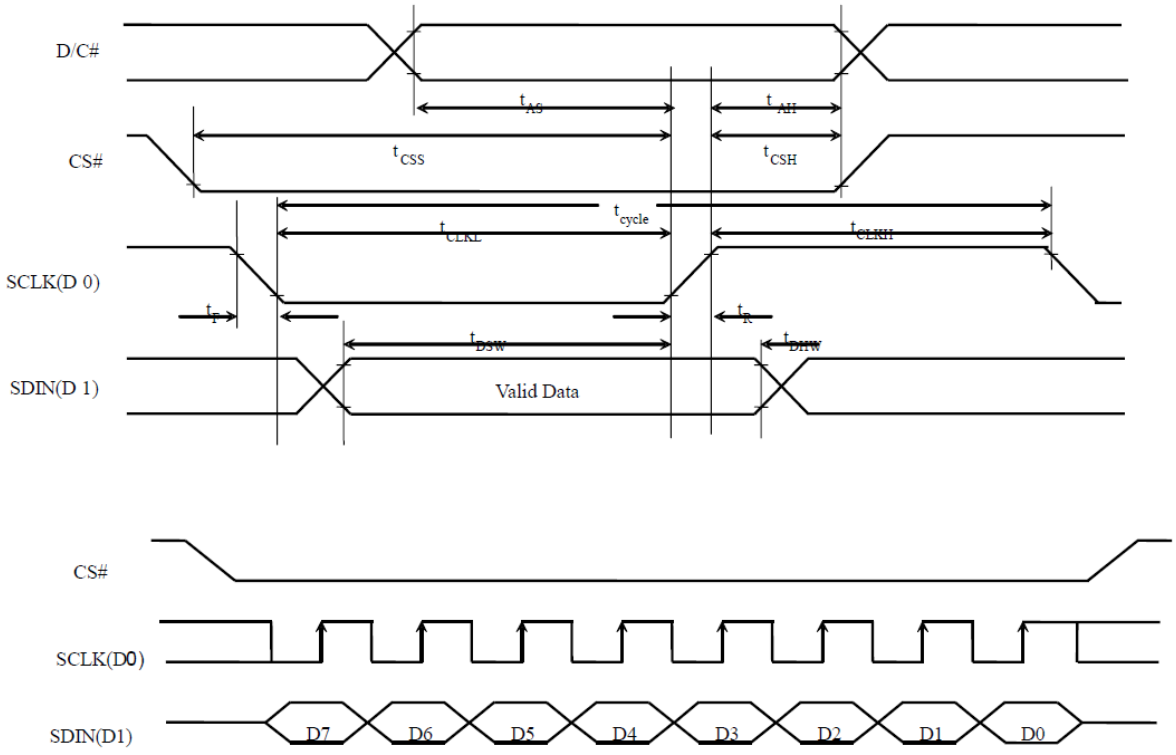


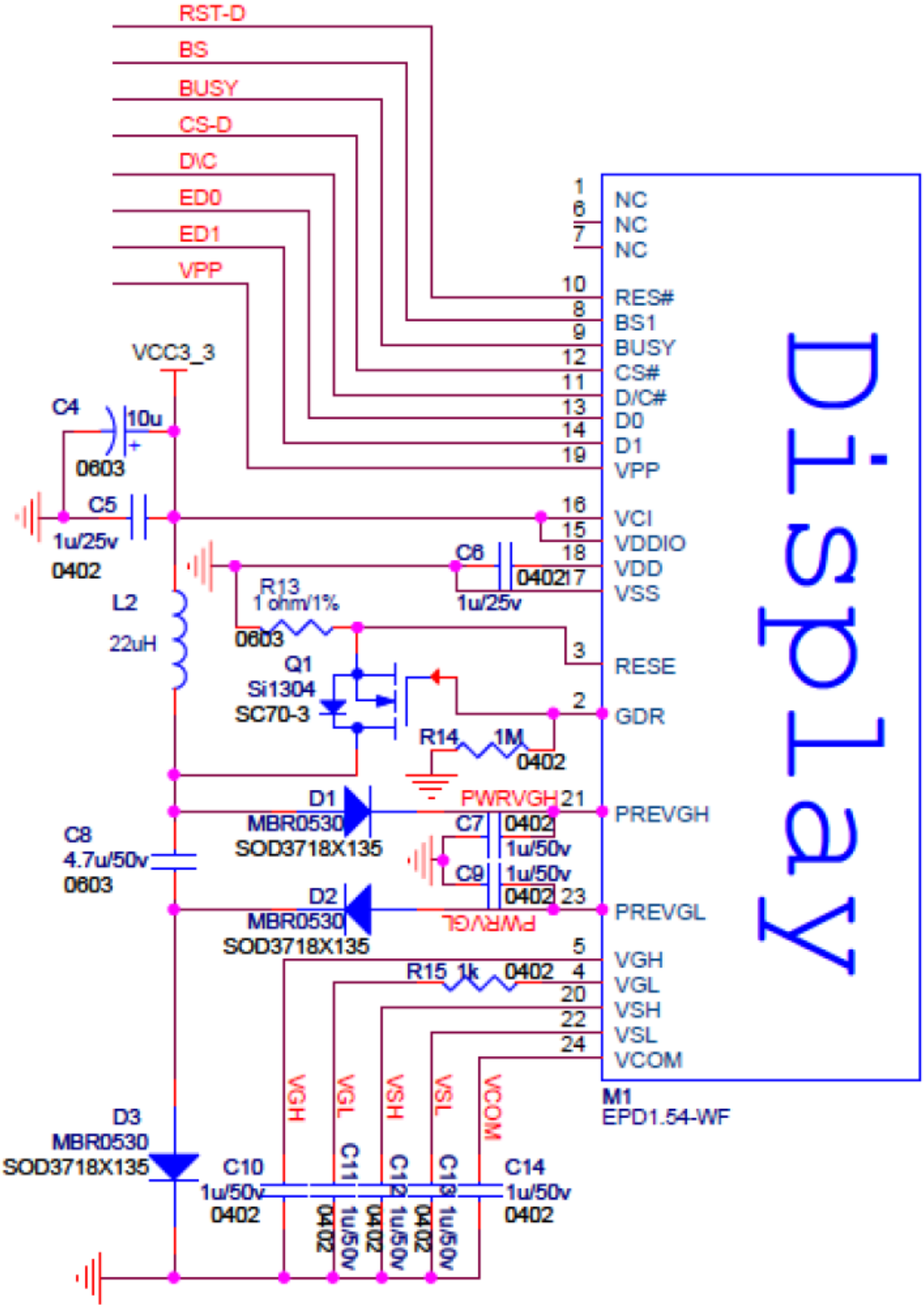
Figure 10-2: Serial Peripheral Interface Characteristics

10.1. Power Consumption

Parameter	Symbol	Condition	Typ	Max	Unit
Panel Power Consumption During Update	-	-	26.4	40	mW
Power Consumption in Standby Mode	-	-	-	0.017	mW

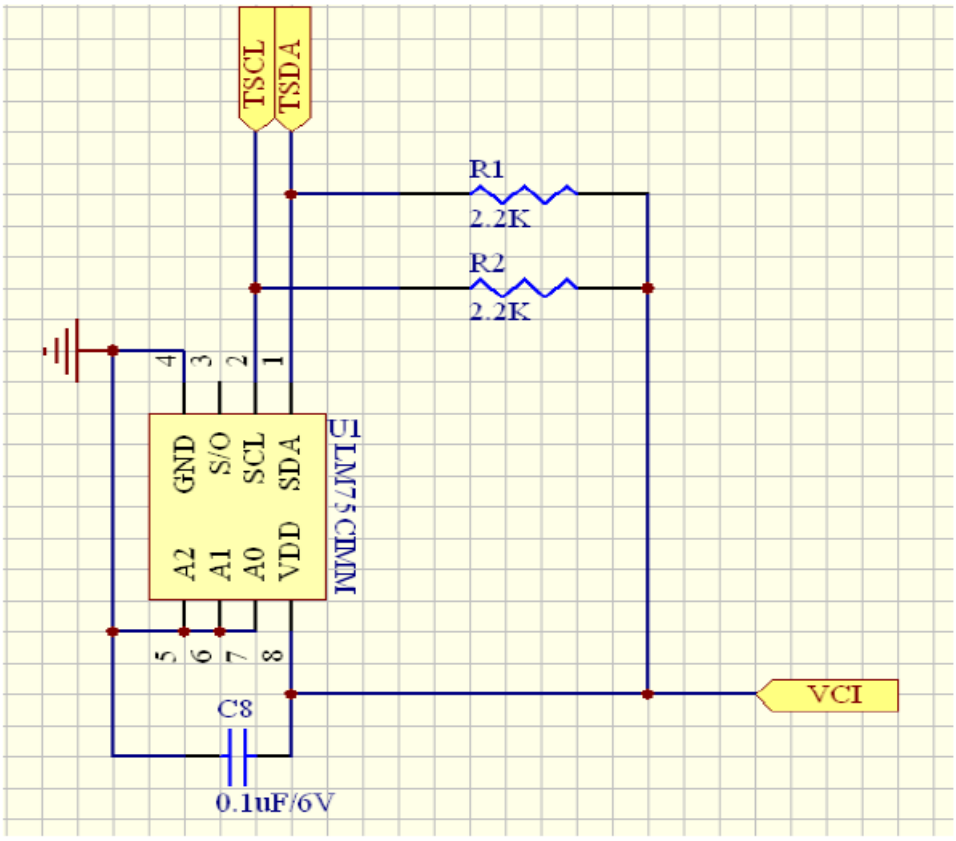
11. Reference Circuit

11.1. Reference Circuit for Panel

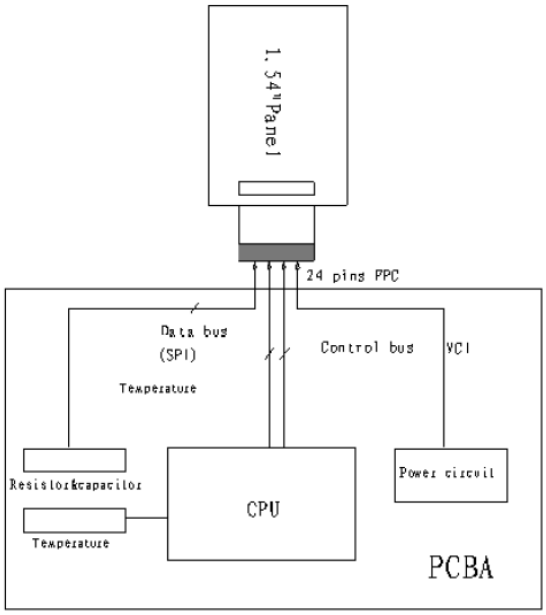


11.2. Reference Circuit for Temperature Sensor

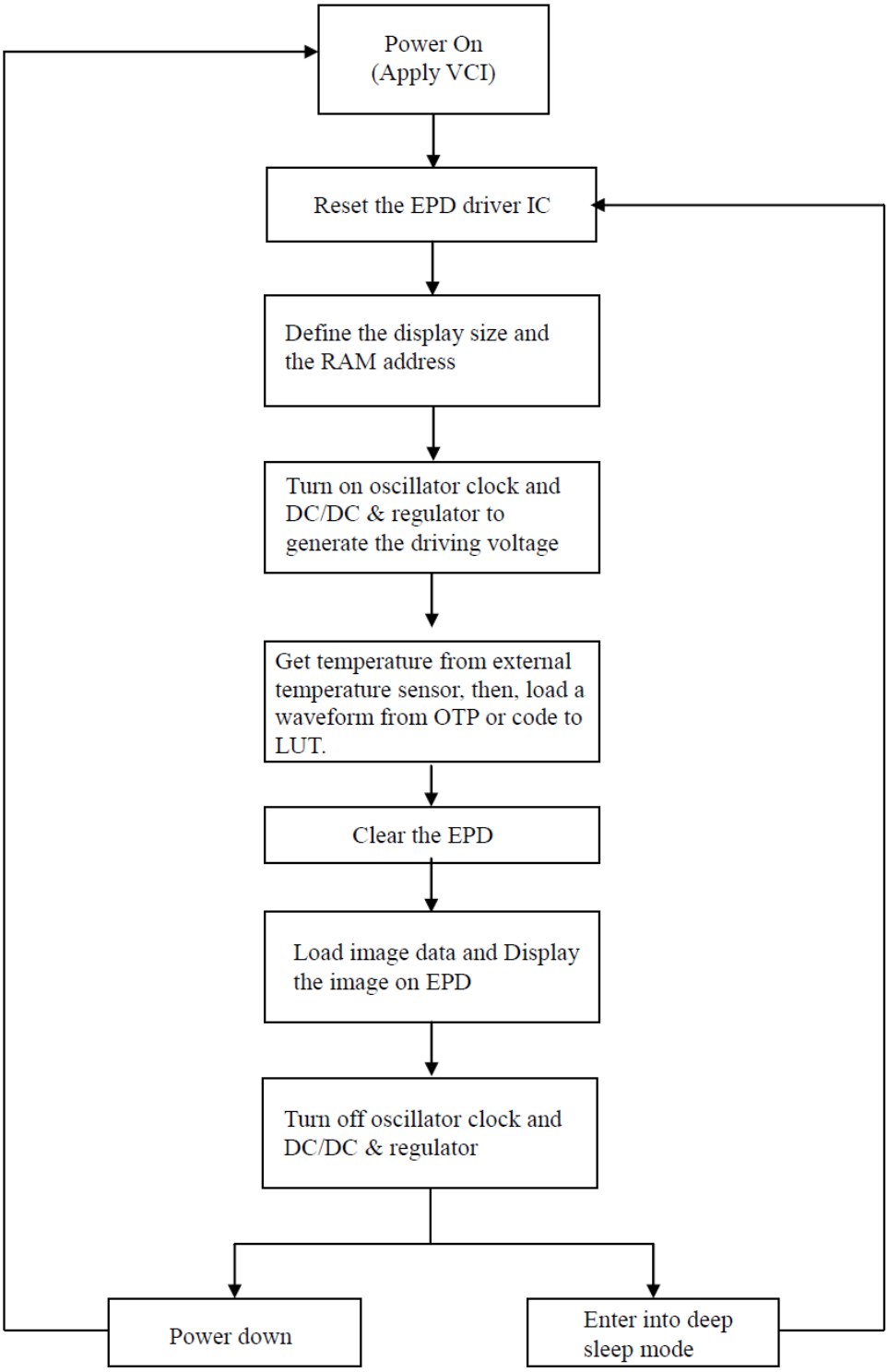
Temperature Sensor I²C bus needs to be connected with CPU.



12. Block Diagram



13. Typical Operating Sequence



14. Optical Characteristics

14.1. Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 14-1
Gn	2Gray Level	-	-	DS+(WS-DS) ^{x}n(m-1)	-	L*	-
CR	Contrast Ratio	Indoor	8		-	-	-
Panel Life	-	0°C~50°C	-	1,000,000 times or 5 years	-	-	Note 14-2

WS: White State, DS: Dark State

Gray State from Dark to White: DS, WS

m: 2

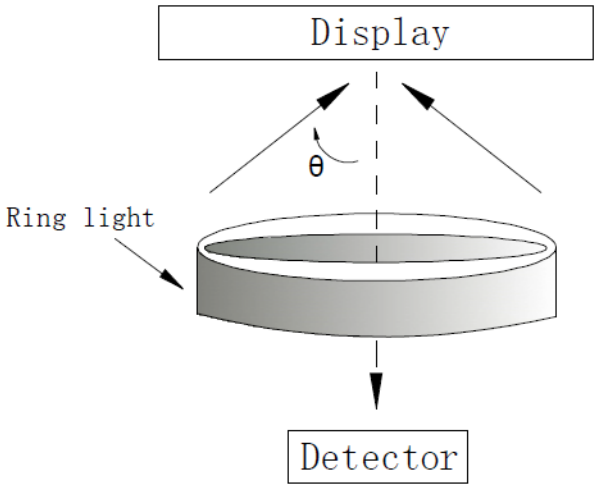
Note (14-1): Luminance Meter: Eye – One Pro Spectrophotometer
Note (14-2): Panel life is not guaranteed when working in temperatures below 0 degrees or above 50 degrees.

14.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

CR = R1/Rd

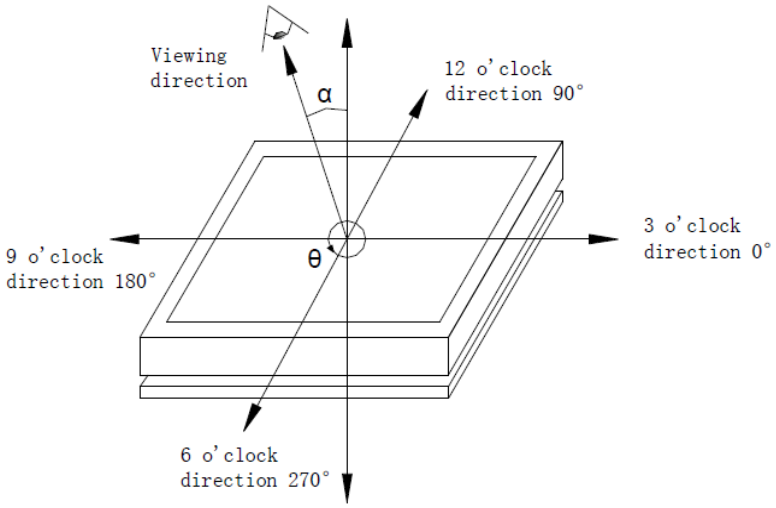


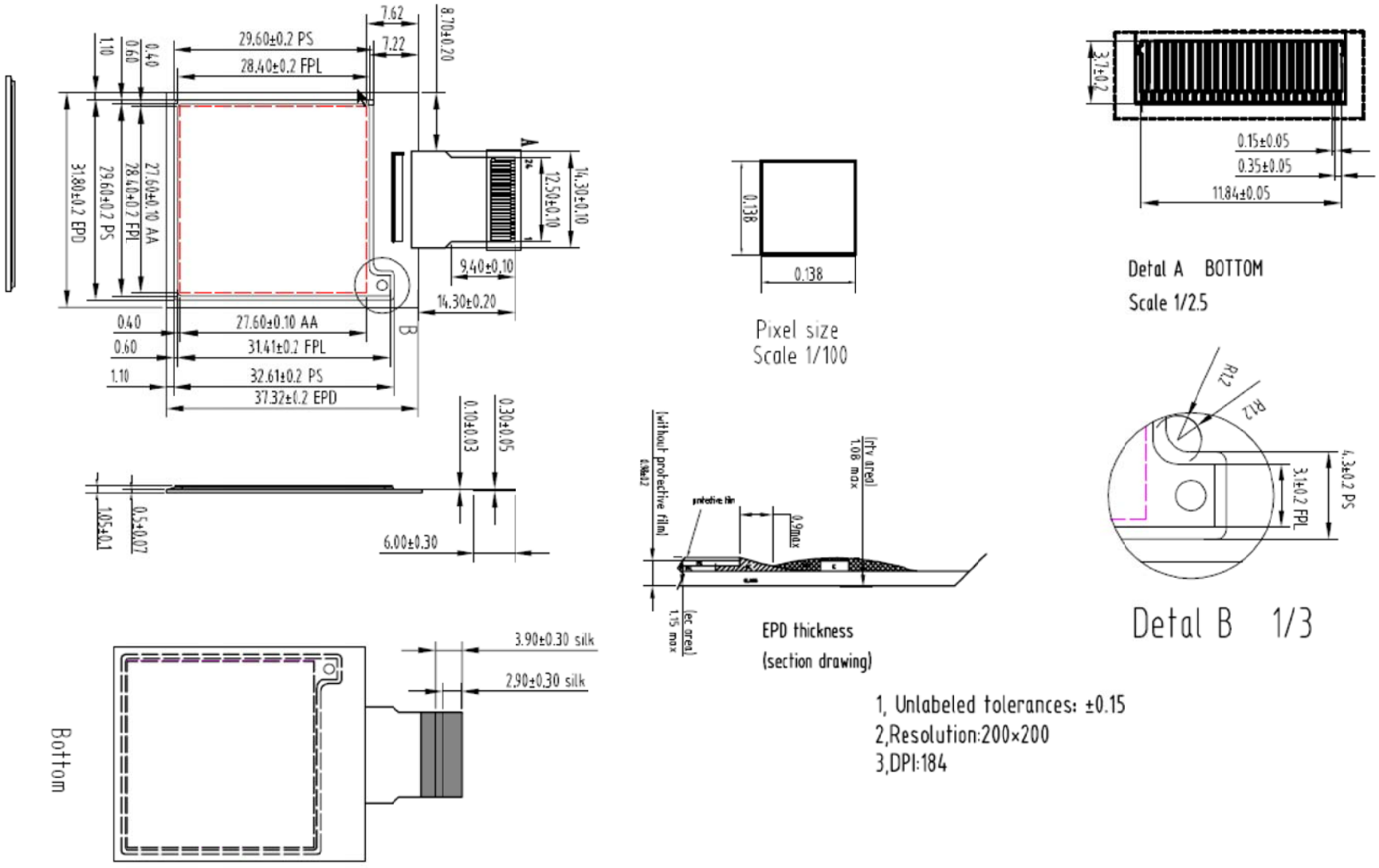
14.3. Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{WHITE BOARD}} \times (L_{\text{CENTER}} / L_{\text{WHITE BOARD}})$

L_{CENTER} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{WHITE BOARD}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.





Crystalfontz	PART NUMBER(S) CFAP200200A0-0154	SCALE Not to Scale	
	DRAWING NUMBER CFAP200200A0-0154 master	UNITS Millimeters	DATE 2017-08-16

16. ePaper Breakout Board Schematic