DISPLAY MODULE DATASHEET

Datasheet Release 2016-06-24
for
CFAP104212B0-0213

Crystalfontz America, Incorporated

12412 East Saltese Avenue
Spokane Valley, WA 99216-0357

Phone: 888-206-9720
Fax: 509-892-1203
Email: support@crystalfontz.com
URL: www.crystalfontz.com

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GENERAL INFORMATION

Datasheet Revision History

Datasheet Release: 2016-06-24
First datasheet for a new product, the CFAP104212B0-0213 display module.

Product Change Notifications

To check for Product Change Notifications for this display module, see the Product Notices tab on a product's web page. Product pages without a Product Notices tab do not have Product Change Notifications.

About Variations

Slight variations (for example, contrast, color, or intensity) between lots are normal.

The Fine Print

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OVERVIEW, FEATURES, & MECHANICAL SPECIFICATIONS

1. Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 2.13" active area contains 212×104 pixels, and has 1-bit black/white and highlight red full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

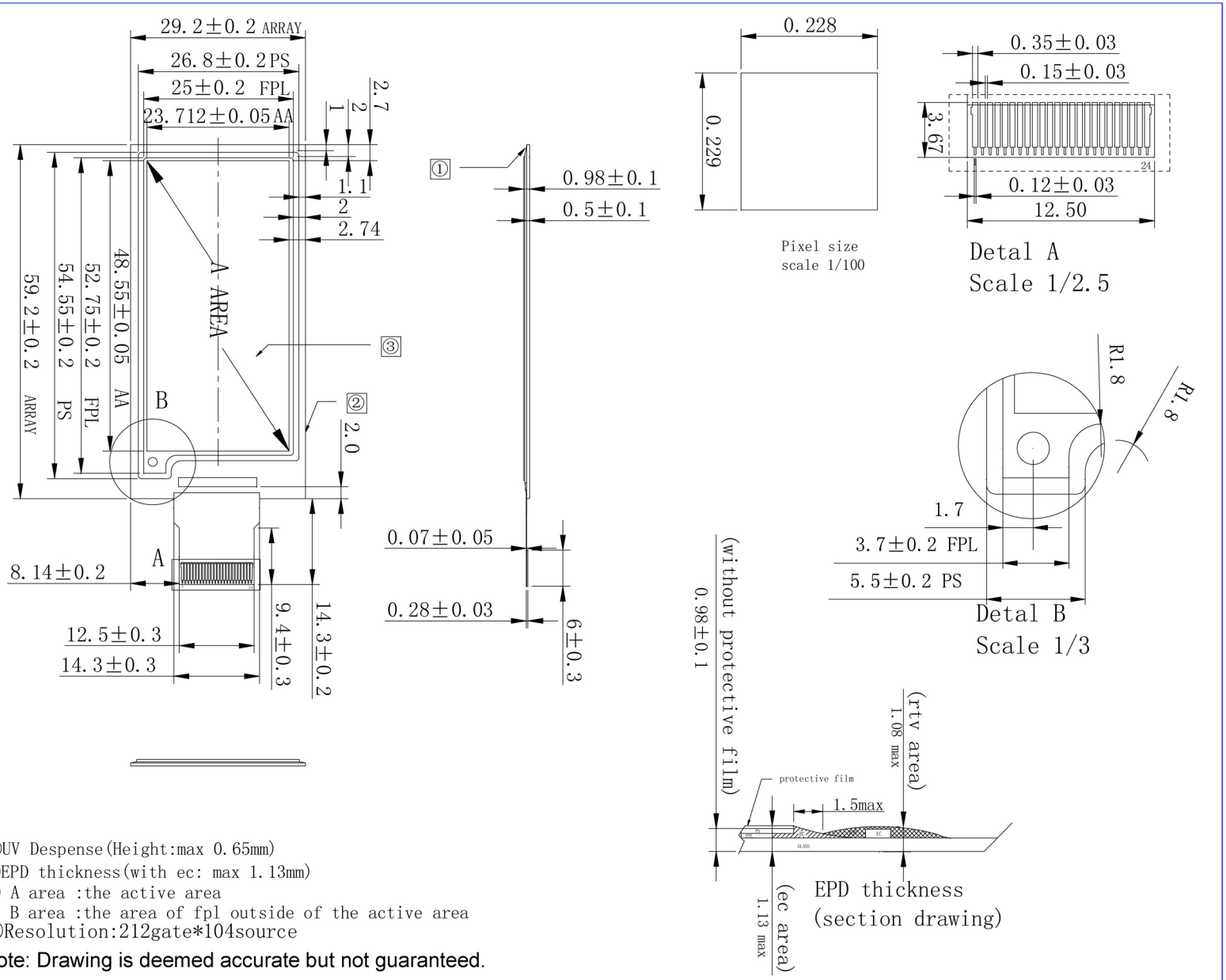
2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 300um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	212(H)×104(V)	Pixel	Dpi:111
Active Area	48.55 (H)×23.80 (V)	mm	
Pixel Pitch	0.229×0.228	mm	
Pixel Configuration	Rectangle		
Outline Dimension	59.2(H)×29.2 (V) ×0.98(D)	mm	
Weight	3.36±0.5	g	

MODULE OUTLINE



①UV Despense(Height:max 0.65mm)
②EPD thickness(with ec: max 1.13mm)
③ A area :the active area
B area :the area of fpl outside of the active area
④Resolution:212gate*104source

Note: Drawing is deemed accurate but not guaranteed.

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Part No.(s):	Scale:	Drawing Number:	Hardware Rev.:
CFAP104212B0-0213	1:1	CFAP	
	Units: Millimeters	Date: 2016-06-23	Sheet: 1 of 1

PIN DESCRIPTIONS

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I^2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I^2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 5-5
9	O	BUSY	Busy state output pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command control pin	Note 5-2
12	I	CS #	Chip Select input pin	Note 5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19		NC	No connection and do not connect with other NC pins	Keep Open
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled High, the

data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

COMMAND TABLE

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R01H	**PWR**	W	0	0	0	0	0	0	0	0	1	(01H)
	1st Para	W	1	-	-	-	-	**RVSHLS**	**RVSHLS**	**VDS_EN**	**VDG_EN**	03H
	2ndPara	W	1	-	-	-	-	-	-	0	0	00H
	3ndPara	W	1				VDPS_LV4	VDPS_LV3	VDPS_LV2	VDPS_LV1	VDPS_LV0	08H
	4ndPara	W	1				VDNS_LV4	VDNS_LV3	VDNS_LV2	VDNS_LV1	VDNS_LV0	08H
R02H	**POF**	W	0	0	0	0	0	0	0	1	0	(02H)
R04H	**PON**	W	0	0	0	0	0	0	1	0	0	(04H)
R06H	**BTST**	W	0	0	0	0	0	0	1	1	0	(06H)
	1st Para	W	1	-	0	0	**BT_PHA4**	**BT_PHA3**	1	1	1	0FH
	2ndPara	W	1	-	0	0	**BT_PHB4**	**BT_PHB3**	1	1	0	0EH
	3rd Para	W	1	-	-	-	**BT_PHC4**	**BT_PHC3**	1	0	1	0DH
R10H	**DTM1**	W	0	0	0	0	1	0	0	0	0	(10H)
	1st Para	W	1	**KPxl1[0]**	**KPxl2[1]**	**KPxl2[0]**	**KPxl3[1]**	**KPxl3[0]**	**KPxl4[1]**	**KPxl4[0]**	**KPxl1[1]**	00H
	……	W	1									00H
	MthPara	W	1	KPxl(N-1)[1]	KPxl(N-1)[0]	KPxlN[1]	KPxlN[0]					00H
R12H	**DRF**	W	0	0	0	0	1	0	0	1	0	(12H)
R13H	**DTM2**	W	0	0	0	0	1	0	0	1	1	(13H)
	1st Para	W	1	PRxl1	PRxl2	PRxl3	PRxl4	PRxl5	PRxl6	PRxl7	PRxl8	00H
	……	W	1									00H
	Mth Para	W	1	PRxl(N-1)	PRxlN							00H

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R30H	**PLL**	W	0	0	0	1	1	0	0	0	0	(30H)
	1st Para	W	0	-	-	M2	M1	M0	N2	N1	N0	3CH
R40H	**TSC**	W	0	0	1	0	0	0	0	0	0	(40H)
	1st Para	R	1	D10	D9	D8	D7	D6/TS3	D5/TS2	D4/TS1	D3/TS0	00H
	2nd Para	R	1	D2	D1	D0	-	-	-	-	-	00H
R41H	**TSE**	W	0	0	1	0	0	0	0	0	1	(41H)
	1st Para	W	1	TSE	-	-	-	-	-	-	-	00H
R42H	**TSW**	W	0	0	1	0	0	0	0	1	0	(42H)
	1st Para	W	1	WATTR7	WATTR6	WATTR5	WATTR4	WATTR3	WATTR2	WATTR1	WATTR0	00H
	2nd Para	W	1	WMSB7	WMSB6	WMSB5	WMSB4	WMSB3	WMSB2	WMSB1	WMSB0	00H
	3rd Para	W	1	WLSB7	WLSB6	WLSB5	WLSB4	WLSB3	WLSB2	WLSB1	WLSB0	00H
R43H	**TSR**	W	0	0	1	0	0	0	0	1	1	(43H)
	1st Para	R	1	RMSB7	RMSB6	RMSB5	RMSB4	RMSB3	RMSB2	RMSB1	RMSB0	00H
	2nd Para	R	1	RLSB7	RLSB6	RLSB5	RLSB4	RLSB3	RLSB2	RLSB1	RLSB0	00H
R50H	**CDI**	W	0	0	1	0	1	0	0	0	0	(50H)
	1st Para	W	1	-	-	-	DDX	CDI3	CDI2	CDI1	CDI0	17H
R61H	**TRES**	W	0	0	1	1	0	0	0	0	1	(61H)
	1st Para	W	1	HRES7	HRES6	HRES5	HRES4	HRES3	HRES2	HRES1	0	00H
	2nd Para	W	1	-	-	-	-	-	-	-	VRES8	00H
	3rd Para	W	1	VRES7	VRES6	VRES5	VRES4	VRES3	VRES2	VRES1	VRES0	00H
R82H	**VDCS**	W	0	1	0	0	0	0	0	1	0	(82H)
	1st Para	W	1	-	-	VDCS5	VDCS4	VDCS3	VDCS2	VDCS1	VDCS0	00H

Power Setting Register

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R01H	**PWR**	W	0	0	0	0	0	0	0	0	1	(01H)
	1st Para	W	1	-	-	-	-	RVSHLS	RVSHLS	VDS_EN	VDG_EN	03H
	2nd Para	W	1	-	-	-	-	-	-	0	0	00H
	3rd Para	W	1	-	-	-	VDPS_LV4	VDPS_LV3	VDPS_LV2	VDPS_LV1	VDPS_LV0	08H
	4th Para	W	1	-	-	-	VDNS_LV4	VDNS_LV3	VDNS_LV2	VDNS_LV1	VDNS_LV0	08H

RVSHLS[1:0]: Source power selection

RVSHLS[1:0]	VSH	VSL
00	+2.4 ~ +8.0V	-2.4 ~ -8.0V
01	+2.4 ~ +8.0V	-15V
10	+15V	-2.4 ~ -8.0V
11	+15V	-15V

Name	Control	Value	Function Description
VDS_EN	Source Power Selection	0	External positive source voltage from VDH pin and negative source voltage from VDL pin
		1	Internal voltage generation circuit for both VDH/VDL
VDG_EN	Gate Power Selection	0	External positive source voltage from VDH pin and negative source voltage from VDL pin
		1	Internal voltage generation circuit for both VDH/VDL
VDPS_LV[4:0]	Source Voltage Level(Red)	-	Internal positive source voltage level for red LUT (range: 2.4V ~ 8.0V / step:0.2V)
VDNS_LV[4:0]	Source Voltage Level(Red)	-	Internal negative source voltage level for red LUT (range: -2.4V ~ -8.0V / step:0.2V)

Note: For this panel the 2nd Para must set as 0x00.

Power OFF

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R02H	**POF**	W	0	0	0	0	0	0	0	1	0	(02H)

After the Power Off command, driver will power off based on the power off Sequence, BUSY will become “0”. This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

SD output and Vcom will base on previous condition. It may have 2 conditions: 0V or floating.

This command can be active only when BUSY = “1”.

Power ON / Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R04H	**PON**	W	0	0	0	0	0	0	1	0	0	(04H)
R06H	**BTST**	W	0	0	0	0	0	0	1	1	0	(06H)
	1st Para	W	1	-	0	0	BT_PHA4	BT_PHA3	1	1	1	0FH
	2nd Para	W	1	-	0	0	BT_PHB4	BT_PHB3	1	1	0	0EH
	3rd Para	W	1	-	-	-	BT_PHC4	BT_PHC3	1	0	1	0DH

Name	Control	Value	Description	
BT_PHA[4:3] BT_PHB[4:3] BT_PHC[4:3]	Driving Strength	00	1	↓
		01	2	
		10	3	
		11	4	

NOTE: For this panel, You 'd better to set these bits's (BT_PHA \BT_PHB\BT_PHC) value to 00.

Data Start Transmission 1 / Data Stop Command (B/W)

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R10H	**DTM1**	W	0	0	0	0	1	0	0	0	0	(10H)
	1st Para	W	1	KPixel1[1:0]		KPixel2[1:0]		KPixel3[1:0]		KPixel4[1:0]		00H
		W	1	…		…		…		…		00H
	Mth Para	W	1	KPixel(n-1)[1:0]		KPixel(n)[1:0]		-	-	-	-	00H

This Command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

	KPixel(x)[1:0]	LUT
When DDX=0	00	White
	11	Black
When DDX=1	00	Black
	11	White

This command can be active only when BUSY = "1".

Data Refresh Command

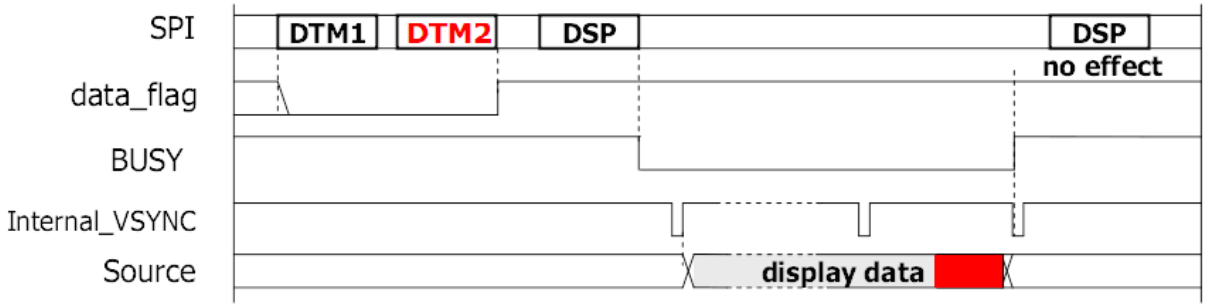
Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R12H	**DRF**	W	0	0	0	0	1	0	0	1	0	(12H)

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

This command can be active only when BUSY ="1". After display refresh command, BUSY signal will become "0".

Data Start Transmission 1&2 / Data Stop Command (B/W/Red)

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R13H	**DTM2**	W	0	0	0	0	1	0	0	1	1	(13H)
	1st Para	W	1	PRxl1	PRxl2	PRxl3	PRxl4	PRxl5	PRxl6	PRxl7	PRxl8	00H
	……	W	1									00H
	Mth Para	W	1	PRxl(N-1)	PRxlN							00H



1. <data_flag>=1 while writing both DTM1 and DTM2 parameters fully (B/W/Red)
2. SEG/BG/VCOM change based on internal frame clock

PLL Control

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R30H	**PLL**	W	0	0	0	1	1	0	0	0	0	(30H)
	1st Para	W	0	-	-	M2	M1	M0	N2	N1	N0	3CH

Note: For this panel the R30H Must be set as follow:

When Temperature ≥30 value=0x39;

When Temperature ＜30 value=0x2A.

Temperature Sensor Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R40H	**TSC**	W	0	0	1	0	0	0	0	0	0	(40H)
	1st Para	R	1	D10	D9	D8	D7	D6/TS3	D5/TS2	D4/TS1	D3/TS0	00H
	2nd Para	R	1	D2	D1	D0	-	-	-	-	-	00H

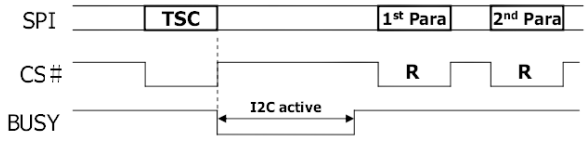
Internal Sensor Mapping

TS[3:0]	temperature
0000	0 ℃
0001	5 ℃
0010	10 ℃
0011	15 ℃
0100	20 ℃
0101	25 ℃
0110	30 ℃
0111	35 ℃
1000	40 ℃
1001	45 ℃
1010	50 ℃

External LM75 Sensor Mapping (D10~D0)

Table 10. Temp register value

11-bit binary (2's complement)	Hexadecimal value	Decimal value	Value
011 1111 1000	3F8	1016	+127.000 °C
011 1111 0111	3F7	1015	+126.875 °C
011 1111 0001	3F1	1009	+126.125 °C
011 1110 1000	3E8	1000	+125.000 °C
000 1100 1000	0C8	200	+25.000 °C
000 0000 0001	001	1	+0.125 °C
000 0000 0000	000	0	0.000 °C
111 1111 1111	7FF	–1	–0.125 °C
111 0011 1000	738	–200	–25.000 °C
110 0100 1001	649	–439	–54.875 °C
110 0100 1000	648	–440	–55.000 °C



Typical External Sensor Cycles

Temperature Sensor Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R41H	**TSE**	W	0	0	1	0	0	0	0	0	1	(41H)
	1st Para	W	1	TSE	0	0	0	0	0	0	0	00H

Name	Control	Value	Description
TSE	Temperature Sensor Selection	0	Internal temperature sensor
		1	External temperature sensor

VCOM and Data Interval Setting Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R50H	**CDI**	W	0	0	1	0	1	0	0	0	0	(50H)
	1st Para	W	1	-	-	-	DDX	CDI3	CDI2	CDI1	CDI0	17H

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync). This command can be active only when BUSY = "1".

SD_BDHZ: Border output selection

0 : Border output normal voltage

1 : Border floating

DDX: Internal temperature sensor switch

0: 0 – white / 1 – black

1: 0 – black / 1 – white (default)

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data interval		CDI[3:0]	Vcom and Data interval
0000b	17 hsync		1000	9
0001	16		1001	8
0010	15		1010	7
0011	14		1011	6
0100	13		1100	5
0101	12		1101	4
0110	11		1110	3
0111	10 (default)		1111	2

Resolution Setting Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R61H	**TRES**	W	0	0	1	1	0	0	0	0	1	(61H)
	1st Para	W	1	HRES7	HRES6	HRES5	HRES4	HRES3	HRES2	HRES1	0	00H
	2nd Para	W	1	-	-	-	-	-	-	-	VRES8	00H
	3rd Para	W	1	VRES7	VRES6	VRES5	VRES4	VRES3	VRES2	VRES1	VRES0	00H

Name	Control	Description
HRES[7:0]	Horizontal Resolution	(1) Horizontal resolution setting (HRES[0] is forced to '0') (2) Minimum active SD channel = S0 (3) Maximum active SD channel = min_active SD + HRES[7:0] - 1
VRES[8:0]	Vertical Resolution	(1) Vertical resolution setting (2) Minimum active GD channel = G0 (3) Maximum active GD channel = min_active GD + VRES[8:0] - 1

Resolution setting (R61H) has higher priority than RES [1:0] (R00H).

Note : For this panel R61H ‘s value must be 0x68、0x00、0xD4.

For command code R71H, see controller datasheet in Appendix.

VCOM-DC Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R82H	**VDCS**	W	0	1	0	0	0	0	0	1	0	(82H)
	1st Para	W	1	-	-	VDCS5	VDCS4	VDCS3	VDCS2	VDCS1	VDCS0	0CH

VDCS[5:0]	VCOM Value		VDCS[5:0]	VCOM Value
000000	0v		……	……
000001	-0.1v		011011	-2.7v
000010	-0.2v		011100	-2.8v
000011	-0.3v		011101	-2.9v
000100	-0.4v		011110	-3.0v
000101	-0.5v		……	
000110	-0.6v		111111	

ELECTRICAL CHARACTERISTICS

7-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.5 to +3.6	V
Logic Input Voltage	V_{IN}	-0.5 to VCI +0.5	V
Logic Output Voltage	V_{OUT}	-0.5 to VCI +0.5	V
Operating Temp. range	T_{OPR}	0 to +40	℃
Storage Temp. range	T_{STG}	-25 to +60	℃

7-2) Panel DC Characteristics

The following specifications apply for : VSS = 0V, VCI = 3.0V, TA = 25℃

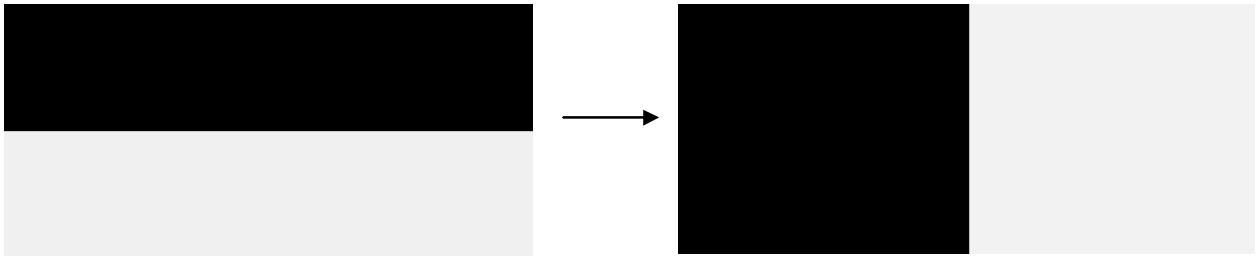
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.3	3.0	3.6	V
High level input voltage	VIH	-	0.8VCI	-	-	V
Low level input voltage	VIL	-	-	-	0.2VCI	V
High level output voltage	VOH	IOH= -100uA	0.9VCI	-	-	V
Low level output voltage	VOL	IOH= 100uA	-	-	0.1VCI	V
Image update current	I_{UPDATE}	-	-	8	10	mA
Standby panel current	Istandby	-	-	-	5	uA
Power panel (update)	P_{UPDATE}	-	-	26.4	40	mW
Standby power panel	P_{STBY}	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	40	℃
Storage temperature	-	-	-25	-	60	℃
Image update time at 25℃	-	-	-	8	12	Sec
Sleep mode current	VCI	DC/DC off No clock No input load Ram data not retain	-	2	5	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz -

Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 7-1

The Typical power consumption



7-3) Panel AC Characteristics

7-3-1) MCU Interface

7-3-1-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDin	SCLK	CS#	D/C#	RES#
SPI3	SDin	SCLK	CS#	L	RES#

Table 7-1: MCU interface assignment under different bus interface mode

Note 7-2: L is connected to VSS

Note 7-3: H is connected to VCI

7-3-1-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

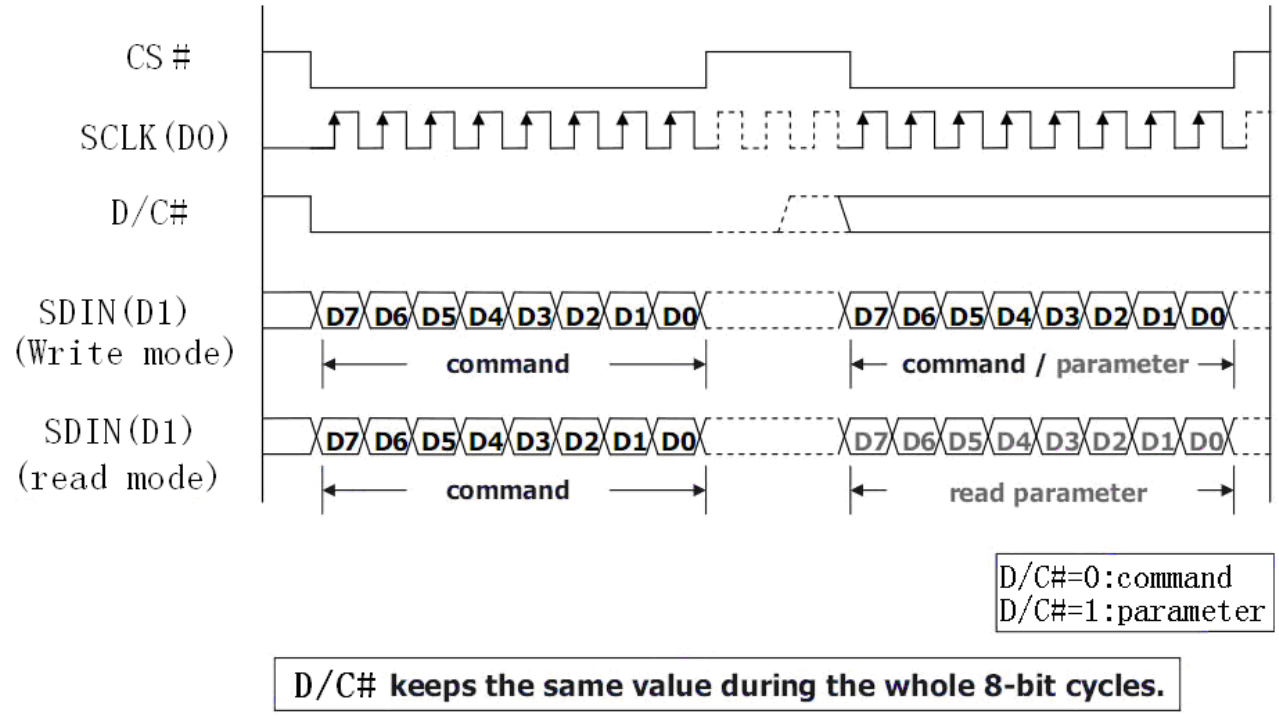
Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 7-2: Control pins of 4-wire Serial Peripheral interface

Note 7-9: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.
Under serial mode, only write operations are allowed.

Figure 7-1: Write procedure in 4-wire Serial Peripheral Interface mode



7-3-1-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

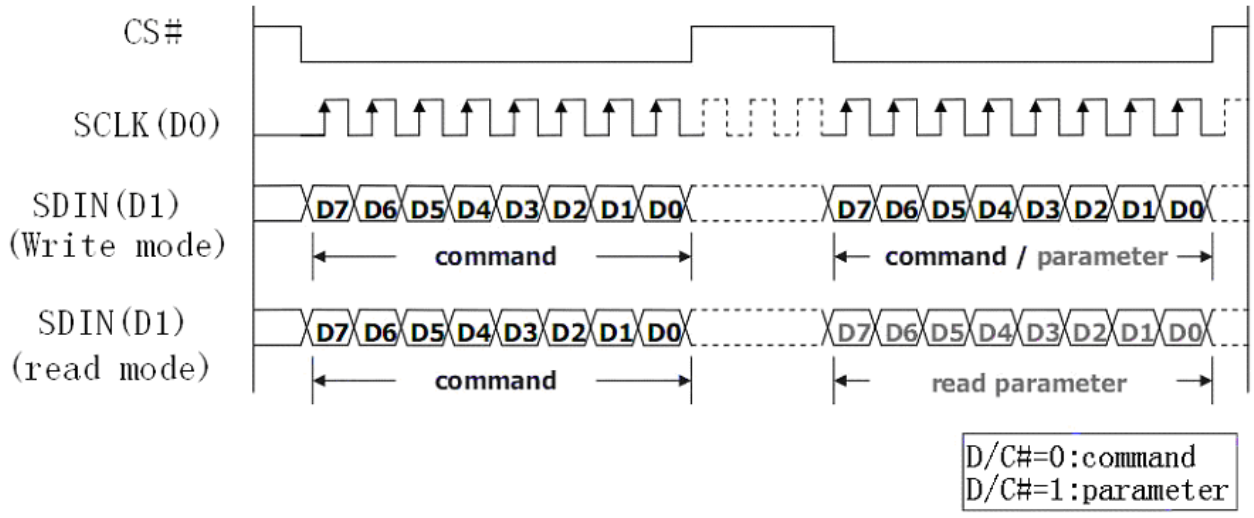
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of t sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie Low	↑
Write data	L	Tie Low	↑

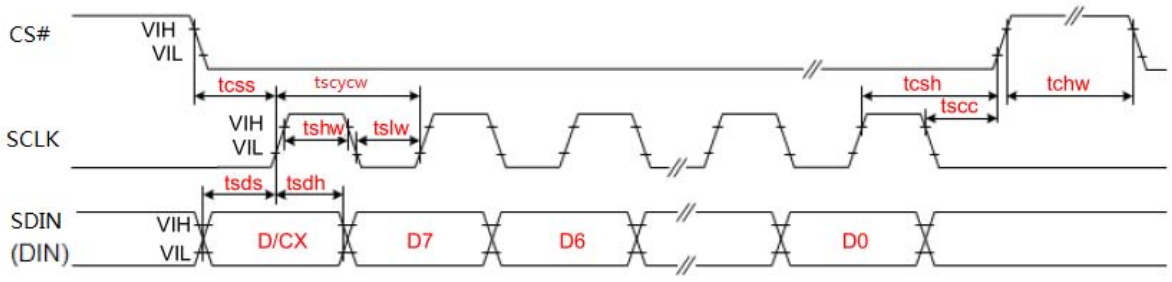
Table 7-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-10: ↑stands for rising edge of signal

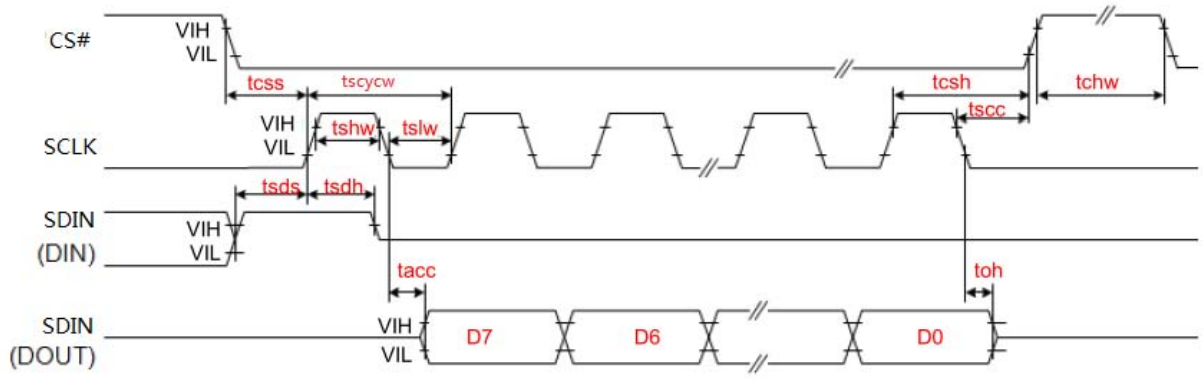
Figure 7-2: Write procedure in 3-wire Serial Peripheral Interface mode



7-3-2) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter		Min	Typ	Max	Unit
SERIAL COMMUNICATION							
tcss	CSB	Chip Select Setup Time		60	-	-	ns
tcsh		Chip Select Hold Time		65	-	-	ns
tscc		Chip Select Setup Time		20	-	-	ns
tchw		Chip Select Setup Time		40	-	-	ns
tscycw	SCL	Serial clock cycle (write)		100	-	-	ns
tshw		SCL “H” pulse width (write)		35	-	-	ns
tslw		SCL“L” pulse width (write)		35	-	-	ns
tscycr		Serial clock cycle (Read)		150	-	-	ns
tshr		SCL “H” pulse width (Read)		60	-	-	ns
tslr		SCL “L” pulse width (Read)		60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time		30	-	-	ns
tsdh		Data hold time		30	-	-	ns
tacc		Access time		10	-	-	ns
toh		Output disable time		15	-	-	ns

7-4) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	26.4	40	mW	-
Power consumption in standby mode	-	25℃	-	0.0165	mW	-

7-5) Reference Circuit

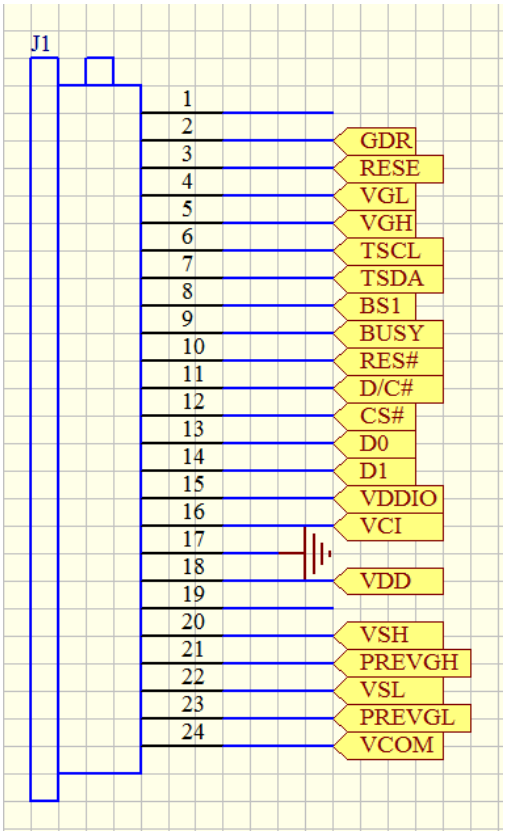


Figure . 7-5 (1)

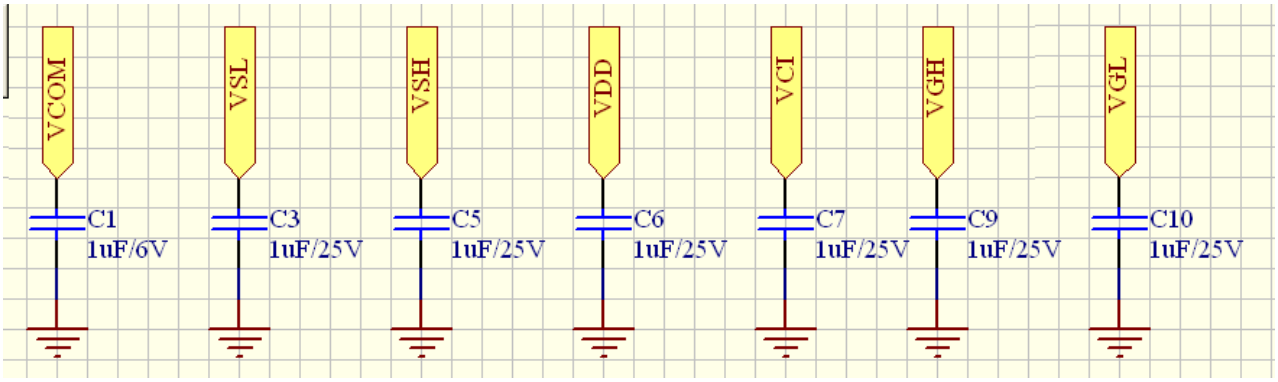
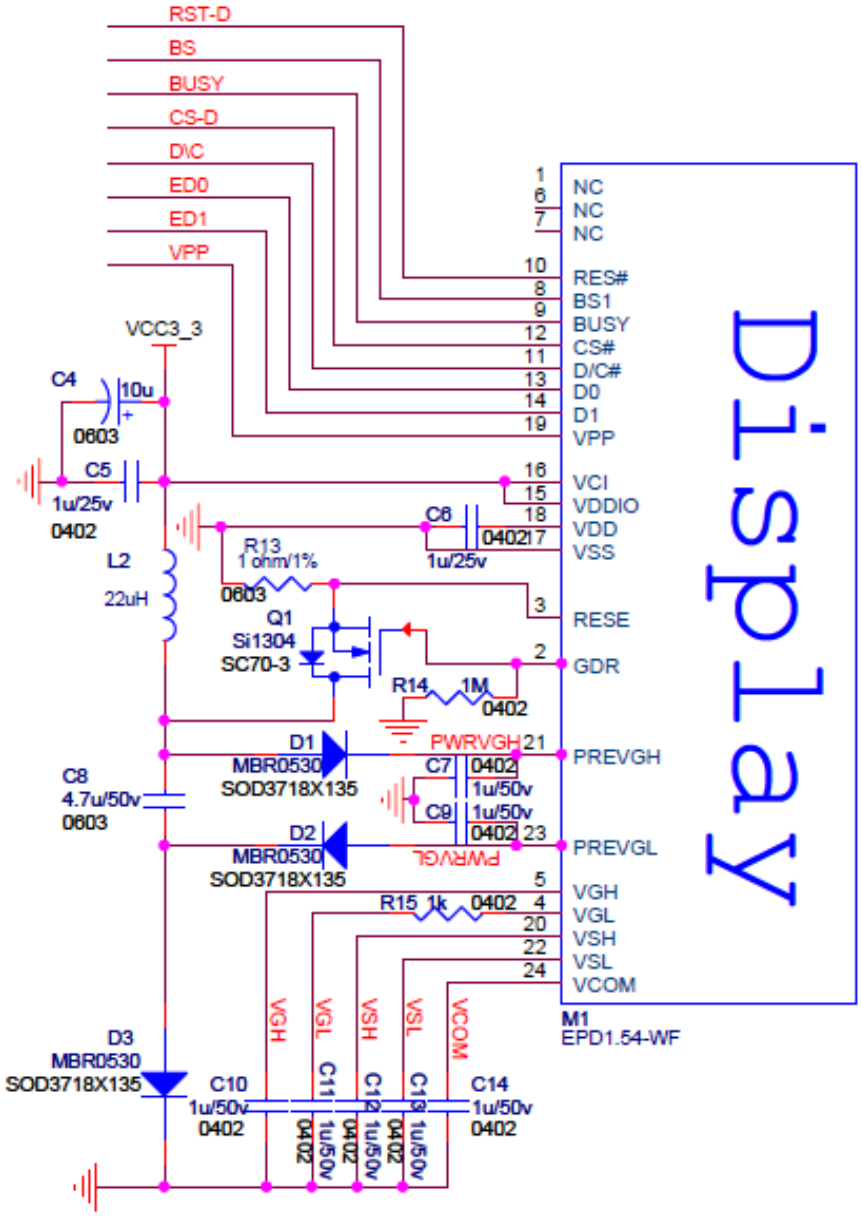


Figure . 7-5 (2)


RST-D
BS
BUSY
CS-D
D\C
ED0
ED1
VPP
VCC3_3
C4
10u
0603
C5
1u/25v
0402
L2
22uH
R13
1 ohm/1%
0603
C6
1u/25v
0402
Q1
Si1304
SC70-3
R14
1M
0402
D1
MBR0530
SOD3718X135
C7
0402
1u/50v
C9
1u/50v
0402
C8
4.7u/50v
0603
D2
MBR0530
SOD3718X135
R15 1k
0402
D3
MBR0530
SOD3718X135
C10
1u/50v
0402
C11
1u/50v
0402
C12
1u/50v
0402
C13
1u/50v
0402
C14
1u/50v
0402
VGH
VGL
VSH
VSL
VCOM
1
6
7
10
8
9
12
11
13
14
19
16
15
18
17
3
2
21
23
5
4
20
22
24
NC
NC
NC
RES#
BS1
BUSY
CS#
D/C#
D0
D1
VPP
VCI
VDDIO
VDD
VSS
RESE
GDR
PREVGH
PREVGL
VGH
VGL
VSH
VSL
VCOM
M1
EPD1.54-WF
Display

WAVEFORM LUT CONTROL SOFTWARE

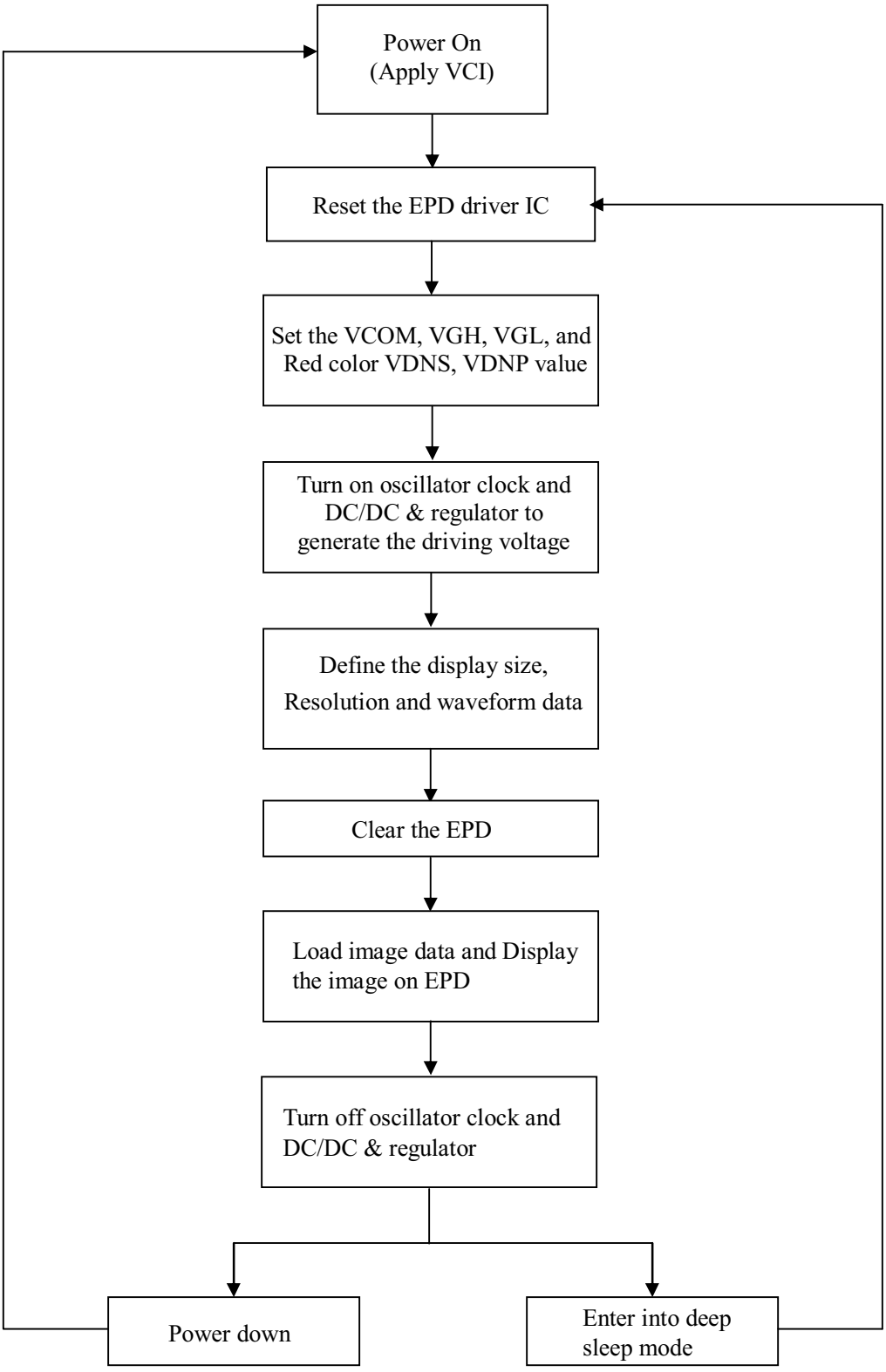
For every bunch of EPD the waveform data is different.You just need to use the follow sequence to download the waveform in the Crystalfontz zipped file into driver IC.

sequence	command	Action Description	remark
1	04	Power on	Send cmd 04
2	20	VCOM LUT Setting	Send cmd 20 data lut_vcom0[]
3	21	White LUT Setting	Send cmd 21 data lut_w[]
4	22	Black LUT Setting	Send cmd 22 data lut_b[]
5	25	RED VCOM LUT Setting	Send cmd 25 data lut_vcom1[]
6	26	RED0 LUT Setting	Send cmd 26 data lut_red0[]
7	27	RED1 LUT Setting	Send cmd 27 data lut_red1[]

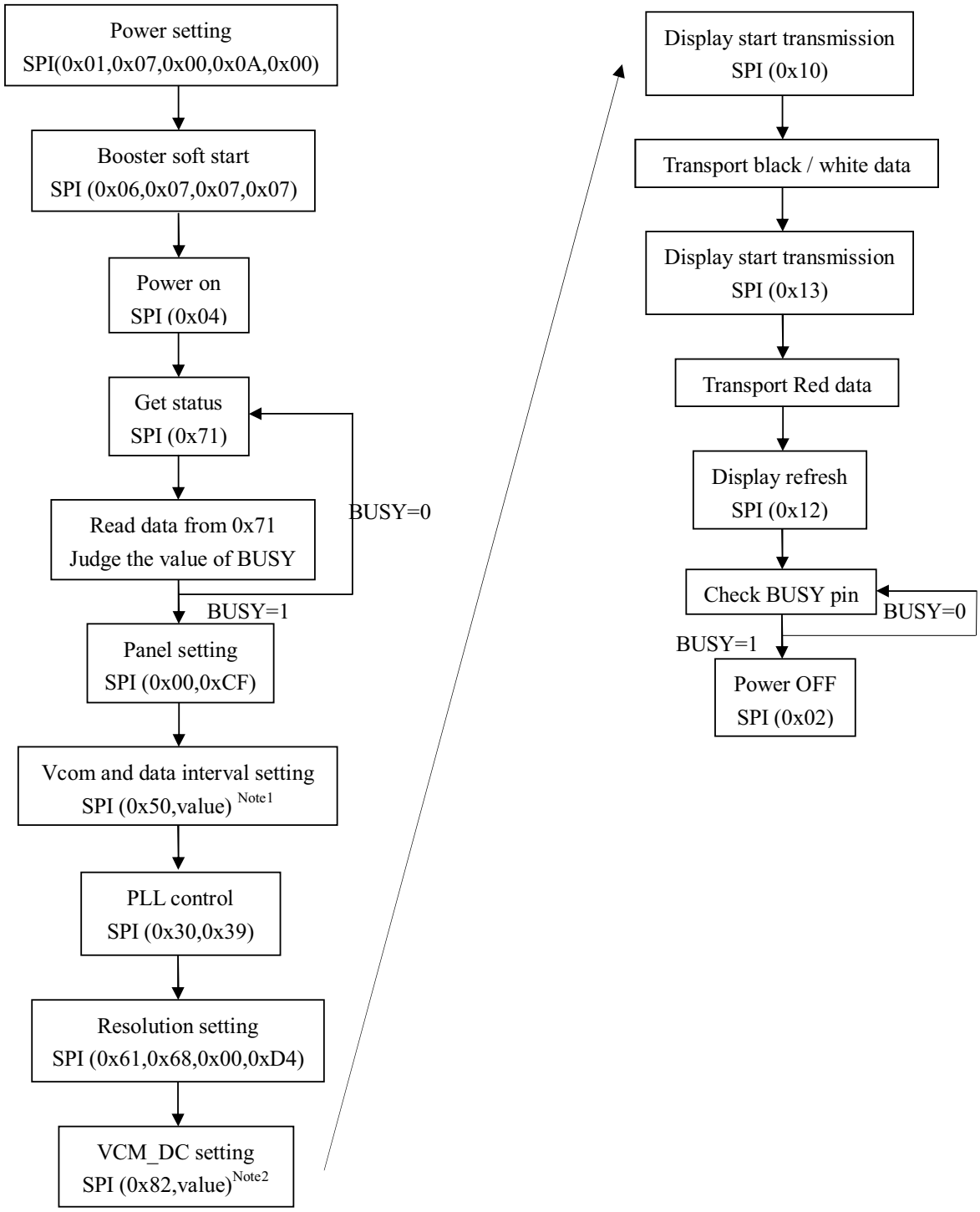
Note: To download the waveform into driver ic, you must send command 04 first, then send 20, 21, 22, 25, 26, 27 command.
The data of lut_vcom0[],lut_w[],lut_b[],lut_vcom1[],lut_red0[],lut_red1[],each batch of EPD is different.

For maximum performance, each batch of EDP has a unique LUT. Contact Technical Support to make sure you have the correct LUT for the batch that your displays were produced in.

TYPICAL OPERATION SEQUENCE, NORMAL FLOW



REFERENCE PROGRAM CODE



Note1: When value=0x37, border will be drive to black after refresh. When value=0x17, the border is set to floating.

Note2: Different EPD with different VCOM value,CFA will provide different values according to different batches of EPD.

OPTICAL CHARACTERISTICS

10-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 10-1
RS_a	Red State a value	Red	30	35	45	-	
Gn	2Grey Level	-	-	DS+(WS-DS) xn (m-1)	-	L*	-
CR	Contrast Ratio	indoor	8	-	-	-	-
Panel's life		0℃~40℃		1000000 times or 5 years			Note 10-2

WS: White state, DS: Dark state, RS: Red state.

Gray state from Dark to White : DS、WS

m: 2

Note 10-1: Luminance meter: Eye – One Pro Spectrophotometer

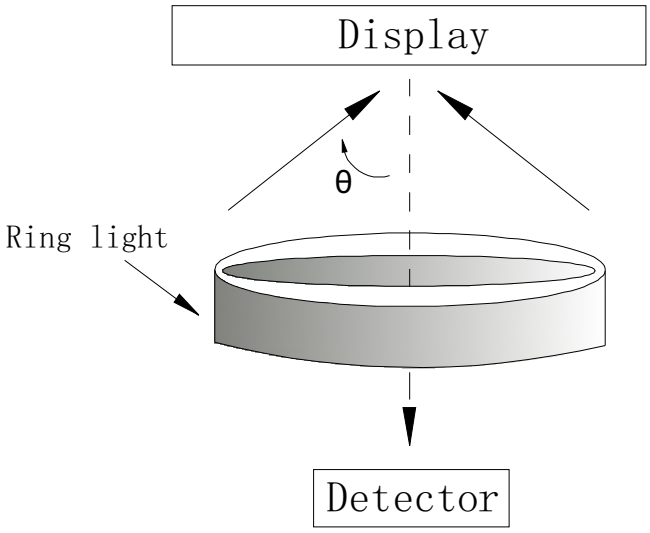
Note 10-2: When work in temperature below 0 degree or above 40 degree, we do not recommend because the panel's life will not be guaranteed.

10-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

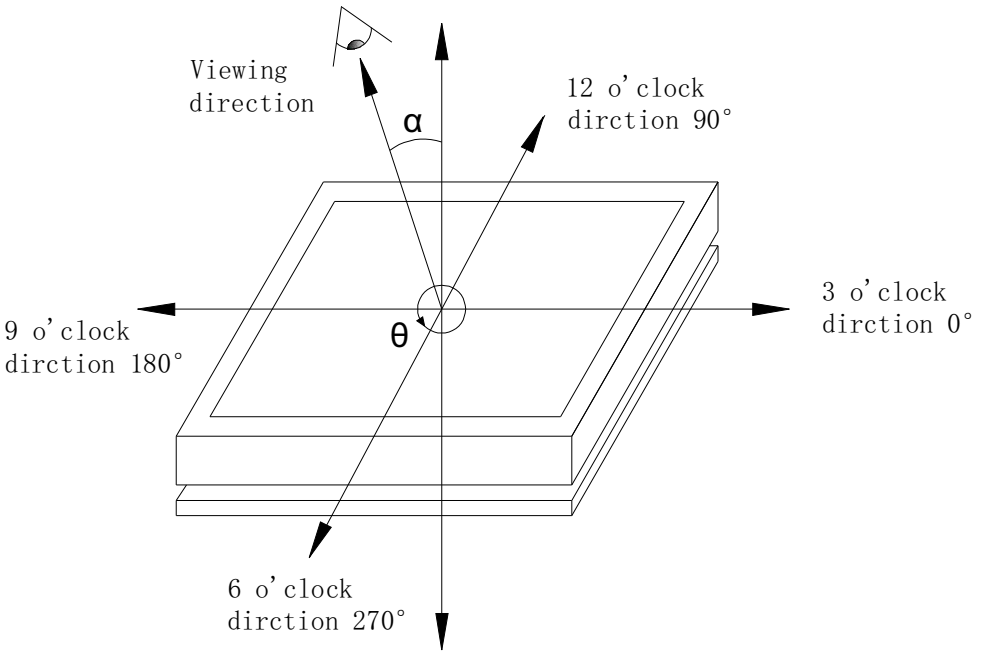


10-3) Reflection Ratio

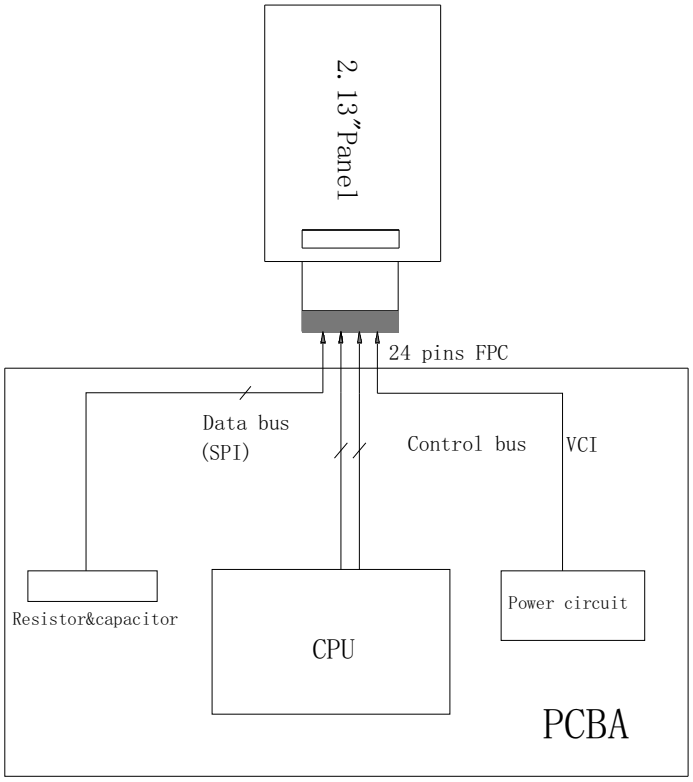
The reflection ratio is expressed as:

R = Reflectance Factor $_{white\ board}$ x (L_{center} / $L_{white\ board}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



BLOCK DIAGRAM



APPENDIX: UC8154 CONTROLLER SPECIFICATIONS

These controller specifications are supplied as an appendix for the

CFAP104212B0-0213

Display Datasheet Release 2016-06-24

Table of Content

INTRODUCTION

This driver is an all-in-one driver with timing controller for ESL. Its output is of 2-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for the source driver and gate drivers.

The DC-DC controller allows it to generate the source output voltage VDPS/VDNS (+/-2.4V~+/-8V, +/-15V). The chip also includes an output buffer for the supply of the COM electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

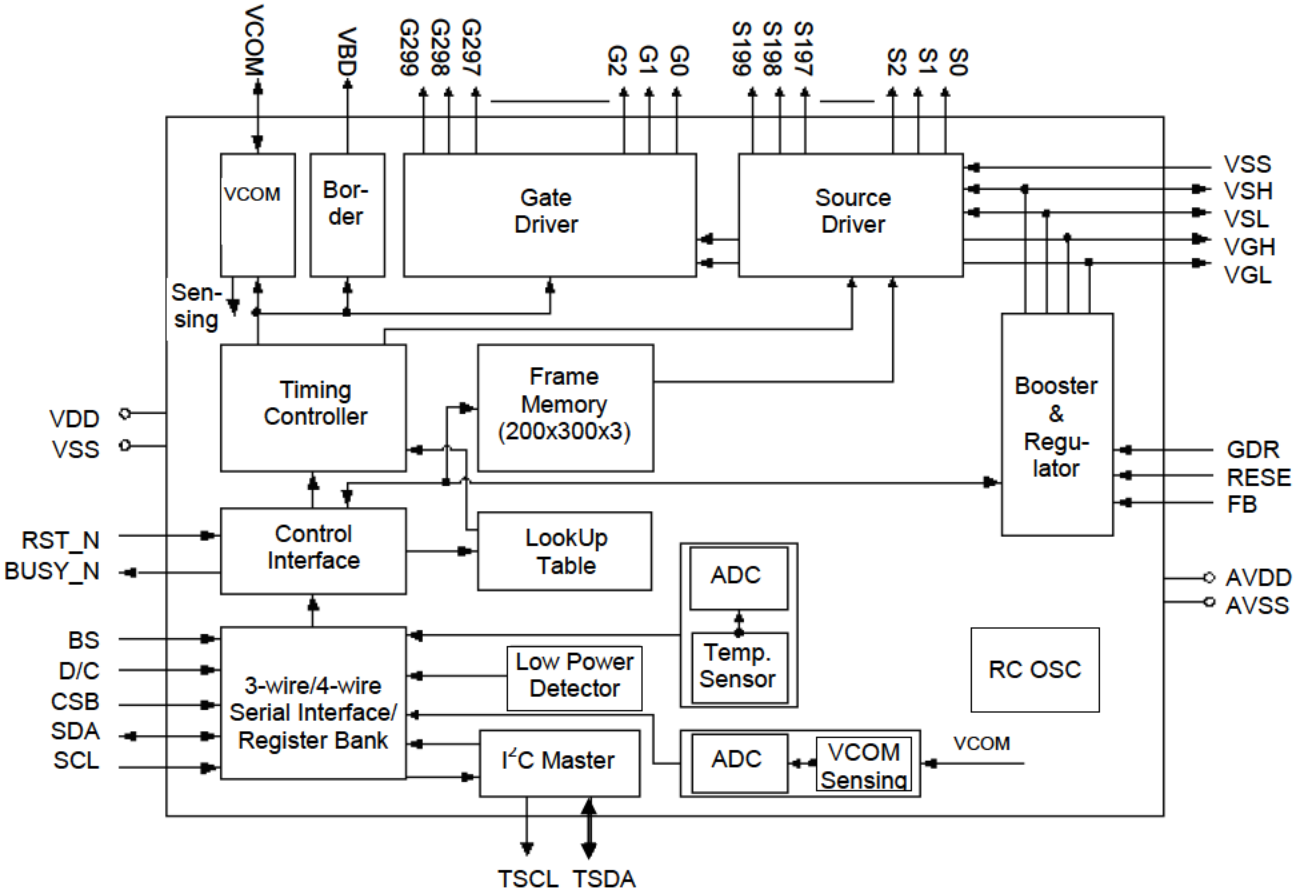
MAIN APPLICATIONS

- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several all-resolutions
- Preselectable resolution (SourcexGate):
  - 94x230
  - 94x252
  - 128x296
  - 200x300
- Built-in Frame memory (Max.): 300x200x3bit
- Support LUT1 (VCOM1, White, Black, Gray1, Gray2)
- Support LUT2 (VCOM2, Red0, Red1)
- Source Driver with 2-bit white/black resolution and 1-bit red resolution
  - 200 channels
  - Output dynamic range: VDNS, 0, VDPS
  - Output deviation: 0.2 V
  - Left and Right shift capability
- Gate Driver:
  - 300 channel outputs
  - Output voltage VDNG+40
  - Up and Down scan capability
- 3-wire/4-wire (SPI) serial interface
- DC-DC controller for generating the analog power supply
- COM electrode (VCOM AC) level
- Built-in temperature sensor
- Digital supply voltage: 2.3~ 3.6V
- Operating frequency: 20MHz (max)
- COG Package
- COM/SEG bump information
  Bump pitch: 42 μM
  Bump gap: 24 μM ± 3μM
  Bump surface: 1350 μM^2

BLOCK DIAGRAM



PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, P: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY			
VDD	7	P	Digital power
VDDA	10	P	Analog power
VDDIO	10	P	IO power
GND	18	P	Digital Ground.
GNDA	17	P	Analog Ground
VDM	4	P	Driver Ground
SERIAL COMMUNICATION INTERFACE			
CSB	1	I (Pull-up)	Serial communication chip select.
SDA	1	I/O	Serial communication data input.
SCL	1	I	Serial communication clock input.
DC	1	I	Serial communication Command/Data input. L: command H: data
CONTROL INTERFACE			
BS	1	I (Pull-up)	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF. **H: 3-wire IF. (Default)**
RST_N	1	I (Pull-up)	Global reset pin. Low: reset. When RST_N become low, driver will reset. All register will be reset to default value, and all driver functions will be disabled. SD output and VCOM will base on previous condition; and they may have two conditions: 0v or floating.
BUSY_N	1	O	This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver.
TEST1~7	7	--	Test pins. Reserved for testing. Leave them open.
TSCL	2	O	I^2C clock for external temperature sensor.
TSDA	2	I/O	I^2C data for external temperature sensor.

Pin (Pad) Name	Pin Count	Type	Description
OUTPUT DRIVER			
S[0..199] (S<0>~S<199>)	200	O	Source driver output signals.
G[0..299] (G<0>~G<299>)	300	O	Gate driver output signals.
VBD (VBD<1>~VBD<2>)	2	O	Border output pins. It outputs black WF.
CL	1	I/O	Clock pin for cascade mode. In single-chip mode, keep CL open. In cascade mode, the CL pin of the slave chip should be connected to the CL pin of the master chip.
MS	1	I	Master/Slave selection for cascade mode. Low: Slave, High: Master In single-chip mode, MS should be connect to VDD.
VSYNC	1	I/O	Vsync pin for cascade mode. In single-chip mode, VSYNC should be connected to GND or VDD. In cascade mode, VSYNC pin of slave chip shoulde be connected to VSYNC pin of master chip.
VCOM GENERATOR			
VCOM	16	O	VCOM output. It has the following voltage states: (VDPS+VCM_DC) V, (VCM_DC) V, (VDNS+VCM_DC) V, Floating
POWER CIRCUIT			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	20	C	Positive Gate voltage.
VGL	24	C	Negative Gate voltage.
VSH	10	C	Positive Source voltage.
VSL	10	C	Negative Source voltage.
MISC. PINS			
NC	40		Not Connected.
Dummy	26		Dummy pins.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	--	#	#	#	#	#	RES, KW/R, UD, SHL, SHD_N, RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	--	--	--	--	#	#	#	#	RVSHLS, VDS_EN, VDG_EN	03h
		0	1	--	--	--	--	--	--	#	#	VGHL_LV	00h
		0	1	--	--	--	#	#	#	#	#	VDPS_LV	08h
		0	1	--	--	--	#	#	#	#	#	VDNS_LV	08h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	--	#	#	#	#	#	#	#	BT_PHA[6:0]	0Fh
		0	1	--	#	#	#	#	#	#	#	BT_PHB[6:0]	0Eh
		0	1	--	--	--	#	#	#	#	#	BT_PHC[4:0]	0Dh
8	Display Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	#	#	#	#	#	KPixel1, KPixel2, KPixel3, KPixel4	00h
		0	1	..	..	..	..	..	..	..	..	..	:
		0	1	#	#	#	#	--	--	--	--	KPixel(n-1), KPixel(n)	00h
9	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--	data_flag	--
10	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
11	Display Start transmission 2 (DTM2) (y-byte command)	0	0	0	0	0	1	0	0	1	1		13h
		0	1	#	#	#	#	#	#	#	#	RPixel1, RPixel2, RPixel3, RPixel4	00h
		0	1	..	..	..	..	..	..	..	..	..	:
		0	1	#	#	--	--	--	--	--	--	RPixel(n-1), RPixel(n)	00h
12	Vcom1 LUT (LUTC1) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	0	0		20h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
13	White LUT (LUTW) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	0	1		21h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
14	Black LUT (LUTB) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	1	0		22h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
15	Gray1 LUT (LUTG1) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	1	1		23h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
16	Gray2 LUT (LUTG2) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	1	0	0		24h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
17	Vcom2 LUT (LUTC2) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	1	0	1		25h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
18	Red0 LUT (LUTR0) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	1	1	0		26h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
19	Red1 LUT (LUTR1) (16-byte command, bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	1	1	1		27h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
20	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	--	--	#	#	#	#	#	#	M, N	2Ah
21	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	TSE[D10:D0] / TS[3:0]	00h
		1	1	#	#	#	--	--	--	--	--		
22	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	--	--	--	--	--	--	--	TSE	00h
23	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
24	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
25	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	--	--	#	#	#	#	#	#	SD_BDHZ, DDX, CDI	17h
26	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	--	--	--	--	--	--	--	#	LPD	--
27	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G, G2S	22h
28	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	#	#	0	HRES	00h
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
29	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		1	1	0	0	0	0	0	0	0	0		00h
30	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	--	--	--	--	--	--	#	#	I2C_ERR, I2C_BUSYN, data_flag, PON, POF, BUSY_N	02h
31	Auto Measurement Vcom	0	0	1	0	0	0	0	0	0	0		80h
		0	1	--	--	#	#	--	--	#	#	AMVT, AMV, AMVE	10h
32	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	--	--	#	#	#	#	#	#	VV	00h
33	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	--	--	#	#	#	#	#	#	VDCS	00h

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

(5) All registers are accessible, (i.e., Host can send command/data to driver), only when BUSY_N =1; except R01h (PWR), R03h (PFS), R04h (PON), R05h (PMES), R06h(BTST), R51h (LPD), and R71h(FLG), which are accessible either when BUSY_N=0 or 1.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	--	KWR	UD	SHL	SHD_N	RST_N

RES[1:0]: Display Resolution setting (source x gate)

00b: 94x230 (Default) Active source channels: S0 ~ S93. Active gate channels: G0 ~ G229.
01b: 94x252 Active source channels: S0 ~ S93. Active gate channels: G0 ~ G251.
10b: 128x296 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.
11b: 200x300 Active source channels: S0 ~ S199. Active gate channels: G0 ~ G299.

KWR: KW/R function

0: Pixel with K/W/Red. Will run both LU1 and LU2. (Default)
1: Pixel with K/W. Will run LU1 only.

UD:
0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL:
0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N:
0: DC-DC converter will be turned OFF
1: DC-DC converter will be turned ON (Default)

When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and SD output and VCOM will remain previous condition. SHD_N may have two conditions: 0v or floating.

RST_N:
0: The controller is reset. Reset all registers to default value.
1: No effect (Default)

When RST_N become LOW, the driver will be reset, all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

This command can be active only when BUSY_N = "1".

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	RVSHLS	RVSHLS	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	-	VGHL_LV[1:0]	
	0	1	-	-	-	VDPS_LV[4:0]				
	0	1	-	-	-	VDNS_LV[4:0]				

RVSHLS[1:0]: Source power selection

RVSHLS[1:0]	VSH	VSL
00	+2.4 ~ +8.0V	-2.4 ~ -8.0V
01	+2.4 ~ +8.0V	-15V
10	+15V	-2.4 ~ -8.0V
11	+15V	-15V

VDS_EN: Source power selection
0 : External source power from VDH/VDL pins
1 : Inetrnal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL

VGHL_LV[1:0]: VGHL_LVL / VDNG_LVL power selection.

VGHL_LV	VGHL_LVL power
00 (DEFAULT)	VGH=20V, VGL= -19.3V
01	VGH=19V, VGL= -18.3V
10	VGH=18V, VGL= -17.3V
11	VGH=17V, VGL= -16.3V

VDPS_LV[4:0]: Internal VDPS power selection for Red LUT.(**Default value: 01000b**)

VDPS_LV	VDPS	VDPS_LV	VDPS	VDPS_LV	VDPS	VDPS_LV	VDPS
00000	2.4 V	**01000**	**4.0 V**	10000	5.6 V	11000	7.2 V
00001	2.6 V	01001	4.2 V	10001	5.8 V	11001	7.4 V
00010	2.8 V	01010	4.4 V	10010	6.0 V	11010	7.6 V
00011	3.0 V	01011	4.6 V	10011	6.2 V	11011	7.8 V
00100	3.2 V	01100	4.8 V	10100	6.4 V	11100	8.0 V
00101	3.4 V	01101	5.0 V	10101	6.6 V	(others)	4.0 V
00110	3.6 V	01110	5.2 V	10110	6.8 V		
00111	3.8 V	01111	5.4 V	10111	7.0 V		

VDNS_LV[4:0]: Internal VDNS power selection for Red LUT. (**Default value: 01000b**)

VDNS_LV	VDNS	VDNS_LV	VDNS	VDNS_LV	VDNS	VDNS_LV	VDNS
00000	-2.4 V	01000	-4.0 V	10000	-5.6 V	11000	-7.2 V
00001	-2.6 V	01001	-4.2 V	10001	-5.8 V	11001	-7.4 V
00010	-2.6 V	01010	-4.4 V	10010	-6.0 V	11010	-7.6 V
00011	-3.0 V	01011	-4.6 V	10011	-6.2 V	11011	-7.8 V
00100	-3.2 V	01100	-4.8 V	10100	-6.4 V	11100	-8.0 V
00101	-3.4 V	01101	-5.0 V	10101	-6.6 V	(others)	-4.0 V
00110	-3.6 V	01110	-5.2 V	10110	-6.8 V		
00111	-3.8 V	01111	-5.4 V	10111	-7.0 V		

This command can be active only when BUSY_N = “1”.

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, driver will power off based on the Power Off Sequence, BUSY_N will become "0". This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

SD output and Vcom will base on previous condition. It may have 2 conditions: 0V or floating.

This command can be active only when BUSY_N = "1".

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	0
	0	1	-	-	T_VDS_OFF[1:0]		-		-	

T_VDS_OFF[1:0]: Power OFF Sequence of VDPS and VDNS.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

This command can be active only when BUSY_N = "1".

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON following the Power ON Sequence. After the Power ON command and all power sequence are ready, the BUSY_N signal will become "1". Refer to the Power ON Sequence section.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	1

This command releases BUSY_N restriction for command TSC and command LPD until next Power Off.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	-	BTPHA6	BTPHA5	BTPHA4	BTPHA3	BTPHA2	BTPHA1	BTPHA0
	0	1	-	BTPHB6	BTPHB5	BTPHB4	BTPHB3	BTPHB2	BTPHB1	BTPHB0
	0	1	-	-	-	BTPHC4	BTPHC3	BTPHC2	BTPHC1	BTPHC0

BTPHA[6:5]: Soft start period of phase A. **00b: 10mS** 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[4:3] : Driving strength of phase A

00b: strength 1 **01b: strength 2** 10b: strength 3 11b: strength 4 (strongest)

BTPHA[2:0] : Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[6:5] : Soft start period of phase B. **00b: 10mS** 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[4:3] : Driving strength of phase B

00b: strength 1 **01b: strength 2** 10b: strength 3 11b: strength 4 (strongest)

BTPHB[2:0] : Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS **110b: 3.34uS** 111b: 6.58uS

BTPHC[4:3] : Driving strength of phase C

00b: strength 1 **01b: strength 2** 10b: strength 3 11b: strength 4 (strongest)

BTPHC[2:0] : Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS **010b: 0.40uS** 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

(8) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	kpixel1[1:0]		kpixel2[1:0]		kpixel3[1:0]		kpixel4[1:0]	
	0	1	...		...		...		...	
	0	1	kpixel(n-1)[1:0]		kpixel(n)[1:0]		-	-	-	-

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

This command can be active only when BUSY_N = "1".

KPixel(x)[1:0]:

DDX	KPixel (x) [1:0]	LUT
0	00	White
	01	Gray2
	10	Gray1
	11	Black
1	00	Black
	01	Gray1
	10	Gray2
	11	White

(9) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.
0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data.

This command can be active only when BUSY_N = "1". After data start (10h) and data stop (11h) command, BUSY_N signal will become "0".

(10) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

This command can be active only when BUSY_N = "1". After display refresh command, BUSY_N signal will become "0".

(11) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	RPixel1	RPixel2	RPixel3	RPixel4	RPixel5	RPixel6	RPixel7	RPixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	RPixel(n-1)	RPixel(n)	-	-	-	-	-	-

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

This command can be active only when BUSY_N = "1".

RPixel(x):

DDX	RPixel (x)	LUT
0	0	Red1
	1	Red0
1	0	Red0
	1	Red1

(12) VCOM1 LUT (LUTC1) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for Vcom 1 (16-byte command, Bytes 2~4 repeated 5 times)	0	0	0	0	1	0	0	0	0	0
	0	1	LEVEL SELECT.		NUMBER OF FRAMES					
	0	1	LEVEL SELECT.		NUMBER OF FRAMES.					
	0	1	TIMES TO REPEAT							
	0	1	:		:					
	0	1	:		:					
	0	1	:							
	0	1	:		:					
	0	1	:		:					
	0	1	:							

This command stores VCOM Look-Up Table with 5 groups of data. Each group contains information for one phase and is stored with 3 bytes, while the third byte indicates how many times that phase will repeat.

Bytes 2, 3, 5, 6, 8, 9, 11, 12, 14, 15:

{D7:D6}: Level selection. 00b: VCM_DC 01b: 15V+VCM_DC (VCOMH) 10b: -15V+VCM_DC (VCOML) 11b: Floating

{D5:D0}: Number of Frames. 00 0000b~11 1111b: 0 ~ 63 frames, respectively.

Bytes 4, 7, 10, 13, 16:

{D7:D0}: Times to repeat

(13) WHITE LUT (LUTW) (R21H)

This command builds Look-up Table for White. Please refer to command (12) Vcom1 LUT (LUTC1) for similar definition details.

(14) BLACK LUT (LUTB) (R22H)

This command builds Look-up Table for Black. Please refer to command (12) Vcom1 LUT (LUTC1) for similar definition details.

(15) GRAY1 LUT (LUTG1) (R23H)

This command builds Look-up Table for Gray 1. Please refer to command (12) Vcom1 LUT (LUTC1) for similar definition details.

(16) GRAY2 LUT (LUTG2) (R24H)

This command builds Look-up Table for Gray 2. Please refer to command (12) Vcom1 LUT (LUTC1) for similar definition details.

For commands (13)~(16), Level selection: 00b: 0V 01b: 15V (VSH) 10b: -15V (VSL) 11b: floating

(17) VCOM2 LUT (LUTC2) (R25H)

This command builds Look-up Table for Vcom 2. Please refer to command (12) Vcom1 LUT (LUTC1) for similar definition details.

Level selection: 00b: VCM_DC 01b: VSH (red)+VCM_DC(VCOMH) 10b: VSL (red)+VCM_DC(VCOML) 11b: floating

(18) RED0 LUT (LUTR0) (R26H)

This command builds Look-up Table for Red 0. Please refer to command (12) Vcom1 LUT (LUTC1) for similar definition details.

(19) RED1 LUT (LUTR1) (R27H)

This command builds Look-up Table for Red 1. Please refer to command (12) Vcom1 LUT (LUTC1) for similar definition details.

For commands (18)~(19), Level selection: 00b: 0V 01b: VSH (red) 10b: VSL (red) 11b: floating

(20) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

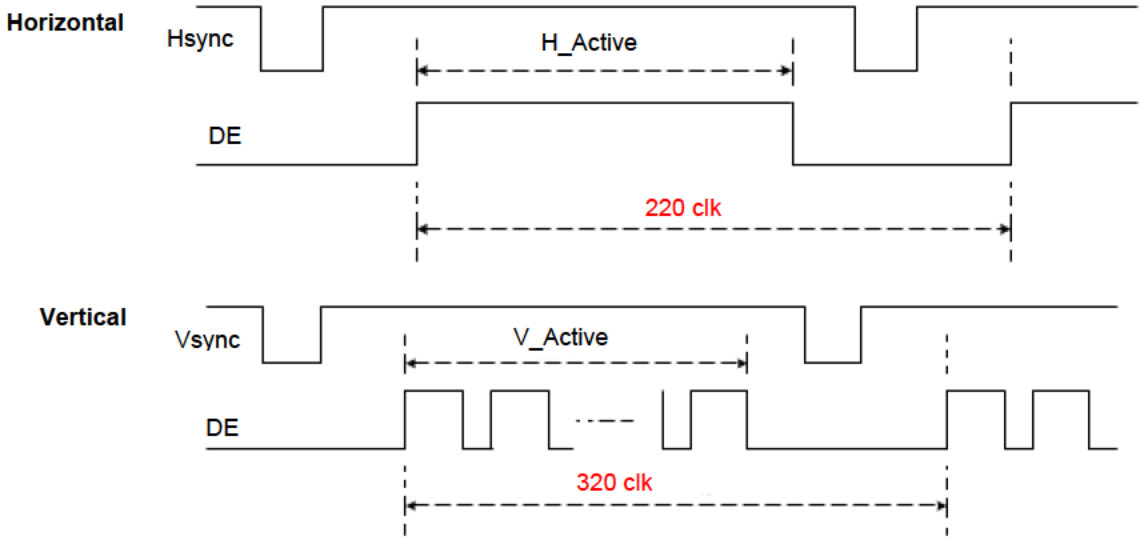
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame rate
1	1	20 Hz
	2	10 Hz
	3	7 Hz
	4	5 Hz
	5	4 Hz
	6	3 Hz
	7	3 Hz
2	1	39 Hz
	2	20 Hz
	3	13 Hz
	4	10 Hz
	5	8 Hz
	6	7 Hz
	7	6 Hz

M	N	Frame rate
3	1	59 Hz
	2	29 Hz
	3	20 Hz
	4	15 Hz
	5	12 Hz
	6	10 Hz
	7	8 Hz
4	1	78 Hz
	2	39 Hz
	3	26 Hz
	4	20 Hz
	5	16 Hz
	6	13 Hz
	7	11 Hz

M	N	Frame rate
5	1	98 Hz
	2	**50 Hz (default)**
	3	33Hz
	4	24 Hz
	5	20 Hz
	6	16 Hz
	7	14 Hz
6	1	117 Hz
	2	59 Hz
	3	39 Hz
	4	29 Hz
	5	23 Hz
	6	20 Hz
	7	17 Hz

M	N	Frame rate
7	1	137 Hz
	2	68 Hz
	3	46 Hz
	4	34 Hz
	5	27 Hz
	6	23 Hz
	7	20 Hz



This command can be active only when BUSY_N = "1".

(21) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10	D9	D8	D7	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS[3:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

(22) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	-	-	-	-	-	-

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

(23) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	1	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: **D[7:6]:** I^2C Write Byte Number
00 : 1 byte (head byte only)
01 : 2 bytes (head byte + pointer)
10 : 3 bytes (head byte + pointer + 1st parameter)
11 : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(24) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(25) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	-	-	SD_BDHZ	DDX	CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync). This command can be active only when BUSY_N = "1".

SD_BDHZ: Border output selection
0 : Border output normal voltage
1 : Border floating

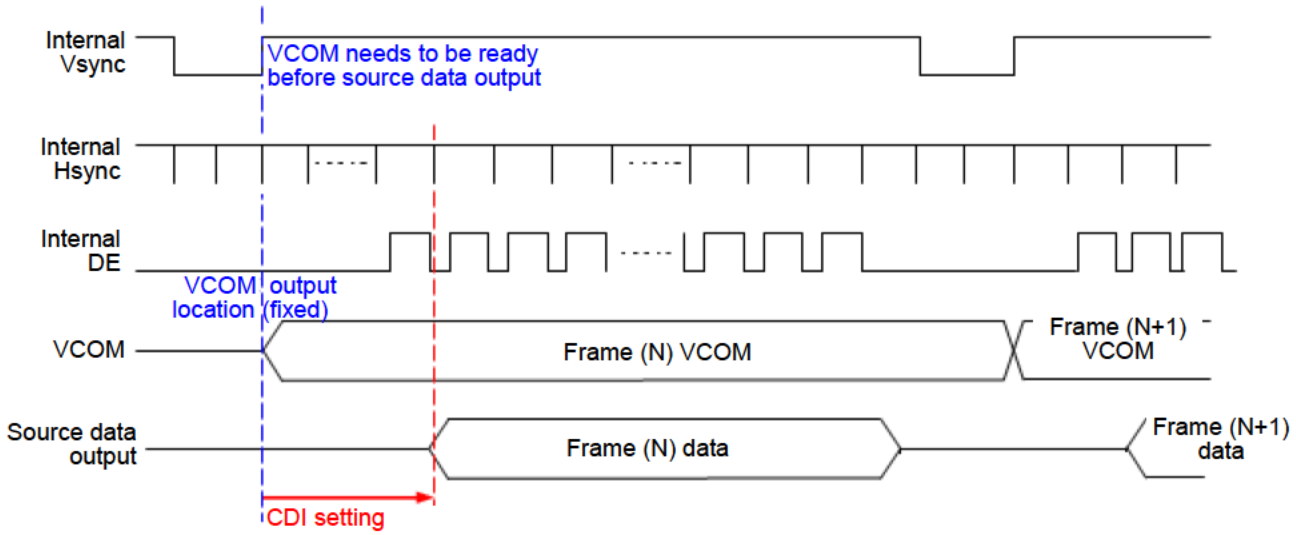
DDX: Internal temperature sensor switch

0: 0 – white / 1 – black **1: 0 – black / 1 – white (default)**

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	Vcom and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



(26) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (V_{DD}<2.5V) **1: Normal status (default)**

(27) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

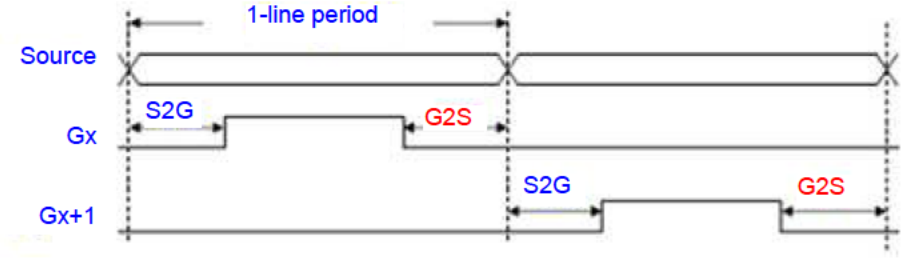
This command defines non-overlap period of Gate and Source. This command can be active only when BUSY_N = "1".

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4 clock
0001	8
0010	12 (Default)
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	(reserved)
1111	(reserved)

Clock frequency is 2MHz.



(28) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:1]							0
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	1	VRES[7:0]							

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:1]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

GD : First G active = G0; LAST active GD= first active +VRES -1

SD : First active channel: =S0 ; LAST active SD= first active +HRES-1

EX :128x296

GD: First G active = G0, LAST active GD= 0+296-1= 295; (G295)

SD: First active channel = S0, LAST active SD= 0+128-1=93; (S127)

This command can be active only when BUSY_N = "1".

(29) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	0	0	0	0	0			

This command can be active only when BUSY_N = "1".

(30) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	-	I^2C_ERR	I^2C_ BUSYN	data_ flag	PON	POF	BUSY_N

This command reads the IC status.

I^2C_ERR: I^2C master error status

I^2C_BUSYN: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(31) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		-	-	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s
01b: 5s (default)
10b: 8s
11b: 10s

AMV: 0 – Get Vcom value with the VV command (R81h)
1 – Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0 – No effect
1 – Trigger auto Vcom sensing.

This command can be active only when BUSY_N = "1".

(32) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV[5:0]: Vcom Value

VV[5:0]	Vcom value
00 0000b	0 V
00 0001b	-0.1 V
00 0010b	-0.2 V
:	:
01 0100b	-2.0 V (Default)
:	:
10 1000b	-4.0 V
10 1001b	-4.1 V
:	:
11 1111b	-6.3 V

This command can be active only when BUSY_N = "1".

(33) VCM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value

VDCS[5:0]: Vcom Value

VDCS[5:0]	Vcom value
00 0000b	**0 V** (Default)
00 0001b	-0.1 V
00 0010b	-0.2 V
00 0011b	-0.3 V
:	:
01 1110b	-3.0 V
:	
11 1111b	

This command can be active only when BUSY_N = "1".

HOST INTERFACES

3-WIRE SPI

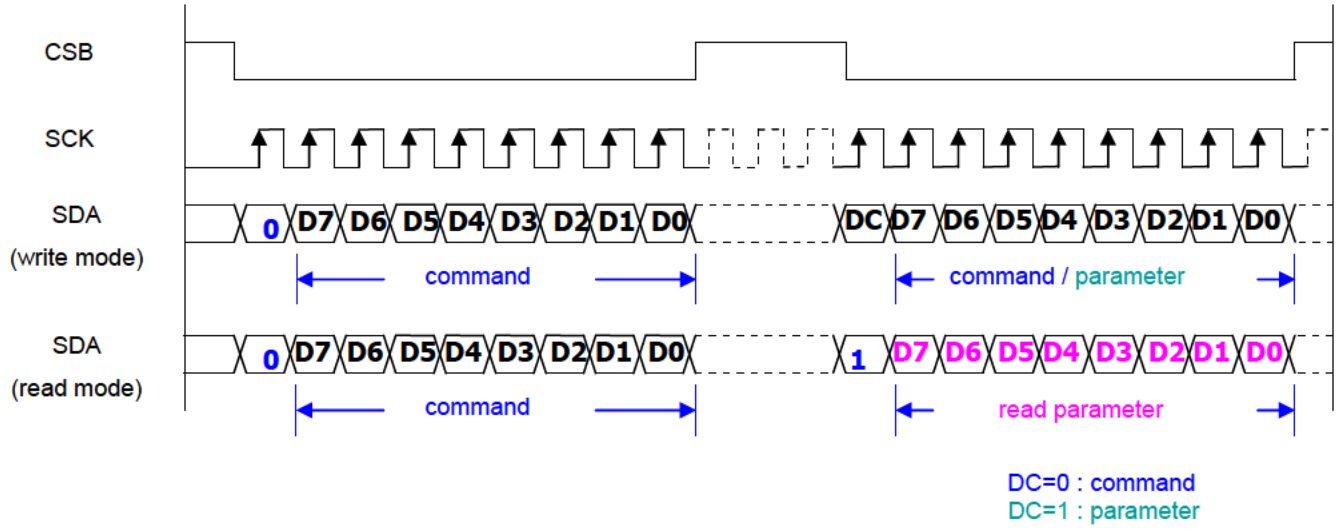


Figure : 3-wire SPI Typical Waveform – BS=1

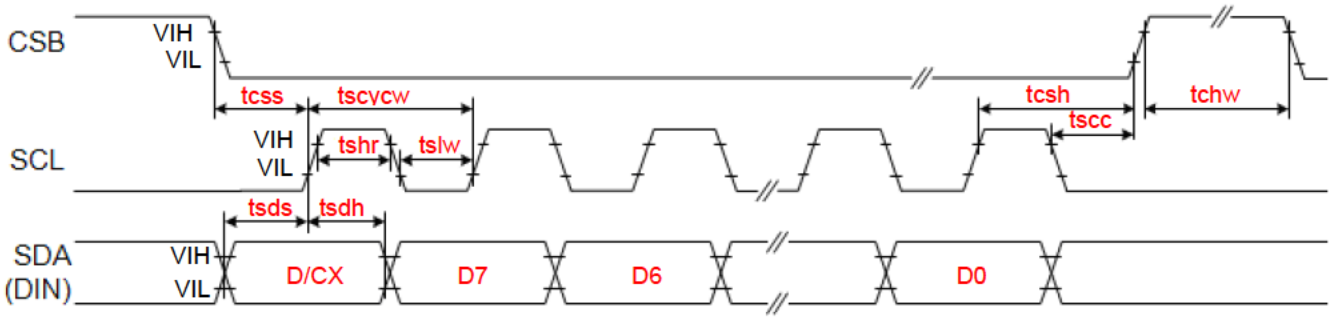


Figure : 3-wire Serial Interface – Write

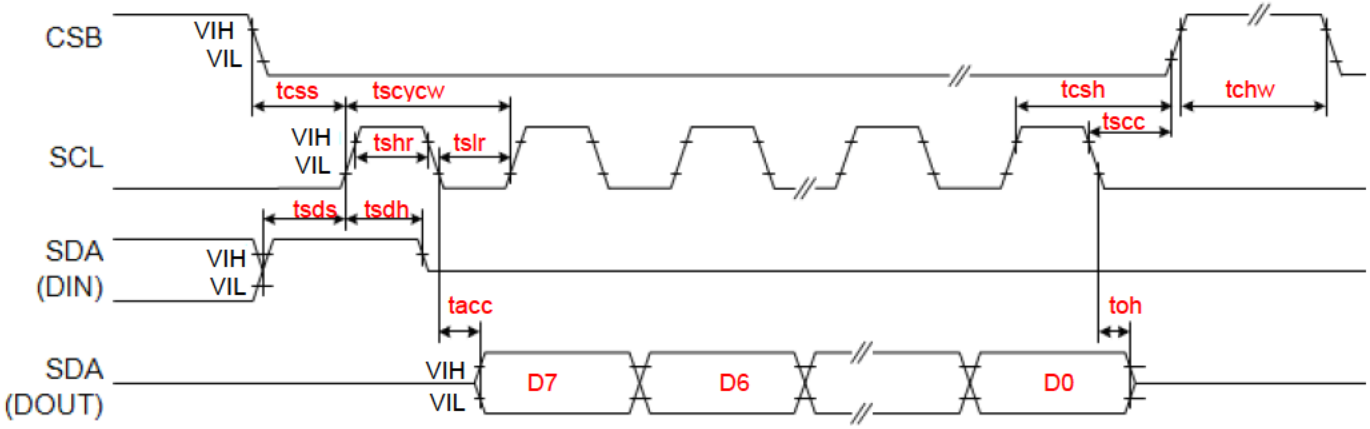
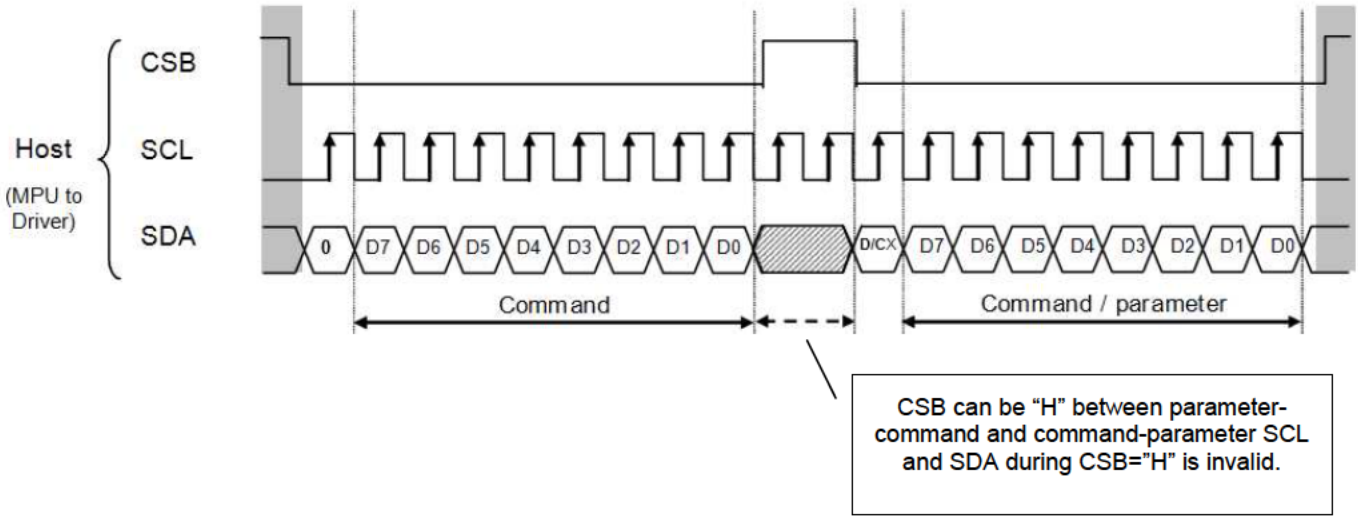


Figure : 3-wire Serial Interface – Read


Host
(MPU to Driver)
CSB
SCL
SDA
0
D7
D6
D5
D4
D3
D2
D1
D0
D/CX
D7
D6
D5
D4
D3
D2
D1
D0
Command
Command / parameter
CSB can be “H” between parameter-command and command-parameter SCL and SDA during CSB=”H” is invalid.

4-WIRE SPI

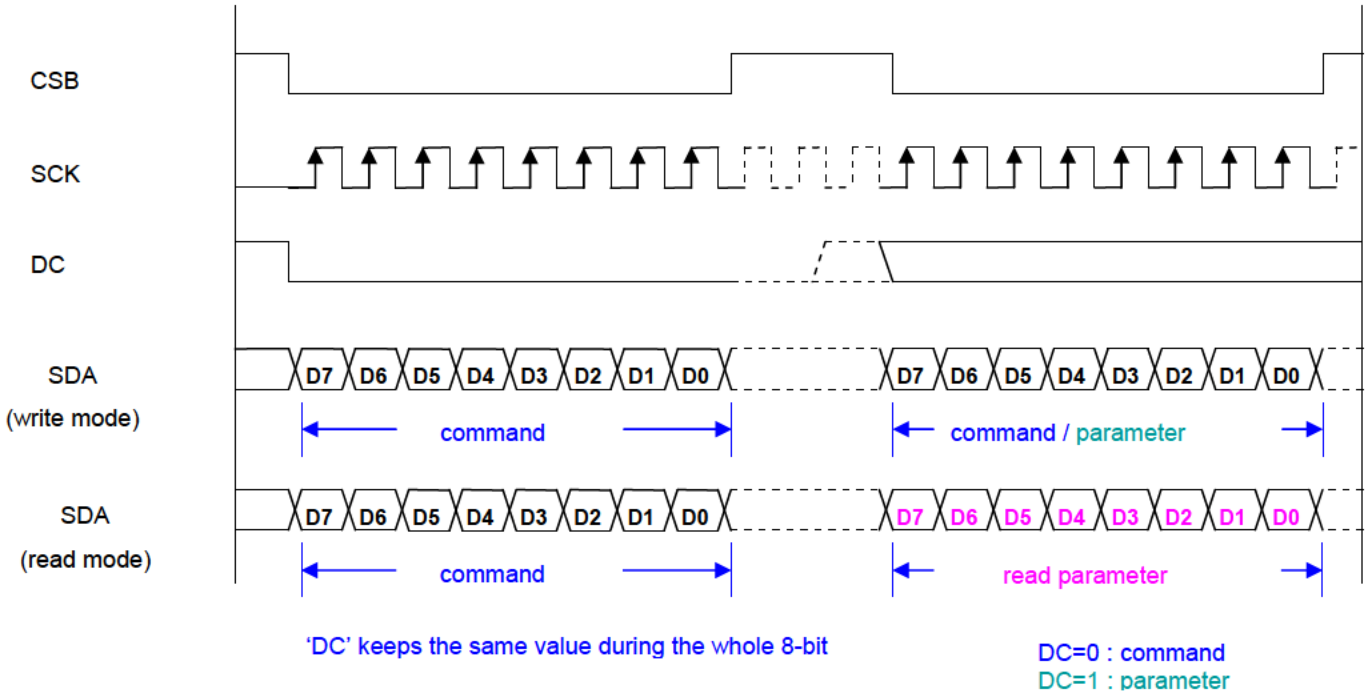


Figure : 4-wire SPI Typical Waveform – BS=0

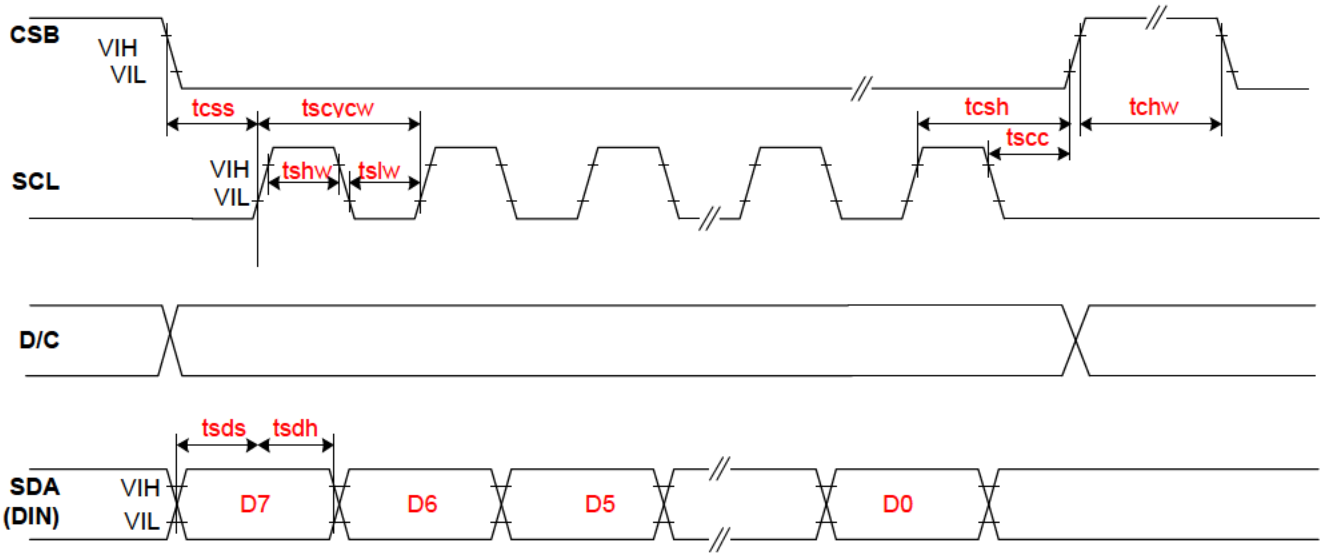
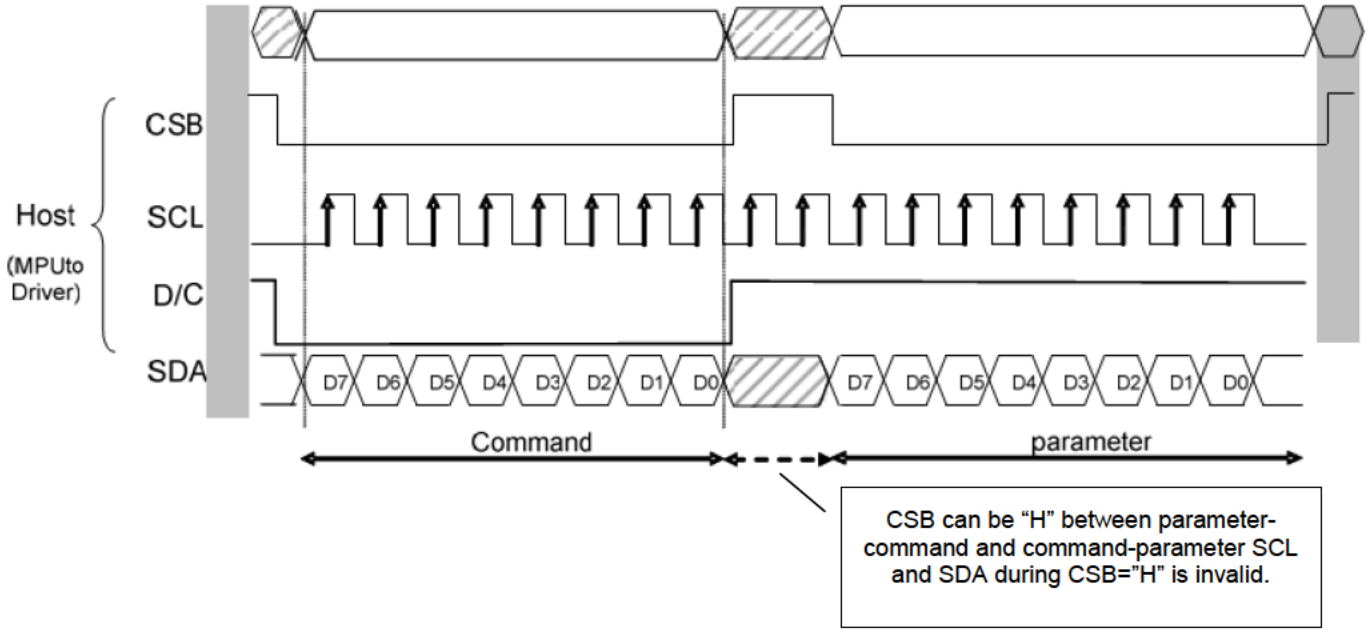
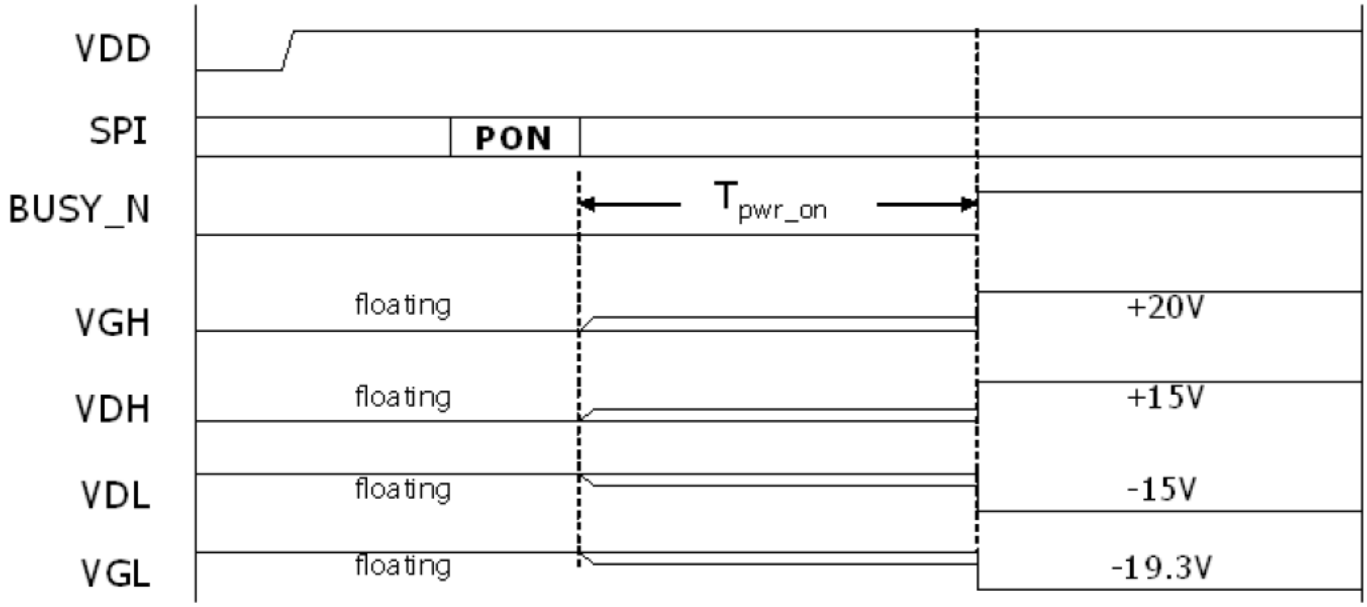


Figure : 4-wire Serial Interface – Read


Host
(MPUto
Driver)
CSB
SCL
D/C
SDA
D7
D6
D5
D4
D3
D2
D1
D0
D7
D6
D5
D4
D3
D2
D1
D0
Command
parameter
CSB can be “H” between parameter-command and command-parameter SCL and SDA during CSB=”H” is invalid.

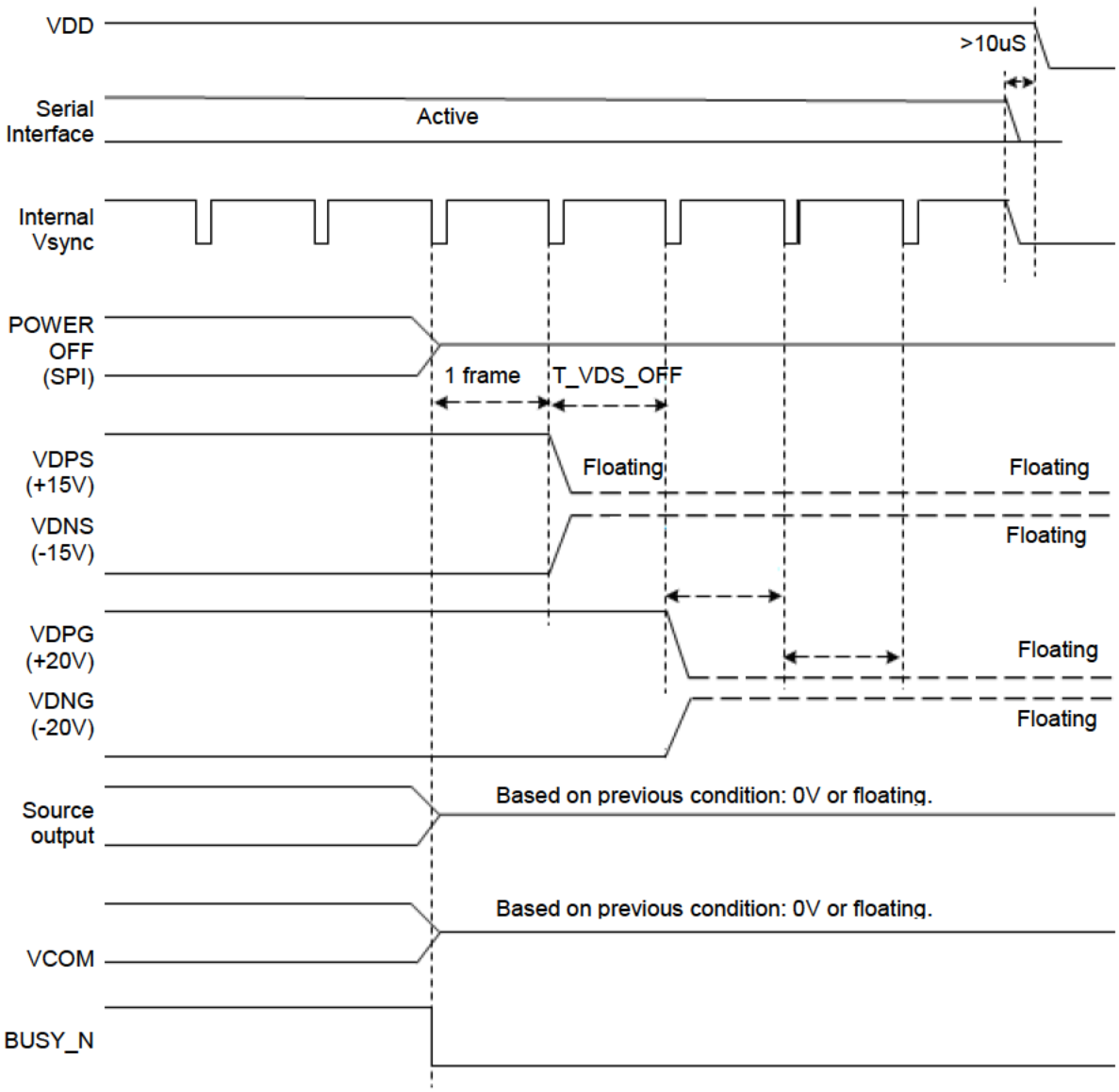
POWER MANAGEMENT

Power ON Sequence



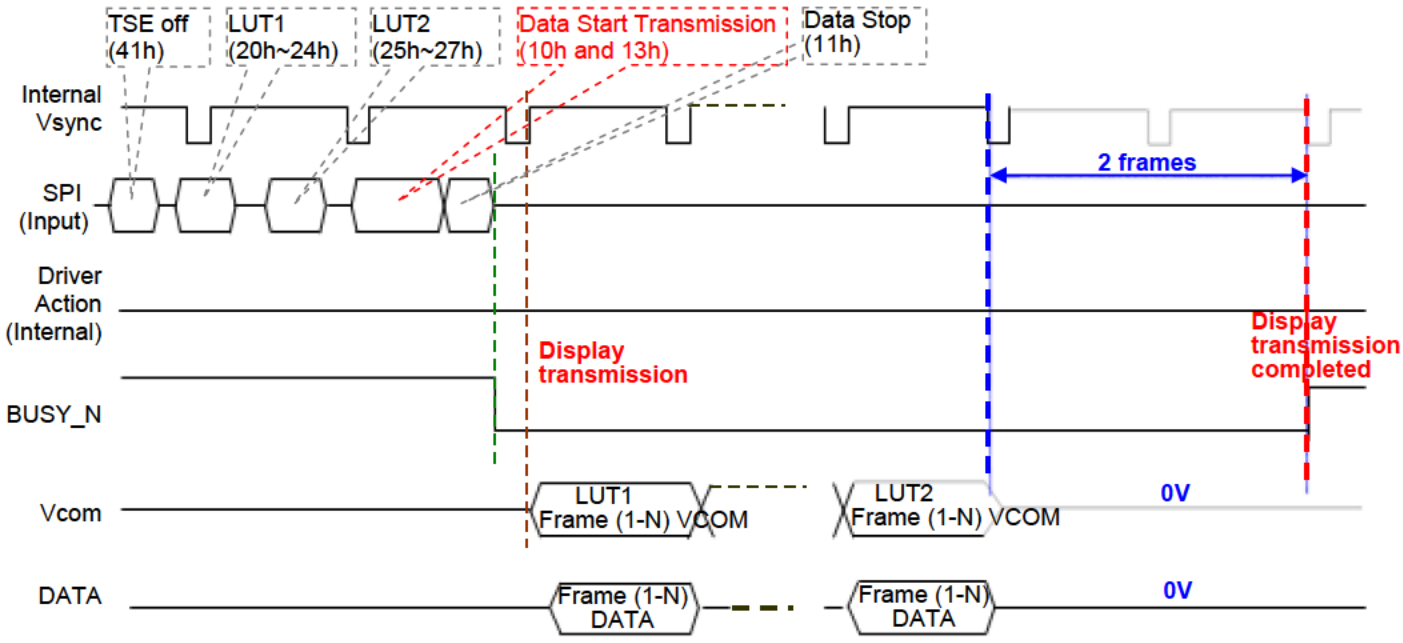
T_{pwr_on} = ~80ms (default)

Power OFF Sequence

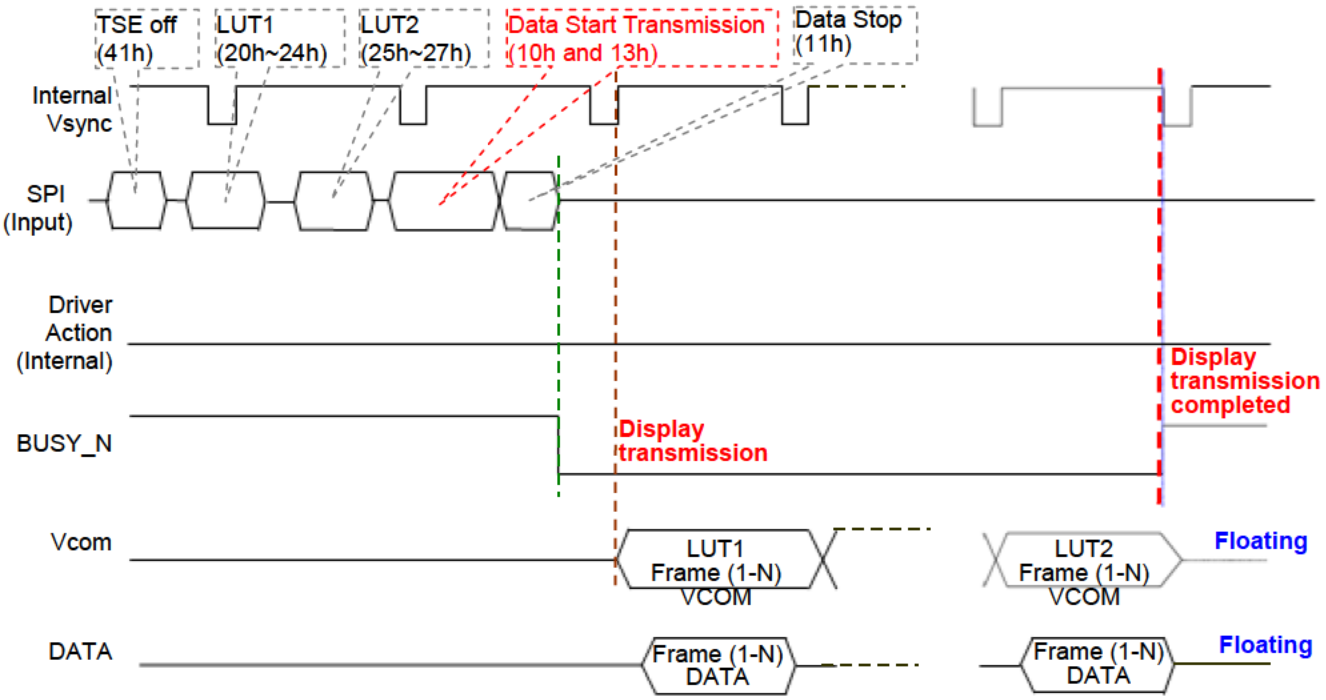


Data Transmission Waveform

Example 1: LUT all states (5 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 V.

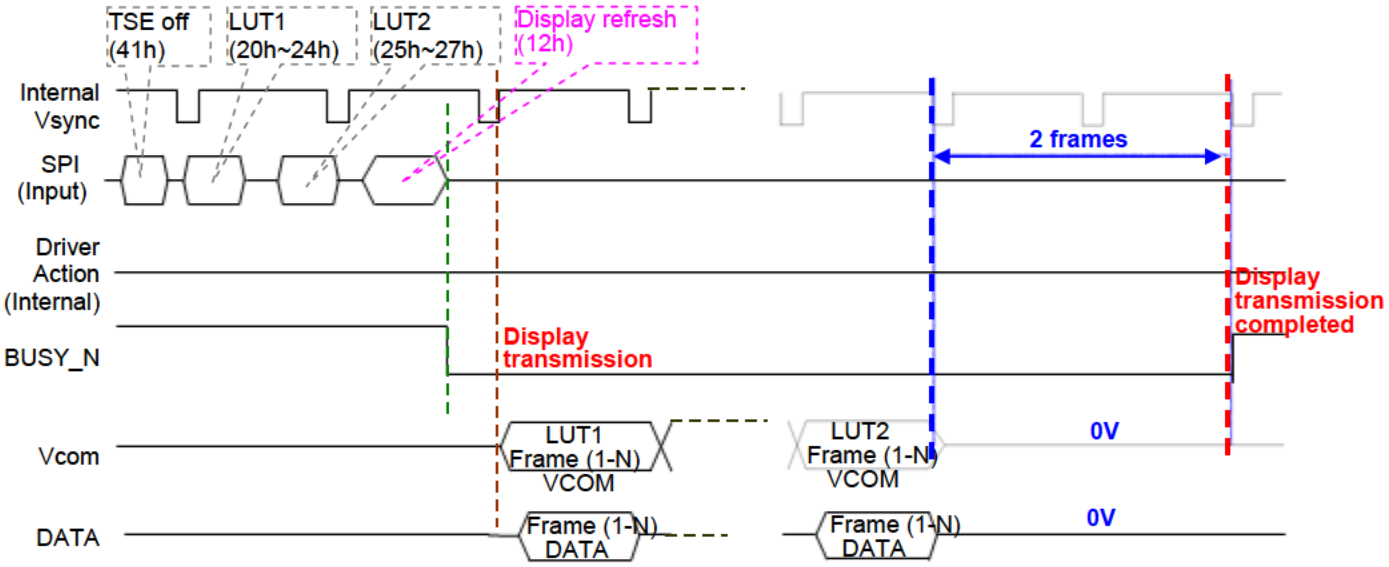


Example 2: While level selection in LUT is "11", the driver will float VCOM and data.

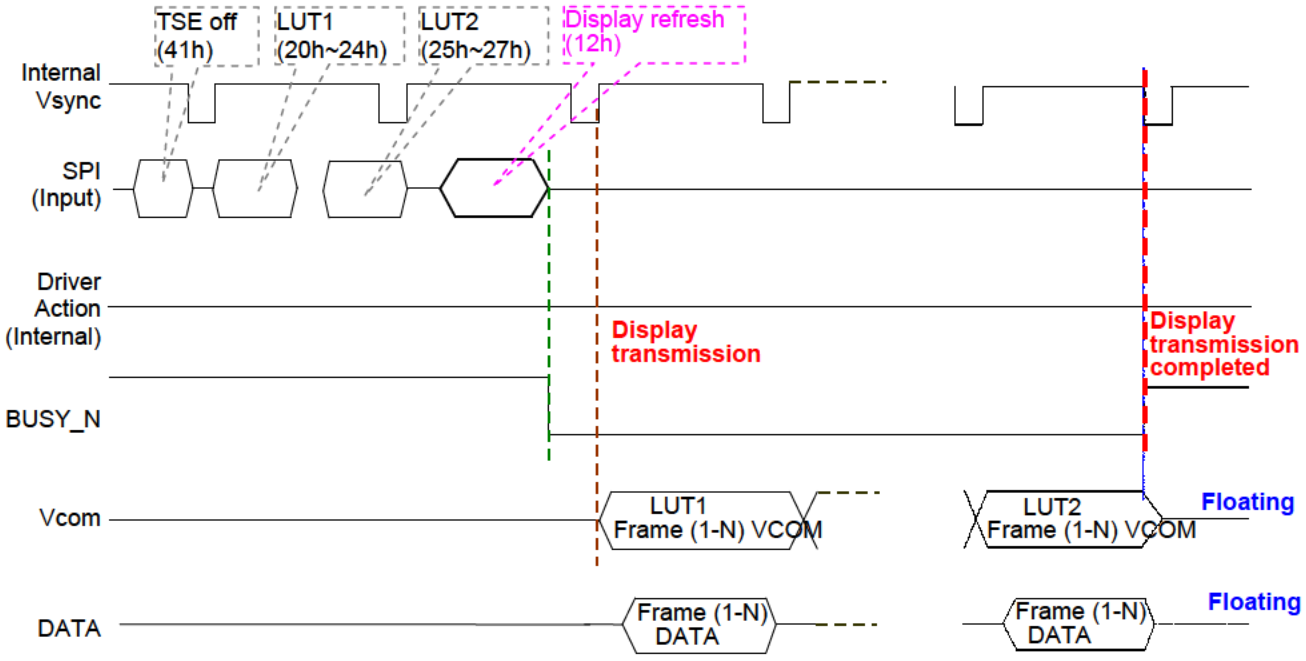


Display Refresh Waveform

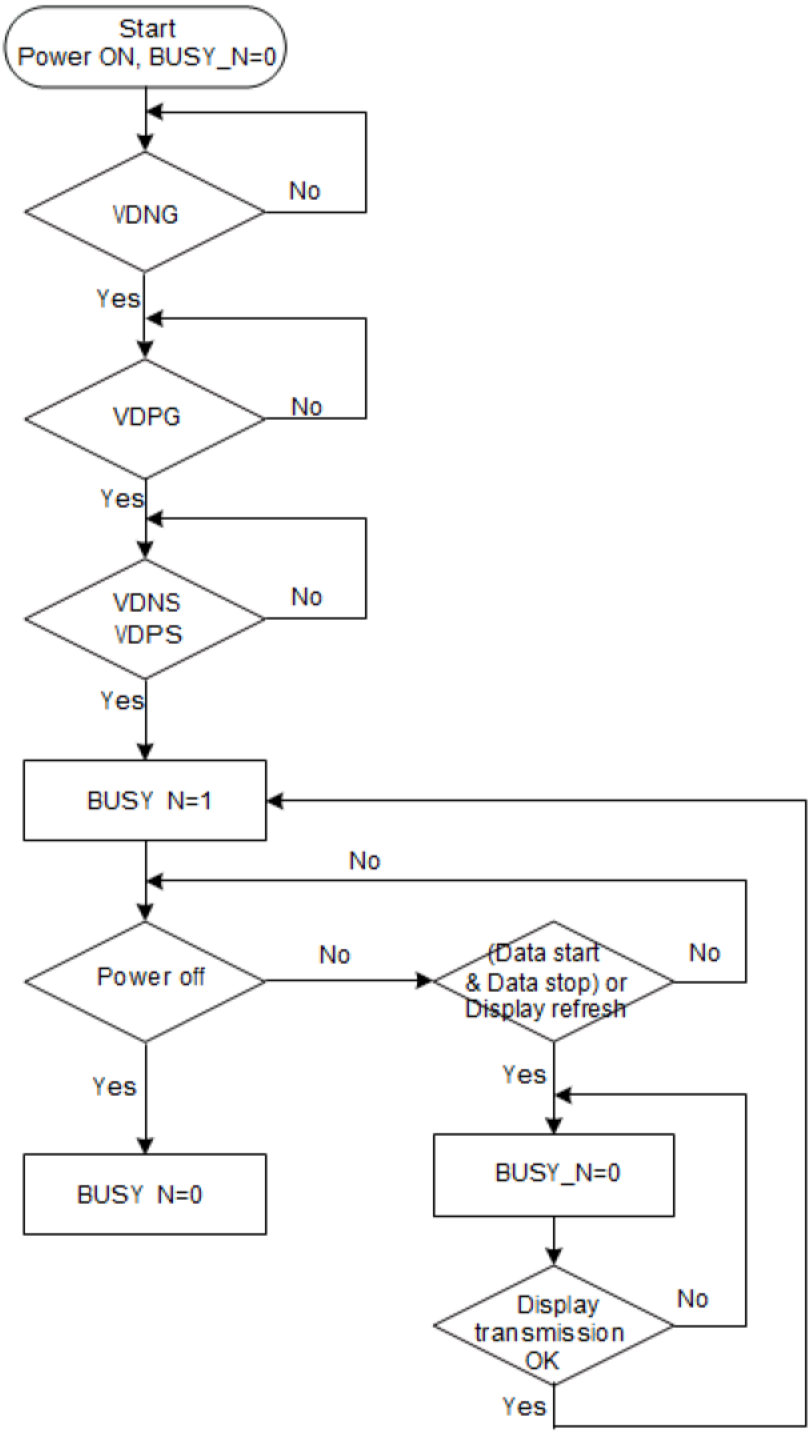
Example 1: LUT all states (5 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 V.



Example2: While level selection in LUT is "11", the driver will float VCOM and data.



BUSY_N Signal Flow Chart



BUSY_N Signal Flow Chart

ABSOLUTE MAXIMUM RATINGS

V_{DD}= 2~3.6V (Typ. 3.3V), GND=0V, VDH=3~9V (Typ. 6V), VDL=0~6V (Typ. 3V), T_A=0~70°C (Typ. 25°C)

Signal	Item	Min	Max.	Unit
V_{DD}, V_{IO}, V_{DD1}, V_{PP}	Logic Supply voltage	- 0.3	+6.0	V
V_I	Digital input range	-0.3	V_{DDIO}+40	V
V_{DPS}-V_{DNS}	Supply range	V_{DNG}-0.3	V_{DPG}+0.3	V
Source				
V_{DPS}	Analog supply voltage – positive	+20		V
V_{DNS}	Analog supply voltage -- nagetive	-20		V
Gate				
V_{DPS}	Analog supply voltage – positive	-0.3	V_{DNG}+40	V
V_{DNS}	Analog supply voltage -- nagetive	V_{DPG}-40	0.3	V
I_{VDPS}	Input rush current for V_{DPS}	(TBD)	(TBD)	mA
I_{VDNS}	Input rush current for V_{DNS}	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	°C

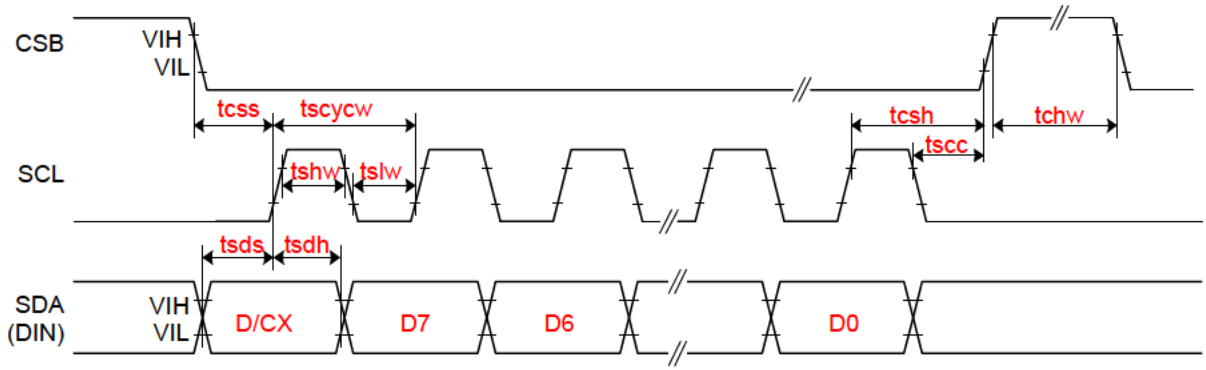
Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

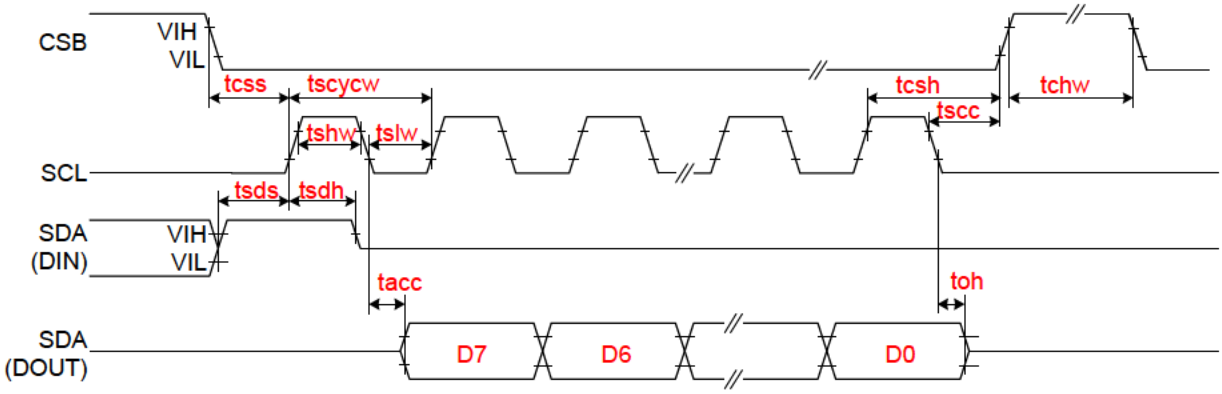
DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
V_{IO}	IO supply voltage		2.3	3.3	3.6	V
V_{DD}	Supply voltage		2.3	3.3	3.6	V
$V_{DD}1$	DCDC driver supply voltage	DRVU, DRVD	2.3	3.3	3.6	V
V_{IL}	LOW Level input voltage	Digital input pins	0	--	0.3xV_{DD}	V
V_{IH}	HIGH Level input voltage	Digital input pins	0.7xV_{IO}	--	V_{IO}	V
V_{OH}	HIGH Level output voltage	Digital input pins, I_{OH}=400uA	V_{IO}-0.4	--	--	V
V_{OHD}	HIGH Level output voltage	Digital input pins, I_{OH}=400uA, DRVD, DRVU	V_{DD}1-0.4	--	--	V
V_{OL}	LOW Level Output voltage	Digital input pins, I_{OL}=-400uA	0	--	0.4	V
I_{IN}	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
I_{SLP}	Sleep Current	V_{DD}=3.3 All stopped (Power OFF mode)			1	mA
R_{IN}	Pull-up/down impedance			200		KΩ
T_{OP}	Operating temperature		-30		85	°C
VDPS	Supply Voltage	For source driver/VCOM		15		V
dVDPS	Supply voltage dev		-300	0	+300	mV
VDNS	Supply Voltage	For source driver/VCOM		-15		V
dVDNS	Supply voltage dev		-300	0	+300	mV
Idd	Analog Operating Current	No load,		TBD		mA
V_{VD}	Voltage Deviation of Outputs		--	±20	±35	mV
V_{DR}	Dynamic Range of Output		0.1	--	VDPS-0.1	V
VDPG-VDNG	Voltage Range of VDPG - VDNG		12		40	V
VDNG	VDNG voltage Range	For gate driver	-20		-17	V
dVDNG	VDNG Supply voltage dev		-400	0	+400	mV
VDPG	VDPG voltage Range	For gate driver	17		VDNG+40	V
dVDPG	VDPG Supply voltage dev		-400	0	+400	mV
Iopr	Operating Current	V_{DD}=3.3 DC/DC ON No waveform transitions No loading No RAM Read/Write		2		mA

AC CHARACTERISTICS



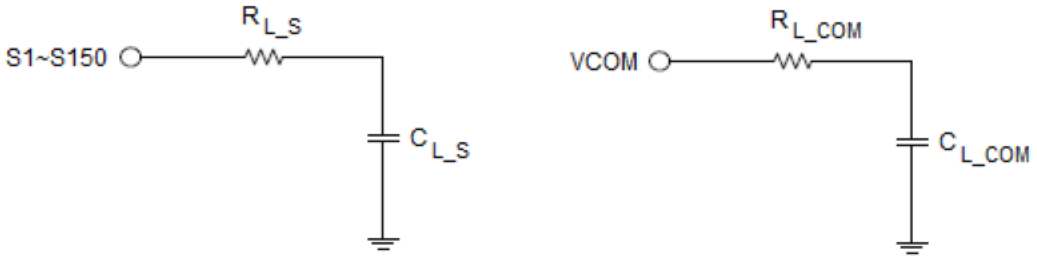
3-wire Serial Interface – Write



3-wire Serial Interface – Read

SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
SERIAL COMMUNICATION							
tCSS	CSB	Chip select setup time		60			ns
tCSH		Chip select hold time		65			ns
tSCC		Chip select setup time		20			ns
tCHW		Chip select setup time		40			ns
tSCYCW	SCL	Serial clock cycle (Write)		100			ns
tSHW		SCL “H” pulse width (Write)		35			ns
tSLW		SCL “L” pulse width (Write)		35			ns
tSCYCR		Serial clock cycle (Read)		150			ns
tSHR		SCL “H” pulse width (Read)		60			ns
tSLR		SCL “L” pulse width (Read)		60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time		30			ns
tSDH		Data hold time		30			ns
tACC		Access time		10			ns
tOH		Output disable time		15			ns

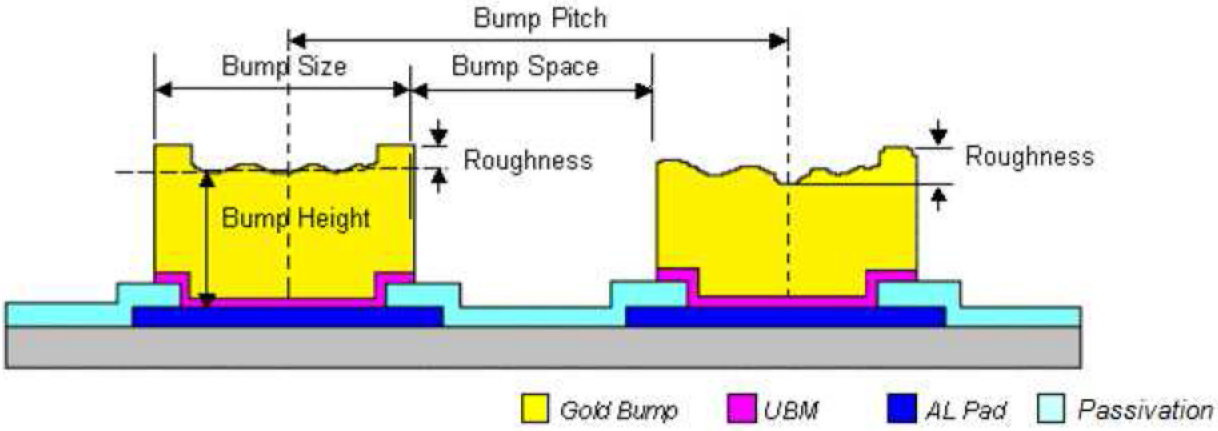
SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
DRIVER							
trS		Source driver rise time	99% final value		5		us
tFS		Source driver fall time			5		us
trG		Gate driver rise time	99% final value		5		us
tFG		Gate driver fall time			5		us
trCOM		VCOM rise time	99% final value		1		ms
tFCOM		VCOM fall time			1		ms
RC LOADING							
RL_S		Source driver output loading			13.362		K Ω
CL_S					39.194		pf
RL_G		Gate driver output loading			12.329		KΩ
CL_G					32.095		pf
RL_com		VCOM output loading			61.26		Ω
CL_com					3365.7		pf

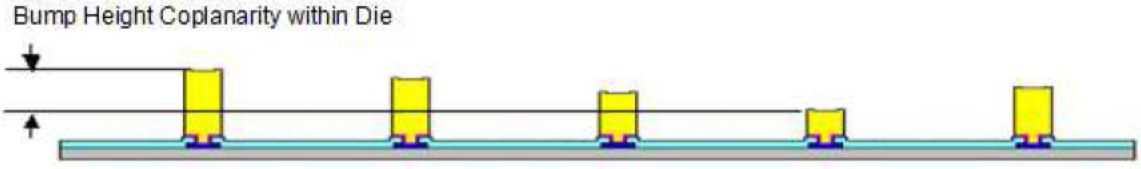


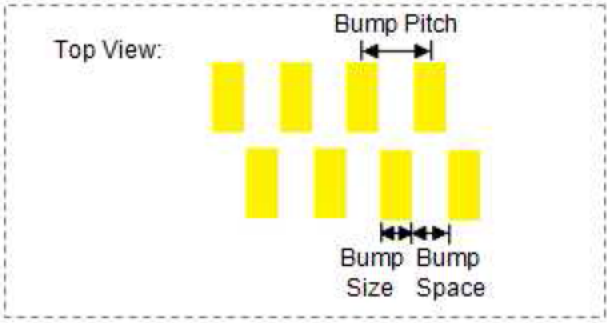
RC Loading

PHYSICAL DIMENSIONS

Die Size:	(13090μM ± 40μM) x (1530μM ± 40μM)
Die Thickness:	300μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ≤ 2μM
Hardness:	65Hv ± 15Hv
Bump Size:	18μM x 75μM ± 2μM
Bump Pitch:	42μM
Bump Gap:	24μM ± 3μM
Bump Area:	1350μM^2
Total Bump Area:	114300μM^2
Area Ratio:	1.761 : 1 (Output pad : Input pad)
	1 : 1 (Side power pad)
Coordinate origin:	Chip center
Pad reference:	Pad center

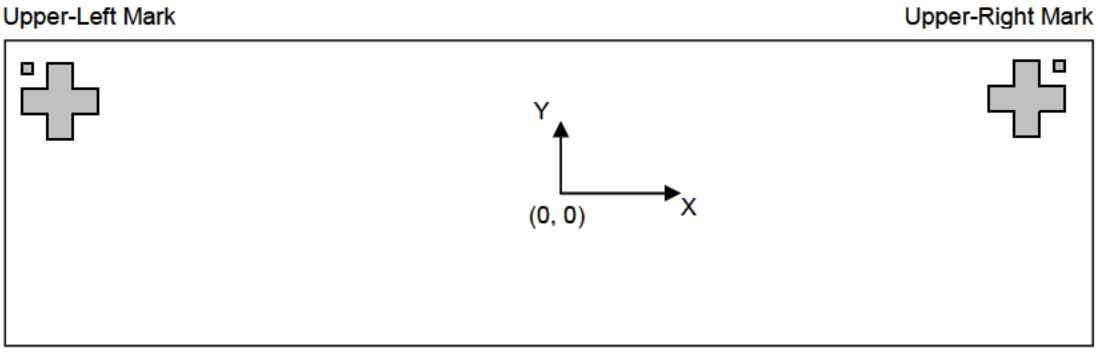




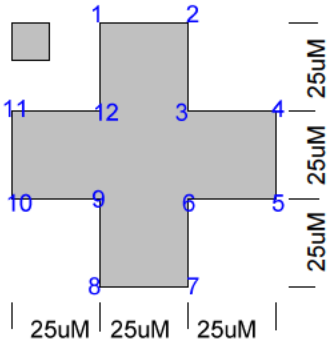


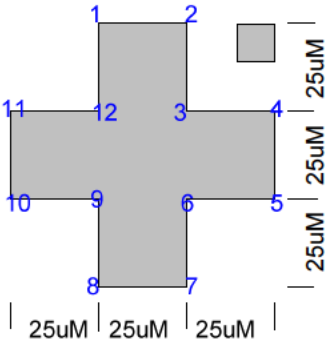
ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:





Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-6382	642	6382	642
1	-6394.5	679.5	6369.5	679.5
2	-6369.5	679.5	6394.5	679.5
3	-6369.5	654.5	6394.5	654.5
4	-6344.5	654.5	6419.5	654.5
5	-6344.5	629.5	6419.5	629.5
6	-6369.5	629.5	6394.5	629.5
7	-6369.5	604.5	6394.5	604.5
8	-6394.5	604.5	6369.5	604.5
9	-6394.5	629.5	6369.5	629.5
10	-6419.5	629.5	6344.5	629.5
11	-6419.5	654.5	6344.5	654.5
12	-6394.5	654.5	6369.5	654.5

PAD COORDINATES

No.	Name	X	Y	W	H
1	NC	-6180	-680	40	50
2	VCOM	-6120	-680	40	50
3	VCOM	-6060	-680	40	50
4	VCOM	-6000	-680	40	50
5	VCOM	-5940	-680	40	50
6	VCOM	-5880	-680	40	50
7	VCOM	-5820	-680	40	50
8	VCOM	-5760	-680	40	50
9	VCOM	-5700	-680	40	50
10	VDM	-5640	-680	40	50
11	VGL	-5580	-680	40	50
12	VGL	-5520	-680	40	50
13	VGL	-5460	-680	40	50
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15	VGL	-5340	-680	40	50
16	VGL	-5280	-680	40	50
17	VGL	-5220	-680	40	50
18	VGL	-5160	-680	40	50
19	VGL	-5100	-680	40	50
20	VGL	-5040	-680	40	50
21	VGL	-4980	-680	40	50
22	VGL	-4920	-680	40	50
23	VGL	-4860	-680	40	50
24	VGL	-4800	-680	40	50
25	VGL	-4740	-680	40	50
26	VGL	-4680	-680	40	50
27	GNDA	-4620	-680	40	50
28	VSL	-4560	-680	40	50
29	VSL	-4500	-680	40	50
30	VSL	-4440	-680	40	50
31	VSL	-4380	-680	40	50
32	VSL	-4320	-680	40	50
33	VSL	-4260	-680	40	50
34	VSL	-4200	-680	40	50
35	VSL	-4140	-680	40	50
36	VSL	-4080	-680	40	50
37	VSL	-4020	-680	40	50
38	GNDA	-3960	-680	40	50
39	VGH	-3900	-680	40	50
40	VGH	-3840	-680	40	50
42	VGH	-3780	-680	40	50
41	VGH	-3720	-680	40	50
43	VGH	-3660	-680	40	50
44	VGH	-3600	-680	40	50
45	VGH	-3540	-680	40	50
46	VGH	-3480	-680	40	50
47	VGH	-3420	-680	40	50
48	VGH	-3360	-680	40	50
49	VGH	-3300	-680	40	50
50	VGH	-3240	-680	40	50
51	GNDA	-3180	-680	40	50
52	VSH	-3120	-680	40	50
53	VSH	-3060	-680	40	50
54	VSH	-3000	-680	40	50
55	VSH	-2940	-680	40	50
56	VSH	-2880	-680	40	50
57	VSH	-2820	-680	40	50
58	VSH	-2760	-680	40	50

No.	Name	X	Y	W	H
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60	VSH	-2640	-680	40	50
61	VSH	-2580	-680	40	50
62	GNDA	-2520	-680	40	50
63	DUMMY	-2460	-680	40	50
64	DUMMY	-2400	-680	40	50
65	DUMMY	-2340	-680	40	50
66	DUMMY	-2280	-680	40	50
67	DUMMY	-2220	-680	40	50
68	DUMMY	-2160	-680	40	50
69	DUMMY	-2100	-680	40	50
70	DUMMY	-2040	-680	40	50
71	DUMMY	-1980	-680	40	50
72	DUMMY	-1920	-680	40	50
73	DUMMY	-1860	-680	40	50
74	DUMMY	-1800	-680	40	50
75	DUMMY	-1740	-680	40	50
76	DUMMY	-1680	-680	40	50
77	DUMMY	-1620	-680	40	50
78	DUMMY	-1560	-680	40	50
79	GND	-1500	-680	40	50
80	VDM	-1440	-680	40	50
81	VDM	-1380	-680	40	50
82	GND	-1320	-680	40	50
83	GND	-1260	-680	40	50
84	GND	-1200	-680	40	50
85	GND	-1140	-680	40	50
86	GND	-1080	-680	40	50
87	GND	-1020	-680	40	50
88	GND	-960	-680	40	50
89	GND	-900	-680	40	50
90	GND	-840	-680	40	50
91	GND	-780	-680	40	50
92	GND	-720	-680	40	50
93	GNDA	-660	-680	40	50
94	GNDA	-600	-680	40	50
95	GNDA	-540	-680	40	50
96	GNDA	-480	-680	40	50
97	GNDA	-420	-680	40	50
98	GNDA	-360	-680	40	50
99	GNDA	-300	-680	40	50
100	GNDA	-240	-680	40	50
101	GNDA	-180	-680	40	50
102	GNDA	-120	-680	40	50
103	VDDA	-60	-680	40	50
104	VDDA	0	-680	40	50
105	VDDA	60	-680	40	50
106	VDDA	120	-680	40	50
107	VDDA	180	-680	40	50
108	VDDA	240	-680	40	50
109	VDDA	300	-680	40	50
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112	VDDA	480	-680	40	50
113	VDD	540	-680	40	50
114	VDD	600	-680	40	50
115	VDD	660	-680	40	50
116	VDD	720	-680	40	50

No.	Name	X	Y	W	H
117	VDD	780	-680	40	50
118	VDD	840	-680	40	50
119	VDD	900	-680	40	50
120	TEST1	960	-680	40	50
121	TEST2	1020	-680	40	50
122	VDDIO	1080	-680	40	50
123	VDDIO	1140	-680	40	50
124	VDDIO	1200	-680	40	50
125	VDDIO	1260	-680	40	50
126	TEST3	1320	-680	40	50
127	DUMMY	1380	-680	40	50
128	DUMMY	1440	-680	40	50
129	DUMMY	1500	-680	40	50
130	DUMMY	1560	-680	40	50
131	DUMMY	1620	-680	40	50
132	SDA	1680	-680	40	50
133	SCL	1740	-680	40	50
134	GND	1800	-680	40	50
135	CSB	1860	-680	40	50
136	VDDIO	1920	-680	40	50
137	DUMMY	1980	-680	40	50
138	GND	2040	-680	40	50
139	DC	2100	-680	40	50
140	VDDIO	2160	-680	40	50
141	DUMMY	2220	-680	40	50
142	GND	2280	-680	40	50
143	RST_N	2340	-680	40	50
144	BUSY_N	2400	-680	40	50
145	CL	2460	-680	40	50
146	VDDIO	2520	-680	40	50
147	VSYNC	2580	-680	40	50
148	GND	2640	-680	40	50
149	DUMMY	2700	-680	40	50
150	VDDIO	2760	-680	40	50
151	BS	2820	-680	40	50
152	GND	2880	-680	40	50
153	DUMMY	2940	-680	40	50
154	VDDIO	3000	-680	40	50
155	DUMMY	3060	-680	40	50
156	GND	3120	-680	40	50
157	MS	3180	-680	40	50
158	VDDIO	3240	-680	40	50
159	TSDA	3300	-680	40	50
160	TSDA	3360	-680	40	50
161	TSCL	3420	-680	40	50
162	TSCL	3480	-680	40	50
163	TEST4	3540	-680	40	50
164	TEST5	3600	-680	40	50
165	TEST6	3660	-680	40	50
166	TEST7	3720	-680	40	50
167	VGH	3780	-680	40	50
168	VGH	3840	-680	40	50
169	VGH	3900	-680	40	50
170	VGH	3960	-680	40	50
171	VGH	4020	-680	40	50
172	VGH	4080	-680	40	50
173	VGH	4140	-680	40	50
174	VGH	4200	-680	40	50
175	VGL	4260	-680	40	50
176	VGL	4320	-680	40	50

No.	Name	X	Y	W	H
177	VGL	4380	-680	40	50
178	VGL	4440	-680	40	50
179	VGL	4500	-680	40	50
180	VGL	4560	-680	40	50
181	VGL	4620	-680	40	50
182	VGL	4680	-680	40	50
183	GNDA	4740	-680	40	50
184	FB	4800	-680	40	50
185	FB	4860	-680	40	50
186	GNDA	4920	-680	40	50
187	RESE	4980	-680	40	50
188	RESE	5040	-680	40	50
189	GNDA	5100	-680	40	50
190	GDR	5160	-680	40	50
191	GDR	5220	-680	40	50
192	GDR	5280	-680	40	50
193	GDR	5340	-680	40	50
194	GDR	5400	-680	40	50
195	GDR	5460	-680	40	50
196	GDR	5520	-680	40	50
197	GDR	5580	-680	40	50
198	VDM	5640	-680	40	50
199	VCOM	5700	-680	40	50
200	VCOM	5760	-680	40	50
201	VCOM	5820	-680	40	50
202	VCOM	5880	-680	40	50
203	VCOM	5940	-680	40	50
204	VCOM	6000	-680	40	50
205	VCOM	6060	-680	40	50
206	VCOM	6120	-680	40	50
207	NC	6180	-680	40	50
208	NC	6170	561.5	18	75
209	NC	6149	681.5	18	75
210	NC	6128	561.5	18	75
211	NC	6107	681.5	18	75
212	NC	6086	561.5	18	75
213	NC	6065	681.5	18	75
214	G<0>	6044	561.5	18	75
215	G<2>	6023	681.5	18	75
216	G<4>	6002	561.5	18	75
217	G<6>	5981	681.5	18	75
218	G<8>	5960	561.5	18	75
219	G<10>	5939	681.5	18	75
220	G<12>	5918	561.5	18	75
221	G<14>	5897	681.5	18	75
222	G<16>	5876	561.5	18	75
223	G<18>	5855	681.5	18	75
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225	G<22>	5813	681.5	18	75
226	G<24>	5792	561.5	18	75
227	G<26>	5771	681.5	18	75
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229	G<30>	5729	681.5	18	75
230	G<32>	5708	561.5	18	75
231	G<34>	5687	681.5	18	75
232	G<36>	5666	561.5	18	75
233	G<38>	5645	681.5	18	75
234	G<40>	5624	561.5	18	75
235	G<42>	5603	681.5	18	75
236	G<44>	5582	561.5	18	75

No.	Name	X	Y	W	H
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238	G<48>	5540	561.5	18	75
239	G<50>	5519	681.5	18	75
240	G<52>	5498	561.5	18	75
241	G<54>	5477	681.5	18	75
242	G<56>	5456	561.5	18	75
243	G<58>	5435	681.5	18	75
244	G<60>	5414	561.5	18	75
245	G<62>	5393	681.5	18	75
246	G<64>	5372	561.5	18	75
247	G<66>	5351	681.5	18	75
248	G<68>	5330	561.5	18	75
249	G<70>	5309	681.5	18	75
250	G<72>	5288	561.5	18	75
251	G<74>	5267	681.5	18	75
252	G<76>	5246	561.5	18	75
253	G<78>	5225	681.5	18	75
254	G<80>	5204	561.5	18	75
255	G<82>	5183	681.5	18	75
256	G<84>	5162	561.5	18	75
257	G<86>	5141	681.5	18	75
258	G<88>	5120	561.5	18	75
259	G<90>	5099	681.5	18	75
260	G<92>	5078	561.5	18	75
261	G<94>	5057	681.5	18	75
262	G<96>	5036	561.5	18	75
263	G<98>	5015	681.5	18	75
264	G<100>	4994	561.5	18	75
265	G<102>	4973	681.5	18	75
266	G<104>	4952	561.5	18	75
267	G<106>	4931	681.5	18	75
268	G<108>	4910	561.5	18	75
269	G<110>	4889	681.5	18	75
270	G<112>	4868	561.5	18	75
271	G<114>	4847	681.5	18	75
272	G<116>	4826	561.5	18	75
273	G<118>	4805	681.5	18	75
274	G<120>	4784	561.5	18	75
275	G<122>	4763	681.5	18	75
276	G<124>	4742	561.5	18	75
277	G<126>	4721	681.5	18	75
278	G<128>	4700	561.5	18	75
279	G<130>	4679	681.5	18	75
280	G<132>	4658	561.5	18	75
281	G<134>	4637	681.5	18	75
282	G<136>	4616	561.5	18	75
283	G<138>	4595	681.5	18	75
284	G<140>	4574	561.5	18	75
285	G<142>	4553	681.5	18	75
286	G<144>	4532	561.5	18	75
287	G<146>	4511	681.5	18	75
288	G<148>	4490	561.5	18	75
289	G<150>	4469	681.5	18	75
290	G<152>	4448	561.5	18	75
291	G<154>	4427	681.5	18	75
292	G<156>	4406	561.5	18	75
293	G<158>	4385	681.5	18	75
294	G<160>	4364	561.5	18	75
295	G<162>	4343	681.5	18	75
296	G<164>	4322	561.5	18	75

No.	Name	X	Y	W	H
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298	G<168>	4280	561.5	18	75
299	G<170>	4259	681.5	18	75
300	G<172>	4238	561.5	18	75
301	G<174>	4217	681.5	18	75
302	G<176>	4196	561.5	18	75
303	G<178>	4175	681.5	18	75
304	G<180>	4154	561.5	18	75
305	G<182>	4133	681.5	18	75
306	G<184>	4112	561.5	18	75
307	G<186>	4091	681.5	18	75
308	G<188>	4070	561.5	18	75
309	G<190>	4049	681.5	18	75
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311	G<194>	4007	681.5	18	75
312	G<196>	3986	561.5	18	75
313	G<198>	3965	681.5	18	75
314	G<200>	3944	561.5	18	75
315	G<202>	3923	681.5	18	75
316	G<204>	3902	561.5	18	75
317	G<206>	3881	681.5	18	75
318	G<208>	3860	561.5	18	75
319	G<210>	3839	681.5	18	75
320	G<212>	3818	561.5	18	75
321	G<214>	3797	681.5	18	75
322	G<216>	3776	561.5	18	75
323	G<218>	3755	681.5	18	75
324	G<220>	3734	561.5	18	75
325	G<222>	3713	681.5	18	75
326	G<224>	3692	561.5	18	75
327	G<226>	3671	681.5	18	75
328	G<228>	3650	561.5	18	75
329	G<230>	3629	681.5	18	75
330	G<232>	3608	561.5	18	75
331	G<234>	3587	681.5	18	75
332	G<236>	3566	561.5	18	75
333	G<238>	3545	681.5	18	75
334	G<240>	3524	561.5	18	75
335	G<242>	3503	681.5	18	75
336	G<244>	3482	561.5	18	75
337	G<246>	3461	681.5	18	75
338	G<248>	3440	561.5	18	75
339	G<250>	3419	681.5	18	75
340	G<252>	3398	561.5	18	75
341	G<254>	3377	681.5	18	75
342	G<256>	3356	561.5	18	75
343	G<258>	3335	681.5	18	75
344	G<260>	3314	561.5	18	75
345	G<262>	3293	681.5	18	75
346	G<264>	3272	561.5	18	75
347	G<266>	3251	681.5	18	75
348	G<268>	3230	561.5	18	75
349	G<270>	3209	681.5	18	75
350	G<272>	3188	561.5	18	75
351	G<274>	3167	681.5	18	75
352	G<276>	3146	561.5	18	75
353	G<278>	3125	681.5	18	75
354	G<280>	3104	561.5	18	75
355	G<282>	3083	681.5	18	75
356	G<284>	3062	561.5	18	75

No.	Name	X	Y	W	H
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359	G<290>	2999	681.5	18	75
360	G<292>	2978	561.5	18	75
361	G<294>	2957	681.5	18	75
362	G<296>	2936	561.5	18	75
363	G<298>	2915	681.5	18	75
364	NC	2893	561.5	18	75
365	NC	2871	681.5	18	75
366	NC	2849	561.5	18	75
367	NC	2827	681.5	18	75
368	NC	2805	561.5	18	75
369	NC	2783	681.5	18	75
370	NC	2761	561.5	18	75
371	NC	2739	681.5	18	75
372	NC	2717	561.5	18	75
373	NC	2695	681.5	18	75
374	NC	2673	561.5	18	75
375	NC	2343	681.5	18	75
376	NC	2321	561.5	18	75
377	VBD<1>	2299	681.5	18	75
378	S<0>	2277	561.5	18	75
379	S<1>	2255	681.5	18	75
380	S<2>	2233	561.5	18	75
381	S<3>	2211	681.5	18	75
382	S<4>	2189	561.5	18	75
383	S<5>	2167	681.5	18	75
384	S<6>	2145	561.5	18	75
385	S<7>	2123	681.5	18	75
386	S<8>	2101	561.5	18	75
387	S<9>	2079	681.5	18	75
388	S<10>	2057	561.5	18	75
389	S<11>	2035	681.5	18	75
390	S<12>	2013	561.5	18	75
391	S<13>	1991	681.5	18	75
392	S<14>	1969	561.5	18	75
393	S<15>	1947	681.5	18	75
394	S<16>	1925	561.5	18	75
395	S<17>	1903	681.5	18	75
396	S<18>	1881	561.5	18	75
397	S<19>	1859	681.5	18	75
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400	S<22>	1793	561.5	18	75
401	S<23>	1771	681.5	18	75
402	S<24>	1749	561.5	18	75
403	S<25>	1727	681.5	18	75
404	S<26>	1705	561.5	18	75
405	S<27>	1683	681.5	18	75
406	S<28>	1661	561.5	18	75
407	S<29>	1639	681.5	18	75
408	S<30>	1617	561.5	18	75
409	S<31>	1595	681.5	18	75
410	S<32>	1573	561.5	18	75
411	S<33>	1551	681.5	18	75
412	S<34>	1529	561.5	18	75
413	S<35>	1507	681.5	18	75
414	S<36>	1485	561.5	18	75
415	S<37>	1463	681.5	18	75
416	S<38>	1441	561.5	18	75

No.	Name	X	Y	W	H
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418	S<40>	1397	561.5	18	75
419	S<41>	1375	681.5	18	75
420	S<42>	1353	561.5	18	75
421	S<43>	1331	681.5	18	75
422	S<44>	1309	561.5	18	75
423	S<45>	1287	681.5	18	75
424	S<46>	1265	561.5	18	75
425	S<47>	1243	681.5	18	75
426	S<48>	1221	561.5	18	75
427	S<49>	1199	681.5	18	75
428	S<50>	1177	561.5	18	75
429	S<51>	1155	681.5	18	75
430	S<52>	1133	561.5	18	75
431	S<53>	1111	681.5	18	75
432	S<54>	1089	561.5	18	75
433	S<55>	1067	681.5	18	75
434	S<56>	1045	561.5	18	75
435	S<57>	1023	681.5	18	75
436	S<58>	1001	561.5	18	75
437	S<59>	979	681.5	18	75
438	S<60>	957	561.5	18	75
439	S<61>	935	681.5	18	75
440	S<62>	913	561.5	18	75
441	S<63>	891	681.5	18	75
442	S<64>	869	561.5	18	75
443	S<65>	847	681.5	18	75
444	S<66>	825	561.5	18	75
445	S<67>	803	681.5	18	75
446	S<68>	781	561.5	18	75
447	S<69>	759	681.5	18	75
448	S<70>	737	561.5	18	75
449	S<71>	715	681.5	18	75
450	S<72>	693	561.5	18	75
451	S<73>	671	681.5	18	75
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453	S<75>	627	681.5	18	75
454	S<76>	605	561.5	18	75
455	S<77>	583	681.5	18	75
456	S<78>	561	561.5	18	75
457	S<79>	539	681.5	18	75
458	S<80>	517	561.5	18	75
459	S<81>	495	681.5	18	75
460	S<82>	473	561.5	18	75
461	S<83>	451	681.5	18	75
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No.	Name	X	Y	W	H
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714	G<55>	-5477	561.5	18	75
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716	G<51>	-5519	561.5	18	75

No.	Name	X	Y	W	H
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720	G<43>	-5603	561.5	18	75
721	G<41>	-5624	681.5	18	75
722	G<39>	-5645	561.5	18	75
723	G<37>	-5666	681.5	18	75
724	G<35>	-5687	561.5	18	75
725	G<33>	-5708	681.5	18	75
726	G<31>	-5729	561.5	18	75
727	G<29>	-5750	681.5	18	75
728	G<27>	-5771	561.5	18	75
729	G<25>	-5792	681.5	18	75
730	G<23>	-5813	561.5	18	75
731	G<21>	-5834	681.5	18	75
732	G<19>	-5855	561.5	18	75

No.	Name	X	Y	W	H
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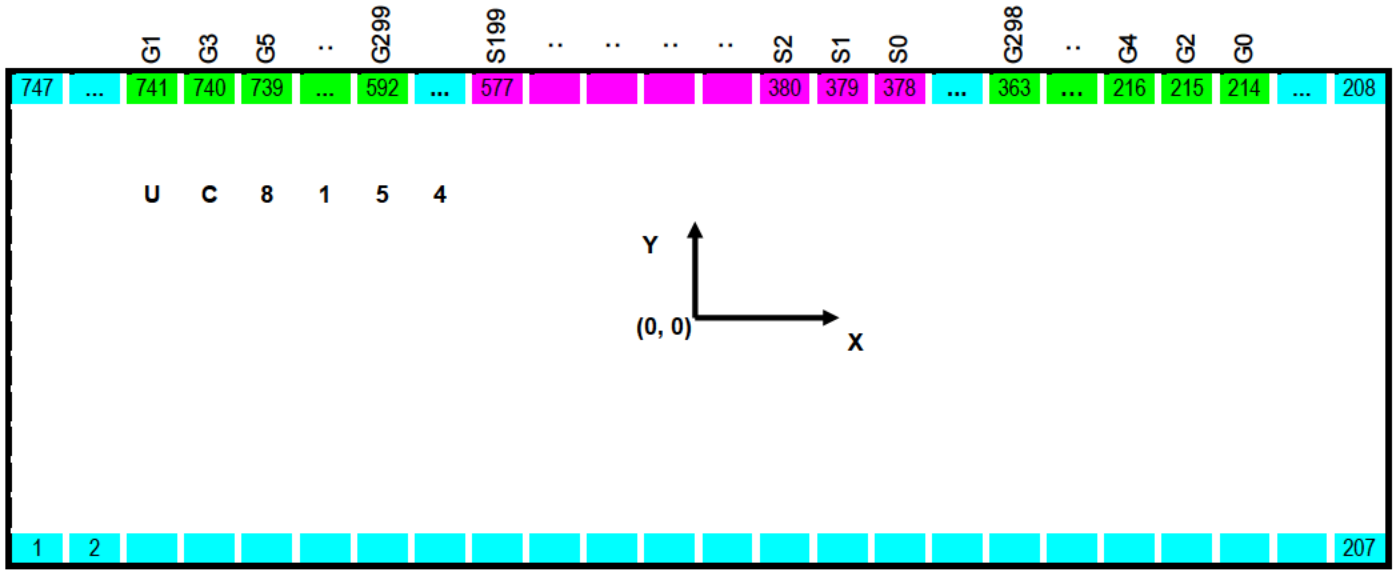
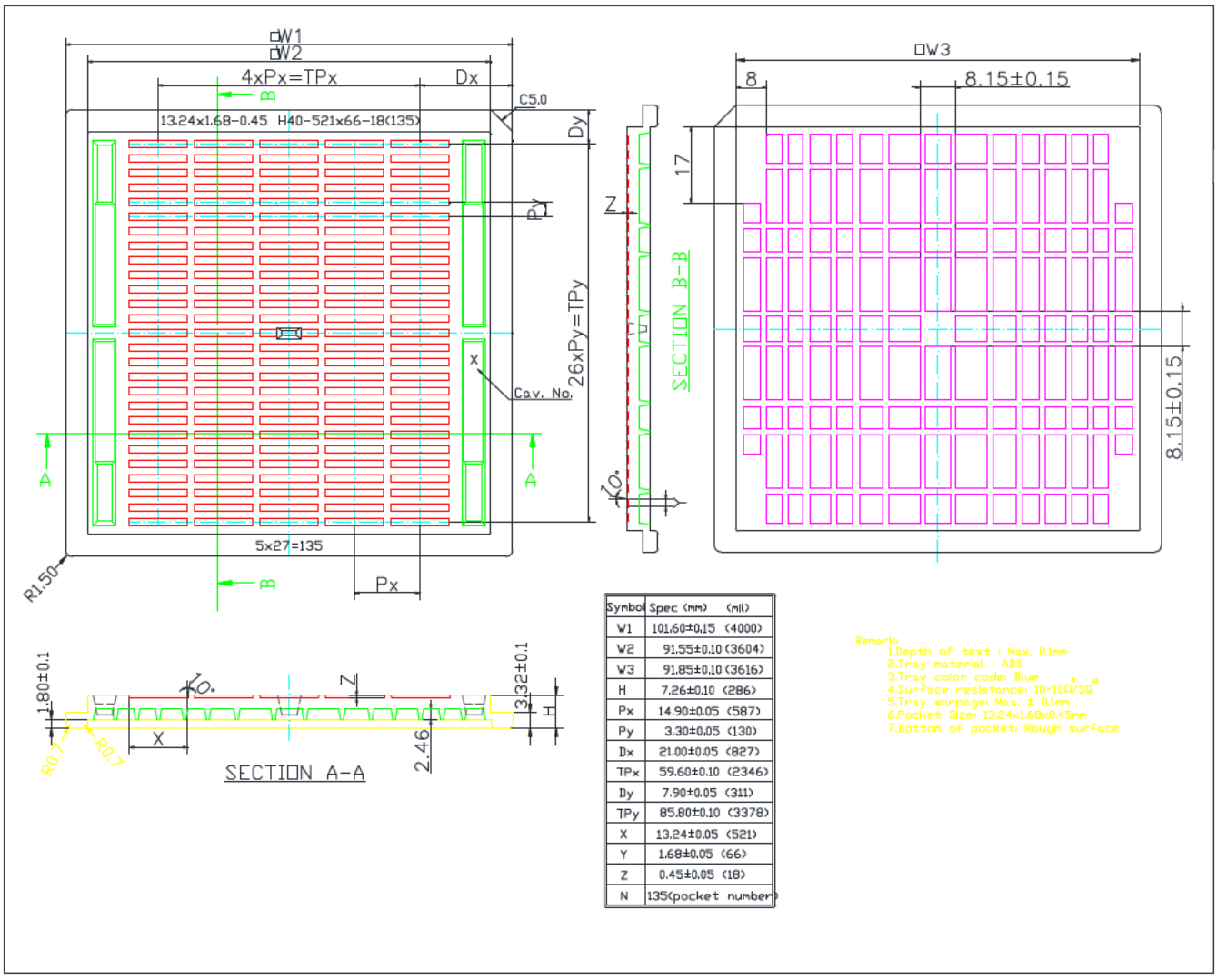


TRAY INFORMATION



Symbol	Spec (mm) (mil)
W1	101.60±0.15 (4000)
W2	91.55±0.10 (3604)
W3	91.85±0.10 (3616)
H	7.26±0.10 (286)
Px	14.90±0.05 (587)
Py	3.30±0.05 (130)
Dx	21.00±0.05 (827)
TPx	59.60±0.10 (2346)
Dy	7.90±0.05 (311)
TPy	85.80±0.10 (3378)
X	13.24±0.05 (521)
Y	1.68±0.05 (66)
Z	0.45±0.05 (18)
N	135(pocket number)

Remark:
1.Depth of text : Max. 0.1mm
2.Tray material : ABS
3.Tray color code: Blue
4.Surface resistance: 10~10Ω/SQ
5.Tray warpage: Max. ± 0.1mm
6.Pocket Size: 13.24x1.68x0.45mm
7.Bottom of pocket: Rough surface