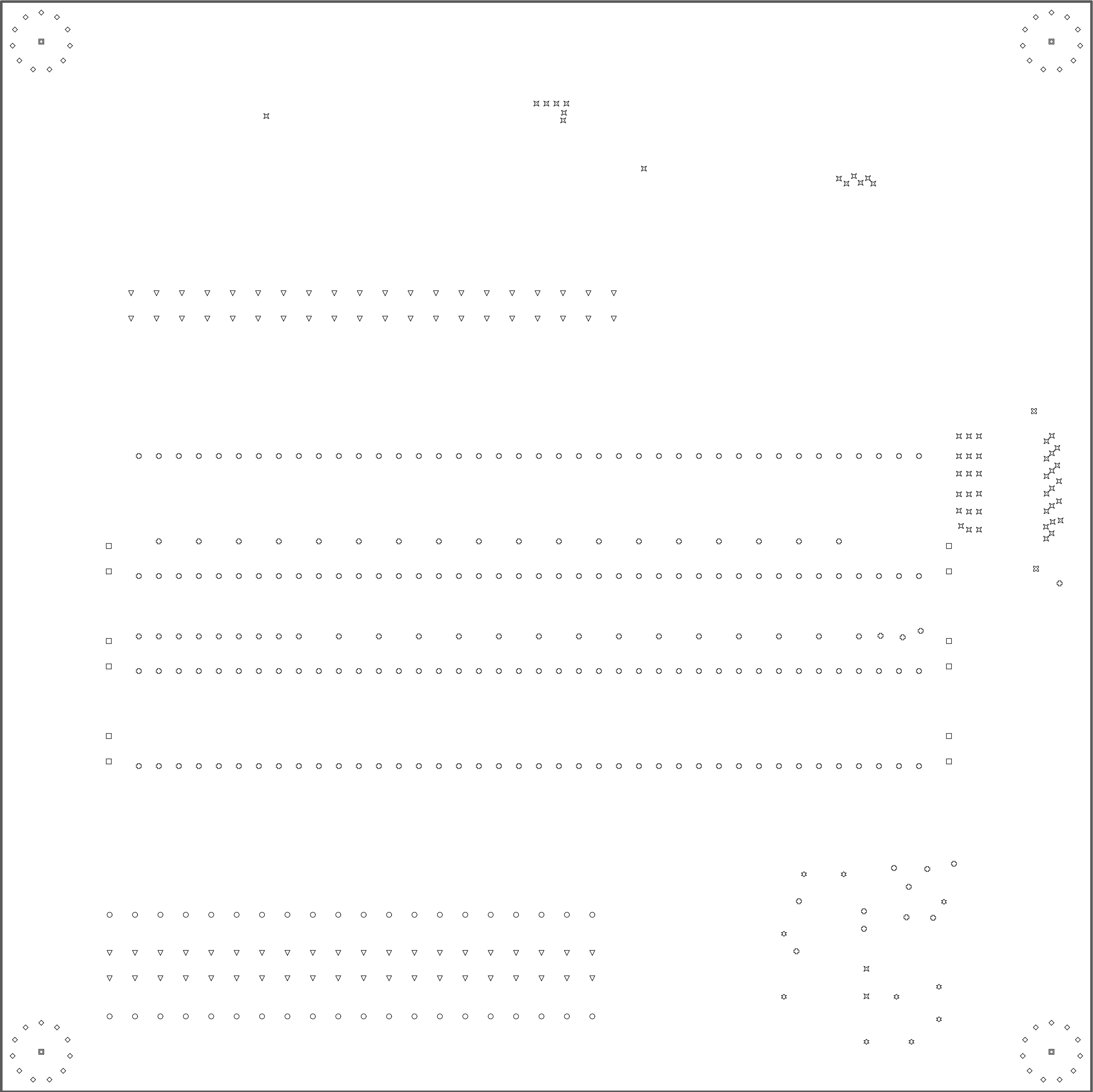


Symbol	Count	Hole Size	Plated	Drill Layer Pair	Pad Shape
⌘	53	0.254mm (10.00mil)	PTH	Top Layer - Bottom Layer	Rounded
⊗	215	0.381mm (15.00mil)	PTH	Top Layer - Bottom Layer	Rounded
◇	44	0.400mm (15.75mil)	PTH	Top Layer - Bottom Layer	Rounded
⊗	2	0.508mm (20.00mil)	PTH	Top Layer - Bottom Layer	Rounded
☆	10	0.711mm (28.00mil)	PTH	Top Layer - Bottom Layer	Rounded
□	12	0.889mm (35.00mil)	PTH	Top Layer - Bottom Layer	Rounded
▽	80	1.020mm (40.16mil)	PTH	Top Layer - Bottom Layer	(Mixed)
○	40	1.100mm (43.31mil)	PTH	Top Layer - Bottom Layer	(Mixed)
■	4	4.000mm (157.48mil)	PTH	Top Layer - Bottom Layer	Rounded
	460 Total				




LAYERS: 2  
MATERIAL: FR4, RoHS, 94v0  
THICKNESS: 1.6mm (~62 mils)  
FINISH: Gold (ENIG) RoHS  
SILK SCREEN: White  
SOLDER MASK: GREEN  
COPPER WEIGHT: 1oz

>> IMPORTANT FABRICATION NOTES <<

- 1) Many pads have intentional undersize solder mask openings/oversize pads for physical strength.
- 2) Make top and bottom solder masks exactly as shown. Do \_NOT\_ "open-up" the solder mask layers. This design uses "solder-mask-defined-pads".
- 3) Silkscreened Legend (white) must be clean and clear. Silkscreen legend must have good registration. Silkscreen is intentionally placed over bare copper. Do not clip silkscreen to solder mask layer.

BARE TRACE BEYOND EDGE IS INTENTIONAL  
ESD HANDLING FEATURE. ROUTING WILL  
TRIM COPPER TO EXACT BOARD OUTLINE.  
SEE "CFA10100\_0v2\_PCB\_Preview.pdf"  
Edge plating is not required.



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PROJECT

CFA-10102

VERSION

0v2

PCB

PCB10102

REVISION

0v2

DATE

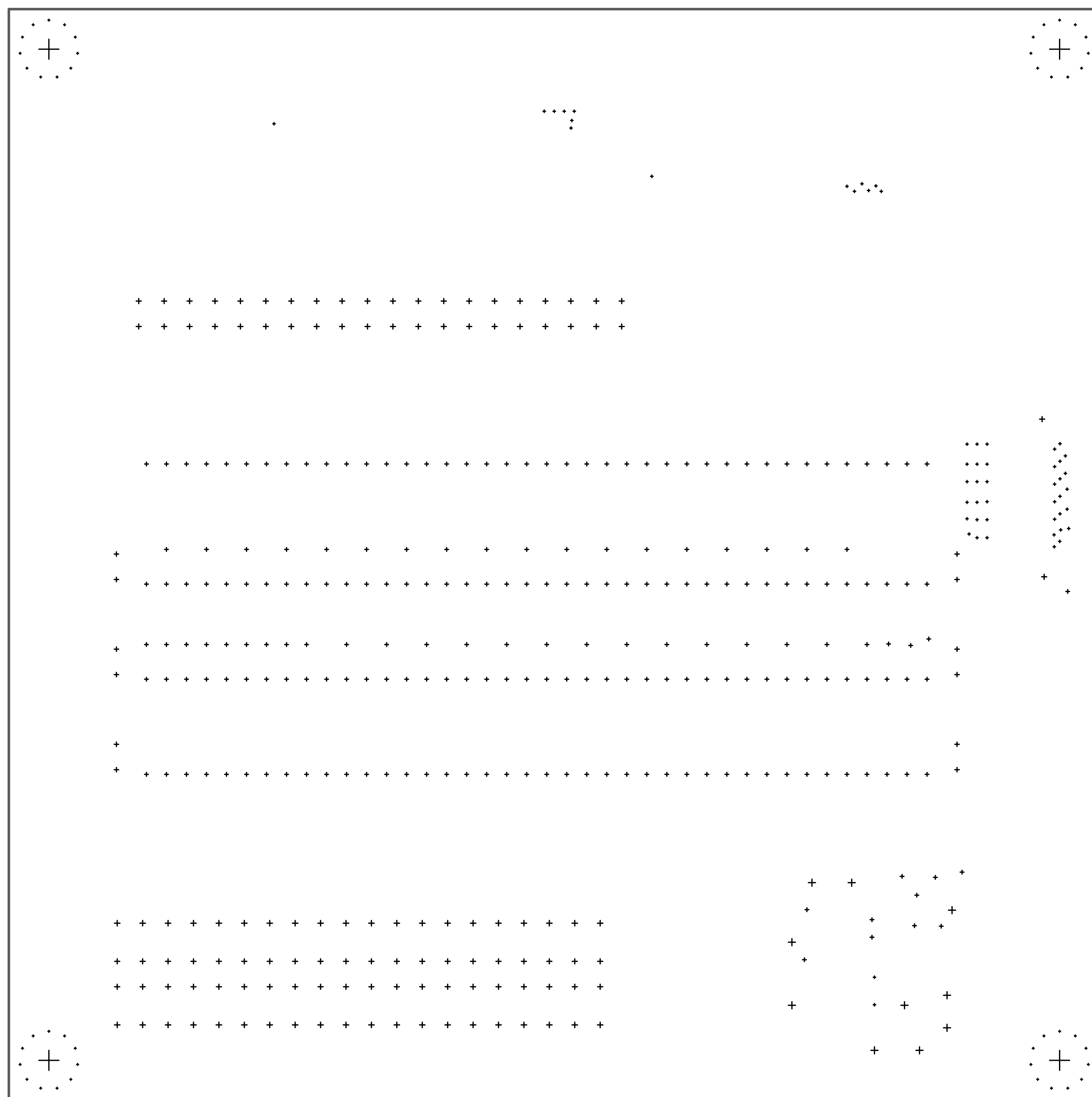
2019-12-13

LAYER

Drill Drawing/Notes

FILE NAME

CFA10102\_0v1.GD1



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PROJECT	CFA-10102	VERSION	0v2
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PCB	REVISION	DATE
PCB10102	0v2	2019-12-13

LAYER
Drill Guide

FILE NAME
CFA10102_0v1.GG1

