DATA SHEET

SAP1024B

Dot Matrix STN LCD Controller with 1024-byte Font ROM

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1 GENERAL

1.1 Description

The SAP1024B is a dot-matrix STN LCD controller. It is desinged to be used together with SEGMENT drivers, COMMON drivers, and Display data SRAM to build a complete display system for STN LCD modules.

The SAP1024B has on-chip font ROM. Each font is composed of 8 dots x 8 dots, and totally 128 fonts are available on-chip. The fonts are pre-defined during chip fabrication.

The SAP1024B has 16-bit address bus and necessary control bus to interface to an external Display Memory of up to 64K bytes. Text data, graphic data, or both can be freely allocated to the Display Memory. In addition to storing text data and graphic data, user-definable fonts can also be stored on the Display Memory. The maximum number of user-definable fonts is 256.

The SAP1024B has an 8-bit data bus and necessary control bus to interface to a host microcontroller. The host microcontroller, via the SAP1024B, can send commands to the SAP1024B, such that the SAP1024B can perform various display operation. User-definable fonts can also be written to the Display Memory via the SAP1024B. Many types of microcontrollers, such as 80C51 or Z80, can easily interface to the SAP1024B.

A wide variety of LCD panels are surpported. Both the number of characters in horizontal direction (columns) and the number of characters in vertical direction (lines) are hardware-programmable. Number of dots of a font in both the horizontal direction and vertical direction is also hardware-programmable. In addition, the actual number of displayed columns can be adjusted via software programming.

The following diagram shows a typical SAP1024B-based dot-matrix STN display system. Please note that interface between the microcontroller and the SAP1024B may be different for different types of microcontroller.

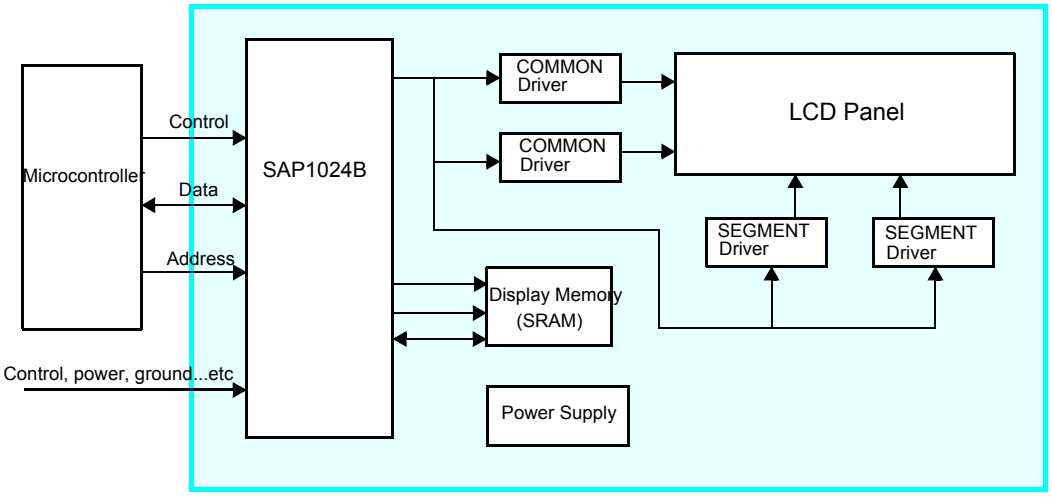


Fig.1 A SAP1024B-based dot-matrix STN LCD display system

2 FEATURES

- Display format (pin-selectable)
  - Columns : 32, 40, 64, 80 (number of characters in X-direction.)
  - Lines : 2, 4, 6, 8, 10, 12, 14, 16, 20, 24, 28, 32 (number of characters in Y-direction.)
- Character font:
  - Horizontal dots : 5, 6, 7, 8 (pin-selectable)
  - Vertical dots : 8 (fixed, that is, always 8 dots in the vertical direction.)
- Display duty : 1/16 to 1/128
- 128 on-chip fonts, with each font having 8-dots x 8-dots.
- Interface to external Display Memory of up to 64K bytes.
- Memory space in Display Memory for text area, graphic area and font generator area can be freely allocated via softeware programming of related registers.
- 256 user-definable fonts on the external Display Memory.
- Read/Write operations between the host microcontroller and the SAP1024B do not disturb the display.
- On-chip crystal oscillator.
- Attribute functions, such as blinking and reverse display, for text display.
- Logical OR, AND, and EXOR operation between text display and graphic display.
- 1~8 raster scan lines for cursor pattern
- 8-bit parrallel interface with a host microcontroller.
- Read/Write operation between the host microcontroller and the SAP1024B for status check, command, and data.
- Operating voltage range (control logic): 2.7 ~ 5.5 volts..
- Operating frequency range: 5.5 MHz, when V_{DD}= 5 volts.
- Operating temperature range: -20 to +70 °C.
- Storage temperature range: -55 to +125 °C.

3 ORDERING INFORMATION

Table 1 Ordering information

TYPE NUMBER	DESCRIPTION
SAP1024B-0101-LQFPG	Code 0101, LQFP67 Pb-free package.
SAP1024B-0101-QFPG	Code 0101, QFP67 Pb-free package.
SAP1024B-0101-LQFP	Code 0101, LQFP67 general package.
SAP1024B-0101-QFP	Code 0101, QFP67 general package.
SAP1024B-customer code	Font ROM codes can also be custom-made.

4 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

4.1 Funtional block diagram

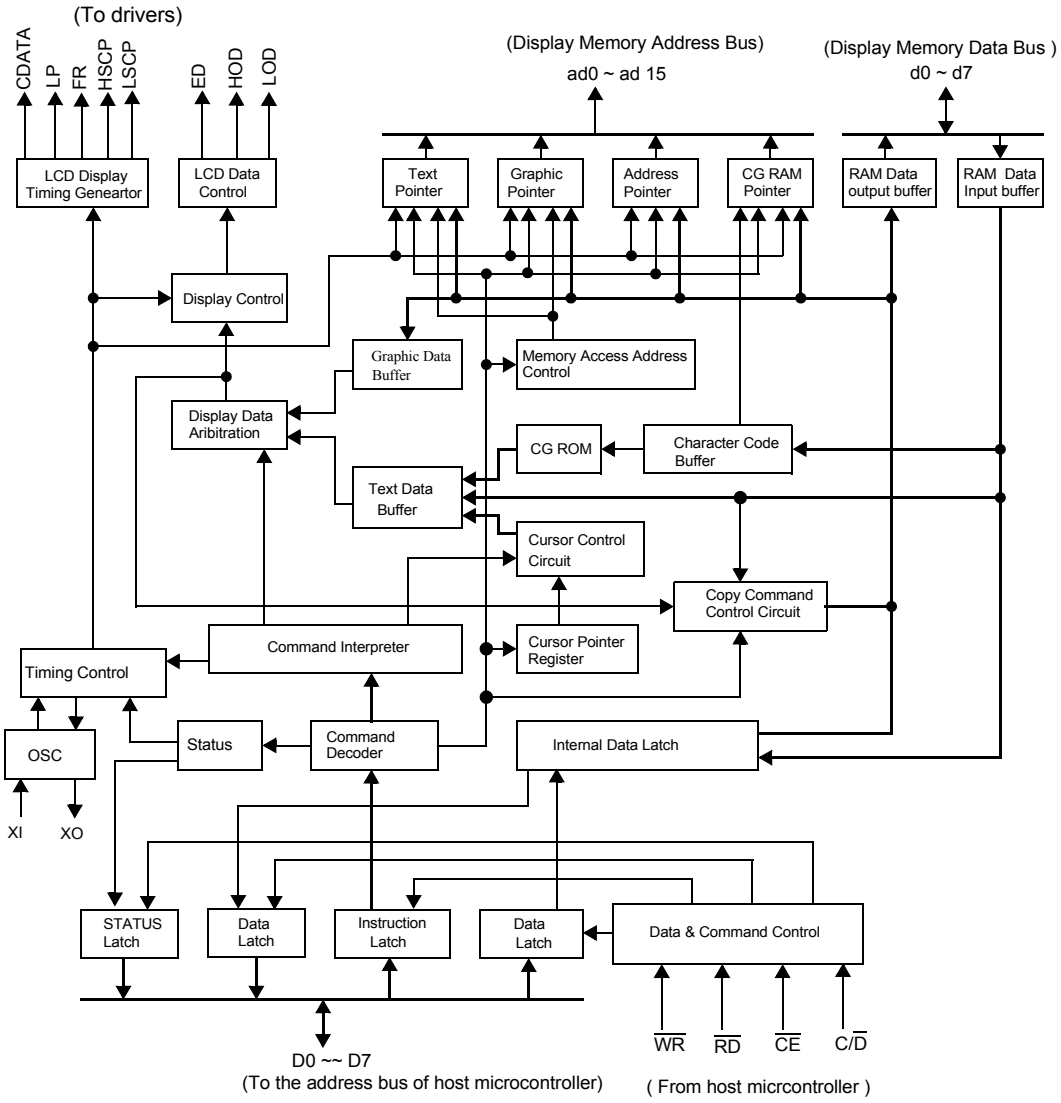


Fig.2 Functional diagram

5 PIN ASSIGNMENT, PAD PLACEMENT AND COORDINATES, SIGNAL DESCRIPTION

5.1 Pin assignment (LQFP67)

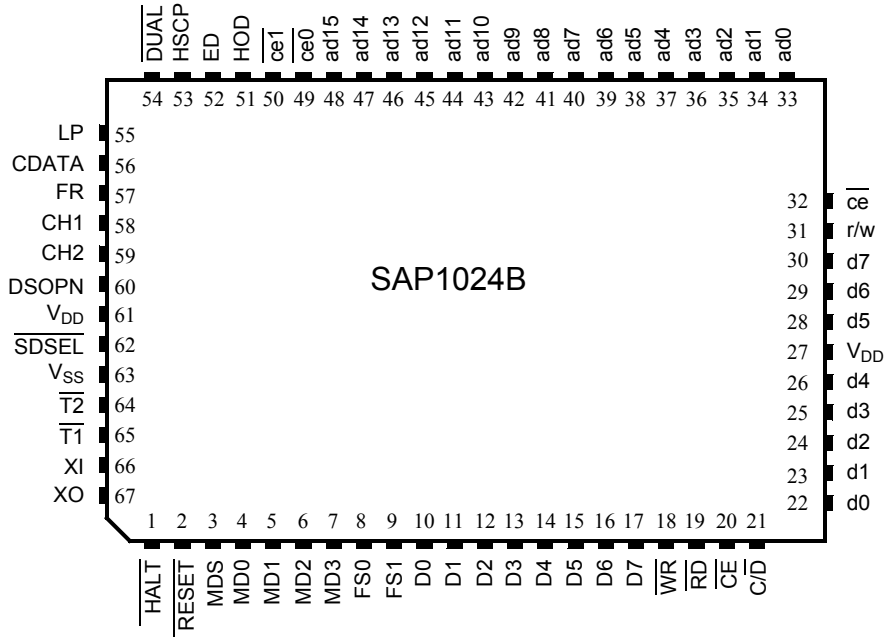


Fig.3 Pin assignment of the LQFP67 package.

5.2 Signal description

Table 2 Pin signal description.

To avoid a latch-up effect at power-on: $V_{SS} - 0.5\ V <$ voltage at any pin at any time $< V_{DD} + 0.5\ V$.

<table>
<tr><th>Pin number</th><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>$\overline{\text{HALT}}$</td><td>input</td><td>Oscillator halt input. This pin has an internal pull-up resistor.

When this pin is at logic LOW, the on-chip oscillator is halted. When this pin is at logic HIGH, the oscillator runs normally.</td></tr>
<tr><td>2.</td><td>$\overline{\text{RESET}}$</td><td>Input</td><td>Reset input. This pin has an internal pull-up resistor.

A low pulse to this input resets the SAP1024B. To completely reset the SAP1024B, this pin should be held low for at least 6 XI clock cycles.</td></tr>
<tr><td>3, 4, 5</td><td>MDS, MD0, MD1</td><td>input</td><td>Selection of line number (i.e., dot number in vertical direction).

These three pins, together with the $\overline{\text{DUAL}}$ pin, provide hardware selection of the number of display lines (i.e., number of characters in the vertical direction). Line number of a dual-screen display is twice that of a single-screen display.

The following table gives the available selection.

<table>
<tr><td></td><td colspan="8">1 screen</td><td colspan="8">2 screens</td></tr>
<tr><td>DUAL</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr>
<tr><td>MDS</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>MD1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>MD0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Lines</td><td>2</td><td>4</td><td>6</td><td>8</td><td>10</td><td>12</td><td>14</td><td>16</td><td>4</td><td>8</td><td>12</td><td>16</td><td>20</td><td>24</td><td>28</td><td>32</td></tr>
<tr><td>v-dots</td><td>16</td><td>32</td><td>48</td><td>64</td><td>80</td><td>96</td><td>112</td><td>128</td><td>32</td><td>64</td><td>96</td><td>128</td><td>160</td><td>192</td><td>224</td><td>256</td></tr>
</table>
Note: In the above table, “Lines” is the total number of characters in the vertical direction. v-dots is the total number of dots in vertical direction.</td></tr>
<tr><td>6, 7</td><td>MD2, MD3</td><td>input</td><td>Selection for column number.

These two pins are for hardware selection of maximum number of display columns. Display column number is the number of characters in horizontal direction.

The column numbers can be adjusted by programming the Text Area Register or Graphic Area Register. Please refer to Section 12.

<table>
<tr><td>MD2</td><td>H</td><td>L</td><td>H</td><td>L</td></tr>
<tr><td>MD3</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>Columns</td><td>32</td><td>40</td><td>64</td><td>80</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Pin number</th><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>8, 9</td><td>FS0, FS1</td><td>Input</td><td>Selection of character font type.
These two pins are for hardware selection of font types. In vertical direction, total number of dots of a font is fixed to 8. In horizontal direction, total number of dots of a font can be 5, 6, 7, or 8. However, fonts are always constructed in a font cell of 8x8 dots. Please refer to Section 21 Character Code Map for font pattern.
<table><tr><td>FS0</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>FS1</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>Font</td><td>5 x 8</td><td>6 x 8</td><td>7 x 8</td><td>8 x 8</td></tr></table></td></tr>
<tr><td>10 ~ 17</td><td>D0 ~ D7</td><td>I/O</td><td>Bi-directional data bus between the SAP1024B and the system microcontroller.
Data, commands, and status are written to or read from the SAP1024B via these data lines. This data bus has an internal latch for each bit.</td></tr>
<tr><td>18</td><td>$\overline{WR}$</td><td>Input</td><td>WRITE control bus between the SAP1024B and the system microcontroller.
When $\overline{WR}$ = Low, the system microcontroller can write data to the SAP1024B. The data is on the D0~D7 data bus.</td></tr>
<tr><td>19</td><td>$\overline{RD}$</td><td>Input</td><td>READ control bus between the SAP1024B and the system microcontroller.
When $\overline{RD}$ = Low, the system microcontroller can read data from the SAP1024B. The data is on the D0~D7 data bus.</td></tr>
<tr><td>20</td><td>$\overline{CE}$</td><td>Input</td><td>Chip Enable signal of the SAP1024B.
System microcontroller must put this signal to LOW to do READ/WRITE operation to the SAP1024B.</td></tr>
<tr><td>21</td><td>C/$\overline{D}$</td><td>Input</td><td>Selection of COMMAN / STATUS or DATA for data transfer between the SAP1024B and the host microcontroller.
<table><tr><td>$\overline{WR}$</td><td>L</td><td>L</td><td>H</td><td>H</td></tr><tr><td>$\overline{RD}$</td><td>H</td><td>H</td><td>L</td><td>L</td></tr><tr><td>C/$\overline{D}$</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>Operation</td><td>write command to the SAP1024B</td><td>write data to the SAP1024B</td><td>Read status from the SAP1024B</td><td>Read data from the SAP1024B</td></tr></table></td></tr>
<tr><td>22~26, 28~30</td><td>d0~d7</td><td>I/O</td><td>Data bus between the SAP1024B and Display Memory.</td></tr>
<tr><td>27</td><td>VDD</td><td></td><td>Power supply pin.</td></tr>
<tr><td>31</td><td>r/$\overline{w}$</td><td>Output</td><td>Control signal for the external Display Memory.
r/$\overline{w}$=H, read from Display memory. r/$\overline{w}$=L, write to Display memory.</td></tr>
<tr><td>32</td><td>ce</td><td>Output</td><td>Chip Enable signal for the external Display Memory.</td></tr>
<tr><td>33~48</td><td>ad0~ad15</td><td>Output</td><td>Address bus for the Display Memory.
ad15=L is for upper area of LCD (LCD1).
ad15=H is for lower area of LCD (LCD2).</td></tr>
</table>

Pin number	SYMBOL	I/O	DESCRIPTION
49	$\overline{ce0}$(LOD)	Output	This is a dual function pin. When $\overline{DUAL}$=H, this pin acts as $\overline{ce0}$ pin. $\overline{ce0}$ is the Chip Enable signal for the external Display Memory in the address range from 0000H to 07FFH. When $\overline{DUAL}$=L, this pin ascts as LOD pin. LOD is the serial data output for odd columns in the lower area of LCD.
50	$\overline{ce1}$ (LSCP)	Output	This is a dual function pin. When $\overline{DUAL}$=H, this pin acts as $\overline{ce1}$ pin. $\overline{ce1}$ is the Chip Enable signal for the external Display Memory in the address range from 0800H to 0FFFH. When $\overline{DUAL}$=L, this pin ascts as LSCP pin. LSCP is the shift clock pulse for column(segment) drivers for the lower area of LCD.
51	HOD	Output	Data output for odd columns in upper area of LCD.
52	ED	Output	If $\overline{SDSEL}$=H, this pin is the data output for even columns in both upper and lower areas of LCD. If $\overline{SDSEL}$= L, this pin is the data output for columns in both upper and lower areas of LCD.
53	HSCP	Output	Shift clock pulse for column(segment) driver of the upper area of LCD.
54	$\overline{DUAL}$	Input	$\overline{DUAL}$=H→ Select single-scan LCD. $\overline{DUAL}$=L→ Select dual-scan LCD.
55	LP	Output	Line Pulse, indicating the start of a horizontal scan line. This output is used as latch pulse of the column (segment) driver, for latching display data. This ouput is also used as shift clock pulse of row (common) driver.
56	CDATA	Output	Synchronous signal for row (common) driver.
57	FR	Output	Frame signal, indicating the start of a new display frame.
58	CH1	Output	Check signal.
59	CH2	Output	Check singal.
60	DSOPN	Output	Control pin for external DC/DC converter. DSPON goes to LOW, when either $\overline{HALT}$ or $\overline{RESET}$ is low.
61	VDD		Power supply.
62	$\overline{SDSEL}$	Input	H → sending data by odd/even separation. L → sending data by simple serial method.
63	VSS		Ground.
64	$\overline{T2}$	input	Test pin.
65	$\overline{T1}$	Input	Test pin.
66	XI	Input	Crystal oscillator input.
67	XO	Output	Crystal oscillator output.

5.3 Pin states after $\overline{\text{RESET}}$, $\overline{\text{HALT}}$

Table 3 Pin state after $\overline{\text{RESET}}$, $\overline{\text{HALT}}$

PIN	$\overline{\text{HALT}}$	$\overline{\text{RESET}}$
D0~D7	floating	floating
d0~d7	floating	floating
r/w	H	H
$\overline{\text{ce}}$	H(1)	H(1)
ad0~ad15	H(2)	H(2)
$\overline{\text{ce0}}$, $\overline{\text{ce1}}$	H(1)	H(1)
ED, HOD	Unchanged, that is, the state prior to the occurence of $\overline{\text{HALT}}$	Unchanged, that is, the state prior to the occurenc of $\overline{\text{RESET}}$
HSCP	L	L
LP	L	L
CDATA	H	H
FR	H	H
DSPON	L	L
XO	H	OSC clock
CH1	L	Test signal
CH2	L	Test signal

Note

1. In Attribute mode, High or Low according to state of graphic pointer.
2. In Attribute mode, data of graphic pointer.

6 THE RELATIONSHIP BETWEEN NUMBER OF ROW/COLUMN AND OSCILLATION CLOCK

6.1 Caculation of oscillator frequency

The calculation of oscillator frequency is described below:

f_{OSC}: Frequency of oscillation

f_{SCP}: Frequency of shift clock

f_R: Frequency of Frame

M: Number of characters on one horizontal row. As the maximun number of dots of each scan line of a character has 8 horizontal dots, total number of dots in a horizontal scan line is 8M.

N: Number of horizontal rows. As the maximum number of each character has 8 dots in vertical direction, the total liner of scan lines is 8N and the display duty cycle is 1/8N.

Total number of dots per frame= 8M x 8N

Time needed to display a frame= $1/f_R$ = [total number of dots per frame] x [period of a dot clock] = (8M x 8N) x ($1/f_{SCP}$).

$$\frac{8M}{f_{SCP}} \times 8N = \frac{1}{f_R}$$

As fosc= 2 x f_{SCP}, the above equation can be re-written as **fosc= f_R x 2 x 8M x 8N**, where f_R is usually 60Hz.

The following table gives the oscillator frequency for various combination of M and N, with f_R = 60 Hz.

Table 4 Oscillator frequency

N \ M	32	40	64	80	DUTY
2	0.492	0.614	0.983	1.229	1/16
	0.983	1.229	1.966	2.458	
4	0.983	1.229	1.966	2.458	1/32
	1.966	2.458	3.932	4.915	
6	1.475	1.843	2.949	3.686	1/48
	2.949	3.686	5.898	7.372	
8	1.966	2.458	3.932	4.915	1/64
	3.932	4.915	7.864	9.830	
10	2.458	3.072	4.915	6.144	1/80
	4.915	6.144	9.830	12.288	
12	2.949	3.686	5.898	7.373	1/96
	5.898	7.373	11.776	14.746	
14	3.440	4.300	6.881	8.602	1/112
	6.881	8.601	13.763	17.203	
16	3.932	4.915	7.864	9.830	1/128
	7.864	9.830	15.729	19.660	

Note:

1. The upper cell with yellow shading is for single scan.
2. The lower cell without yellow shading is for dual scan.
3. The frame frequency (f_R) is 60 Hz.

6.2 External clock source

External clock source can be used to replace the on-chip oscillator. When using external clock source, use the XI pin as clock input and leave XO pin unconnected.

6.3 The on-chip oscillator

The value of the external capacitors C1 and C2 for crystal resonator should be in the range from 20 pF to 30 pF. The value of C1 and C2 for ceramic resonator should be in the range from 30 pF to 100 pF.

On PCB layout, C1 and C2 should be placed as close to the chip as possible, such that the side effect of parasitic inductance, capacitance and resistance can be minimized.

The value of the on-chip feedback resistor R_f is 900 kΩ (typ.)

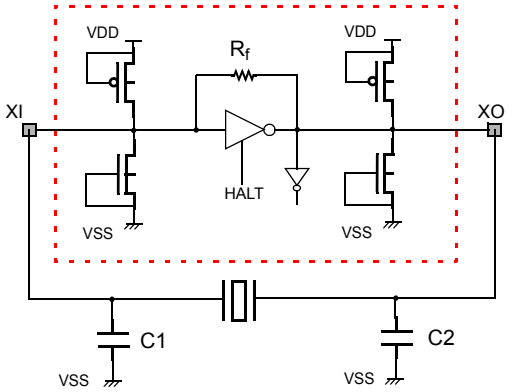


Fig.4 Oscillator application circuit.

7 EXTERNAL DISPLAY MEMORY

The external Display Memory must be static RAM. It is for storing text data, graphic data, external user-defined Character Generator (CG) fonts, and attribute data for text display. Memory for attribute data of text display can overlap with or reside in graphic area.

In single-scan application, text data, graphic data, attribute data, and external user-defined CG data can be freely allocated to the whole memory space of the Display Memory (maximum 64K).

In dual-scan application, the memory area for LCD1 is allocated to the space from 0000H to 7FFFH (32K bytes, maximum) and that for LCD2 is allocated to the space from 8000H to FFFFH (32K bytes, maximum). Text data, graphic data, and CG data can be freely allocated to any area of the memory space in LCD1. In LCD2, the corresponding memory regions, as that for the LCD1, must be allocated to the text area, graphic area, and the Character Generator RAM, except address bit ad15. Address bit ad15 can be used in the address decoding circuit to distinguish LCD1 from LCD2. ad15=L selects LCD1 and ad15=H selects LCD2.

Two signals, $\overline{ce0}$ and $\overline{ce1}$, can be used to help decoding memory blocks with 4K boundary. $\overline{ce0}$ can be used to decode memory block in the range from 0000H to 07FFH. $\overline{ce1}$ can be used to decode memory blocks in the range from 0800H to 0FFFH.

An example of memory space allocation is given below:

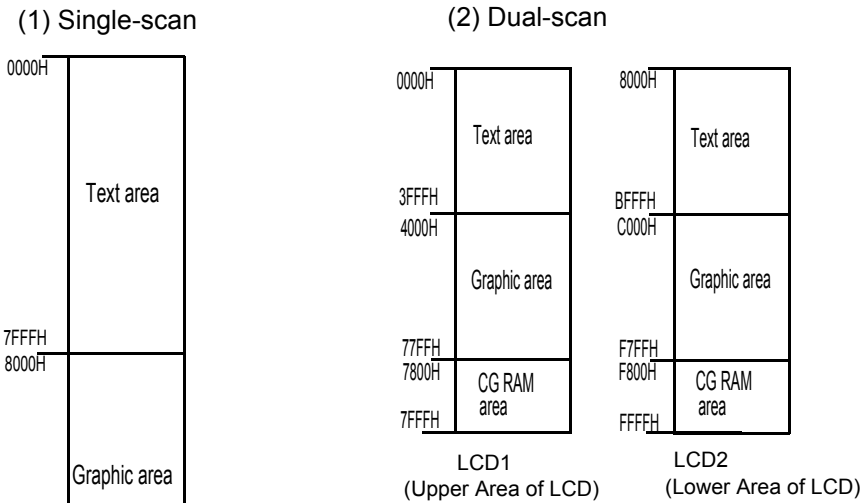


Fig.5 Display Memory allocation

8 MICROCONTROLLER INTERFACE

8.1 READ/WRITE operation to the SAP1024B

A microcontroller can write command to the SAP1024B or read status from it. A microcontroller can do Read/Write operation to the Display Memory, via SAP1024B.

Data or commands are put on the data bus D0~D7. Inside the SAP1024B, there is an latch for each bit of D0~D7.

The operations between the host microcontroller and the SAP1024B are: Write Data, Read Data, Write Command, and Read Status. It is the host microcontroller's responsibility to put proper control signals and timing on the contol bus for these Read/Write operation.

Table 5 gives control signal setting.

Table 5 Read/Write operation between the host microcontroller and the SAP1024B

Operation	Description
Write Data to the Display Memory	1. The data to be written should be put on D0~D7. 2. C/$\overline{D}$ should be set to low. 3. $\overline{WR}$ should be set to low. 4. $\overline{RD}$ should be set to high. 5. $\overline{CE}$ should be set to low.
Read Data from the Display Memory	1. C/$\overline{D}$ should be set to low. 2. $\overline{WR}$ should be set to high. 3. $\overline{RD}$ should be set to low. 4. $\overline{CE}$ should be set to low. 5. The data appears on D0~D7.
Write Command to the SAP1024B	1. The command to be written should be put on D0~D7. 2. C/$\overline{D}$ should be set to high. 3. $\overline{WR}$ should be set to low. 4. $\overline{RD}$ should be set to high. 5. $\overline{CE}$ should be set to low.
Read Status from the SAP1024B	1. C/$\overline{D}$ should be set to high. 2. $\overline{WR}$ should be set to high. 3. $\overline{RD}$ should be set to low. 4. $\overline{CE}$ should be set to low. 5. The status of the SAP1024B appears on D0~D7.

8.2 Hardware interface connection

Examples of hardware interface connection with host microcontroller are given in Fig 30 and Fig 31.

8.3 Interface timing

For detailed interface timing, please refer to Fig.26.

9 STATUS CHECK

The system microcontroller must perform a status check before writing data to or reading data from the SAP1024B. The purpose of status check is to make sure that the SAP1024B has finished previous command or operation and is ready to accept new command or data.

9.1 Status Register

To read the status of the SAP1024B, the host microcontroller must set the control bus to the proper states, as described in Table 5. The content of Status Register appears on D0~D7.

The format of the Status Register is given in table 6.

Table 6 Status Register format

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0

Table 7 Description of Status Register bits

BIT	SYMBOL	FUNCTION
D0	STA0	Command flag. STA0=0 indicates that the SAP1024B is busy and can not accept new command. STA0=1 indicates that the SAP1024B is ready for accepting new command.
D1	STA1	Data Read/Write flag. STA0=0 indicates that the SAP1024B is busy and can not accept data read/write request. STA0=1 indicates that the SAP1024B is ready for accepting data/reqd write request.
D2	STA2	Auto Data Read flag. STA2=0 indicates that the SAP1024B is busy and can not accept Auto Data Read request. STA2=1 indicates that the SAP1024B is ready for accepting Auto Data Read request.
D3	STA3	Auto Data Write flag. STA3=0 indicates that the SAP1024B is busy and can not accept Auto Data Write request. STA3=1 indicates that the SAP1024B is ready for accepting Auto Data Write request.
D4	STA4	Reserved.

BIT	SYMBOL	FUNCTION
D5	STA5	Check controller operation capability. 0= Disabled, 1= Enabled.
D6	STA6	Error flag. This command is used for commands SCREEN PEAK or SCREEN COPY. STA6=0 indicates that Address Pointer is valid and that there is no error. STA6=1 indicates that Address Pointer is out of Graphic RAM area.
D7	STA7	Blink flag. Check the blink status. 0=blinking area of display off, 1= blinking area of display on.

Note:

1. STA0 and STA1 must be checked at the same time. If a hardware interrupt occurs to the microcontorller during the check, the status on the data bus D0~D7 may not be correct.
2. For most modes, STA0 and STA1 are used as status check.
3. In AUTO READ/WRITE mode, STA2 and STA3 indicates the real status of the SAP1024B. STA0 and STA1 do not indicates the real status of the SAP1024B in AUTO READ/WRITE mode.

9.2 Status check flowchart

Fig. 6 gives flow charts for writing status check subroutines.

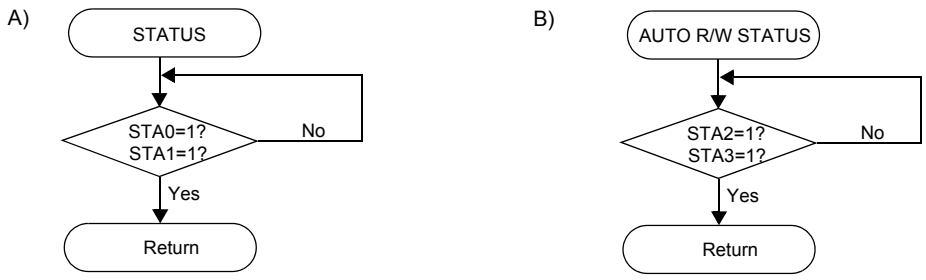


Fig.6 Status check flowchart.

Note the following:

- Status check must be performed prior to issuing a MSB=0 command. If a status check is not performed, there is danger that the SAP1024B may not work properly, even after a delayed period of time.
- A hardware interrupt to the microcontroller may occur during the address calculation period (at the end of each line). If a MSB=0 command is sent to the SAP1024B during this period of time, it enters into Wait status.
- If a command is issued during Wait status, there is danger that command or data may not be received by the SAP1024B.

10 COMMANDS AND REGISTERS

10.1 Commands

The SAP1024B has three types of command: one-byte command, two-byte command, and three-byte commands. A one-byte comand has only command code. A two-byte command has command code and one operand (data). A three-byte command has command code and two operands.

Table 8 lists all the commands.

Table 8 Commands and Registers.

COMMAND	CODE	OPERAND 1	OPERAND 2	FUNCTION
Register Setting	0010 0001	X address	Y address	Set cursor pointer
	0010 0010	Data	00H	Set offset register
	0010 0100	Low address	High address	Set address pointer
Set Control Word	0100 0000	Low address	High address	Set text home address
	0100 0001	Columns	00H	Set text area
	0100 0010	Low address	High address	Set graphic home address
	0100 0011	Columns	00H	Set graphic area
Mode Set	1000 x000			OR mode
	1000 x001			EXOR mode
	1000 x011			AND mode
	1000 x100			Text Attribute mode
	1000 0xxx			Internal CG ROM mode
	1000 1xxx			External CG RAM mode
Display mode	1001 0000			Display OFF.
	1001 xx10			Cursor ON, blink OFF.
	1001 xx11			Cursor ON, blink ON.
	1001 01xx			Text ON, graphic OFF.
	1001 10xx			Text OFF, graphic ON.
	1001 11xx			Text ON, graphic ON.
Cursor Pattern Select	1010 0000			Selec one-line cursor.
	1010 0001			Select two-line cursor.
	1010 0010			Select three-line cursor.
	1010 0011			Select four-line cursor.
	1010 0100			Select five-line cursor.
	1010 0101			Select six-line cursor.
	1010 0110			Selec seven-line cursor.
	1010 0111			Select eight-line cursor.
Data Auto Read/Write	1011 0000			Select Data Auto Write
	1011 0001			Select Data Auto Read
	1011 0010			Reset Auto Read/Write

COMMAND	CODE	OPERAND 1	OPERAND 2	FUNCTION
Data READ / WRITE	1100 0000	Data		Data Write and increment Address Pointer
	1100 0001			Data Read and increment Address Pointer
	1100 0010	Data		Data Write and decrement Address Pointer.
	1100 0011			Data Read and decrement Address Pointer
	1100 0100	Data		Data Write and Keep Address Pointer
	1100 0101			Data Read and Keep Address Pointer
Screen Peek	1110 0000			Screen peek
Screen Copy	1110 1000			Screen copy
Bit Set/Reset	1111 0xxxx			Bit Reset
	1111 1xxxx			Bit Set
	1111 x000			Bit 0
	1111 x001			Bit 1
	1111 x010			Bit 2
	1111 x011			Bit 3
	1111 x100			Bit 4
	1111 x101			Bit 5
	1111 x110			Bit 6
	1111 x111			Bit 7

10.2 Sending a command and its operands.

When a command is sent, its operands should be sent out first. For a two-operand command, operand 2 should be sent out first. The command code itself is the last to be sent out.

The flow chart for sending a command is given below.

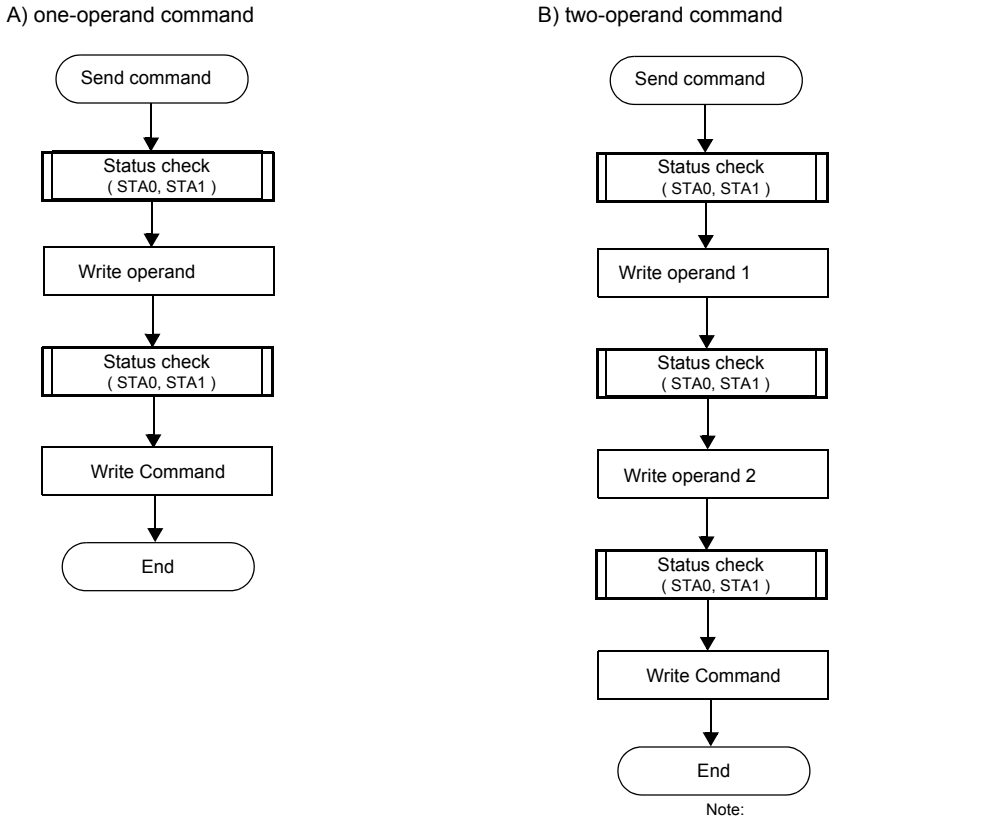


Fig.7 Flowchart for sending commands.

11 PROGRAMMING REGISTERS

Each of the three registers, Cursor Pointer register, Offset Register, and Address Pointer Register, needs to be programmed with two operands, in addition to the command code.

Table 9 Setting registers

Code	Hex	Function	D1	D2
0010 0001	21H	programming the Cursor Pointer Register.	X address	Y address
0010 0010	22H	programming the Offset Register	Data(offset address for accessing the external Font RAM)	00H
0010 0100	24H	programming the Address Pointer Register	Low address	High address

11.1 Programming the Cursor Pointer Register

The position of cursor is software-programmable by programming the Cursor Pointer Register. The Cursor Pointer Register specifies X address and Y address of the cursor. The position of the cursor can be changed only by changing the content of the Cursor Pointer Register.

For single-scan LCD, the range of X address is from 00H to 4FH, and the range of Y address is from 00H to 1FH.

For dual-scan LCD, the range of X address is: 00H to 4FH. The Y address range of the upper screen is: 00H to 0FH. The address range of the lower screen is: 10H to 1FH.

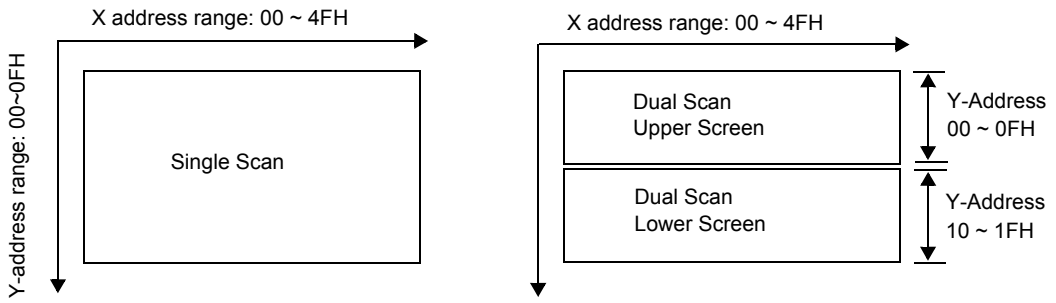


Fig.8 Address range of Cursor Pointer Register.

11.2 Programming the Offset Register

11.2.1 THE OFFSET REGISTER

The Offset Register is a three-byte command. Its first operand is a data byte and its second operand is fixed with 00H. The lower five bits of its first operand is used as ad15, ad14, ad13, ad12, and ad11 of the ad15~ad0 address bus between the SAP1024B and the external Display Memory. This address is generated for programming external Character Generator Font RAM.

The ad15~ad0 address bus for programming external Character Generator Font RAM is cascaded from Leading 5 bits of the Offset Register, Font Character Code, and Scan line, as illustrated below.

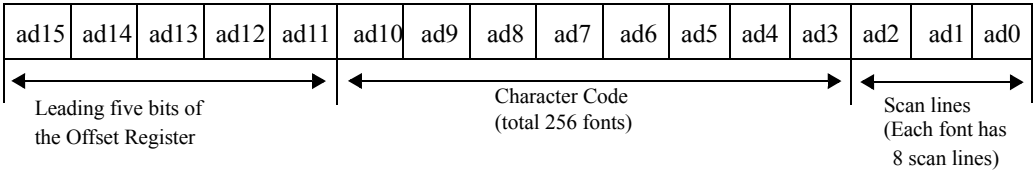


Fig.9 Character Font RAM address generation

The upper five bits (ad15~ad11) points at the starting address in external memory of the Character Generator RAM area. The next 8 bits (ad10~ad3) points at the starting address for each Character Code (font). Totally, 256 fonts can be defined if there is enough external Display Memory. The three least significant bits (ad2 ad0) points at each of the eight rows of each font. Each row of a font has 8 dots (pixel).

In Internal CG ROM mode, each of character codes from 00H to 7FH accesses a character or graphic font from on-chip Font ROM and each of character codes from 80H to FFH accesses a user-defined character or graphic font from external Font RAM. In External CG RAM mode, each of the 256 codes from 00H to FFH accesses a user-defined character or graphic font from external Font RAM.

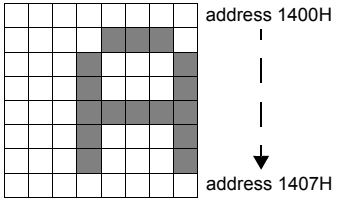
11.2.2 Example of font ROM address and Offset Register

Assume that the Offset Register's first operand is programmed with a value of 02H (0000 0010B). So the lower five bits= 0 0 0 1 0 = ad15 ad14 ad13 ad12 ad11.

Assume that the Character Code is 80H= 1000 0000B = ad10 ad9 ad8 ad7 ad6 ad5 ad4 ad3.

The initial value of ad2, ad1, ad0 = 000.

So, the **starting address** of the font for Character Code 80H= ad15~ad0= 00010 1000 0000 000=1400H.



Address	Data
1400H	00H
1401H	0EH
1402H	11H
1403H	11H
1404H	1FH
1405H	11H
1406H	11H
1407H	00H

Note: blank pixel=0, black pixel=1.

Fig.10 Font Pattern in Character Generator RAM for Character Code 80H

11.3 Progamming the Address Pointer Register

The Address Pointer Register points at a byte address of the Display Memory where a data Read/Write is to be performed.

The flow chart for progarmming Address Pointer Register is given in Figure 11.

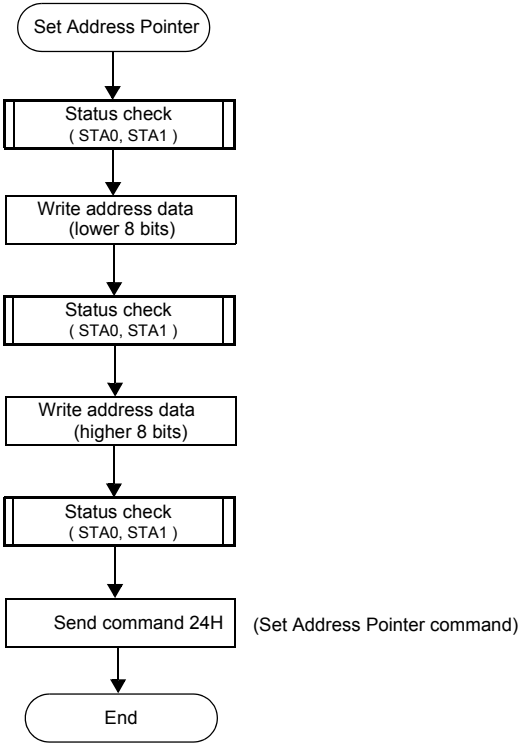


Fig.11 The flowchart for programming Address Pointer Register

12 SET CONTROL WORD

Four registers, Text Home Address Register, Text Area Register, Graphic Home Address Register, and Graphic Area Register, need to be programmed to define text display and graphic display.

Table 10 Set control word

CODE	HEX	FUNCTION	D1	D2
0100 0000	40H	Set text home address	Low address	High address
0100 0001	41H	Set text area	Columns	00H
0100 0010	42H	Set graphic home address	Low address	High address
0100 0011	43H	Set graphic area.	Columns	00H

12.1 the Text Home Address Register

The Text Home Address Register is a 16-bit register and it points at the starting byte address of a block of memory space in the Display Memory, where data for text display are stored. The corresponding character of the first byte of the memory block is displayed at the left-most and top-most position on the LCD screen.

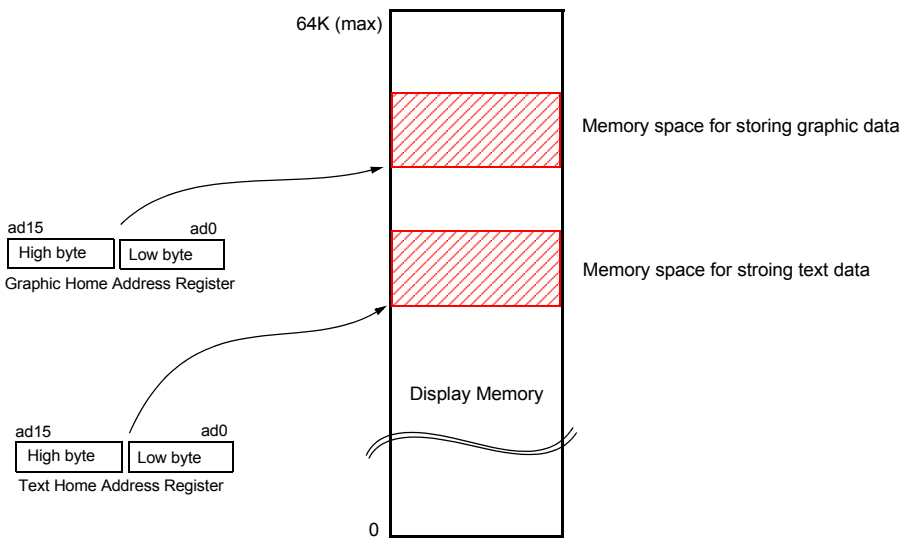


Fig.12 Text Home Address and Graphic Home Address

12.2 The relation between Display Memory and display position on LCD screen

As previously described, the first character on the LCD screen is the top-most and the left-most character and the memory address of this first character is pointed at by the Text Home Adrress Register. The characters on each line are displayed from left to right until the total number of displayed characters is equal to the value of Text Area Register.

The following figure illustrates the relation between Display Memory address and the display position on the LCD screen. Note that actual display on the LCD screen is adjusted by the Text Area Register (TA).

TH= Content of Text Home Address Register.

TA= Content of Text Area Register.

CL= Column number, selected by setting the MD2 pin and the MD3 pin.

n= line number, selected by setting pins $\overline{\text{DUAL}}$, MDS, MD0, MD1.

TH+0	TH+1	- - - - - - - - - - - - - - - - -	TH+(CL-2)	TH+(CL-1)
TH+TA+0	TH+TA+1	- - - - - - - - - - - - - - - - -	TH+TA+(CL-2)	TH+TA+(CL-1)
(TH+TA)+TA+0	(TH+TA)+TA+1	- - - - - - - - - - - - - - - - -	(TH+TA)+TA+(CL-2)	(TH+TA)+TA+(CL-1)
(TH+2TA)+TA+0	(TH+2TA)+TA+1	- - - - - - - - - - - - - - - - -	(TH+2TA)+TA+(CL-2)	(TH+2TA)+TA+(CL-1)
		- - - - - - - - - - - - - - - - -		
TH+(n-1)TA+0	TH+(n-1)TA+1	- - - - - - - - - - - - - - - - -	TH+(n-1)TA+(CL-2)	TH+(n-1)TA+(CL-1)

Example:

Text Home Address Register(TH)= 0000H

Text Area Register(TA)= 0020H

Column number(CL)= 20H (MD2=H, MD3=H)

Line number(n)= 4, ($\overline{\text{DUAL}}$=H, MDS=L, MD0=L, MD1=H)

0000	0001	- - - - - - - - - - - - - - - - -	001E	001F
0020	0021	- - - - - - - - - - - - - - - - -	003E	003F
0040	0041	- - - - - - - - - - - - - - - - -	005E	005F
0060	0061	- - - - - - - - - - - - - - - - -	007E	007F

Fig.13 The relation between text display memory address and display position on the LCD screen

12.3 The Text Area Register

The number of characters displayed on a horizontal line, called columns, is decided by both hardware setting and software setting. The hardware setting of the MD2 pin and the MD3 pin selects hardware column number. The value of the Text Area Register selects the actual number of columns displayed on the LCD screen. For example, if hardware selection of display column number is 32 columns (MD2=1, MD3=1) and the Text Area Register is programmed with 14H (20 columns), then only 20 columns (characters) will be displayed on each horizontal line.

Hardware setting of columns per line only decides the “maximum” number of columns that can possibly be displayed on the LCD screen. Software setting of columns per line decides the actual display column number.

The following figure illustrates the hardware setting and software setting of columns.

Physical LCD size= 20 columns, 4 lines= 80 characters per frame.
Text Home Address Register= 0000H.
Text Area Register= 0014H= 20(decimal) (software setting of columns per line).
MD2=H, MD3=H --> 32 columns (hardware setting of columns per line.
DUAL=H, MDS=L, MD0=L, MD1=H --> 4 lines (hardware setting of line number)

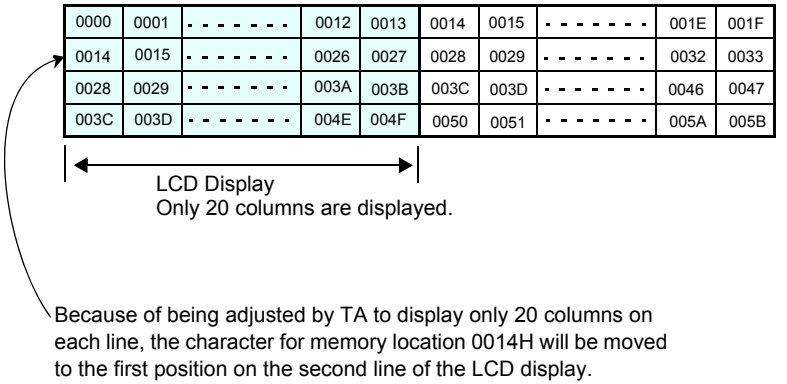


Fig.14 Text Area Register

12.4 The Graphic Home Address Register

The Graphic Home Address Register, like the Text Home Address Register, is a 16-bit register and it points at the starting byte address of a block of memory space in the Display Memory, where data for text display are stored. Please refer to Fig. 12.

The corresponding graphic pattern of the first byte of the memory block is displayed at the left-most and top-most position on the LCD screen. The relation between display position and graphic display memory is illustrated below.

GH= Content of Graphic Home Address Register.

GA= Content of Graphic Area Register.

CL= Column number, selected by setting the MD2 pin and the MD3 pin.

n= line number, selected by setting pins $\overline{\text{DUAL}}$, MDS, MD0, MD1.

GH+0	GH+1	- - - - - - - - - - - - - - - - -	GH+(CL-2)	GH+(CL-1)
GH+GA+0	GH+GA+1	- - - - - - - - - - - - - - - - -	GH+GA+(CL-2)	GH+GA+(CL-1)
(GH+GA)+GA+0	(GH+GA)+GA+1	- - - - - - - - - - - - - - - - -	(GH+GA)+GA+(CL-2)	(GH+GA)+GA+(CL-1)
(GH+2GA)+GA+0	(GH+2GA)+GA+1	- - - - - - - - - - - - - - - - -	(GH+2GA)+GA+(CL-2)	(GH+2GA)+GA+(CL-1)
		- - - - - - - - - - - - - - - - -		
GH+(n-1)GA+0	GH+(n-1)GA+1	- - - - - - - - - - - - - - - - -	GH+(n-1)GA+(CL-2)	GH+(n-1)GA+(CL-1)

Example:

Content of Graphic Home Address Register=GH= 0000H

Content of Graphic Area Register=GA= 0020H

Column number= CL= 32 columns (selected by setting pins MD2=H and MD3=H)

Line number=n= 2=16 horizonal scan lines, (selected by setting pins $\overline{\text{DUAL}}$=H, MDS=L, MD0=H, MD1=H)

32 columns

16 scan lines

1	0000H	0001H	- - - - - - - - - - - - - - - - -	001EH	001FH
2	0020H	0021H	- - - - - - - - - - - - - - - - -	003EH	003FH
3	0040H	0041H	- - - - - - - - - - - - - - - - -	005EH	005FH
4	0060H	0061H	- - - - - - - - - - - - - - - - -	007EH	007FH
5	0080H	0081H	- - - - - - - - - - - - - - - - -	009EH	009FH
6	00A0H	00A1H	- - - - - - - - - - - - - - - - -	00BEH	00BFH
7	00C0H	00C1H	- - - - - - - - - - - - - - - - -	00DEH	00DFH
8	00E0H	00E1H	- - - - - - - - - - - - - - - - -	00FEH	00FFH
9	0100H	0101H	- - - - - - - - - - - - - - - - -	011EH	011FH
10	0120H	0121H	- - - - - - - - - - - - - - - - -	013EH	013FH
11	0140H	0141H	- - - - - - - - - - - - - - - - -	015EH	015FH
12	0160H	0161H	- - - - - - - - - - - - - - - - -	017EH	017FH
13	0180H	0181H	- - - - - - - - - - - - - - - - -	019EH	019FH
14	01A0H	01A1H	- - - - - - - - - - - - - - - - -	01BEH	01BFH
15	01C0H	01C1H	- - - - - - - - - - - - - - - - -	01DEH	01DFH
16	01E0H	01E1H	- - - - - - - - - - - - - - - - -	01FEH	01FFH

Fig.15 The relation between graphic display memory address and display position on the LCD screen

12.5 The Graphic Area Register

The number of columns on a horizontal line is decided by both hardware setting and software setting. The hardware setting of the MD2 pin and the MD3 pin selects hardware column number. The value of the Graphic Area Register selects the actual number of columns displayed on the LCD screen. For example, if hardware selection of display column number is 32 columns (MD2=1, MD3=1) and the Graphic Area Register is programmed with 14H (20 columns), then only 20 columns will be displayed on each horizontal line. In Graphic Display mode, the width of a column is 8 dots in horizontal direction.

Hardware setting of columns per line only decides the “maximum” number of columns that can possibly be displayed on the LCD screen. Software setting of columns per line decides the actual display column number.

The following figure illustrates the hardware setting and software setting of columns.

Physical LCD size= 20 columns, 2 lines.
Grapic Home Address Register= 0000H.
Graphic Area Register= 0014H= 20(decimal) (software setting of columns per line).
MD2=H, MD3=H --> 32 columns (hardware setting of columns per line.
DUAL=H, MDS=L, MD0=H, MD1=H --> 2 lines (hardware setting of line number)

0000	0001	- - - - - - -	0012	0013	0014	0015	- - - - - - -	001E	001F
0014	0015	- - - - - - -	0026	0027	0028	0029	- - - - - - -	0032	0033
0028	0029	- - - - - - -	003A	003B	003C	003D	- - - - - - -	0046	0047
003C	003D	- - - - - - -	004E	004F	0050	0051	- - - - - - -	005A	005B
0050	0051	- - - - - - -	0062	0063	0064	0065	- - - - - - -	006E	006F
0064	0065	- - - - - - -	0076	0077	0078	0079	- - - - - - -	0082	0083
0078	0079	- - - - - - -	008A	008B	008C	008D	- - - - - - -	0096	0097
008C	008D	- - - - - - -	009E	009F	00A0	00A1	- - - - - - -	00AA	00AB
00A0	00A1	- - - - - - -	00B2	00B3	00B4	00B5	- - - - - - -	00BE	00BF
00B4	00B5	- - - - - - -	00C6	00C7	00C8	00C9	- - - - - - -	00D2	00D3
00C8	00C9	- - - - - - -	00DA	00DB	00DC	00DD	- - - - - - -	00E6	00E7
00DC	00DD	- - - - - - -	00EE	00EF	00F0	00F1	- - - - - - -	00FA	00FB
00F0	00F1	- - - - - - -	0102	0103	00104	0105	- - - - - - -	011E	011F
0104	0105	- - - - - - -	0126	0127	0128	0129	- - - - - - -	0132	0133
0128	0129	- - - - - - -	013A	013B	013C	013D	- - - - - - -	0146	0147
013C	013D	- - - - - - -	014E	014F	0150	0151	- - - - - - -	015A	015B

LCD Display
Only 20 columns are displayed.

Because of being adjusted by GA to display only 20 columns on each line, the 8 pixels of memory location 0014H will be moved to the first position on the second line of the LCD display.

Fig.16 Graphic Area Register

13 MODE SET

13.1 commands

The display mode is defined by these commands. Display mode does not change until the next command is issued. These commands are listed in Table 11.

Table 11 Display Mode set

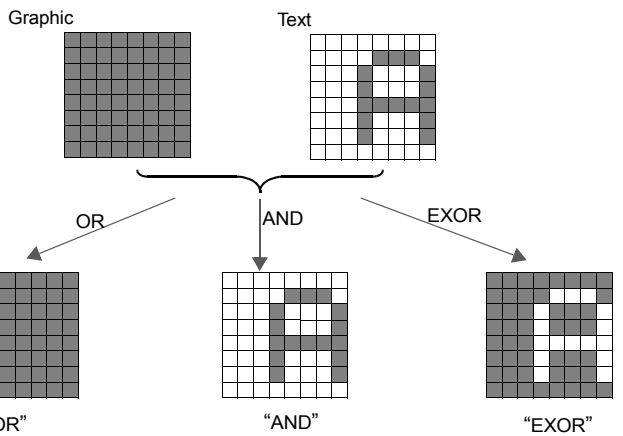
CODE	OPERATION
1000 x000	OR mode.
1000 x001	EXOR mode.
1000 x011	AND mode.
1000 x100	Text Attribute mode.
1000 0xxx	Internal Character Generator mode.
1000 1xxx	External Character Generator mode.

OR mode, EXOR mode, and AND mode display, respectively, the logical operation of text display and graphic display. Text Attribute mode is for setting the display attribute, such as reverse display and blinking, of text. In Text Attribute mode, graphic data can not be displayed, because the memory space for graphic data is used to store attribute of text.

In Internal Character Generator mode, Character Codes 00~7FH (128 fonts) access on-chip Font ROM and Character Codes 80~FFH (128 fonts) access external user-defined Character Generator RAM (Font RAM).

In External Character Generator mode, all Character Codes (00~FFH) access external user-defined Character Generator RAM (Font RAM).

13.2 Example



Note:

Since the attribute function of text data is stored in the corresponding area of the graphic RAM area, the attribute function is only available to text display.

Fig.17 Display Modes

13.3 Attribute of text data

An attribute can be defined for each text data (character). The attributes are: reverse display, blinking, and Inhibit. Attribute data for text characters are stored in a block of memory space in the Display Memory, called Attribute RAM, which may occupy the Graphic Display RAM or in another block of Display Memory.

To use attribute function, it is first necessary to re-assign the Graphic Home Address Register to point at the first byte of the Attribute RAM area. Second, it is necessary to write attribute data for each character. The attribute data for the first character in Text RAM should be written to the first byte of the Attribute RAM and the attribute data of the Nth character should be written to the Nth byte in the Attribute RAM.

Although, in Attribute mode, graphic display is automatically disabled, graphic display still needs to be turned on to enable attribute function, by executing Display Mode command Text ON, Graphic ON (code 1001 11xx). Please refer to Section 14.

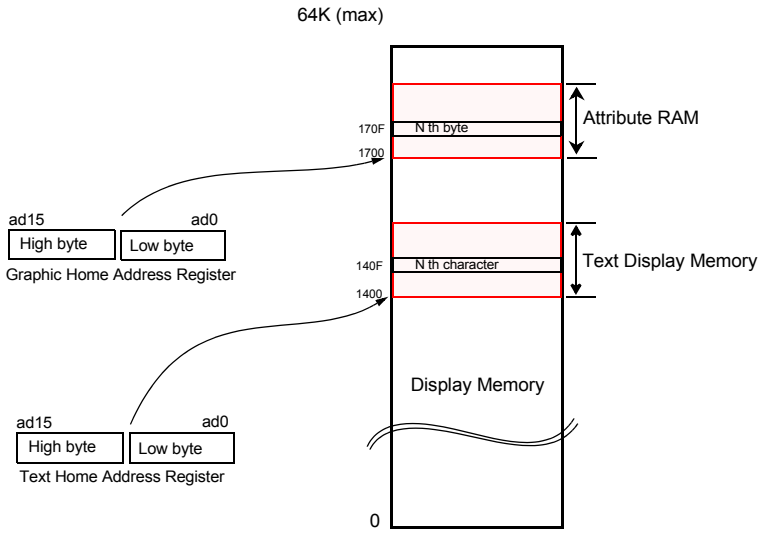
The bit definition for the attribute RAM byte (1 byte) of a text data (character) is defined in Table 12 and Table 13.

Table 12 Attribute RAM byte

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0(LSB)
don't care	don't care	don't care	don't care	d3	d2	d1	d0

Table 13 Description of Attribute RAM byte

d3 d2 d1 d0	attribute
0000	Normal display.
0101	Reverse display
0011	Inhibit display
1000	Blink of normal display
1101	Blink of reverse display
1011	Blink of inhibit display



Note:

1. Graphic Home Address should be re-assigned to point at the first byte of Attribute RAM.
2. The attribute of the Nth character is stored at the Nth byte of Attribute RAM.
3. Graphic display is automatically disabled, but Graphic display still needs to be turned on.
3. Example:

- Text Home Address Register= 1400H.
- Graphic Home Address Register= 1700H.
- If the attribute of the 16th character of the displayed text is to be Reverse Blink, then the value 0DH should be written to memory byte at address 170FH.

Fig.18 Attribute of characters and Attribute RAM

14 DISPLAY MODE COMMANDS

The Display Mode command is used to turn on or turn off text display, graphic display, or cursor blink. It can also be used to turn off the whole display.

The Display Mode command format is given below. Note that the leading 4 bits of the command are always 1001.

Table 14 Bit allocation of Display Mode command

Bit allocation	Description	Remark
Bit 7, 6, 5, 4	1001	
Bit 3	Turn of/off graphic display. d3=1 → graphic display on; d3=0 → graphic display off.	Graphic ON/OFF flag.
Bit 2	Turn of/off text display. d2=1 → text display on. d2=0 → text display off.	Text ON/OFF flag.
Bit 1	Turn of/off cursor. d1=1 → cursor on. d1=0 → cursor off.	Cursor ON/OFF flag.
Bit 0	Turn of/off cursor blink. d1=1 → cursor blink on. d1=0 → cursor blink off.	Cursor blink flag.

Table 15 Display Mode command codes

code	Function
1001 0000	Display OFF.
1001 xx10	Cursor ON, blink OFF.
1001 xx11	Cursor ON, blink ON.
1001 01xx	Text ON, graphic OFF.
1001 10xx	Text OFF, graphic ON.
1001 11xx	Text ON, graphic ON.

Note:

1. Both text display and graphic display must be turned ON for displaying combination of text and graphics.
2. Both text display and graphic display must be turned ON for enabling attribute function of tex.
3. For example, the comamand for graphic and text display on, with cursor, no blink= 1001 1110= 9E hex.

15 CURSOR PATTERN SELECT

A cursor pattern can have horizontal raster scan lines in the range from 1 to 8. The Cursor Display command must be turned on to display cursor. The location of cursor is defined by Cursor Point register.

The following table gives code for commands of selecting horizontal lines of cursor pattern.

Table 16 Cursor pattern selection

Code	horizontal lines of cursor
1010 0000	One scan line.
1010 0001	Two scan lines.
1010 0010	Three scan lines.
1010 0011	Four scan lines.
1010 0100	Five scan lines.
1010 0101	Six scan lines.
1010 0110	Seven scan lines.
1010 0111	Eight scan lines.

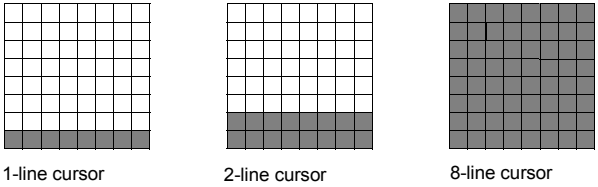


Fig.19 Example of cursor patterns

16 DATA AUTO READ/WRITE COMMANDS

Data Auto Read, Data Auto Write, and Auto Mode Reset commands are single-byte commands. Auto Read/Write commands are useful for transferring a block of data to or from the Display Memory. After sending a Data Auto Read or Data Auto Write command, it is not necessary to send Data Read or Data Write command for each data byte transfer to or from the Display Memory.

Address Pointer Register should be programmed to point at the initial byte address in the Display Memory. The Address Pointer Register will be automatically incremented by one after each Data Read/Data Write. After finishing the data transfer, a Auto Mode Reset command should be issued to terminate Auto Read/Write mode.

Note that no commands will be accepted during Auto Read/Write mode.

Table 17 Data Auto Read/Write commands.

Code(Binary)	Code(Hex)	Description
1011 0000	B0	Set Data Auto Write mode.
1011 0001	B1	Set Data Auto Read mode.
1011 0010	B2	Terminate Auto Read/Write mode.

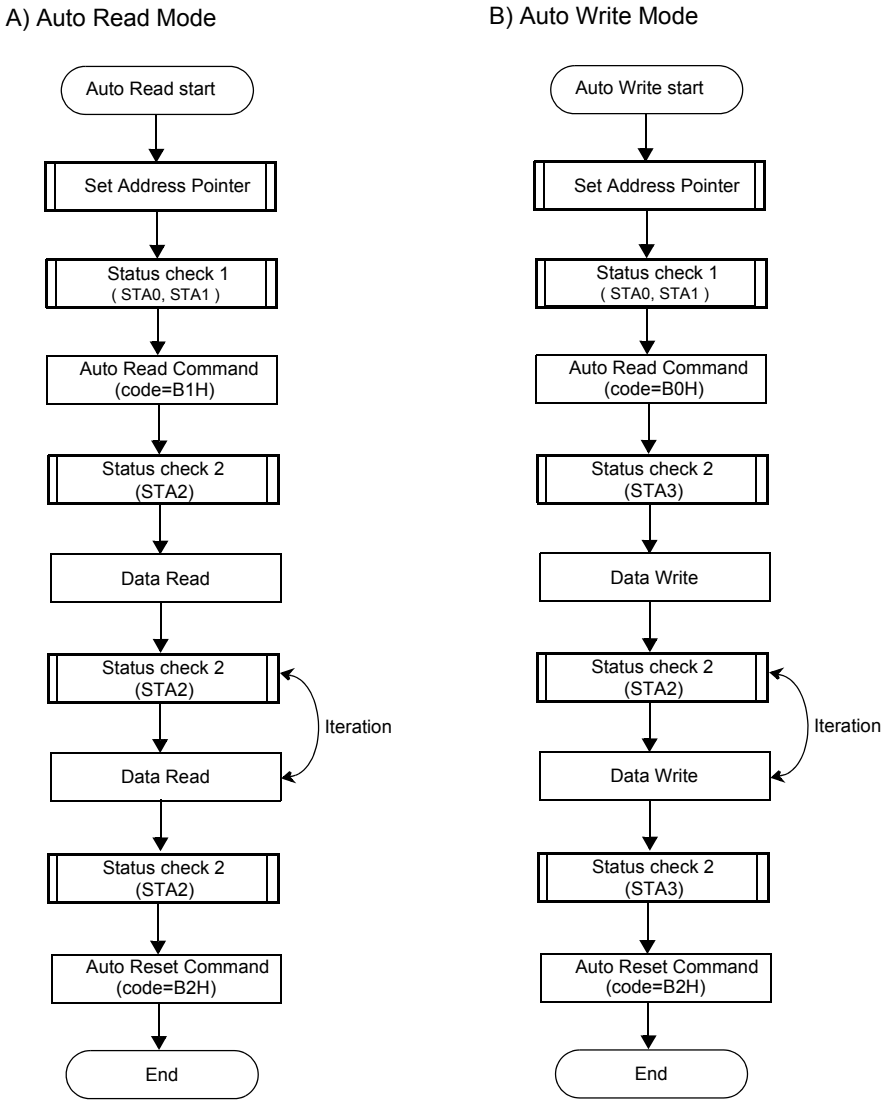


Fig.20 Flowchart for Data Auto Read/Write mode

17 DATA READ/WRITE COMMANDS

These commands are for single-byte data transfer between the microcontroller and the Display Memory.

A single byte of data can be written to or read from the Display Memory by the system microcontroller. The single byte of data is located at the address pointed to by the Address Pointer register. So, before executing these commands, Address Pointer register must be programed to the desired location. After reading or writing operation, the Address Pointer register is automatically incremented or decremented by 1, or kept unchanged.

The commands are given in the following table.

Command code (Binary)	Command code (Hex)	Description	Operand
1100 0000	C0	Data write and increment Address Pointer.	Data
1100 0001	C1	Data read and imcrement Address Pointer.	
1100 0010	C2	Data write and decrement Address Pointer.	Data
1100 0011	C3	Data read and decrement Address Pointer.	
1100 0100	C4	Data write and Address Pointer unchanged.	Data
1100 0101	C5	Data read and Address Pointer unchanged.	

The flow chart for this command is given below.

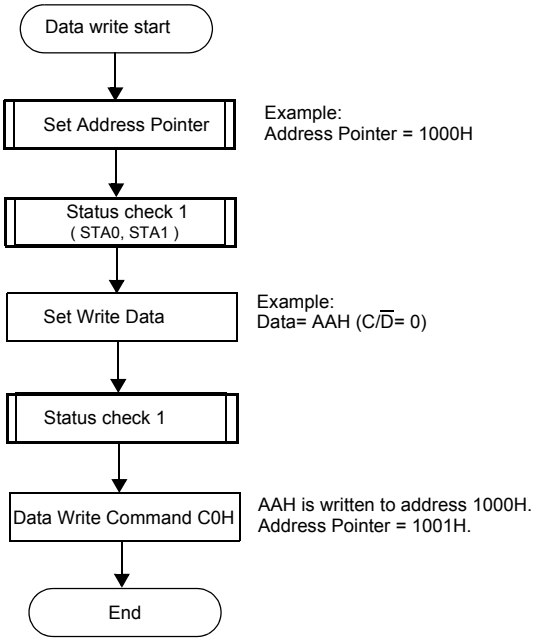


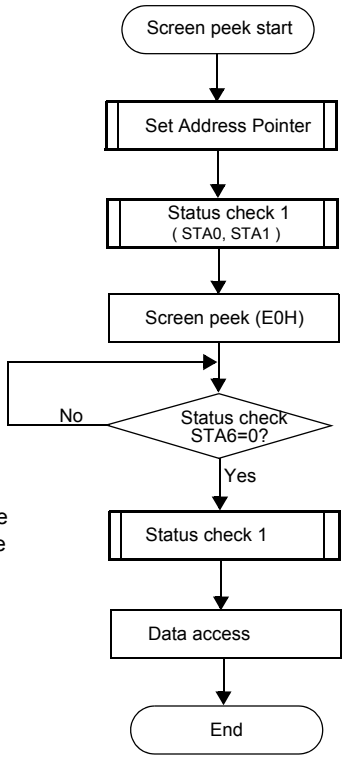
Fig.21 Flowchart for data Read/Write command

18 SCREEN PEAK

The code for this command is 1110 0000 (E0 Hex). It is used to transfer 1 byte of displayed data to the data bus. This byte of data can then be read by the host microcontroller. The logical combination of text and graphic display data on the LCD screen can be read by this command.

The status bit STA6 should be checked right after the Screen Peak command. If the address defined by the Set Address Pointer command is not in the graphic area, this command is ignored and a status flag (STA6) is set.

The flow chart for this command is given below.



This command is available when hardware column number and software column number are the same. Hardware column numbers are selected by MD2 and MD3. Software column number is selected by commands Set Text Area and Set Graphic area.

Fig.22 Flowchart for Screen Copy command

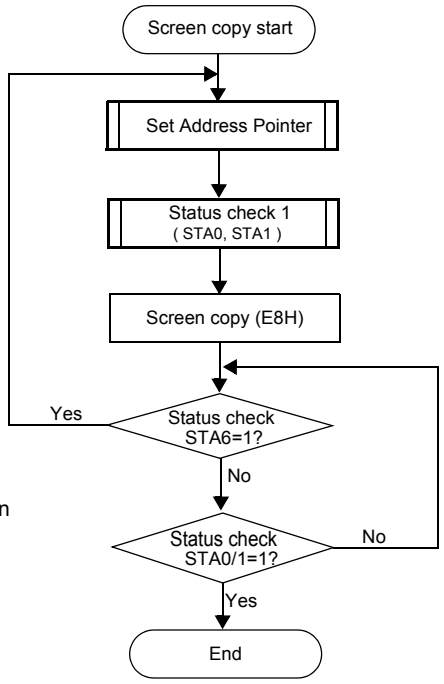
19 SCREEN COPY

The code for Screen Copy command is 1110 1000 (E8 Hex). It copies a single raster scan line of data to the graphic area. The starting address must be set using the Set Address Pointer command.

When Attribute Function is enabled, this command is not available, because the graphic area is used for storing attribute function of the text data.

Because the SAP1024B can not separate the upper screen data from the lower screen data, this command can not be used in dual-scan mode.

The flow chart for this command is given below.



This command is available only when hardware column number and software column number are the same. Hardware column number is defined by MD2 and MD3. Software column number is decided by the commands Set Text Area or Set Graphic area.

Fig.23 Flowchart for Screen Copy command

20 BIT SET / RESET COMMAND

Bit SET/RESET command is used to set or reset an individual bit in the Display Memory. The byte address of the bit is pointed at by the Address Pointer register. This is a one-byte command.

The command table is given below.

Table 18 Bit SET/RESET commands

command	Function
1111 0000	Reset bit 0
1111 0001	Reset bit 1
1111 0010	Reset bit 2
1111 0011	Reset bit 3
1111 0100	Reset bit 4
1111 0101	Reset bit 5
1111 0110	Reset bit 6
1111 0111	Reset bit 7
1111 1000	Set bit 0
1111 1001	Set bit 1
1111 1010	Set bit 2
1111 1011	Set bit 3
1111 1100	Set bit 4
1111 1101	Set bit 5
1111 1110	Set bit 6
1111 1111	Set bit 7

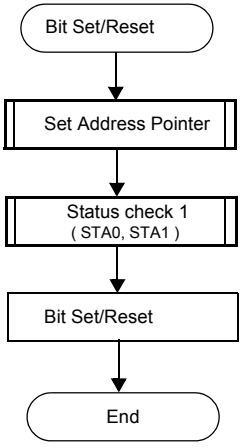
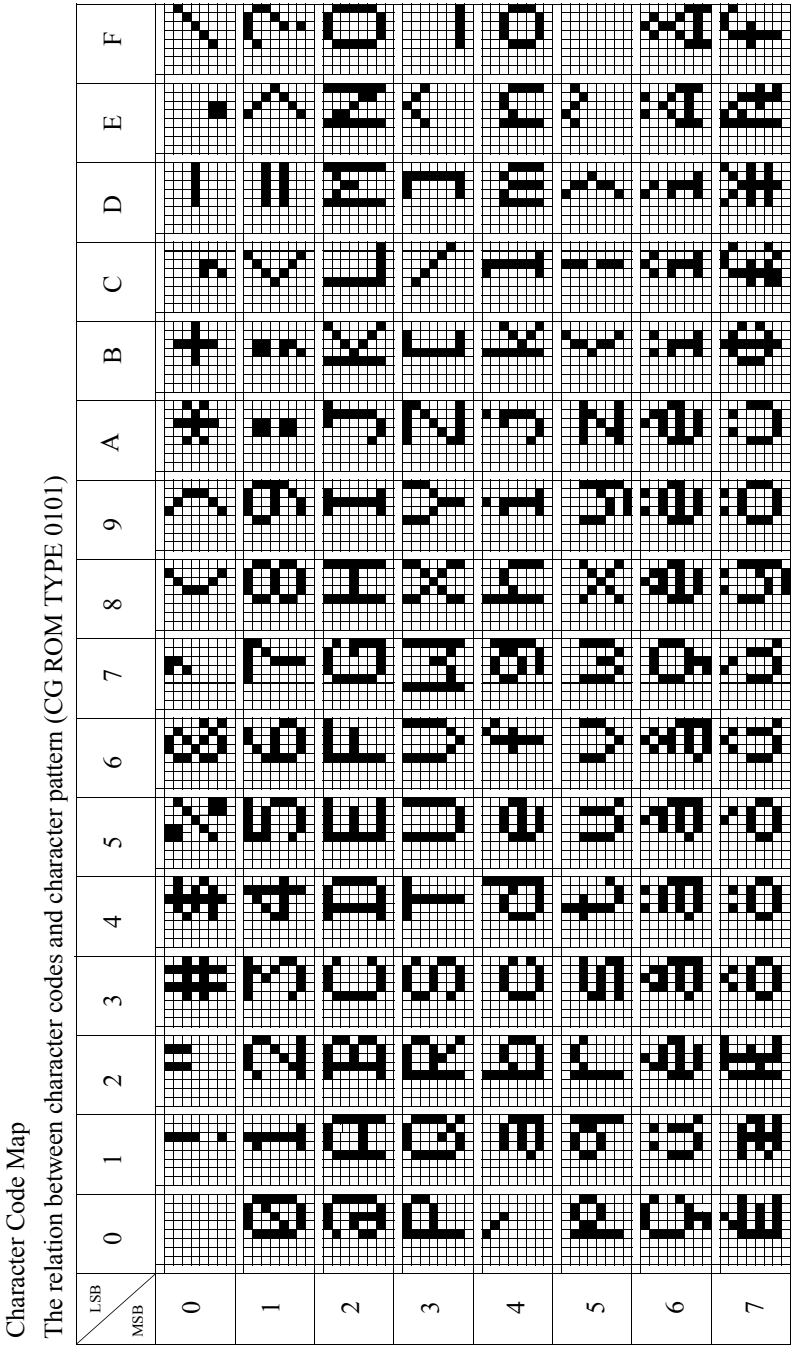


Fig.24 Flowchart for Bit Set/Rest command

21 CHARACTER CODE MAP (CG ROM CODE 0101)

Character Code Map

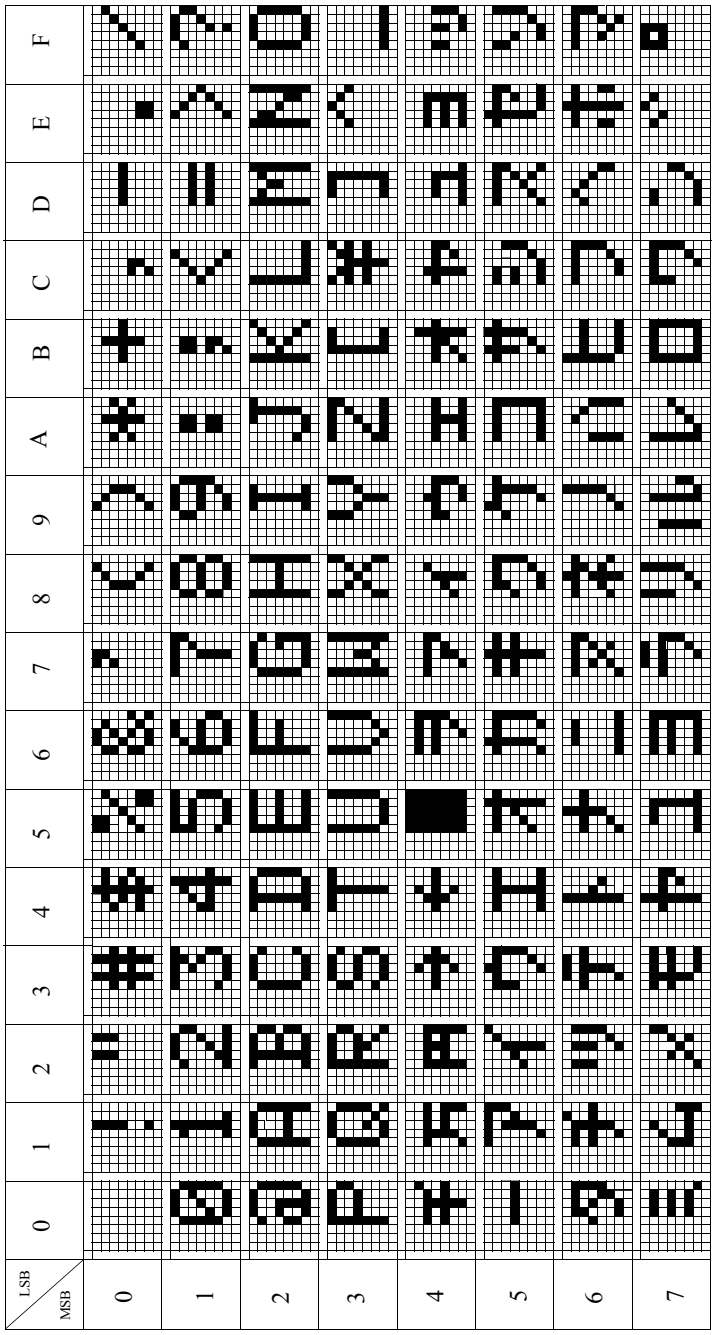
The relation between character codes and character pattern (CG ROM TYPE 0101)



Character Code map (CG ROM type 0201)

Character Code Map

The relation between character codes and character pattern (CG ROM TYPE 0201)



22 ELECTRICAL CHARACTERISTICS

22.1 Absolute maximum rating

Table 19 Absolute maximum rating

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on the VDD input.	–0.3	+7.0	V
V_I (note 1)	input voltage on any pin with respect to V_{SS}	–0.3	V_{DD} + 0.3	V
T_{stg}	storage temperature range	–55	+125	°C
T_{amb}	operating ambient temperature range.	-20	+ 70	°C

Notes

1. The following applies to the Absolute Maximum Rating:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
   b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

22.2 DC characteristics

Table 20 DC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = –20 to +70 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage		2.7	5.0	5.5	V
V_{IL}	LOW level input voltage		0		0.8	V
V_{IH}	HIGH level input voltage		V_{DD}-2.2		V_{DD}	V
V_{OL}	LOW level output voltage		–0.0		0.3	V
V_{OH}	HIGH level output voltage		V_{DD} – 0.3		V_{DD}	V
I_{STBY}	Standby current at V_{DD}=5 volts	Note 1			3.0	µA
$I_{DD(VDD=5V)}$	Operating current at V_{DD}=5 volts	fosc=3.0 MHz and Note 1		3.3	6.0	mA
fosc	Operating frequency		0.4	8.0	12.0	MHZ
$R_{pull-up}$	Internal pull-up resistor of input pins	Note 2, input pins	50	100	200	KΩ
R_{OH}	Pull-up resistance when output is high.	Output pins			400	Ω
R_{OL}	Pull-low resistance when output is low.	Output pins			400	Ω

Notes to the DC characteristics

1. Conditions for the measurement: MDS=L, MD0=L, MD1=L, MD2=H, MD3=H, FS0=L, FS1=L, $\overline{\text{SDSEL}}$=L, $\overline{\text{DUAL}}$=H, D7 to D0=1010101.
2. Measured for T1, T2 and $\overline{\text{RESET}}$.

22.3 Driver clock characteristics

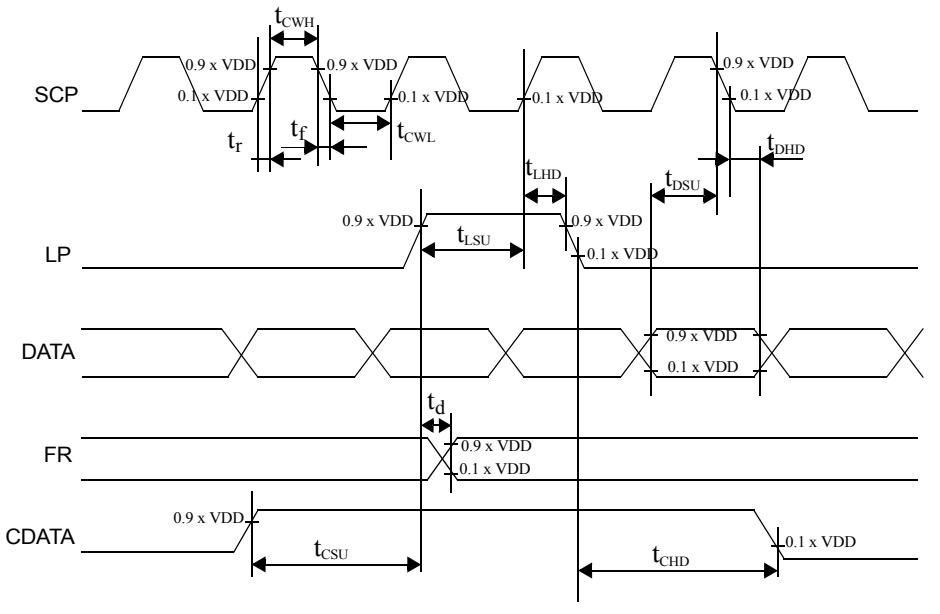


Fig.25 Driver clock characteristics

Table 21 Driver clock characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = −20 to +70 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCP}	Operating frequency	T_{amb} = −10 to +70 °C		2.75	MHz
T_{CWH}, T_{CWL}	SCP pulse width		150		ns
T_r,T_f	SCP Rise/Fall time			30	ns
t_{LSU}	LP set-up time		150	290	ns
t_{LHD}	LP hold time		5	40	ns
t_{DSU}	Data set-up time		170		ns
t_{DHD}	Data hold time		80		ns
t_d	Frame delay time			90	ns
t_{CSU}	CDATA set-up time		450	850	ns
t_{CHD}	CDATA hold time		450	950	ns

22.4 Microcontroller bus interface timing

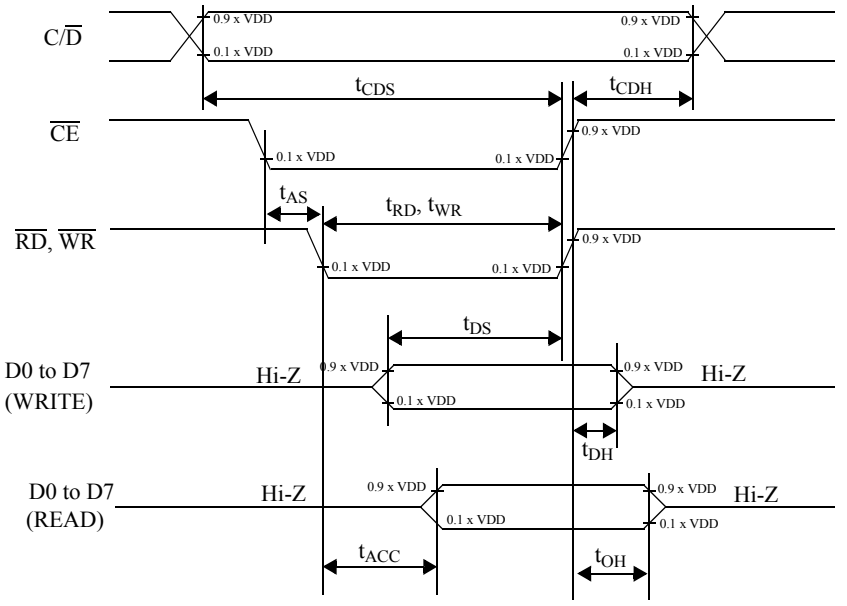


Fig.26 Microcontroller bus interface timing

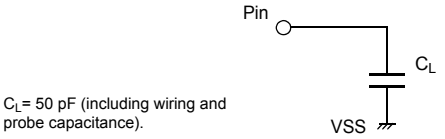
Table 22 Microcontroller interface timing

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = -20 °C to +70°C.

symbol	parameter	MIN.	MAX.	test conditons	Unit
t_{CDS}	C/$\overline{D}$ set-up time	100			ns
t_{CDH}	C/$\overline{D}$ hold time	10			ns
t_{RD}, t_{WR}	$\overline{RD}$, $\overline{WR}$ pulse width	80			ns
t_{AS}	Address set-up time	0			ns
t_{AH}	Address hold time	0			ns
t_{DS}	Data set-up time	80			ns
t_{DH}	Data hold time	40		Note	ns
t_{ACC}	Access time		150	Note	ns
t_{OH}	Output hold time	10	50	Note	ns

Note:

The measurement is with the load circuit connected.



C_L= 50 pF (including wiring and probe capacitance).

Fig.27 Load circuit.

22.5 Display Memory Read/Write Timing

22.5.1 DISPLAY MEMORY READ TIMING

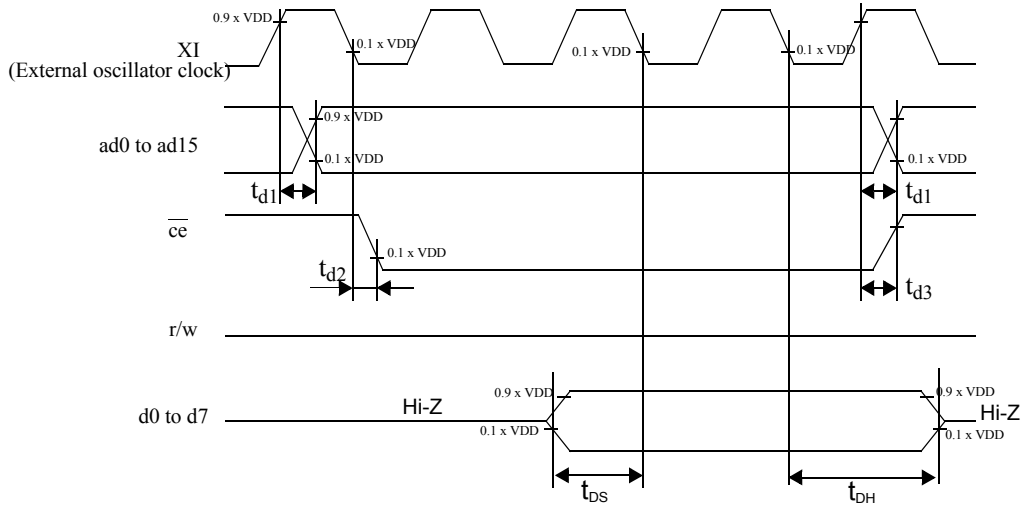


Fig.28 Display Memory Read timing

22.5.2 DISPLAY MEMORY WRITE TIMING

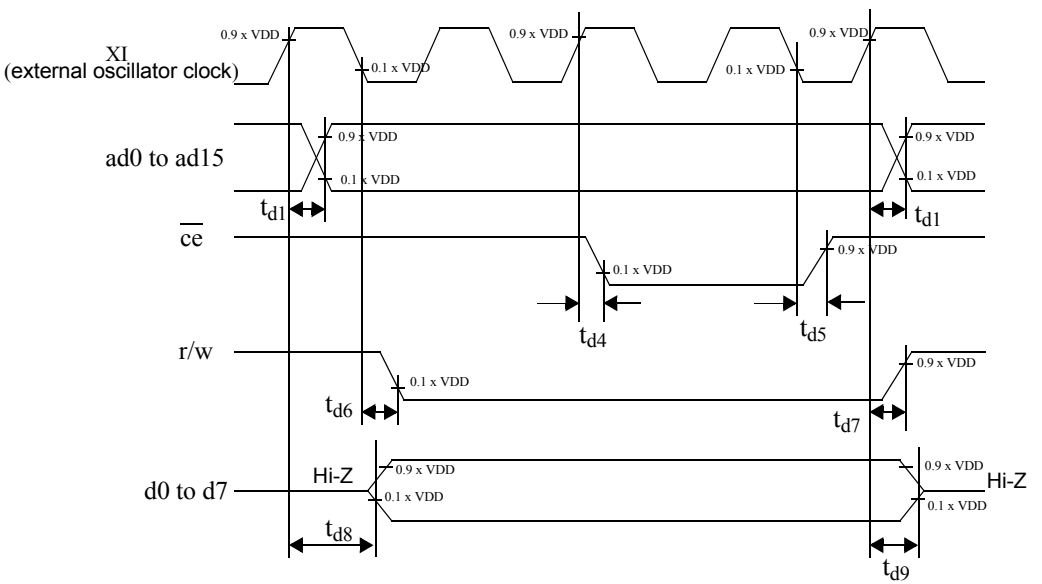


Fig.29 Display Memory Write timing

Table 23 Switcing characteristics (3)

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = -20 °C to +70°C.

symbol	parameter	MIN.	MAX.	test condition	unit
t_{d1}	Address delay time		250		ns
t_{d2}	$\overline{ce}$ fall delay time (Read)		180		ns
t_{d3}	$\overline{ce}$ rise delay time (Read)		180		ns
t_{DS}	Data set-up time	0			ns
t_{DH}	Data hold time	30			ns
t_{d4}	$\overline{ce}$ fall delay time (Write)		200		ns
t_{d5}	$\overline{ce}$ fall delay time (Write)		200		ns
t_{d6}	r/w fall delay time		180		ns
t_{d7}	r/w rise delay time		180		ns
t_{d8}	Data stable time		450	Refer to Fig.27 for measuring condition.	ns
t_{d9}	Data hold time		200		ns

23 EXAMPLE OF INTERFACE CIRCUITS

23.1 Example for Interfacing with a Z80-like microcontroller

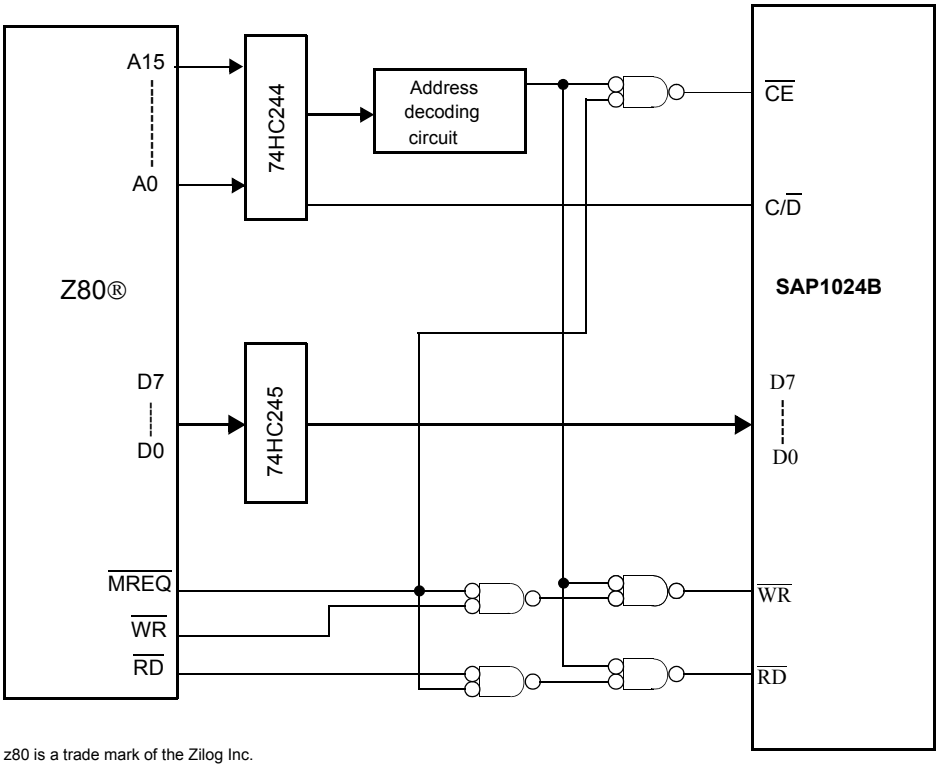


Fig.30 Interface with a Z80-like MPU.

23.2 Example for interfacing with a C51 microcontroller

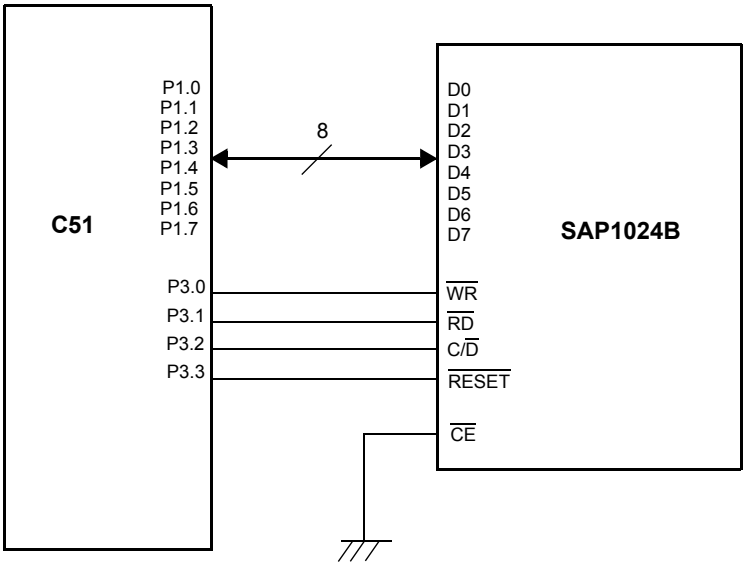


Fig.31 Interface with C51 microcontorller.

24 APPLICATION CIRCUIT

24.1 Application circuit (64 x 320 dots)

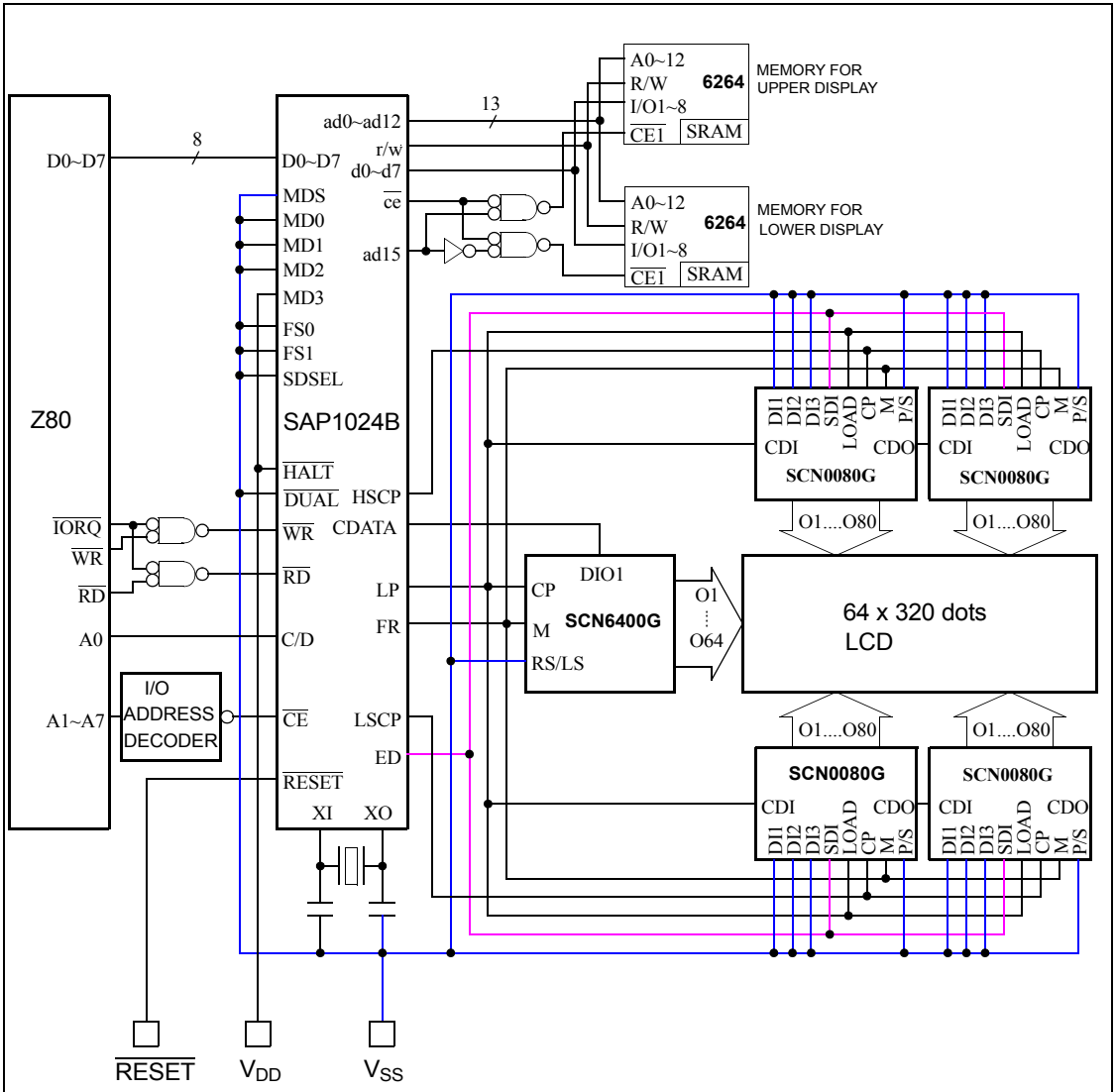


Fig.32 Application circuit for 64 x 320 dots

24.2 Application circuit (64 x 160 dots)

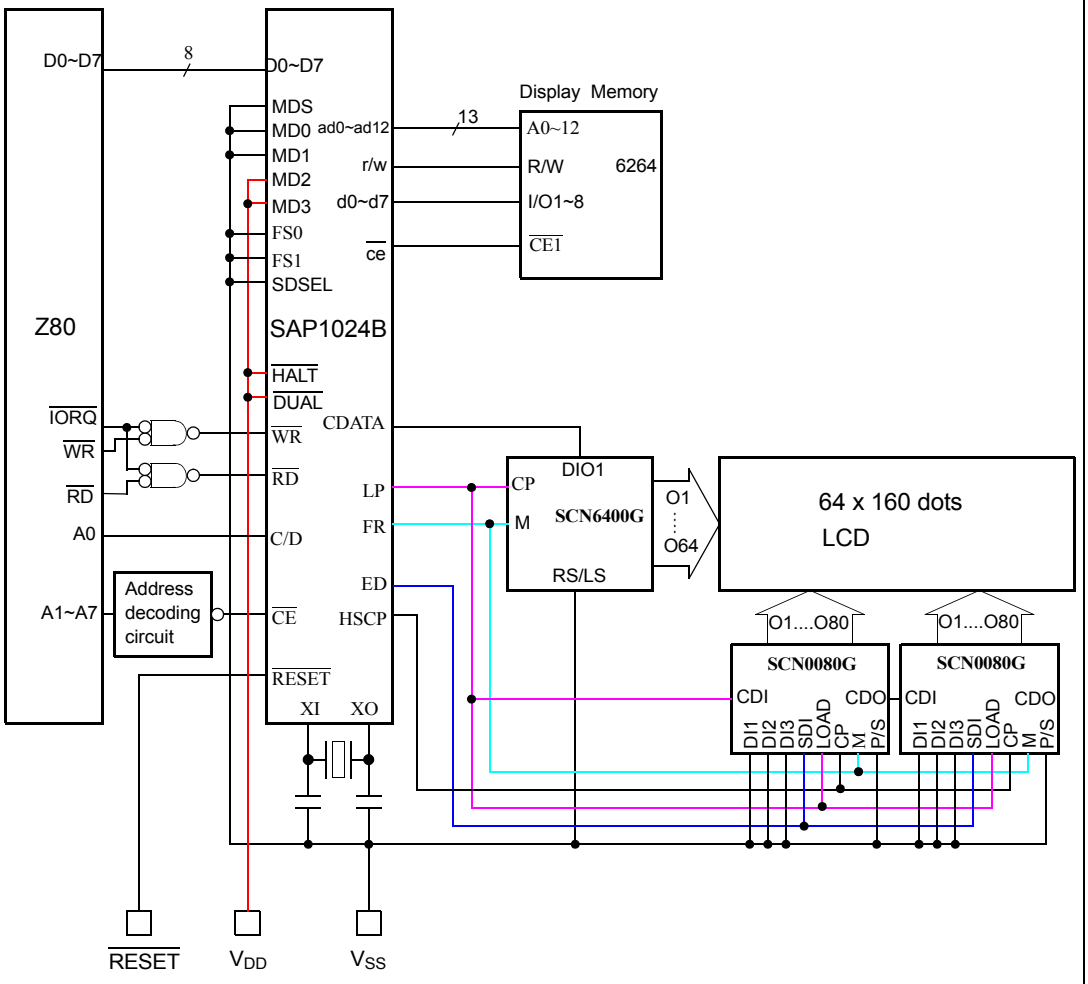
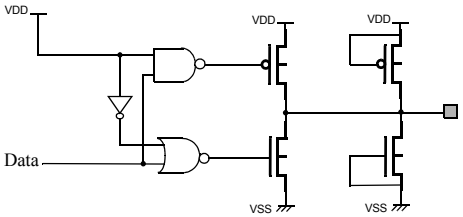
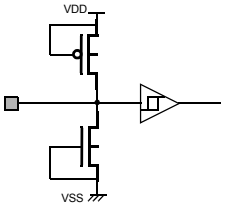
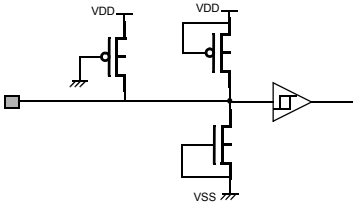
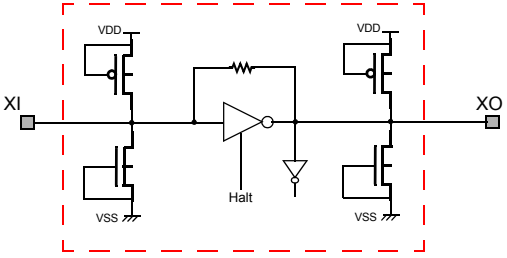
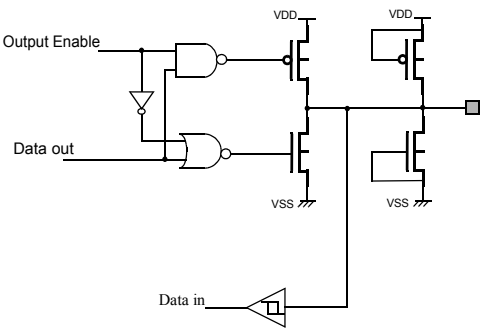


Fig.33 Application circuit for 64 x 160 dots.

25 PIN CIRCUITS

Table 24 MOS-level schematics of all input, output, and I/O pins.

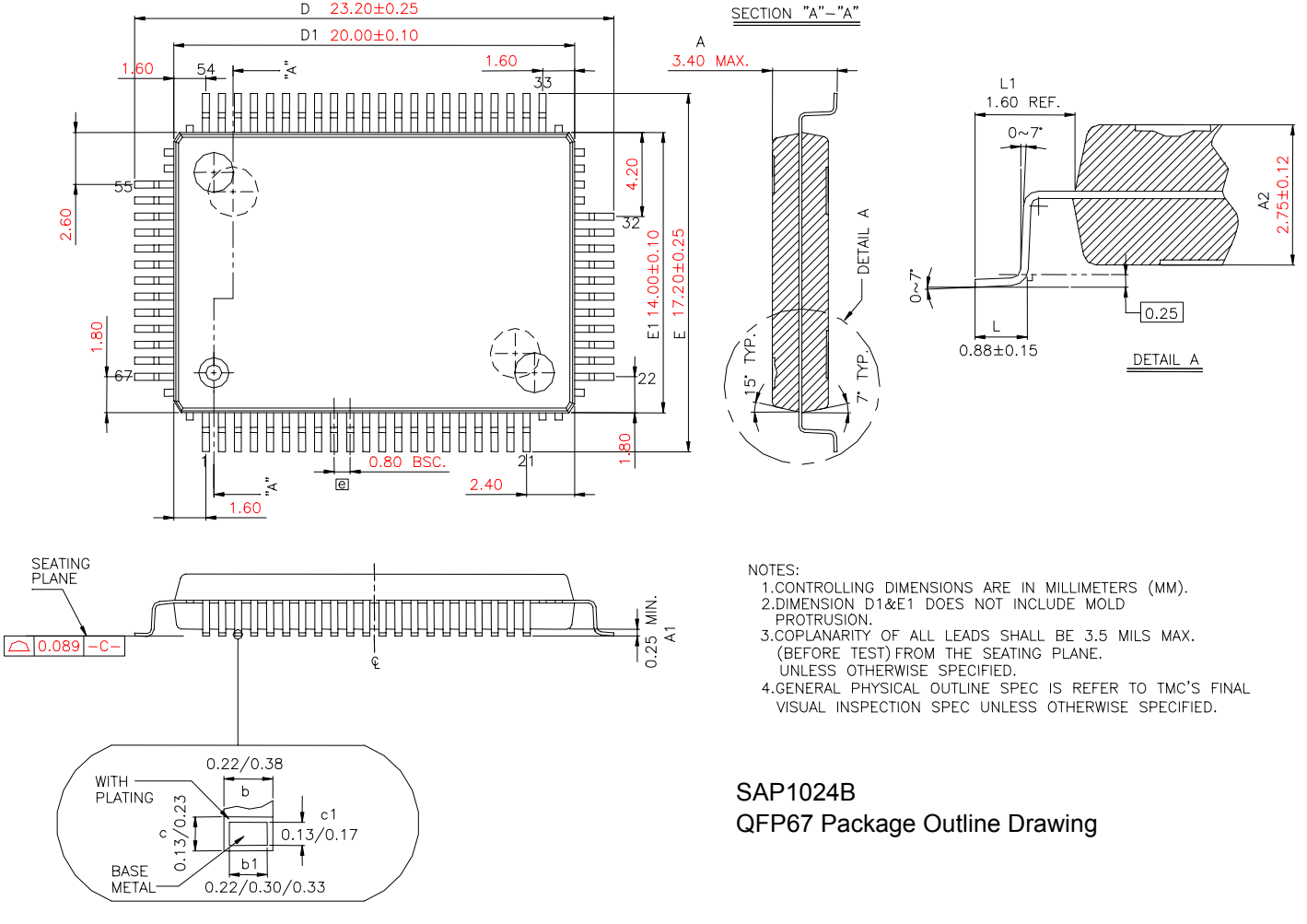
SYMBOL	Input/ output	CIRCUIT	NOTES
r/w, $\overline{ce}$, $\overline{ad0}$~$\overline{ad15}$, $\overline{ce0}$, $\overline{ce1}$, HOD, ED, HSCP, LP, CDATA, FR, CH1, CH2, DPSON	Outputs		These outputs are for interface with Display Memory, COMMON drivers, and SEGMENT drivers.
MDS, MD0, MD1, MD2, MD3, $\overline{FS0}$, $\overline{FS1}$, $\overline{WR}$, $\overline{RD}$, $\overline{CE}$, C/$\overline{D}$, $\overline{DUAL}$, $\overline{SDEL}$	Inputs		
$\overline{RESET}$, $\overline{HALT}$, $\overline{T1}$, $\overline{T2}$	Input with internal pull-up		
XI, XO	Input and output		The circuit encircled inside the red dashed frame is the oscillator circut.

SYMBOL	Input/ output	CIRCUIT	NOTES
D0~D7, d0~d7	I/O		

26 APPLICATION NOTES

- After power-on, it is necessary to reset the SAP1024B. To ensure complete reset, $\overline{\text{RESET}}$ should be kept L for at least 5 XI oscillator period.
- When $\overline{\text{HALT}}$ =L, the oscillation stops.The power supply of the LCD must now be turned off to protect the LCD from DC bias.
- The $\overline{\text{HALT}}$ function includes the RESET function.
- The SAP1024B maintains an internal column counter and a line counter. The column counter indicates which character in the horizontal direction is being display. The line counter indicates which character in the vertical direction is being displayed. Both the column counter and the line counter are cleared to zero at RESET. Therefore, after RESET, the starting position of display is at the leftmost position of the topmost line. Other internal registers are not cleared.
- Disable the display using the clear-display command.
- The status check must be performed before data or commands are sent, to ensure that the SAP1024B is ready for accepting new command or data.
- Hardware interrupt to the host microcontroller in the middle of data read/write or status check may cause erroneous operation.
- STA0 and STA1 must be checked simultaneously.
- The character codes used by the SAP1024B are different from ASCII codes.

27 PACKAGE INFORMATION



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (MM).
2. DIMENSION D1&E1 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE 3.5 MILS MAX. (BEFORE TEST) FROM THE SEATING PLANE. UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLINE SPEC IS REFER TO TMC'S FINAL VISUAL INSPECTION SPEC UNLESS OTHERWISE SPECIFIED.

SAP1024B
QFP67 Package Outline Drawing

28 SOLDERING

28.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

28.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

28.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

28.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

29 LIFE SUPPORT APPLICATIONS

Avant's products, unless specifically specified, are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling Avant's products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.