DATA SHEET

SDN0080G
80-Segment Dot-matrix STN LCD Driver

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1 GENERAL

1.1 Description

The SDN0080G is an 80-segment dot-matrix STN LCD driver. It is to be paired with the SDN8000G 80-common driver.

1.2 Features

- 80-output segment driver for dot-matrix STN LCD.
- Display duty : 1/64 to 1/256
- Power-down mode (Display OFF) for reducing power consumption.
- External LCD bias voltage.
- 4-bit parallel data bus for interfacing with a controller.
- Can be cascaded to expand segment number.
- Operating voltage range (for control logic): 2.7 ~ 5.5 volts.
- Operating voltage range (for high-voltage LCD bias, V_{DD}-V_{EE}): 12 ~ 32 volts.
- Data transfer clock: 6.0 MHz, when V_{DD}= 5 volts.
- Operating temperature range: -20 to +75 °C.
- Storage temperature range: -40 to +125 °C.
- ESD (Human Body Model): ≥ 4K volts.
- Latch-up: ≥ 250 mA.

1.3 Ordering information

Table 1 Ordering information

TYPE NUMBER	DESCRIPTION
SDN0080G-LQFPG	LQFP100 green package.
SDN0080G-QFPG	QFP100 green package.
SDN0080G-LQFP	LQFP100 package.
SDN0080G-QFP	QFP100 package.
SDN0080G-D	tested die.

2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

2.1 Functional block diagram

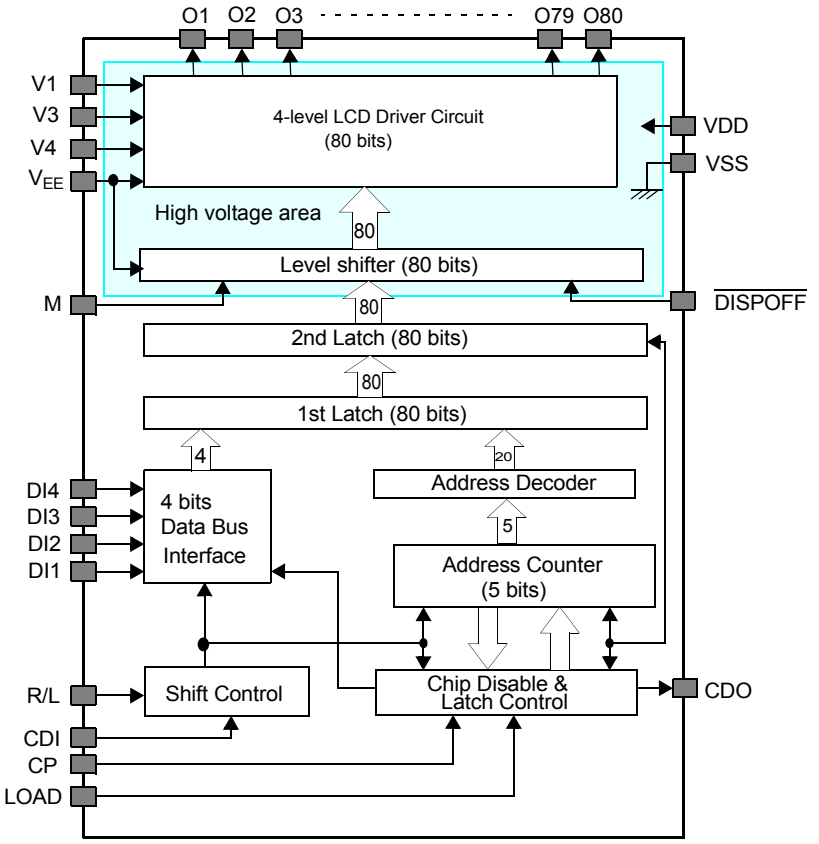


Fig.1 Functional Block Diagram

3 PINNING INFORMATION

3.1 Pinning diagram

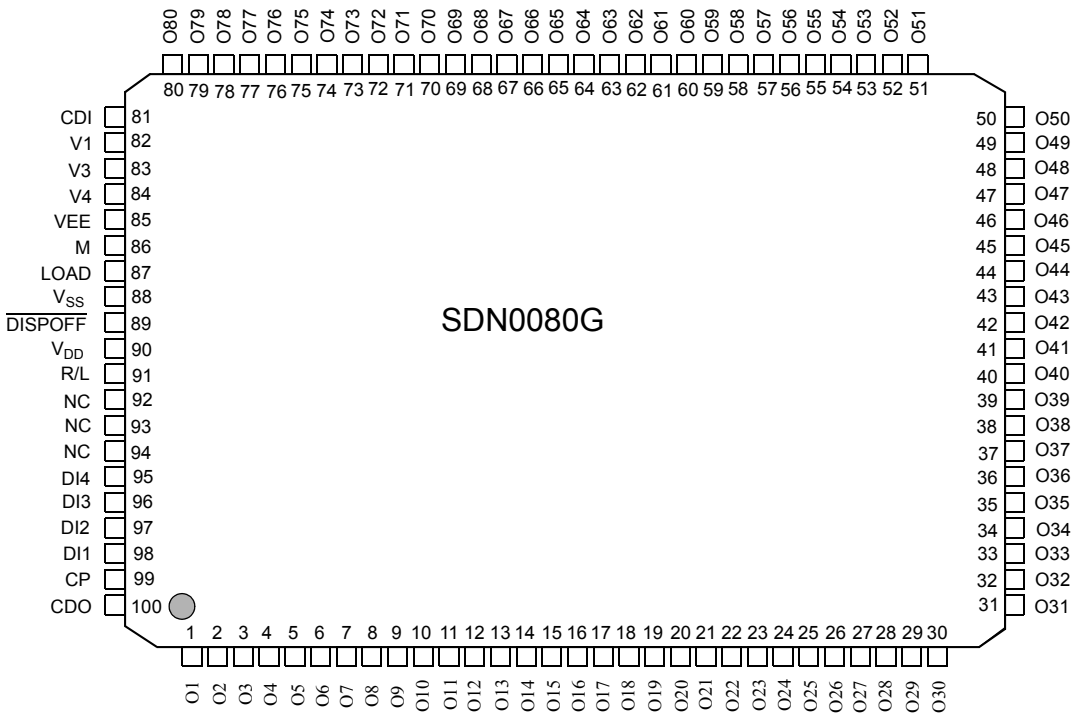


Fig.2 Pin diagram of QFP100 / LQFP100 package

3.2 Signal description

Table 2 Pin signal description.

To avoid a latch-up effect at power-on: $V_{SS} - 0.5\ V <$ voltage at any pin at any time $< V_{DD} + 0.5\ V$.

Pin number	SYMBOL	I/O	DESCRIPTION
1~80	O1~O80	Output	Segment driver output. Please refer to Table 3 for output voltage level.
81	CDI	Input	Chip Disable pin. When CDI=High, on-chip data reception circuit is disabled and data can not be sent into the SDN0080G. When CDI=LOW, data can be sent into the SDN0080G.
82, 83, 84	V1, V3, V4	Input	LCD bias voltage. V1 and V_{EE} are selected levels. V3 and V4 are unselected levels.
85	V_{EE}	Input	Negative power supply for LCD bias.
86	M	Input	Frame signal.
87	LOAD	Input	Display data (80 bits) latch clock. At the falling edge of the LOAD signal, 80-bit segment data is transferred from the first latch to the second latch for output. (Refer to Fig. 1, Functional Block Diagram.
88	V_{SS}	Input	Ground.
89	$\overline{\text{DISPOFF}}$	Input	Display Disable. When $\overline{\text{DISPOFF}}$=L, the outputs O1~O81 are all at a fixed level of V1.
90	V_{DD}	Input	Power supply for control logic.
91	R/L	Input	Shift direction control for display data reception from a controller.
92, 93, 94	NC		No Connection. These pins are not used in application and must be left open.
95, 96, 97, 98	DI4 ~ DI1	Input	4-bit parallel data bus for interfacing with a controller. The 4 bits of data are latched into the SDN0080G at the falling edge of the CP clock. Please refer to Fig 3.
99	CP	Input	Display data latch clock. 4 bits of display data (DI1~DI4) are latched into the internal 80-bit latch at the falling edge of CP. Please refer to Fig 3.
100	CDO	Output	Cascading output when the SDN0080G are used in cascade.

4 FUNCTIONAL DESCRIPTION

4.1 Segment output drive (O1~O80)

The voltage level of the outputs O1~O80 is determined by Input data (display data), M (frame signal), and $\overline{\text{DISPOFF}}$, as given in the following table.

Table 3 output voltage level of O1~O80

M	Data	$\overline{\text{DISPOFF}}$	Output
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	V_{EE}
X	X	L	V1

In the above table, X= don't care and must be tied either to H or L.

4.2 Display Data Inputs (DI1~DI4)

The SDN0080G has a 4-bit parallel data bus (DI1~DI4) to interface with a controller. A logic High of a bit represents an ON cell (black pixel on the LCD screen).

Table 4 Data bits

Display data	**LCD drive output**	**LCD display**
H	Selected level (V1, V_{EE})	ON
L	Unselected level (V3, V4)	OFF

4.3 Sequence of data input

When R/L=L, the 4-bit data that is first latched goes to O77 ~ O80 and the 4-bit data that is last latched goes to O1 ~ O4.
When R/L=H, the 4-bit data that is first latched goes to O1 ~ O4 and the 4-bit data that is last latched goes to O77 ~ O80.

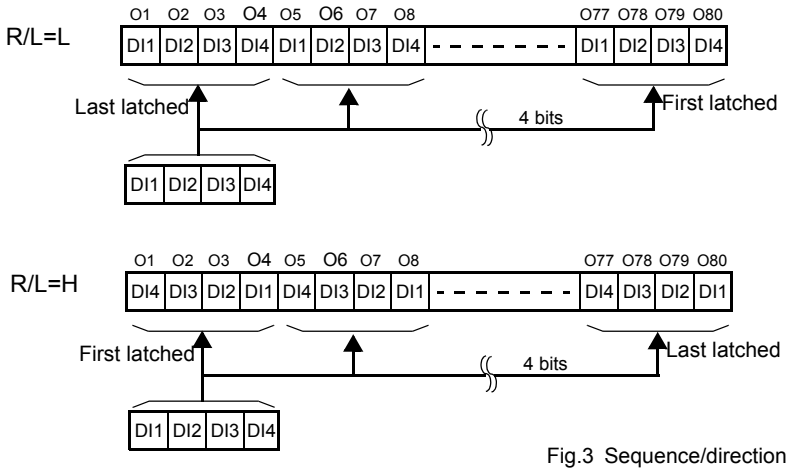


Fig.3 Sequence/direction of display data input

5 ABSOLUTE MAXIMUM RATING

Table 5 Absolute maximum rating

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25±2°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Voltage on the V_{DD} input	−0.3	+7.0	V
V_{DD}-V_{EE}	LCD bias voltage, note 1	0	35	V
Vi(max)	Maximum input voltage to input pins	-0.3	V_{DD} + 0.3	V
T_{amb}	Operating ambient temperature range	-20	+ 75	°C
T_{stg}	Storage temperature range	−40	+125	°C

Note:

1. The condition $V_{DD} \geq V1 > V3 > V4 > V_{EE}$ must always be met.

6 DC CHARACTERISTICS

Table 6 DC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage for control logic	Please refer to Fig. 10 for DC power-up sequence.	2.7	5.0	5.5	V
V_{DD}-V_{EE}	LCD bias voltage	Note 1.	12		32	
V_{IL}	Input LOW voltage of input pins	DI1~DI4, CP, LOAD, CDI, R/L, M, $\overline{\text{DISPOFF}}$	0		0.2V_{DD}	V
V_{IH}	Input HIGH voltage of input pins	DI1~DI4, CP, LOAD, CDI, R/L, M, $\overline{\text{DISPOFF}}$	0.8V_{DD}		V_{DD}	V
I_{IL}	Input LOW leakage current of input pins (i. e. Reverse leakage current of input ESD protection diode)	V_{IN}=V_{SS}, LOAD, CP, CDI, R/L, DI1~DI4, M, $\overline{\text{DISPOFF}}$			1	μA
I_{IH}	Input HIGH leakage current of input pins (i. e. Reverse leakage current of input protection diode)	V_{IN}=V_{DD}, LOAD, CP, CDI, R/L, DI1~DI4, M, DISPOFF			1	μA
V_{OL}	Output LOW voltage level of the CDO pin	I_{OL}=400μA	0.0		0.4	V
V_{OH}	Output HIGH voltage level of the CDO pin	I_{OH}=-400μA	V_{DD} − 0.4		V_{DD}	V
I_{STBY}	Standby current	Note 2.			200	μA
I_{SS}	Operating current	Note 3.			4.0	mA
I_{EE}	Operating current	Note 4.			0.5	mA
Ci	Input capacitance of the CP pin	The CP clock frequency is 6.0 MHz.		5.0		pF
R_{ON1}	Driver ON resistance at V_{LCD}= 30 V	Note 5.		1.5	3.0	KΩ
R_{ON2}	Driver ON resistance at V_{LCD}= 20 V	Note 6.		2.0	3.5	KΩ

Notes:

1. The condition $V_{DD} \geq V1 > V3 > V4 > V_{EE}$ must always be met.
2. CDI=V_{DD}, V_{DD}-V_{EE}=30 V, CP=6.0MHz, Output unloaded; measured at the V_{SS} pin.
3. Condition for the measurement: V_{LCD}=V_{DD}-V_{EE}=30 V, CP=6.0 MHz, LOAD=14 KHz, M=35 Hz. This is the current flowing from V_{DD} to V_{SS}, measured at the V_{SS} pin.
4. Condition for the measurement: V_{LCD}=V_{DD}-V_{EE}=30 V, CP=6.0 MHz, LOAD=14 KHz, M=35 Hz. This is the current flowing from V_{DD} to V_{EE}, measured at the V_{EE} pin.
5. Condition for the measurement: V_{DD}-V_{EE}=30 V, $|V_{DE}$-$V_O|$=0.5 V, where V_{DE}= one of V1, V3, V4, or V_{EE}. V1=V_{DD}, V3= (15/17) x (V_{DD}-V_{EE}), V4= (2/17) x (V_{DD}-V_{EE}). For the driver circuits (O1~O80), please refer to Section 11 Pin Circuits.
6. Condition for the measurement: V_{DD}-V_{EE}=20 V, $|V_{DE}$-$V_O|$=0.5 V, where V_{DE}= one of V1, V3, V4, or V_{EE}. V1=V_{DD}, V3= (15/17) x (V_{DD}-V_{EE}), V4= (2/17) (V_{DD}-V_{EE}). For the driver circuits (O1~O80), please refer to Section 11 Pin Circuits.

7 AC CHARACTERISTICS

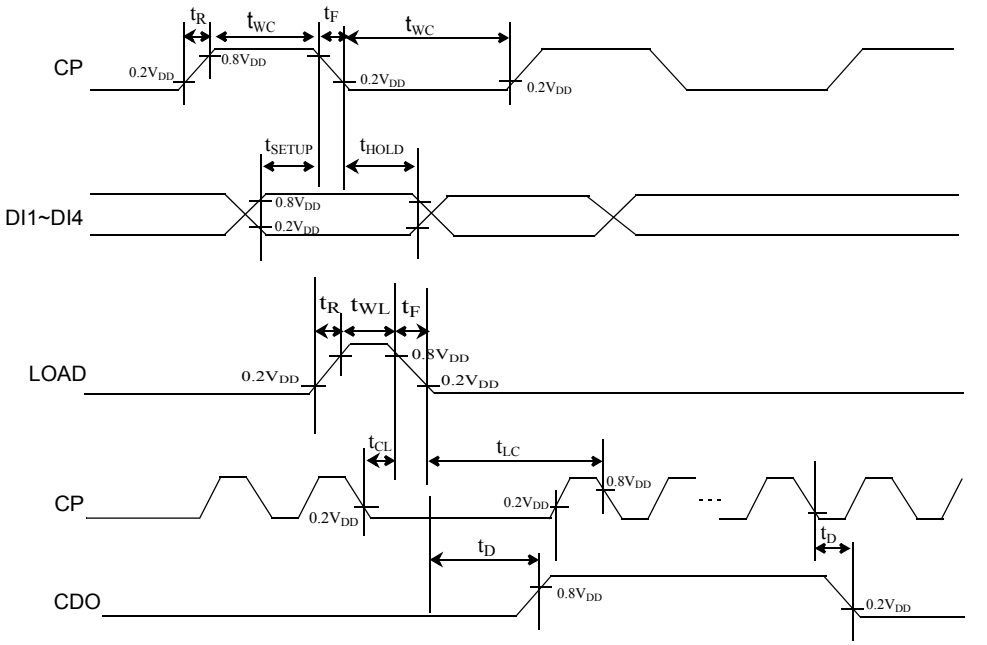


Fig.4 AC characteristics

Table 7 AC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25 ±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{CP}	CP clock frequency			6.0	MHz
T_{WC}	CP clock pulse width		50		ns
T_{WL}	LOAD clock pulse width		50		ns
t_{SETUP}	Input data setup time	DI1~DI4 data to the falling edge of the CP clock.	30		ns
t_{HOLD}	Input data hold time.	Falling edge of the CP clock to DI1~DI4 data change.	30		ns
t_{CL}	CP to LOAD		80		ns
t_{LC}	LOAD to CP		110		ns
t_R	CP and LOAD rise time	Note 1.		4	ns
t_F	CP and LOAD fall time	Note 1.		4	ns
t_D	Output delay time	the CDO pin, Load=15pF.		80	ns

Note:

1. The rise time t_R and the fall time t_F of CP and LOAD must comply with the following two conditions.
   a) $t_R, t_F < \frac{1}{2f_{CP}} - t_{WC}$
   b) t_R, t_F < 50 ns.

8 OUTPUT TIMING DIAGRAM

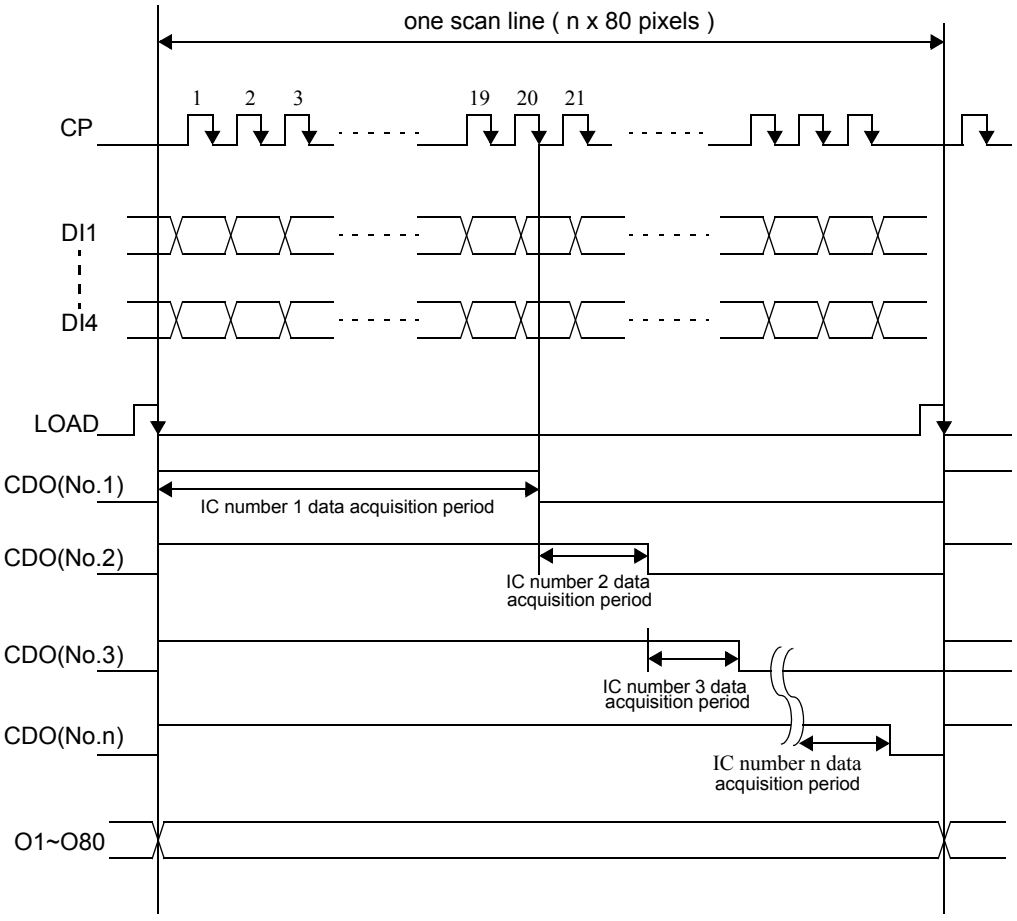


Fig.5 Output timing diagram

9 TIMING CHART (1/240 DUTY, 1/16 BIAS)

9.1 1/240 duty timing chart

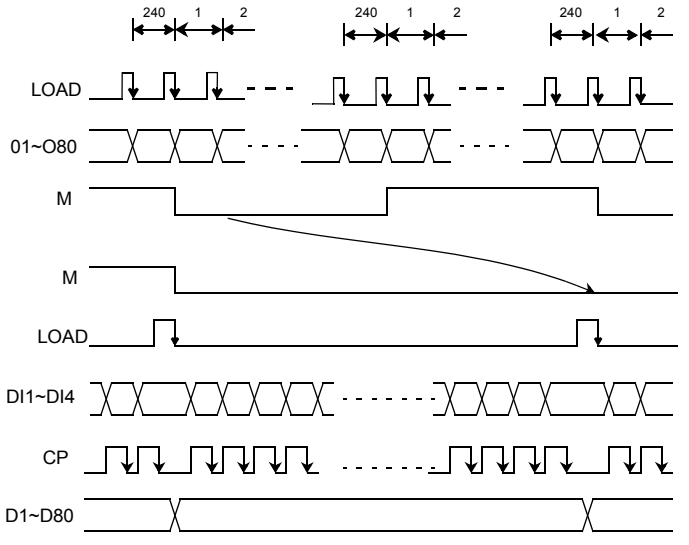


Fig.6 1/240 duty timing chart

9.2 1/16 bias

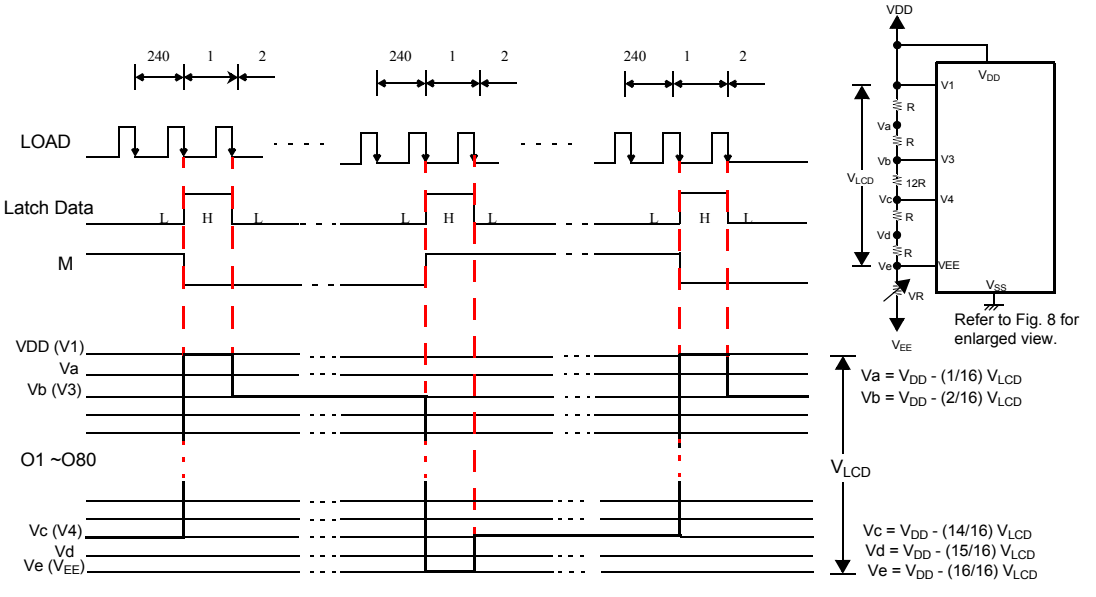
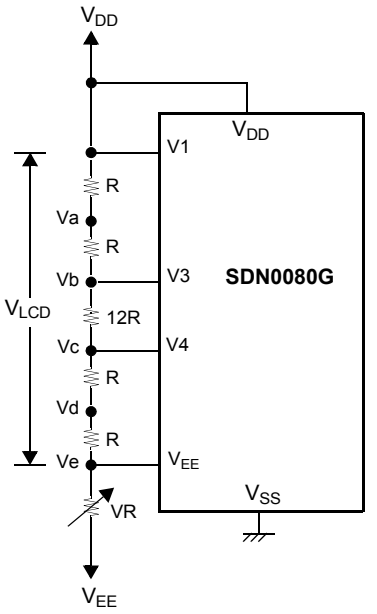


Fig.7 1/16 bias

9.3 Bias circuit



Va = V_{DD} - (1/16) V_{LCD}

Vb = V_{DD} - (2/16) V_{LCD}

Vc = V_{DD} - (14/16) V_{LCD}

Vd = V_{DD} - (15/16) V_{LCD}

Ve = V_{DD} - (16/16) V_{LCD}

Fig.8 LCD bias voltage

10 APPLICATION CIRCUIT (240 X 640 DOT)

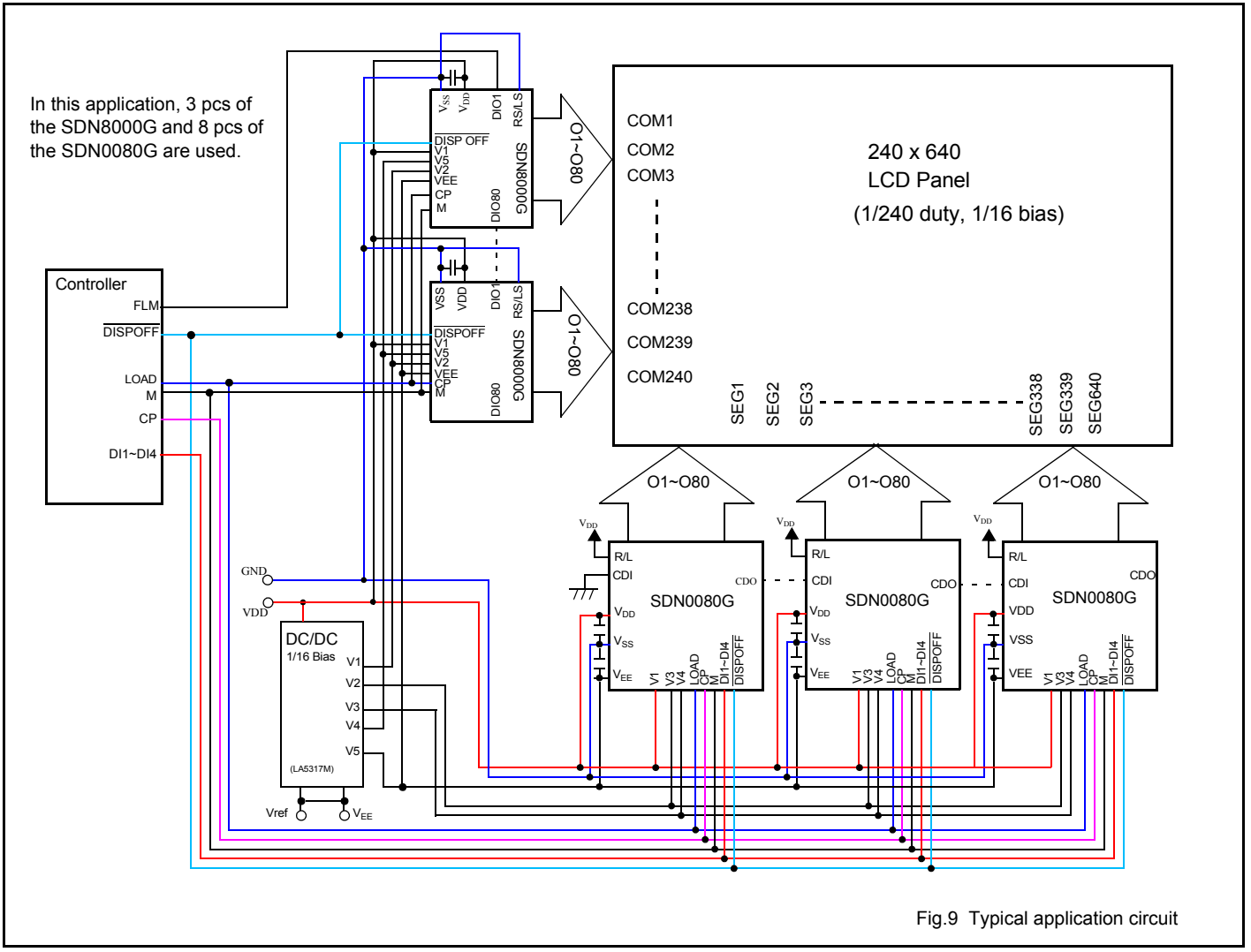
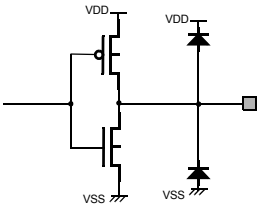
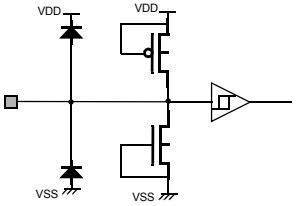
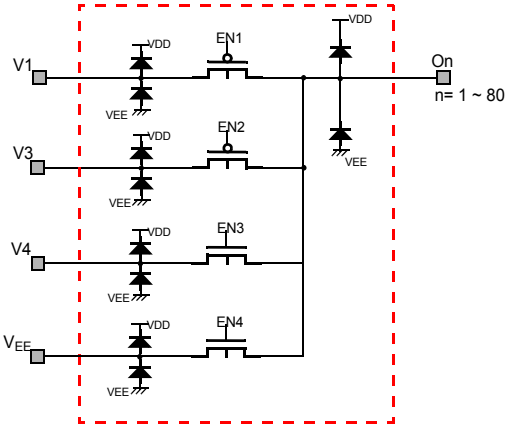


Fig.9 Typical application circuit

11 PIN CIRCUITS

Table 8 MOS-level schematics of all input, output, and I/O pins.

SYMBOL	Input/ output	CIRCUIT	NOTES
CDO	Output		
CP, LOAD, DI1~DI4, R/L, M, CDI, DISPOFF	Inputs		
O1~O80, V1, V3, V4, V_{EE}	Driver outputs, High voltage inputs		

12 APPLICATION NOTES

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias (V_{EE}).

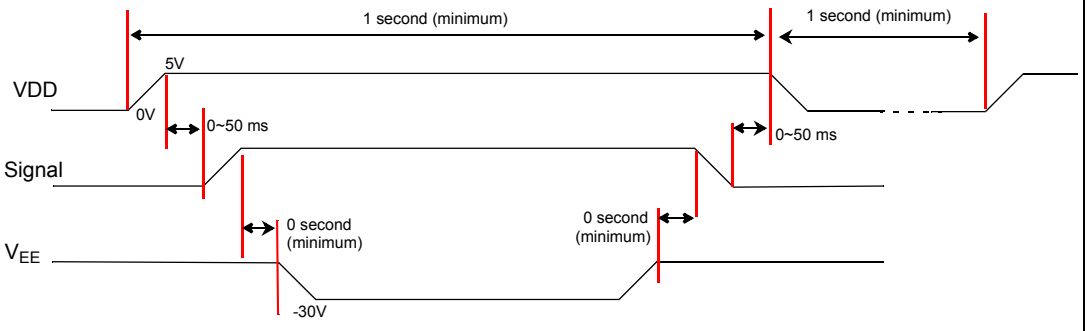
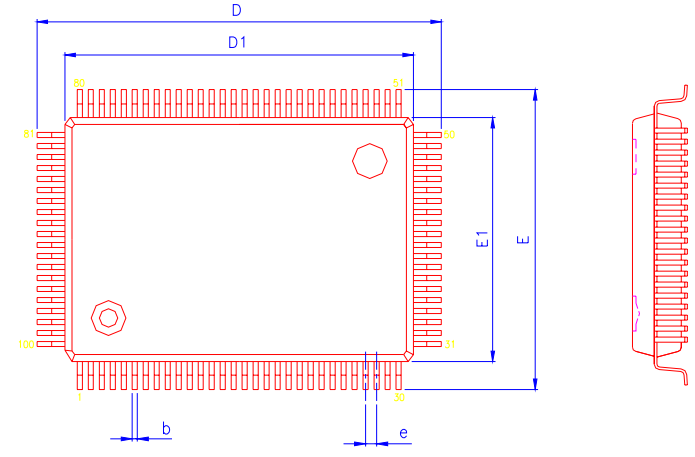
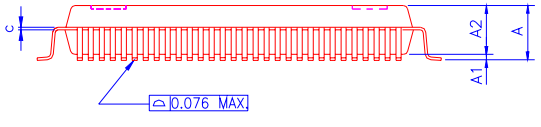
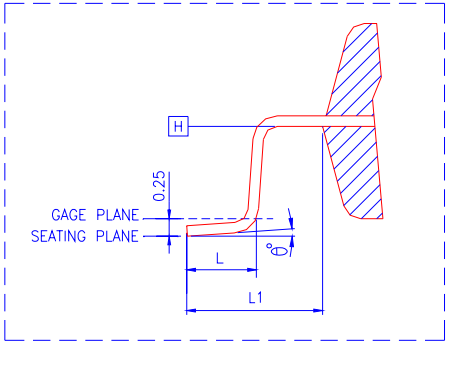


Fig.10 Recommended power up/down sequence

13 PACKAGE INFORMATION







SYMBOLS	MIN.	NOM	MAX.
A	–	–	3.40
A1	0.25	–	0.50
A2	2.50	2.70	2.90
b	0.22	–	0.40
c	0.11	–	0.23
D		23.20 BASIC	
D1		20.00 BASIC	
e		0.65 BASIC	
E		17.20 BASIC	
E1		14.00 BASIC	
L	0.73	0.88	1.03
L1	–	1.60	–
θ°	0	–	7

UNIT : mm

NOTES:

1.JEDEC OUTLINE:MS-022 GC-1

2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

SDN0080G

QFP100 Package Outline Drawing

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

14.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.