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DATA SHEET

SEN6A39
80-COLUMN driver for dot-matrix STN LCD

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1 GENERAL

1.1 Description

The SEN6A39 is an 80-COLUMN (SEGMENT) driver for dot-matrix STN LCD. It is desinged to be paired with the SEN6A40 68-ROW (COMMON) driver.

1.2 Features

- 80-output COLUMN driver for dot-matrix STN LCD module.
- Display duty : up to 1/240.
- Data transfer with a controller: 1, 2, 4-bits, bi-directional.
- Data transfer clock: 6.0 MHz, when V_{DD}= 5 volts.
- Can be cascaded to expand column number.
- External LCD bias voltage.
- Operating voltage range (control logic): 2.7 ~ 5.5 volts.
- Operating voltage range (LCD bias, V_{DD}-V5): 8 ~ 30 volts.
- Operating temperature range: -20 to +75 °C.
- Storage temperature range: -55 to +125 °C.

1.3 Ordering information

Table 1 Ordering information

TYPE NUMBER	DESCRIPTION
SEN6A39-LQFPG	LQFP100 Green package.
SEN6A39-QFPG	QFP100 Green package.
SEN6A39-LQFP	LQFP100 package.
SEN6A39-QFP	QFP100 package.

2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

2.1 Funtional block diagram

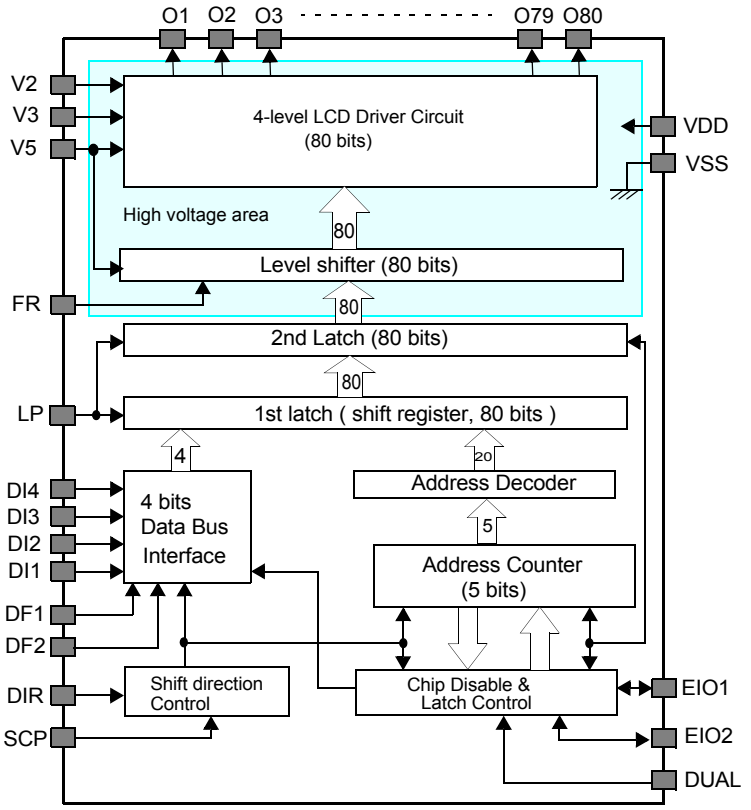


Fig.1 Functional Block Diagram

3 PINNING INFORMATION

3.1 Pinning diagram

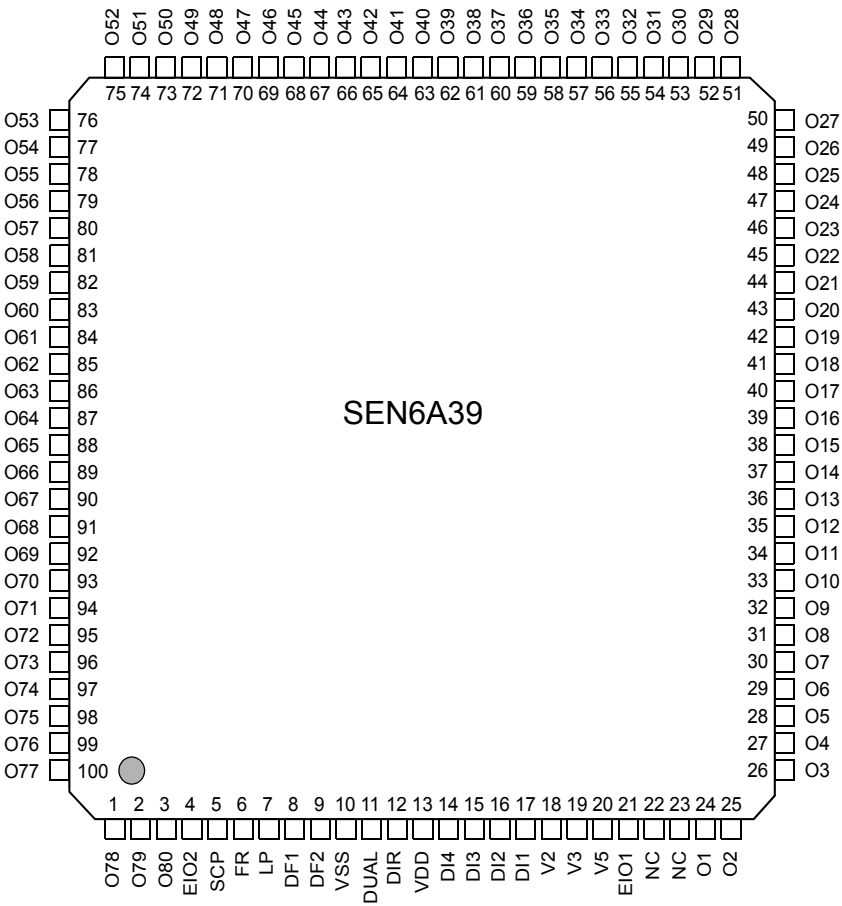


Fig.2 Pin diagram of LQFP100/QFP100 package

3.2 Signal description

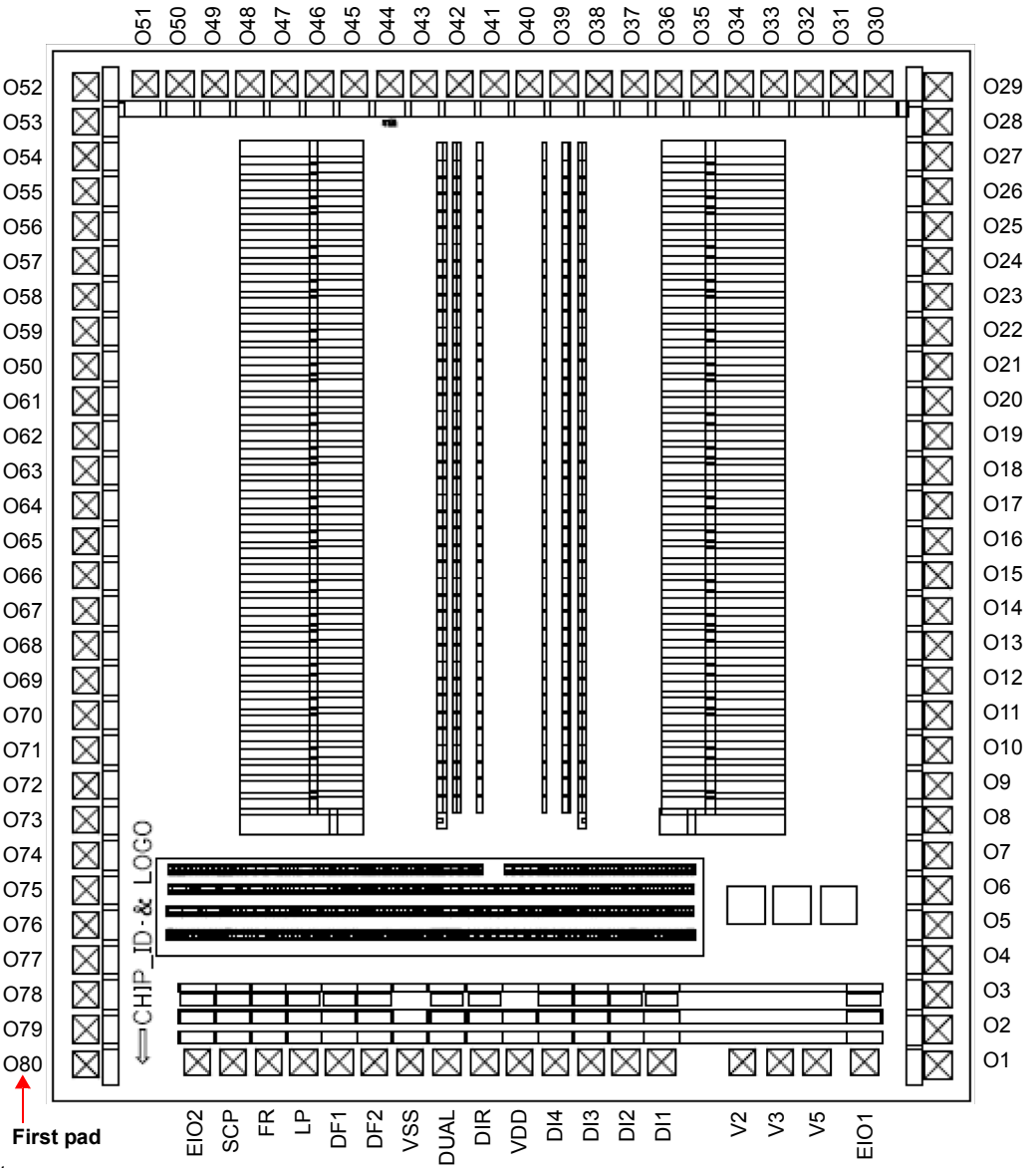
Table 2 Pin signal description.

To avoid a latch-up effect at power-on: $V_{SS} - 0.5\ V <$ voltage at any pin at any time $< V_{DD} + 0.5\ V$.

<table>
<tr><th>Pin number</th><th>SYMBOL</th><th>I/O</th><th>DESCRIPTION</th></tr>
<tr><td>1~3,
24~100</td><td>O78~O80,
O1~O77</td><td>Output</td><td>Column (segment) driver output.
Please refer to Table 4 for output voltage level.</td></tr>
<tr><td>4, 21</td><td>EIO1, EIO2</td><td>I/O</td><td>ENABLE input/output for cascading application.
The functionality of these two inputs are decided by DUAL and DIR, as shown in the following table.
<table>
<tr><th>DUAL</th><th>DIR</th><th>EIO1</th><th>EIO2</th></tr>
<tr><td>L</td><td>L</td><td>input</td><td>output</td></tr>
<tr><td>L</td><td>H</td><td>output</td><td>input</td></tr>
<tr><td>H</td><td>don’t care</td><td>input</td><td>output</td></tr>
</table></td></tr>
<tr><td>5</td><td>SCP</td><td>Input</td><td>Input data shift clock, for shifting bit data.</td></tr>
<tr><td>6</td><td>FR</td><td>Input</td><td>Frame signal, indicating a display frame.
This signal is used to generate alternating LCD bias voltage.</td></tr>
<tr><td>7</td><td>LP</td><td>Input</td><td>Line pulse, used as latch clock for internal 80-bit shift register.</td></tr>
<tr><td>8, 9</td><td>DF1, DF2</td><td>Input</td><td>Data Format selection.
These two inputs are used to select bit number of data transfer between a controller (such as the SAP1024B, for example) and the SEN6A39. The data transfer can be 1-bit, 2-bit, or 4-bit, as shown in the following table.
<table>
<tr><th>DF1</th><th>DF2</th><th>BITS</th></tr>
<tr><td>L</td><td>L</td><td>1-bit</td></tr>
<tr><td>H</td><td>L</td><td>2-bit</td></tr>
<tr><td>don’t care</td><td>H</td><td>4-bit</td></tr>
</table></td></tr>
<tr><td>10</td><td>V_{SS}</td><td>Input</td><td>Ground terminal.</td></tr>
<tr><td>11</td><td>DUAL</td><td>Input</td><td>Selection of dual-input mode or single-input mode.</td></tr>
<tr><td>12</td><td>DIR</td><td>Input</td><td>Selecting shift direction of input data.</td></tr>
<tr><td>13</td><td>V_{DD}</td><td>input</td><td>Positive power supply for control logic.</td></tr>
<tr><td>14~17</td><td>DI4 ~ DI1</td><td>Input</td><td>4-bit parallel data bus for display data.</td></tr>
<tr><td>18,19,
20</td><td>V2, V3, V5</td><td>Input</td><td>External LCD bias voltage.</td></tr>
<tr><td>22, 23</td><td>NC</td><td></td><td>No Connection.
Leave these two pins unconnected in application.</td></tr>
</table>

4 PAD DIAGRAM AND COORDINATES

4.1 Pad diagram



Note:

1. For chip_on_board (COB) bonding, chip carrier should be connected to VDD or left open. Chip carrier is the metal pad to which die is attached.
2. The chip size is : (X-axis, Y-axis)= 2786 μm x 3184 μm.
3. The Chip ID is: 3006.

Fig.3 Pad locations.

4.2 Pad description

Table 3 Pad signal names and coordinates

The unit for coordinates is μm.

PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES	
		X	Y			X	Y			X	Y
1	O80	98.70	108.60	35	O46	800.10	3055.90	69	O12	2657.5	1263.60
2	O79	98.70	213.60	36	O45	905.10	3055.90	70	O11	2657.5	1158.60
3	O78	98.70	318.60	37	O44	1010.10	3055.90	71	O10	2657.5	1053.60
4	O77	98.70	423.60	38	O43	1115.10	3055.90	72	O9	2657.5	948.60
5	O76	98.70	528.60	39	O42	1220.10	3055.90	73	O8	2657.5	843.60
6	O75	98.70	633.60	40	O41	1325.10	3055.90	74	O7	2657.5	738.60
7	O74	98.70	738.60	41	O40	1430.10	3055.90	75	O6	2657.5	633.60
8	O73	98.70	843.60	42	O39	1535.10	3055.90	76	O5	2657.5	528.60
9	O72	98.70	948.60	43	O38	1640.10	3055.90	77	O4	2657.5	423.60
10	O71	98.70	1053.60	44	O37	1745.10	3055.90	78	O3	2657.5	318.6
11	O70	98.70	1158.60	45	O36	1850.10	3055.90	79	O2	2657.5	213.60
12	O69	98.70	1263.60	46	O35	1955.10	3055.90	80	O1	2657.5	107.50
13	O68	98.70	1368.60	47	O34	2060.10	3055.90	81	EIO1	2436.0	117.10
14	O67	98.70	1473.60	48	O33	2165.10	3055.90	82	V5	2293.0	117.10
15	O66	98.70	1578.60	49	O32	2270.10	3055.90	83	V3	2183.6	117.10
16	O65	98.70	1683.60	50	O31	2375.10	3055.90	84	V2	2071.0	117.10
17	O64	98.70	1788.60	51	O30	2480.10	3055.90	85	DI1	1827.3	117.10
18	O63	98.70	1893.60	52	O29	2657.5	3048.60	86	DI2	1721.0	117.10
19	O62	98.70	1998.60	53	O28	2657.5	2943.60	87	DI3	1614.7	117.10
20	O61	98.70	2103.60	54	O27	2657.5	2838.60	88	DI4	1058.4	117.10
21	O60	98.70	2208.60	55	O26	2657.5	2733.60	89	VDD	1402.0	117.10
22	O59	98.70	2313.60	56	O25	2657.5	2628.60	90	DIR	1295.8	117.10
23	O58	98.70	2418.60	57	O24	2657.5	2523.60	91	DUAL	1182.5	117.10
24	O57	98.70	2523.60	58	O23	2657.5	2418.60	92	VSS	1071.5	117.10
25	O56	98.70	2628.60	59	O22	2657.5	2313.60	93	DF2	965.2	117.10
26	O55	98.70	2733.60	60	O21	2657.5	2208.60	94	DF1	858.80	117.10
27	O54	98.70	2838.60	61	O20	2657.5	2103.60	95	LP	752.6	117.10
28	O53	98.70	2943.60	62	O19	2657.5	1998.60	96	FR	646.3	117.10
29	O52	98.70	3048.60	63	O18	2657.5	1893.60	97	SCP	540.0	117.10
30	O51	275.10	3055.90	64	O17	2657.5	1788.60	98	EIO2	433.7	117.10
31	O50	380.10	3055.90	65	O16	2657.5	1683.60				
32	O49	485.10	3055.90	66	O15	2657.5	1578.60				
33	O48	590.10	3055.90	67	O14	2657.5	1473.60				
34	O47	695.10	3055.90	68	O13	2657.5	1368.60				

5 FUNCTIONAL DESCRIPTION

5.1 Segment output drive (O1~O80)

The voltage level of the outputs O1~O80 is determined by Input data (display data) and FR (frame signal), as given in the following table.

Table 4 output voltage level of O1~O80

FR	Data	SEN6A39 O1~O80 outputs	SEN6A40 O1~O68 outputs
L	L	V2	V1
L	H	VDD	V5
H	L	V3	V4
H	H	V5	VDD

5.2 Display Data Inputs (DI1~DI4)

The SEN6A39 has a 4-bit parallel data bus (DI1~DI4) to interface with a controller. A logic HIGH bit represents an ON cell (black pixel on the LCD screen).

Table 5 Data bits

Display data	**LCD drive output**	**LCD display**
H	Selected level (VDD, V5)	ON
L	Unselected level (V2, V3)	OFF

5.3 Data input format

Data input format is given in the following table.

DF1	DF2	DUAL	DIR	bits	Data input				Data format			
					DI1	DI2	DI3	DI4	DI1	DI2	DI3	DI4
L	L	L	L	1-bit				IN				O80,O79,...O2,O1
L	L	L	H		IN				O1,O2,...O79,O80			
L	L	H	L					IN				O80,O79...O42,O41
L	L	H	H		IN			IN	O1,O2,...O39,O40			O80,O79,...O42,O41
H	L	L	L	2-bits			IN	IN			O79,O77,...O3,O1	O80,O78,...O4,O2
H	L	L	H		IN	IN			O1,O3,...O77,O79	O2,O4,...O78,O80		
H	L	H	L				IN	IN			O79,O77,...O43,O41	O80,O78,...O44,O42
H	L	H	H		IN	IN	IN	IN	O1,O3,...O37,O39	O2,O4,...O38,O40	O79,O77,...O43,O41	O80,O78,...O44,O42
*	H	L	L	4-bits	IN	IN	IN	IN	O77,O73,...O5,O1	O78,O74,...O6,O2	O79,O75,...O7,O3	O80,O76,...O8,O4
*	H	L	H		IN	IN	IN	IN	O1,O5,...O73,O77	O2,O6,...O74,O78	O3,O7,...O75,O79	O4,O8,...O76,O80
*	H	H	L		IN	IN	IN	IN	O77,O73,...O45,O41	O78,O74,...O46,O42	O79,O75...O47,O43	O80,O76...O48,O44
*	H	H	H	don't use								

Note:

1. When DF1=DF2=DUAL=DIR="L", 1-bit data transfer between the SEN6A39 and controller is selected, DI4 is used as input, and the first bit sent by the controller goes to O1; the last bit goes to O80.
2. When DF1=DF2=DUAL="L" and DIR="H", 1-bit data transfer between the SEN6A39 and controller is selected, DI1 is used as input, and the first bit sent by the controller goes to O80; the last bit goes to O1.

6 ABSOLUTE MAXIMUM RATING

Table 6 Absolute maximum rating

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25±2°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Voltage on the V_{DD} input	−0.3	+7.0	V
V_{DD}-V5	LCD bias voltage, note 1	0	30	V
Vi(max)	Maximum input voltage to input pins	-0.3	V_{DD} + 0.3	V
T_{amb}	Operating ambient temperature range	-20	+ 75	°C
T_{stg}	Storage temperature range	−55	+125	°C

Note:

1. The condition $V_{DD} \geq V2 > V3 > V5$ must always be met.

7 DC CHARACTERISTICS

Table 7 DC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage for control logic	Please refer to Fig. 8 for DC power-up sequence.	2.7	5.0	5.5	V
V_{DD}-V5	LCD bias voltage	Note 1.	12		30	
V_{IL}	Input LOW voltage of input pins	DI1~DI4, SCP, DIR, EIO1, EIO2, LP, FR, DUAL, DF1, DF2	0		$0.2V_{DD}$	V
V_{IH}	Inout HIGH voltage of input pins	DI1~DI4, SCP, DIR, EIO1, EIO2, LP, FR, DUAL, DF1, DF2	$0.8V_{DD}$		V_{DD}	V
I_{IL}	Input LOW leakage current of input pins (i. e. Reverse leakage current of input ESD protection diode)	V_{IN}=V_{SS}, DI1~DI4, SCP, DIR, EIO1, EIO2, LP, FR, DUAL, DF1, DF2			1	μA
I_{IH}	Input HIGH leakage current of input pins (i. e. Reverse leakage current of input protection diode)	V_{IN}=V_{DD}, DI1~DI4, SCP, DIR, EIO1, EIO2, LP, FR, DUAL, DF1, DF2			1	μA
V_{OL}	Output LOW voltage level of the EIO1 and EIO2 pins	I_{OL}=400μA	0.0		0.4	V
V_{OH}	Output HIGH voltage level of the EIO1 and EIO2 pins	I_{OH}=-400μA	V_{DD} – 0.4		V_{DD}	V
I_{STBY}	Standby current	Note 2.			200	μA
I_{SS}	Operating current	Note 3.			4.0	mA
I_{EE}	Operating current	Note 4.			0.5	mA
Ci	Input capacitance of the SCP pin	The SCP clock frequency is 6.0 MHz.		5.0		pF
R_{ON1}	Driver ON resistance at V_{LCD}= 30 V	Note 5.		1.5	3.0	KΩ
R_{ON2}	Driver ON resistance at V_{LCD}= 20 V	Note 5.		2.0	3.5	KΩ

Notes:

1. The condition $V_{DD} \geq V2 > V3 > V5$ must always be met.
2. EIO1=EIO2=V_{DD}, V_{DD}-V5=30 V, SCP=6.0MHz, Output unloaded; measured at the V_{SS} pin.
3. Condition for the measurement: V_{LCD}=V_{DD}-V5=30 V, SCP=6.0 MHz, LP=14 KHz, FR=35 Hz. This is the current flowing from V_{DD} to V_{SS}, measured at the V_{SS} pin.
4. Condition for the measurement: V_{LCD}=V_{DD}-V5=30 V, SCP=6.0 MHz, LP=14 KHz, FR=35 Hz. This is the current flowing from V_{DD} to V5, measured at the V5 pin.
5. Condition for the measurment: V_{DD}-V5=30 V, $|V_{DE}-V_O|$=0.5 V, where V_{DE}= one of V_{DD}, V2, V3, or V5. V2=V_{DD} - (2/9) x (V_{DD}-V5), V3=V_{DD} - (7/9) x (V_{DD}-V5). For the driver circuits (O1~O80), please refer to Section 11 Pin Circuits.

8 AC CHARACTERISTICS

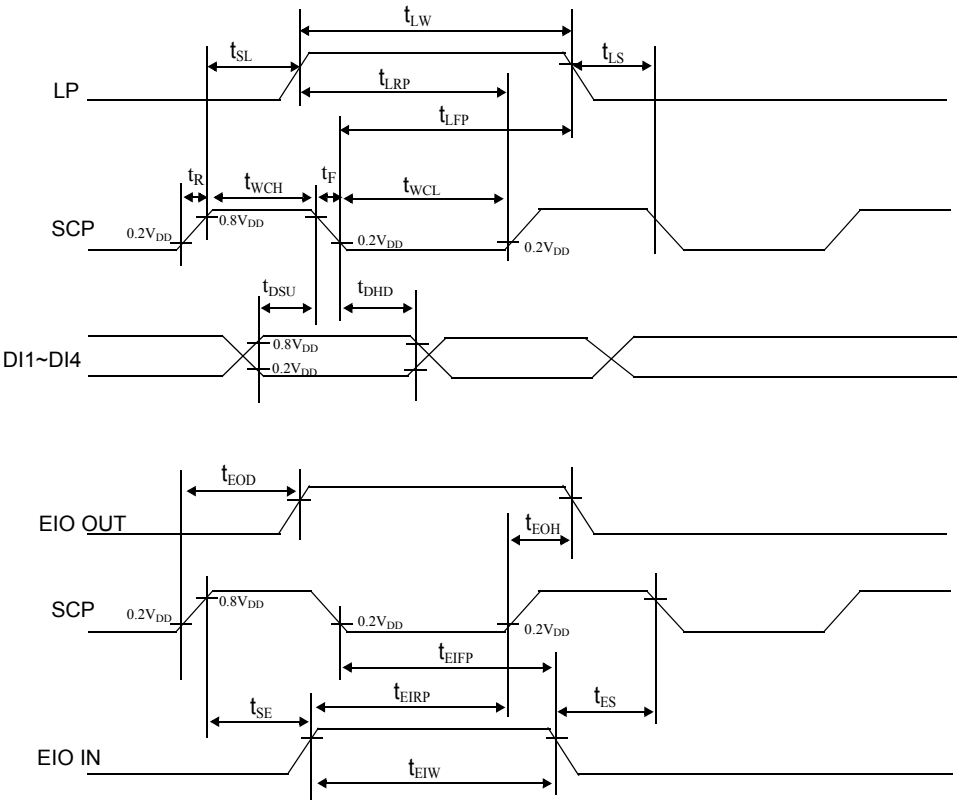


Fig.4 AC characteristics

Table 8 AC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25 ±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SCP}	SCP clock frequency			6.0	MHz
T_{WCL}	SCP clock LOW pulse width		50		ns
T_{WCH}	SCP clock HIGH pulse width		50		ns
T_r, T_f	SCP clock rising/falling time			30	30
t_{DSU}	Input data setup time	DI1~DI4 data to the falling edge of the CP clock.	20		ns
t_{DHD}	Input data hold time.	Falling edge of the CP clock to DI1~DI4 data change.	30		ns
t_{SL}	SCP-rising-edge-to-LP-rising-edge		10		ns
t_{LW}	LP pulse width		40		ns
t_{LS}	LP-falling-edge-to-SCP-falling-edge		10		ns
t_{LRP}	LP set-up time		20		ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{LFP}	LP hold time		40		ns
t_{EIRP}	EIO IN set-up time		20		ns
t_{EIFP}	EIO IN hold time		40		ns
t_{EIW}	EIO IN pulse width		40		ns
t_{SE}	SCP-rising-edge-to-EIO-rising-edge	the EIO pin, load= 10 pF.	10		ns
t_{ES}	Output delay time	the EIO pin, load= 10 pF.	10		ns
t_{EOD}	EIO OUT data delay time			100	ns
t_{EOH}	EIO OUT hols time			95	ns

9 TIMING CHART (1/240 DUTY) AND BIAS CIRCUIT

9.1 1/240 duty timing chart

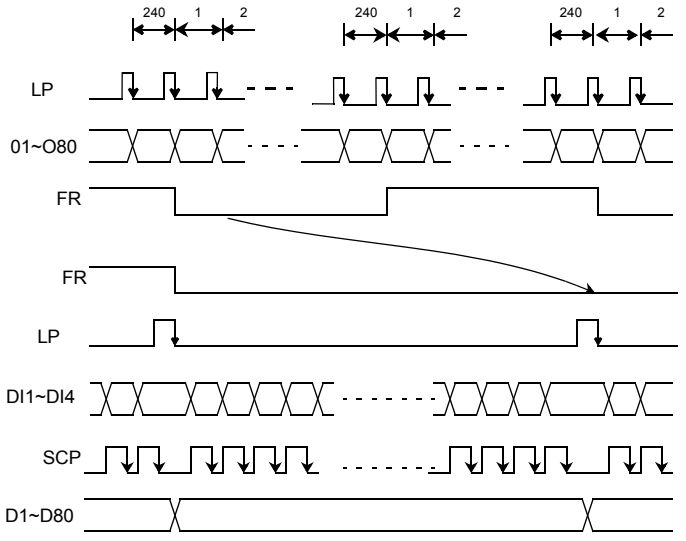
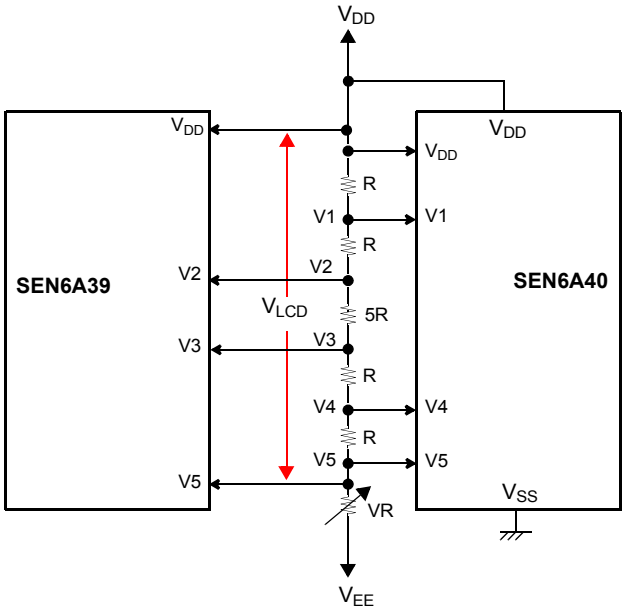


Fig.5 1/240 duty timing chart

9.2 Bias circuit



$V_{LCD}=V_{DD}-V5$

$V1 = V_{DD} - (1/9)\ V_{LCD}$

$V2 = V_{DD} - (2/9)\ V_{LCD}$

$V3 = V_{DD} - (7/9)\ V_{LCD}$

$V4 = V_{DD} - (8/9)\ V_{LCD}$

$V5 = V_{DD} - (9/9)\ V_{LCD}$

Fig.6 LCD bias voltage

10 APPLICATION CIRCUIT (64 X 160 DOTS)

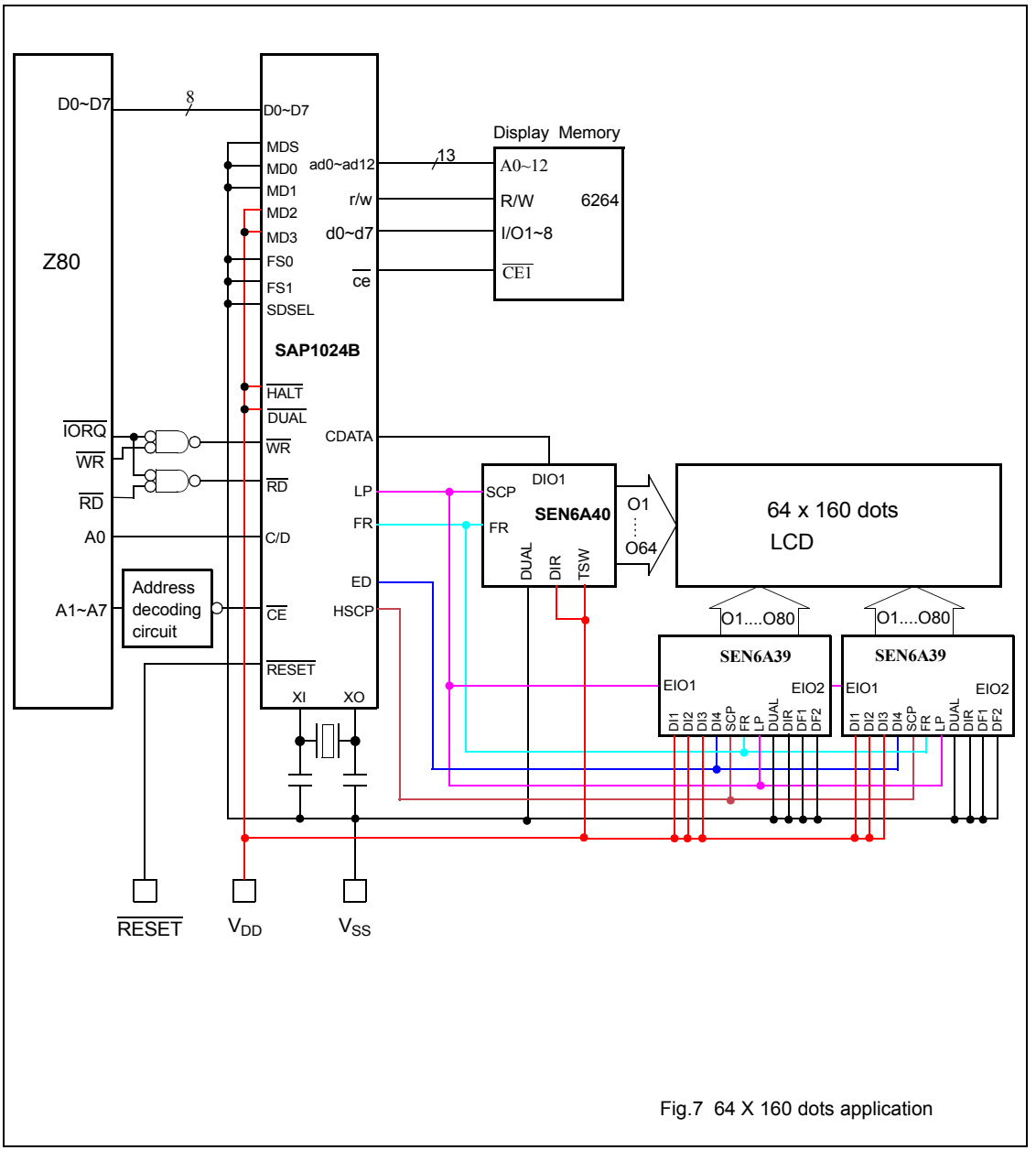
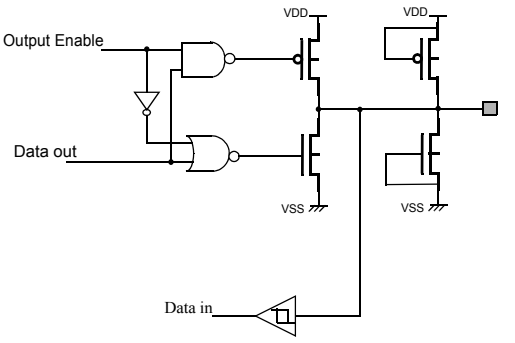
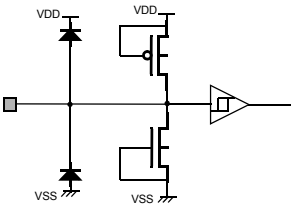
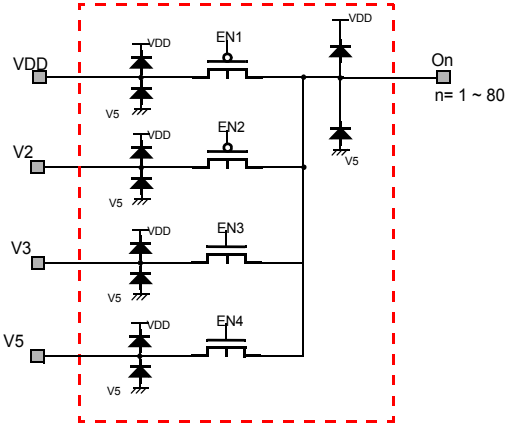


Fig.7 64 X 160 dots application

11 PIN CIRCUITS

Table 9 MOS-level schematics of all input, output, and I/O pins.

SYMBOL	Input/ output	CIRCUIT	NOTES
EIO1, EIO2	I/O		
SCP, DIR, LP, DI1~DI4, FR	Inputs		
O1~O80, VDD, V2, V3, V5	Driver outputs, High voltage inputs		

12 APPLICATION NOTES

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias (V5).

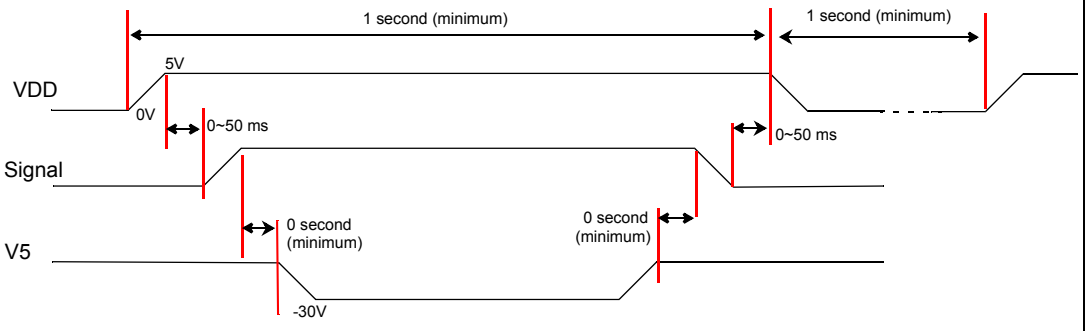
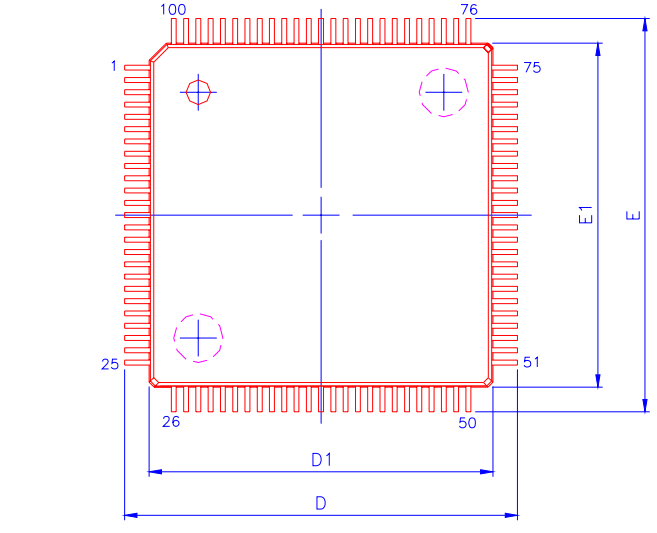
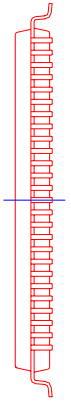


Fig.8 Recommended power up/down sequence

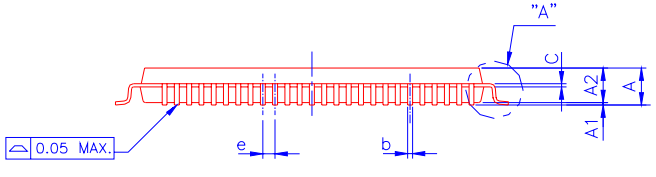
13 PACKAGE INFORMATION

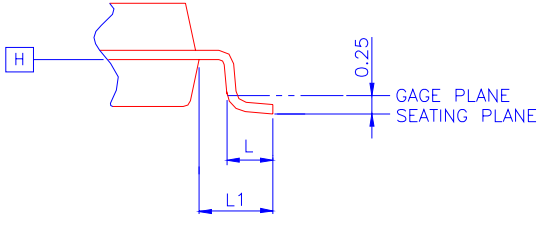




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		





DETAIL A

NOTES:

1. JEDEC OUTLINE:MS-026 BED
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

SEN6A39
LQFP100 Package Outline Drawing

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

14.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 LIFE SUPPORT APPLICATIONS

This product is not designed for use in life support appliances, devices, or systems, where malfunction of this product can reasonably be expected to result in personal injury. Avant customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.