EPL43102

43 Com / 102 Seg LCD Driver

Product Specification

DOC. VERSION 1.9

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2000/11/20
0.2	Added 1/3 and 1/3.5 bias	2001/02/15
0.3	1. Added one more VDD and VSS pad. 2. Modified the Pad sequence and configuration.	2001/03/02
0.4	Modified the DC and AC characteristics.	2001/07/17
0.5	1. Added pin configuration 2. Added program example 3. Modified the DC characteristics	2001/07/25
1.1	Modified the operating temperature range from –30 to 80°C	2001/09/07
1.2	Added COG package	2003/01/06
1.3	Added TEST pin description	2003/04/25
1.4	Modified the reading timing of /WR	2003/08/04
1.5	Adjusted the Data RAM arrangement	2003/12/29
1.6	1. Modified the table on the relationship between duty ratio and common output 2. Modified the A0 voltage level of Display ON/OFF instruction	2004/02/27
1.7	1. Added a Note on the M/S description under System Control section. 2. Modified the table for Common and Segment Driver Circuits.	2004/08/18
1.8	1. Modified the COG part no. to EPL43102GH 2. Modified the TEST pin description	2006/01/20
1.9	Added Tray information	2006/04/13

1 General Description

The EPL43102 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It can be interfaced with the MPU via serial or 8-bit interface. It contains 43 common and 102 segment driver circuits. With one chip, it is possible to drive a graphic display system with a maximum of 102 × 43 dots.

2 Features

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM : 102 × 43 = 4386 bits
- 145 LCD Drivers : 102-seg segment drivers, 42-common drivers and 1-icon
- Serial Interface (SPI) or 8-Bit Parallel Interface Mode (80-series, 68-series MPU)
- On-chip oscillator circuit
- Multi-chip operation (Master, Slave) available
- Programmable Duty Ratio :

Duty Ratio	Common	Segment
1: 42 (+ ICON)	42 (+ ICON)	102
1: 36 (+ ICON)	36 (+ ICON)	102
1: 32 (+ ICON)	32 (+ ICON)	102
1: 24 (+ ICON)	24 (+ ICON)	102
1: 16 (+ ICON)	16 (+ ICON)	102
1: 8 (+ ICON)	8 (+ ICON)	102

Note: ICON = "0" : Pin disable
ICON = "1" : Pin enable

- Selectable LCD driving bias level:
  1/3, 1/3.5, 1/4, 1/4.5, 1/5, 1/5.5, 1/6, 1/6.5, 1/7, 1/7.5, 1/8 bias
- Selectable LCD display clock frequency
- Electronic contrast control functions (64 steps)
- Built-in Instruction Set: Display data read/write, Display on/off, Inverse display, Page address set, Common address set, LCD display contrast control, Set Sleep mode, Standby mode, etc.
- Operating Voltage range:
  Supply voltage: 2.2 to 5.5 V
  LCD driving voltage: 4.0 to 15.0 V

Package (Ordering information)**:**

Part Number	Package	Description	Package Information
EPL43102H	Bare die	NA	Page 2
EPL43102GH	Gold bumped die	NA	Page 2

Note: The EPL43102 series has the following sub-codes, depending on their shapes.
H: Bare chip (Aluminum pad without bump); **GH**: Gold bumped chip
F: COF package; **T**: TAB (TCP) package

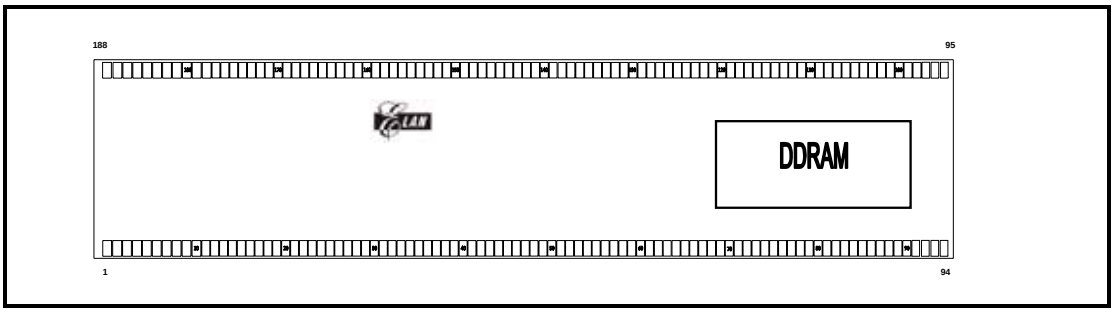
Example:

EPL43102AGH → **EPL43102:** Elan number;
A: Package Version;
GH: Gold bumped chip

3 Applications

Organizer
Electronic Dictionary
Scientific calculator
Cellular phone
Graphic pager
Handy Terminals (PDA)

4 Pin Assignment



Note: *With the Elan logo at the center (as shown in the figure) and DDRAM (black color) on the right side, Pin 1 is at the bottom left corner.*

Figure 4-1 Pin Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	8440	1790	μm
Pad Pitch	1~15, 80~94 95~109,174~188	95		
	16~79 110~173	85		
Pad Size (EPL43102H) Al pad	1~15, 80~94 95~109,174~188	85	150	
	16~79 110~173	75	150	
Bump Size (EPL43102GH) Au pad	1~15, 80~94 95~109,174~188	82	147	
	16~79 110~173	72	147	
Die thickness	525 ± 25			
Bump Height	All Pad 17 ± 3 (within die)			
Minimum Bump Gap	13			
Coordinate Origin	Die center			

4.1 Pad Coordinates

Pad No.	Symbol	X	Y
1	COM21	-4095.0	-742.5
2	COM22	-4000.0	-742.5
3	COM23	-3905.0	-742.5
4	COM24	-3810.0	-742.5
5	COM25	-3715.0	-742.5
6	COM26	-3620.0	-742.5
7	COM27	-3525.0	-742.5
8	COM28	-3430.0	-742.5
9	COM29	-3335.0	-742.5
10	COM30	-3240.0	-742.5
11	COM31	-3145.0	-742.5
12	COM32	-3050.0	-742.5
13	COM33	-2955.0	-742.5
14	COM34	-2860.0	-742.5
15	COM35	-2765.0	-742.5
16	COM36	-2675.0	-742.5
17	COM37	-2590.0	-742.5
18	COM38	-2505.0	-742.5
19	COM39	-2420.0	-742.5
20	COM40	-2335.0	-742.5
21	COM41	-2250.0	-742.5
22	COMI1	-2165.0	-742.5
23	VDD	-2080.0	-742.5
24	VDD	-1995.0	-742.5
25	C1+	-1910.0	-742.5
26	C1-	-1825.0	-742.5
27	C3	-1740.0	-742.5
28	C4	-1655.0	-742.5
29	C2-	-1570.0	-742.5
30	C2+	-1485.0	-742.5
31	VOUT	-1400.0	-742.5
32	V0	-1315.0	-742.5
33	V1	-1230.0	-742.5
34	V2	-1145.0	-742.5
35	V3	-1060.0	-742.5
36	V4	-975.0	-742.5
37	VR	-890.0	-742.5
38	GND	-805.0	-742.5
39	GND	-720.0	-742.5
40	MS	-635.0	-742.5
41	PS	-550.0	-742.5
42	FR	-465.0	-742.5
43	C86	-380.0	-742.5
44	/DOF	-295.0	-742.5
45	CLS	-210.0	-742.5
46	CL	-125.0	-742.5
47	OSC	-40.0	-742.5
48	FRS	45.0	-742.5
49	IRS	130.0	-742.5
50	/RES	215.0	-742.5

Pad No.	Symbol	X	Y
51	D7	300.0	-742.5
52	D6	385.0	-742.5
53	D5	470.0	-742.5
54	D4	555.0	-742.5
55	D3	640.0	-742.5
56	D2	725.0	-742.5
57	D1	810.0	-742.5
58	D0	895.0	-742.5
59	CS2	980.0	-742.5
60	/CS1	1065.0	-742.5
61	A0	1150.0	-742.5
62	/WR	1235.0	-742.5
63	/RD	1320.0	-742.5
64	TEST	1405.0	-742.5
65	COM20	1490.0	-742.5
66	COM19	1575.0	-742.5
67	COM18	1660.0	-742.5
68	COM17	1745.0	-742.5
69	COM16	1830.0	-742.5
70	COM15	1915.0	-742.5
71	COM14	2000.0	-742.5
72	COM13	2085.0	-742.5
73	COM12	2170.0	-742.5
74	COM11	2255.0	-742.5
75	COM10	2340.0	-742.5
76	COM9	2425.0	-742.5
77	COM8	2510.0	-742.5
78	COM7	2595.0	-742.5
79	COM6	2680.0	-742.5
80	COM5	2770.0	-742.5
81	COM4	2865.0	-742.5
82	COM3	2960.0	-742.5
83	COM2	3055.0	-742.5
84	COM1	3150.0	-742.5
85	COM0	3245.0	-742.5
86	COMI2	3340.0	-742.5
87	SEG101	3435.0	-742.5
88	SEG100	3530.0	-742.5
89	SEG99	3625.0	-742.5
90	SEG98	3720.0	-742.5
91	SEG97	3815.0	-742.5
92	SEG96	3910.0	-742.5
93	SEG95	4005.0	-742.5
94	SEG94	4100.0	-742.5
95	SEG93	4100.0	742.5
96	SEG92	4005.0	742.5
97	SEG91	3910.0	742.5
98	SEG90	3815.0	742.5
99	SEG89	3720.0	742.5
100	SEG88	3625.0	742.5

Pad No.	Symbol	X	Y
101	SEG87	3530.0	742.5
102	SEG86	3435.0	742.5
103	SEG85	3340.0	742.5
104	SEG84	3245.0	742.5
105	SEG83	3150.0	742.5
106	SEG82	3055.0	742.5
107	SEG81	2960.0	742.5
108	SEG80	2865.0	742.5
109	SEG79	2770.0	742.5
110	SEG78	2680.0	742.5
111	SEG77	2595.0	742.5
112	SEG76	2510.0	742.5
113	SEG75	2425.0	742.5
114	SEG74	2340.0	742.5
115	SEG73	2255.0	742.5
116	SEG72	2170.0	742.5
117	SEG71	2085.0	742.5
118	SEG70	2000.0	742.5
119	SEG69	1915.0	742.5
120	SEG68	1830.0	742.5
121	SEG67	1745.0	742.5
122	SEG66	1660.0	742.5
123	SEG65	1575.0	742.5
124	SEG64	1490.0	742.5
125	SEG63	1405.0	742.5
126	SEG62	1320.0	742.5
127	SEG61	1235.0	742.5
128	SEG60	1150.0	742.5
129	SEG59	1065.0	742.5
130	SEG58	980.0	742.5
131	SEG57	895.0	742.5
132	SEG56	810.0	742.5
133	SEG55	725.0	742.5
134	SEG54	640.0	742.5
135	SEG53	555.0	742.5
136	SEG52	470.0	742.5
137	SEG51	385.0	742.5
138	SEG57	895.0	742.5
139	SEG49	215.0	742.5
140	SEG48	130.0	742.5
141	SEG47	45.0	742.5
142	SEG46	-40.0	742.5
143	SEG45	-125.0	742.5
144	SEG44	-210.0	742.5
145	SEG43	-295.0	742.5
146	SEG42	-380.0	742.5
147	SEG41	-465.0	742.5
148	SEG40	-550.0	742.5
149	SEG39	-635.0	742.5
150	SEG38	-720.0	742.5

Pad No.	Symbol	X	Y
151	SEG37	-805.0	742.5
152	SEG36	-890.0	742.5
153	SEG35	-975.0	742.5
154	SEG34	-1060.0	742.5
155	SEG33	-1145.0	742.5
156	SEG32	-1230.0	742.5
157	SEG31	-1315.0	742.5
158	SEG30	-1400.0	742.5
159	SEG29	-1485.0	742.5
160	SEG28	-1570.0	742.5
161	SEG27	-1655.0	742.5
162	SEG26	-1740.0	742.5
163	SEG25	-1825.0	742.5
164	SEG24	-1910.0	742.5
165	SEG23	-1995.0	742.5
166	SEG22	-2080.0	742.5
167	SEG21	-2165.0	742.5
168	SEG20	-2250.0	742.5
169	SEG19	-2335.0	742.5
170	SEG18	-2420.0	742.5
171	SEG17	-2505.0	742.5
172	SEG16	-2590.0	742.5
173	SEG15	-2675.0	742.5
174	SEG14	-2765.0	742.5
175	SEG13	-2860.0	742.5
176	SEG12	-2955.0	742.5
177	SEG11	-3050.0	742.5
178	SEG10	-3145.0	742.5
179	SEG9	-3240.0	742.5
180	SEG8	-3335.0	742.5
181	SEG7	-3430.0	742.5
182	SEG6	-3525.0	742.5
183	SEG5	-3620.0	742.5
184	SEG4	-3715.0	742.5
185	SEG3	-3810.0	742.5
186	SEG2	-3905.0	742.5
187	SEG1	-4000.0	742.5
188	SEG0	-4095.0	742.5

Note: For PCB layout, the IC substrate must be connected to VSS or floating.
Refer to the correlation between Duty Ratio and Common Output (Section 7.3.2).

5 Block Diagram

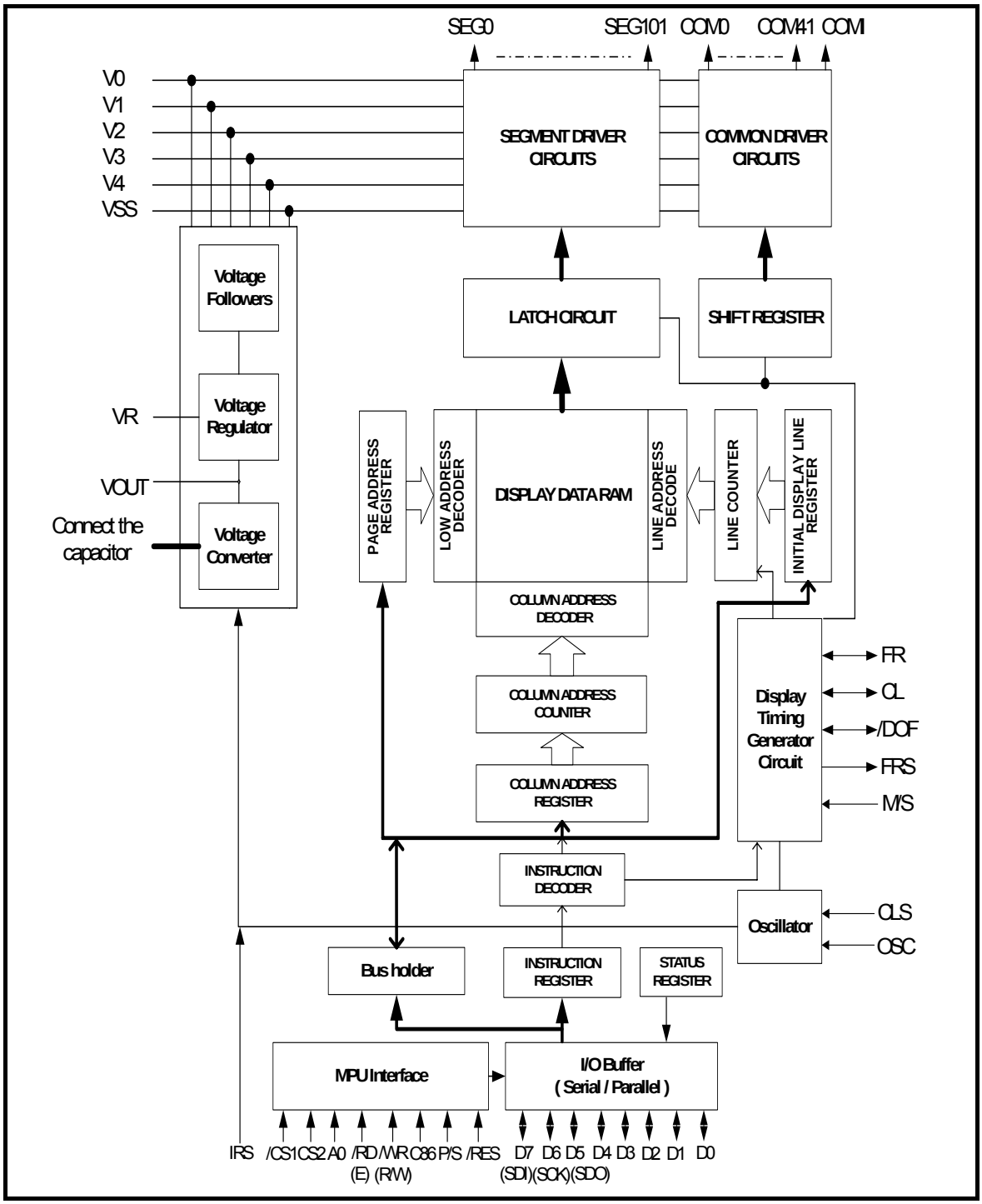


Figure 5-1 System Block Diagram

6 Pin Description

6.1 Power Supply

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Power</td><td>VDD Power Supply</td></tr>
<tr><td>VSS</td><td>Power</td><td>0V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>Power</td><td>LCD driver supply voltages. The voltage applied is determined by the LCD pixel and is changed by changing the impedance using an operational amplifier (OPA) for various applications. Voltage levels are determined based on V0, and must maintain the relative magnitudes shown below:
V0≧V1≧V2≧V3≧V4≧Vss
When the internal power circuit is active, these voltages are generated according to the state of the LCD bias. The selection of voltages is determined by the “LCD bias select” instruction, as shown in the table below.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/8 Bias</td><td>(7/8) × V0</td><td>(6/8) × V0</td><td>(2/8) × V0</td><td>(1/8) × V0</td></tr>
<tr><td>1/7.5 Bias</td><td>(6.5/7.5) × V0</td><td>(5.5/7.5) × V0</td><td>(2/7.5) × V0</td><td>(1/7.5) × V0</td></tr>
<tr><td>1/7 Bias</td><td>(6/7) × V0</td><td>(5/7) × V0</td><td>(2/7) × V0</td><td>(1/7) × V0</td></tr>
<tr><td>1/6.5 Bias</td><td>(5.5/6.5) × V0</td><td>(4.5/6.5) × V0</td><td>(2/6.5) × V0</td><td>(1/6.5) × V0</td></tr>
<tr><td>1/6 Bias</td><td>(5/6) × V0</td><td>(4/6) × V0</td><td>(2/6) × V0</td><td>(1/6) × V0</td></tr>
<tr><td>1/5.5 Bias</td><td>(4.5/5.5) × V0</td><td>(3.5/5.5) × V0</td><td>(2/5.5) × V0</td><td>(1/5.5) × V0</td></tr>
<tr><td>1/5 Bias</td><td>(4/5) × V0</td><td>(3/5) × V0</td><td>(2/5) × V0</td><td>(1/5) × V0</td></tr>
<tr><td>1/4.5 Bias</td><td>(3.5/4.5) × V0</td><td>(2.5/4.5) × V0</td><td>(2/4.5) × V0</td><td>(1/4.5) × V0</td></tr>
<tr><td>1/4 Bias</td><td>(3/4) × V0</td><td>(2/4) × V0</td><td>(2/4) × V0</td><td>(1/4) × V0</td></tr>
<tr><td>1/3.5 Bias</td><td>(2.5/3.5) × V0</td><td>(1.5/3.5) × V0</td><td>(2/3.5) × V0</td><td>(1/3.5) × V0</td></tr>
<tr><td>1/3 Bias</td><td>(2/3) × V0</td><td>(1/3) × V0</td><td>(2/3) × V0</td><td>(1/3) × V0</td></tr>
</table>
</td></tr>
</table>

6.2 LCD Driver Supply

Name	I/O	Description
C1+ C1-	O	Boosted capacitor connecting terminals used for voltage booster.
C2+ C2-	O	Boosted capacitor connecting terminals used for voltage booster.
C3 C4	O	Boosted capacitor connecting terminals used for voltage booster.
VOUT	I/O	Voltage converter output
VR	I	V0 voltage adjustment pin

6.3 System Control

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>M/S</td><td>I</td><td>Master/slave operation select pin.
- MS = "H": Master operation
- MS = "L": Slave operation
<table>
<tr><th>M/S</th><th>CLS</th><th>OSC.</th><th>Power supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>/DOF</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Available</td><td>Available</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>“L”</td><td>Unavailable</td><td>Available</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>“L”</td><td>*</td><td>Unavailable</td><td>Unavailable</td><td>I</td><td>I</td><td>Hi-Z</td><td>I</td></tr>
</table>
Note: * : Don’t Care
O : Output
I : Input</td></tr>
<tr><td>P/S</td><td>I</td><td>Select Interface mode of the MPU.
When PS = "High": Parallel interface mode
When PS = "Low": Serial interface mode</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC signal input/output pin.
When used in master/slave mode (multi-chip), the FR pins must be connected to each other.
- MS = “H”: Output
- MS = “L”: Input</td></tr>
<tr><td>C68</td><td>I</td><td>Select the kind of the MPU to interface.
When C68 = "High": 68-series MPU interface mode
When C68 = "Low": 80-series MPU interface</td></tr>
<tr><td>/DOF</td><td>I/O</td><td>LCD Display blanking control pin. In multi-chip mode, the /DOF pin must be connected to each other.
M/S = ”H” (Master) : /DOF is output pin.
→ Display “On” = “H”, Display “Off” = “L”
M/S = ”L” (Slave) : /DOF is input pin.
→ Via external control. Refer to the following table.
<table>
<tr><th rowspan="2">Instruction</th><th colspan="2">/DOF</th></tr>
<tr><th>H</th><th>L</th></tr>
<tr><td>Display “On”</td><td>On</td><td>Off</td></tr>
<tr><td>Display “Off”</td><td>Off</td><td>Off</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Internal oscillator circuit enable / disable select pin.
CLS = “H”: Enable Internal oscillator circuit
CLS = “L”: Disable Internal oscillator circuit is
(External display clock input to OSC pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
When the EPL43102 is used in master/slave mode (multi-chip), the CL pins must be connected to each other.
<table>
<tr><th>M/S</th><th>CL</th></tr>
<tr><td>“H”</td><td>Output</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
</table></td></tr>
</table>

Name	I/O	Description
OSC	I	When using an external oscillator, input the clock to the OSC pin. When using an internal oscillator, leave this pin open.
FRS	O	Static driver output pin. This pin is used in combination with the FR pin.
IRS	I	Internal resistor select pin. This pin selects the resistors for adjusting V0 voltage level and is available only in master mode. - IRS = "H": The internal resistors are used. - IRS = "L": The external resistors are used. V0 voltage is controlled using the external divider resistor connect the VR pin.
TEST	I	Test pin. Fixed at VSS.

6.4 MPU Interface

Name	I/O	Description
/RES	I	Hardware reset input. The LSI is reset when this signal is pulled low. (Active low)
/CS1, CS2	I	These are the chip select signals. The Chip Select of the LSI becomes active when CS1 is "L" and also CS2 is "H" and allows the input/output of data or commands. /CS1 / CS2 / Status "L" / "L" / The device is not active. (D7~D0 is Hi-Z) "L" / "H" / Data and instruction are available. "H" / "L" / The device is not active. (D7~D0 is Hi-Z) "H" / "H" / The device is not active. (D7~D0 is Hi-Z)
A0	I	Used as register selection input. When A0 = "High", Data register When A0 = "Low", Instruction register
/WR (R/W)	I	When C68 = "High" (68-series MPU interfacing), used as Read (/WR = "High"), Write (/WR = "Low") When C68 = "Low " (80-series MPU interfacing), used as write enable input (/WR).
/RD (E)	I	When C68 = "High" (68-series MPU interfacing), used as read/write enable input (E). When C68 = "Low " (80-series MPU interfacing), used as read enable input (/RD).
D0 to D7	I/O	When in serial mode, D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin and the others are not used. When in parallel mode, D0 to D7 are used as bidirectional data bus pin.

6.5 LCD Driver Output

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>COM0 to
COM41</td><td>O</td><td>The LCD common output pins.
<table>
<tr><th>Scan Data</th><th>FR</th><th>COMs Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Vss</td></tr>
<tr><td>L</td><td>V0</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>Vss</td></tr>
</table></td></tr>
<tr><td>COMI</td><td>O</td><td>These are two icon display pins. Both pins output the same signal.
Leave these pins open when they are not used.</td></tr>
<tr><td>SEG0 to
SEG101</td><td>O</td><td>The LCD segment output pins.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">FR</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power Save Mode</td><td colspan="2">Vss</td></tr>
</table></td></tr>
</table>

Refer to Section 7.3.2 on the correlation between Duty Ratio and Common Output.

7 Function Description

7.1 System Interface

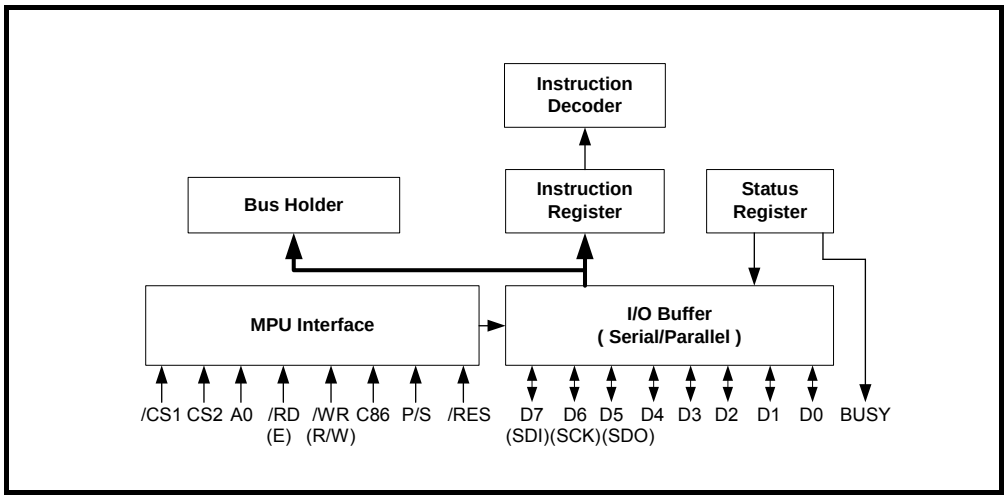


Figure 7-1 System Interface

7.2 MPU Interface

7.2.1 Chip Select

The EPL43102 has two chip select pins /CS1 and CS2. When /CS1="L" and CS2="H", MPU interface is available. When the chip select pin is inactive (other /CS1 and CS2 condition), D7 to D0 are high impedance (invalid) and input of A0, /RD, or /WR inputs are not effective. If serial interface is selected, the shift register and counter are both reset. However, reset is always operated in any conditions of /CS1 and CS2.

P/S	C68	A0	/WR	/RD	D0~D4	D5	D6	D7
Serial Mode (L)	SPI interface (-)	A0	R/W	–	*	SDO	SCK	SDI
Parallel mode (H)	80-series (L)	A0	/WR	/RD	D0~D7			
	68-series (H)	A0	R/W	E	D0~D7			

Note: " * " Don't care ("High", "Low" or "Open")

"–" Indicates that it is fixed to either "High" (VDD) or "Low" (VSS)

7.2.2 Selecting the Interface Type

The EPL43102 can be operated with serial interface (SPI) and parallel interface (80-series or 68-series) as selected by the P/S pin.

7.2.2.1 Serial Interface (SPI)

When serial mode (PS = "L"), D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin. When the LSI is active (/CS1="L", CS2="H"), serial data input (D7), serial clock input (D6) and serial data output (D5) are enabled. The 8-bit shift register and 3-bit counter are reset to the initial condition when the chip is not selected. The data input/output from SDI/SDO terminal is MSB first as in the order of D7, D6…D0, and is latched at the rising edge of the serial clock SCK. Serial input data is display data when A0="H" and instruction when A0="L". The A0 input is read and identified at the rising edge of the (8 × n) serial clock pulse. Since the clock signal (D6) is easy to be affected by the external noise caused by the line length, operation check on the actual machine is recommended.

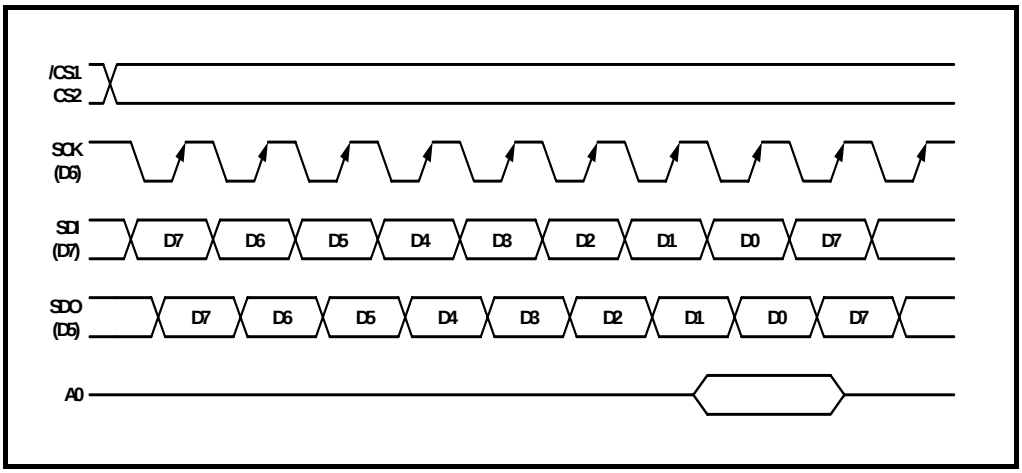


Figure 7-2 Serial Interface Signal Chart

A0	/WR (R/W)	D7 (SDI)	D5 (SDO)
0	0	Instruction Write	Status Read
0	1	Invalid	Status Read
1	0	Display Data Write	Status Read
1	1	Invalid	Display Data Read

7.2.2.2 Parallel Interface (8-bit Length)

When the parallel input is selected (PS = ”H”), D0~D7 can be connected directly to the 80-series or 68-series MPU by setting the C86 pin to high or low.

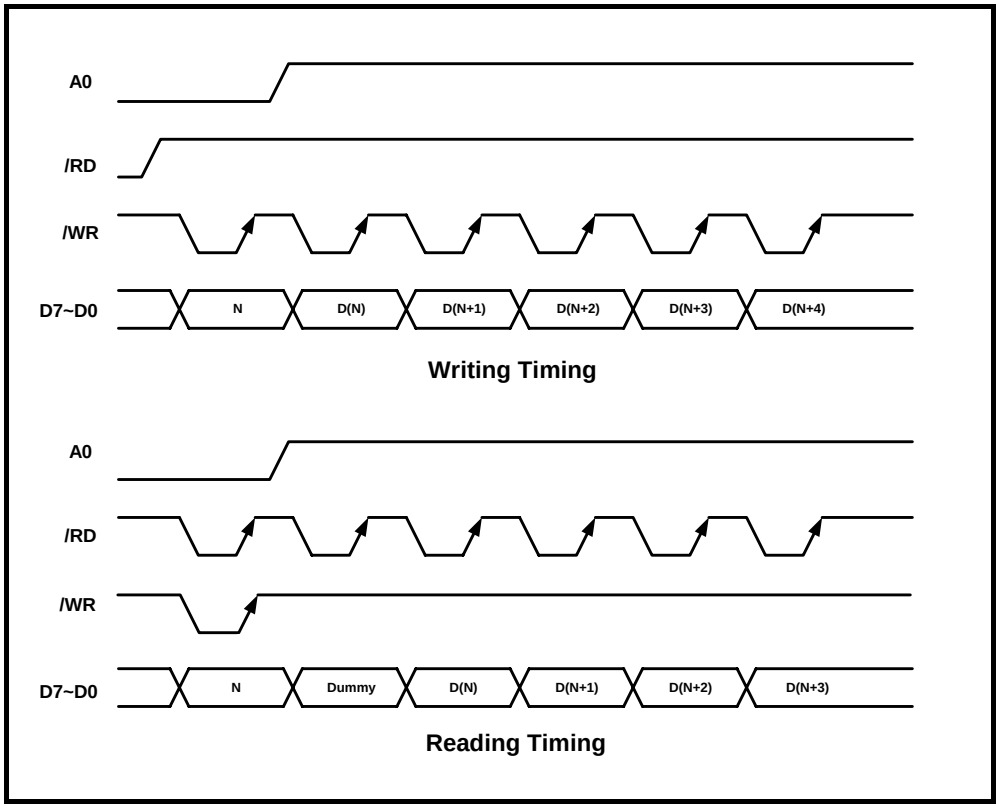


Figure 7-3 Write and Read Timing Diagrams

Common	80-series		68-series	Description
A0	/RD	/WR	R/W	
H	L	H	H	Display data read
H	H	L	L	Display data write
L	L	H	H	Register status read
L	H	L	L	Write to the Instruction register

7.3 Data Transfer

The EPL43102 uses a bus holder and an internal data bus for data transfer with MPU. When writing data from the MPU to the DDRAM, data is automatically transferred from the bus holder to the DDRAM. When reading data from the DDRAM to the MPU, data for the initial read cycle is stored in the bus holder (dummy read) and MPU reads this stored data from the bus holder for the next data read cycle.

7.3.1 Display Data RAM

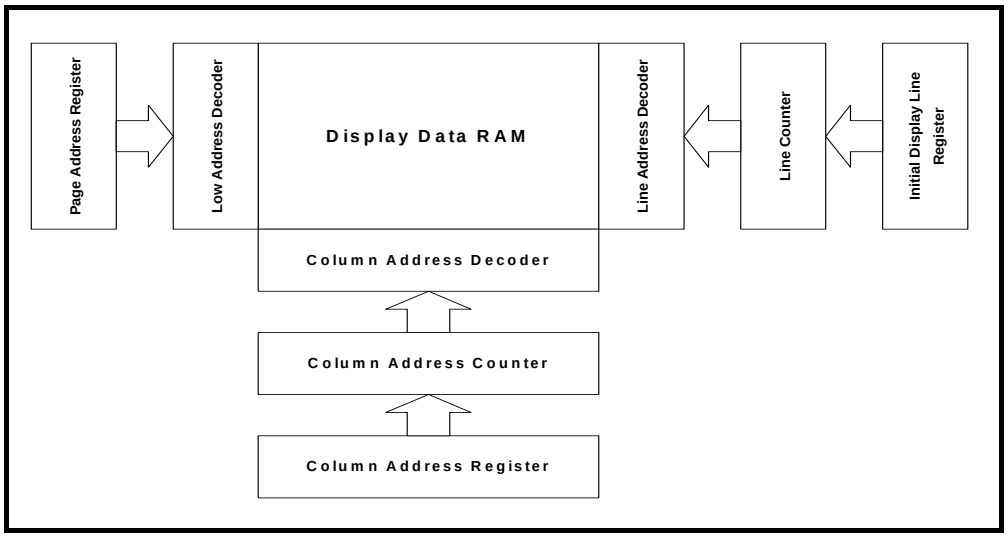


Figure 7-4 Display Data RAM Diagram

The display data RAM (DDRAM) stores pixel data for the LCD. It is a 43-row × 102-column addressable array. It is possible to access any required bit by specifying the page address and the column address. The 43 rows are divided into 5 pages of 8 lines, 1 page with 2 lines (D0, D1) and the seventh page with a single line (D0 only).

Each bit in the Display Data RAM corresponds to the each pixel of the LCD panel and controls the display by applying the following bit data.

When in Normal Display : On = "1" , Off = "0"

When in Inverse Display : On = "0" , Off = "1"

Refer to Section 8.1.3, *"Inverse Display On/Off"* instruction for more details.

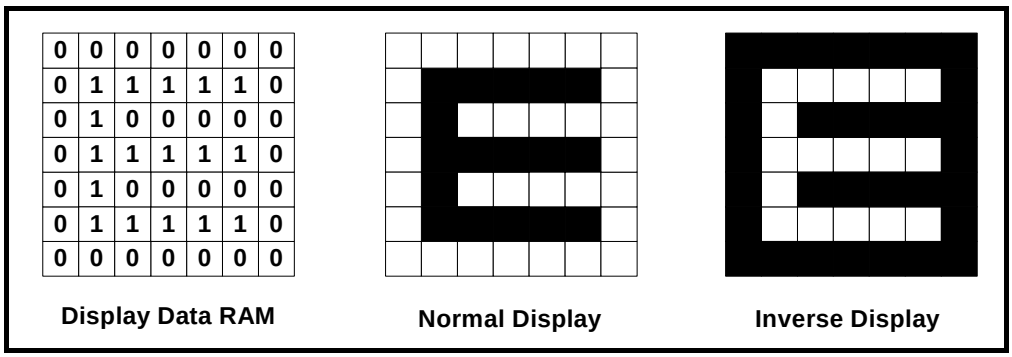


Figure 7-5 Display Data RAM, Normal and Inverse Liquid Crystal Display Diagrams

The microprocessor (MPU) can read from and write to the RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into the RAM at the same time as data is being displayed without causing the LCD to flicker.

Page Address P3,P2,P1,P0				Data	Column Address								Line Address (HEX)	Common Output (1/42,1/43)	Common Output (1/36,1/37)	Common Output (1/32,1/33)	Common Output (1/16,1/17)
0	0	0	0	D0				PAGE0					00	COM0	COM0	COM0	COM0
				D1									01	COM1	COM1	COM1	COM1
				D2									02	COM2	COM2	COM2	COM2
				D3									03	COM3	COM3	COM3	COM3
				D4									04	COM4	COM4	COM4	COM4
				D5									05	COM5	COM5	COM5	COM5
				D6									06	COM6	COM6	COM6	COM6
				D7									07	COM7	COM7	COM7	COM7
0	0	0	1	D0				PAGE1					08	COM8	COM8	COM8	COM8
				D1									09	COM9	COM9	COM9	COM9
				D2									0A	COM10	COM10	COM10	COM10
				D3									0B	COM11	COM11	COM11	COM11
				D4									0C	COM12	COM12	COM12	COM12
				D5									0D	COM13	COM13	COM13	COM13
				D6									0E	COM14	COM14	COM14	COM14
				D7									0F	COM15	COM15	COM15	COM15
0	0	1	0	D0				PAGE2					10	COM16	COM16	COM16	
				D1									11	COM17	COM17	COM17	
				D2									12	COM18	COM18	COM18	
				D3									13	COM19	COM19	COM19	
				D4									14	COM20	COM20	COM20	
				D5									15	COM21	COM21	COM21	
				D6									16	COM22	COM22	COM22	
				D7									17	COM23	COM23	COM23	
0	0	1	1	D0				PAGE3					18	COM24	COM24	COM24	
				D1									19	COM25	COM25	COM25	
				D2									1A	COM26	COM26	COM26	
				D3									1B	COM27	COM27	COM27	
				D4									1C	COM28	COM28	COM28	
				D5									1D	COM29	COM29	COM29	
				D6									1E	COM30	COM30	COM30	
				D7									1F	COM31	COM31	COM31	
0	1	0	0	D0				PAGE4					20	COM32	COM32		
				D1									21	COM33	COM33		
				D2									22	COM34	COM34		
				D3									23	COM35	COM35		
				D4									24	COM36			
				D5									25	COM37			
				D6									26	COM38			
				D7									27	COM39			

Page Address P3,P2,P1,P0				Data	Column Address								Line Address (HEX)	Common Output (1/42,1/43)	Common Output (1/36,1/37)	Common Output (1/32,1/33)	Common Output (1/16,1/17)
0	1	0	1	D0				PAGE5					28	COM40			
				D1									29	COM41			
0	1	1	0	D0				PAGE6						COMI	COMI	COMI	COMI
Column Address (HEX)				ADC =0	00	01	02	- - - - - - - - -	62	63	64	65					
				ADC =1	65	64	63	- - - - - - - - -	03	02	01	00					
LCD Output					SEG0	SEG1	SEG2	- - - - - - - - -	SEG98	SEG99	SEG100	SEG101					

7.3.2 Programmable Duty Ratio

The duty ratio is selected by using the “Set Duty Ratio” instruction.

The common output circuits are shown in the following figure. They are separated into three shift registers and controlled by the "duty ratio register".

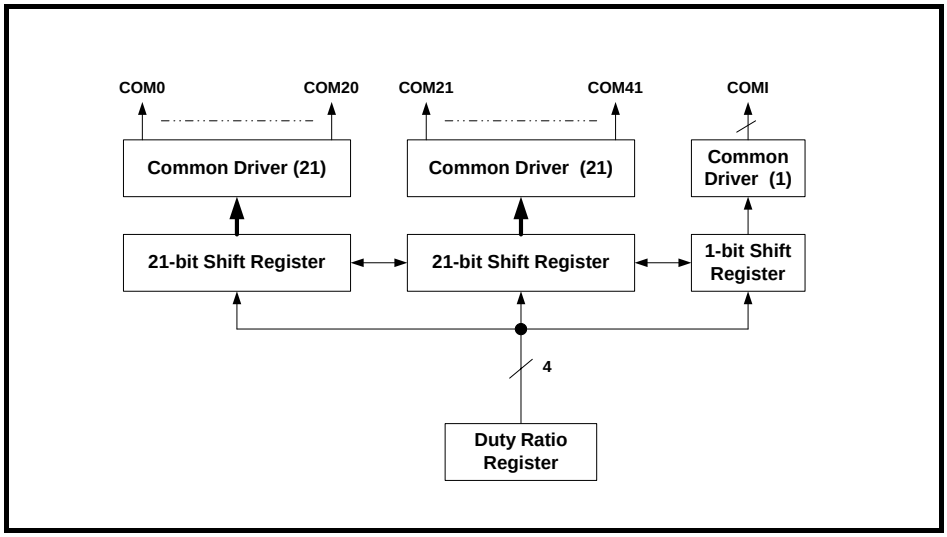


Figure 7-6 Common Output Circuits

Duty	SHL		Common Output Pins (COMxx, refer to the Pad No.)																			
			COM0 ~ 3	~	7	~	11	~	15	~	17	~	24	~	26	~	30	~	34	~	COM38 ~ 41	COMI
1/9	0	Line address	CCOM[0..3]																		CCOM[4..7]	COMI
1/8	1		CCOM[7..4]																		CCOM[3..0]	–
1/17	0		CCOM[0..7]																CCOM[8..15]			COMI
1/16	1		CCOM[15..8]																CCOM[7..0]			–
1/25	0		CCOM[0..11]														CCOM[12..23]					COMI
1/24	1		CCOM[23..12]														CCOM[11..0]					–
1/33	0		CCOM[0..15]												CCOM[16..31]							COMI
1/32	1		CCOM[31..16]												CCOM[15..0]							–
1/37	0		CCOM[0..17]										CCOM[18..35]									COMI
1/36	1		CCOM[35..18]										CCOM[17..0]									–
1/43	0		CCOM[0..41]																			COMI
1/42	1		CCOM[41..0]																			–

Correlation between Duty Ratio and Common Output

Initial Display Line Register

The initial display line register assigns a DDRAM line address which corresponds to COM0 by using the "Initial display line set" instruction. It is used not only for normal display but also for vertical display scrolling and page switching without changing the contents of the DDRAM. However, the 43rd address for icon display cannot be assigned for the initial display line address.

Line Counter

The line counter provides a DDRAM line address. It initializes its contents at the switching of the frame reversal signal (FR), and also counts-up in synchronization with common timing signal.

Column Address Counter

The column address counter is an 8-bit preset counter which provides a DDRAM column address, and is independent of the page address register.

It will increment (+1) the column address whenever "display data read" or "display data write" instructions are issued. However, the incrementing of the column address is stopped at column address 65H. The count-lock will be released by the "column address set" instruction again. The counter can invert the correspondence between the column address and segment driver direction by means of "ADC select" instruction.

Page Address Register

The page address register provides a DDRAM page address. Page Address 6 is used for icon display, and only D0 is valid.

7.4 LCD Driver Circuits

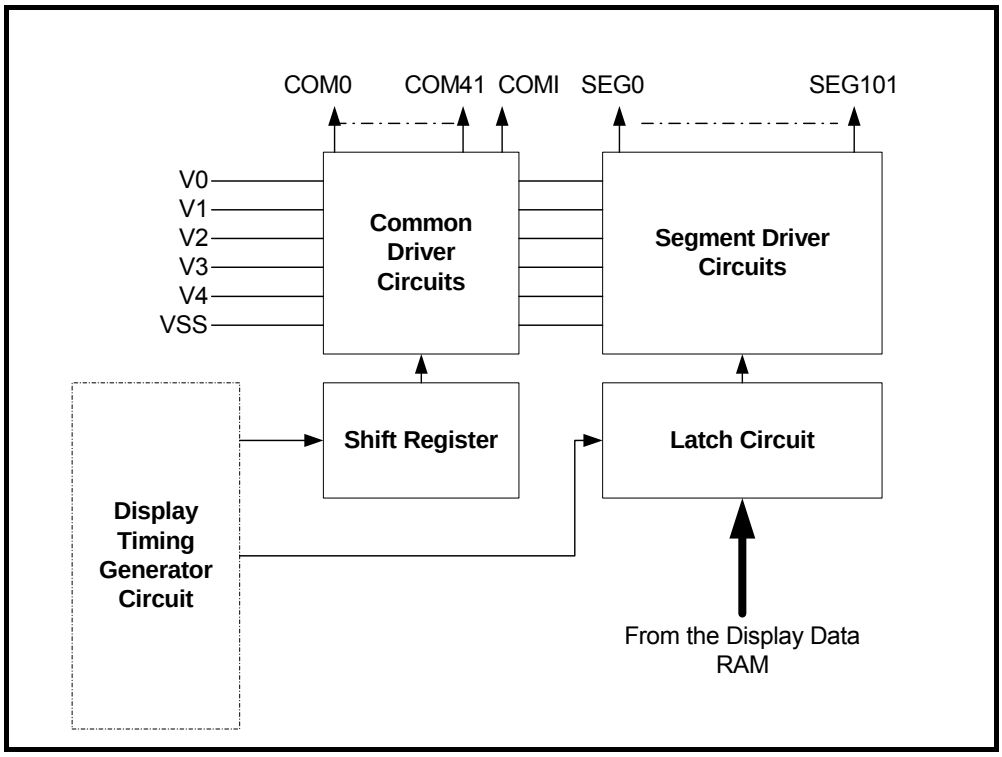


Figure 7-7 LCD Driver Circuits

This driver circuit is configured by 42-common drivers, 102-segment drivers and 1-icon-common driver. This LCD panel driver voltage depends on the combination of display data and FR (internal) signal.

7.4.1 Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. “Display on/off”, “Inverse display on/off” and “Entire display on/off” instructions control only the contents of this latch circuit, they cannot change the contents of the DDRAM.

7.4.2 Shift Register Circuit

The circuit contains a 42-bit shift register to shift and turn-on data required for the LCD drive common signals and 1-bit shift register used for icon. The clock of this shift register is generated by the display clock CL.

Examples of 1/33 and 1/43 Duty (ICON enable) Driving Waveform

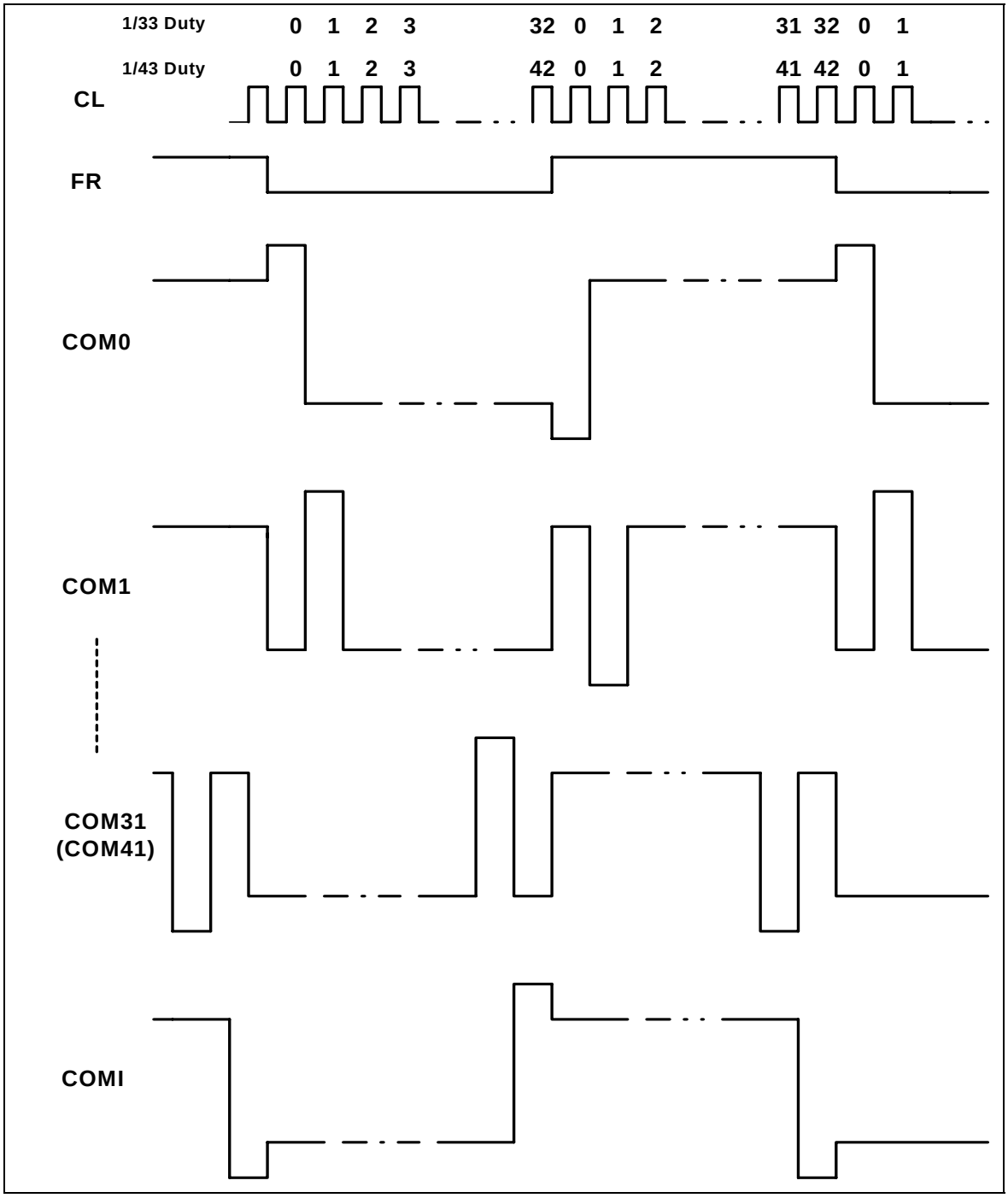


Figure 7-8 1/33 and 1/43 Duty Driving Waveform

Examples of 1/32 and 1/42 duty (ICON disable) Driving Waveform

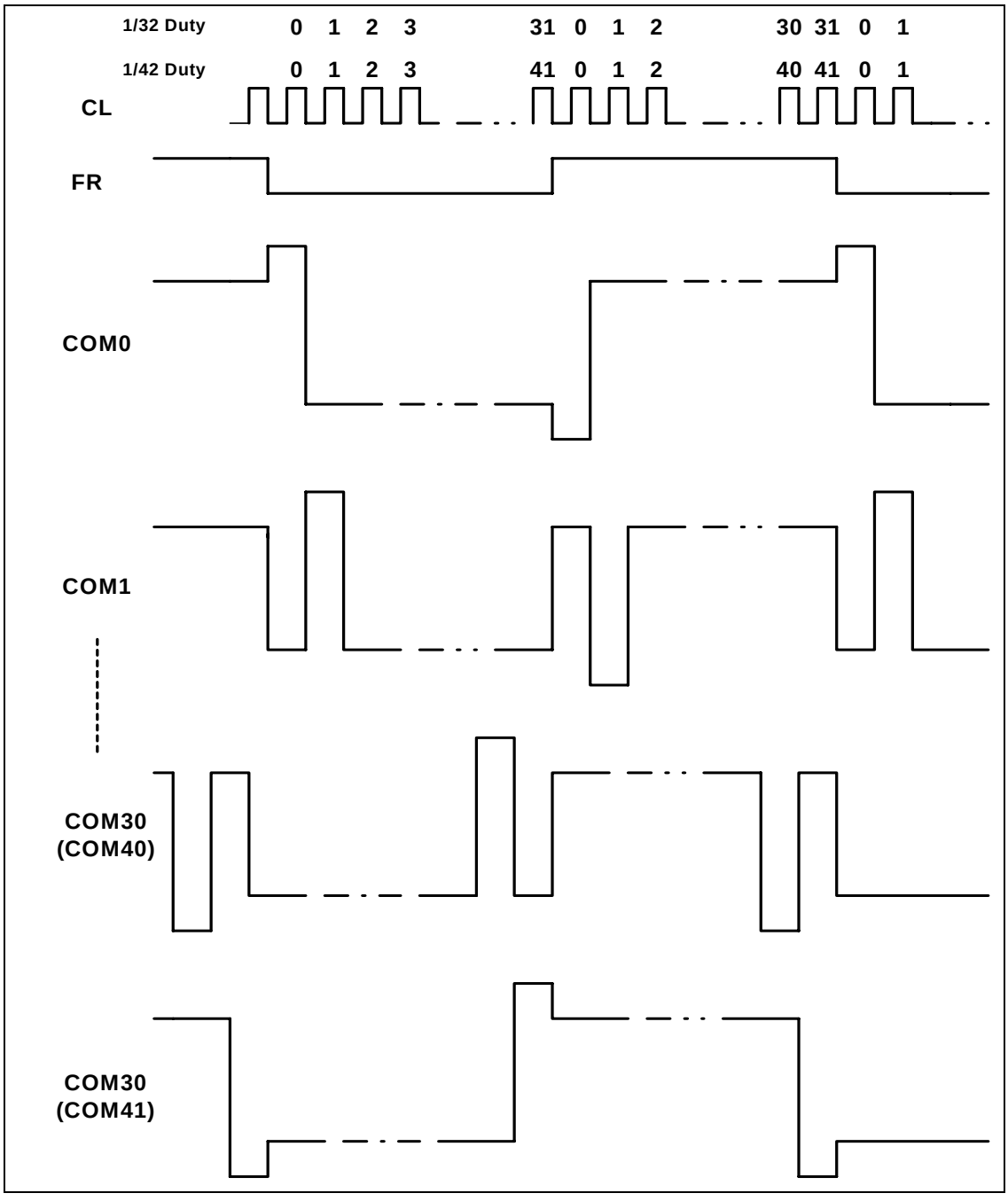
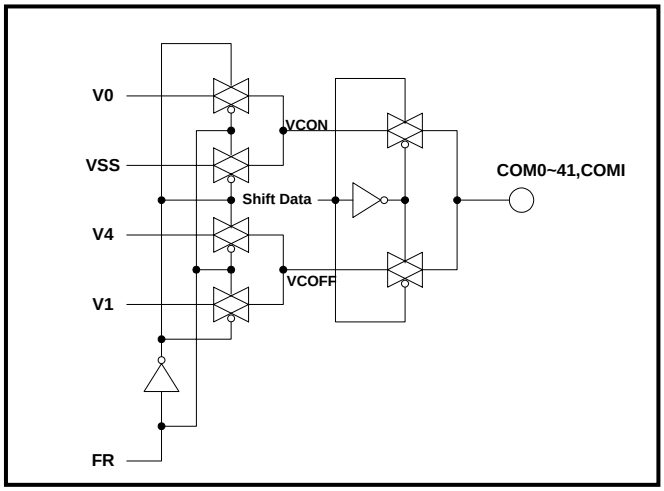


Figure 7-9 1/32 and 1/42 Duty Driving Waveform

7.4.3 Common Driver Circuit

The Common driver circuit consists of 43 drive circuits. One of the four LCD driving level is selected by the combination of FR and data from the shift register.

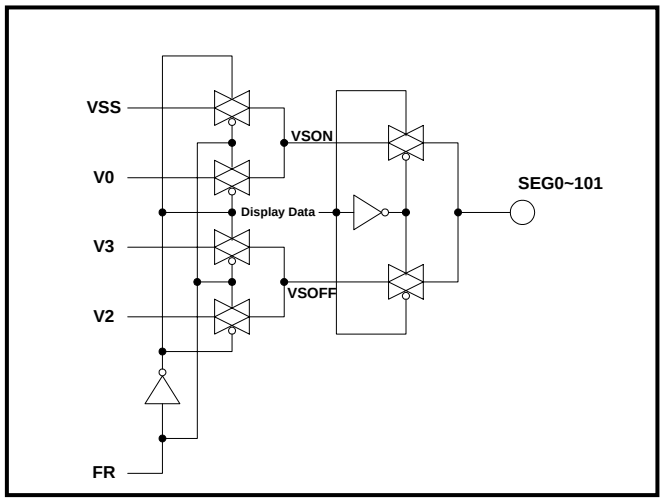


Scan Data	FR	COMs Output Voltage
H	H	VSS
	L	V0
L	H	V1
	L	V4
Power save mode		VSS

Figure 7-10 Common Driver Circuit

7.4.4 Segment Driver Circuit

The Segment driver circuit consists of 102 driver circuits. One of the four LCD driving level is selected by the combination of FR and the display data transferred from the latch circuit.



Display Data	FR	SEGs Output Voltage	
		Normal Display	Inverse Display
H	H	V0	V2
	L	VSS	V3
L	H	V2	V0
	L	V3	VSS
Power save mode		VSS	

Figure 7-11 Common Driver Circuit

7.4.5 LCD Driving Waveform

The following illustration is an example of how the common and segment drivers are attached to an LCD panel.

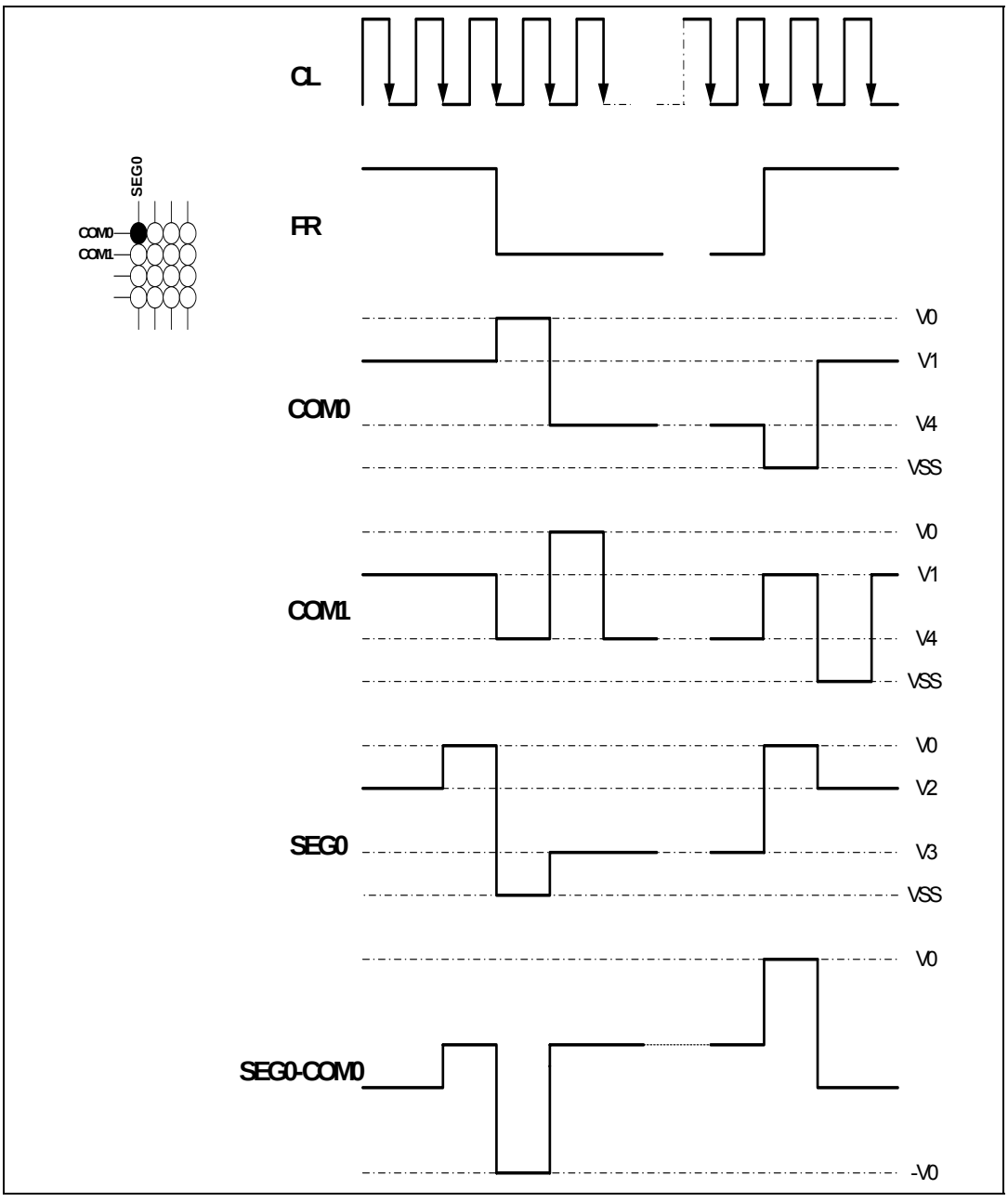


Figure 7-12 LCD Driver Waveform

7.5 Internal Power Circuits

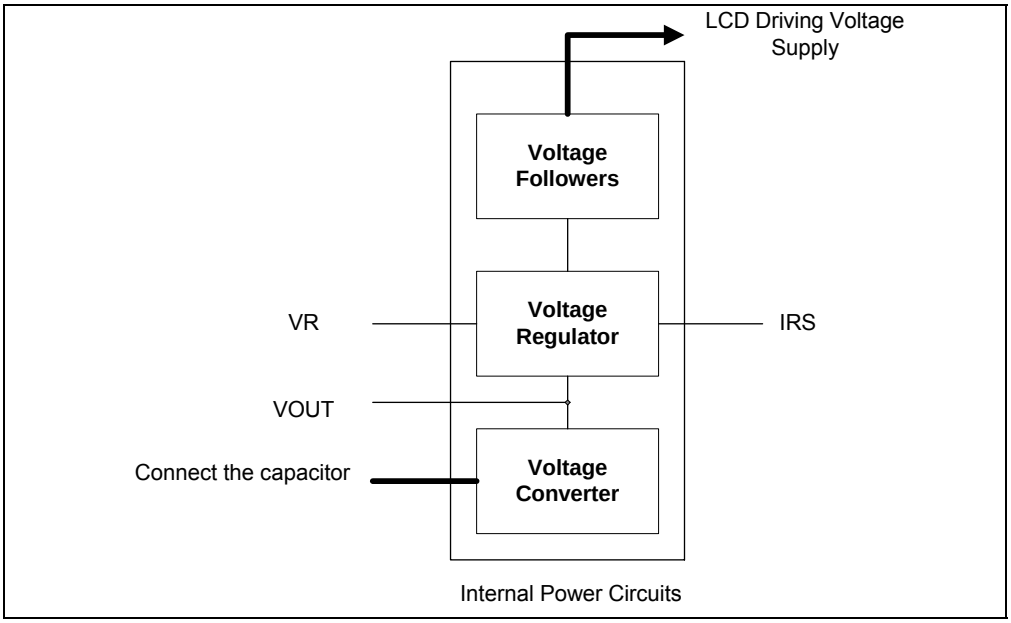


Figure 7-13 Internal Power Circuits

The internal power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter (V/C) circuits, voltage regulator (V/R) circuits, and voltage follower (V/F) circuits. They are valid only in **master** operation and controlled by "Power Control" instruction. For details, refer to Section 8, *"Instruction Description"*.

User Setup	Power Control (VC VR VF)	V/C Circuits	V/R Circuits	V/F Circuits	VOUT	V0	V1~V4
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage Regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External Input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External Input	External Input

7.5.1 Voltage Converter Circuits

These circuits boost up the electric potential between VDD and VSS to 2, 3, 4, or 5 times towards the positive side and the boosted voltage is outputted from the VOUT pin. The boosting magnitude of the internal booster circuit is selected by the capacitor connection (Refer to the Figure below). The internal oscillator is required to be operating when using this converter, since the divided signal provided from the oscillator is used for the internal timing of this circuit.

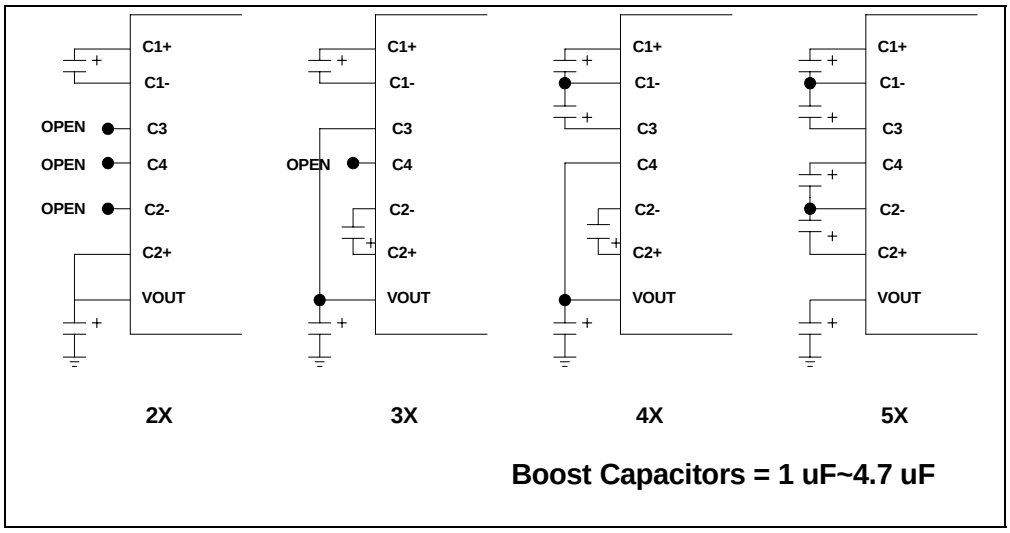


Figure 7-14 Capacitor Connections

7.5.2 Voltage Regulator Circuits

The voltage regulator determines the LCD driving voltage V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Since VOUT is the operating voltage of the operational-amplifier circuits, it is necessary to be applied internally or externally. For Equation 1, we determine V0 by Ra, Rb and VEV. Ra and Rb are connected internally or externally by the IRS pin. **VEV** which is the voltage of the electronic volume is determined by Equation 2, where the parameter α is the value selected by instruction, "Set Contrast Control Mode", within the range 0 to 63.

VREF, a constant voltage source is about 2V at TA=25°C.

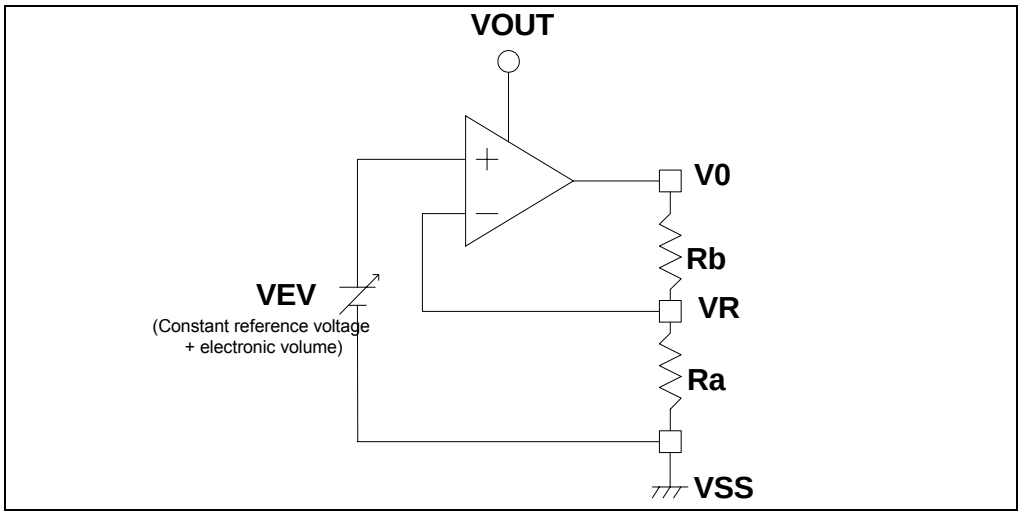


Figure 7-15 Resistor Connection

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV \quad \text{.....Equation 1}$$

$$VEV = (1 - \frac{(63 - \alpha)}{252}) \times VREF \quad \text{.....Equation 2}$$

Register Value (R2 R1 R0)	1+ (Rb/Ra)	Value
0 0 0	3.5	Small . . . . . . Large
0 0 1	4.0	
0 1 0	4.5	
0 1 1	5.0	
1 0 0	5.5	
1 0 1	6.0	
1 1 0	6.5	
1 1 1	7.0	

Refer to Section 8.20, "*Regulator Resistor Select*" instruction for further details.

α	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	0	0	0	0	0	1
..	.	.	.	.	.	.
..	.	.	.	.	.	.
62	1	1	1	1	1	0
63	1	1	1	1	1	1

Refer to Section 8.91, *"Set Contrast Control Mode"* instruction for further details.

Using Internal Resistors, Ra and Rb (IRS = "H")

When the IRS pin is “H”, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. V0 is determined by using the two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Using External Resistors, Ra and Rb (IRS = "L")

When IRS pin is “L”, it is necessary to connect the external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

For a particular liquid, the optimum V_{LCD} can be calculated for a given multiplex rate.

For a 1/43 duty ratio, the optimum operating voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1+\sqrt{43}}{\sqrt{2\times\left(1-\frac{1}{\sqrt{43}}\right)}}\times V_{th} = 5.805\times V_{th}$$

where Vth is the threshold voltage of the liquid crystal material used.

7.5.3 Voltage Follower Circuits

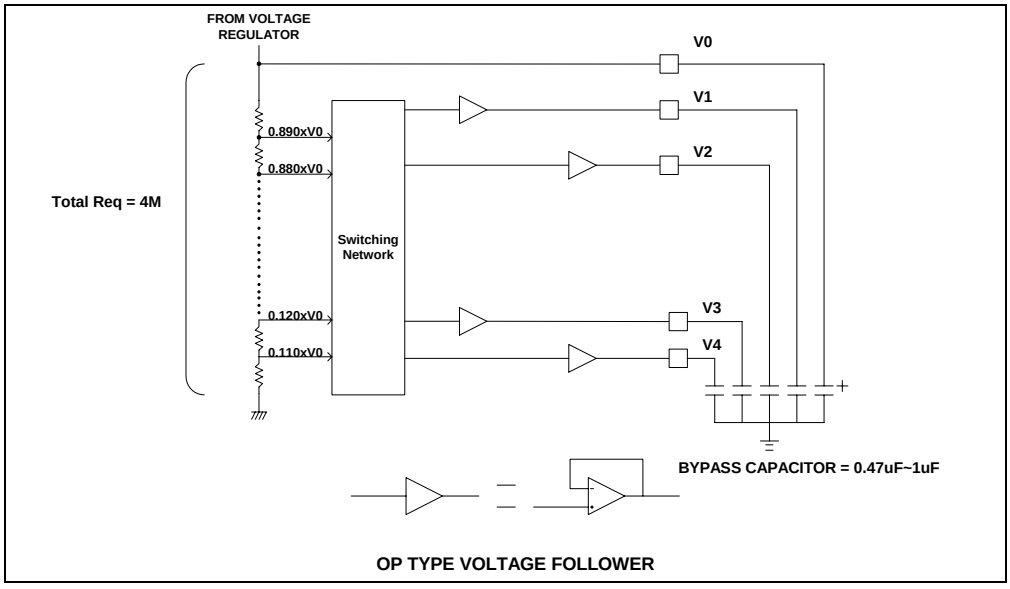


Figure 7-16 OTP Voltage Follower Circuit

The VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower (OPA) to increase the drive capability. A total of six levels LCD reference voltage (V0, V1, V2, V3, V4, VSS) is generated by the voltage follower circuits.

LCD Bias	V1	V2	V3	V4
1/8	0.875*V0	0.750*V0	0.250*V0	0.125*V0
1/7.5	0.865*V0	0.735*V0	0.265*V0	0.135*V0
1/7	0.855*V0	0.715*V0	0.285*V0	0.145*V0
1/6.5	0.845*V0	0.690*V0	0.310*V0	0.155*V0
1/6	0.835*V0	0.665*V0	0.335*V0	0.165*V0
1/5.5	0.820*V0	0.635*V0	0.365*V0	0.180*V0
1/5	0.800*V0	0.600*V0	0.400*V0	0.200*V0
1/4.5	0.780*V0	0.555*V0	0.445*V0	0.220*V0
1/4	0.750*V0	0.500*V0	0.500*V0	0.250*V0
1/3.5	0.715*V0	0.430*V0	0.570*V0	0.285*V0
1/3	0.665*V0	0.335*V0	0.665*V0	0.335*V0

Different duty radio requires different bias level. For optimum bias level, BL can be calculated from:

$$B_L = \frac{1}{\sqrt{Duty\ ratio} + 1}$$

Changing the bias system from the optimum will have a consequence on the contrast and viewing angle.

The LCD Bias affects the display quality. But for the purpose of reducing the current consumption, the unsuitable bias may be selected. Hence, the LCD Bias could be selected by “Select LCD bias” instruction.

7.6 LCD Display Circuits

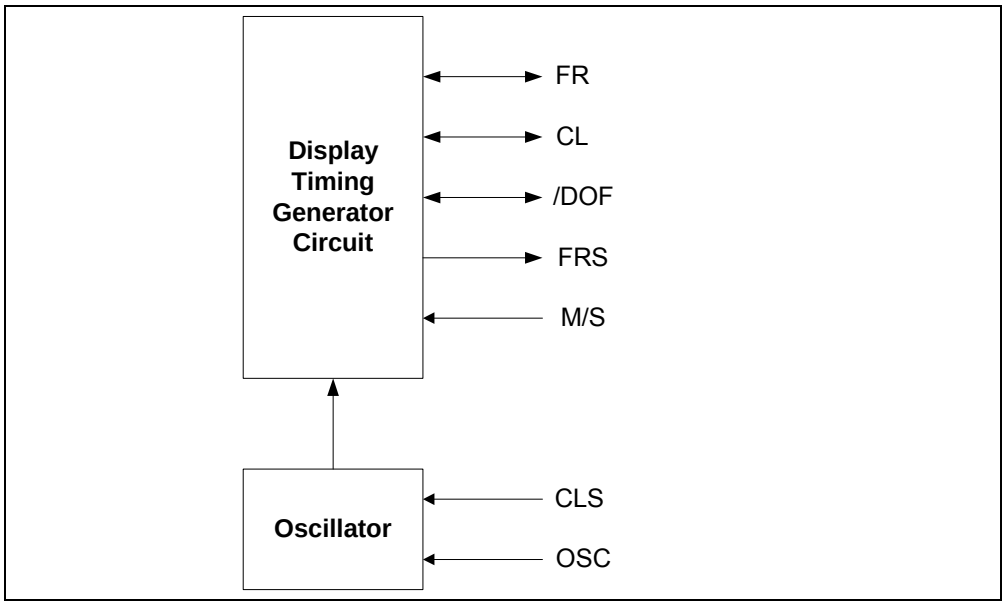


Figure 7-17 LCD Display Circuit

7.6.1 Oscillator

The on-chip RC type oscillator provides the display clock and voltage converter timing clock. It has low power consumption and its frequency is nearly independent of VDD.

When **"M/S="H" and "CLS"="H"**, the oscillator circuit is enabled. When CLS="L", the oscillator is stopped, and the oscillator clock has to be input to the OSC pin.

The oscillator circuit is available in **master** mode only. The oscillator signal is divided and output as display clock at CL pin.

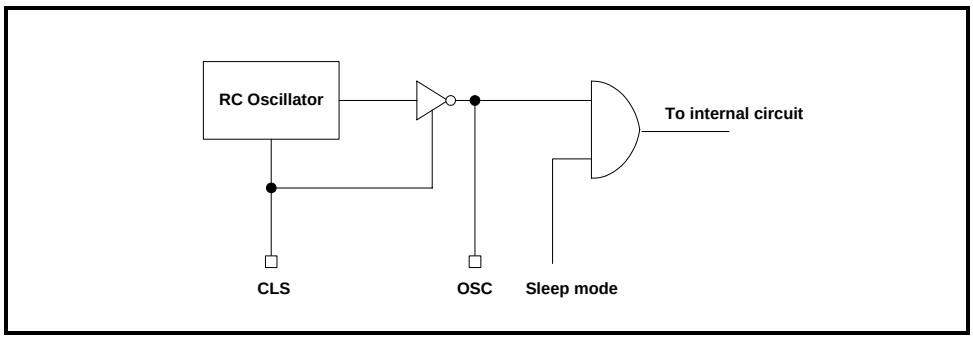


Figure 7-18 RC Oscillator

7.6.2 /DOF Pin Description

The pin is used to control the blinking of the LCD display.

Instruction	M/S= "H"	M/S="L"	
	/DOF (Output)	/DOF (Input) ="H"	/DOF (Input) ="L"
Display "ON"	"H"	LCD On	LCD Off
Display "OFF"	"L"	LCD Off	LCD Off

When the "Power Save" Instruction is activated, the /DOF pin is set to low level.

7.6.3 Display Timing Generator Circuit

This circuit generates some signals to be used to display the LCD. When used in master/slave mode (multi-chip), some pins must be connected to each other. That is due to synchronization output. The display clock (CL) generated by the oscillation clock, generates a clock for the line counter and a latch signal for the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CL). While the 102-bit display data is latched by the display data latch circuit in synchronization with the display clock, the display data which is read to the LCD driver is completely independent from any access to the display data RAM from the microprocessor.

The display clock generates an LCD frame reversal signal (FR) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. When this EPL43102 is used for a multi-chip, the slave chip must receive the FR, CL, /DOF signals from the master.

Operation Mode		FR	CL	/DOF	FRS	OSC
Master (M/S="H")	Internal oscillator is enable(CLS="H")	Output	Output	Output	Output	Open
	Internal oscillator is disable (CLS="L")	Output	Output	Output	Output	Input
Slave (M/S="L")	Internal oscillator is disable (CLS ="L" or "H")	Input	Input	Input	Hi-Z	Open
		Input	Input	Input	Hi-Z	Open

Note: Open means leave this pin open

7.6.4 Oscillator Frequency

The EPL43102 contains an RC oscillator. The frame frequency (f_{FM}) is derived from the RC circuit's oscillation frequency (f_{OSC}) by giving it an appropriate value. The relationship between the oscillation frequency (f_{OSC}), display clock frequency (f_{CL}) and the frame frequency (f_{FM}) is shown in an equation below.

The f_{OSC} could be selected from an internal or external oscillator via the CLS pin, the f_{CL} could be selected using the "Set display clock CL frequency" instruction, and frame frequency could be calculated using the following equation.

$$f_{CL} = (\text{Duty ratio}) \times (\text{Frame frequency})$$

7.7 Reset Circuit

When the /RES input comes to the "L" level, these LSI return to their default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC select instruction D0 = "L")
4. SHL select: Normal (SHL select instruction D3 = "L")
5. Power control register: (D2, D1, D0) = (0, 0, 0)
6. Serial interface internal register data clear
7. Duty ratio = 1/43
8. CL frequency Register (D4, D3, D2, D1,D0) = (0, 0, 0, 0, 1, 1)
9. LCD power supply bias level = (1/8)
10. Entire display OFF (Entire display instruction D0 = "L")
11. Power saving clear

12. Modify-Read OFF
13. Static indicator OFF

    Static indicator register: (D1, D2) = (0, 0)
14. Display initial line set to the first line: 0
15. Column address set to Address: 0
16. Page address set to Page: 0
17. V0 voltage regulator internal resistor ratio set mode clear: (R2, R1, R0) = (0, 0, 0)
18. Contrast control set mode clear

    Contrast control register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)

8 Instruction Description

Instruction	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Description
Read Display Data	1	0	1	Read Data								Read data from DDRAM
Write Display Data	1	1	0	Write Data								Write data into DDRAM
Read Status	0	0	1	Status				0	0	0	0	Read the internal status
Set Duty Ratio Mode	0	1	0	1	0	0	0	0	1	0	0	Set duty ratio Mode
Duty Ratio Register	0	1	0	*	*	*	*	ICON	D2	D1	D0	Select the duty ratio
Set CL frequency Mode	0	1	0	1	0	0	0	0	0	1	0	Set CL frequency Mode
CL frequency Register	0	1	0	*	*	*	D4	D3	D2	D1	D0	Set CL frequency Register
Set LCD Bias select Mode	0	1	0	1	0	0	0	0	1	0	1	Set LCD Bias select Mode
LCD Bias select Register	0	1	0	*	*	*	*	D3	D2	D1	D0	Select the LCD Bias
Display On/Off	0	1	0	1	0	1	0	1	1	1	Don	Turn on/off LCD panel When DON=0: display off When DON=1: display on
Initial Display Line	0	1	0	0	1	D5	D4	D3	D2	D1	D0	Specify DDRAM line for COM0
Set Contrast Control Mode	0	1	0	1	0	0	0	0	0	0	1	Set Contrast Control Mode
Set Contrast Control Register	0	1	0	*	*	D5	D4	D3	D2	D1	D0	Set Contrast Control Register
Set Page Address	0	1	0	1	0	1	1	Page Address				Set page address
Set Column Address MSB	0	1	0	0	0	0	1	Higher order Column Add.				DDRAM column address of the Higher 4 bits
Set Column Address LSB	0	1	0	0	0	0	0	Lower order column Add.				DDRAM column address of the lower 4 bits
ADC Select	0	1	0	1	0	1	0	0	0	0	ADC	Select segment direction When ADC=0: normal direction (SEG0 → SEG101) When ADC=1: reverse direction (SEG101 → SEG0)

Instruction	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Description
Inverse Display ON/OFF	0	1	0	1	0	1	0	0	1	1	REV	Select normal/inverse display 0: Normal display 1: Inverse display on
Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON=0: normal display. When EON=1: entire display ON
Set Modify-read	0	1	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset Modify-read	0	1	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL Select	0	1	0	1	1	0	0	SHL	*	*	*	Select COM output direction When SHL=0: normal direction (COM0 → COM41) When SHL=1: reverse direction (COM41 → COM0)
Power Control	0	1	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator Resistor Select	0	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set Static Indicator Mode	0	1	0	1	0	1	0	1	1	0	SM	Set static indicator mode When SM = 0: off When SM = 1: on
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	S1	S0	Set static indicator register
Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON

Note: * *Don't care*

8.1 Read Display Data

The 8-bit data from the display data RAM specified by the column address and page address can be read by this instruction. As the column address is automatically incremented by 1 after each instruction execution, the microprocessor can continuously read data from the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8.2 Write Display Data

The 8-bit display data from the microprocessor can be written to the RAM location specified by the column address and page address. After writing the display data, the column address is automatically incremented so that the microprocessor can continuously write data to the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

8.3 Read Status

This instruction reads out the internal status of the “ADC select”, “Display on/off” and “Reset”.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	-	ADC	On/Off	RESET	0	0	0	0

Flag	Description
ADC	It shows the correspondence between the column address and segment drivers. ADC = 0 : Reverse direction (SEG101 → SEG0) ADC = 1 : Normal direction (SEG0 → SEG101)
On/Off	This bit indicates the ON/OFF state of the display. 0: Display ON 1: Display OFF
RESET	Indicates the initialization in progress by RESETB signal. RESET = 0 : Normal display operation state RESET = 1 : Internal reset operation state with reset command.

8.4 Set Duty Ratio (Two-Byte Instruction)

This consists of 2-byte instruction. The first instruction sets the duty ratio mode, the second instruction updates the contents of the duty ratio register. After the second instruction, the set duty mode is released. The LSI cannot accept any instructions except for the “Set duty ratio register” during the set duty ratio mode.

8.4.1 Set Duty Ratio Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	0

8.4.2 Set Duty Ratio Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Duty Ratio
0	1	0	*	*	*	*	ICON	0	0	0	8 (+ICON)
								0	0	1	16 (+ICON)
								0	1	0	24 (+ICON)
								0	1	1	32 (+ICON)
								1	0	0	36 (+ICON)
								1	0	1	42 (+ICON)

ICON : “0” Disable COMI (icon display) pin

ICON : “1” Enable COMI (icon display) pin

8.5 Set Display Clock CL Frequency (Two-Byte Instruction)

The display clock CL affects the current consumption and the frame frequency affects the flicker, so fine adjustments are required for the display clock CL and the frame frequency.

8.5.1 Set CL Frequency Select Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	1	0

8.5.2 Set CL Frequency Select Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	CL Frquency
0	1	0	*	*	*	0	0	0	0	0	f_{osc}
						0	0	0	0	1	f_{osc} / 2
						0	0	0	1	0	f_{osc} / 3
						0	0	0	1	1	f_{osc} / 4
						0	0	1	0	0	f_{osc} / 5
						0	0	1	0	1	f_{osc} / 6
						0	0	1	1	0	f_{osc} / 7
						0	0	1	1	1	f_{osc} / 8
						0	1	0	0	0	f_{osc} / 9
						0	1	0	0	1	f_{osc} / 10
						0	1	0	1	0	f_{osc} / 11
						0	1	0	1	1	f_{osc} / 12
						0	1	1	0	0	f_{osc} / 13
						0	1	1	0	1	f_{osc} / 14
						0	1	1	1	0	f_{osc} / 15
						0	1	1	1	1	f_{osc} / 16
						1	*	*	*	*	f_{osc} / 32

8.6 Select LCD Bias (Two-Byte Instruction)

This instruction selects the LCD bias ratio of the voltage required for driving the LCD.

8.6.1 Set the LCD Bias Select Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	1

8.6.2 Set the LCD Bias Select Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	LCD Bias
0	1	0	*	*	*	*	0	0	0	0	1/3
							0	0	0	1	1/3.5
							0	0	1	0	1/4
							0	0	1	1	1/4.5
							0	1	0	0	1/5
							0	1	0	1	1/5.5
							0	1	1	0	1/6
							0	1	1	1	1/6.5
							1	0	0	0	1/7
							1	0	0	1	1/7.5
							1	0	1	0	1/8

8.7 Display On/Off

This instruction is used to control the turning on or off of the LCD panel regardless of the contents of the DDRAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display On or Off
0	1	0	1	0	1	0	1	1	1	0	0 :Off
										1	1 :On

8.8 Initial Display Line

This instruction sets the line address of the display RAM to determine the initial display line. The initial display line corresponds to COM0. The display area read from the display data RAM corresponds to the number of lines set by the Duty select command.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Line Address for COM0
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					.	.	.	.	.	.	.
					.	.	.	.	.	.	.
					1	0	1	0	0	0	40
					1	0	1	0	0	1	41

8.9 Electronic Contrast Control Set (Two-Byte instruction)

This consists of 2-byte instruction. The first instruction sets contrast control mode, the second instruction updates the contents of the contrast control register. After second instruction, the contrast control mode is released. The LSI cannot accept any instructions except for the “Set Contrast Control Register” during the Contrast Control Mode.

8.9.1 Set Contrast Control Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

8.9.2 Set Contrast Control Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Electronic Volume Value (α)
0	1	0	*	*	0	0	0	0	0	0	0 Minimum
					0	0	0	0	0	1	1
					.	.	.	.	.	.	.
					.	.	.	.	.	.	.
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

8.10 Set Page Address

This instruction sets the page address of the display data RAM from the microprocessor into the page address register. It is possible to access any required bit in the display data RAM by specifying the page address and the column address.

Along with the column address, the page address defines the address of the display RAM used to write or read the display data. Changing the page address does not affect the display status. Page 8 is assigned for the icon display. Only D0 is valid.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Page Address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							.	.	.	.	.
							.	.	.	.	.
							0	1	1	0	6

8.11 Set Column Address

This instruction sets the column address of the display data RAM from the microprocessor into the column address register. When accessing the display data RAM from the MPU, the column address is incremented. The incrementing of the column address is stopped at address 65H.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Column Address Setting
0	1	0	0	0	0	1	A7	A6	A5	A4	Upper 4-bit
						0	A3	A2	A1	A0	Lower 4-bit

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
0	1	1	0	0	1	0	0	100
0	1	1	0	0	1	0	1	101

8.12 ADC Select

This instruction selects the segment driver direction. Normal or reverse can be selected in the correlation between the display data RAM column address and the segment output terminal.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Segment Driver Direction
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

D0 = 0 Normal Column addresses 00H to 65H correspond to segment outputs 0 to 101.

D0 = 1 Reverse Column addresses 00H to 65H correspond to segment outputs 101 to 0.

8.13 Inverse Display On/Off

This instruction is used to invert the display status of the LCD panel without rewriting the contents of the display data RAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display Status
0	1	0	1	0	1	0	0	1	1	0	Normal
										1	Inverse

D0 = 0 Normal Display data “1” turns the LCD on.

D0 = 1 Inverse Display data “0” turns the LCD on.

8.14 Entire Display On/Off

This instruction forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM will be retained. This instruction has priority over the Reverse Display On/Off instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Entire Display On/Off
0	1	0	1	0	1	0	0	1	0	0	Normal
										1	Entire display on

8.15 Set Modify-Read

This instruction stops the automatic increment of the column address by the Read Display Data instruction, but the column address is still incremented by the Write Display Data instruction. This instruction can reduce the load of the MPU. During the display, the data in a specific DDRAM area is repeatedly changed for cursor blinking or other functions. This mode is canceled by the Reset Modify-read instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

8.16 Reset Modify-Read

This instruction cancels the Modify-read mode. The column address of the display data RAM returns to the address before the Read Modify Write is executed.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

8.17 Reset

This instruction resets the initial display line, column address, page address, and the common output status is reset to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the /RES pin.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Reset status by “Reset” instruction:

1. Read modify write off
2. Static indicator off and static indicator register: (S1, S0) = (0, 0)
3. Initial display line address: (00)H
4. Column address: (00)H
5. Page address: (0) page
6. SHL select: Normal mode (D3 = 0)
7. Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
8. Sets contrast control set mode off and contrast control register: (20)H

8.18 SHL Select

The COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Common Driver Direction
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Reverse

Note: * *Don’t care*

D3 = 0 Normal Normal direction (COM0 → COM 41)

D3 = 1 Reverse Reverse direction (COM41 → COM 0)

8.19 Power Control

This instruction is used to select one of the eight power circuit functions by using the 3-bit register. An external power supply and part of the internal power supply functions can be used simultaneously.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	VC	VR	VF

VC: Voltage converter
0: Off
1: On

VR: Voltage regulator
VF: Voltage follower

8.20 Regulator Resistor Select

This selects the resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit for more details.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb/Ra] Ratio
0	0	0	Small
0	0	1	…
..	..	..	..
1	1	0	..
1	1	1	Large

8.21 Set Status Indicator (Two-Byte Instruction)

This consists of two bytes instruction. The first byte instruction (Set Static Indicator Mode) enables the second byte instruction (Set Static Indicator Register) to be valid. The first byte sets the static indicator on/off. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this status indicator state is released after setting the data of the indicator register.

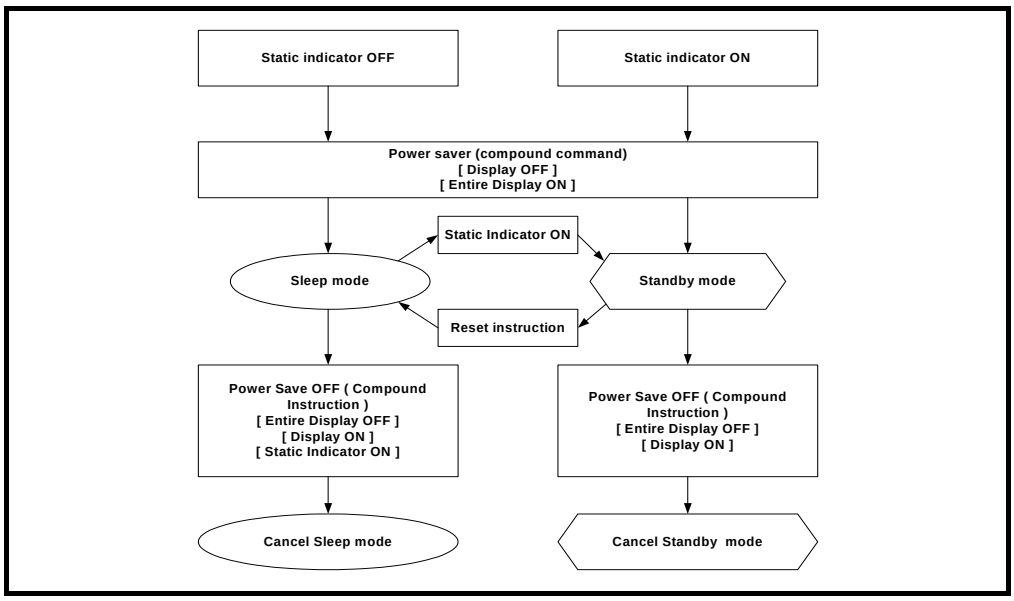
8.21.1 Set Status Indicator Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	Off
										1	On

8.21.2 Set Status Indicator Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Status
0	1	0	*	*	*	*	*	*	0	0	Off
									0	1	On (Blink at 4-frame intervals)
									1	0	On (Blink at 2-frame intervals)
									1	1	On (Turn on at all time)

8.22 Power Save (Compound Instruction)



The current consumption can be greatly reduced by entering the power save status and by inputting the “Entire Display ON” instruction while the display is in OFF mode. According to the status in static indicator mode, power save is entered through one of two modes (sleep and standby mode). When Static Indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the “Display ON” & “Entire Display OFF” instruction.

8.22.1 Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

1. The oscillator circuit and the LCD power supply circuit are stopped.
2. All liquid crystal drive circuits are stopped, and the segment and common driver output VSS level.

When a “static indicator on” instruction is issued in sleep mode, the LSI goes into a *standby mode*.

8.22.2 Standby Mode

All operations of the dynamic LCD display section are stopped, only the static display circuits for the indicators operate and hence the current consumption will be the minimum necessary for static drive. The internal conditions in the standby state are as follows:

1. The power supply circuit for LCD drive is stopped. The oscillator circuit will be operating.
2. The LCD drive circuits for dynamic display are stopped and the segment and common driver outputs will be at the VSS level. The static display section will be operating.

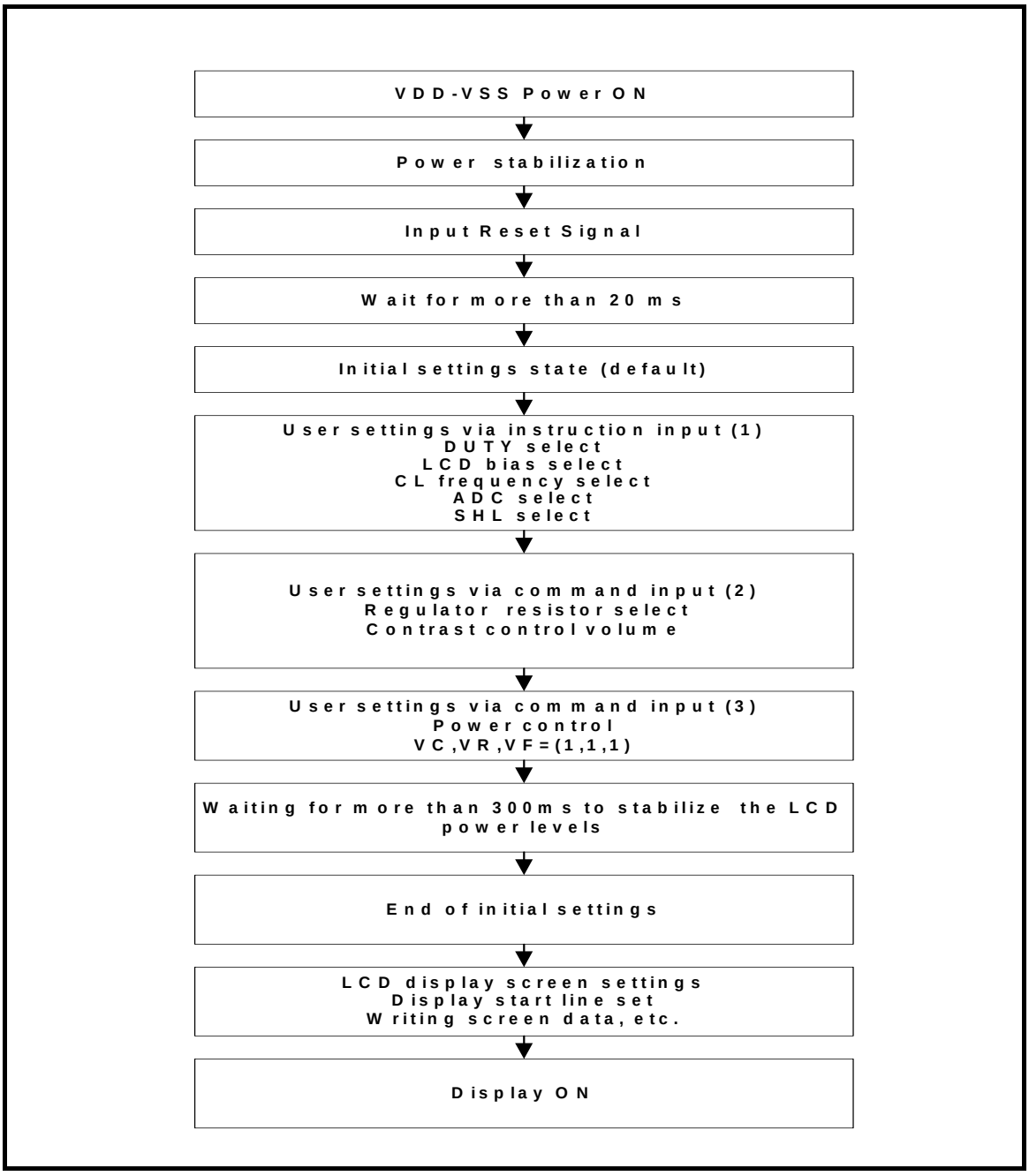
When a reset instruction is issued in the standby mode, the LSI goes into the *sleep* mode.

9 Application Information

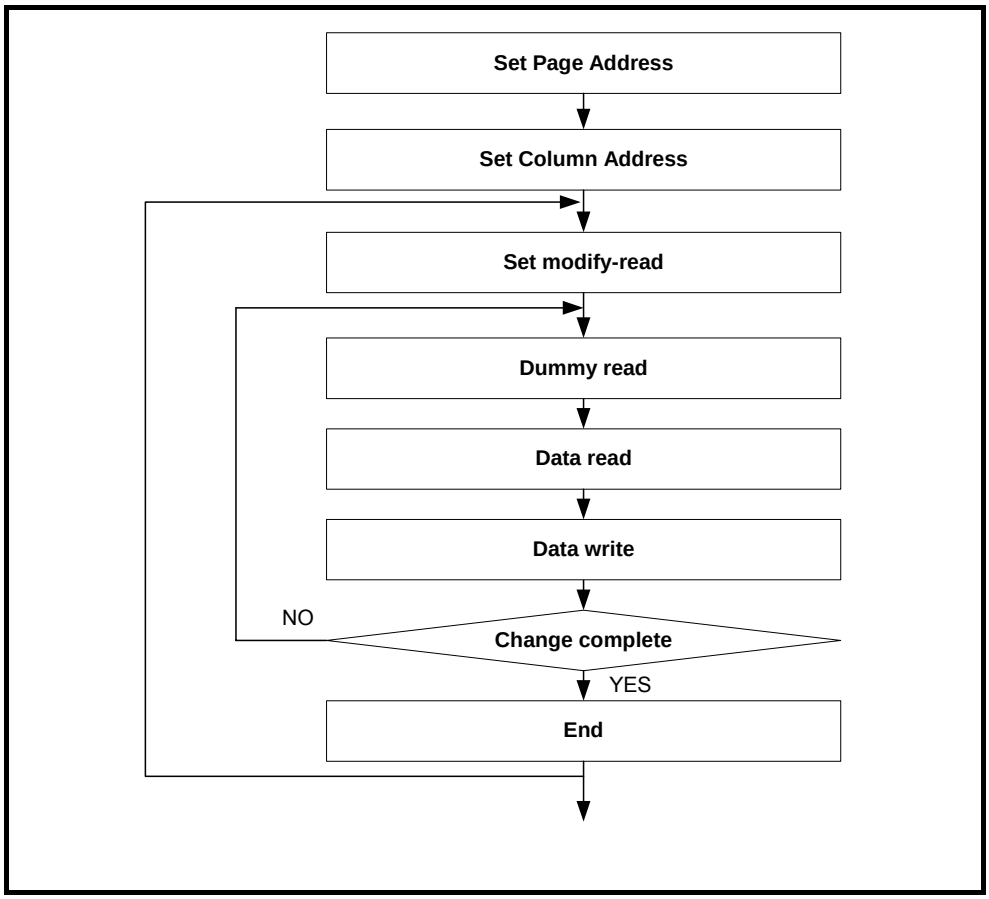
9.1 Instruction Procedure Examples

9.1.1 Initial Setup

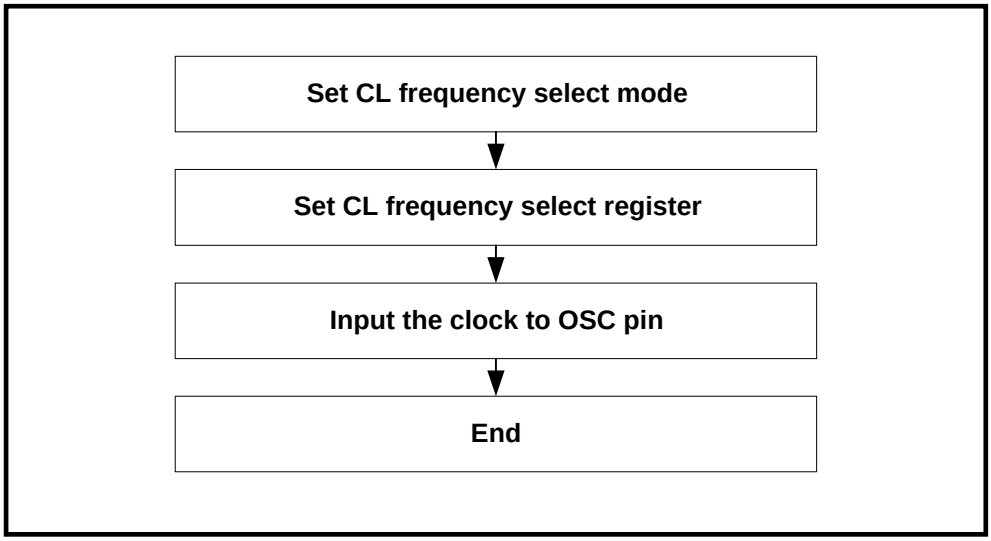
(From power application to display ON using internal power supply circuits)



“Modify-read” Sequence



External Oscillator Input” Sequence



9.2 Program Examples

Use Elan RISC II MCU assembly

```
;*************************************************************************
;            Initialization Setting Example of EPL43102
;*************************************************************************
INI_DRIVER_IC:
  MOV   A,#LCD_COM_RESET          ;INITIAL SETTINGS STATE (DEFAULT)
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_DUTY           ;SET DUTY 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#DUTY_SET               ;SET DUTY 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_BIAS           ;SET LCD BIAS 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,BIAS_SET                ;SET BIAS 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_FREQ           ;SET LCD CL FREQUENCY 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#CL_FREQ                ;SET CL FREQUENCE 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_ADC_SET            ;SET ADC FUNCTION SELECT
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_SHL_SET            ;SET SHL FUNCTION SELECT
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_REGULATOR_RES_SET  ;SET REGULATOR RESISTOR 1+(Rb/Ra)
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_CONTRAST       ;SET CONTRAST 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#CONTRAST_SET           ;SET CONTRAST 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_POWER_CONTROL_SET  ;SET POWER CONTROL (INTERNAL OR EXTERNAL)
  CALL  WRITE_LCD_1BYTE
  BS    REG_CPUCON,F_CKS          ;ADD CLOCK BY OSC PIN (CLOCK FROM CPU)
  MOV   A,#150                    ;WAIT TO STABILIZE THE LCD POWER
  CALL  WAIT_A_MS
  CALL  LCD_DISPLAY_ON            ;TURN ON LCD
  MOV   A,#LCD_DISPLAY_INI_LINE   ;SET INITIAL DISPLAY LINE
  CALL  WRITE_LCD_1BYTE
  CALL  LCD_DATA_WRITE            ;WRITING SCREEN DATA
  RET
```

```
*******************************************************************************
;  Write Display_Picture Data into Display Data RAM of EPL43102
;*******************************************************************************
DATA_WRITE:
  TBPTL   #DISPLAY_PICTURE*2      ;DEFINE DISPLAY PICTURE DATA INDEX
  TBPTM   #DISPLAY_PICTURE/0x80
  TBPTH   #DISPLAY_PICTURE/0x8000
DATA_WRITE_43102:
  MOV     A,#LINE_Y_MAX           ;MAX PAGES OF DDRAM
  MOV     REG_LCDARH,A
DATA_W1:
  MOV     A,#LINE_X_MAX           ;SET MAX SEGMENTS OF DDRAM
  MOV     REG_LCDARL,A
  BC      REG_PORTB,F_LCD_A0      ;SET LCD /A0=0 INSTRUCTION OUTPUT
  MOV     A,#LCD_COM_PAGE
  ADD     A,REG_LCDARH
  CALL    WRITE_LCD_1BYTE
  MOV     A,#0b00000000           ;SET LOWER ORDER COLUMN ADDRESS=0000
  CALL    WRITE_LCD_1BYTE
  MOV     A,#0b00010000           ;SET HIGHER ORDER COLUMN ADDRESS=0000
  CALL    WRITE_LCD_1BYTE
  BS      REG_PORTB,F_LCD_A0      ;SET LCD /A0 = 1 DATA OUTPUT
DATA_W2:
  TBRD    01,REG_ACC              ;ACCESS THE DATA OF DISPLAY_PICTURE
  CALL    WRITE_LCD_1BYTE
  DEC     REG_LCDARL
  JBS     REG_STATUS,F_C,DATA_W2  ;IDENTIFY RES_STATUS CARRY BIT SET OR NOT
  DEC     REG_LCDARH
  JBS     REG_STATUS,F_C,DATA_W1
  BC      REG_PORTB,F_LCD_A0      ;LCD /A0 = 0 FOR INSTRUCTION OUTPUT
  RET
```

```
;*************************************************************************
;
;   Write One Byte Data into DDRAM (Parallel Mode 80 Series)
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION WRITE
WRITE_LCD_1BYTE:
  JBS   REG_DCRG,F_LAHEN,WRITE_LCD_1BYTE_1     ;CHECK REG_DCRG LAHEN BIT=1 OR NOT
  BC    REG_PORTC,F_LCD_WR                     ;SET /WR=0 ENABLE WRITE
  MOV   REG_DATA,A                             ;MOVE A → PORT_G
  NOP                                          ;Write low pulse( Wait 2 instruction cycles)
  NOP
  BS   REG_PORTC,F_LCD_WR                      ;SET /WR=1 DISABLE WRITE
  NOP
  NOP
  NOP
  NOP
  RET
WRITE_LCD_1BYTE_1:
  MOV   REG_DATA,                              ;MOVE A → PORT_G
  RET


;*************************************************************************
;
;   Read One Byte Data into DDRAM (Parallel Mode 80 Series)
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION READ
READ_LCD_1BYTE:
  BC    REG_PORTB,F_LCD_RD                     ;SET /RD=0 ENABLE READ
  NOP
  NOP
  MOV   A,REG_DATA                             ;MOVE PORT_G → A
  NOP
  BS    REG_PORTB,F_LCD_RD                     ;SET /RD=1 DISABLE READ
  NOP
  RET
```

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Applicable Pins	Symbol	Condition	Rated Value	Unit
Power supply voltage	VDD	VDD	—	-0.3 to +7	V
Driver supply voltage	VOUT	VLCD	—	-0.3 to +17	
Input voltage	All Input	VIN	—	-0.3 to VDD+0.3	
Operating temperature range	—	TA	—	-30 to +80	°C
Storage temperature range	—	—	—	-55 to +125	

10.2 Recommended Operating Conditions

Parameter	Applicable Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power supply Voltage	VDD	VDD	—	2.2	—	5.5	V
Voltage converter output voltage	VOUT	VOUT	—	4.0	—	15	
Output voltage	—	VOH	—	0.7VDD	—	VDD	
	—	VOL	—	VSS	—	0.3VDD	
Input voltage	—	VIH	—	0.7VDD	—	VDD	
	—	VIL	—	VSS	—	0.3VDD	
Operating temperature range	—	TA	—	0	—	40	°C

10.3 DC Characteristics

VSS=0V, VDD=2.6 to 3.3V, TA= -30~80°C

Parameter	Applicable Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	VDD	VDD	–	2.2	—	5.5	V
Voltage converter input voltage	VDD	VDD2	2 × boost	2.2	—	5.5	
	VDD	VDD3	3 × boost	2.2	—	5.0	
	VDD	VDD4	4 × boost	2.2	—	3.75	
	VDD	VDD5	5 × boost	2.2	—	3.0	
Reference voltage	–	V_{REF0}	TA = 0°C	2.07	2.16	2.25	
		V_{REF20}	TA = 20°C	1.96	2.05	2.14	
		V_{REF40}	TA = 40°C	1.86	1.94	2.02	
Regulated voltage	V0 [1]	V0	TA = 0~40°C	V0-4%	V0	V0+4%	
OP Amp voltage output of LCD power supply	V0	VOUT0	No load [2 & 3]	—	V0	—	mV
	V1	VOUT1		—	V1	—	
	V2	VOUT2		—	V2	—	
	V3	VOUT3		—	V3	—	
	V4	VOUT4		—	V4	—	
Voltage converter output voltage	VOUT	VOUT	x2/x3/x4/x5 No load	95	99	100	%
LCD driver ON resistance	COMn SEGn	RON	Current load I_{load}= 50µA	—	2	5	kΩ
Reset resistor	/RES	R_{RESET}	VDD=3V, Vin=0V	400	800	1200	
			VDD=3V, Vin=1.7V	25	50	75	
Output current (Source and Drain)	[5]	IOH	VDD=3V, VOH=2.4V	-3	-4	-5	mA
		IOL	VDD=3V, VOL=0.2V	1.2	2.2	3.2	
Input leakage current	All Input [4]	IIL	VIN= VDD or 0V	—	—	±1	µA
Output Tri-state	[5]	—	—	—	—	± 3	
Dynamic current consumption (1/43 duty)	—	IDDD1	VDD=3V, TA=25°C, Five boosting, Internal OSC, f_{OSC}=22kHz, 1/43 duty ratio, no load All display pattern off,	—	70	100	µA
Dynamic current consumption (1/32 duty)	—	IDDD2	VDD=3V, TA=25°C Double boosting, External OSC,. f_{OSC}=22kHz, 1/32 duty ratio, no load All display pattern off	—	40	55	µA
V1 sink ability	V1	Isv1	V0=3.6V, V1=2.4V (No load) VOH=2.8V	0.75	1	—	µA
V4 source ability	V4	Isv4	V0=3.6V, V4=1.2V (No load) VOL=0.8V	-0.75	-1	—	µA

Parameter	Applicable Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Current consumption		IDDs1	Standby mode	—	5	10	μA
		IDDs2	Sleep mode	—	1	2	
Frame frequency		fFM	–	—	85	—	Hz
Internal Oscillator frequency	—	fOSC	TA=25°C	17	22	27	kHz
External input Oscillator	OSC	fOSC	TA=25°C	—	22	—	

Note [1]: $V0 = (1 + \frac{Rb}{Ra}) \times VEV \;\; ; \; VEV = (1 - \frac{(63 - \alpha)}{252}) \times VREF$

[2]:

LCD Bias		V1	V2	V3	V4
1/8 Bias	V0	(7/8) × V0	(6/8) × V0	(2/8) × V0	(1/8) × V0
1/7.5 Bias		(6.5/7.5) × V0	(5.5/7.5) × V0	(2/7.5) × V0	(1/7.5) × V0
1/7 Bias		(6/7) × V0	(5/7) × V0	(2/7) × V0	(1/7) × V0
1/6.5 Bias		(5.5/6.5) × V0	(4.5/6.5) × V0	(2/6.5) × V0	(1/6.5) × V0
1/6 Bias		(5/6) × V0	(4/6) × V0	(2/6) × V0	(1/6) × V0
1/5.5 Bias		(4.5/5.5) × V0	(3.5/5.5) × V0	(2/5.5) × V0	(1/5.5) × V0
1/5 Bias		(4/5) × V0	(3/5) × V0	(2/5) × V0	(1/5) × V0
1/4.5 Bias		(3.5/4.5) × V0	(2.5/4.5) × V0	(2/4.5) × V0	(1/4.5) × V0
1/4 Bias		(3/4) × V0	(2/4) × V0	(2/4) × V0	(1/4) × V0
1/3.5 Bias		(2.5/3.5) × V0	(1.5/3.5) × V0	(2/3.5) × V0	(1/3.5) × V0
1/3 Bias		(2/3) × V0	(1/3) × V0	(2/3) × V0	(1/3) × V0

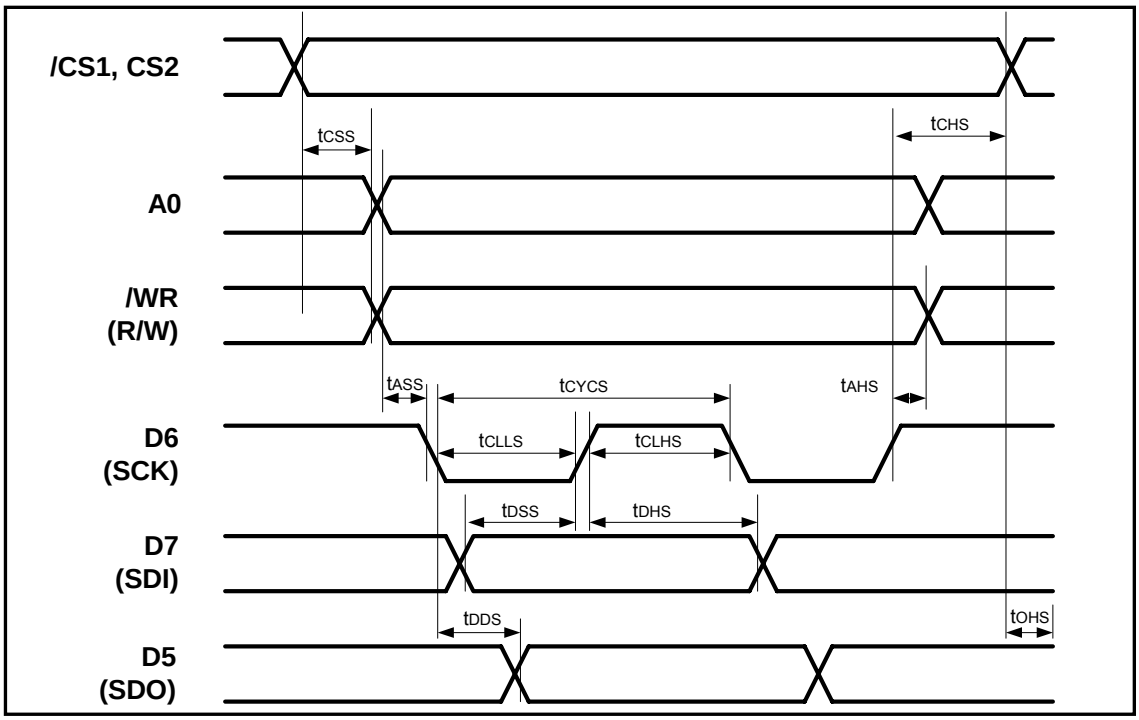
[3]: **The** target value of V0~V4 is Theoretical Value ± 50mV

[4]: Input pin D0~D7, A0, /RD, /WR, /CS1, CS2, CLS, M/S, C86, P/S, IRS

[5]: Output pin D0~D7, FR, FRS, /DOF, CL

10.4 AC Characteristics

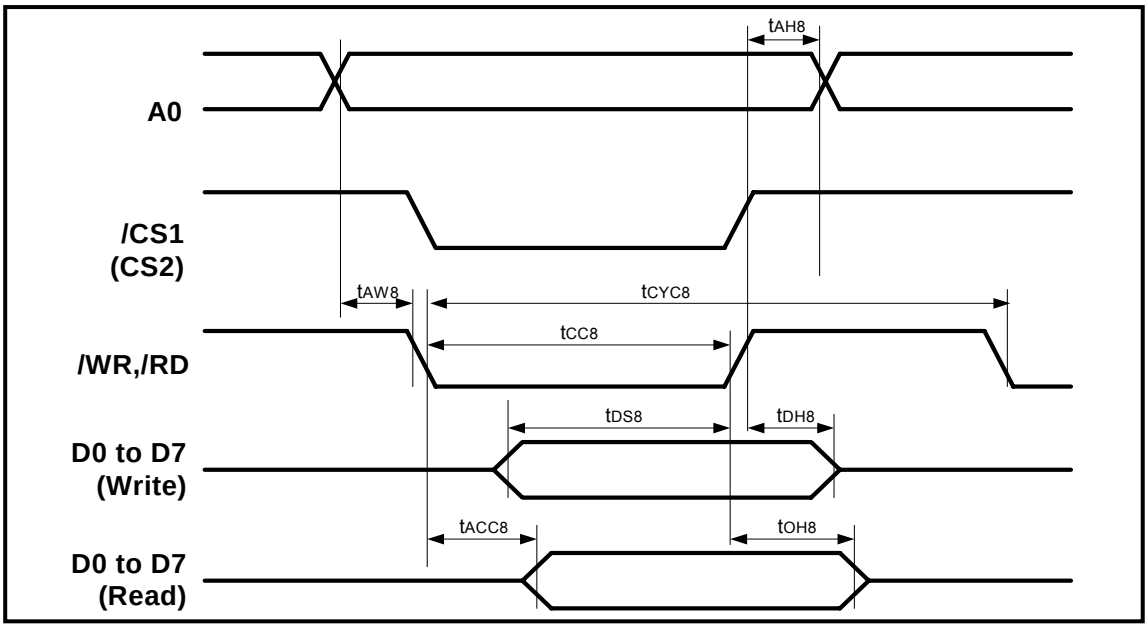
Serial Interface Timing Characteristics



VSS=0V, VDD=2.6 to 3.3V, TA= 0~40°C

Parameter	Applicable Pins	Symbol	Condition	Rated Value		Unit
				Min.	Max.	
Chip Select Setup Time Chip Select Hold Time	/CS1 CS2	tCSS tCHS		100 100	—	ns
Address Setup time Address Hold time	A0 R/W	tASS tAHS		100 100	—	
Data Setup Time Data Hold Time	D7 (SDI)	tDSS tDHS	DATA→SCK↑ SCK↑→DATA	80 80	—	
Clock Cycle Time Clock L Time Clock H Time	D6 (SCK)	tCYCS tCLLS tCLHS		300 100 100	—	
Data Delay Time Data Disable Time	D5 (SDO)	tDDS tOHS	CL= 100 pF	 10	80 50	

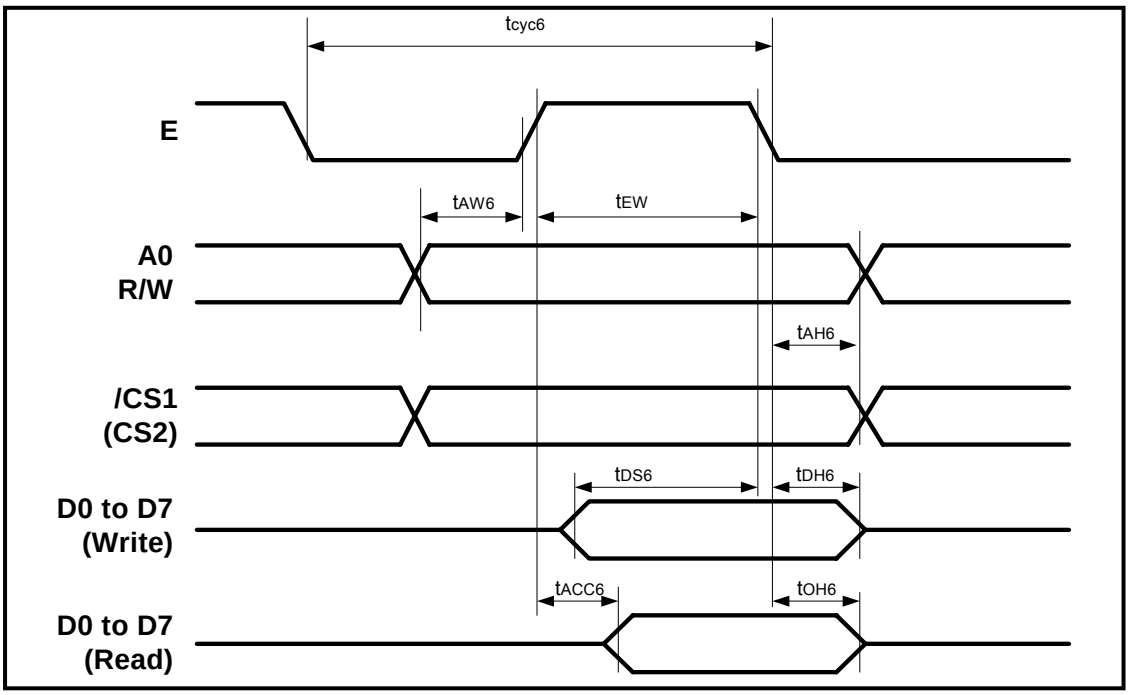
10.5 80-Family MPU Read/Write Timing Characteristics



VSS = 0V, VDD = 2.6 to 3.3V, TA = 0~40°C

Parameter	Applicable Pins	Symbol	Condition	Rated Value		Unit
				Min.	Max.	
Address Setup Time Address Hold Time	A0	tAW8 tAH8	—	0 0	—	ns
System Cycle Time	A0	tCYC8	—	500	—	
Pulse Width(/WR) Pulse Width(/RD)	/WR /RD	tCC8	—	160 200	—	
Data Setup Time Data Hold Time	D0~D7	tDS8 tDH8	—	20 10	—	
Read Access Time Output Disable Time		tACC8 tOH8	CL=100pF	— 10	60 40	

10.6 68-Family MPU Read/Write Timing Characteristics

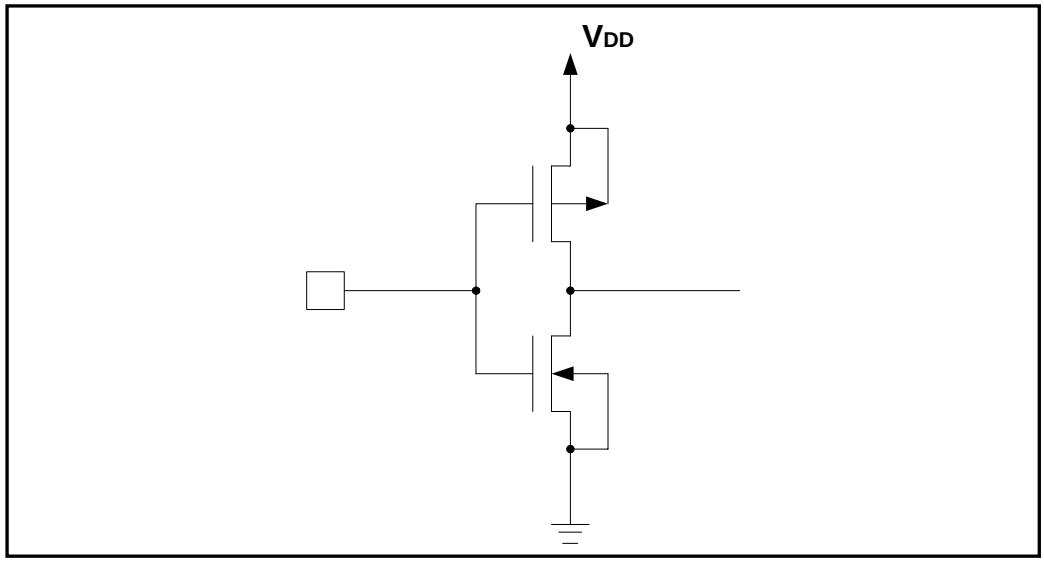


VSS=0V, VDD=2.6 to 3.3V, TA= 0~40°C

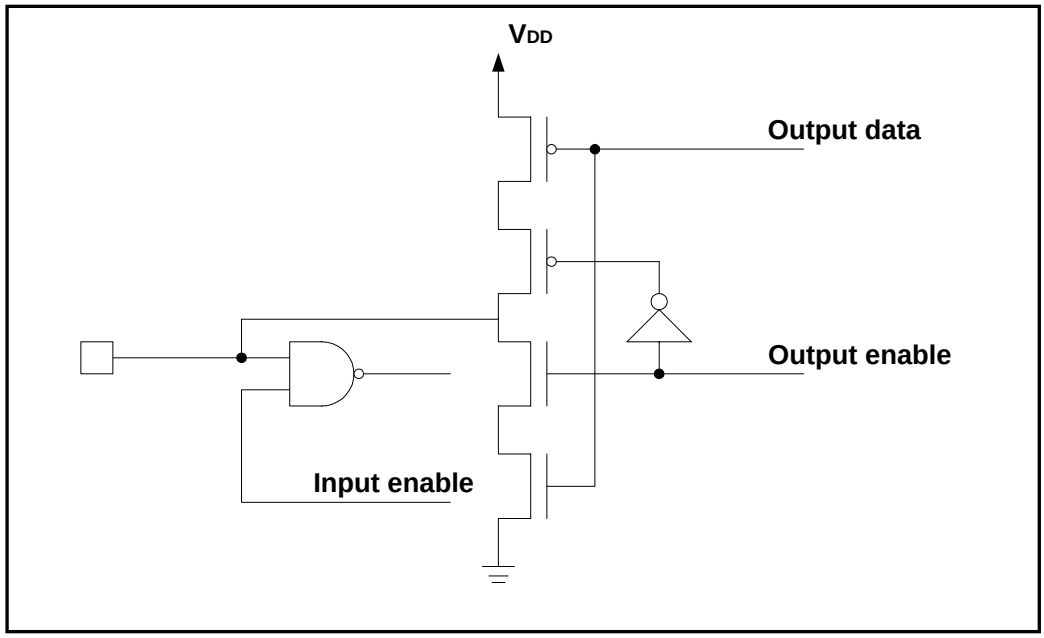
Parameter	Applicable Pins	Symbol	Condition	Rated Value		Unit
				Min.	Max.	
Address Setup Time Address Hold Time	A0 R/W	tAW6 tAH6	—	0 0	—	ns
System Cycle Time	A0	tCYC6	—	500	—	
Pulse Width(/WR) Pulse Width(/RD)	E	tEW	—	160 200	—	
Data Setup Time Data Hold Time	D0~D7	tDS6 tDH6	—	20 10	—	
Read Access Time Output Disable Time		tACC6 tOH6	CL=100pF	— 10	60 40	

11 Pin Configuration

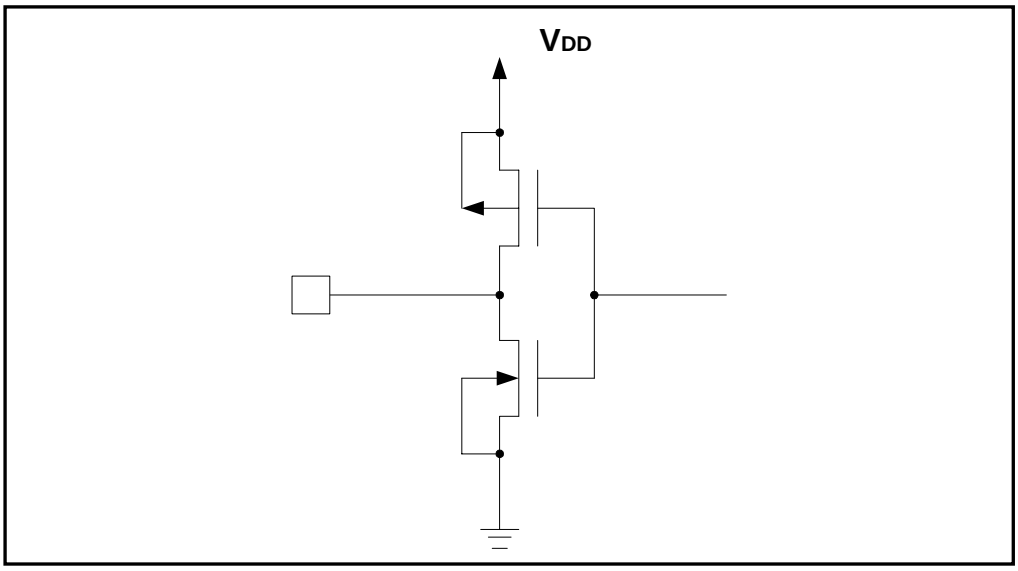
Input Pin Configuration



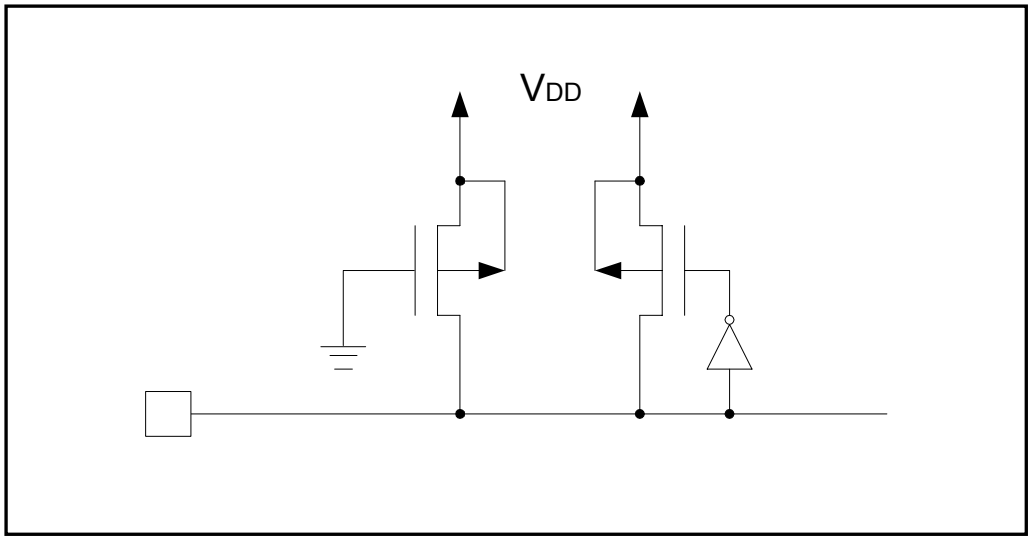
Input/Output Pin Configuration



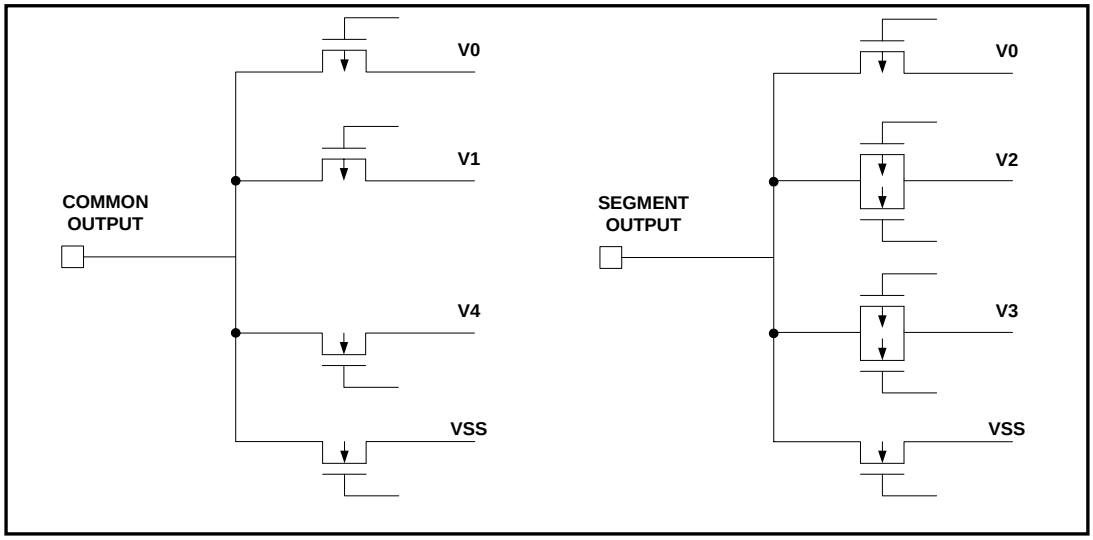
Output Pin Configuration



Reset Pin Configuration

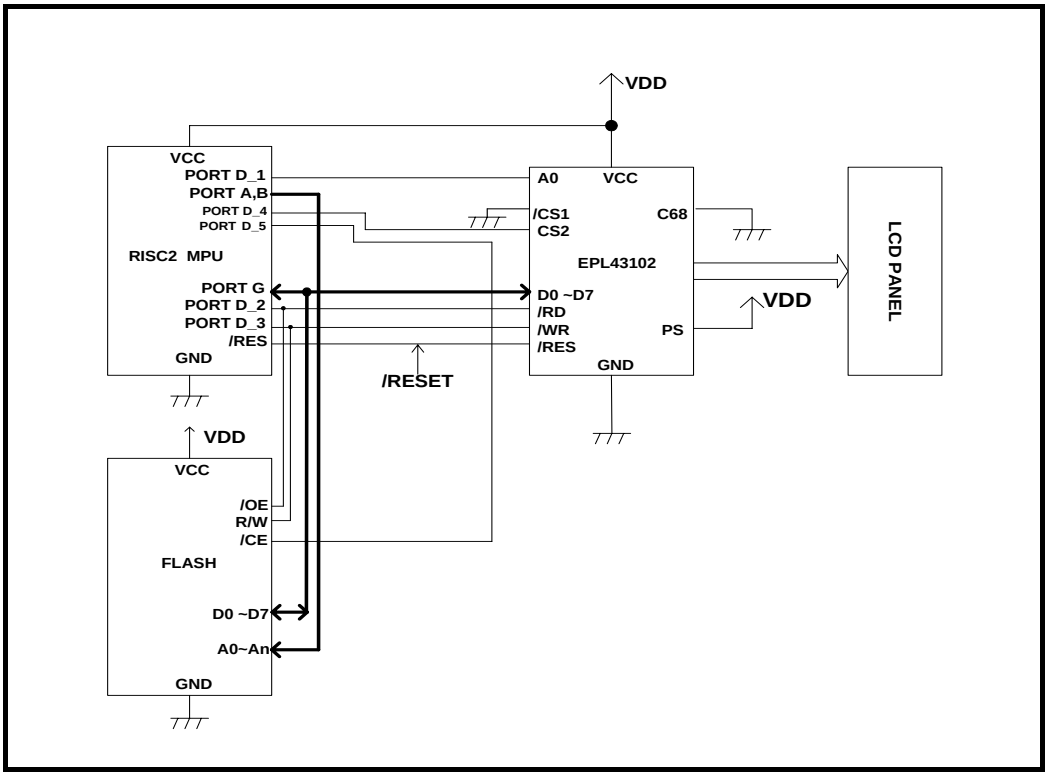


LCD Output Pin Configuration

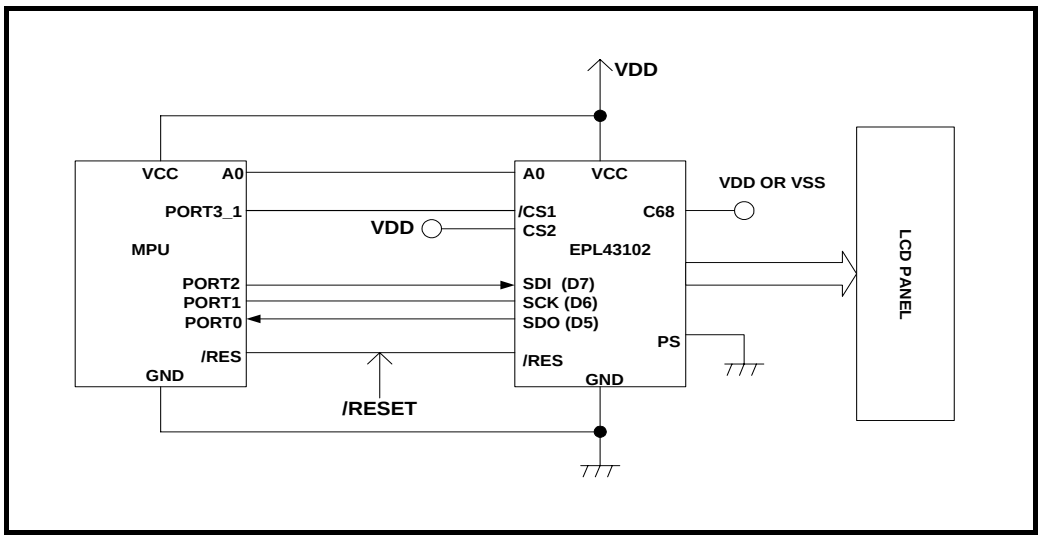


12 MPU Interface

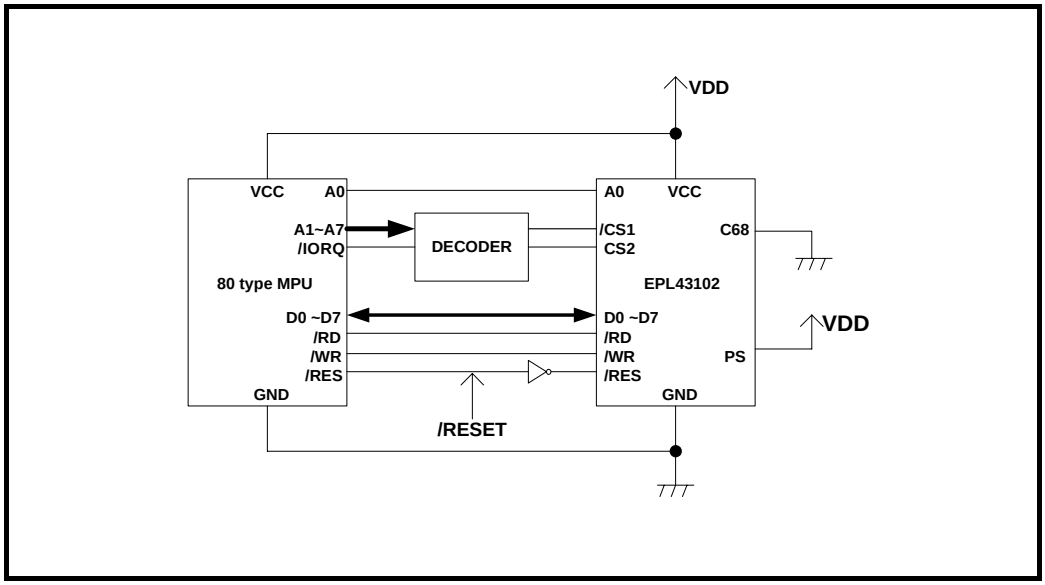
Elan 8-bit MPU (with external memory)



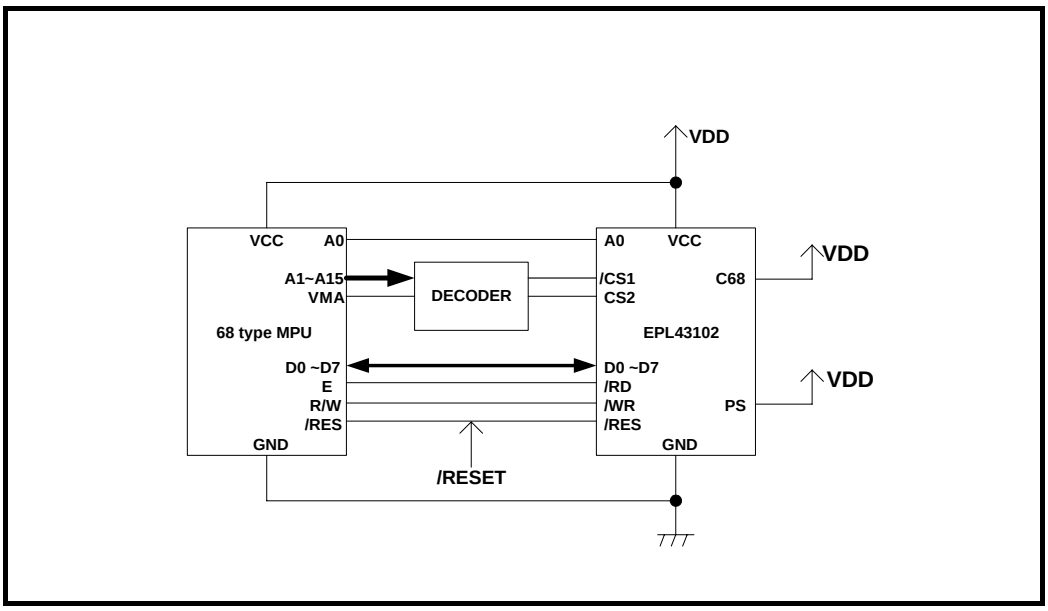
Serial Interface (SPI)



80-Family MPU



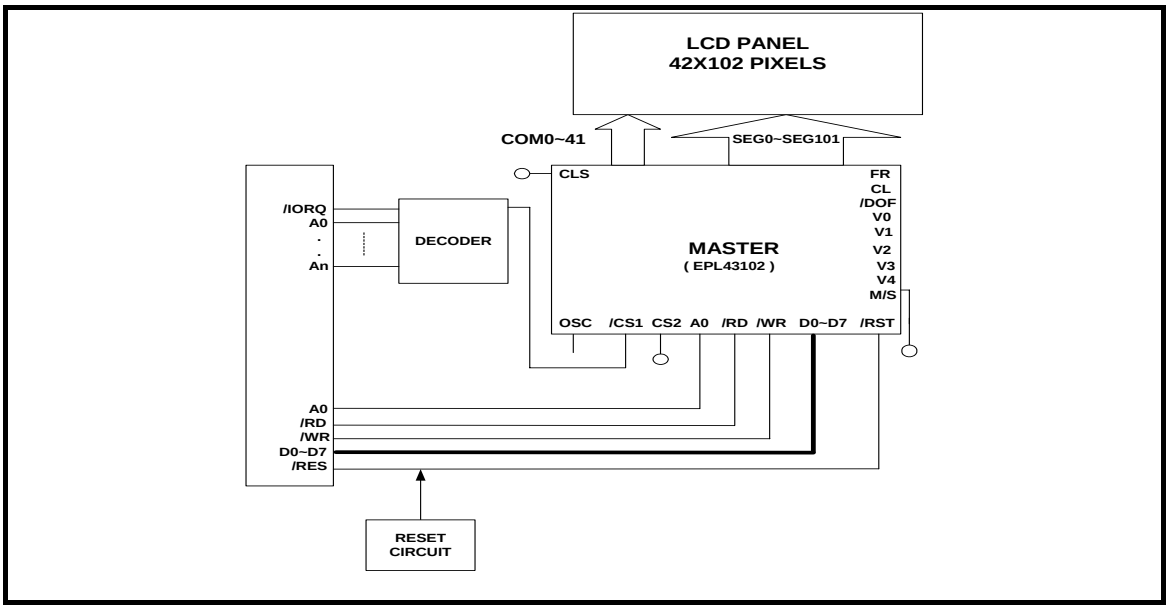
68-Family MPU



13 Application Circuits

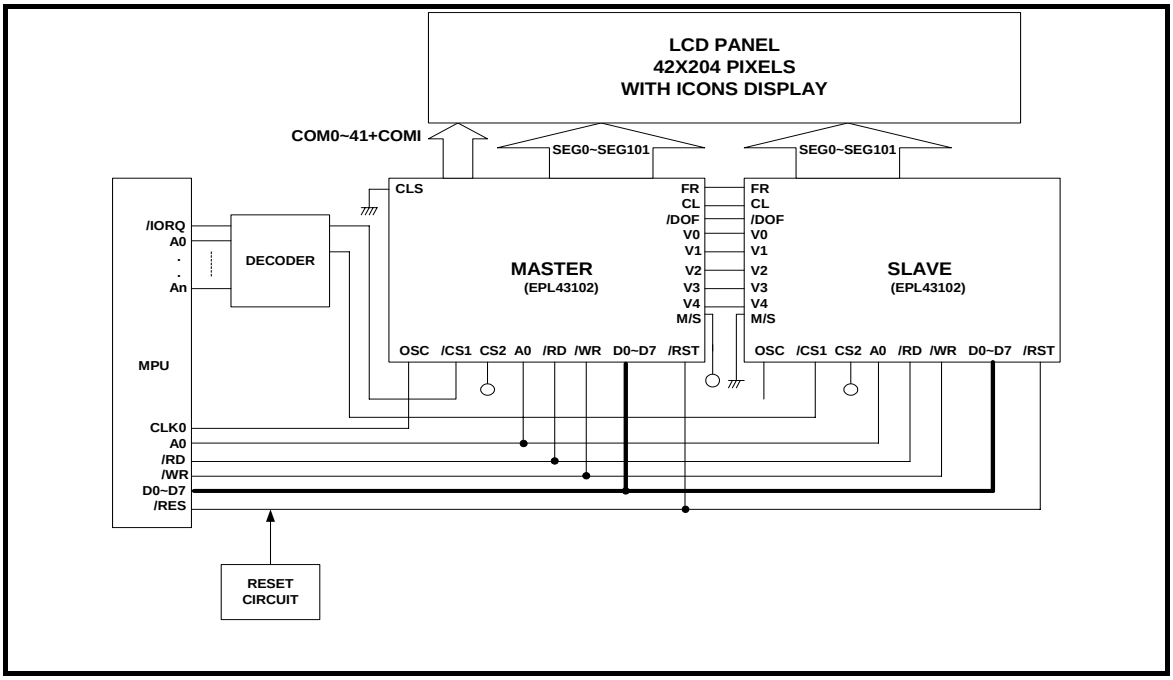
Example 1:

42×102 pixels driving application circuits ("Single-chip" using internal oscillator)

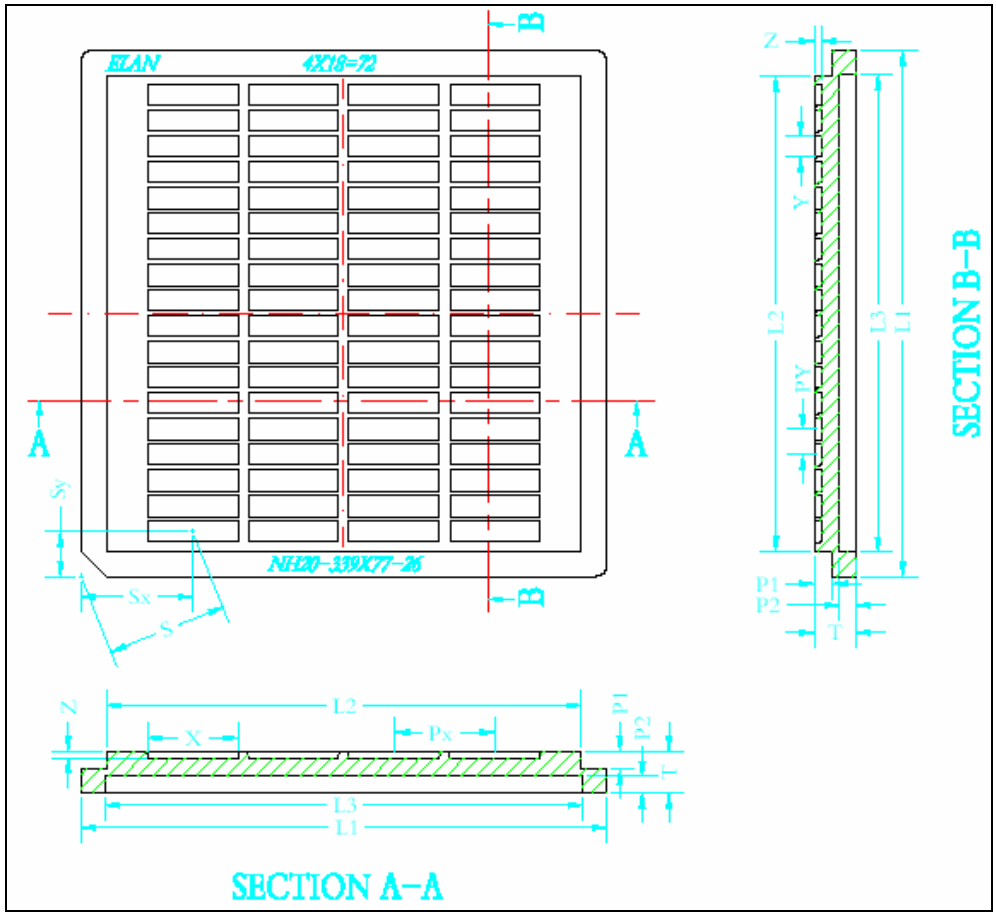


Example 2:

43×204 pixels driving application circuits ("Multi-chip" using external oscillator)



14 Tray Information



Tray Outline Dimensions

L1	50.80	Z	0.66
L2	45.40	Px	9.61
L3	45.80	Py	2.41
T	4.00	Nx	4
Sx	10.32	Ny	18
Sy	4.13	N	72
S	11.12	P1	1.76
X	8.61	P2	1.60
Y	1.96		

Unit: mm