EPL65132

65 COM / 132 SEG LCD Driver

Product Specification

DOC. VERSION 1.8

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Doc. Version	Revision Description	Date
0.1	Drafting version	2000/04/10
0.2	Initial version	2000/04/17
0.3	1. Modified the DC and AC characteristics. 2. Modified the “Select LCD bias” instruction. 3. Added “Set display clock frequency” instruction.	2000/05/15
0.4	1. Modified the error of voltage bias divider. 2. Modified the voltage follower block diagram.	2000/06/08
0.5	1. Added “Regulator resistor select register” in reset instruction. 2. Added Voltage converter capacitor connection. 3. Delete the busy state (without busy check). 4. Add DC current spec.	2000/09/15
0.6	1. Added one more VDD and VSS pad. 2. Modified the Pad sequence and configuration.	2001/03/02
0.7	1. Modified the operating temperature range: -30 to 80°C 2. Added program examples.	2001/09/07
0.8	1. Added “high power mode” instruction. 2. Modifed the pad and pitch size.	2001/10/30
0.9	Modified the Pad Coordinates.	2002/03/07
1.0	Modified the DC Characteristics: Reference voltage and Dynamic current consumption	2002/03/19
1.1	Added “LCD power on” sequence.	2002/03/28
1.2	1. Add at the DC characteristics: Regulated voltage 2. Added Pin Configuration.	2002/06/06
1.3	Added ELAN logo on the Pin Configuration.	2003/04/30
1.4	Modified the read timing of /WR.	2003/08/04
1.5	Adjusted the Data RAM arrangement.	2003/12/29
1.6	1. Modified the table on the relationship between duty ratio and common output. 2. Modified the A0 voltage level on the Display ON/OFF instruction.	2004/02/27
1.7	1. Added Notes after the Pad Coordinates table. 2. Modified the table on the Relationship between Duty Ratio and Common Output.	2004/08/19
1.8	1. Modified the TEST pin description. 2. Added V4 voltage range on the A.C. Characteristics table.	2006/01/12

1 General Description

The EPL65132 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It can be interfaced to the MPU via serial or 8-bit interface. It contains 65 common and 132 segment driver circuits. With one chip, it is possible to drive a graphic display system with a maximum of 132 × 65 dots.

2 Features

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM : 132 x 65 = 8580 bits
- 197 LCD Drivers : 132-seg segment drivers, 64-common drivers and 1-icon
- Serial Interface (SPI) or 8-Bit Parallel Interface Mode (80-series , 68-series MPU)
- On-chip oscillator circuit
- Multi-chip operation (Master, Slave) available
- Programmable Duty Ratio :

Duty ratio	Common	Segment
1: 64 (+ ICON)	64 (+ ICON)	132
1: 48 (+ ICON)	48 (+ ICON)	132
1: 42 (+ ICON)	42 (+ ICON)	132
1: 36 (+ ICON)	36 (+ ICON)	132
1: 32 (+ ICON)	32 (+ ICON)	132
1: 24 (+ ICON)	24 (+ ICON)	132
1: 16 (+ ICON)	16 (+ ICON)	132
1: 8 (+ ICON)	8 (+ ICON)	132

Note: ICON = "0" : Pin disable
ICON = "1" : Pin enable

- Selectable LCD driving bias level :
  1/4, 1/4.5, 1/5, 1/5.5, 1/6, 1/6.5, 1/7, 1/7.5, 1/8, 1/8.5, 1/9 bias
- Selectable LCD display clock frequency
- Electronic contrast control functions (64 steps)
- Built-in Instruction Set : Display data read/write, Display on/off, Inverse display, Page address set, Common address set, LCD display contrast control, Set Sleep mode, Standby mode, etc.
- Operating Voltage range :
  Supply voltage : 2.2V to 5.5 V
  LCD driving voltage : 4.0V to 15.0V

3 Applications

Organizer	Electronic Dictionary
Scientific calculator	Cellular phone
Graphic pager	Handy Terminals (PDA)

4 Pin Configurations

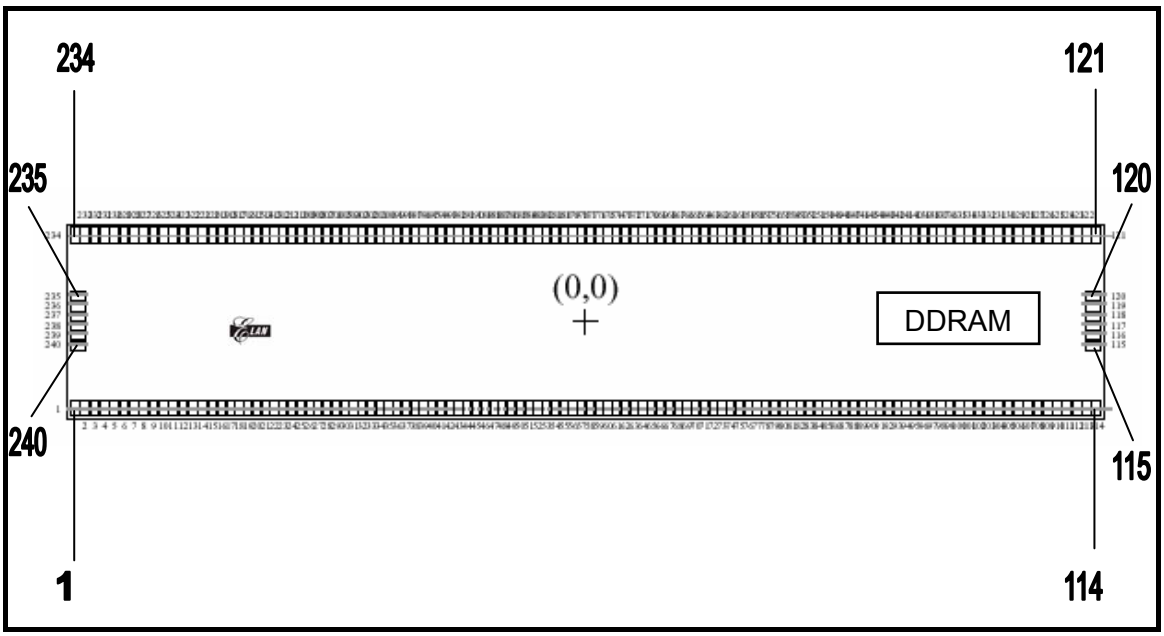


Figure 1 Pin Configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	10240	1820	um
Pad size (Type A)	001-015 100-114 115-120 121-135 220-234 235-240	85	100	
Pad size (Type B)	016-099 136-219	75	100	
Pad pitch	Type A	95		
	Type B	85		

4.1 Pad Coordinates

Pad No.	Symbol	X	Y
1	COM32	-4950.0	-782.5
2	COM33	-4855.0	-782.5
3	COM34	-4760.0	-782.5
4	COM35	-4665.0	-782.5
5	COM36	-4570.0	-782.5
6	COM37	-4475.0	-782.5
7	COM38	-4380.0	-782.5
8	COM39	-4285.0	-782.5
9	COM40	-4190.0	-782.5
10	COM41	-4095.0	-782.5
11	COM42	-4000.0	-782.5
12	COM43	-3905.0	-782.5
13	COM44	-3810.0	-782.5
14	COM45	-3715.0	-782.5
15	COM46	-3620.0	-782.5
16	COM47	-3530.0	-782.5
17	COM48	-3445.0	-782.5
18	COM49	-3360.0	-782.5
19	COM50	-3275.0	-782.5
20	COM51	-3190.0	-782.5
21	COM52	-3105.0	-782.5
22	COM53	-3020.0	-782.5
23	COM54	-2935.0	-782.5
24	COM55	-2850.0	-782.5
25	COM56	-2765.0	-782.5
26	COM57	-2680.0	-782.5
27	COM58	-2595.0	-782.5
28	COM59	-2510.0	-782.5
29	COM60	-2425.0	-782.5
30	COM61	-2340.0	-782.5
31	COM62	-2255.0	-782.5
32	COM63	-2170.0	-782.5
33	COMI1	-2085.0	-782.5
34	VDD	-2000.0	-782.5
35	VDD	-1915.0	-782.5
36	C1+	-1830.0	-782.5
37	C1-	-1745.0	-782.5
38	C3	-1660.0	-782.5
39	C4	-1575.0	-782.5
40	C2-	-1490.0	-782.5
41	C2+	-1405.0	-782.5
42	VOUT	-1320.0	-782.5
43	V0	-1235.0	-782.5
44	V1	-1150.0	-782.5
45	V2	-1065.0	-782.5
46	V3	-980.0	-782.5
47	V4	-895.0	-782.5
48	VR	-810.0	-782.5
49	GND	-725.0	-782.5
50	GND	-640.0	-782.5

Pad No.	Symbol	X	Y
51	MS	-555.0	-782.5
52	PS	-470.0	-782.5
53	FR	-385.0	-782.5
54	C86	-300.0	-782.5
55	/DOF	-215.0	-782.5
56	CLS	-130.0	-782.5
57	CL	-45.0	-782.5
58	OSC	40.0	-782.5
59	FRS	125.0	-782.5
60	IRS	210.0	-782.5
61	/RES	295.0	-782.5
62	D7	380.0	-782.5
63	D6	465.0	-782.5
64	D5	550.0	-782.5
65	D4	635.0	-782.5
66	D3	720.0	-782.5
67	D2	805.0	-782.5
68	D1	890.0	-782.5
69	D0	975.0	-782.5
70	CS2	1060.0	-782.5
71	/CS1	1145.0	-782.5
72	A0	1230.0	-782.5
73	/WR	1315.0	-782.5
74	/RD	1400.0	-782.5
75	TEST	1485.0	-782.5
76	COM31	1570.0	-782.5
77	COM30	1655.0	-782.5
78	COM29	1740.0	-782.5
79	COM28	1825.0	-782.5
80	COM27	1910.0	-782.5
81	COM26	1995.0	-782.5
82	COM25	2080.0	-782.5
83	COM24	2165.0	-782.5
84	COM23	2250.0	-782.5
85	COM22	2335.0	-782.5
86	COM21	2420.0	-782.5
87	COM20	2505.0	-782.5
88	COM19	2590.0	-782.5
89	COM18	2675.0	-782.5
90	COM17	2760.0	-782.5
91	COM16	2845.0	-782.5
92	COM15	2930.0	-782.5
93	COM14	3015.0	-782.5
94	COM13	3100.0	-782.5
95	COM12	3185.0	-782.5
96	COM11	3270.0	-782.5
97	COM10	3355.0	-782.5
98	COM9	3440.0	-782.5
99	COM8	3525.0	-782.5
100	COM7	3615.0	-782.5

Pad No.	Symbol	X	Y
101	COM6	3710.0	-782.5
102	COM5	3805.0	-782.5
103	COM4	3900.0	-782.5
104	COM3	3995.0	-782.5
105	COM2	4090.0	-782.5
106	COM1	4185.0	-782.5
107	COM0	4280.0	-782.5
108	COMI2	4375.0	-782.5
109	SEG131	4470.0	-782.5
110	SEG130	4565.0	-782.5
111	SEG129	4660.0	-782.5
112	SEG128	4755.0	-782.5
113	SEG127	4850.0	-782.5
114	SEG126	4945.0	-782.5
115	SEG125	4992.5	-241.1
116	SEG124	4992.5	-146.1
117	SEG123	4992.5	-51.1
118	SEG122	4992.5	43.9
119	SEG121	4992.5	138.9
120	SEG120	4992.5	233.9
121	SEG119	4945.0	782.5
122	SEG118	4850.0	782.5
123	SEG117	4755.0	782.5
124	SEG116	4660.0	782.5
125	SEG115	4565.0	782.5
126	SEG114	4470.0	782.5
127	SEG113	4375.0	782.5
128	SEG112	4280.0	782.5
129	SEG111	4185.0	782.5
130	SEG110	4090.0	782.5
131	SEG109	3995.0	782.5
132	SEG108	3900.0	782.5
133	SEG107	3805.0	782.5
134	SEG106	3710.0	782.5
135	SEG105	3615.0	782.5
136	SEG104	3525.0	782.5
137	SEG103	3440.0	782.5
138	SEG102	3355.0	782.5
139	SEG101	3270.0	782.5
140	SEG100	3185.0	782.5
141	SEG99	3100.0	782.5
142	SEG98	3015.0	782.5
143	SEG97	2930.0	782.5
144	SEG96	2845.0	782.5
145	SEG95	2760.0	782.5
146	SEG94	2675.0	782.5
147	SEG93	2590.0	782.5
148	SEG92	2505.0	782.5
149	SEG91	2420.0	782.5
150	SEG90	2335.0	782.5

Pad No.	Symbol	X	Y
151	SEG89	2250.0	782.5
152	SEG88	2165.0	782.5
153	SEG87	2080.0	782.5
154	SEG86	1995.0	782.5
155	SEG85	1910.0	782.5
156	SEG84	1825.0	782.5
157	SEG83	1740.0	782.5
158	SEG82	1655.0	782.5
159	SEG81	1570.0	782.5
160	SEG80	1485.0	782.5
161	SEG79	1400.0	782.5
162	SEG78	1315.0	782.5
163	SEG77	1230.0	782.5
164	SEG76	1145.0	782.5
165	SEG75	1060.0	782.5
166	SEG74	975.0	782.5
167	SEG73	890.0	782.5
168	SEG72	805.0	782.5
169	SEG71	720.0	782.5
170	SEG70	635.0	782.5
171	SEG69	550.0	782.5
172	SEG68	465.0	782.5
173	SEG67	380.0	782.5
174	SEG66	295.0	782.5
175	SEG65	210.0	782.5
176	SEG64	125.0	782.5
177	SEG63	40.0	782.5
178	SEG62	-45.0	782.5
179	SEG61	-130.0	782.5
180	SEG60	-215.0	782.5
181	SEG59	-300.0	782.5
182	SEG58	-385.0	782.5
183	SEG57	-470.0	782.5
184	SEG56	-555.0	782.5
185	SEG55	-640.0	782.5
186	SEG54	-725.0	782.5
187	SEG53	-810.0	782.5
188	SEG52	-895.0	782.5
189	SEG51	-980.0	782.5
190	SEG50	-1065.0	782.5
191	SEG49	-1150.0	782.5
192	SEG48	-1235.0	782.5
193	SEG47	-1320.0	782.5
194	SEG46	-1405.0	782.5
195	SEG45	-1490.0	782.5
196	SEG44	-1575.0	782.5
197	SEG43	-1660.0	782.5
198	SEG42	-1745.0	782.5
199	SEG41	-1830.0	782.5
200	SEG40	-1915.0	782.5

Pad No.	Symbol	X	Y
201	SEG39	-2000.0	782.5
202	SEG38	-2085.0	782.5
203	SEG37	-2170.0	782.5
204	SEG36	-2255.0	782.5
205	SEG35	-2340.0	782.5
206	SEG34	-2425.0	782.5
207	SEG33	-2510.0	782.5
208	SEG32	-2595.0	782.5
209	SEG31	-2680.0	782.5
210	SEG30	-2765.0	782.5
211	SEG29	-2850.0	782.5
212	SEG28	-2935.0	782.5
213	SEG27	-3020.0	782.5
214	SEG26	-3105.0	782.5
215	SEG25	-3190.0	782.5
216	SEG24	-3275.0	782.5
217	SEG23	-3360.0	782.5
218	SEG22	-3445.0	782.5
219	SEG21	-3530.0	782.5
220	SEG20	-3620.0	782.5
221	SEG19	-3715.0	782.5
222	SEG18	-3810.0	782.5
223	SEG17	-3905.0	782.5
224	SEG16	-4000.0	782.5
225	SEG15	-4095.0	782.5
226	SEG14	-4190.0	782.5
227	SEG13	-4285.0	782.5
228	SEG12	-4380.0	782.5
229	SEG11	-4475.0	782.5
230	SEG10	-4570.0	782.5
231	SEG9	-4665.0	782.5
232	SEG8	-4760.0	782.5
233	SEG7	-4855.0	782.5
234	SEG6	-4950.0	782.5
235	SEG5	-4992.5	233.9
236	SEG4	-4992.5	138.9
237	SEG3	-4992.5	43.9
238	SEG2	-4992.5	-51.1
239	SEG1	-4992.5	-146.1
240	SEG0	-4992.5	-241.1

Note: For PCB layout, the IC substrate must be connected to VSS or floating.
Refer to the relationship between Duty Ratio and Common Output.

5 Block Diagram

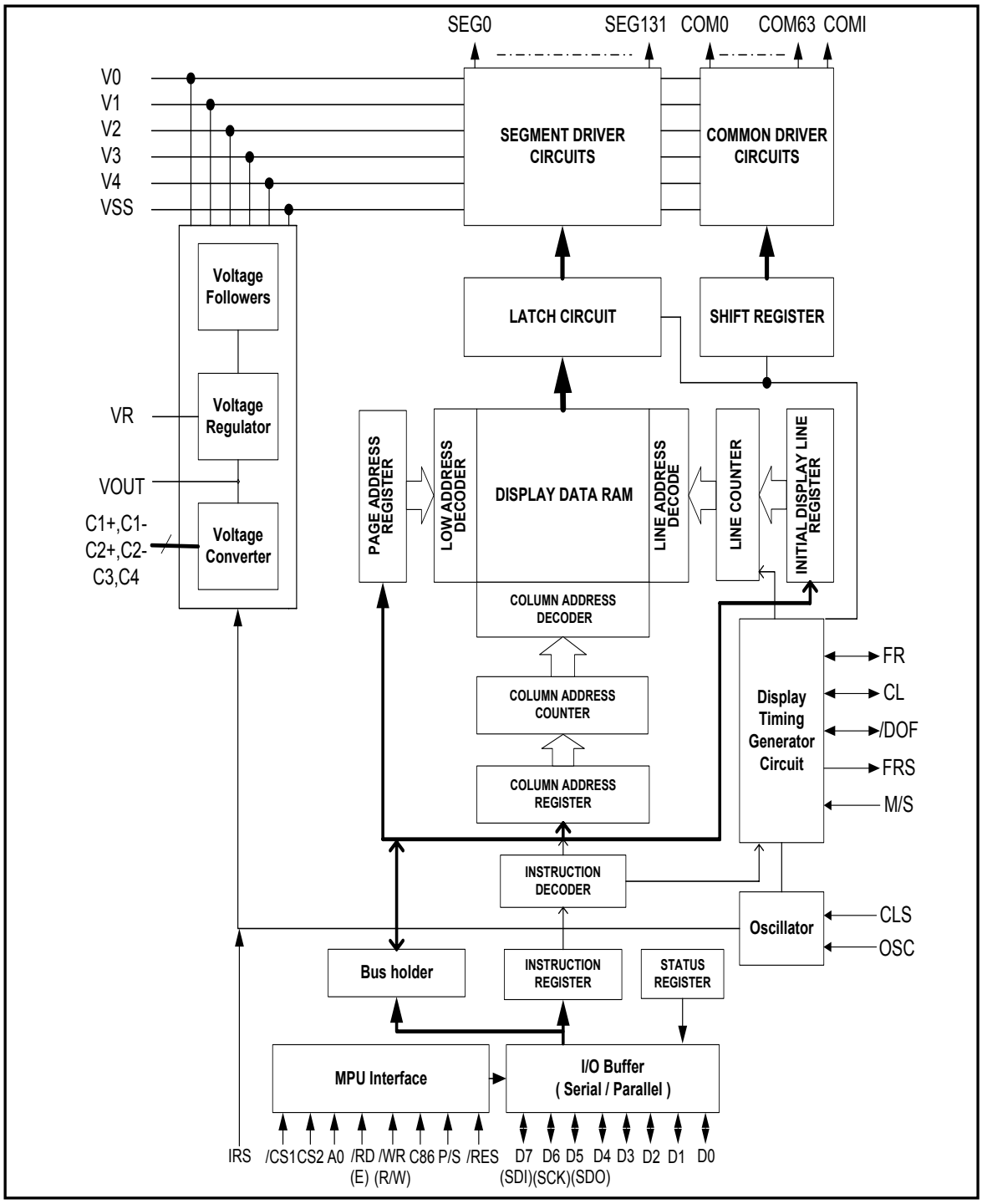


Figure 2 System Block Diagram

6 Pin Description

6.1 Power Supply

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Power</td><td>VDD Power Supply</td></tr>
<tr><td>VSS</td><td>Power</td><td>0V (GND)</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>Power</td><td>LCD driver supply voltages. The voltage applied is determined by the LCD pixel and is changed through changing the impedance using an operational amplifier (OPA) for various applications. Voltage levels are determined based on V0, and must maintain the relative magnitudes shown below:
V0≧V1≧V2≧V3≧V4≧Vss
When the internal power circuit is active, these voltages are generated according to the state of the LCD bias, The selection of voltages is determined by the “LCD bias select” instruction, as shown in the table below.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/9 Bias</td><td>(8/9) × V0</td><td>(7/9) × V0</td><td>(2/9) × V0</td><td>(1/9) × V0</td></tr>
<tr><td>1/8.5 Bias</td><td>(7.5/8.5) × V0</td><td>(6.5/8.5) × V0</td><td>(2/8.5) × V0</td><td>(1/8.5) × V0</td></tr>
<tr><td>1/8 Bias</td><td>(7/8) × V0</td><td>(6/8) × V0</td><td>(2/8) × V0</td><td>(1/8) × V0</td></tr>
<tr><td>1/7.5 Bias</td><td>(6.5/7.5) × V0</td><td>(5.5/7.5) × V0</td><td>(2/7.5) × V0</td><td>(1/7.5) × V0</td></tr>
<tr><td>1/7 Bias</td><td>(6/7) × V0</td><td>(5/7) × V0</td><td>(2/7) × V0</td><td>(1/7) × V0</td></tr>
<tr><td>1/6.5 Bias</td><td>(5.5/6.5) × V0</td><td>(4.5/6.5) × V0</td><td>(2/6.5) × V0</td><td>(1/6.5) × V0</td></tr>
<tr><td>1/6 Bias</td><td>(5/6) × V0</td><td>(4/6) × V0</td><td>(2/6) × V0</td><td>(1/6) × V0</td></tr>
<tr><td>1/5.5 Bias</td><td>(4.5/5.5) × V0</td><td>(3.5/5.5) × V0</td><td>(2/5.5) × V0</td><td>(1/5.5) × V0</td></tr>
<tr><td>1/5 Bias</td><td>(4/5) × V0</td><td>(3/5) × V0</td><td>(2/5) × V0</td><td>(1/5) × V0</td></tr>
<tr><td>1/4.5 Bias</td><td>(3.5/4.5) × V0</td><td>(2.5/4.5) × V0</td><td>(2/4.5) × V0</td><td>(1/4.5) × V0</td></tr>
<tr><td>1/4 Bias</td><td>(3/4) × V0</td><td>(2/4) × V0</td><td>(2/4) × V0</td><td>(1/4) × V0</td></tr>
</table>
</td></tr>
</table>

6.2 LCD Driver Supply

Name	I/O	Description
C1+ C1-	O	Boosted capacitor connecting terminals used for voltage booster.
C2+ C2-	O	Boosted capacitor connecting terminals used for voltage booster.
C3 C4	O	Boosted capacitor connecting terminals used for voltage booster.
VOUT	I/O	Voltage converter output
VR	I	V0 voltage adjustment pin.

6.3 System Control

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>M/S</td><td>I</td><td>Master/slave operation select pin.
- MS = "H": Master operation
- MS = "L": Slave operation

<table>
<tr><th>M/S</th><th>CLS</th><th>OSC.</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>/DOF</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Available</td><td>Available</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>“L”</td><td>Unavailable</td><td>Available</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td>“L”</td><td>*</td><td>Unavailable</td><td>Unavailable</td><td>I</td><td>I</td><td>Hi-Z</td><td>I</td></tr>
</table>
Note: * : Don’t Care
O : Output
I : Input</td></tr>
<tr><td>P/S</td><td>I</td><td>Select Interface mode of the MPU.
When PS = "High": Parallel interface mode
When PS = "Low": Serial interface mode</td></tr>
<tr><td>FR</td><td>I/O</td><td>LCD AC signal input/output pin
When is used in master/slave mode (multi-chip), the FR pins must be connected each other.
- MS = “H”: Output
- MS = “L”: Input</td></tr>
<tr><td>C68</td><td>I</td><td>Select the kind of MPU interface.
When C68 = "High": 68-series MPU interface mode
When C68 = "Low": 80-series MPU interface</td></tr>
<tr><td>/DOF</td><td>I/O</td><td>LCD Display blanking control pin. In multi-chip mode, the /DOF pin must be connected to each other.
M/S = ”H” (Master) : /DOF is output pin
→ Display “On” = “H”, Display “Off” = “L”
M/S = ”L” (Slave) : /DOF is input pin
→ Via external control. Refer to the following table.

<table>
<tr><th rowspan="2">Instruction</th><th colspan="2">/DOF</th></tr>
<tr><th>H</th><th>L</th></tr>
<tr><td>Display “On”</td><td>On</td><td>Off</td></tr>
<tr><td>Display “Off”</td><td>Off</td><td>Off</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Internal oscillator circuit enable / disable select pin.
CLS = “H”: Internal oscillator circuit is enable
CLS = “L”: Internal oscillator circuit is disable
(External display clock input to OSC pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
When the EPL65132 is used in master/slave mode (multi-chip), the CL pins must be connected to each other.

<table>
<tr><th>M/S</th><th>CL</th></tr>
<tr><td>“H”</td><td>Output</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
</table></td></tr>
</table>

Name	I/O	Description
OSC	I	When using an external oscillator, input the clock to OSC pin. When using an internal oscillator, leave this pin open.
FRS	O	Static driver output pin. This pin is used in combination with the FR pin.
IRS	I	Internal resistor select pin. This pin selects the resistors for adjusting V0 voltage level and is available only in master mode. - IRS = "H": The internal resistors are used. - IRS = "L": The external resistors are used. V0 voltage is controlled using the external divider resistor connected to the VR pin.
TEST	I	Test pin. Fixed at VSS.

6.4 MPU Interface

Name	I/O	Description
/RES	I	Hardware reset input. The LSI is reset when this signal is pulled low. (Active low)
/CS1,CS2	I	These are the chip select signals. The Chip Select of the LSI becomes active when CS1 is "L" and also CS2 is "H" and allows the input/output of data or commands.

/CS1	CS2	Status
“L”	“L”	The device is not active. (D7~D0 is Hi-Z)
“L”	“H”	Data and instruction are available.
“H”	“L”	The device is not active. (D7~D0 is Hi-Z)
“H”	“H”	The device is not active. (D7~D0 is Hi-Z)

A0	I	Used as register selection input. When A0 = "High", Data register. When A0 = "Low", Instruction register.
/WR (R/W)	I	When C68 = "High" (68-series MPU interfacing), used as read (/WR = "High"), write (/WR = "Low") When C68 = "Low" (80-series MPU interfacing), used as write enable input (/WR).
/RD (E)	I	When C68 = "High" (68-series MPU interfacing), used as read/write enable input (E). When C68 = "Low" (80-series MPU interfacing), used as read enable input (/RD).
D0 to D7	I/O	When in serial mode, D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin and the others are not used. When in parallel mode, D0 to D7 are used as bi-directional data bus pin.

6.5 LCD Driver Output

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>COM0 to COM63</td><td>O</td><td>The LCD common output pins.
<table>
<tr><th>Scan Data</th><th>FR</th><th>COMs Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Vss</td></tr>
<tr><td>L</td><td>V0</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power Save Mode</td><td>Vss</td></tr>
</table></td></tr>
<tr><td>COMI</td><td>O</td><td>These are two icon display pins. Both pins output the same signal. Leave these pins open when they are not used.</td></tr>
<tr><td>SEG0 to SEG131</td><td>O</td><td>The LCD segment output pins.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">FR</th><th colspan="2">SEGs Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power Saving Mode</td><td colspan="2">Vss</td></tr>
</table></td></tr>
</table>

Refer to the relationship between Duty Ratio and Common Output.

7 Function Description

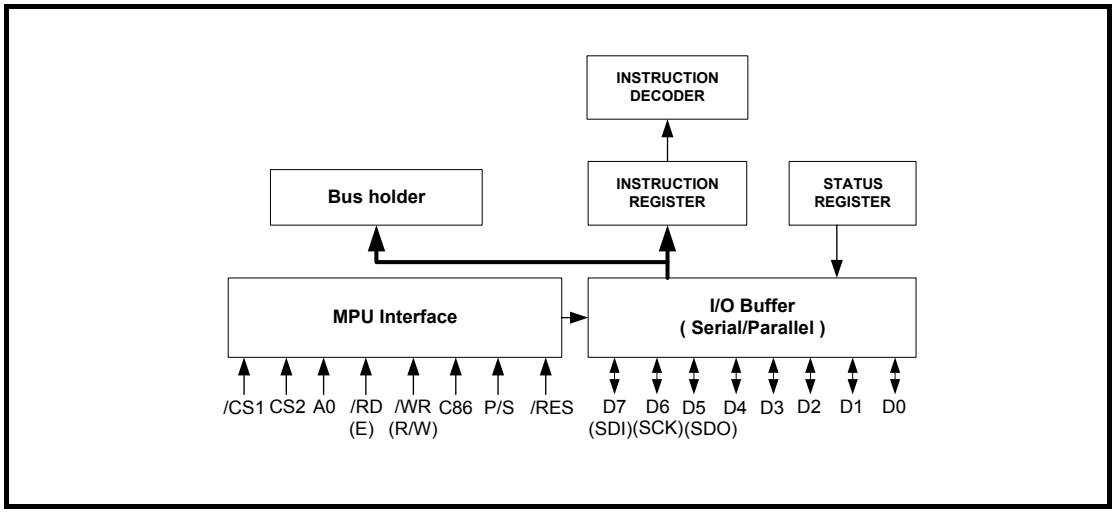


Figure 3 System Interface

7.1 MPU Interface

7.1.1 Chip Select

The EPL65132 has two chip select pins /CS1 and CS2. When /CS1="L" and CS2="H", MPU interface is available. When the chip select pin is inactive (other /CS1 and CS2 condition), D7 to D0 are high impedance (invalid) and input of A0, /RD, or /WR inputs are not effective. If serial interface is selected, the shift register and counter are both reset. However, reset is always operated in any conditions of /CS1 and CS2.

P/S	C68	A0	/WR	/RD	D0~D4	D5	D6	D7
Serial Mode (L)	SPI interface (–)	A0	R/W	-	*	SDO	SCK	SDI
Parallel mode (H)	80-series (L)	A0	/WR	/RD	D0~D7			
	68-series (H)	A0	R/W	E	D0~D7			

Note: " * " Don't care ("High", "Low" or "Open")

"–" Indicates that it is fixed to either "High" (VDD) or "Low" (VSS)

7.1.2 Selecting the Interface Type

The EPL65132 can be operated with serial interface (SPI) and parallel interface (80-series or 68-series) as selected by the P/S pin.

Serial Interface (SPI)

When serial mode (PS = "L"), D6 (SCK) is used as serial clock input pin, D7 (SDI) is used as serial data input pin, D5 (SDO) is used as serial data output pin. When the LSI is active (/CS1="L", CS2="H"), serial data input (D7), serial clock input (D6) inputs and serial data output (D5) are enabled. The 8-bit shift register and 3-bit counter are reset to the initial condition when the chip is not selected. The data input/output from SDI/SDO terminal is MSB first as in the order of D7, D6…D0, and is latched at the rising edge of the serial clock SCK. Serial input data is display data when A0="H" and instruction when A0="L". The A0 input is read and identified at the rising edge of the (8 × n) serial clock pulse. Since the clock signal (D6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

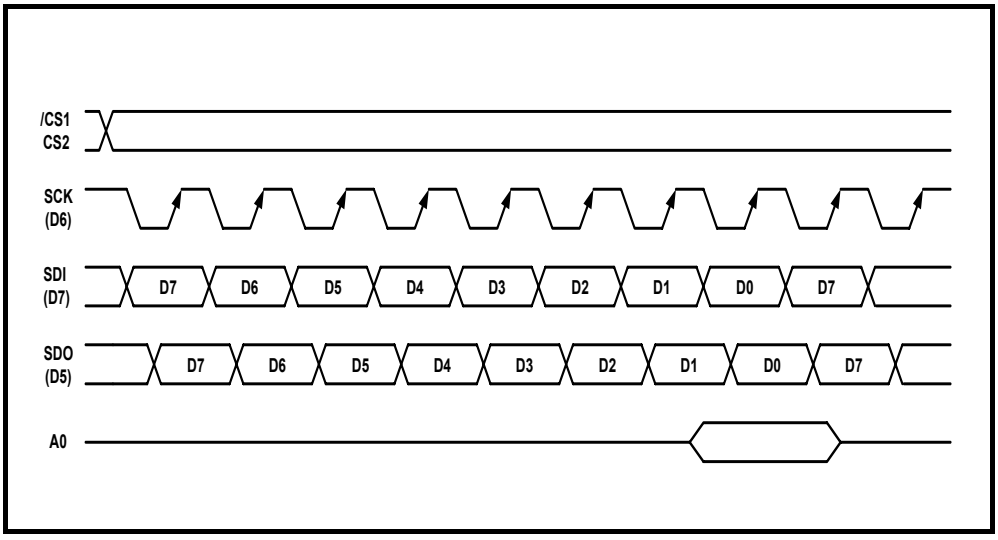


Figure 4 Serial Interface Signal Chart

A0	/WR (R/W)	D7 (SDI)	D5 (SDO)
0	0	Instruction Write	Status Read
0	1	Invalid	Status Read
1	0	Display Data Write	Status Read
1	1	Invalid	Display Data Read

Parallel Interface (8-bit Length)

Parallel mode (8-bit length): When parallel input is selected (PS = ”H”), D0~D7 can be connected directly to the 80-series or 68-series MPU by setting the C86 pin to high or low.

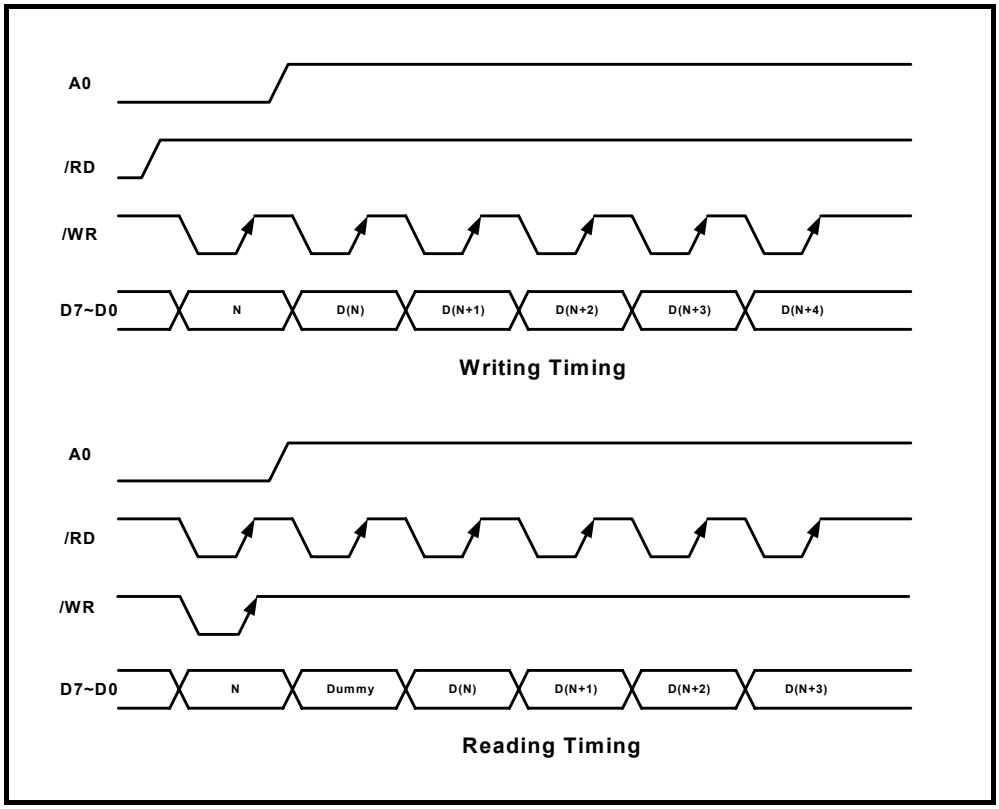


Figure 5 Write and Read Timing Diagrams

Common	80-Series		68-Series	Description
A0	/RD	/WR	R/W	
H	L	H	H	Display data read
H	H	L	L	Display data write
L	L	H	H	Register status read
L	H	L	L	Writes to Instruction register

7.2 Data Transfer

The EPL65132 uses a bus holder and an internal data bus for data transfer with MPU. When writing data from the MPU to the DDRAM, data is automatically transferred from the bus holder to the DDRAM. When reading data from the DDRAM to MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and MPU reads this stored data from bus holder for the next data read cycle.

7.2.1 Display Data RAM

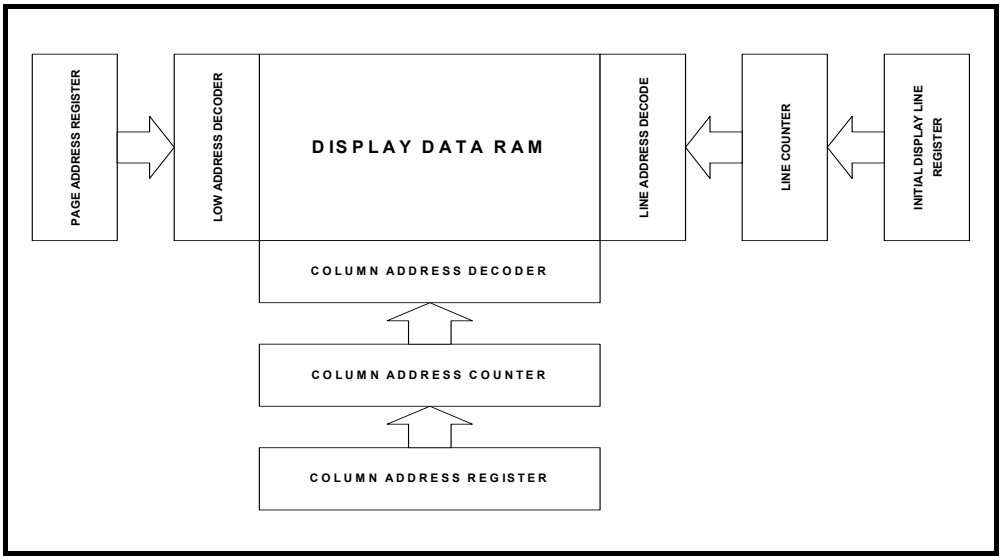


Figure 6 Display Data RAM Diagram

The display data RAM (DDRAM) stores pixel data for the LCD. It is a 65-row ((8-page × 8-bit + 1) x 132-column addressable array. It is possible to access any required bit by specifying the page address and the column address. The 65 rows are divided into 8 pages of 8 lines and the ninth page with a single line (D0 only).

Each bit in the Display Data RAM corresponds to each pixel of the LCD panel. Each bit in the Display Data RAM corresponds to each pixel of the LCD panel and controls the display by applying the following bit data.

When in Normal Display : On="1" , Off="0"

When in Inverse Display : On="0" , Off="1"

(Refer to the “Inverse Display On/Off” instruction for more details.)

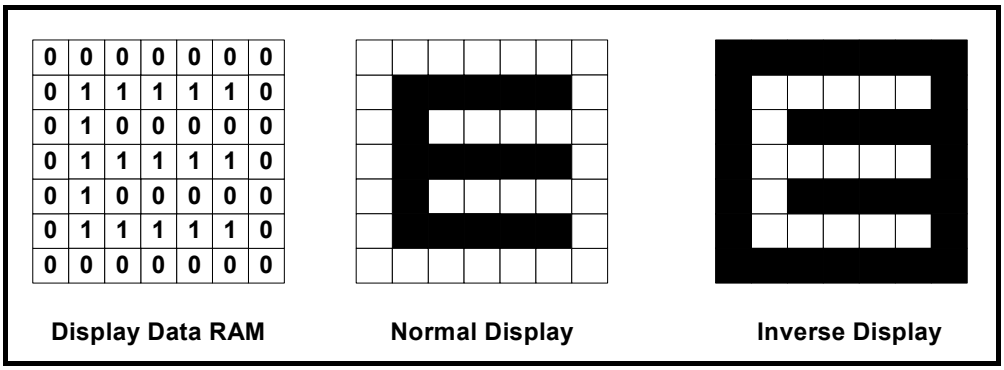


Figure 7 Display Data RAM, Normal and Inverse Liquid Crystal Display Diagrams

The microprocessor (MPU) can read from and write to the RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into the RAM at the same time as data is being displayed without causing the LCD to flicker.

Page Address P3, P2, P1, P0				Data	Column Address								Line Address (HEX)	Common Output (1/65,1/64)	Common Output (1/49,1/48)	Common Output (1/42,1/36)	Common Output (1/33,1/32)
0	0	0	0	D0				Page 0					00	COM0	COM0	COM0	COM0
				D1									01	COM1	COM1	COM1	COM1
				D2									02	COM2	COM2	COM2	COM2
				D3									03	COM3	COM3	COM3	COM3
				D4									04	COM4	COM4	COM4	COM4
				D5									05	COM5	COM5	COM5	COM5
				D6									06	COM6	COM6	COM6	COM6
				D7									07	COM7	COM7	COM7	COM7
0	0	0	1	D0				Page 1					08	COM8	COM8	COM8	COM8
				D1									09	COM9	COM9	COM9	COM9
				D2									0A	COM10	COM10	COM10	COM10
				D3									0B	COM11	COM11	COM11	COM11
				D4									0C	COM12	COM12	COM12	COM12
				D5									0D	COM13	COM13	COM13	COM13
				D6									0E	COM14	COM14	COM14	COM14
				D7									0F	COM15	COM15	COM15	COM15
0	0	1	0	D0				Page 2					10	COM16	COM16	COM16	COM16
				D1									11	COM17	COM17	COM17	COM17
				D2									12	COM18	COM18	COM18	COM18
				D3									13	COM19	COM19	COM19	COM19
				D4									14	COM20	COM20	COM20	COM20
				D5									15	COM21	COM21	COM21	COM21
				D6									16	COM22	COM22	COM22	COM22
				D7									17	COM23	COM23	COM23	COM23
0	0	1	1	D0				Page 3					18	COM24	COM24	COM24	COM24
				D1									19	COM25	COM25	COM25	COM25
				D2									1A	COM26	COM26	COM26	COM26
				D3									1B	COM27	COM27	COM27	COM27
				D4									1C	COM28	COM28	COM28	COM28
				D5									1D	COM29	COM29	COM29	COM29
				D6									1E	COM30	COM30	COM30	COM30
				D7									1F	COM31	COM31	COM31	COM31
0	1	0	0	D0				Page 4					20	COM32	COM32	COM32	
				D1									21	COM33	COM33	COM33	
				D2									22	COM34	COM34	COM34	
				D3									23	COM35	COM35	COM35	
				D4									24	COM36	COM36	COM36	
				D5									25	COM37	COM37	COM37	
				D6									26	COM38	COM38	COM38	
				D7									27	COM39	COM39	COM39	
0	1	0	1	D0				Page 5					28	COM40	COM40	COM40	
				D1									29	COM41	COM41	COM41	
				D2									2A	COM42	COM42		
				D3									2B	COM43	COM43		
				D4									2C	COM44	COM44		
				D5									2D	COM45	COM45		
				D6									2E	COM46	COM46		
				D7									2F	COM47	COM47		

Page Address P3, P2, P1, P0				Data	Column Address								Line Address (HEX)	Common Output (1/65,1/64)	Common Output (1/49,1/48)	Common Output (1/42,1/36)	Common Output (1/33,1/32)
0	1	1	0	D0				Page 6					30	COM48			
				D1									31	COM49			
				D2									32	COM50			
				D3									33	COM51			
				D4									34	COM52			
				D5									35	COM53			
				D6									36	COM54			
				D7									37	COM55			
0	1	1	1	D0				Page 7					38	COM56			
				D1									39	COM57			
				D2									3A	COM58			
				D3									3B	COM59			
				D4									3C	COM60			
				D5									3D	COM61			
				D6									3E	COM62			
				D7									3F	COM63			
1	0	0	0	D0				Page 8						COMI	COMI		COMI
Column Address(HEX)				ADC =0	00	01	02	- - - - - - - - -	80	81	82	83					
				ADC =1	83	82	81	- - - - - - - - -	03	02	01	00					
LCD Output					SEG0	SEG1	SEG2	- - - - - - - - -	SEG128	SEG129	SEG130	SEG131					

7.2.2 Programmable Duty Ratio

The duty ratio is selected by using the “Set Duty Ratio” instruction.
The common output circuits are shown in the following figure. They are separated into three shift registers and controlled by the "duty ratio register".

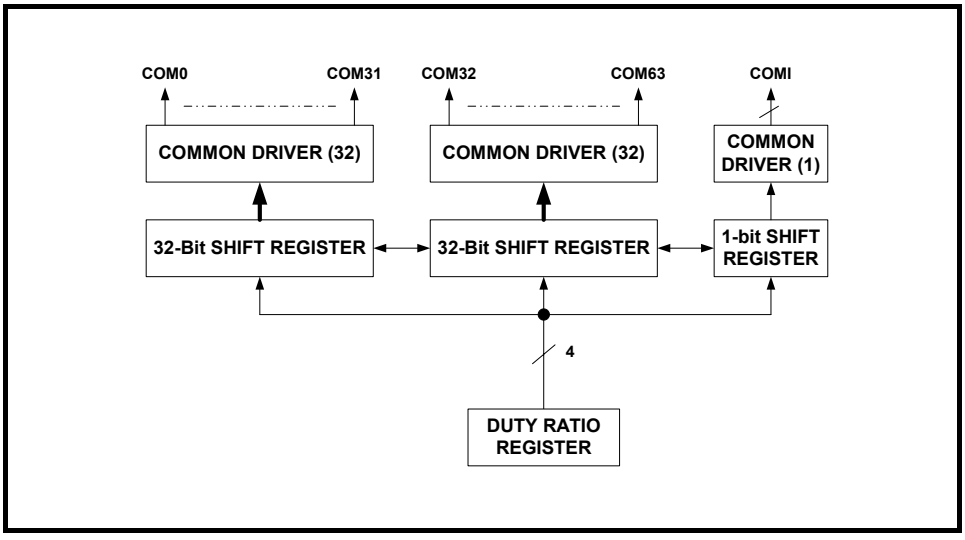


Figure 8 Common Output Circuits

Duty	SHL		Common Output Pins (COMxx, refer to the Pad No.)														
			COM0 ~ 3	~7	~11	~15	~17	~20	~23	~	40~	43~	46~	48~	52~	56~	COM60 ~ 63	COMI
1/9 1/8	0	Line Address (Pages 0~7)	CCOM[0..3]														CCOM[4..7]	COMI
	1		CCOM[7..4]														CCOM[3..0]	–
1/17 1/16	0		CCOM[0..7]													CCOM[8..15]		COMI
	1		CCOM[15..8]													CCOM[7..0]		–
1/25 1/24	0		CCOM[0..11]												CCOM[12..23]			COMI
	1		CCOM[23..12]												CCOM[11..0]			–
1/33 1/32	0		CCOM[0..15]											CCOM[16..31]				COMI
	1		CCOM[31..16]											CCOM[15..0]				–
1/37 1/36	0		CCOM[0..17]										CCOM[18..35]					COMI
	1		CCOM[35..18]										CCOM[17..0]					–
1/43 1/42	0		CCOM[0…20]									CCOM[21…41]						COMI
	1		COM[41…21]									CCOM[20…0]						–
1/49 1/48	0		CCOM[0…23]								CCOM[24…47]							COMI
	1		CCOM[47…24]								CCOM[23…0]							–
1/65 1/64	0		CCOM[0..63]															COMI
	1		CCOM[63..0]															–

Relationship between Duty Ratio and Common Output

Initial Display Line Register

The initial display line register assigns a DDRAM line address which corresponds to COM0 by using the “Initial display line set” instruction. It is used for not only normal display but also vertical display scrolling and page switching without changing the contents of the DDRAM. However, the 65th address for icon display cannot be assigned for the initial display line address.

Line Counter

The line counter provides a DDRAM line address. It initializes its contents at the switching of frame reversal signal (FR), and also counts-up in synchronization with common timing signal.

Column Address Counter

The column address counter is an 8-bit preset counter which provides a DDRAM column address, and is independent of the page address register.

It will increment (+1) the column address whenever “display data read” or “display data write” instructions are issued. However, the incrementing of the column address is stopped at column address 83H. The count-lock will be released by the “column address set” instruction again. The counter can invert the correspondence between the column address and segment driver direction by means of “ADC select” instruction.

Page Address Register

The page address register provides a DDRAM page address. The Page Address 8 is used for icon display, and only D0 is valid.

7.3 LCD Driver Circuits

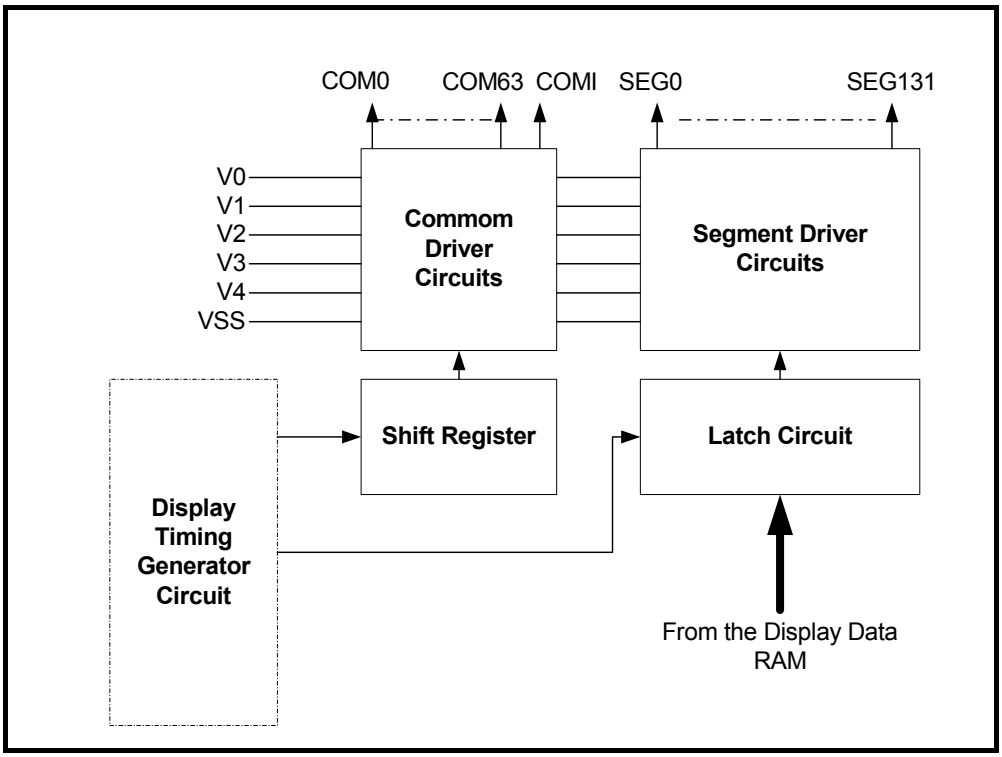


Figure 9 LCD Driver Circuits

This driver circuit is configured by 64-common drivers, 132-segment drivers and 1-icon-common driver. This LCD panel driver voltage depends on the combination of display data and FR (internal) signal.

7.3.1 Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. "Display on/off", "Inverse display on/off" and "Entire display on/off" instructions control only the contents of this latch circuit, they cannot change the contents of the DDRAM.

7.3.2 Shift Register Circuit

The circuit contains a 64-bit shift register to shift and turn-on data required for the LCD drive common signals and 1-bit shift register used for icon. The clock of this shift register is generated by display clock CL.

Example of 1/33 and 1/65 duty (ICON enable) driving waveform

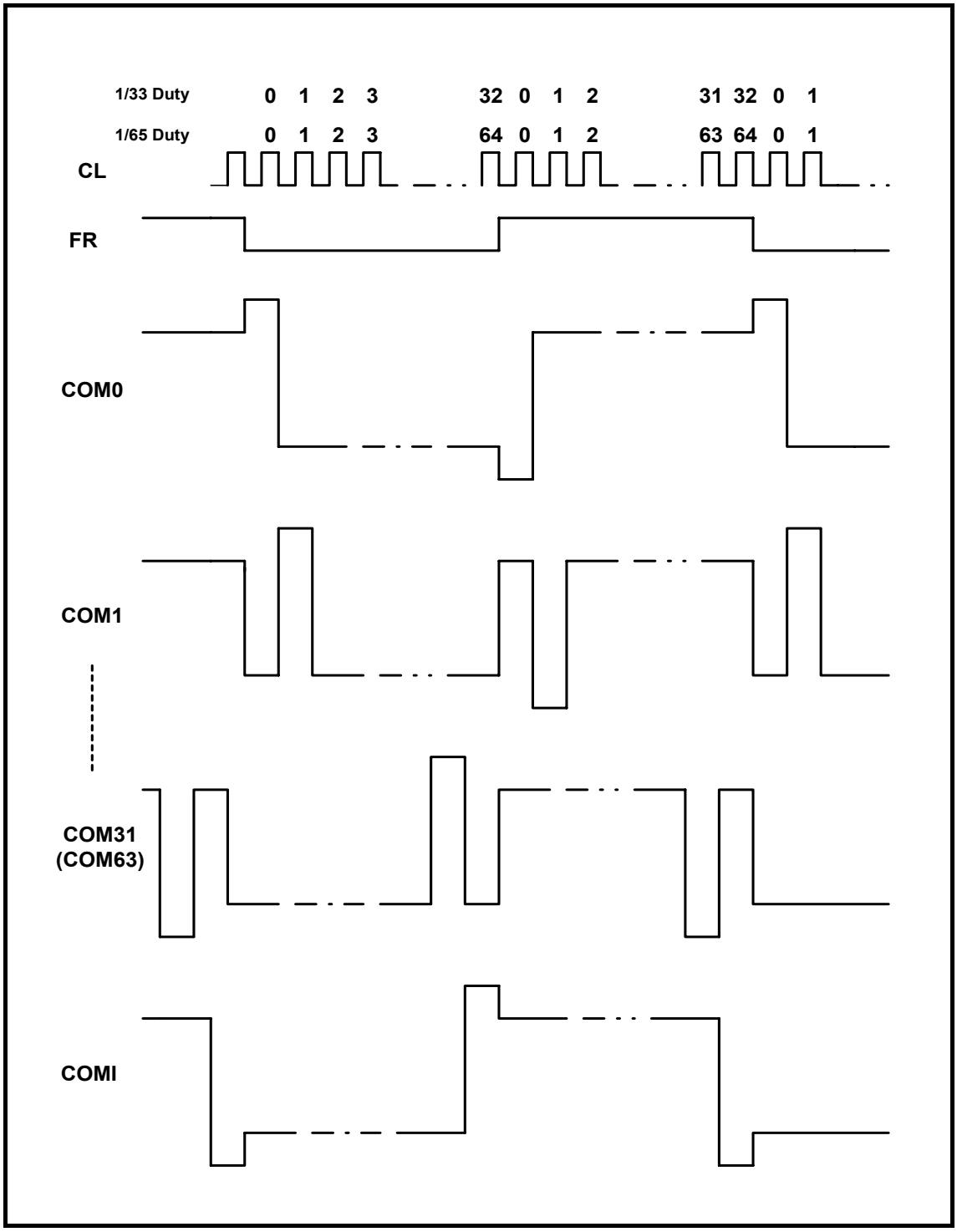


Figure 10 1/33 and 1/65 Duty Driving Waveform

Example of 1/32 duty and 1/64 Duty (Icon disable) driving waveform

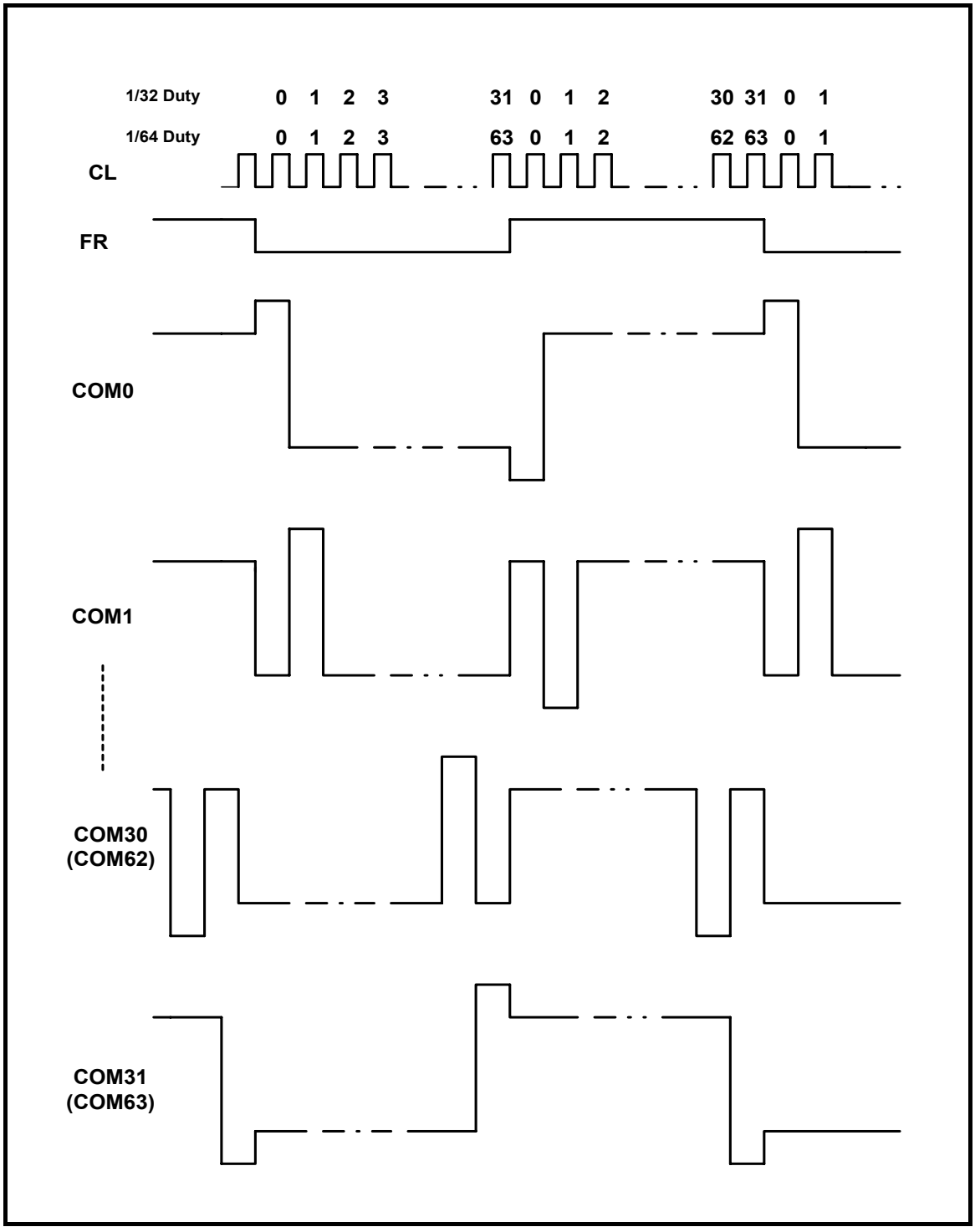


Figure 11 1/32 and 1/64 Duty Driving Waveform

7.3.4 Common Driver Circuit

The Common driver circuit consists of 65 drive circuits. One of the four LCD driving level is selected by the combination of FR and data from the shift register.

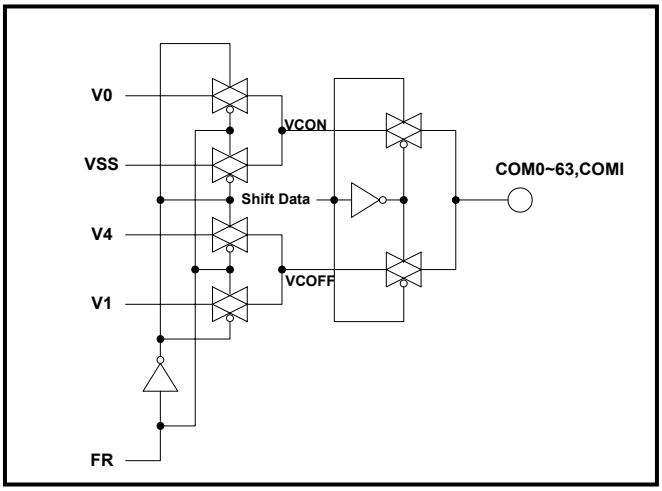


Figure 12 Common Driver Circuit

Scan Data	FR	COMs Output Voltage
H	H	VSS
	L	V0
L	H	V1
	L	V4
Power save mode		VSS

7.3.5 Segment Driver Circuit

The Segment driver circuit consists of 132 driver circuits. One of the four LCD driving level is selected by the combination of FR and the display data transferred from the latch circuit.

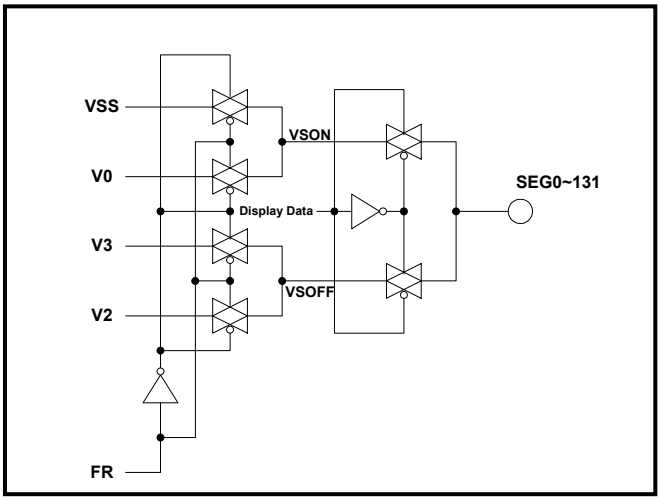


Figure 13 Common Driver Circuit

Display Data	FR	SEGs Output Voltage	
		Normal Display	Inverse Display
H	H	V0	V2
	L	VSS	V3
L	H	V2	V0
	L	V3	VSS
Power save mode		VSS	

7.3.6 LCD Driving Waveform

The following illustration is an example of how the common and segment drivers are attached to an LCD panel.

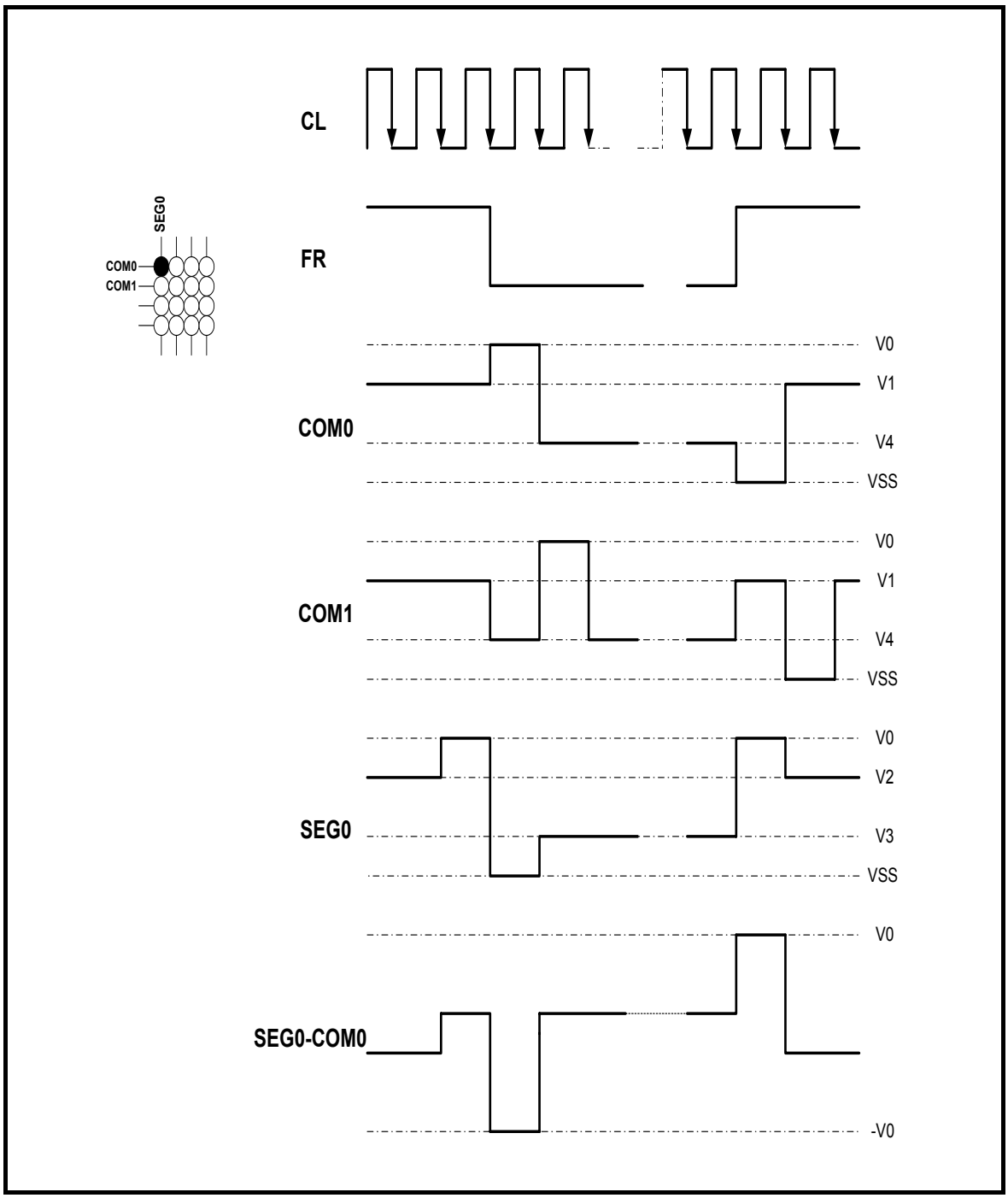


Figure 14 LCD Driver Waveform

7.4 Internal Power Circuits

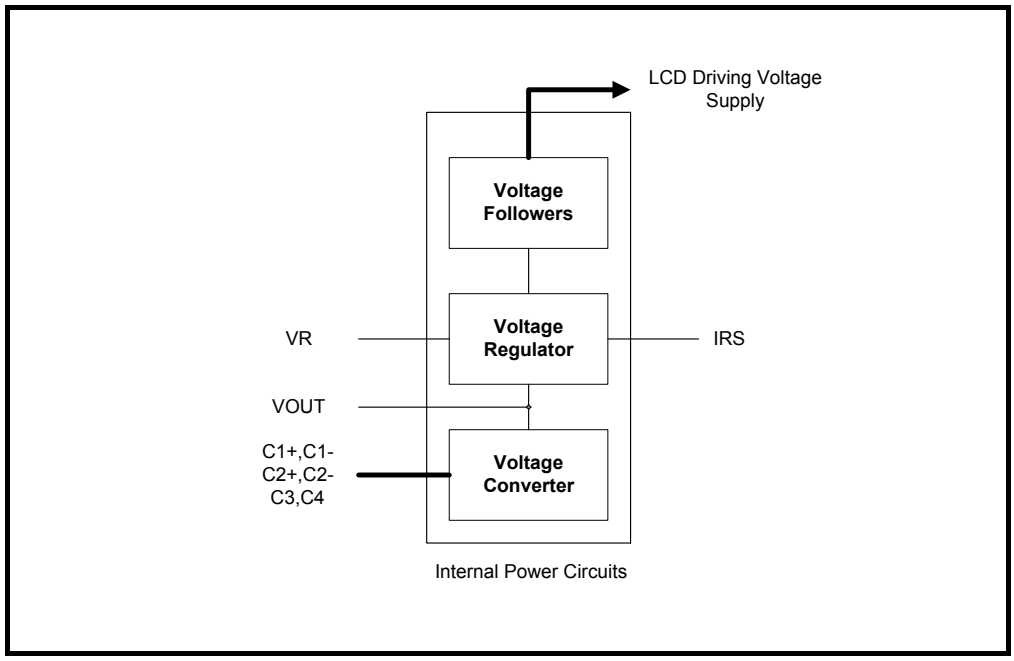


Figure 15 Internal Power Circuits

The internal power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter (V/C) circuits, voltage regulator (V/R) circuits, and voltage follower (V/F) circuits. They are valid only in **master** operation and controlled by “Power Control” instruction. For details, refers to "Instruction Description".

User Setup	Power Control (VC VR VF)	V/C Circuits	V/R Circuits	V/F Circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	On	On	On	Open	Open	Open
Only the voltage Regulator circuits and voltage follower circuits are used	0 1 1	Off	On	On	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	Off	Off	On	Open	External input	Open
Only the external power supply circuits are used	0 0 0	Off	Off	Off	Open	External input	External input

7.4.1 Voltage Converter Circuits

These circuits boost up the electric potential between VDD and VSS to 2, 3, 4, or 5 times toward positive side and the boosted voltage is outputted from VOUT pin. The boosting magnitude of internal booster circuit is selected by the means of the capacitor connection (Refer Figure 16 below). The internal oscillator is required to be operating when using this converter, since the divided signal provided from the oscillator is used for the internal timing of this circuit.

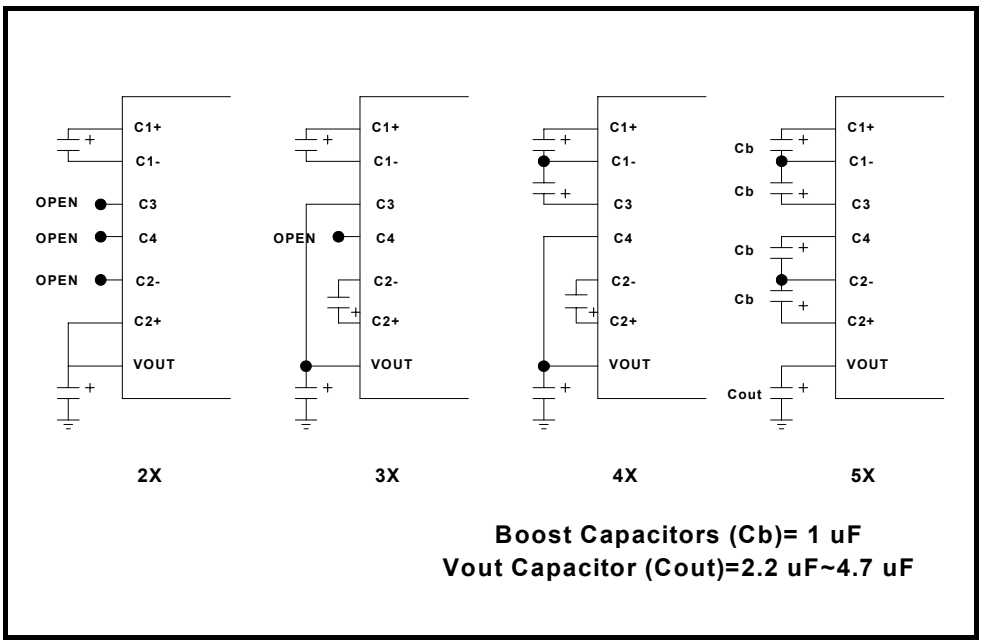


Figure 16 Capacitor Connections

7.4.2 Voltage Regulator Circuits

The voltage regulator determines the LCD driving voltage V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Since VOUT is the operating voltage of the operational-amplifier circuits, it is necessary to be applied internally or externally. For Equation 1, we determine V0 by Ra, Rb and VEV. Ra and Rb are connected internally or externally by the IRS pin. **VEV** which is the voltage of the electronic volume is determined by Equation 2, where the parameter α is the value selected by instruction, "Set Contrast Control Mode", within the range 0 to 63.

VREF, a constant voltage source is about 2V at TA=25°C.

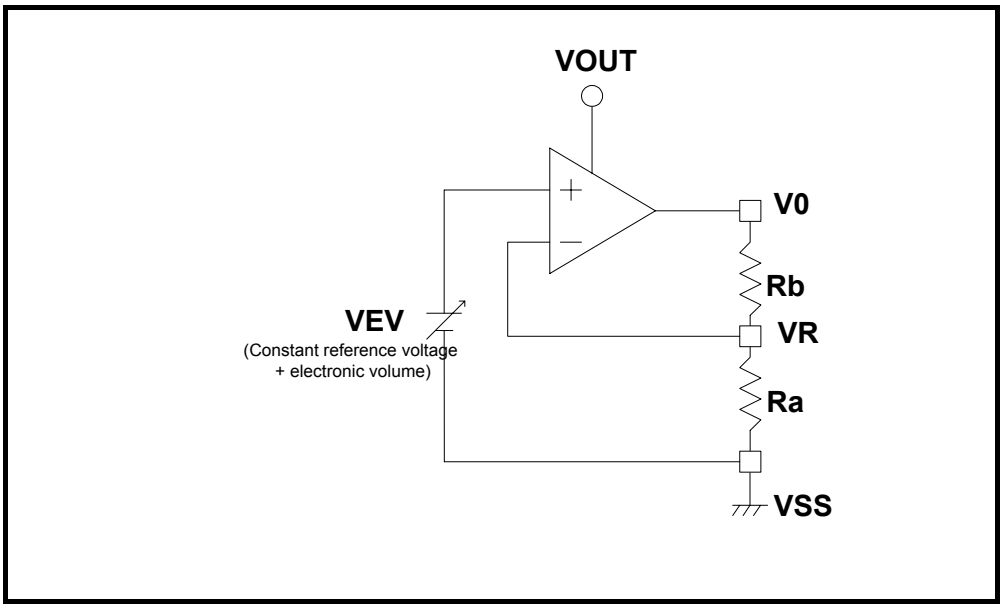


Figure 17 Resistor Connection

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV \quad \text{.....Equation 1}$$

$$VEV = (1 - \frac{(63 - \alpha)}{252}) \times VREF \quad \text{.....Equation 2}$$

Register Value (R2, R1, R0)	1+ (Rb/Ra)	Value
0 0 0	3.5	Small . . . . . . Large
0 0 1	4.0	
0 1 0	4.5	
0 1 1	5.0	
1 0 0	5.5	
1 0 1	6.0	
1 1 0	6.5	
1 1 1	7.0	

Refer to “Regulator Resistor Select” instruction for details.

α	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	0	0	0	0	0	1
..	.	.	.	.	.	.
..	.	.	.	.	.	.
62	1	1	1	1	1	0
63	1	1	1	1	1	1

Refer to “Set Contrast Control Mode” instruction for details.

Using Internal Resistors, Ra and Rb (IRS = "H")

When the IRS pin is “H”, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. V0 is determined by using the two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Using External Resistors, Ra and Rb (IRS = "L")

When IRS pin is “L”, it is necessary to connect the external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

For a particular liquid, the optimum V_{LCD} can be calculated for a given multiplex rate.

For a 1/65 duty ratio, the optimum operating voltage of the liquid can be calculated as:

$$V_{LCD} = \frac{1+\sqrt{65}}{\sqrt{2\times\left(1-\frac{1}{\sqrt{65}}\right)}}\times V_{th} = 6.85\times V_{th}$$

where V_{th} is the threshold voltage of the liquid crystal material used.

7.4.3 Voltage Follower Circuits

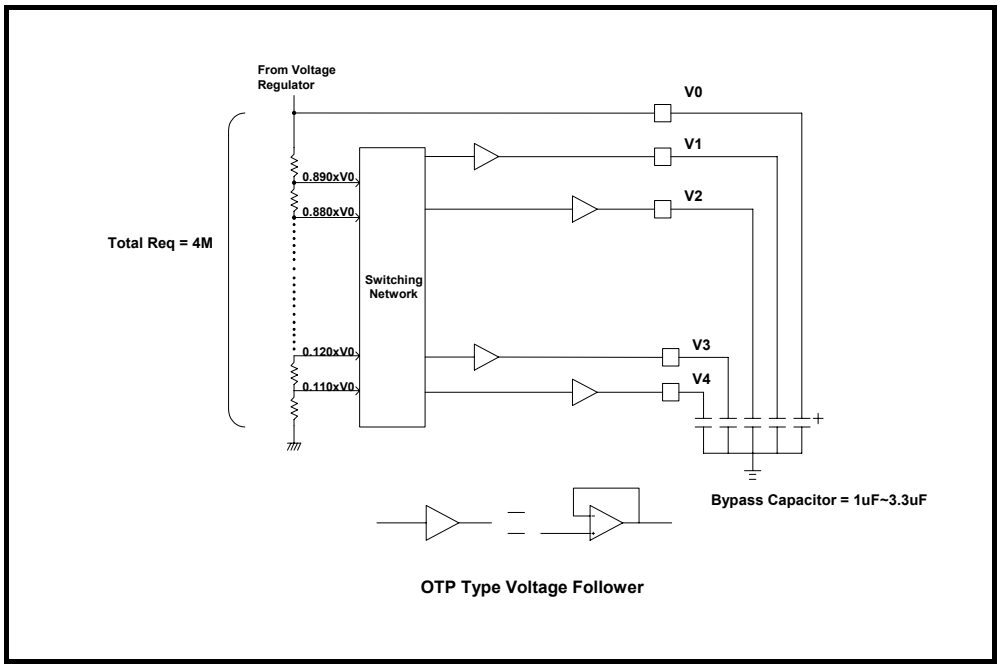


Figure 18 OTP Voltage Follower Circuit

The VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3, V4), and those output impedance are converted by the voltage follower (OPA) to increase the drive capability. A total of six levels LCD reference voltage (V0, V1, V2, V3, V4, VSS) is generated by the voltage follower circuits.

LCD Bias	V1	V2	V3	V4
1/9	0.890*V0	0.780*V0	0.220*V0	0.110*V0
1/8.5	0.880*V0	0.765*V0	0.235*V0	0.120*V0
1/8	0.875*V0	0.750*V0	0.250*V0	0.125*V0
1/7.5	0.865*V0	0.735*V0	0.265*V0	0.135*V0
1/7	0.855*V0	0.715*V0	0.285*V0	0.145*V0
1/6.5	0.845*V0	0.690*V0	0.310*V0	0.155*V0
1/6	0.835*V0	0.665*V0	0.335*V0	0.165*V0
1/5.5	0.820*V0	0.635*V0	0.365*V0	0.180*V0
1/5	0.800*V0	0.600*V0	0.400*V0	0.200*V0
1/4.5	0.780*V0	0.555*V0	0.445*V0	0.220*V0
1/4	0.750*V0	0.500*V0	0.500*V0	0.250*V0

Different duty radio requires different bias level. For optimum bias level, B_L can be calculated from:

$$B_L = \frac{1}{\sqrt{Duty\ ratio} + 1}$$

Changing the bias system from the optimum will have a consequence on the contrast and viewing angle.

The LCD Bias affects the display quality. But for the purpose of reducing the current consumption, the unsuitable bias may be selected. Hence, the LCD Bias could be selected by “Select LCD bias” instruction.

7.5 LCD Display Circuits

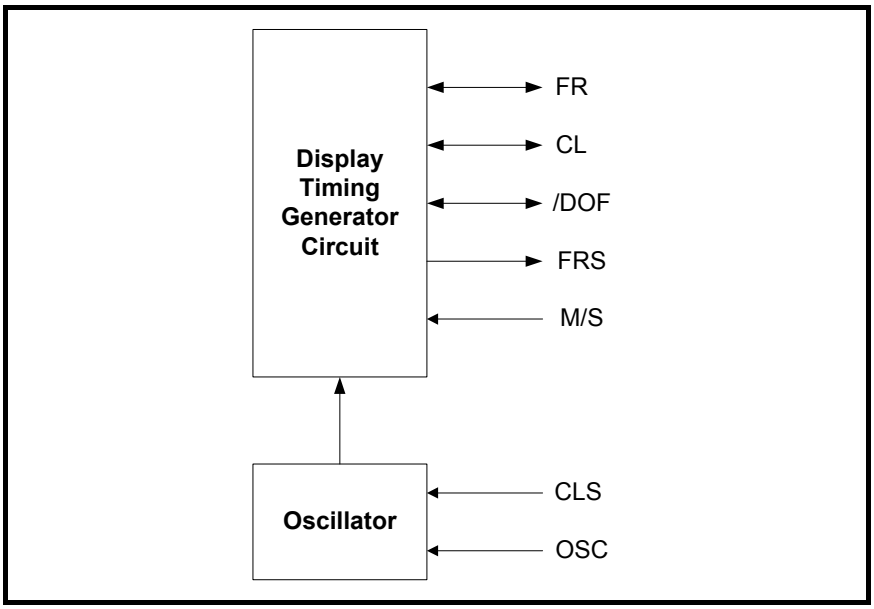


Figure 19 LCD Display Circuit

7.5.1 Oscillator

The on-chip RC type oscillator provides the display clock and voltage converter timing clock. It has low power consumption and its frequency is nearly independent of VDD.

When **"M/S"= "H"** and **"CLS"= "H"**, the oscillator circuit is enabled. When CLS="L", the oscillator is stopped, and the oscillator clock has to be input to the OSC pin.

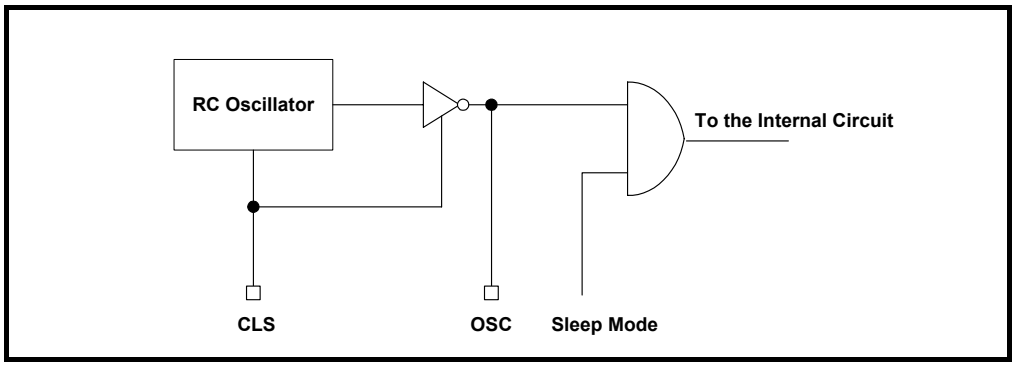


Figure 20 RC Oscillator

The oscillator circuit is available in **master** mode only. The oscillator signal is divided and output as display clock at the CL pin.

7.5.2 /DOF Pin Description

The pin is used to control the blinking of the LCD display.

Instruction	M/S= "H"	M/S="L"	
	/DOF (Output)	/DOF (Input) ="H"	/DOF (Input) ="L"
Display "ON"	"H"	LCD On	LCD Off
Display "OFF"	"L"	LCD Off	LCD Off

When the "Power Save" Instruction is activated, the /DOF pin is set to low level.

7.5.3 Display Timing Generator Circuit

This circuit generates some signals to be used to display the LCD. When used in master/slave mode (multi-chip), some pins must be connected to each other. That is due to synchronization output. The display clock (CL) generated by the oscillation clock, generates a clock for the line counter and a latch signal for the display data latch. The line address of the on-chip RAM is generated in synchronization with the display clock (CL). While the 132-bit display data is latched by the display data latch circuit in synchronization with the display clock, the display data which is read to the LCD driver is completely independent from any access to the display data RAM from the microprocessor.

The display clock generates an LCD frame reversal signal (FR) which enables the LCD driver to make an AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. When this EPL65132 is used as a multi-chip, the slave chip must receive the FR, CL, /DOF signals from the master.

Operation Mode		FR	CL	/DOF	FRS	OSC
Master (M/S="H")	Internal oscillator is enabled (CLS="H")	Output	Output	Output	Output	Open
	Internal oscillator is disable (CLS="L")	Output	Output	Output	Output	Input
Slave (M/S="L")	Internal oscillator is disabled (CLS ="L" or "H")	Input	Input	Input	Hi-Z	Open
		Input	Input	Input	Hi-Z	Open

Note: Open means leave this pin open

7.5.4 Oscillator Frequency

The EPL65132 contains an RC oscillator. The frame frequency (f_{FM}) is derived from the RC circuit's oscillation frequency (f_{OSC}) by giving it an appropriate value. The relationship between the oscillation frequency (f_{OSC}), display clock frequency (f_{CL}) and the frame frequency (f_{FM}) is shown below.

The f_{OSC} could be selected from an internal or external oscillator via the CLS pin, f_{CL} could be selected using the "Set display clock CL frequency" instruction, and frame frequency could be calculated using the following equation.

$$f_{CL} = (\text{Duty ratio}) \times (\text{Frame frequency})$$

7.6 The Reset Circuit

When the /RES input comes to the "L" level, these LSI return to their default state. Their default states are as follows:

1. Display OFF
2. Normal display
3. ADC select: Normal (ADC select instruction D0 = "L")
4. SHL select: Normal (SHL select instruction D3 = "L")
5. Power control register: (D2, D1, D0) = (0, 0, 0)
6. Serial interface internal register data clear
7. Duty ratio = 1/65
8. CL frequency Register (D4, D3, D2, D1, D0) = (0, 0. 0, 0, 1, 1)
9. LCD power supply bias level = (1/9)
10. Entire display OFF (Entire display instruction D0 = "L")
11. Power saving clear

12. Modify-Read OFF
13. Static indicator OFF
    Static indicator register: (D1, D2) = (0, 0)
14. Display initial line set to first line: 0
15. Column address set to Address: 0
16. Page address set to Page: 0
17. Normal power mode: HP=0
18. V0 voltage regulator internal resistor ratio set mode clear: (R2, R1, R0) = (0, 0, 0)
19. Contrast control set mode clear
    Contrast control register: (D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0, 0)

8 Instruction Description

Instruction	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Description
Read Display Data	1	0	1	Read Data								Read data from DDRAM
Write Display Data	1	1	0	Write Data								Write data into DDRAM
Read Status	0	0	1	-	Status			0	0	0	0	Read the internal status
Set Duty Ratio Mode	0	1	0	1	0	0	0	0	1	0	0	Set duty ratio Mode
Duty Ratio Register	0	1	0	*	*	*	*	ICON	D2	D1	D0	Select the duty ratio
Set CL Frequency Mode	0	1	0	1	0	0	0	0	0	1	0	Set CL frequency Mode
CL Frequency Register	0	1	0	*	*	*	D4	D3	D2	D1	D0	Set CL frequency Register
Set LCD Bias Select Mode	0	1	0	1	0	0	0	0	1	0	1	Set LCD Bias select Mode
LCD Bias Select Register	0	1	0	*	*	*	*	D3	D2	D1	D0	Select the LCD Bias
Display On/Off	0	1	0	1	0	1	0	1	1	1	Don	Turn on/off LCD panel When DON=0: display off When DON=1: display on
Initial Display Line	0	1	0	0	1	D5	D4	D3	D2	D1	D0	Specify DDRAM line for COM0
Set Contrast Control Mode	0	1	0	1	0	0	0	0	0	0	1	Set Contrast Control Mode
Set Contrast Control Register	0	1	0	*	*	D5	D4	D3	D2	D1	D0	Set Contrast Control Register
Set Page Address	0	1	0	1	0	1	1	Page Address				Set page address
Set Column Address MSB	0	1	0	0	0	0	1	Higher order Column Add.				DDRAM column address of the Higher 4-bits
Set Column Address LSB	0	1	0	0	0	0	0	Lower order column Add.				DDRAM column address of the lower 4-bits
ADC Select	0	1	0	1	0	1	0	0	0	0	ADC	Select segment direction When ADC=0: normal direction (SEG0 → SEG131) When ADC=1: reverse direction (SEG131→ SEG0)
Inverse Display ON/OFF	0	1	0	1	0	1	0	0	1	1	REV	Select normal/inverse display 0: Normal display 1: Inverse display on

Instruction	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Description
Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	EON	Select normal/entire display ON When EON=0: normal display. When EON=1: entire display ON
Set Modify-read	0	1	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset Modify-read	0	1	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL Select	0	1	0	1	1	0	0	SHL	*	*	*	Select COM output direction When SHL=0: normal direction (COM0 → OM63) When SHL=1: reverse direction (COM63 → COM0)
Power Control	0	1	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Set high power mode	0	1	0	1	0	0	0	0	1	1	HP	Select high or normal power mode
Regulator Resistor Select	0	1	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio off the regulator resistor
Set Static Indicator Mode	0	1	0	1	0	1	0	1	1	0	SM	Set static indicator mode When SM = 0: off When SM = 1: on
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	S1	S0	Set static indicator register
Power Save	-	-	-	-	-	-	-	-	-	-	-	Compound display instruction OFF and entire display ON

Note: * means Don't care

8.1 Read Display Data

The 8-bit data from the display data RAM specified by the column address and page address can be read by this instruction. As the column address is automatically incremented by 1 after each instruction execution, the microprocessor can continuously read data from the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8.2 Write Display Data

The 8-bit display data from the microprocessor can be written to the RAM location specified by the column address and page address. After writing the display data, the column address is automatically incremented so that the microprocessor can continuously write data to the addressed page.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

8.3 Read Status

This instruction reads out the internal status of the “ADC select”, “Display on/off” and “Reset”.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	-	ADC	On/Off	RESET	0	0	0	0

Flag	Description
ADC	It shows the correspondence between the column address and segment drivers. ADC =0 : Reverse direction (SEG131 → SEG0) =1 : Normal direction (SEG0 → SEG131)
On/Off	This bit indicates the ON/OFF state of the display. 0: Display ON 1: Display OFF
RESET	Indicates the initialization is in progress by RESETB signal. RESET =0 : Normal display operation state =1 : Internal reset operation state with reset command.

8.4 Set Duty Ratio (Two-Byte Instruction)

This consists of 2-byte instruction. The first instruction sets the duty ratio mode, the second instruction updates the contents of the duty ratio register. After the second instruction, the set duty mode is released. The LSI cannot accept any instructions except for the “Set duty ratio register” during the set duty ratio mode.

8.4.1 Set Duty Ratio Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	0

8.4.2 Set Duty Ratio Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Duty ratio
0	1	0	*	*	*	*	ICON	0	0	0	8 (+ICON)
								0	0	1	16 (+ICON)
								0	1	0	24 (+ICON)
								0	1	1	32 (+ICON)
								1	0	0	36 (+ICON)
								1	0	1	42 (+ICON)
								1	1	0	48 (+ICON)
								1	1	1	64 (+ICON)

ICON : “1” Enable COMI (icon display) pin

: ”0” Disable COMI (icon display) pin

8.5 Set Display Clock CL Frequency (Two-Byte Instruction)

The display clock CL affects the current consumption and the frame frequency affects the flicker, so fine adjustments are required for the display clock CL and the frame frequency.

8.5.1 Set CL Frequency Select Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	1	0

8.5.2 Set CL Frequency Select Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	CL Frequency
0	1	0	*	*	*	0	0	0	0	0	f_{osc}
						0	0	0	0	1	f_{osc} / 2
						0	0	0	1	0	f_{osc} / 3
						0	0	0	1	1	f_{osc} / 4
						0	0	1	0	0	f_{osc} / 5
						0	0	1	0	1	f_{osc} / 6
						0	0	1	1	0	f_{osc} / 7
						0	0	1	1	1	f_{osc} / 8
						0	1	0	0	0	f_{osc} / 9
						0	1	0	0	1	f_{osc} / 10
						0	1	0	1	0	f_{osc} / 11
						0	1	0	1	1	f_{osc} / 12
						0	1	1	0	0	f_{osc} / 13
						0	1	1	0	1	f_{osc} / 14
						0	1	1	1	0	f_{osc} / 15
						0	1	1	1	1	f_{osc} / 16
						1	*	*	*	*	f_{osc} / 32

8.6 Select LCD Bias (Two-Byte Instruction)

This instruction selects the LCD bias ratio of the voltage required for driving the LCD.

8.6.1 Set the LCD Bias Select Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	1

8.6.2 Set the LCD Bias Select Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	LCD Bias
0	1	0	*	*	*	*	0	0	0	0	1/4
							0	0	0	1	1/4.5
							0	0	1	0	1/5
							0	0	1	1	1/5.5
							0	1	0	0	1/6
							0	1	0	1	1/6.5
							0	1	1	0	1/7
							0	1	1	1	1/7.5
							1	0	0	0	1/8
							1	0	0	1	1/8.5
							1	0	1	0	1/9

8.7 Display On/Off

This instruction is used to control the turning on or off of the LCD panel regardless of the contents of the DDRAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display On or Off
0	1	0	1	0	1	0	1	1	1	0	0 : Off
										1	1 : On

8.8 Initial Display Line

This instruction sets the line address of the display RAM to determine the initial display line. The initial display line corresponds to COM0. The display area read from the display data RAM corresponds to the number of lines set by the Duty select command.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Line Address for COM0
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					.	.	.	.	.	.	.
					.	.	.	.	.	.	.
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

8.9 Electronic Contrast Control Set (Two-Byte instruction)

This consists of 2-byte instruction. The first instruction sets contrast control mode, the second instruction updates the contents of the contrast control register. After second instruction, the contrast control mode is released. The LSI cannot accept any instructions except for the “Set Contrast Control Register” during the Contrast Control Mode.

8.9.1 Set Contrast Control Mode (First Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

8.9.2 Set Contrast Control Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Electronic Volume Value (α)
0	1	0	*	*	0	0	0	0	0	0	0 Minimum
					0	0	0	0	0	1	1
					.	.	.	.	.	.	.
					.	.	.	.	.	.	.
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

8.10 Set Page Address

This instruction sets the page address of the display data RAM from the microprocessor into the page address register. It is possible to access any required bit in the display data RAM by specifying the page address and the column address.

Along with the column address, the page address defines the address of the display RAM used to write or read the display data. Changing the page address does not affect the display status. Page 8 is assigned for the icon display. Only D0 is valid.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Page Address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							.	.	.	.	.
							.	.	.	.	.
							0	1	1	1	7
							1	0	0	0	8

8.11 Set Column Address

This instruction sets the column address of the display data RAM from the microprocessor into the column address register. When accessing the display data RAM from the MPU, the column address is incremented. The incrementing of the column address is stopped at address 83H.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Column Address Setting
0	1	0	0	0	0	1	A7	A6	A5	A4	Upper 4-bit
						0	A3	A2	A1	A0	Lower 4-bit

A7	A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

8.12 ADC Select

This instruction selects the segment driver direction. Normal or reverse can be selected in the correlation between the display data RAM column address and the segment output terminal.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Segment Driver Direction
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

D0 = 0 Normal Column addresses 00H to 83H correspond to segment outputs 0 to 131.

D0 = 1 Reverse Column addresses 00H to 83H correspond to segment outputs 131 to 0.

8.13 Inverse Display On/Off

This instruction is used to invert the display status of the LCD panel without rewriting the contents of the display data RAM.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Display Status
0	1	0	1	0	1	0	0	1	1	0	Normal
										1	Inverse

D0 = 0 Normal Display data “1” turns the LCD On.

D0 = 1 Inverse Display data “0” turns the LCD On.

8.14 Entire Display On/Off

This instruction forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM will be retained. This instruction has priority over the Reverse Display On/Off instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Entire Display On/Off
0	1	0	1	0	1	0	0	1	0	0	Normal
										1	Entire display On

8.15 Set Modify-Read

This instruction stops the automatic increment of the column address by the Read Display Data instruction, but the column address is still incremented by the Write Display Data instruction. This instruction can reduce the load of the MPU. During the display, the data in a specific DDRAM area is repeatedly changed for cursor blinking or other functions. This mode is canceled by the Reset Modify-read instruction.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

8.16 Reset Modify-Read

This instruction cancels the Modify-read mode. The column address of the display data RAM returns to the address before the Read Modify Write is executed.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

8.17 Reset

This instruction resets the initial display line, column address, page address, and the common output status is reset to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the /RES pin.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Reset status by “Reset” instruction:

1. Read modify write off
2. Static indicator off and static indicator register: (S1,S0)=(0,0)
3. Initial display line address : (00)H
4. Column address : (00)H
5. Page address : (0) page
6. SHL select : Normal mode (D3=0)
7. Regulator resistor select register: (R2, R1, R0)=(0,0,0)
8. Sets contrast control set mode off and contrast control register: (20)H

8.18 SHL Select

The COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Common Driver Direction
0	1	0	1	1	0	0	0	*	*	*	Normal
							1				Reverse

Note: * means Don’t care

D3 = 0 Normal Normal direction (COM0 → COM 63)

D3 = 1 Reverse Reverse direction (COM63 → COM 0)

8.19 Power Control

This instruction is used to select one of the eight power circuit functions by using the 3-bit register. An external power supply and part of the internal power supply functions can be used simultaneously.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	VC	VR	VF

VC: Voltage converter
0: Off
1: On

VR: Voltage regulator
VF: Voltage follower

8.20 Set High Power Mode

When driving an LCD panel with large loads, the normal power mode may cause a poorer display quality. In such a case, setting to the high mode (HP=1) can improve the display quality.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	1	HP

D0 = 0 Normal power mode
D0 = 1 High power mode

8.21 Regulator Resistor Select

This selects the resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit for more details.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb/Ra] Ratio
0	0	0	Small
0	0	1	…
..	..	..	..
1	1	0	..
1	1	1	Large

8.22 Set Status Indicator (Two-Byte Instruction)

This consists of two bytes instruction. The first byte instruction (Set Static Indicator Mode) enables the second byte instruction (Set Static Indicator Register) to be valid. The first byte sets the static indicator on/off. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this status indicator state is released after setting the data of the indicator register.

8.22.1 Set Status Indicator Mode (First Instruction)

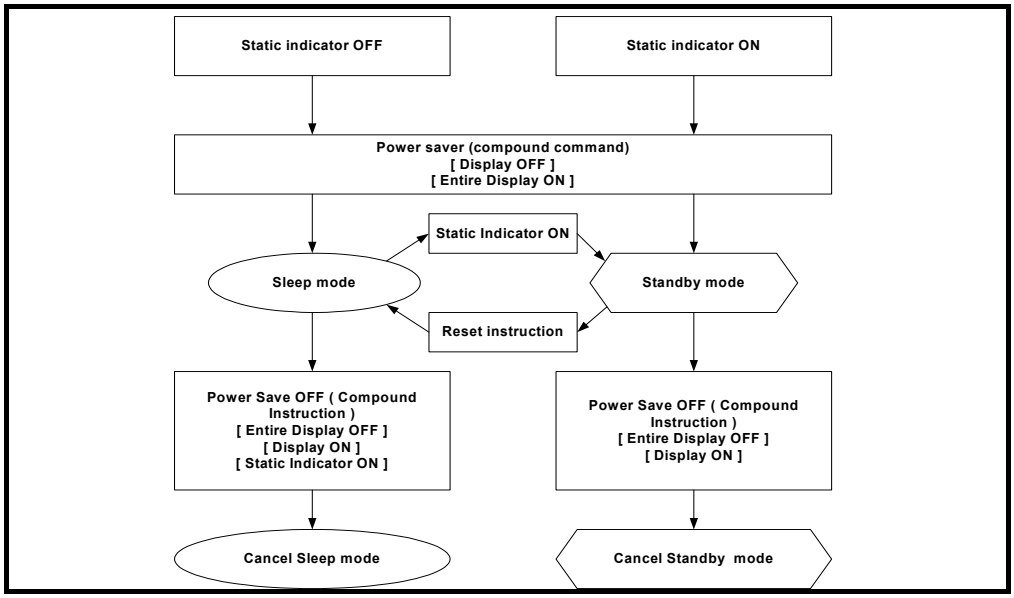
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Status Indicator
0	1	0	1	0	1	0	1	1	0	0	Off
										1	On

8.22.2 Set Static Indicator Register (Second Instruction)

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Status
0	1	0	*	*	*	*	*	*	0	0	Off
									0	1	On (Blink at 4-frame intervals)
									1	0	On (Blink at 2-frame intervals)
									1	1	On (Turn on at all time)

8.23 Power Save (Compound Instruction)

The current consumption can be greatly reduced by entering the power save status and inputting the “Entire Display ON” instruction while the display is in OFF mode. According to the status in static indicator mode, power save is entered through one of two modes (sleep and standby mode). Power Save mode is released by the “Display ON” & “Entire Display OFF” instructions.



8.23.1 Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

1. The oscillator circuit and the LCD power supply circuit are stopped.
2. All liquid crystal drive circuits are stopped, and the segment and common driver output VSS level.

When a “static indicator on” instruction is issued in the sleep mode, the LSI goes into a *standby mode*.

8.23.2 Standby Mode

All operations of the dynamic LCD display section are stopped, only the static display circuits for the indicators operate and hence the current consumption will be the minimum necessary for static drive. The internal conditions in the standby state are as follows:

1. The power supply circuit for LCD drive is stopped. The oscillator circuit will be operating.
2. The LCD drive circuits for dynamic display are stopped and the segment and common driver outputs will be at the VSS level. The static display section will be operating.

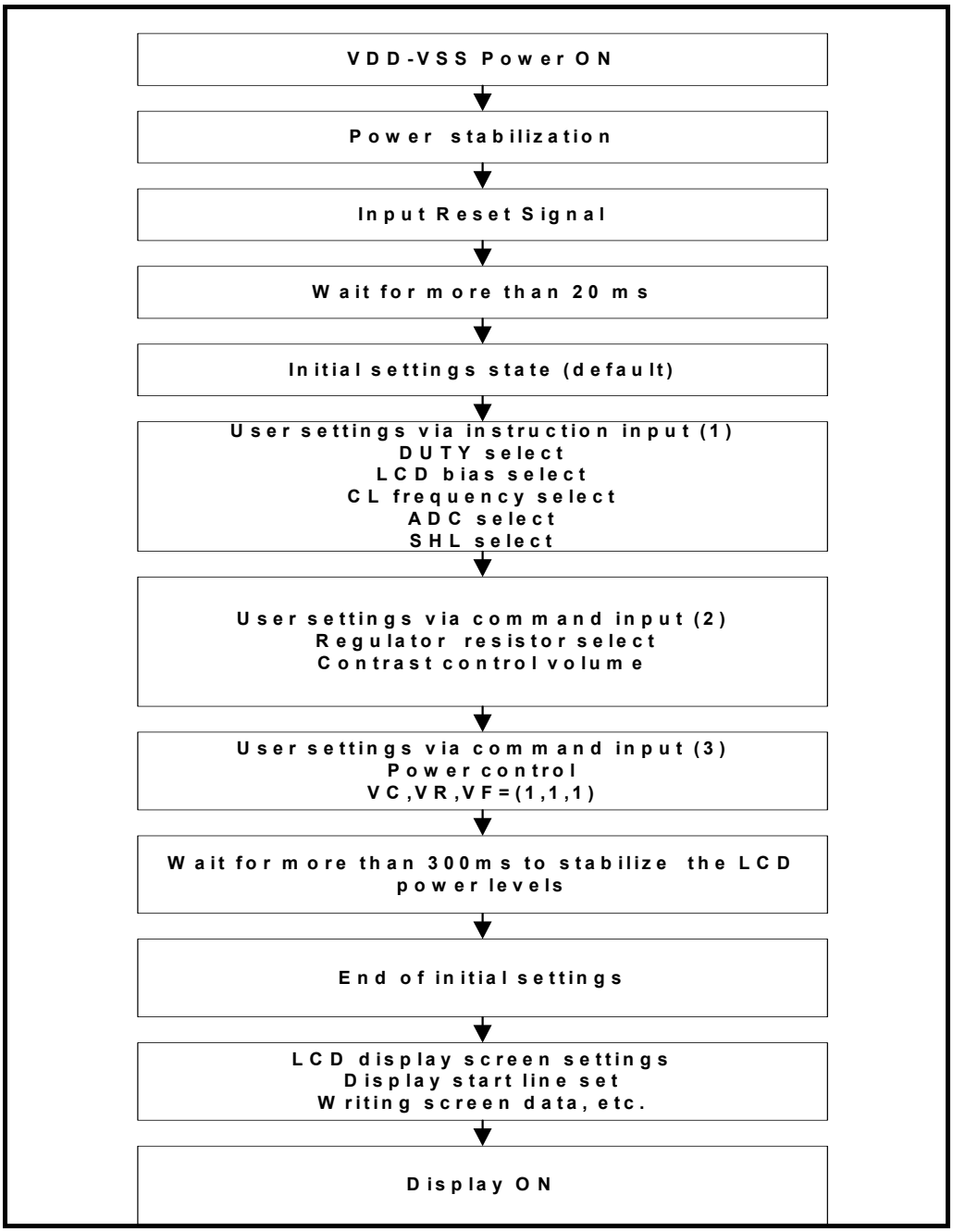
When a reset instruction is issued in the standby mode, the LSI goes into the *sleep mode.*

9 Application Information

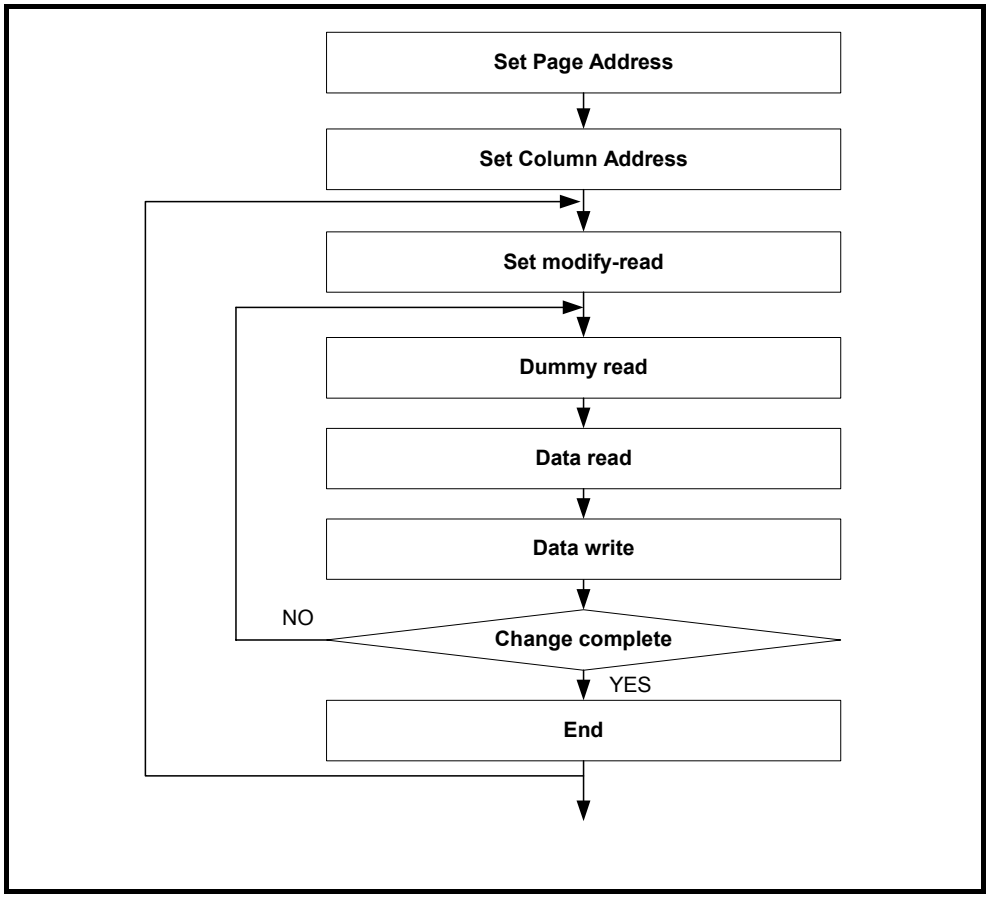
9.1 Instruction Procedure Examples

9.1.1 Initial Setup

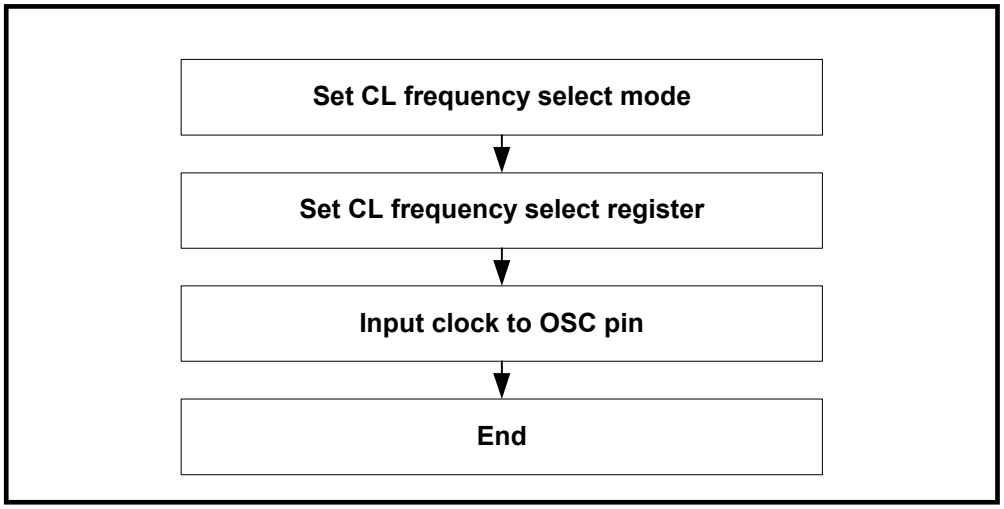
(From power application to display ON using internal power supply circuits)



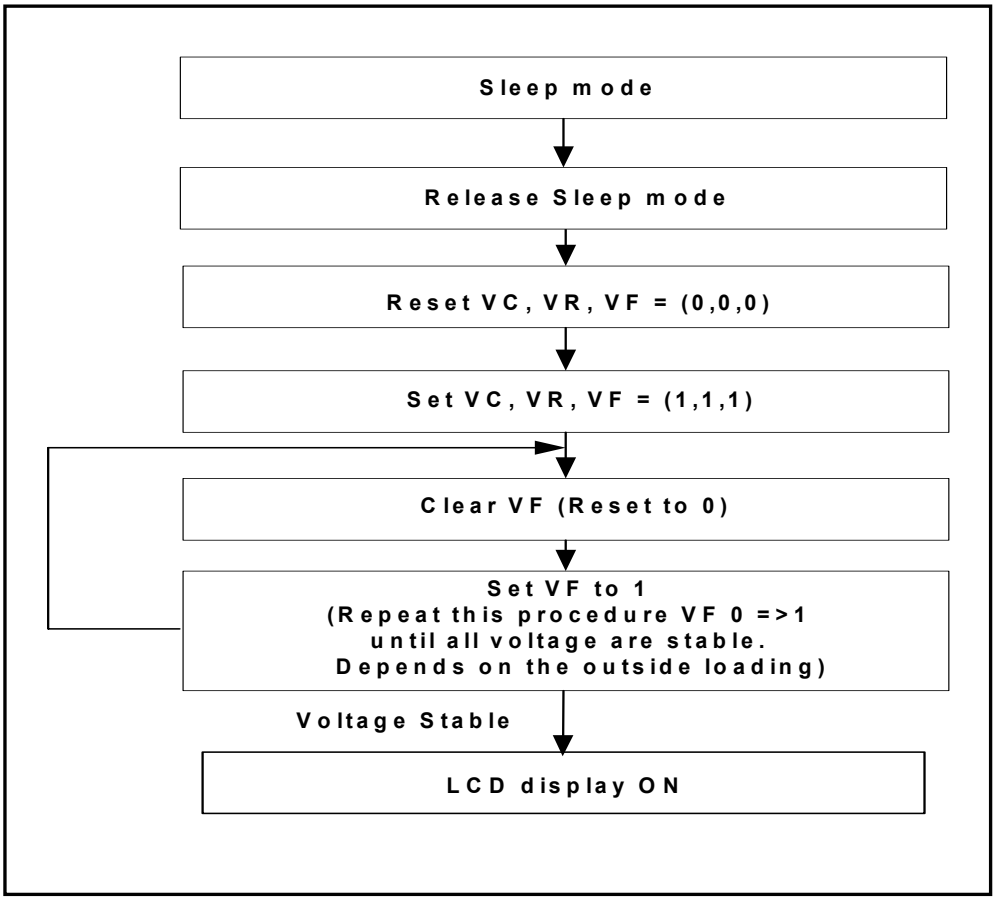
"Modify-read" Sequence



"External Oscillator Input" Sequence



"LCD Power-on" Sequence (Use Internal Power Circuit)



9.2 Program Examples

Use Elan Risc II MCU assembly

```
;*************************************************************************
;            Initialization Setting Example of EPL65132
;*************************************************************************
INI_DRIVER_IC:
  MOV   A,#LCD_COM_RESET          ;INITIAL SETTINGS STATE (DEFAULT)
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_DUTY           ;SET DUTY 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#DUTY_SET               ;SET DUTY 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_BIAS           ;SET LCD BIAS 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,BIAS_SET                ;SET BIAS 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_FREQ           ;SET LCD CL FREQUENCY 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#CL_FREQ                ;SET CL FREQUENCE 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_ADC_SET            ;SET ADC FUNCTION SELECT
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_SHL_SET            ;SET SHL FUNCTION SELECT
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_REGULATOR_RES_SET  ;SET REGULATOR RESISTOR 1+(Rb/Ra)
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_COM_CONTRAST       ;SET CONTRAST 1ST INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#CONTRAST_SET           ;SET CONTRAST 2ND INSTRUCTION
  CALL  WRITE_LCD_1BYTE
  MOV   A,#LCD_POWER_CONTROL_SET  ;SET POWER CONTROL (INTERNAL OR EXTERNAL)
  CALL  WRITE_LCD_1BYTE
  BS    REG_CPUCON,F_CKS          ;ADD CLOCK BY OSC PIN (CLOCK FROM CPU)
  MOV   A,#150                    ;WAIT TO STABILIZE THE LCD POWER
  CALL  WAIT_A_MS
  CALL  LCD_DISPLAY_ON            ;TURN ON LCD
  MOV   A,#LCD_DISPLAY_INI_LINE   ;SET INITIAL DISPLAY LINE
  CALL  WRITE_LCD_1BYTE
  CALL  LCD_DATA_WRITE            ;WRITING SCREEN DATA
  RET
```

```
;*******************************************************************************
;   Write Display_Picture Data into Display Data RAM of EPL65132
;*******************************************************************************
DATA_WRITE:
  TBPTL   #DISPLAY_PICTURE*2      ;DEFINE DISPLAY PICTURE DATA INDEX
  TBPTM   #DISPLAY_PICTURE/0x80
  TBPTH   #DISPLAY_PICTURE/0x8000
DATA_WRITE_65132:
  MOV     A,#LINE_Y_MAX           ;MAX PAGES OF DDRAM
  MOV     REG_LCDARH,A
DATA_W1:
  MOV     A,#LINE_X_MAX           ;SET MAX SEGMENTS OF DDRAM
  MOV     REG_LCDARL,A
  BC      REG_PORTB,F_LCD_A0      ;SET LCD /A0=0 INSTRUCTION OUTPUT
  MOV     A,#LCD_COM_PAGE
  ADD     A,REG_LCDARH
  CALL    WRITE_LCD_1BYTE
  MOV     A,#0b00000000           ;SET LOWER ORDER COLUMN ADDRESS=0000
  CALL    WRITE_LCD_1BYTE
  MOV     A,#0b00010000           ;SET HIGHER ORDER COLUMN ADDRESS=0000
  CALL    WRITE_LCD_1BYTE
  BS      REG_PORTB,F_LCD_A0      ;SET LCD /A0 = 1 DATA OUTPUT
DATA_W2:
  TBRD    01,REG_ACC              ;ACCESS THE DATA OF DISPLAY_PICTURE
  CALL    WRITE_LCD_1BYTE
  DEC     REG_LCDARL
  JBS     REG_STATUS,F_C,DATA_W2  ;IDENTIFY RES_STATUS CARRY BIT SET OR NOT
  DEC     REG_LCDARH
  JBS     REG_STATUS,F_C,DATA_W1
  BC      REG_PORTB,F_LCD_A0      ;LCD /A0 = 0 FOR INSTRUCTION OUTPUT
  RET
```

```
;*************************************************************************
;
;   Write One Byte Data into DDRAM (Parallel Mode 80 Series)
;
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION WRITE
WRITE_LCD_1BYTE:
  JBS   REG_DCRG,F_LAHEN,WRITE_LCD_1BYTE_1     ;CHECK REG_DCRG LAHEN BIT=1 OR NOT
  BC    REG_PORTC,F_LCD_WR                     ;SET /WR=0 ENABLE WRITE
  MOV   REG_DATA,A                             ;MOVE A → PORT_G
  NOP                                          ;Write low pulse( Wait 2 instruction cycles)
  NOP
  BS   REG_PORTC,F_LCD_WR                      ;SET /WR=1 DISABLE WRITE
  NOP
  NOP
  NOP
  NOP
  RET
WRITE_LCD_1BYTE_1:
  MOV   REG_DATA,                              ;MOVE A → PORT_G
  RET


;*************************************************************************
;
;   Read One Byte Data into DDRAM (Parallel Mode 80 Series)
;
;*************************************************************************
;AT FIRST DEFINE A0 TO IDENTIFY DATA OR INSTRUCTION READ
READ_LCD_1BYTE:
  BC    REG_PORTB,F_LCD_RD                     ;SET /RD=0 ENABLE READ
  NOP
  NOP
  MOV   A,REG_DATA                             ;MOVE PORT_G → A
  NOP
  BS    REG_PORTB,F_LCD_RD                     ;SET /RD=1 DISABLE READ
  NOP
  RET
```

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Applicable Pins	Symbol	Condition	Rated Value	Unit
Power supply voltage	VDD	VDD	TA=25°C	-0.3 to +7	V
Driver supply voltage	VOUT	VLCD	TA=25°C	-0.3 to +17	
Input voltage	All InpuT	VIN	TA=25°C	-0.3 to VDD+0.3	
Operating temperature range	-	TA	-	-30 to +80	°C
Storage temperature range	-	-	-	-55 to +125	

10.2 Recommended Operating Conditions

Parameter	Applicable Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power supply Voltage	VDD	VDD	-	2.2	-	5.5	V
Voltage converter output voltage	VOUT	VOUT	-	4.0	-	15	
Output voltage	-	VOH	-	0.7VDD	-	VDD	
	-	VOL	-	VSS	-	0.3VDD	
Input voltage	-	VIH	-	0.7VDD	-	VDD	
	-	VIL	-	VSS	-	0.3VDD	
Operating temperature range	-	TA	-	0	-	40	°C

10.3 DC Characteristics

VSS=0V, VDD=2.7V to 3.3V, TA=-30°C ~ 80°C

Parameter	Applicable Pins	Symbol	Condition	Rated Value			Unit
				Min.	Typ.	Max.	
Power Supply Voltage	VDD	VDD		2.2	-	5.5	V
Voltage Converter Input voltage	VDD	VDD2	2 × boost	2.2	-	5.5	
	VDD	VDD3	3 × boost	2.2	-	5.0	
	VDD	VDD4	4 × boost	2.2	-	3.75	
	VDD	VDD5	5 × boost	2.2	-	3.0	
Reference Voltage	-	V_{REF}	TA = 25°C	1.98	2.06	2.14	
Regulated Voltage	V0 [1]	V0	TA = 25°C	V0-4%	V0	V0+4%	
Bias Voltage	V4	V4	TA = 25°C	0.75			
Output Voltage	-	VOH	IOH = -0.5mA	0.8VDD	-	VDD	
	-	VOL	IOL = 0.5mA	VSS	-	0.2VDD	
Voltage Converter Output Voltage	VOUT	VOUT	×2/×3/×4/×5 No load	95	99	100	%
LCD Driver ON Resistance	COMn SEGn	R_{ON}	Current load I_{load} = 50μA	-	2	5	kΩ
Reset Resistor	/RES	R_{RESET}	VDD = 3V, Vin = 0V	400	800	1200	
			VDD = 3V, Vin = 1.7V	25	50	75	
LCD Voltage Capacitor	V0, V1, V2, V3, V4	Cv		1	-	3.3	μF
Boost Capacitor	C1, -C1, C2, -C2, C3, C4	Cb		-	1	-	
Vout Capacitor	Vout	Cout		2.2	-	4.7	
Input Leakage Current	All Input [2]	IIL	VIN = VDD or 0V	-	-	±1	μA
Output Current (Source and Drain)	[3]		V_{OUT} = V_{DD} or V_{SS}			± 500	
Output Tri-state	[3]					± 3	
Dynamic Current Consumption	-	IDDD	VDD = 3V, TA = 25°C, Quad boosting, f_{OSC} = 22kHz, 1/65 duty ratio, All display pattern off	-	88	140	
Current Consumption	-	IDDs1	Standby mode	-	5	10	
Current Consumption	-	IDDs2	Sleep mode	-	1	2	
Frame Frequency	-	f_{FM}		-	85	-	Hz
Internal Oscillator Frequency	-	f_{OSC}	TA = 25°C	17	22	27	kHz
External Input Oscillator	OSC	f_{OSC}	TA = 25°C	-	22	-	

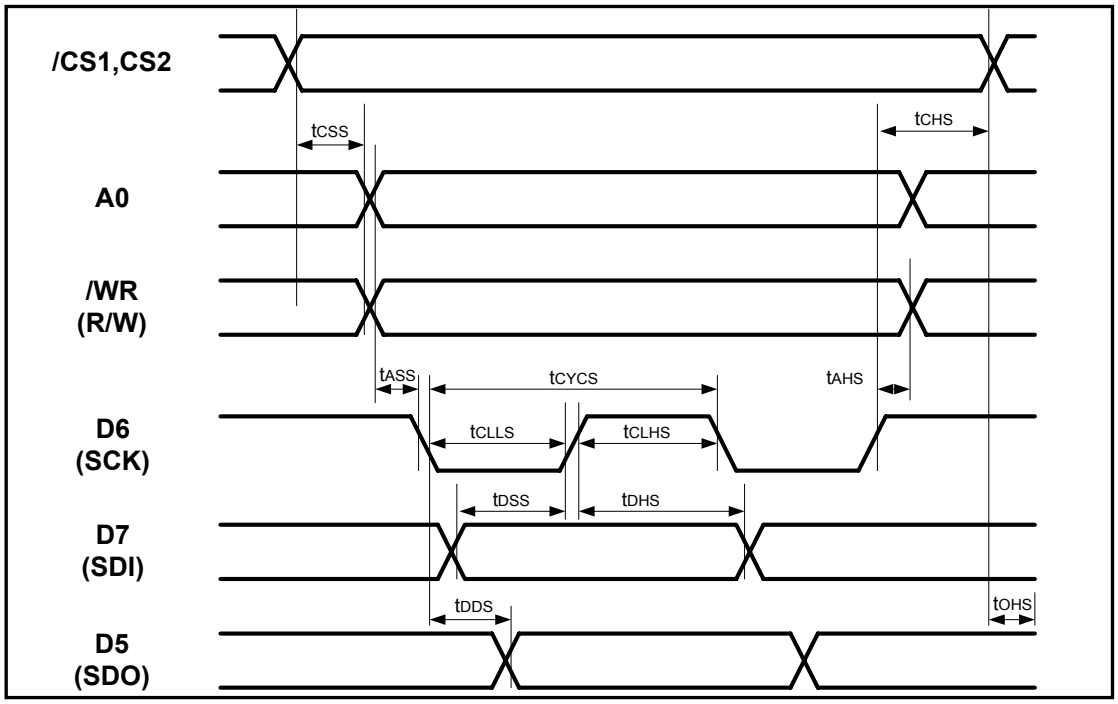
Note [1]: $V0 = (1+\frac{Rb}{Ra}) \times VEV \;\; ; \; VEV = (1-\frac{(63-\alpha)}{252}) \times VREF$

[2]: Input pin D0~D7, A0, /RD, /WR, /CS1, CS2, CLS, M/S, C86, P/S, /RES, IRS, OSC

[3]: Output pin D0~D7, FR, FRS, /DOF, CL

10.4 AC Characteristics

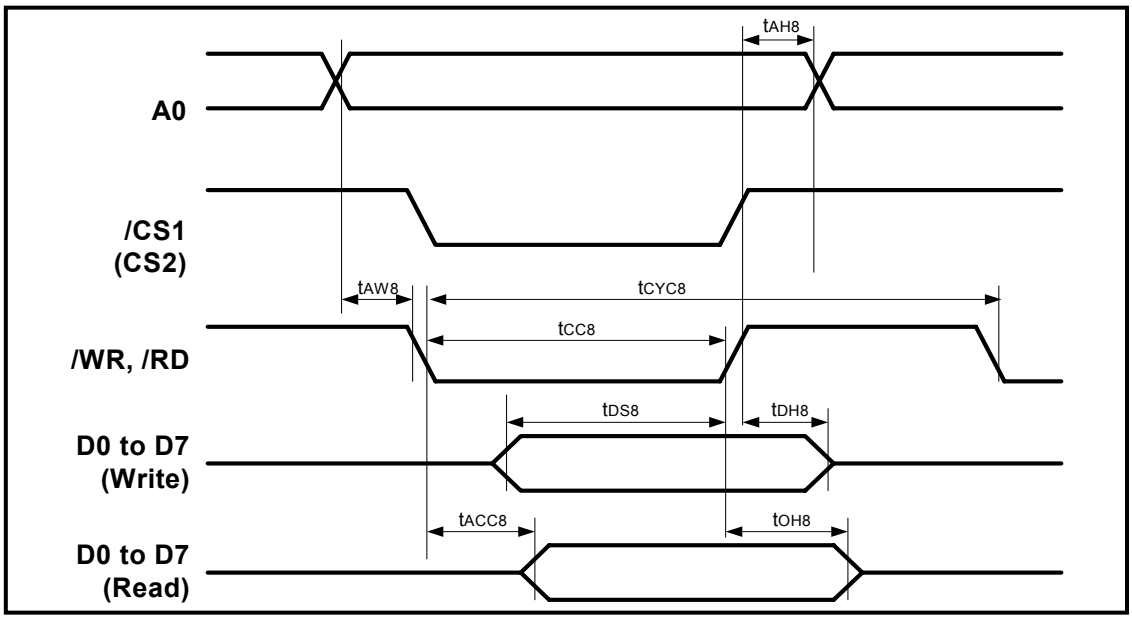
10.4.1 Serial Interface Timing Characteristics



VSS= 0V, VDD= 3.0 V, TA=25°C

Parameter	Applicable Pins	Symbol	Condition	Rated Value		Unit
				Min.	Max.	
Chip Select Setup Time Chip Select Hold Time	/CS1 CS2	t_{CSS} t_{CHS}	-	100 100	-	ns
Address Setup time Address Hold time	A0 R/W	t_{ASS} t_{AHS}	-	100 100	-	
Data Setup Time Data Hold Time	D7 (SDI)	t_{DSS} t_{DHS}	DATA→SCK↑ SCK↑→DATA	80 80	-	
Clock Cycle Time Clock L Time Clock H Time	D6 (SCK)	t_{CYCS} t_{CLLS} t_{CLHS}	-	300 100 100	-	
Data Delay Time Data Disable Time	D5 (SDO)	t_{DDS} t_{OHS}	CL= 100 pF	- 10	80 50	

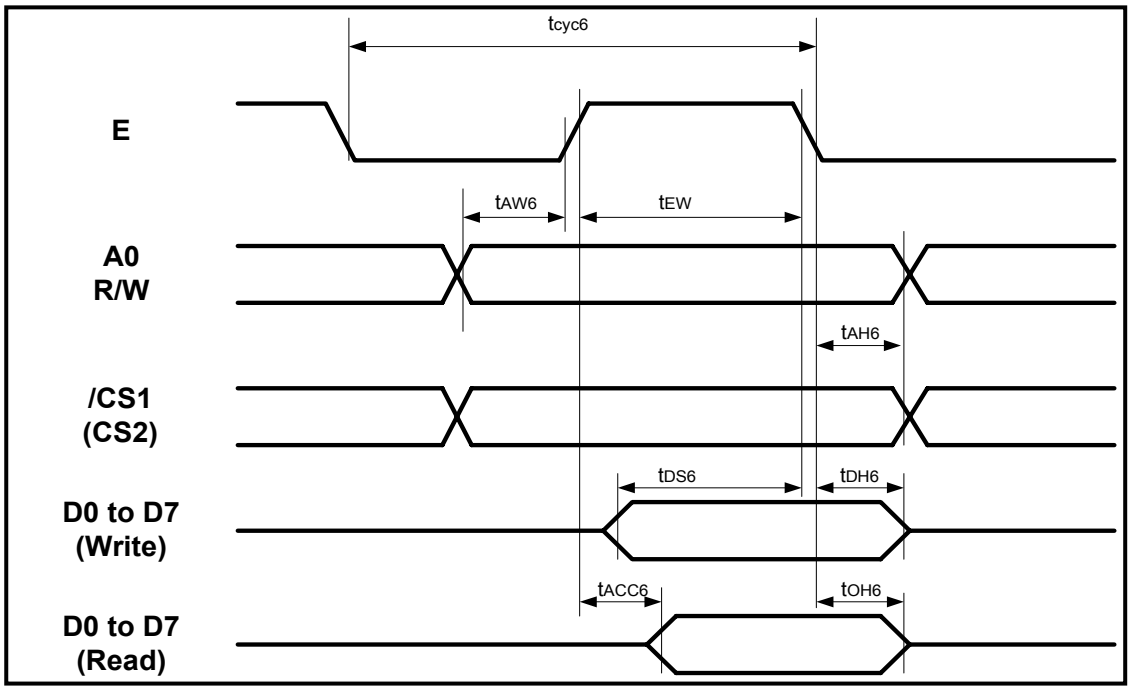
10.4.2 80-Family MPU Read/Write Timing Characteristics



VSS= 0V, VDD= 3.0 V, TA= 25°C

Parameter	Applicable Pins	Symbol	Condition	Rated Value		Unit
				Min.	Max.	
Address Setup Time Address Hold Time	A0	t_{AW8} t_{AH8}	-	0 0	-	ns
System Cycle Time	A0	t_{CYC8}	-	500	-	
Pulse Width(/WR) Pulse Width(/RD)	/WR /RD	t_{CC8}	-	160 200	-	
Data Setup Time Data Hold Time	D0~D7	t_{DS8} t_{DH8}	-	20 10	-	
Read Access Time Output Disable Time		t_{ACC8} t_{OH8}	CL=100pF	- 10	60 40	

10.4.3 68-Family MPU Read/Write Timing Characteristics

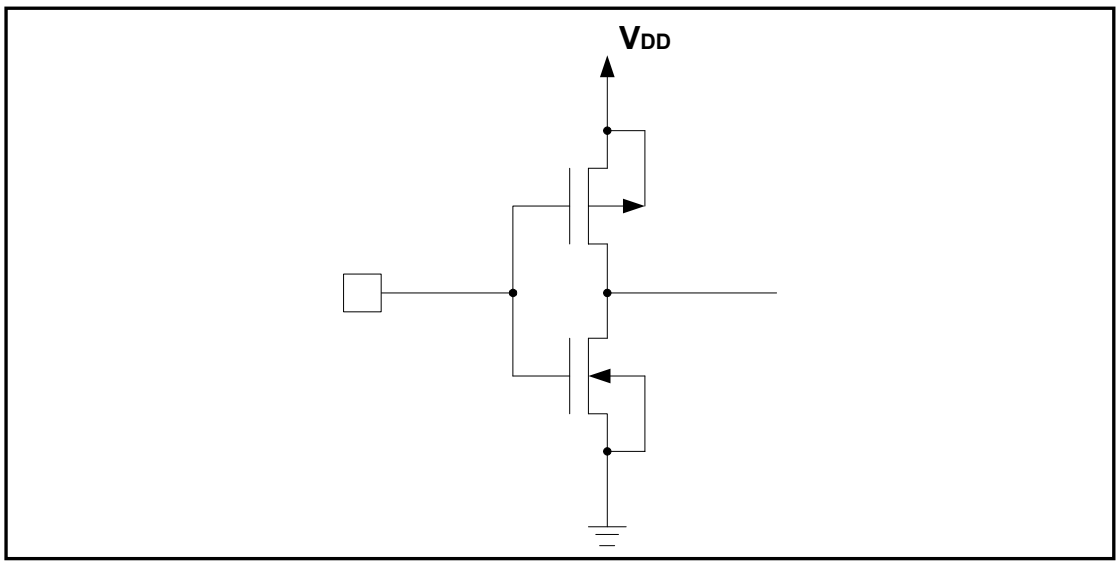


VSS= 0V, VDD= 3.0 V, TA= 25°C

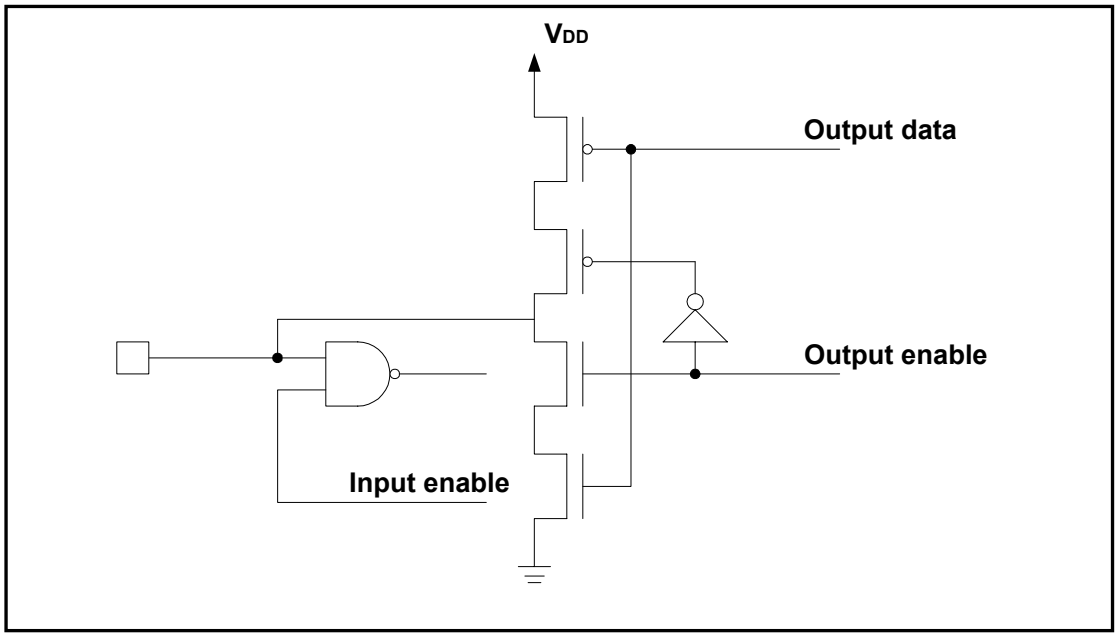
Parameter	Applicable Pins	Symbol	Condition	Rated value		Unit
				Min.	Max.	
Address Setup Time Address Hold Time	A0 R/W	t_{AW6} t_{AH6}	-	0 0	-	ns
System Cycle Time	A0	t_{CYC6}	-	500	-	
Pulse Width(/WR) Pulse Width(/RD)	E	t_{EW}	-	160 200	-	
Data Setup Time Data Hold Time	D0~D7	t_{DS6} t_{DH6}	-	20 10	-	
Read Access Time Output Disable Time		t_{ACC6} t_{OH6}	CL=100pF	- 10	60 40	

11 Pin Configuration

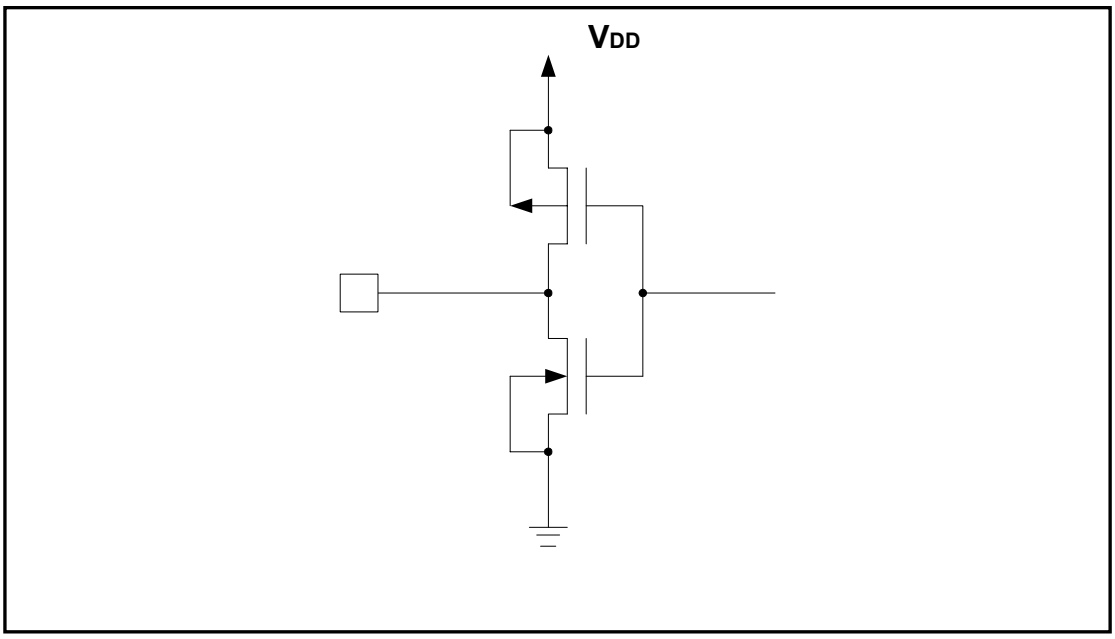
11.1 Input Pin Configuration



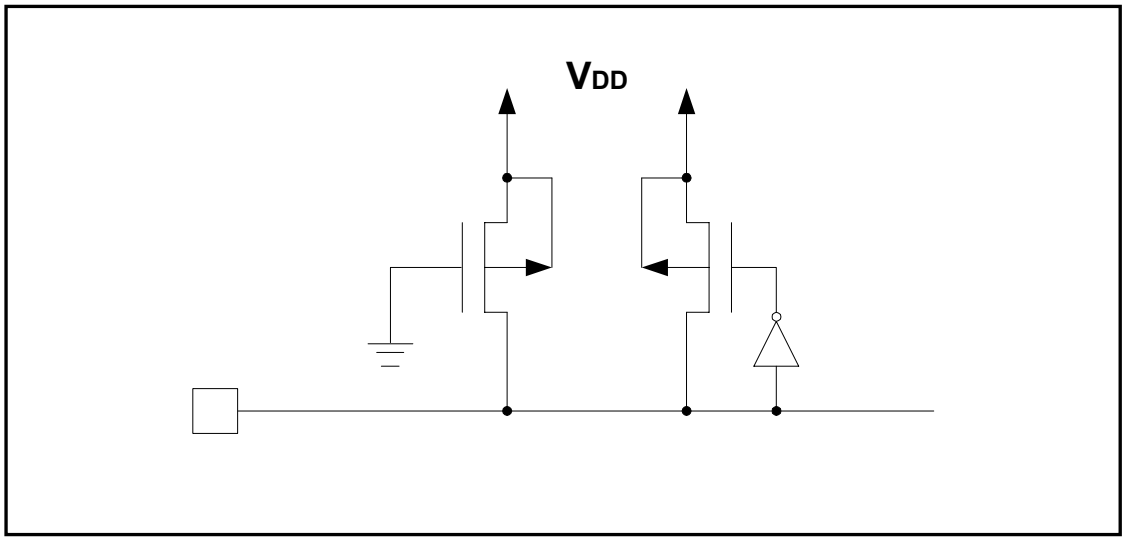
11.2 Input/Output Pin Configuration



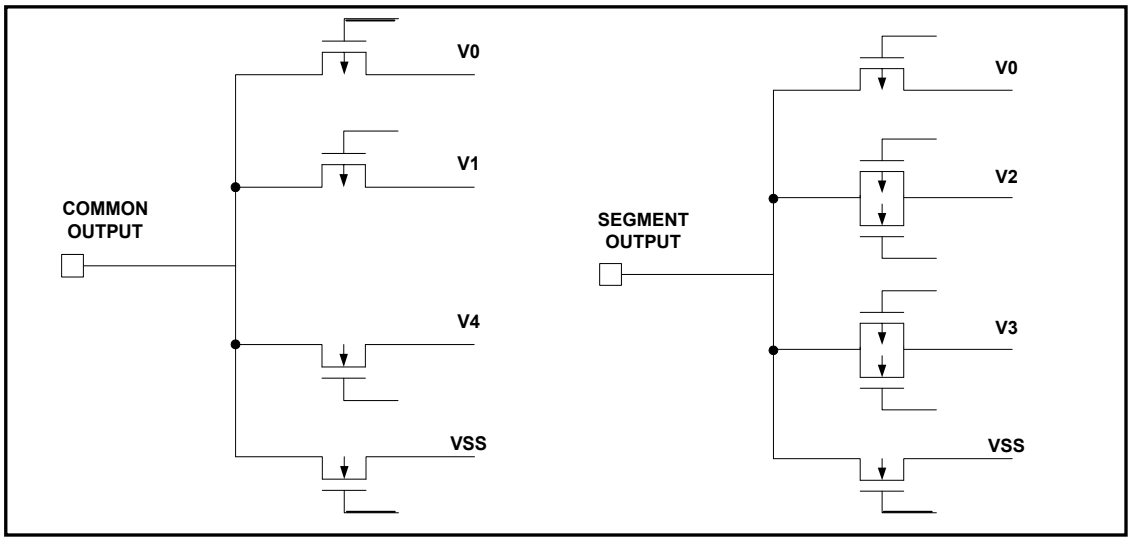
11.3 Output Pin Configuration



11.4 Reset Input Pin Configuration

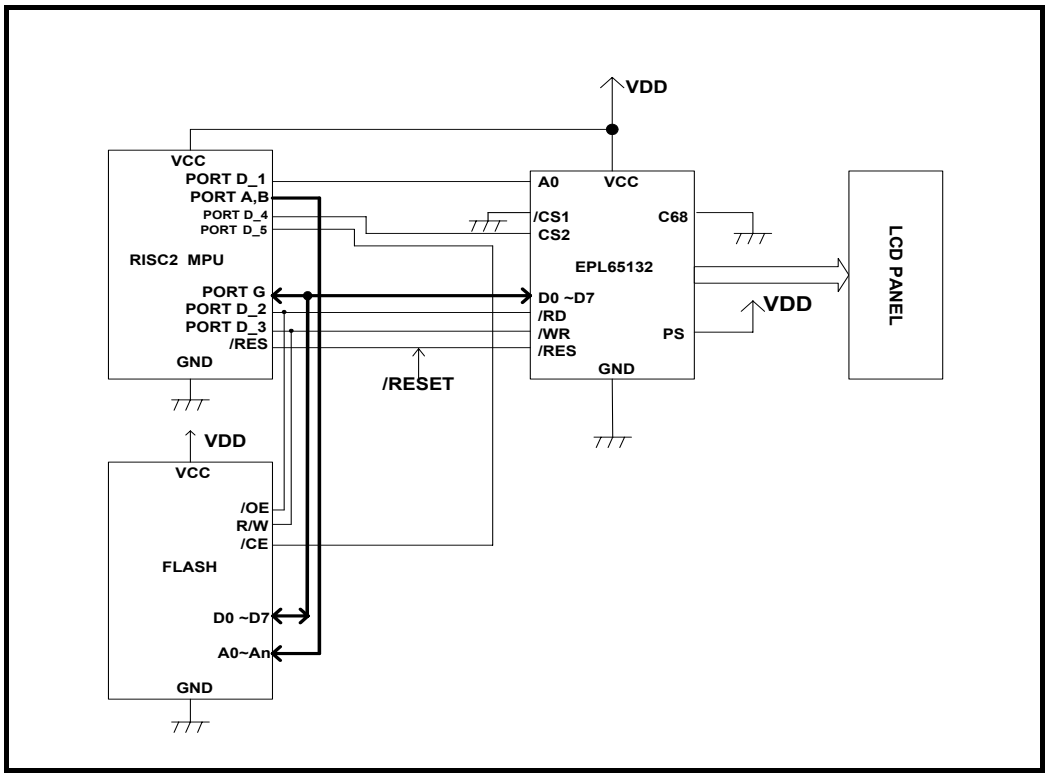


11.5 LCD Output Pin Configuration

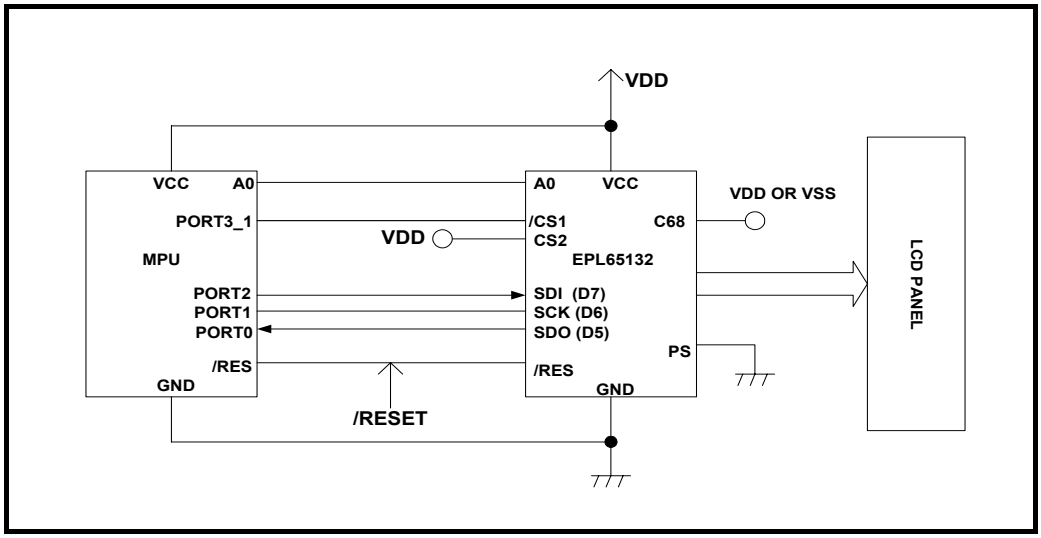


12 MPU Interface

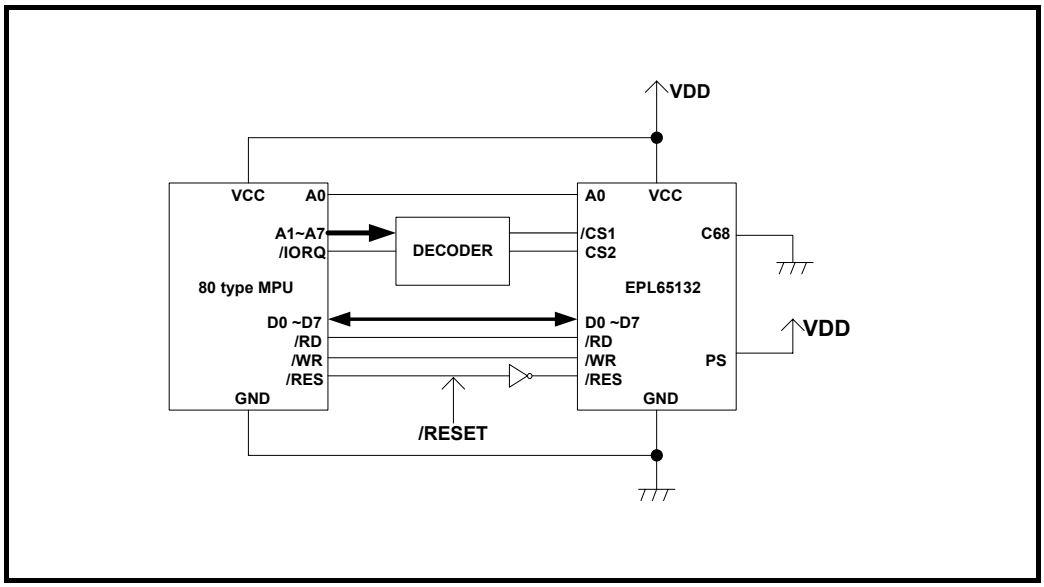
12.1 Elan 8-bit MPU (with external memory)



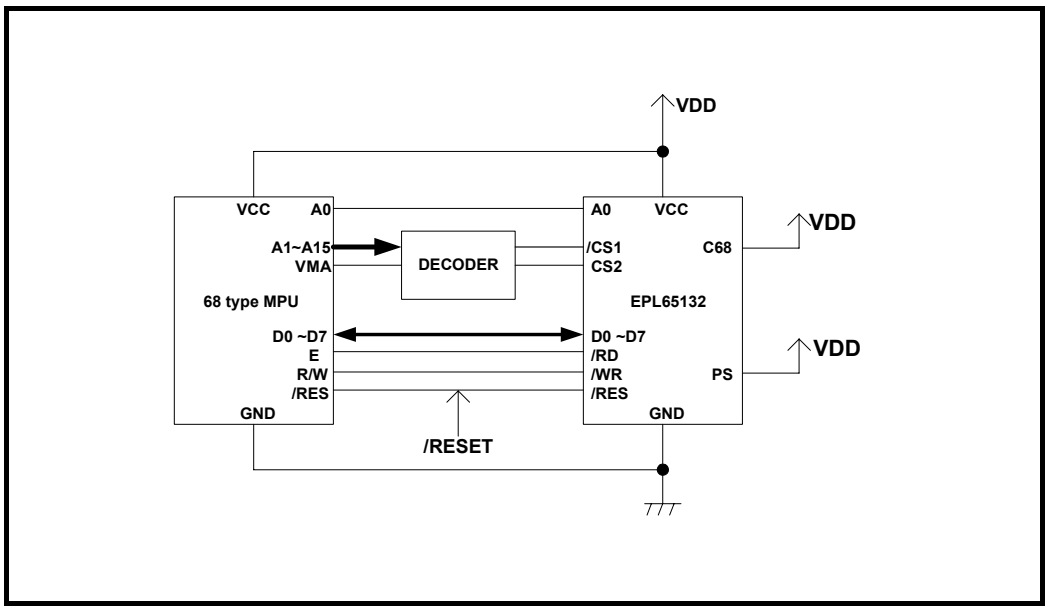
12.2 Serial Interface (SPI)



12.3 80-Family MPU



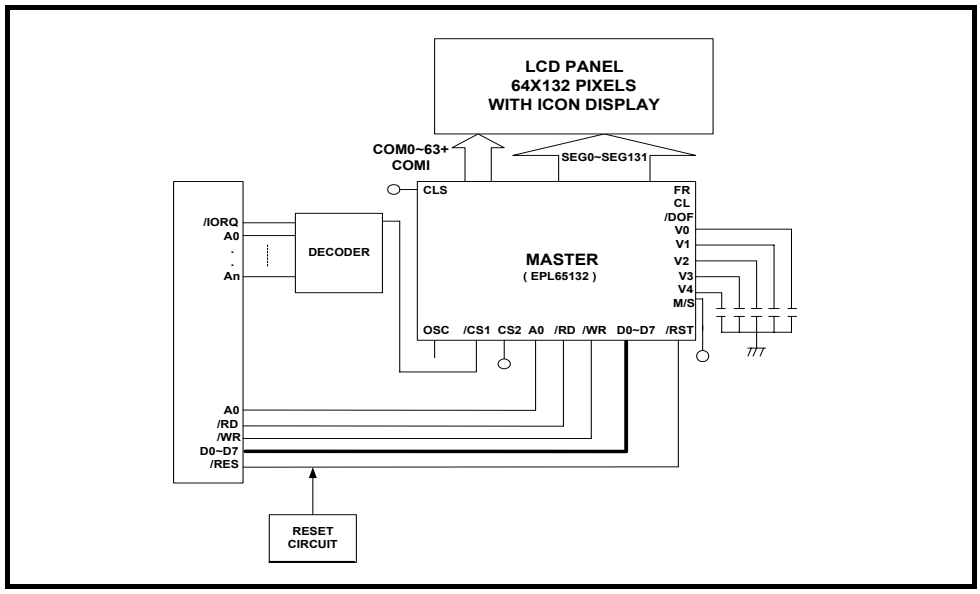
12.4 68-Family MPU



13 Application Circuits

Example 1:

65×132 pixels driving application circuits (“Single-chip” using internal oscillator)



Example 2:

65×264 pixels driving application circuits (“Multi-chip” using external oscillator)