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## 1. OVERVIEW

The SED1335 series is a controller IC that can display text and graphics on LCD panel.

The SED1335 series can display layered text and graphics, scroll the display in any direction and partition the display into multiple screens.

The SED1335 series stores text, character codes and bit-mapped graphics data in external frame buffer memory. Display controller functions include transferring data from the controlling microprocessor to the buffer memory, reading memory data, converting data to display pixels and generating timing signals for the buffer memory, LCD panel.

The SED1335 series has an internal character generator with 160, 5 × 7 pixel characters in internal mask ROM. The character generators support up to 64, 8 × 16 pixel characters in external character generator RAM and up to 256, 8 × 16 pixel characters in external character generator ROM.

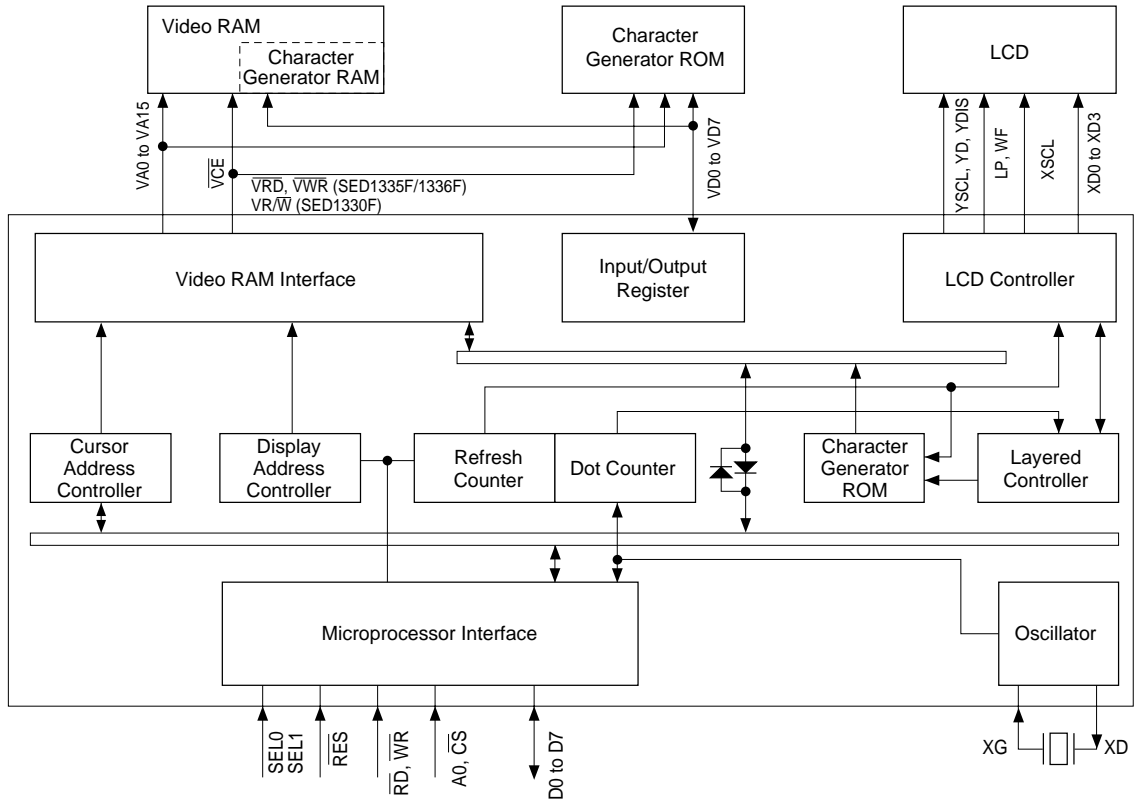
## 2. FEATURES

- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Up to 640 × 256 pixel LCD panel display resolution
- Programmable cursor control
- Smooth horizontal and vertical scrolling of all or part of the display
- 1/2-duty to 1/256-duty LCD drive
- Up to 640 × 256 pixel LCD panel display resolution memory
- 160, 5 × 7 pixel characters in internal mask-programmed character generator ROM
- Up to 64, 8 × 16 pixel characters in external character generator RAM
- Up to 256, 8 × 16 pixel characters in external character generator ROM
- 6800 and 8080 family microprocessor interfaces
- Low power consumption—3.5 mA operating current ( $V_{DD} = 3.5V$ ), 0.05  $\mu A$  standby current
- Package

line-up	Package
SED1335F0A	QFP5-60 pin
SED1335F0B	QFP6-60 pin

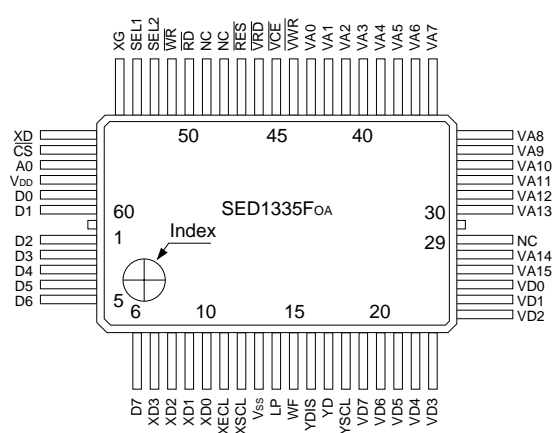
- 2.7 to 5.5 V (SED1335F)

### 3. BLOCK DIAGRAM

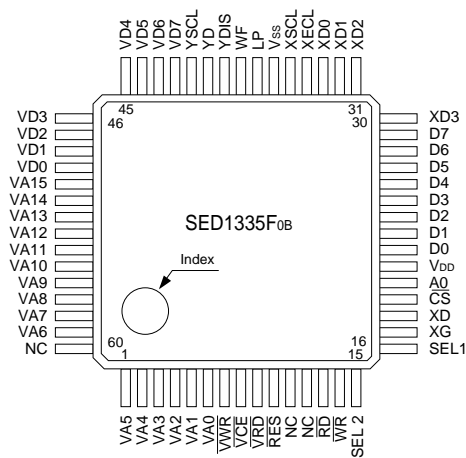


## 4. PINOUTS

◇SED1335F0A



◇SED1335F0B





## 5. PIN DESCRIPTION

### 5.1. SED1335F0A/0B Pin Summary

Name	Number		Type	Description
	SED1335F0A	SED1335F0B		
VA0 to VA15	27 to 28 30 to 43	1 to 6 50 to 59	Output	VRAM address bus
$\overline{VWR}$	44	7	Output	VRAM write signal
$\overline{VCE}$	45	8	Output	Memory control signal
$\overline{VRD}$	46	9	Output	VRAM read signal
$\overline{RES}$	47	10	Input	Reset
NC	28, 48, 49	11, 12, 60	—	No connection
$\overline{RD}$	50	13	Input	8080 family: Read signal 6800 family: Enable clock (E)
$\overline{WR}$	51	14	Input	8080 family: Write signal 6800 family: R/ $\overline{W}$ signal
SEL2	52	15	Input	8080 or 6800 family interface select
SEL1	53	16	Input	8080 or 6800 family interface select
XG	54	17	Input	Oscillator connection
XD	55	18	Output	Oscillator connection
$\overline{CS}$	56	19	Input	Chip select
A0	57	20	Input	Data type select
VDD	58	21	Supply	2.7 to 5.5V supply
D0 to D7	59 to 60 1 to 6	22 to 29	Input/output	Data bus
XD0 to XD3	7 to 10	30 to 33	Output	X-driver data
XECL	11	34	Output	X-driver enable chain clock
XSCL	12	35	Output	X-driver data shift clock
VSS	13	36	Supply	Ground
LP	14	37	Output	Latch pulse
WF	15	38	Output	Frame signal
YDIS	16	39	Output	Power-down signal when display is blanked
YD	17	40	Output	Scan start pulse
YSCL	18	41	Output	Y-driver shift clock
VD0 to VD7	19 to 26	42 to 49	Input/output	VRAM data bus

## 5.2. Pin Functions

### 5.2.1. Power supply

Pin Name	Function
VDD	2.7 to 5.5V supply. This may be the same supply as the controlling microprocessor.
VSS	Ground

**Note:** The peak supply current drawn by the SED1335 series may be up to ten times the average supply current. The power supply impedance must be kept as low as possible by ensuring that supply lines are sufficiently wide and by placing 0.47  $\mu$ F decoupling capacitors that have good high-frequency response near the device's supply pins.

### 5.2.2. Oscillator

Pin Name	Function
XG	Crystal connection for internal oscillator (See section 13). This pin can be driven by an external clock source that satisfies the timing specifications of the EXT $\phi$ 0 signal (See section 6.3.6).
XD	Crystal connection for internal oscillator. Leave this pin open when using an external clock source.

### 5.2.3. Microprocessor interface

Pin Name	Function																					
D0 to D7	Tristate input/output pins. Connect these pins to an 8- or 16-bit microprocessor bus.																					
SEL1, SEL2	Microprocessor interface select pin. The SED1335 series supports both 8080 family processors (such as the 8085 and Z80®) and 6800 family processors (such as the 6802 and 6809).																					
	<table border="1"> <thead> <tr> <th>SEL1</th> <th>SEL2*</th> <th>Interface</th> <th>A0</th> <th><math>\overline{RD}</math></th> <th><math>\overline{WR}</math></th> <th><math>\overline{CS}</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>8080 family</td> <td>A0</td> <td><math>\overline{RD}</math></td> <td><math>\overline{WR}</math></td> <td><math>\overline{CS}</math></td> </tr> <tr> <td>1</td> <td>0</td> <td>6800 family</td> <td>A0</td> <td>E</td> <td>R/W</td> <td><math>\overline{CS}</math></td> </tr> </tbody> </table>	SEL1	SEL2*	Interface	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	0	0	8080 family	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	1	0	6800 family	A0	E	R/W	$\overline{CS}$
SEL1	SEL2*	Interface	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$																
0	0	8080 family	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$																
1	0	6800 family	A0	E	R/W	$\overline{CS}$																

**Note:** SEL1 should be tied directly to VDD or VSS to prevent noise. If noise does appear on SEL1, decouple it to ground using a capacitor placed as close to the pin as possible.



























































































































































































