EPSON

SED1530 Series

LCD driver with RAM

Technical Manual

SEIKO EPSON CORPORATION

ENERGY SAVING EPSON

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SED1500 Series
Selection Guide

■ LCD drivers with RAM for small- and medium-sized displays

Ultra-low power consumption and on-chip RAM make this series ideal for compact LCD-based equipment.

SED1500 series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1510D0C	0.9–6.0	1.8–6.0	1/4	32	4	128	Serial	18 (internal)	Al pad chip	Small segment-type LCD display. Command and data interface
SED1510D0B									Au bump chip	
SED1510F0C									QFP12-48pin	
SED1510F0E									QFP6-60pin	
SED1511D0A									Al pad chip	Small segment-type LCD dislays. Data only interface
SED1520D0A	2.4–7.0	3.5–13	1/16,1/32	61	16	2,560	8-bit parallel	18 (internal, external)	Al pad chip	Dot-matrix LCD displays Extension driver is the SED1521.
SED1520D0B									Au bump chip	
SED1520F0A									QFP5-100pin	
SED1520F0C									QFP15-100pin	
SED1520T0A									TCP	
SED1520DAA								2 (external)	Al pad chip	
SED1520DAB									Au bump chip	
SED1520FAA									QFP5-100pin	
SED1520FAC									QFP15-100pin	
SED1520TAA#									TCP	
SED1521D0A			1/8–1/32	80	–			18 (external)	Al pad chip	Extension driver for the SED1520 and SED1522
SED1521D0B									Au bump chip	
SED1521F0A									QFP5-100pin	
SED1521F0C									QFP15-100pin	
SED1521T0A#									TCP	
SED1521DAA								2 (external)	Al pad chip	
SED1521DAB									Au bump chip	
SED1521FAA									QFP5-100pin	
SED1521FAC									QFP15-100pin	
SED1521TAA#									TCP	
SED152AD0A									Al pad chip	P-substrate version of SED1521
SED1522D0A			1/8,1/16	69	8			18 (internal, external)	Al pad chip	Dot-matrix LCD displays Extension driver is the SED1521.
SED1522D0B									Au bump chip	
SED1522F0A									QFP5-100pin	
SED1522F0C									QFP15-100pin	
SED1522T0A#									TCP	
SED1522DAA								2 (external)	Al pad chip	
SED1522DAB									Au bump chip	
SED1522FAA									QFP5-100pin	
SED1522FAC									QFP15-100pin	
SED1522TAA#									TCP	
SED1540D0A		3.5–11	1/3,1/4	73	3, 4			18 (internal) 4 (external)	Al pad chip	Segment-type displays
SED1540D0B									Au bump chip	
SED1540F0A									QFP5-100pin	

: Planning TCP : Tape Carrier Package

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1560D0A	2.4–6.0	6.0–16.0	1/48, 1/49 1/64, 1/65	102	65	166×65 bits	8-bit parallel or Serial	18	Al pad chip	Built-in power circuit for LCD (voltage tripler) SED1560✻0B (1/9 bias) SED1560✻AB (1/7 bias) SED1561✻0B (1/7 bias) SED1561✻AB (1/5 bias)
SED1560DAA									Al pad chip	
SED1560D0B									Au bump chip	
SED1560DAB									Au bump chip	
SED1560T0B									TCP	
SED1560TQA									QTCP	
SED1561D0A			1/24, 1/25 1/32, 1/33	134	33				Al pad chip	
SED1561DAA									Al pad chip	
SED1561D0B									Au bump chip	
SED1561DAB									Au bump chip	
SED1561T0B									TCP	
SED1561TAB									TCP	
SED1561TQA									QTCP	
SED1562D0A			1/16, 1/17 (1/5bias)	150	17				Al pad chip	
SED1562D0B									Au bump chip	
SED1562T0B									TCP	
SED1562TQA									QTCP	
SED1565D0B	1.8–5.5	4.5–16.0	1/65 (1/7, 1/9 bias)	132	65	132×65 bits		33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
SED1565D1B*									Au bump chip	
SED1565D2B									Au bump chip	
SED1565T0A									TCP	
SED1565T0B									TCP	
SED1565T0C									TCP	
SED1566D0B			1/49 (1/6, 1/8 bias)		49				Au bump chip	
SED1566D1B*									Au bump chip	
SED1566D2B									Au bump chip	
SED1566T0A									TCP	
SED1567D0B			1/33 (1/5, 1/6 bias)		33				Au bump chip	
SED1567D1B*									Au bump chip	
SED1567D2B									Au bump chip	
SED1567T0B									TCP	
SED1567T0C									TCP	
SED1568D0B			1/55 (1/6, 1/8 bias)		55				Au bump chip	
SED1569D0B			1/53 (1/6, 1/8 bias)		53				Au bump chip	
SED1569T**									TCP	
SED1570D0A	2.7–5.5	8.0–20.0	1/64–1/200	80	–	200×80 bits	4-bit parallel	–	Al pad chip	Built-in self-refreshing function
SED1570D0B									Au bump chip	
SED1526D*A	2.4–6.0	3.5–Supply voltage ×3	1/8, 1/9 1/16, 1/17		17	80×33 bits	8-bit parallel or Serial	20	Al pad chip	Built-in power circuit for LCD (voltage tripler) SED1526✻0✻ (VREG) SED1526✻E✻ (no VREG) SED1526✻A✻ (redistribution of COMS) SED1528✻0✻ (VREG) SED1528✻E✻ (no VREG)
SED1526D*B									Au bump chip	
SED1526F*A									QFP5-128pin	
SED1526T*A									TCP	
SED1528D*A			1/32, 1/33	64	33				Al pad chip	
SED1528D*B									Au bump chip	
SED1528F*A									QFP5-128pin	
SED1528T*A									TCP	

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1530D0A	2.4–6.0	4.5–16.0	1/32, 1/33	100	33	132×65 bits	8-bit parallel or Serial	–	Al pad chip	Built-in power circuit for LCD (voltage quadrupler) SED153**0* (Common: Right side) SED153**A* (Common: Both side) SED153**B* (Common: Left side) SED153**F* (no VREG)
SED1530DAA									Al pad chip	
SED1530D0B									Au bump chip	
SED1530DAB									Au bump chip	
SED1530TAA									TCP	
SED1531D0A			1/64, 1/65	132	–				Al pad chip	
SED1531D0B									Au bump chip	
SED1531T0A									TCP	
SED1532D0A				100	33				Al pad chip	
SED1532DBA									Al pad chip	
SED1532D0B									Au bump chip	
SED1532DBA									Au bump chip	
SED1532T0A									TCP	
SED1532TBA									TCP	
SED1535D0B*			1/35	98	35				Au bump chip	

TCP : Tape Carrier Package

5. SED1530 Series

Contents

OVERVIEW

The SED1530 series is a single-chip LCD driver for dot-matrix liquid crystal displays (LCD's) which is directly connectable to a microcomputer bus. It accepts 8-bit serial or parallel display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates an LCD drive signal independent of microprocessor clock.

The use of the on-chip display RAM of 65 × 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom.

As a total of 133 circuits of common and segment outputs are incorporated, a single chip of SED1530 series can make 33 × 100-dot (16 × 16-dot kanji font: 6 columns × 2 lines) displays, and a single chip of SED1531 can make 65 × 132-dot (kanji font: 8 columns x 4 lines) displays when the SED1531 is combined with the common driver SED1635.

The SED1532 can display the 65 × 200-dot (or 12-column by 4-line Kanji font) area using two ICs in master and slave modes. As an independent static indicator display is provided for time-division driving, the low-power display is realized during system standby and others.

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with a minimum current consumption and a smallest LSI configuration.

Two types of SED1530 series are available: one in which common outputs are arranged on a single side and the other in which common outputs are arranged on both sides.

FEATURES

- Direct RAM data display using the display RAM. When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed. (At normal display)
- RAM capacity: 65 × 132 = 8580 bits
- High-speed 8-bit microprocessor interface allowing direct connection to both the 8080 and 6800.
- Serial interface
- Many command functions: Read/Write Display Data, Display ON/OFF, Normal/Reverse Display, Page Address Set, Set Display Start Line, Set Column Address, Read Status, All Display ON/OFF, Set LCD Bias, Electronic contrast Controls, Read Modify Write, Select Segment Driver Direction, Power Save

• Series specifications (in cases of chip shipments)

Type 1 [V_{REG} (Built-in power supply regulating voltage)
Temperature gradient: 0.2% / °C]

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
SED1530D0∗	1/33	1/5, 1/6	100	33	33 × 100	COM single-side layout
SED1530DA∗	1/33	1/5, 1/6	100	33	33 × 100	COM dual-side layout
SED1531D0∗	1/65	1/6, 1/8	132	0	65 × 132	SED1635 is used as the COM.
SED1532D0∗	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, right-hand layout
SED1532DB∗	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, left-hand layout
SED1535DA∗	1/35	1/5, 1/6	98	35	35 × 98	COM both-side layout

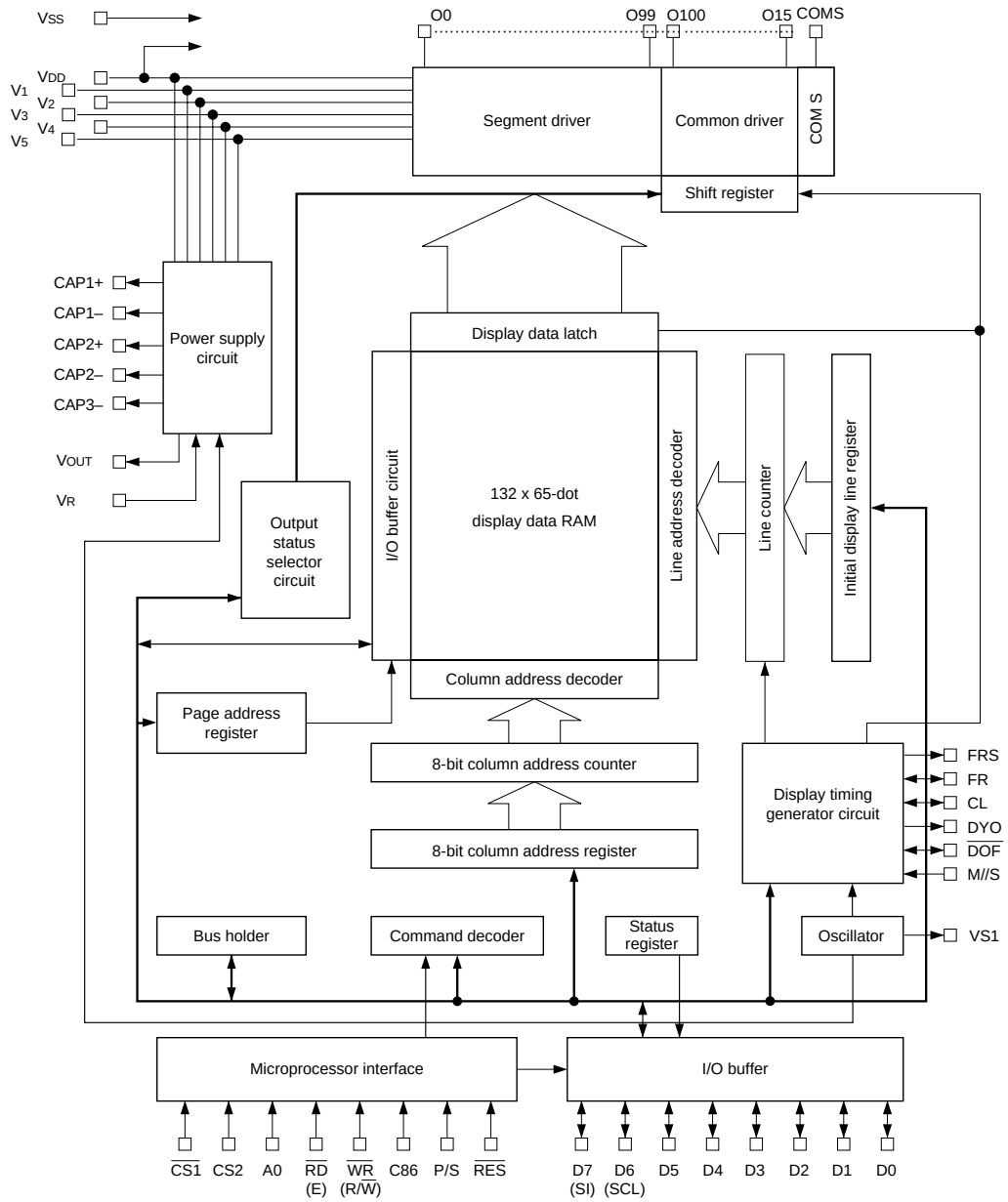
Type 2 [V_{REG} Temperature gradient: 0.00% / °C]

Name	Duty	LCD bias	Segment driver	COM driver	Display area	Remarks
SED1530DF∗	1/33	1/5, 1/6	100	33	33 × 100	COM both-side layout
SED1532DE∗	1/65	1/6, 1/8	100	33	65 × 200	COM single-side, right-hand layout
SED1533DF∗	1/17	1/5	116	17	17 × 116	COM both-side layout
SED1534DE∗	1/9	1/5	124	9	9 × 124	COM single-side layout

Note: The SED1530 series has the following subcodes depending on their shapes. (The SED1530 examples are given.)
SED1530T∗∗ : TCP (The TCP subcode differs from the inherent chip subcode.)
SED1530D∗∗ : Bear chips — SED1530D∗A : Aluminum pad
SED1530D∗B : Gold bump

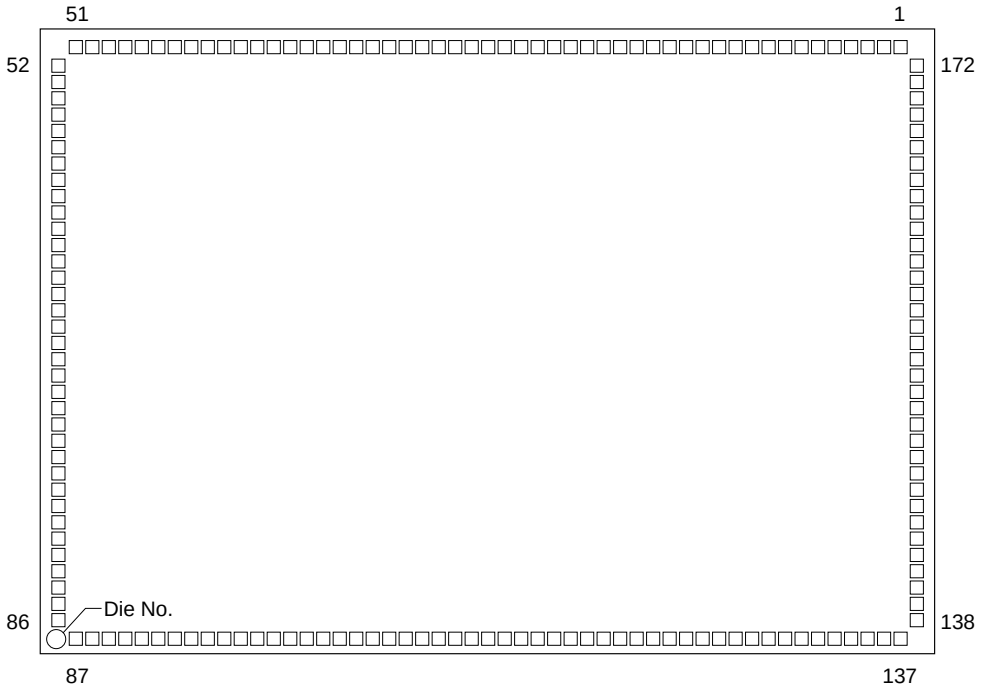
- On-chip LCD power circuit: Voltage booster, voltage regulator, voltage follower × 4.
- On-chip electronic contrast control functions
- Ultra low power consumption
- Power supply voltages: V_{DD} - V_{SS} -2.4 V to -6.0 V
  V_{DD} - V5 -4.5 V to -16.0 V
- Wide operating temperature range:
  Ta = -40 to 85°C
- CMOS process
- Package: TCP and bare chip
- Non-radiation-resistant design

BLOCK DIAGRAM (SED1530D0B)



PIN ASSIGNMENT

SED1530 series chips



Chip Size:	6.65x4.57 mm
Pad Pitch:	118 µm (Min)
SED153*D*A	(Aluminum pad model)
Pad Center Size:	90x90 µm
Chip Thickness:	300 µm
SED153*D*B	(Gold bump model)
Bump Size:	76x76 µm
Bump Height:	23µm (Typ.)
Chip Thickness:	625 µm

Pad Center Coordinates

Unit: μm

PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y	PAD No.	PIN Name	X	Y
1	O127	2986	2142	51	O5	-2986	2142	101	O55	-1298	-2142	151	O105	3178	-472
2	O128	2862		52	O6	-3178	2006	102	O56	-1180		152	O106		-354
3	O129	2738		53	O7		1888	103	O57	-1062		153	O107		-236
4	O130	2614		54	O8		1770	104	O58	-944		154	O108		-118
5	O131	2490		55	O9		1652	105	O59	-826		155	O109		0
6	COMS	2366		56	O10		1534	106	O60	-708		156	O110		118
7	FRS	2242		57	O11		1416	107	O61	-590		157	O111		236
8	FR	2124		58	O12		1298	108	O62	-472		158	O112		354
9	DYO	2006		59	O13		1180	109	O63	-354		159	O113		472
10	CL	1888		60	O14		1062	110	O64	-236		160	O114		590
11	$\overline{DOF}$	1770		61	O15		944	111	O65	-118		161	O115		708
12	VS1	1652		62	O16		826	112	O66	0		162	O116		826
13	M/S	1534		63	O17		708	113	O67	118		163	O117		944
14	$\overline{RES}$	1416		64	O18		590	114	O68	236		164	O118		1062
15	P/S	1298		65	O19		472	115	O69	354		165	O119		1180
16	$\overline{CS1}$	1180		66	O20		354	116	O70	472		166	O120		1298
17	CS2	1062		67	O21		236	117	O71	590		167	O121		1416
18	C86	944		68	O22		118	118	O72	708		168	O122		1534
19	A0	826		69	O23		0	119	O73	826		169	O123		1652
20	$\overline{WR}$(W/$\overline{R}$)	708		70	O24		-118	120	O74	944		170	O124		1770
21	$\overline{RD}$(E)	590		71	O25		-236	121	O75	1062		171	O125		1888
22	V_{DD}	354		72	O26		-354	122	O76	1180		172	O126		2006
23	D0	236		73	O27		-472	123	O77	1298					
24	D1	236		74	O28		-590	124	O78	1416					
25	D2	118		75	O29		-708	125	O79	1534					
26	D3	0		76	O30		-826	126	O80	1652					
27	D4	-118		77	O31		-944	127	O81	1770					
28	D5	-236		78	O32		-1062	128	O82	1888					
29	D6(SCL)	-354		79	O33		-1180	129	O83	2006					
30	D7(SI)	-472		80	O34		-1298	130	O84	2124					
31	V_{SS}	-590		81	O35		-1416	131	O85	2242					
32	V_{OUT}	-708		82	O36		-1534	132	O86	2366					
33	CAP3-	-826		83	O37		-1652	133	O87	2490					
34	CAP1+	-944		84	O38		-1770	134	O88	2614					
35	CAP1-	-1062		85	O39		-1888	135	O89	2738					
36	CAP2+	-1180		86	O40		-2006	136	O90	2862					
37	CAP2-	-1298		87	O41	-2986	-2142	137	O91	2986					
38	V_5	-1416		88	O42	-2862		138	O92	3178	-2006				
39	V_R	-1534		89	O43	-2738		139	O93		-1888				
40	V_{DD}	-1652		90	O44	-2614		140	O94		-1770				
41	V_1	-1770		91	O45	-2490		141	O95		-1652				
42	V_2	-1888		92	O46	-2366		142	O96		-1534				
43	V_3	-2006		93	O47	-2242		143	O97		-1416				
44	V_4	-2124		94	O48	-2124		144	O98		-1298				
45	V_5	-2242		95	O49	-2006		145	O99		-1180				
46	O0	-2366		96	O50	-1888		146	O100		-1062				
47	O1	-2490		97	O51	-1770		147	O101		-944				
48	O2	-2614		98	O52	-1652		148	O102		-826				
49	O3	-2738		99	O53	-1534		149	O103		-708				
50	O4	-2862		100	O54	-1416		150	O104		-590				

PIN DESCRIPTION

Power Supply

Name	I/O	Description	Number of pins
V_{DD}	Supply	+5V power supply. Connect to microprocessor power supply pin V_{CC}.	2
V_{SS}	Supply	Ground	1
V_1, V_2 V_3, V_4 V_5	Supply	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operational amplifier for application. Voltages should be the following relationship: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ When the on-chip operating power circuit is on, the following voltages are given to V_1 to V_4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias command. (The SED1533 and SED1534 are fixed to 1/5 bias.)	6

	SED1530/SED1535	SED1531	SED1532
V_1	1/5•V_5 1/6•V_5	1/6•V_5 1/8•V_5	1/6•V_5 1/8•V_5
V_2	2/5•V_5 2/6•V_5	2/6•V_5 2/8•V_5	2/6•V_5 2/8•V_5
V_3	3/5•V_5 4/6•V_5	4/6•V_5 6/8•V_5	4/6•V_5 6/8•V_5
V_4	4/5•V_5 5/6•V_5	5/6•V_5 7/8•V_5	5/6•V_5 7/8•V_5

	SED1533	SED1534
V_1	1/5•V_5	1/5•V_5
V_2	2/5•V_5	2/5•V_5
V_3	3/5•V_5	3/5•V_5
V_4	4/5•V_5	4/5•V_5

LCD Driver Supplies

Name	I/O	Description	Number of pins
CAP1+	O	DC/DC voltage converter capacitor 1 positive connection	1
CAP1–	O	DC/DC voltage converter capacitor 1 negative connection	1
CAP2+	O	DC/DC voltage converter capacitor 2 positive connection	1
CAP2–	O	DC/DC voltage converter capacitor 2 negative connection	1
CAP3–	O	DC/DC voltage converter capacitor 1 negative connection	1
V_{OUT}	O	DC/DC voltage converter output	1
VR	I	Voltage adjustment pin. Applies voltage between V_{DD} and V5 using a resistive divider.	1

Microprocessor Interface

Name	I/O	Description	Number of pins
D0 to D7 (SI) (SCL)	I/O	8-bit bi-directional data bus to be connected to the standard 8-bit or 16-bit microprocessor data bus. When the serial interface selects; D7: Serial data input (SI) D6: Serial clock input (SCL)	8
A0	I	Control/display data flag input. It is connected to the LSB of micro-processor address bus. When low, the data on D0 to D7 is control data. When high, the data on D0 to D7 is display data.	1
$\overline{RES}$		When $\overline{RES}$ is caused to go low, initialization is executed. A reset operation is performed at the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	Chip select input. Data input/output is enabled when -CS1 is low and CS2 is high. When chip select is non-active, D0 to D7 will be "HZ".	2
RD (E)	I	• When interfacing to an 8080 series microprocessor: Active low. This input connects the RD signal of the 8080 series microprocessor. While this signal is low, the SED1530 series data bus output is enabled. • When interfacing to a 6800 series microprocessor: Active high. This is used as an enable clock input pin of the 6800 series microprocessor.	1

Name	I/O	Description	Number of pins
$\overline{WR}$ (R/$\overline{W}$)	I	• Write enable input. When interfacing to an 8080-series microprocessor, $\overline{WR}$ is active low. • When interfacing to an 6800-series microprocessor, it will be read mode when R/$\overline{W}$ is high and it will be write mode when R/$\overline{W}$ is low. R/$\overline{W}$ = "1":Read R/$\overline{W}$ = "0":Write	1
C86	I	Microprocessor interface select terminal. C86 = high: 6800 series microprocessor interface C86 = low: 8080 series microprocessor interface	1
P/S	I	Serial data input/parallel data input select pin. P/S | Chip select | Data/command | Data | Read/write | Serial clock "H" | $\overline{CS1}$, CS2 | A0 | D0-D7 | $\overline{RD}$, $\overline{WR}$ | — "L" | $\overline{CS1}$, CS2 | A0 | SI(D7) | Write only | SCL(D6) * In serial mode, no data can be read from RAM. When P/S = low, D0 to D5 are HZ and $\overline{RD}$ and $\overline{WR}$ must be fixed high or low.	1

LCD Driver Outputs

Name	I/O	Description	Number of pins
M/S	I	SED1530 series master/slave mode select input. When a necessary signal is output to the LCD, the master operation is synchronized with the LCD system, while when a necessary signal is input to the LCD, the slave operation is synchronized with the LCD system. M/S = high: Master operation M/S = low : Slave operation The following is provided depending on the M/S status. Model | Status | OSC circuit | Power supply circuit | CL | FR | DYO | FRS | DOF SED153*D** | Master | Enabled | Enabled | Output | Output | Output | Output | Output Slave | Disabled | Disabled | Input | Input | HZ | HZ | Input	1
CL	I/O	Display clock input/output. When the SED1530 series selects master/slave mode, each CL pin is connected. When it is used in combination with the common driver, this input/output is connected to common driver YSCL pin. M/S = high: Output M/S = low: Input	1
FR	I/O	LCD AC signal input/output. When the SED1530 series selects master/slave mode, each FR pin is connected. When the SED1530 series selects master mode this input/output is connected to the common driver FR pin. M/S = high: Output M/S = low: Input	1
DYO	I/O	Common drive signal output. This output is enabled for only at master operation and connects to the common driver DIO pin. It becomes HZ at slave operation.	1
VS1	O	Internal power supply voltage monitor output.	1
$\overline{DOF}$	I/O	LCD blanking control input/output. When the SED1530 series selects master/slave mode, the respective $\overline{DOF}$ pin is connected. When it is used in combination with the common driver (SED1635), this output/input is connected to the common driver $\overline{DOFF}$ pin. M/S = high: Output M/S = low: Input	1
FRS	O	Static drive output. This is enabled only at master operation and used together with the FR pin. This output becomes HZ at slave operation.	1

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>On
(SEG n)
(Com n)</td><td>O</td><td>
LCD drive output. The following assignment is made depending on the model.
<table>
<tr><th></th><th>SEG</th><th>COM</th></tr>
<tr><td>SED1530D0*</td><td>O0~O99</td><td>O100~O131</td></tr>
<tr><td>SED1530DA*
SED1530DF*</td><td>O16~O115</td><td>O0~O15, O116~O131</td></tr>
<tr><td>SED1531D0*</td><td>O0~O131</td><td></td></tr>
<tr><td>SED1532D0*
SED1532DE*</td><td>O0~O99</td><td>O100~O131</td></tr>
<tr><td>SED1532DB*</td><td>O32~O131</td><td>O0~O31</td></tr>
<tr><td>SED1533DF*</td><td>O8~O123</td><td>O0~O7, O124~O131</td></tr>
<tr><td>SED1534DE*</td><td>O0~O123</td><td>O124~O131</td></tr>
<tr><td>SED1535DA*</td><td>O18~O115</td><td>O6~O17, O116~O131</td></tr>
</table>
SEG output. LCD segment drive output. One of V_{DD}, V_2, V_3 and V_5 levels is selected by combination of the contents of display RAM and FR signal.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">On output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td rowspan="2">0</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>–</td><td colspan="2">V_{DD}</td></tr>
</table>
COM output. LCD common drive output. One of V_{DD}, V_1, V_4 and V_5 levels is selected by combination of scan data and FR signal.
<table>
<tr><th>Scan data</th><th>FR</th><th>On output voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V_5</td></tr>
<tr><td>L</td><td>V_{DD}</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>V_4</td></tr>
<tr><td>Power save</td><td>–</td><td>V_{DD}</td></tr>
</table>
</td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator COM output. When it is not used, it is made open.
Effective only with the SED1530, SED1532, SED1533 and SED1534, SED1535 and “HZ” with the SED1531.
When multiple numbers of the SED1530, SED1532, SED1533 and SED1534, SED1535 are used, the same COMS signal is output to both master and slave units.</td><td></td></tr>
<tr><td></td><td></td><td>Total</td><td>172</td></tr>
</table>

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Interface type selection

The SED1530 series can transfer data via 8-bit bi-directional data buses (D7 to D0) or via serial data input (SI). When high or low is selected for the polarity of P/S pin, either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, RAM data cannot be read out.

Table 1

P/S	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
H	Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D0 to D5
L	Serial input	$\overline{CS1}$	CS2	A0	–	–	–	SI	SCL	(HZ)

"–" must always be high or low.

Parallel input

When the SED1530 series selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pin to go high or low as shown in Table 2.

Table 2

C86	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	WR	D0 to D7
H	6800 micro-processor bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D0 to D7
L	8080 micro-processor bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{RW}$	D0 to D7

Data Bus Signals

The SED1530 series identifies the data bus signal according to A0, E, R/$\overline{W}$, ($\overline{RD}$, $\overline{WR}$) signals.

Table 3

Common	6800 processor	8080 processor		Function
A0	(R/$\overline{W}$)	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads display data.
1	0	1	0	Writes display data.
0	1	0	1	Reads status.
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface (P/S is low)

The serial interface consists of an 8-bit shift register and a 3-bit counter. The serial data input and serial clock input are enabled when $\overline{CS1}$ is low and CS2 is high (in chip select status). When chip is not selected, the shift register and counter are reset.

Serial data of D7, D6, ..., D0 is read at D7 in this sequence when serial clock (SCL) goes high. They are converted into 8-bit parallel data and processed on rising edge of every eighth serial clock signal.

The serial data input (S1) is determined to be the display data when A0 is high, and it is control data when A0 is low. A0 is read on rising edge of every eighth clock signal.

Figure 1 shows a timing chart of serial interface signals. The serial clock signal must be terminated correctly against termination reflection and ambient noise. Operation checkout on the actual machine is recommended.

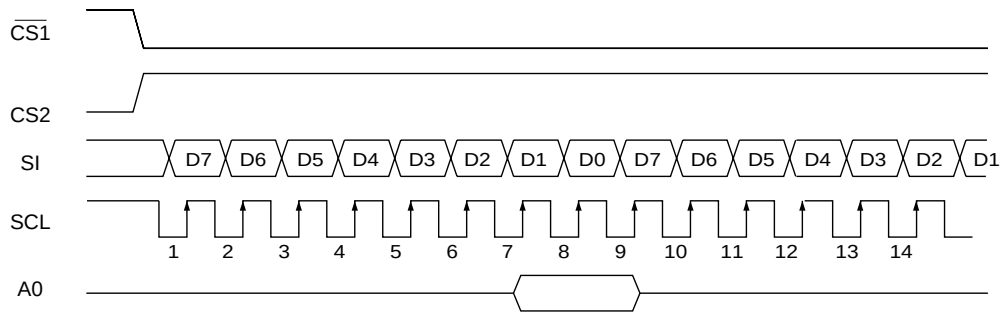


Figure 1

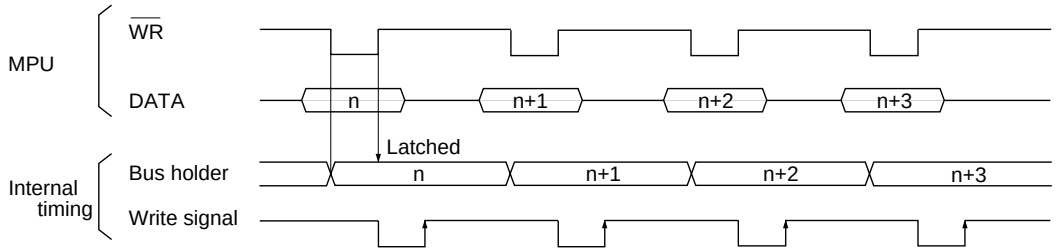
Chip Select Inputs

The SED1530 series has two chip select pins, $\overline{CS1}$ and CS2 and can interface to a microprocessor when $\overline{CS1}$ is low and CS2 is high. When these pins are set to any other combination, D0 to D7 are high impedance and A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled.
When serial input interface is selected, the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The SED1530 series can perform a series of pipeline processing between LSI's using bus holder of internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in bus holder, and outputs it onto system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in bus holder, and stores it in display RAM until the next data write cycle starts.
When viewed from the microprocessor, the SED1530 series access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}). It shows the data transfer speed to/from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during second data read. A single dummy read must be inserted after address setup and after write cycle (refer to Figure 2).

•Write



•Read

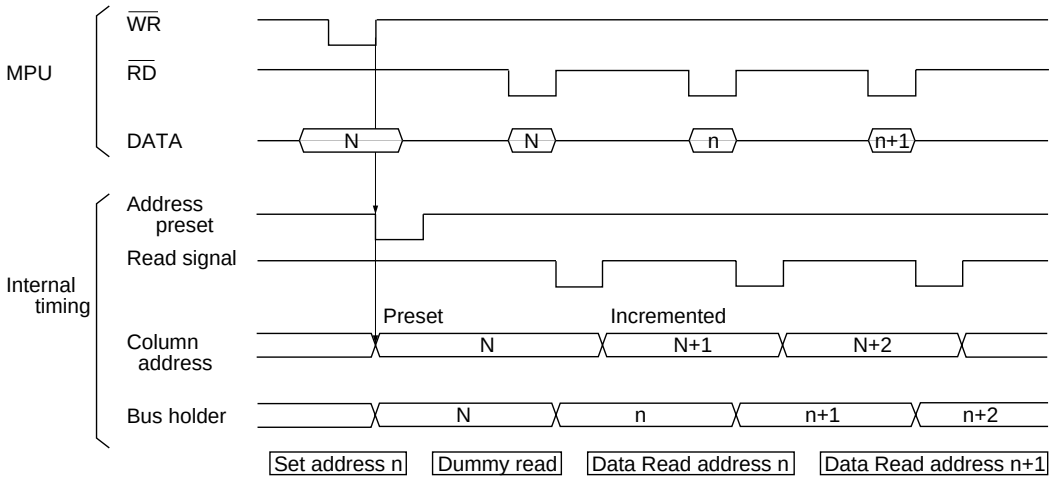


Figure 2

Busy Flag

The Busy flag is set when the SED1530 series starts to operate. During operating, it accepts Read Status instruction only. The busy flag signal is output at pin D7 when Read Status is issued. If the cycle time (t_{cyc}) is correct, the microprocessor needs not to check the flag before issuing a command. This can greatly improve the microprocessor performance.

Initial Display Line Register

When the display RAM data is read, the display line according to COM0 (usually, the top line of screen) is determined using register data. The register is also used for screen scrolling and page switching.

The Set Display Start Line command sets the 6-bit display start address in this register. The register data is preset on the line counter each time FR signal status changes. The line counter is incremented by CL signal and it generates a line address to allow 132-bit

Column Address Counter

This is a 8 bit presettable counter that provides column address to the display RAM (refer to Figure 4). It is incremented by 1 when a Read/Write command is entered. However, the counter is not incremented but locked if a non-existing address above 84H is specified. It is unlocked when a column address is set again. The Column Address counter is independent of Page Address register.
When ADC Select command is issued to display inverse display, the column address decoder inverts the relationship between RAM column address and display segment output.

Page Address Register

This is a 4-bit page address register that provides page address to the display RAM (refer to Figure 4). The microprocessor issues Set Page Address command to change the page and access to another page. Page address 8 (D3 is high, but D2, D1 and D0 are low) is RAM area dedicate to the indicator, and display data D0 is only valid.

Display Data RAM

The display data RAM stores pixel data for LCD. It is a 65-column by 132-row (8-page by 8 bit+1) addressable array. Each pixel can be selected when page and column addresses are specified.
The time required to transfer data is very short because the microprocessor enters D0 to D7 corresponding to LCD common lines as shown in Figure 3. Therefore, multiple SED1530's can easily configure a large display having the high flexibility with very few data transmission restriction.
The microprocessor writes and reads data to/from the RAM through I/O buffer. As LCD controller operates independently, data can be written into RAM at the same time as data is being displayed, without causing the LCD to flicker.

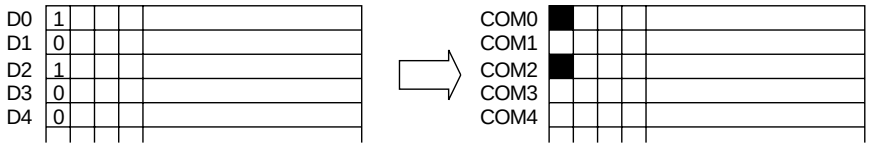


Figure 3

Relationship between display data RAM and addresses (if initial display line is 1CH):

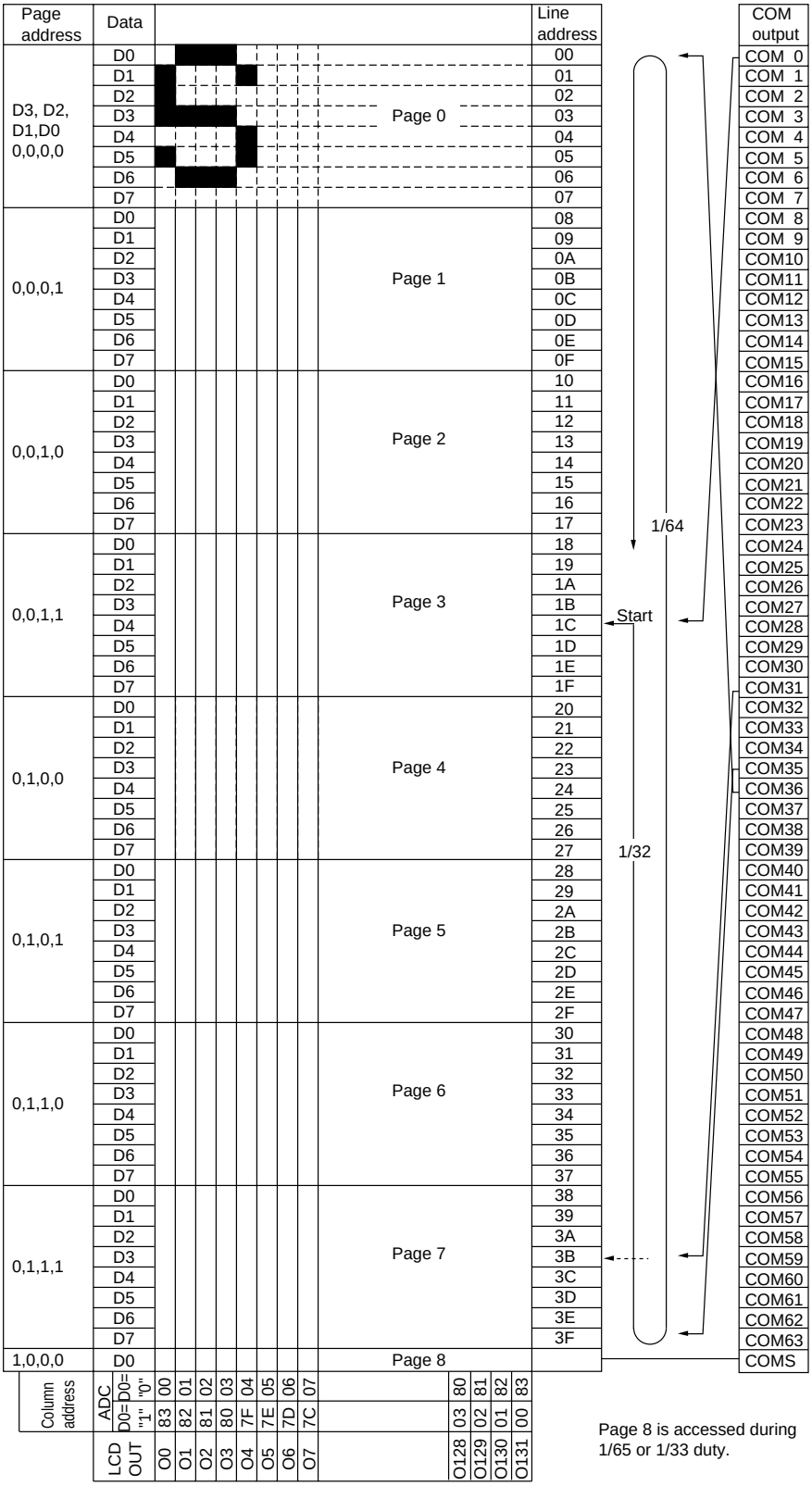


Figure 4

Output Status Selector

The SED1530 series except SED1531 can set a COM output scan direction to reduce restrictions at LCD module assembly. This scan direction is set by setting "1" or "0" in the output status register D3. Fig.5 shows the status.

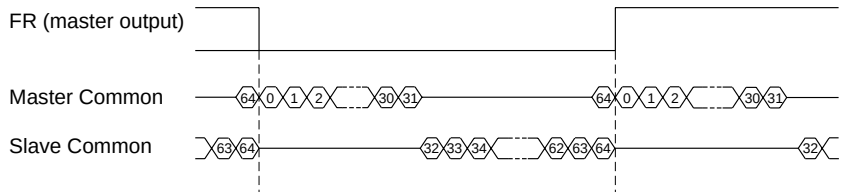
Fig. 5 shows the status.

LCD output		O0		O131
ADC (D0)	"0"	0 (H) →	Column address	→ 83 (H)
	"1"	83 (H) ←		← 0 (H)
		Display data RAM		

	D3			
SED1530D0*	0	SEG100		COM0 ---------- COM31
	1	SEG100		COM31---------- COM0
SED1530DA*	0	COM15--0	SEG100	COM16--31
SED1530DF*	1	COM16--31	SEG100	COM15--0
SED1531D0*	–	SEG132		
SED1532D0*	0	SEG100		COM0 ---------- COM31
SED1532DE*	1	SEG100		COM31---------- COM0
SED1532DB*	0	COM31---------- 0	SEG100	
	1	COM0 ---------- 31	SEG100	
SED1533DF*	0	COM7 --0	SEG116	COM8 --15
	1	COM8 --15	SEG116	COM7 --0
SED1534DE*	0	SEG124		COM0 --7
	1	SEG124		COM7 --0
SED1535DA*	0	COM17--0	SEG98	COM18--33
	1	COM18--33	SEG98	COM17--0

The COMS pin is assigned to COM32 on SED1530 and it is assigned to COM64 on SED1532 independent from their output status. The COMS pin of the SED1533 is assigned to COM16 and the COMS pin of the SED1534 is assigned to COM8.

Figure 5 shows the COM output pin numbers of SED1532D0* and SED1532DB* in the master mode. In the slave mode, COM0 to COM31 must be replaced by COM32 to COM63.



Display Timing Generator

This section explains how the display timing generator circuit operates.

Signal generation to line counter and display data latch circuit

The display clock (CL) generates a clock to the line counter and a latch signal to the display data latch circuit.
The line address of the display RAM is generated in synchronization with the display clock. 132-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
The display data is read to the LCD drive circuit completely independent of access to the display data RAM from the microprocessor.

LCD AC signal (FR) generation

The display clock generates an LCD AC signal (FR). The FR causes the LCD drive circuit to generate a AC drive waveform.
It generates a 2-frame AC drive waveform.

When the SED1530 is operated in slave mode on the assumption of multi-chip, the FR pin and CL pin become input pins.

Common timing signal generation

The display clock generates an internal common timing signal and a start signal (DYO) to the common driver. A display clock resulting from frequency division of an oscillation clock is output from the CL pin.
When an AC signal (FR) is switched, a high pulse is output as a DYO output at the training edge of the previous display clock.
Refer to Fig. 6. The DYO output is output only in master mode.
When the SED1530 series is used for multi-chip, the slave requires to receive the FR, CL, $\overline{DOF}$ signals from the master.
Table 4 shows the FR, CL, DYO and $\overline{DOF}$ status.

Table 4

Model	Operation mode	FR	CL	DYO	$\overline{DOF}$
SED153*D**	Master	Output	Output	Output	Output
	Slave	Input	Input	Hz	Input

HZ denotes a high-impedance status.

Example of SED1530D0B 1/33 duty

- **Dual-frame AC driver waveforms**

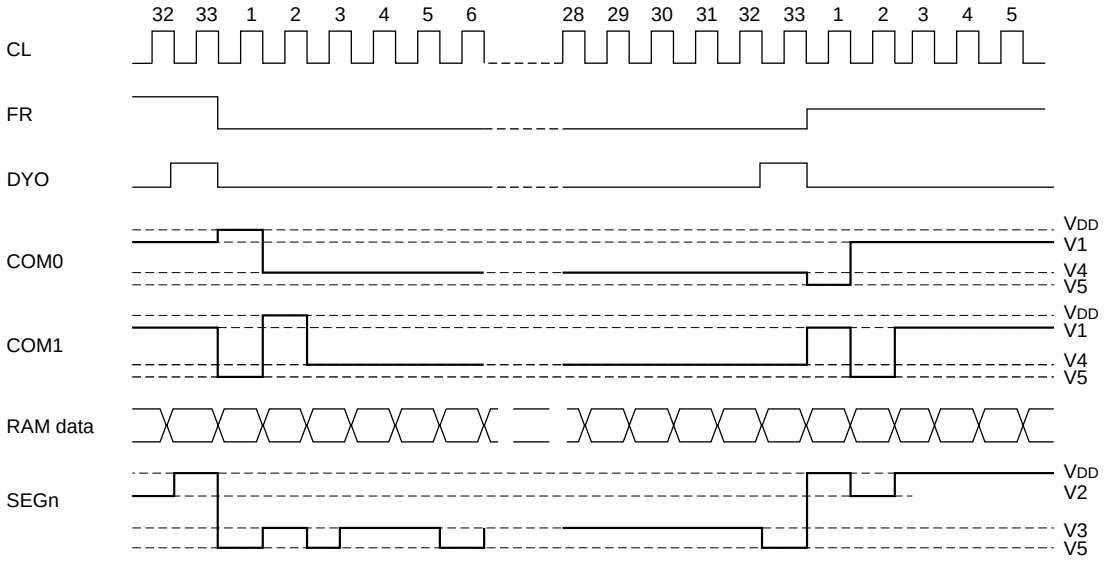


Fig. 6

Display Data Latch Circuit.

This circuit temporarily stores (or latches) display data (during a single common signal period) when it is output from display RAM to LCD panel driver circuit. This latch is controlled by Display in normal/in reverse Display ON/OFF and Static All-display on commands. These commands do not alter the data.

LCD Driver

This is a multiplexer circuit consisting of 133 segment outputs to generate four-level LCD panel drive signals. The LCD panel drive voltage is generated by a specific combination of display data, COM scan signal, and FR signal. Figure 8 gives an example of SEG and COM output waveforms.

Oscillator Circuit

This is an oscillator having a complete built-in type CR, and its output is used as the display timing signal source or as the clock for voltage booster circuit of the LCD power supply.
The oscillator circuit is available in master mode only.
The oscillator signal is divided and output as display clock at CL pin.

Power Supply Circuit

The power supply circuit generates voltage to drive the LCD panel at low power consumption, and is available in SED1530 master mode only. The power supply circuit consists of a voltage booster voltage regulator, and LCD drive voltage follower.
The power supply circuit built in the SED1530 series is set for a small-scale LCD panel and is inappropriate to a large-pixel panel and a large-display-capacity LCD panel using multiple chips. As the large LCD panel has the dropped display quality due to a large load capacity, it must use an external power source.

The power circuit is controlled by Set Power Control command. This command sets a three-bit data in Power Control register to select one of eight power circuit functions. The external power supply and part of internal power circuit functions can be used simultaneously. The following explains how the Set Power Control command works.

[Control by Set Power Control command]

D2 turns on when triple booster control bit goes high, and D2 turns off when this bit goes low.

D1 turns on when voltage regulator control bit goes high, and D1 turns off when this bit goes low.

D0 turns on when voltage follower control bit goes high, and D0 turns off when this bit goes low.

[Practical combination examples]
Status 1: To use only the internal power supply.
Status 2: To use only the voltage regulator and voltage follower.
Status 3: To use only the voltage follower. input the external voltage as V5=Vout.
Status 4: To use only an external power supply because the internal power supply does not operate.

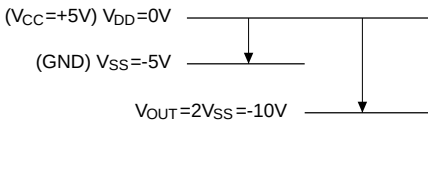
* The voltage booster terminals are CAP1+, CAP1-, CAP2+, CAP2- and CAP3-.
* Combinations other than those shown in the above table are possible but impractical.

	D2 D1 D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Voltage booster terminal	Voltage regulator terminal
①	1 1 1	ON	ON	ON	—	Used	Used
②	0 1 1	OFF	ON	ON	V_{OUT}	OPEN	Used
③	0 0 1	OFF	OFF	ON	V_5	OPEN	OPEN
④	0 0 0	OFF	OFF	OFF	V_1 to V_5	OPEN	OPEN

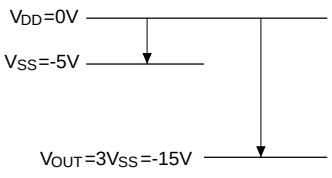
Booster circuit

If capacitors C1 are inserted between CAP1+ and CAP1-, between CAP2+ and CAP2-, CAP1+ and CAP3- and VSS and VOUT, the potential between VDD and VSS is boosted to quadruple toward the negative side and it is output at VOUT.
For triple boosting, remove only capacitor C1 between CAP+1 and CAP3- from the connection of quadruple boosting operation and jumper between CAP3- and VOUT. The triple boosted voltage appears at VOUT (CAP3-).

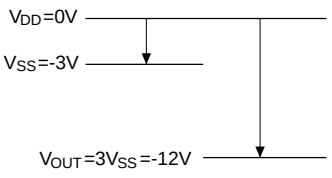
For double boosting, remove only capacitor C1 between CAP2+ and CAP2- from the connection of triple boosting operation, open CAP+2 and jumper between CAP2- and VOUT (CAP3-). The double boosted voltage appears at VOUT (CAP3-, CAP2-).
For quadruple boosting, set a VSS voltage range so that the voltage at VOUT may not exceed the absolute maximum rating.
As the booster circuit uses signals from the oscillator circuit, the oscillator circuit must operate.
Subsection 10.1.1 gives an external wiring example to use master and slave chips when on-board power supply is active.



Potential during double boosting



Potential during triple boosting



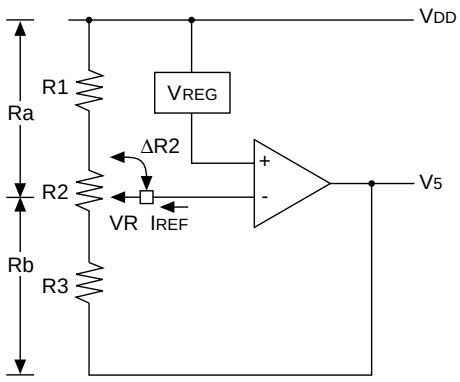
Potential during quadruple boosting

Voltage regulator circuit

The boosting voltage occurring at V_{OUT} is sent to the voltage regulator and the V_5 liquid crystal display (LCD) driver voltage is output. This V_5 voltage can be determined by the following equation when resistors Ra and Rb (R1, R2 and R3) are adjusted within the range of $|V5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) V_{REG} + I_{REF} \cdot Rb$$

$$= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) V_{REG} + I_{REF} \cdot (R3+R2-\Delta R2)$$



V_{REG} is the constant voltage source of the IC, and in case of Type 1, it is constant and $V_{REG} \fallingdotseq -2.55$ V (if V_{DD} is 0 V), In case of Type 2, $V_{REG}=V_{SS}$ (V_{DD} basis). To adjust the V_5 output voltage, insert a variable resistor between V_R, V_{DD} and V_5 as shown. A combination of R1 and R3 constant resistors and R2 variable resistor is recommended for fine-adjustment of V_5 voltage.

Setup example of resistors R1, R2 and R3:

When the Electronic Volume Control Function is OFF (electronic volume control register values are (D4,D3,D2,D1,D0)=(0,0,0,0,0)):

$$V_5 = \frac{(1 + R3 + R2 - \Delta R2)}{R1 + \Delta R2} V_{REG} \quad \cdots\cdots \textcircled{1}$$

(As I_{REF} = 0 A)

- R1 + R2 + R3 = 5MΩ ..... ②
  (Determined by the current passing between V_{DD} and V_5)
- Variable voltage range by R2 V_5 = –6 to –10 V
  (Determined by the LCD characteristics)
  ΔR2 = OΩ, V_{REG} = –2.55V
  To obtain V_5 = -10 V, from equation ①:
  R2 + R3 = 2.92 × R1 ..... ③
  ΔR2 = R2, V_{REG} = –2.55V
  To obtain V_5 = -6 V, from equation ①:
  1.35 × (R1 + R2) = R3 ..... ④

From equations ②, ③ and ④:
R1=1.27MΩ
R2=0.85MΩ
R3=2.88MΩ

The voltage regulator circuit has a temperature gradient of approximately -0.2%/°C as the V_{REG} voltage. To obtain another temperature gradient, use the Electronic Volume Control Function for software processing using the MPU.

As the V_R pin has a high input impedance, the shielded and short lines must be protected from a noise interference.

Voltage regulator using the Electronic Volume Control Function

The Electronic Volume Control Function can adjust the intensity (brightness level) of liquid crystal display (LCD) screen by command control of V_5 LCD driver voltage.
This function sets five-bit data in the electronic volume control register, and the V_5 LCD driver voltage can be one of 32-state voltages.
To use the Electronic Volume Control Function, issue the Set Power Control command to simultaneously operate both the voltage regulator circuit and voltage follower circuit.
Also, when the boosting circuit is off, the voltage must be supplied from V_{OUT} terminal.
When the Electronic Volume Control Function is used, the V_5 voltage can be expressed as follows:

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) V_{REG} + Rb \times \Delta I_{REF} \quad \cdots\cdots \textcircled{5}$$

Variable voltage range

The increased V_5 voltage is controlled by use of I_{REF} current source of the IC. (For 32 voltage levels, $\Delta I_{REF} = I_{REF}/31$)

The minimum setup voltage of the V_5 absolute value is determined by the ratio of external Ra and Rb, and the increased voltage by the Electronic Volume Control Function is determined by resistor Rb. Therefore, the resistors must be set as follows:

1) Determine Rb resistor depending on the V_5 variable voltage range by use of the Electronic Volume Control.

$$Rb = \frac{V_5 \text{ variable voltage range}}{I_{REF}}$$

2) To obtain the minimum voltage of the V_5 absolute value, determine Ra using the Rb of Step 1) above.

$$Ra = \frac{Rb}{\frac{V_5}{V_{REG}} - 1} \qquad \{V_5 = (1 + Rb/Ra) \times V_{REG}\}$$

The SED1526 series have the built-in V_{REG} reference voltage and I_{REF} current source which are constant during voltage variation. However, they may change due to the variation occurring in IC manufacturing and due to the temperature change as shown below. Consider such variation and temperature change, and set the Ra and Rb appropriate to the LCD used.

V_{REG} = –2.55V±0.20V (Type1)	V_{REG} = –0.2%/°C
V_{REG} = V_{SS} (V_{DD} basis) (Type2)	V_{REG} = –0.00%/°C
I_{REF} = –3.2µA±40% (For 16 levels)	I_{REF} = 0.023µA/°C
–6.5µA±40% (For 32 levels)	0.052µA/°C

Ra is a variable resistor that is used to correct the V_5 voltage change due to V_{REG} and I_{REF} variation. Also, the contrast adjustment is recommended for each IC chip.
Before adjusting the LCD screen contrast, set the electronic volume control register values to (D4,D3,D2,D1,D0)=(1,0,0,0,0) or (0,1,1,1,1) first.
When not using the Electronic Volume Control Function, set the register values to (D4,D3,D2,D1,D0)=(0,0,0,0,0) by sending the $\overline{RES}$ signal or the Set Electronic Volume Control Register command.

Setup example of constants when Electronic Volume Control Function is used:

V_5 maximum voltage:	V_5 = –6 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (0,0,0,0,0))
V_5 minimum voltages:	V_5 = –10 V (Electronic volume control register values (D4,D3,D2,D1,D0) = (1,1,1,1,1))
V_5 variable voltage range:	4 V
Variable voltage levels:	32 levels

1) Determining the Rb:

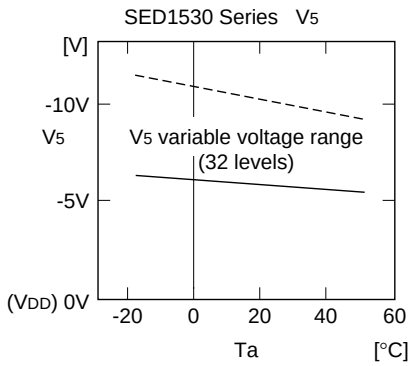
$$R3 = \frac{V_5 \text{ variable voltage range}}{|I_{REF}|} = \frac{4V}{6.5\mu A} \quad \underline{Rb = 625K\Omega}$$

2) Determining the Ra:

$$Ra = \frac{Rb}{\frac{V_5max}{V_{REG}} - 1} = \frac{625k\Omega}{\frac{-6V}{-2.55V} - 1} \qquad \underline{Ra = 462K\Omega}$$

Ta=25°C

$V_5max = (1+Rb/Ra) \times V_{REG}$
$= (1+625k/442k) \times (-2.55V)$
$= -6.0V$
$V_5min = V_5 max + Rb \times I_{REF}$
$= -6V + 625k \times (-6.5\mu A)$
$= -10.0V$



According to the V_5 voltage and temperature change, equation ⑤ can be as follows (if V_{DD} = 0 V reference):

Ta=–10°C

$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=–10°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (-10°C-25°C)\}$
$= -6.42V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=–10°C)
$= -6.42V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times (-10°C-25°C)\}$
$= -11.63V$

Ta=–50°C

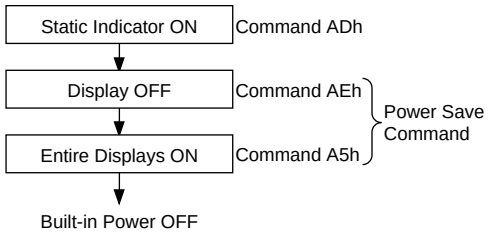
$V_5max = (1+Rb/Ra) \times V_{REG}$ (Ta=50°C)
$= (1+625k/462k) \times (-2.55V)$
$\times \{1+(-0.2\%/°C) \times (50°C-25°C)\}$
$= -5.7V$
$V_5min = V_5max + Rb \times I_{REF}$ (Ta=50°C)
$= -5.7V + 625k$
$\times \{-6.5\mu A+(0.052\mu A/°C) \times (50°C-25°C)\}$
$= -8.95V$

The margin must also be determined in the same procedure given above by considering the V_{REG} and I_{REF} variation. This margin calculation results show that the V_5 center value is affected by the V_{REG} and I_{REF} variation. The voltage setup width of the Electronic Volume Control depends on the I_{REF} variation. When the typical value of 0.2 V/step is set, for example, the maximum variation range of 0.12 to 0.28 V must be considered.

In case of Type 2, it so becomes that V_{REG} = V_{SS} (V_{DD} basis) and there is no temperature gradient. However, I_{REF} carries the same temperature characteristics as with Type 1.

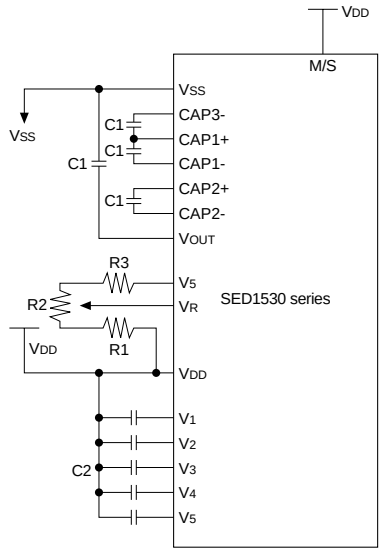
Command Sequence when Built-in Power Supply is Turned OFF

To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system into the standby mode.

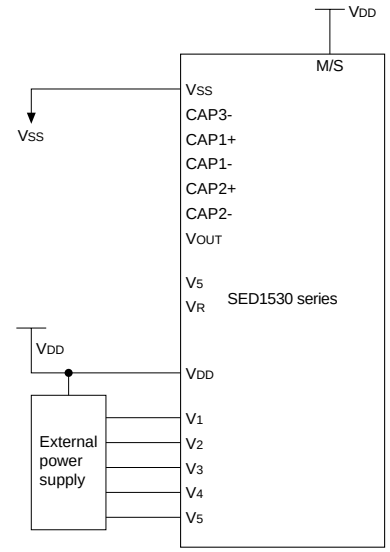


Voltage generator circuit

when the on-chip power circuit is used



when the on-chip power circuit is used



Reference setup value: SED1530 $V_5 \fallingdotseq$ -7 to -9 V
SED1531 $V_5 \fallingdotseq$ -11 to -13 V (variable)
SED1532 $V_5 \fallingdotseq$ -11 to -13 V (variable)

	SED1530	SED1531	SED1532
C1	1.0~4.7 uF	1.0~4.7 uF	1.0~4.7 uF
C2	0.22~0.47 uF	0.47~1.0 uF	0.47~1.0 uF
R1	700 KΩ	1 MΩ	1 MΩ
R2	200 KΩ	200 KΩ	200 KΩ
R3	1.6 MΩ	4 MΩ	4 MΩ
LCD SIZE	16 × 50 mm	32 × 64 mm	32 × 100 mm
DOT CONFIGURATION	32 × 100	64 × 128	64 × 200

1: As the input impedance of V_R is high, a noise protection using short wire and cable shield is required.

*2: C1 and C2 depend on the capacity of the LCD panel to be driven. Set a value so that the LCD drive voltage may be stable.

[Setup example]
Turn on the voltage regulator and voltage follower and give an external voltage to V_{OUT}. Display a horizontal-stripe LCD heavy load pattern and determine C2 so that the LCD drive voltage (V_1 to V_5) may be stable. However, the capacity value of C2 must be all equal. Next, turn on all the on-board power supplies and determine C1.

*3: LCD SIZE means the length and breadth of the display portion of the LCD panel.

Model	LCD drive voltage
SED1530	1/5 or 1/6 bias
SED1531 SED1532	1/6 or 1/8 bias

Reset Circuit

When the RES input goes low, this LSI is initialized.

Initialized status

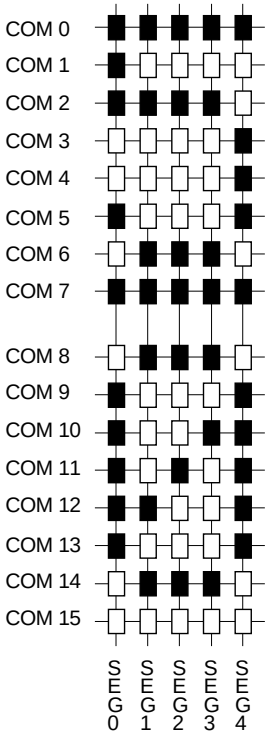
1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = low)
4. Read modify write OFF
5. Power control register (D2, D1, D0) = (0, 0, 0)
6. Register data clear in serial interface
7. LCD power supply bias ratio 1/6 (SED1530), 1/8 (SED1531, SED1532)
8. Static indicator: OFF
9. Display start line register set at line 1
10. Column address counter set at address 0
11. Page address register set at page 0
12. Output status register (D3) = (0)
13. Electronic control register set at 0
14. Test command OFF

As seen in 11. Microprocessor Interface (Reference Example), connect the $\overline{RES}$ pin to the reset pin of the microprocessor and initialize the microprocessor at the same time.

In case the SED1530 series does not use the internal LCD power supply circuit, the $\overline{RES}$ must be low when the external LCD power supply is turned on.

When $\overline{RES}$ goes low, each register is cleared and set to the above initialized status. However, it has no effect on the oscillator circuit and output pins (FR, CL, DYO, D0 to D7).
The initialization by $\overline{RES}$ pin signal is always required during power-on. If the control signal from the MPU is HZ, an overcurrent may flow through the IC. A protection is required to prevent the HZ signal at the input pin during power-on.

Be sure to initialize it by $\overline{RES}$ pin when turning on the power supply. When the reset command is used, only parameters 8 to 14 in the above initialization are executed.


COM 0
COM 1
COM 2
COM 3
COM 4
COM 5
COM 6
COM 7
COM 8
COM 9
COM 10
COM 11
COM 12
COM 13
COM 14
COM 15
SEG 0
SEG 1
SEG 2
SEG 3
SEG 4

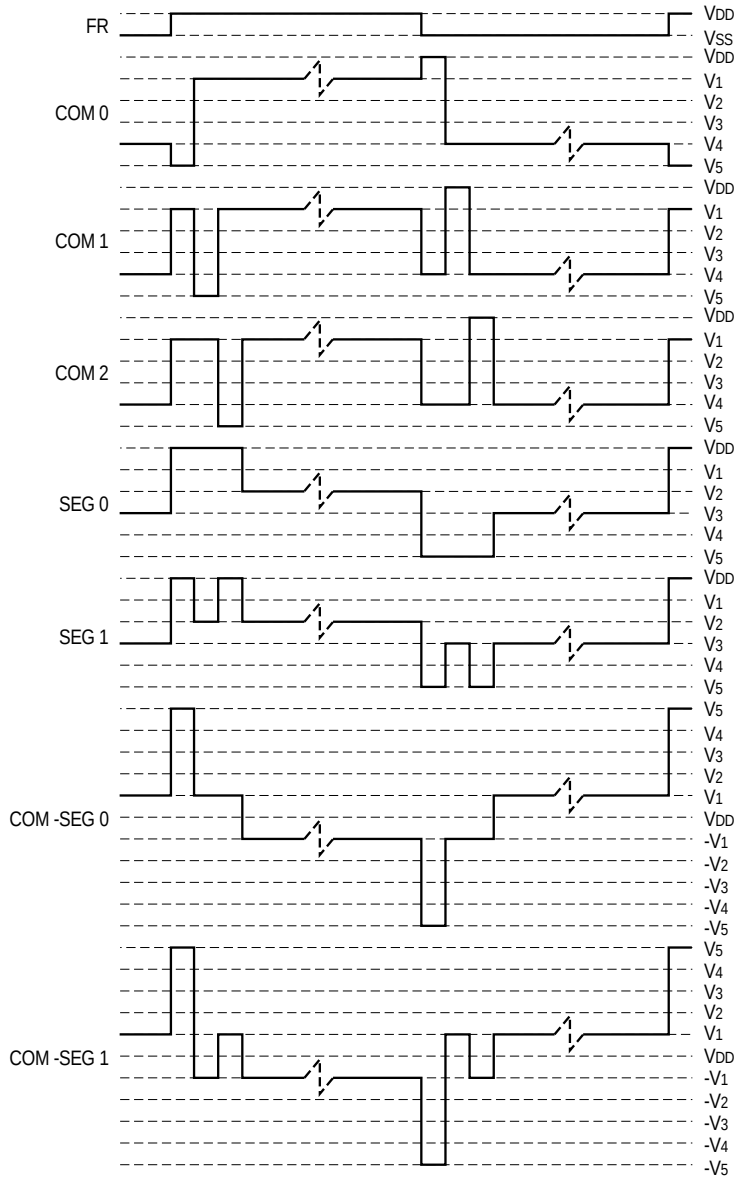

FR
VDD
VSS
COM 0
V1
V2
V3
V4
V5
COM 1
COM 2
SEG 0
SEG 1
COM -SEG 0
-V1
-V2
-V3
-V4
-V5
COM -SEG 1

Figure 8

COMMANDS

The SED1530 series uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pin and a write status when a low pulse is input to the $\overline{WR}$ pin. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/$\overline{W}$ pin and a write status when a low pulse is input to this pin. When a high pulse is input to the E pin, the command is activated. (For timing, see Timing Characteristics.) Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1 (high) when the 6800 series microprocessor interface reads status or display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands will be explained below.
When the serial interface is selected, input data starting from D7 in sequence.

• Command set

(1) Display ON/OFF
Alternatively turns the display on and off.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

The display turns off when D goes low, and it turns on when D goes high.

(2) Start Display Line
Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	6 2
1	1	1	1	1	1	6 3

(3) Set Page Address
Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicate to the indicator, and only D0 is valid for data change.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page Address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

(4) Set Column Address
Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access to the display RAM, the column address counter is incremented by 1 during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	1 3 1

(5) Read Status

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: When high, the SED1526 series is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is normal and column address "131-n" corresponds to segment driver n. When high, the display is reversed and column address n corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When goes low, the display turns on. When goes high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by $\overline{RES}$ signal or by Reset command. When low, the display is on. When high, the chip is being reset.

(6) Write Display Data
Writes 8-bit data in display RAM. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Read Display Data
Reads 8-bit data from display RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select
Changes the relationship between RAM column address and segment driver. The order of segment driver output pins can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, the right rotation (normal direction). When D is high, the left rotation (reverse direction).

(9) Normal/Reverse Display
Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display).
When D is high, the RAM data is low, being LCD ON potential (reverse display).

(10) Entire Display ON
Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.
This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided.
If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power Save mode. Refer to the Power Save section for details.

(11) Set LCD Bias
Selects a bias ratio of the voltage required for driving the LCD. This command is enabled when the voltage follower in the power supply circuit operates.
(The LCD bias setting command is invalid for the SED1533 and SED1534. They are being fixed to the 1/5 bias.)

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	D

The potential V_5 is resistively divided inside the IC to produce potentials V_1, V_2, V_3 and V_4 which are necessary to drive the LCD. The bias ratio can be selected using the LCD bias setting command. (The SED1533 and SED1534 are fixed to 1/5 bias.)
Moreover, the potentials V_1, V_2, V_3 and V_4 are converted in the impedance and supplied to the LCD drive circuit.

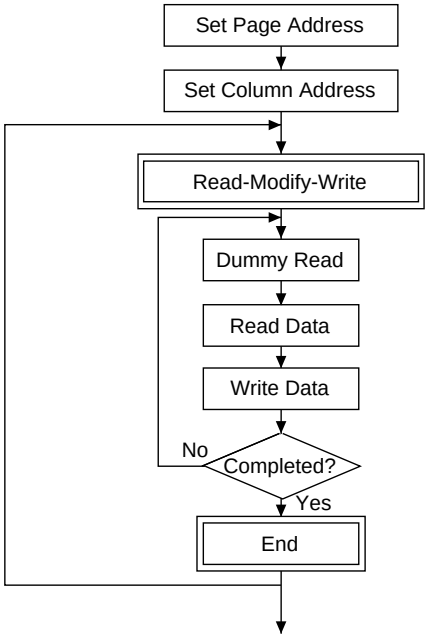
Model	Bias ratio of LCD power supply
SED1530	1/5 bias or 1/6 bias
SED1531 SED1532	1/6 bias or 1/8 bias
SED1533 SED1534	1/5 bias

(12) Read-Modify-Write
A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremented by Read Display Data command but incremented by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write was issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

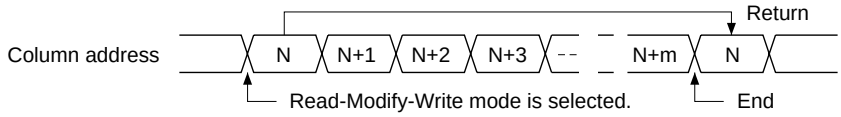
• Cursor display sequence



(13) End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write was issued).

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



(14) Reset

Resets the Initial Display Line register, Column Address counter, Page Address register, and output status selector circuit to their initial status. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of FUNCTIONAL DESCRIPTION.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize LCD power supply. Only the Reset siganl to the $\overline{RES}$ pin can initialize the supplies.

(15) Output Status Select Register

Applicable to the SED1530 and SED1532. When D is high or low, the scan direction of the COM output pin is selectable. Refer to Output Status Selector Circuit in Functional Description for details.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pin
* : Invalid bit

(16) Set Power Control

Selects one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.
When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

(17) Set Electronic Control

Adjusts the contrast of LCD panel display by changing V5 LCD drive voltage that is output by voltage regulator of on-board power supply.
This command selects one of 32 V_5 LCD drive voltages by storing data in 5-bit register. The V_5 voltage adjusting range should be determined depending on the external resistance. Refer to the Voltage Regulator section of FUNCTIONAL DESCRIPTION for details.

A0	RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	A4	A3	A2	A1	A0

D4	D3	D2	D1	D0	| V5 |
0	0	0	0	0	Low
0	0	0	0	1	
0	0	0	1	0	
		:			↓
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	High

Set register to (D4,D3,D2,D1,D0)=(0,0,0,0,0) to suppress electronic control function.

(18) Static Indicator

This command turns on or off static drive indicators. The indicator display is controlled by this command only, and it is not affected by the other display control commands.
Either FR or FRS terminal is connected to either of static indicator LCD drive electrodes, and the remaining terminal is connected to another electrode. When the indicator is turned on, the static drive operates and the indicator blinks at an interval of approximately one second. The pattern separation between indicator electrodes are dynamic drive electrodes is recommended. A closer pattern may cause an LCD and electrode deterioration.

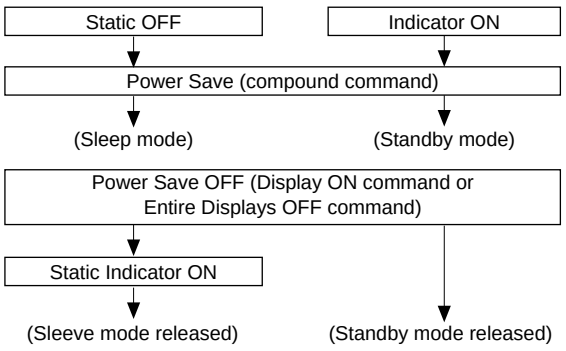
A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D 0: Static indicator OFF
1: Static indicator ON

(19) Power Save (Compound Command)

When all displays are turned on during indicator off, the Power Save command is issued to greatly reduce the current consumption.
If the static indicators are off, the Power Save command sleeps the system. If on, this command stands by the system.

Release the Sleep mode using the both Power Save OFF command (Indicator ON command or All Indicator Displays OFF command) and Static Indictor ON command.
Release the Standby mode using the Power Save OFF command (Indicator ON command or All Indicator Displays OFF command).



Sleep mode
This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access to the built-in display RAM.

Standby mode
Stops the operation of the duty LCD display system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive.
The ON operation of the static drive system indicates that the SED1530 series is in the standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.
(2) Stops the LCD drive and outputs the VDD level as the segment/common driver output. However, the static drive system operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access to the built-in display RAM.
When the RESET command is issued in the standby mode, the sleep mode is set.

When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VDD level, prior to or concurrently with causing the 1530 series to go to the sleep mode or standby mode.

When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VDD level, prior to or concurrently with causing the SED1530 series to go to the sleep mode or standby mode.

When the common driver SED1635 or SED1651 is combined with the SED1531 in the configuration, the $\overline{DOF}$ pin of the SED1531 must be connected to the $\overline{DOFF}$ pin of the SED1635 or SED1651.

(20) Test Command
This is the dedicate IC chip test command. It must not be used for normal operation. If the Test command is issued erroneously, set the -$\overline{RES}$ input to low or issue the Reset command to release the test mode.

A0	E ($\overline{RD}$)	R/$\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* : Invalid bit

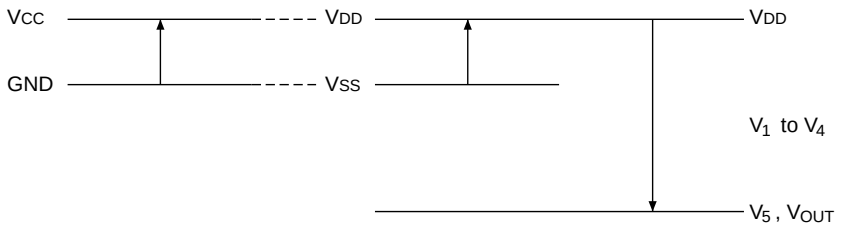
Cautions: The SED1530 Series holds an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. It must be considered to suppress the noise on the its package and system or to prevent an ambient noise insertion. To prevent a spike noise, a built-in software for periodical status refreshment is recommended to use.
The test command can be inserted in an unexpected place. Therefore, it is recommended to enter the test mode reset command F0h during the refresh sequence.

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns on LCD panel when goes high, and turns off when goes low.
(2) Initial Display Line	0	1	0	0	1	Start display address						Specifies RAM display line for COM0.
(3) Set Page Address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register.
(4) Set Column Address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4) Set Column Address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read Status	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Write Display Data	1	1	0	Write data								Writes data in display RAM.
(7) Read Display Data	1	0	1	Read data								Reads data from display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Sets normal relationship between RAM column address and segment driver when low, but reverses the relationship when high.
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	Normal indication when low, but full indication when high.
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1).
(11) Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	Sets LCD drive voltage bias ratio.
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write when high and during each read when low.
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions.
(15) Set Output Status Register	0	1	0	1	1	0	0	0 1	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set Power Control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode.
(17) Set Electronic Control Register	0	1	0	1	0	0	Electronic control value					Sets V5 output voltage to Electronic Control register.
(18) Set Standby	0	1	0	1	0	1	0	1	1	0	0 1	Selects standby status. 0: OFF 1: ON
(19) Power Save	–	–	–	–	–	–	–	–	–	–	–	Compound command of display OFF and entire display ON
(20) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(21) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

Note: Do not use any other command, or the system malfunction may result.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Supply voltage range		V_{DD}	–0.3 to +7.0	V
	Triple boosting		–0.3 to +6.0	
	Quadruple boosting		–0.3 to +4.5	
Supply voltage range (1) (V_{DD} Level)		V_5, V_{OUT}	–18.0 to +0.3	V
Supply voltage range (2) (V_{DD} Level)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage range		V_{IN}	–0.3 to V_{DD}+0.3	V
Output voltage range		V_O	–0.3 to V_{DD}+0.3	V
Operating temperature range		T_{OPR}	–40 to +85	°C
Storage temperature range	TCP	T_{STR}	–55 to +100	°C
	Bear chip		–55 to +125	



Notes: 1. V_1 to V_5, V_{OUT}, voltages are based on V_{DD}=0 V.
2. Voltages $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ must always be satisfied.
3. If an LSI exceeds its absolute maximum rating, it may be damaged permanently. It is desirable to use it under electrical characteristics conditions during general operation. Otherwise, an LSI malfunction or reduced LSI reliability may result.

ELECTRICAL CHARACTERISTICS

DC Characteristics

V_{SS} = 0 V, V_{DD} = 5 V ±10%, Ta = –40 to +85°C unless otherwise noted.

Item		Symbol	Condition		Min.	Typ.	Max.	Unit	Pin used
Power voltage (1)	Recommended Operation	V_{DD}			4.5	5.0	5.5	V	V_{SS} *1
	Operational				2.4	–	6.0		
Operating voltage (2)	Operational	V_5	V_{DD} level (V_{DD} = 0 V)		–16.0	–	–4.5	V	V_5 *2
	Operational	V_1, V_2	V_{DD} level (V_{DD} = 0 V)		$0.4 \times V_5$	–	V_{DD}	V	V_1, V_2
	Operational	V_3, V_4	V_{DD} level (V_{DD} = 0 V)		V_5	–	$0.6 \times V_5$	V	V_3, V_4
CMOS High-level input voltage		V_{IHC}			$0.7 \times V_{DD}$	–	V_{DD}	V	*3
			V_{DD} = 2.7 V		$0.8 \times V_{DD}$	–	V_{DD}		*3
CMOS Low-level input voltage		V_{ILC}			V_{SS}	–	$0.3 \times V_{DD}$	V	*3
			V_{DD} = 2.7 V		V_{SS}	–	$0.2 \times V_{DD}$		*3
CMOS High-level output voltage		V_{OHC}	I_{OH} = –1 mA		$0.8 \times V_{DD}$	–	V_{DD}	V	*5
			V_{DD} = 2.7 V, I_{OH} = –0.5 mA		$0.8 \times V_{DD}$	–	V_{DD}		*5
CMOS Low-level output voltage		V_{OLC}	I_{OL} = 1 mA		V_{SS}	–	$0.2 \times V_{DD}$	V	*5
			V_{DD} = 2.7 V, I_{OL} = 0.5 mA		V_{SS}	–	$0.2 \times V_{DD}$		*5
Schmitt High-level input voltage		V_{IHS}			$0.85 \times V_{DD}$	–	V_{DD}		*4
			V_{DD} = 2.7 V		$0.8 \times V_{DD}$	–	V_{DD}		*4
Schmitt Low-level input voltage		V_{ILS}			V_{SS}	–	$0.15 \times V_{DD}$		*4
			V_{DD} = 2.7 V		V_{SS}	–	$0.2 \times V_{DD}$		*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	–	1.0	µA	*6
Output leakage current		I_{LO}			–3.0	–	3.0	µA	*7
LCD driver ON resistance		R_{ON}	Ta = 25°C	V_5 = –14.0 V	–	2.0	3.0	KΩ	SEG n COM n *8
			V_{DD} level	V_5 = –8.0 V	–	3.0	4.5		
Static current consumption		I_{SSQ}	V_{IN} = V_{DD} or V_{SS}		–	0.01	5.0	µA	V_{SS}
		I_{5Q}	V_5 = –18.0 V (V_{DD} level)		–	0.01	15.0	µA	V_5
Input pin capacity		C_{IN}	Ta = 25°C, f = 1 MHz		–	5.0	8.0	pF	*3 *4
Oscillation frequency		f_{OSC}	Ta = 25°C	V_{DD} = 5 V	18	22	26	kHz	*9
				V_{DD} = 2.7 V	18	22	26		

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Built-in power circuit	Input voltage	V_{DD}	Triple boosting	2.4	–	6.0	V	*10
			Quadruple boosting	2.4	–	4.5		
	Booster output voltage	V_{OUT}	Triple voltage conversion (V_{DD} level)	–18.0	–	–	V	V_{OUT}
	Voltage regulator operation voltage	V_{OUT}	(V_{DD} level)	–18.0	–	–6.0	V	V_{OUT}
	Voltage follower operation voltage	V5	(V_{DD} level)	–18.0	–	–6.0	V	*11
				–16.0	–	–4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C (V_{DD} level)	–2.75	–2.55	–2.35	V	

For the mark *, refer to P. 1–25

Dynamic current consumption (1) when the built-in power supply is OFF

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SED1530/ SED1535	I_{DD} (1)	V_{DD} = 5.0V, V_5 – V_{DD} = –8.0 V	—	24	40	µA	*12
		V_{DD} = 3.0V, V_5 – V_{DD} = –8.0 V	—	22	35		
SED1531		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V	—	40	65		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V	—	36	60		
SED1532		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V	—	39	65		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V	—	32	55		
SED1533		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V	—	20	35		
SED1534		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V	—	20	35		

Dynamic current consumption (2) when the built-in power supply is ON

Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SED1530/ SED1535	I_{DD} (1)	V_{DD} = 5.0V, V_5 – V_{DD} = –8.0 V, dual boosting	—	41	70	µA	*13
		V_{DD} = 3.0V, V_5 – V_{DD} = –8.0 V, triple boosting	—	48	80		
SED1531		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V, triple boosting	—	96	160		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V, quadruple boosting	—	118	190		
SED1532		V_{DD} = 5.0V, V_5 – V_{DD} = –11.0 V, triple boosting	—	95	160		
		V_{DD} = 3.0V, V_5 – V_{DD} = –11.0 V, quadruple boosting	—	114	190		
SED1533		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V, dual boosting	—	30	50		
SED1534		V_{DD} = 3.0V, V_5 – V_{DD} = –5.0 V, dual boosting	—	32	55		

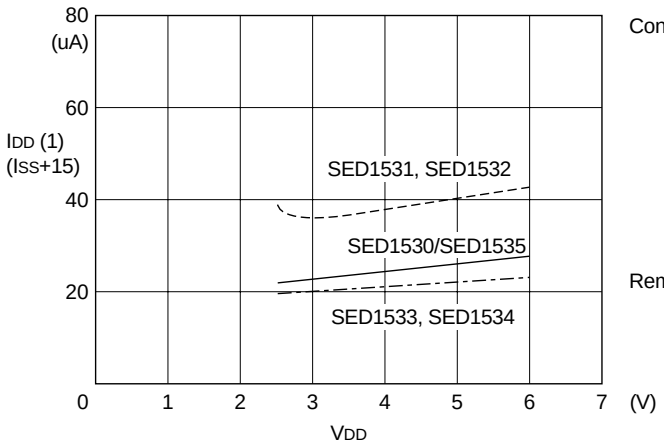
Current consumption during Power Save mode

V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V Ta=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
During sleep	I_{DDS1}	SED1530, SED1531, SED1532	—	0.01	1	µA	
During standby	I_{DDS2}	SED1530, SED1531, SED1532	—	10	20		

Typical current consumption characteristics (reference data)

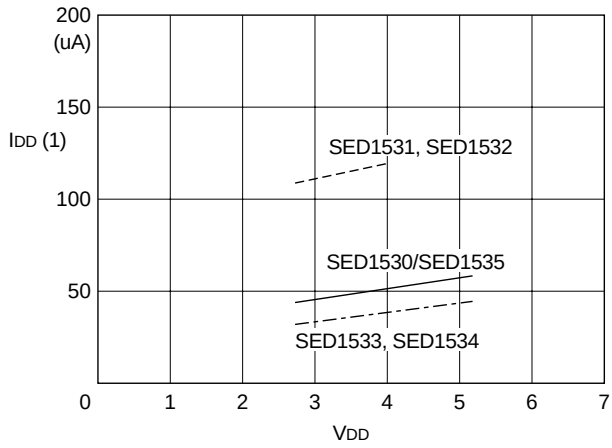
- Dynamic current consumption (1) when LCD external power mode lamp is ON



Condition: The built-in power supply is OFF and an external power supply is used.
SED1530/SED1535 V_5-V_{DD}=–8.0V
SED1531 V_5-V_{DD}=–11.0V
SED1532 V_5-V_{DD}=–11.0V
SED1533 V_5-V_{DD}=–6.0V
SED1534 V_5-V_{DD}=–6.0V
Ta=25°C

Remarks: ✻12

- Dynamic current consumption (2) when the LCD built-in power circuit lamp is ON



Condition: The built-in power circuit is ON.
SED1530/SED1535: V_5-V_{DD}=–8.0 V, triple boosting
SED1531: V_5-V_{DD}=–11.0 V, quadruple boosting
SED1532: V_5-V_{DD}=–11.0 V, quadruple boosting
SED1533: V_5-V_{DD}=–5.0 V, dual boosting
SED1534: V_5-V_{DD}=–5.0 V, dual boosting
Ta=25°C

Remarks: ✻13

*1 Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the microprocessor.
*2 V_{DD} and V_5 operating voltage range. (Refer to Fig. 10.)
The operating voltage range applies if an external power supply is used.
*3 A0, D0 - D5, D6, D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, M/S, C86, P/S and $\overline{DOF}$ pins
*4 CL, SCL (D6) and $\overline{RES}$ pins
*5 D0 - D5, D6, D7 (SI), FR, FRS, DYO, $\overline{DOF}$ and CL pins
*6 A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, $\overline{RES}$, C86 and P/S pins
*7 Applies when the D0 - D7, FR, CL, DYO and $\overline{DOF}$ pins are in high impedance,
*8 Resistance value when 0.1 V is applied between the output pin SEGn or COMn and each power supply pin (V1, V2, V3, V4). This is specified in the operating voltage (2) range.
R ON = 0.1 V/ΔI (ΔI: Current flowing when 0.1 V is applied in the ON status.)
*9 For the relationship between oscillation frequency and frame frequency, refer to Fig. 9.
*10 For triple or quadruple boosting using the on-chip power useing the primary-side power supply V_{DD} must be used within the input voltage range.
*11 The voltage regulator adjusts V_5 within the voltage follower operating voltage range.
*12, *13 Current that each IC unit consumes. It does not include the current of the LCD panel capacity, wiring capacity, etc. This is current consumption under the conditions of display data = checker, display ON, SED1530 = 1/33 duty (1/6 Bias), and SED1531 and SED1532 = 1/65 duty. (1/8 Bias)
*12 Applies to the case where the on-chip oscillator circuit is used and no access is made from the microprocessor.
*13 Applies to the case where the on-chip oscillator circuit and the on-chip power circuit are used and no access is made from the microprocessor.
The current flowing through voltage regulation resistors (R1, R2 and R3) is not included.
The current consumption, when the on-chip voltage booster is used, is for the power supply V_{DD}.

- Relationship between oscillation frequency and frame frequency

The relationship between oscillation frequency f_{OSC} and LCD frame frequency, f_F can be obtained by the following expression.

	Duty	f_{CL}	f_F
SED1530	1/33	$f_{OSC}/8$	$f_{OSC}/(8*33)$
SED1531 SED1532	1/65	$f_{OSC}/4$	$f_{OSC}/(4*65)$
SED1533	1/17	$f_{OSC}/8$	$f_{OSC}/(8*17)$
SED1534	1/9	$f_{OSC}/8$	$f_{OSC}/(8*9)$
SED1535	1/35	$f_{OSC}/8$	$f_{OSC}/(8*35)$

(f_F does not indicate the FR signal cycle but the AC cycle.)

Fig. 9

Relationship between clock (f_{CL}) and frame frequency f_F

- V_{SS} and V_5 operating voltage range

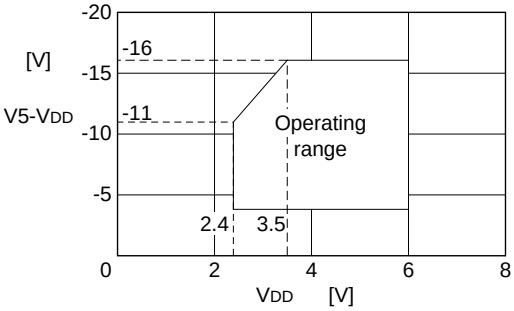
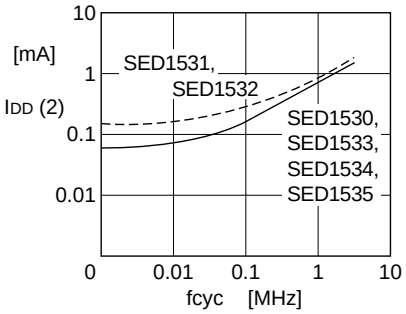


Fig 10

- Current consumption at access IDD (2) - Microprocessor access cycle



This indicates current consumption when data is always written on the checker pattern at fcyc. When no access is made, only IDD (1) occurs.

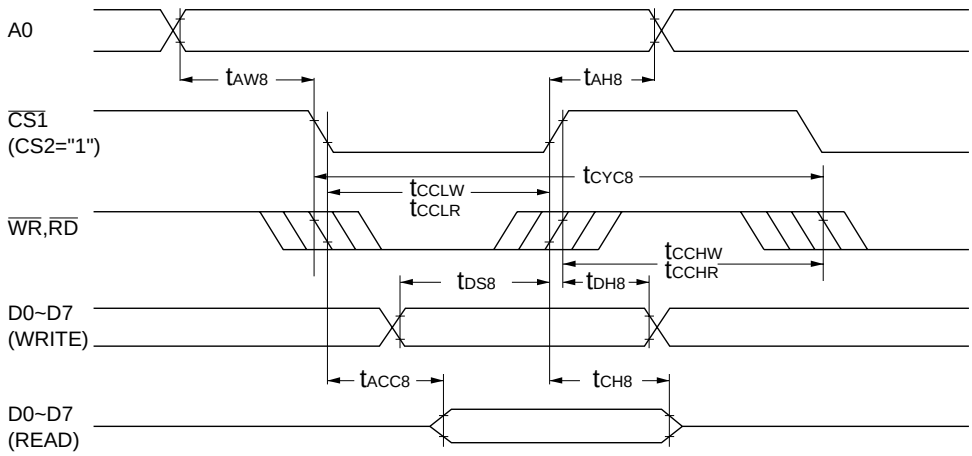
Condition: SED1530/SED1535 V_5-V_{DD}=-8.0V, triple boosting
SED1531 V_5-V_{DD}=-11.0V, quadruple boosting
SED1532 V_5-V_{DD}=-11.0V, quadruple boosting
SED1533 V_5-V_{DD}=-6.0V, dual boosting
SED1534 V_5-V_{DD}=-6.0V, dual boosting
Ta = 25°C

Fig. 11

AC Characteristics

(1) System buses

Read/write characteristics I (8080-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		10	–	ns
Address setup time		t_{AW8}		10	–	ns
System cycle time		t_{CYC8}		166	–	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		30	–	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		70	–	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		100	–	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		70	–	ns
Data setup time		t_{DS8}		20	–	ns
Data hold time		t_{DH8}		10	–	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L=100pF	–	70	ns
Output disable time		t_{CH8}		10	50	ns

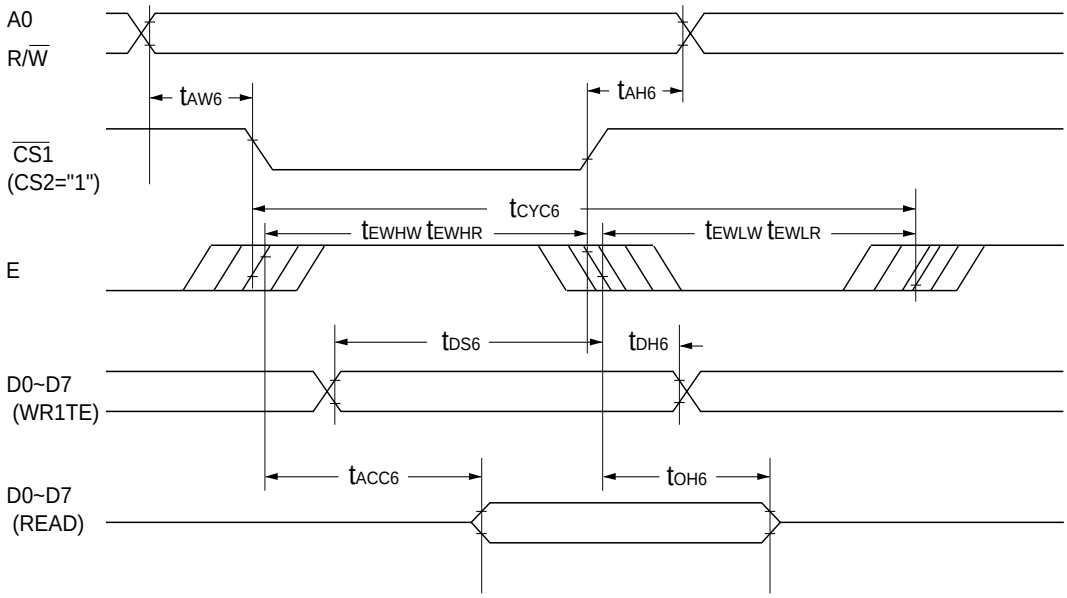
V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Address hold time	A0	t_{AH8}		19	–	ns
Address setup time		t_{AW8}		15	–	ns
System cycle time		t_{CYC8}		450	–	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		60	–	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		140	–	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		200	–	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		140	–	ns
Data setup time		t_{DS8}		40	–	ns
Data hold time		t_{DH8}		15	–	ns
$\overline{RD}$ access time	D0 to D7	t_{ACC8}	C_L=100pF	–	140	ns
Output disable time		t_{CH8}		10	100	ns

Notes: 1. The input signal rise/fall time (t_r, t_f) is specified at 15 ns or less.
When system cycle time is used at a high speed, it is specified by $t_r + t_f \leq (t_{CYC8} - t_{CCLW})$ or $t_r + t_f \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which $\overline{CS1}$ is "0" (CS2 = "1") and $\overline{WR}$ and $\overline{RD}$ are "0".

(2) System buses

Read/write characteristics II (6800-series microprocessor)



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

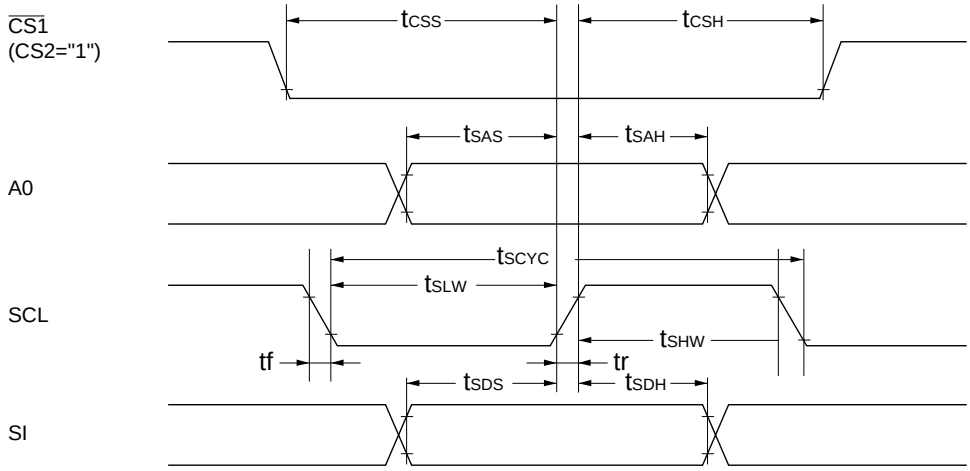
Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		166	–	ns
Address setup time Address hold time		A0 W/$\overline{R}$	t_{AW6} t_{AH6}		10 10	– –	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		20 10	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	C_L=100pF	10 –	50 70	ns ns
Enable low pulse width	READ WRITE	E	t_{EWHR} t_{EWHW}		70 30	– –	ns ns
Enable high pulse width	READ WRITE	E	t_{EWLR} t_{EWLW}		70 100	– –	ns ns

V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter		Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time			t_{CYC6}		450	–	ns
Address setup time Address hold time		A0 R/$\overline{W}$	t_{AW6} t_{AH6}		15 19	– –	ns ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	– –	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	C_L=100pF	10 –	100 140	ns ns
Enable low pulse width	READ WRITE	E	t_{EWHR} t_{EWHW}		140 60	– –	ns ns
Enable high pulse width	READ WRITE	E	t_{EWLR} t_{EWLW}		140 200	– –	ns ns

Notes: 1. The input rise/fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is used at a high speed, it is specified by $t_r + t_f \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $tr + tf \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.
3. t_{EWHR} and t_{EWHW} are specified by the overlap period in which CS1 is "0" (CS2 = "1") and E is "1".

(3) Serial interface



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

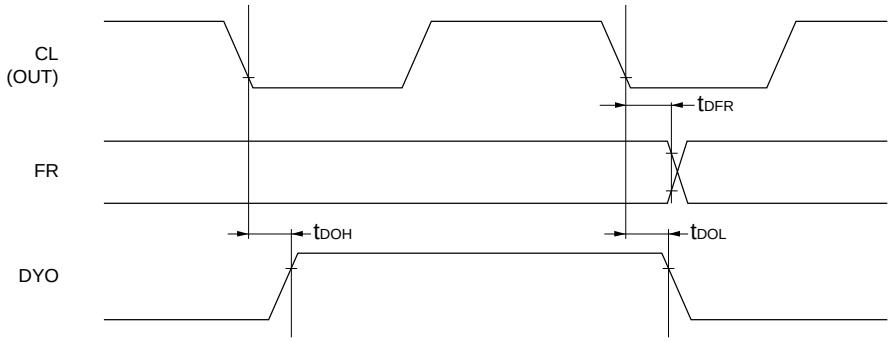
Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		250	–	ns
Serial clock H pulse width		t_{SHW}		100	–	ns
Serial clock L pulse width		t_{SLW}		75	–	ns
Address setup time	A0	t_{SAS}		50	–	ns
Address hold time		t_{SAH}		200	–	ns
Data setup time	SI	t_{SDS}		50	–	ns
Data hold time		t_{SDH}		50	–	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		30	–	ns
		t_{CSH}		100	–	

V_{DD} = 2.7 to 4.5V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle	SCL	t_{SCYC}		500	–	ns
Serial clock H pulse width		t_{SHW}		200	–	ns
Serial clock L pulse width		t_{SLW}		150	–	ns
Address setup time	A0	t_{SAS}		100	–	ns
Address hold time		t_{SAH}		400	–	ns
Data setup time	SI	t_{SDS}		100	–	ns
Data hold time		t_{SDH}		100	–	ns
$\overline{CS}$ serial clock time	CS	t_{CSS}		60	–	ns
		t_{CSH}		200	–	

Notes: 1. The input signal rise and fall times must be within 15 nanoseconds.
2. All signal timings are limited based on 20% and 80% of V_{DD} voltage.

(4) Display control timing



Output timing V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

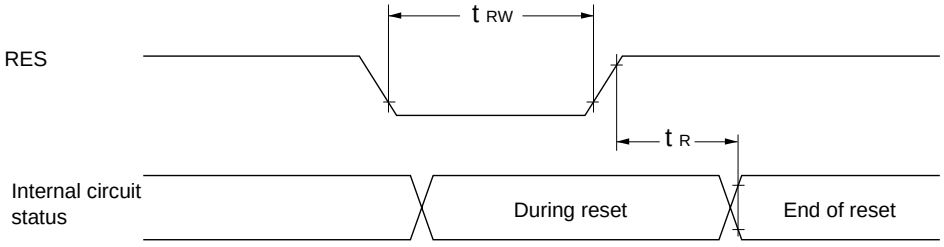
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	C_L = 50 pF	–	10	40	ns
DYO "H" delay time	DYO	t_{DOH}		–	40	100	ns
DYO "L" delay time		t_{DOL}		–	40	100	ns

Output timing V_{SS} = 0 V, V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
FR delay time	FR	t_{DFR}	C_L = 50 pF	–	15	80	ns
DYO "H" delay time	DYO	t_{DOH}		–	70	200	ns
DYO "L" delay time		t_{DOL}		–	70	200	ns

Notes: 1. The otput timing is valid in master mode.
2. Every timing is specified on the basis of 20% and 80% of V_{DD}.

(5) Reset timing



V_{DD} = 5.0 V ±10%, Ta = –40 to +85°C

Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		0.5	–	–	µs
Reset low pulse width	$\overline{RES}$	t_{RW}		0.5	–	–	µs

V_{DD} = 2.7 V to 4.5 V, Ta = –40 to +85°C

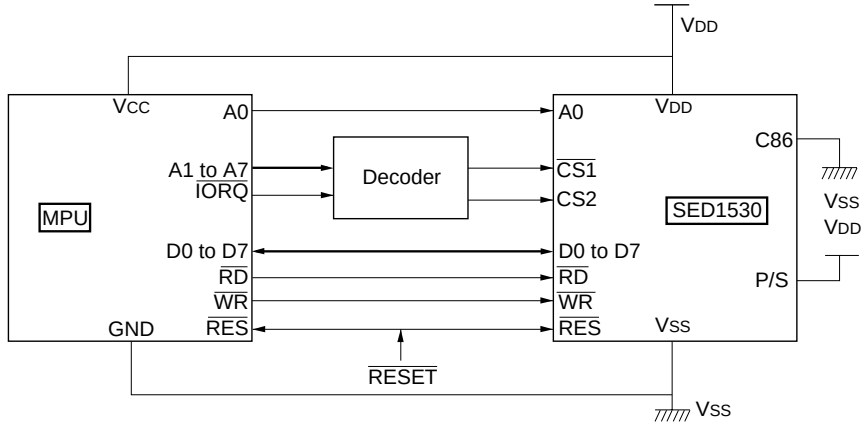
Parameter	Signal	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time		t_R		1.0	–	–	µs
Reset low pulse width	$\overline{RES}$	t_{RW}		1.0	–	–	µs

Note: The reset timing is specified on the basis of 20% and 80% of V_{DD}.

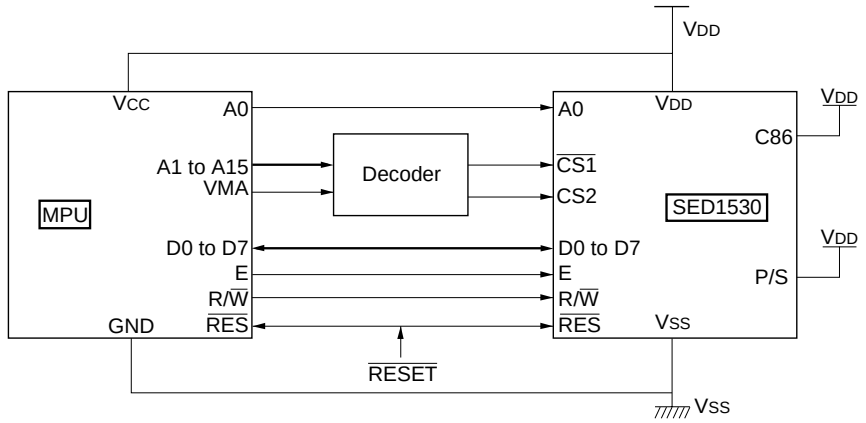
MICROPROCESSOR INTERFACE (Reference example)

The SED1530 series chips can directly connect to 8080 and 6800-series microprocessors. Also, serial interfacing requires less signal lines between them. When multiple chips are used in the SED1530 series they can be connected to the microprocessor and one of them can be selected by Chip Select.

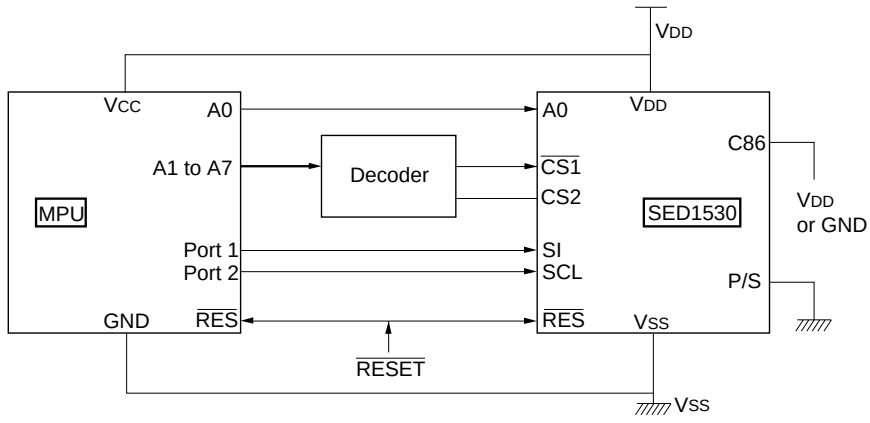
8080-series microprocessors



6800-series microprocessors



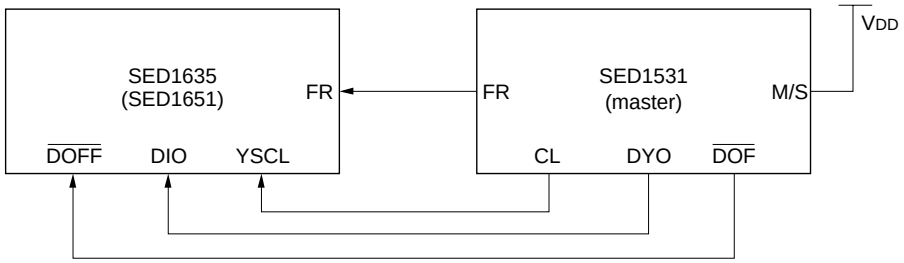
Serial interface



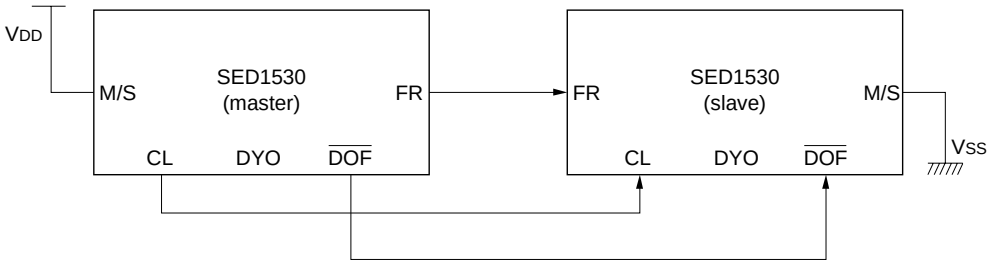
CONNECTION BETWEEN LCD Drivers

The LCD panel display area can easily be expanded by use of multiple SED1530 series chips. The SED1530 series can also be connected to the common driver (SED1635).

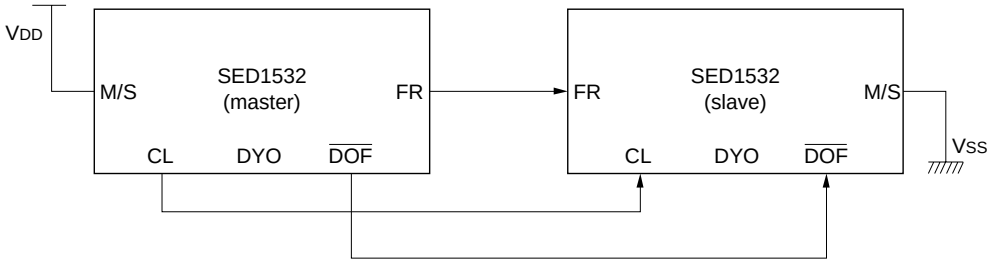
SED1531 to SED1635 (SED1651)

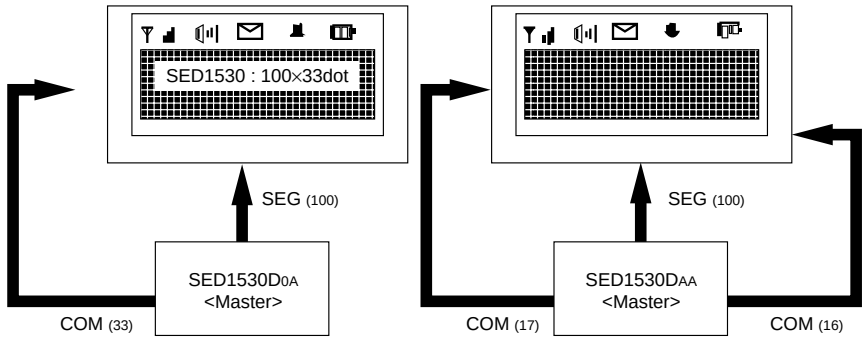


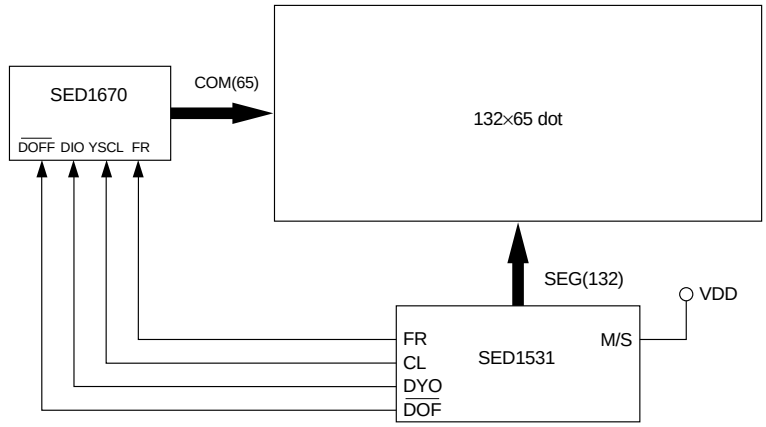
SED1530 to SED1531

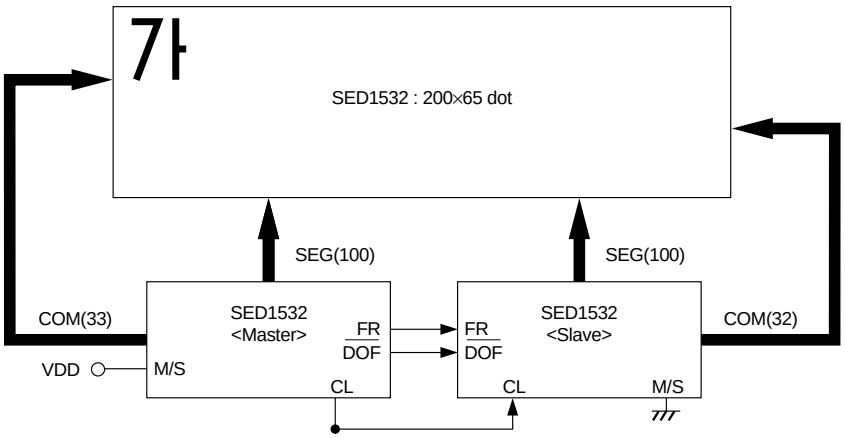


SED1532 to SED1532




SED1530 : 100×33dot
SEG (100)
SED1530D0A
<Master>
COM (33)
SEG (100)
SED1530DAA
<Master>
COM (17)
COM (16)


SED1670
DOFF DIO YSCL FR
COM(65)
132×65 dot
SEG(132)
VDD
FR
CL
DYO
DOF
SED1531
M/S


SED1532 : 200×65 dot
SEG(100)
SEG(100)
COM(33)
VDD
M/S
SED1532
<Master>
FR
DOF
CL
FR
DOF
SED1532
<Slave>
CL
M/S
COM(32)

Dimensional outline drawing of the flexible substrate

(an example) The dimensions are subject to change without prior notice.