DATA SHEET

(DOC No. HX8369-A02-DS)

HX8369-A02

480RGB x 864 dot, 16.7M color,
with internal GRAM,
TFT Mobile Single Chip Driver

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Himax Technologies, Inc.
http://www.himax.com.tw

List of Contents

1. General Description 11

2. Features 12

2.1 Display 12
2.2 Display module 12
2.3 Display / Control interface 13
2.4 Input power 13
2.5 Miscellaneous 13

3. Device Overview 14

3.1 Block diagram 14
3.2 Pin description 15
3.3 Pin assignment 19
3.4 PAD coordinates 20
3.4.1 Bump arrangement 28

4. Interface 30

4.1 System interface 30
4.1.1 MIPI DBI-A / DBI-B interface 32
4.2 Serial data transfer interface (MIPI DBI-C) 43
4.2.2 MIPI DPI interface (Display Pixel Interface) 47
4.2.3 DSI system interface 53
4.2.4 MDDI Interface (Mobile Display Digital Interface) 67
4.2.5 Terminology 68
4.2.6 Order of data transmission 69
4.2.7 Data-STB encoding 69

5. Function Description 82

5.1 Display data GRAM 82
5.2 Address counter (AC) 82
5.3 Source, gate and memory map 83
5.3.1 480RGB x 864 resolution 83
5.3.2 480RGB x 854 resolution 84
5.3.3 480RGB x 800 resolution 85
5.3.4 480RGB x 640 resolution 86
5.3.5 360RGB x 640 resolution 87
5.3.6 480RGB x 720 resolution 88
5.4 MCU to memory write / read direction 89
5.5 Fully display, partial display, vertical scrolling display 91
5.5.1 Fully display 91
5.5.2 Vertical scrolling display 97
5.5.3 Tearing effect output line 100
5.6 Color depth conversion 104
5.6.1 Color depth conversion Look-up tables 104
5.7 Oscillator 110
5.8 Source driver 111
5.9 LCD power generation scheme 112
5.10 DC/DC converter circuit 113
5.10.1 Use PFM DC/DC converter 113
5.10.2 Use HX5186-A 114
5.11 Idle display 115
5.12 Gamma characteristic correction function 116
5.13 Characteristics of I/O 158
5.13.1 Output or bi-directional (I/O) pins 158

List of Contents

5.13.2 Input pins 158
5.14 GIP control singal 159
5.15 Sleep Out –command and self-diagnostic functions of the display module 160
5.15.1 Register loading detection 160
5.15.2 Functionality detection 161
5.16 Power on/off sequence 162
5.16.1 Case 1: RESX line is held high or unstable by host at power on 163
5.16.2 Case 2: RESX line is held low by host at power on 164
5.17 Uncontrolled power off 164
5.18 Content adaptive brightness control (CABC) function 165
5.18.1 Module architectures 166
5.18.2 CABC block 167
5.18.3 Brightness control block 168
5.18.4 Minimum brightness setting of CABC function 169
5.19 OTP programing 170
5.19.1 OTP table 170
5.19.2 OTP programming flow 173
5.19.3 Programming sequence 174
5.19.4 OTP Programming example of VCOM setting VCMC_F and VCMC_B 175
5.19.5 OTP Programming example of ID1, ID2 and ID3 176
5.19.6 OTP read example of 0x1Bh (VCOM setting re-load) 177
5.19.7 OTP read example of VCMC_F1 178

6. Command 179

6.1 Command list 179
6.1.1 Standard command 179
6.1.2 User define command list table 183
6.2 Command description 187
6.2.1 NOP (00h) 187
6.2.2 Software reset (01h) 188
6.2.3 RDNUMPE: Read number of the parity errors (05h) 189
6.2.4 Get_red_channel (06h) 190
6.2.5 Get_green_channel (07h) 191
6.2.6 Get_blue_channel (08h) 192
6.2.7 Get_power_mode (0Ah) 193
6.2.8 Read display MADCTL (0Bh) 194
6.2.9 Get_pixel_format (0Ch) 196
6.2.10 Get_display_mode (0Dh) 198
6.2.11 Get_signal_mode (0Eh) 199
6.2.12 Get_diagnostic_result (0Fh) 200
6.2.13 Enter_sleep_mode (10h) 201
6.2.14 Exit_sleep_omde (11h) 202
6.2.15 Enter_partial_mode (12h) 203
6.2.16 Enter_normal_mode (13h) 204
6.2.17 Exit_inversion_mode (20h) 205
6.2.18 Enter_inversion_mode (21h) 206
6.2.19 Set_gamma_curve (26h) 207
6.2.20 Set_display_off (28h) 208
6.2.21 Set_display_on (29h) 209
6.2.22 Set_clumn_address (2Ah) 210
6.2.23 Set_page_address (2Bh) 211
6.2.24 Write_memory_start (2Ch) 212
6.2.25 Colour Set (2Dh) 213
6.2.26 Raed_memory_start (2Eh) 216
6.2.27 Set_partial_area (30h) 217

6.2.28 Set_scroll_area (33h) 219
6.2.29 Tearing effect line off (34h) 222
6.2.30 Set_tear_on (35h) 223
6.2.31 Set_address_mode (36h) 224
6.2.32 Set_scroll_start (37h) 226
6.2.33 Idle mode off (38h) 227
6.2.34 Enter_Idle_mode (39h) 228
6.2.35 Set_pixel_format (3Ah) 229
6.2.36 Write_memory_contiune (3Ch) 230
6.2.37 Raed_memory_continue (3Eh) 231
6.2.38 Set tear scan lines (44h) 232
6.2.39 Get the current scanline(45h) 233
6.2.40 Write display brightness (51h) 234
6.2.41 Read display brightness value (52h) 235
6.2.42 Write CTRL display (53h) 236
6.2.43 Read CTRL value display (54h) 237
6.2.44 Write content adaptive brightness control (55h) 238
6.2.45 Read content adaptive brightness control (56h) 239
6.2.46 Write CABC minimum brightness (5Eh) 240
6.2.47 Read CABC minimum brightness (5Fh) 241
6.2.48 Read automatic brightness control self-diagnostic result (68h) 242
6.2.49 Read_DDB_start (A1h) 243
6.2.50 Read_DDB_continue (A8h) 245
6.2.51 Read ID1 (DAh) 246
6.2.52 Read ID2 (DBh) 247
6.2.53 Read ID3 (DCh) 248
6.2.54 SETOSC: Set internal oscillator (B0h) 249
6.2.55 SETPOWER: Set power (B1h) 250
6.2.56 SETDISP: Set display related register (B2h) 259
6.2.57 SETRGBIF: Set RGB interface related register (B3h) 262
6.2.58 SETCYC: Set display waveform cycle (B4h) 263
6.2.59 SETVCOM: Set VCOM voltage (B6h) 266
6.2.60 SETEXTC: Set extension command (B9h) 269
6.2.61 SETMIPI: (BAh) 270
6.2.62 SETOTP: Set OTP (BBh) 272
6.2.63 SETDGCLUT: Set DGC LUT (C1h) 273
6.2.64 SETID: Set ID (C3h) 275
6.2.65 SETCABC: Set CABC Control (C9h) 276
6.2.66 SETPANEL (CCh) 278
6.2.67 SETGIP (D5h) 279
6.2.68 SETGAMMA: Set gamma curve related setting (E0h) 286
6.2.69 SETOTPKEY (E9h) 288
6.2.70 GETHXID (F4h) 289
6.2.71 SETCNCD/GETCNCD (FDh) 290
6.2.72 SET SPI READ INDEX (FEh) 291
6.2.73 GETSPIREAD: Read command data (FFh) 292

7. Power Supply 293

7.1 Power supply setup 293
7.1.1 Architecture 1 with PFM circuit 293
7.1.2 Architecture 2 with HX5186-A 294
7.2 Voltage configuration 295

8. Electrical Characteristics 296

8.1 Absolute maximum ratings 296

List of Contents

8.2 ESD protection level 296
8.3 DC characteristics 297
8.4 AC characteristics 298
8.4.1 DBI Type A interface characteristics 298
8.4.2 DBI Type B interface characteristics 299
8.4.3 DBI Type C interface characteristics 300
8.4.4 DPI interface characteristics 301
8.4.5 Reset input timing 304
8.4.6 MDDI electrical characteristics 305
8.4.7 DPI Interface Power On/Off Timing 308
8.4.8 DSI D-PHY electrical characteristics 310
9. Layout Recommendation 318
10. Maximum Layout Resistance 319
11. Ordering Information 320
12. Revision History 320

List of Figures

Figure 4.1: DBI-A system interface protocol, write to register or GRAM 32
Figure 4.2: DBI-A system interface protocol, read from register or GRAM.....32
Figure 4.3: DBI-B system interface protocol, write to register or GRAM 33
Figure 4.4: DBI-B system interface protocol, read from register or GRAM.....33
Figure 4.5 Example of DBI-B system 18-bit parallel bus interface.....34
Figure 4.6: Write data for RGB 8-8-8 (16.7M colours) bit Input in 24-bit parallel interface.....34
Figure 4.7: Example of DBI-A- / DBI-B system 18-bit parallel bus interface.....35
Figure 4.8: Write data for RGB 5-6-5 (65k colours) bit input in 18-bit parallel interface 35
Figure 4.9: Write data for RGB 6-6-6(262k colours) bit input in 18-bit parallel interface 35
Figure 4.10: Write data for RGB 8-8-8 (16.7M colours) bit input in 18-bit parallel interface.....36
Figure 4.11: Example of DBI-A- / DBI-B system 16-bit bus interface.....37
Figure 4.12: Write data for RGB 5-6-5 (65k colours) bit input in 16-bit parallel interface 37
Figure 4.13: Write data for RGB 6-6-6 (262k colours) bit input in 16-bit parallel interface 38
Figure 4.14: Write data for RGB 8-8-8-bit (16.7M colours) input in 16-bit parallel interface.....38
Figure 4.15: Example of DBI-A- / DBI-B- system 9-bit bus interface 39
Figure 4.16: Write data for RGB 5-6-5(65k colours) bit input in 9-bit parallel interface 39
Figure 4.17: Write data for RGB 6-6-6-bit (262k colours) input in 9-bit parallel interface.....40
Figure 4.18: Write data for RGB 8-8-8-bit (16.7 M colours) input in 9-bit parallel interface.....40
Figure 4.19: Example of DBI-A- / DBI-B-system 8-bit bus interface 41
Figure 4.20: Write data for RGB 5-6-5 (65k colours) bit input in 8-bit parallel interface 41
Figure 4.21: Write data for RGB 6-6-6-bit (262k colours) input in 8-bit parallel interface.....42
Figure 4.22: Write data for RGB 8-8-8-bit (16.7 M colours) input in 8-bit parallel interface.....42
Figure 4.23: Serial data stream, write mode 43
Figure 4.24: DBI Type C: Serial interface protocol 3-wire/4-wire, write mode 44
Figure 4.25: Type C:Serial interface protocol 3-wire/4-wire read mode.....45
Figure 4.26: Display module data transfer recovery 46
Figure 4.27: PCLK cycle.....47
Figure 4.28: General timing diagram.....48
Figure 4.29: DPI (480RGB x 864) timing diagram 48
Figure 4.30: 16-bit / pixel 65K colours order on the DPI I/F.....50
Figure 4.31: 18-bit / pixel: 262k colours order on the DPI I/F 51
Figure 4.32: 24-bit / pixel color order on the RGB I/F 52
Figure 4.33: DSI transmitter and receiver interface 53
Figure 4.34: DSI transmitter and receiver interface 54
Figure 4.35: Multiple HS transmission packets.....55
Figure 4.36: Structure of the short packet.....55
Figure 4.37: Structure of the long packet.....56
Figure 4.38: The format of data ID. 56
Figure 4.39: show Short- / Long-packet transmission command sequence 57
Figure 4.40: Physical connection of MDDI host and client.....67
Figure 4.41: MDDI terminology 68
Figure 4.42: Example of Bi-directional MDDI communication.....68
Figure 4.43: Transmission bit ordering for each type.....69
Figure 4.44: Data-STB encoding.....70
Figure 4.45: Data / STB generation & recovery circuit.....70
Figure 4.46: Differential connection between host and client 71
Figure 4.47 MDDI packet structure 72
Figure 4.48: MDDI Transceiver / Receiver state in hibernation 79
Figure 4.49: Host-initiated link wakeup sequence 80
Figure 4.50: MDDI operation mode.....81
Figure 5.1: MCU to Memory write / read direction 89
Figure 5.2: MY, MX, MV setting of 480RGB x 864 dot 89
Figure 5.3: MY, MX, MV setting of 480RGB x 864 dot 89
Figure 5.4: Address direction settings.....90
Figure 5.5: 480RGB x 864 resolution.....91

List of Figures

Figure 5.6: 480RGB x 854 resolution 92
Figure 5.7: 480RGB x 800 resolution 93
Figure 5.8: 480RGB x 640 resolution 94
Figure 5.9: 360RGB x 640 resolution 95
Figure 5.10: 480RGB x 720 resolution 96
Figure 5.11: Vertical scrolling 97
Figure 5.12: Memory map of vertical scrolling 1 97
Figure 5.13: Memory map of vertical scrolling 2 98
Figure 5.14: Vertical scroll example 1 99
Figure 5.15: Vertical scroll example 2 99
Figure 5.16: Tearing effect output line–mode 1 100
Figure 5.17: Tearing effect output line–mode 2 100
Figure 5.18: Tearing effect output line–timing diagrm 100
Figure 5.19: Tearing effect output line –tearing effect line timing 101
Figure 5.20: Tearing effect output line–definition of tf, tr 101
Figure 5.21: Tearing effect output line–example 1 (Timing) 102
Figure 5.22: Tearing effect output line–example 1 (Image) 102
Figure 5.23: Tearing effect output line–example 2 (Timing) 103
Figure 5.24: Tearing effect output line–example 2 (Image) 103
Figure 5.25: OSC aritecture 110
Figure 5.26: LCD power generation scheme 112
Figure 5.27: DC/DC converter circuit (PFM Type C)–PCCS=10 113
Figure 5.28: DC/DC converter circuit (HX5186-A) 114
Figure 5.29: Idle mode grayscale control 115
Figure 5.30: Grayscale control 116
Figure 5.31: Gamma resister stream and gamma reference voltage 118
Figure 5.32: Gamma resister stream 119
Figure 5.33: Sleep out flow chart–command and self-diagnostic functions 160
Figure 5.34: Sleep out flow chart internal function detection 161
Figure 5.35: Case 1: RESX line is held high or unstable by host at power on 163
Figure 5.36: Case 2: RESX line is held low by host at power on 164
Figure 5.37: CABC block diagram 165
Figure 5.38: Module architecture 166
Figure 5.39: CABC gain / CABC duty generation 167
Figure 5.40: CABC_PWM_OUT output duty 168
Figure 5.41: OTP programming sequence 173
Figure 5.42: OTP programming sequence example 1. 175
Figure 5.43: OTP programming sequence example 2. 176
Figure 5.44: OTP programming sequence index 0x1Bh read flow. 177
Figure 5.45: OTP programming sequence read flow. 178
Figure 7.1: Power supply with PFM circuit 293
Figure 7.2: Power supply with HX5186-A 294
Figure 8.1: DBI Type A interface characteristics(CLK-E mode) 298
Figure 8.2: DBI Type B interface characteristics 299
Figure 8.3: DBI Type C interface characteristics 300
Figure 8.4: DPI interface characteristics 301
Figure 8.5: Vertical Timings for RGB I/F 302
Figure 8.6: Horizontal Timing for RGB I/F 303
Figure 8.7: Reset input timing 304
Figure 8.8 Power On Timing 308
Figure 8.9 Power Off Timing 309
Figure 8.10: Electrical functions of a fully D-PHY transceiver 310
Figure 8.11: Shows both the HS and LP signal levels 310
Figure 8.12: Input Glitch Rejections of Low-Power Receivers 313
Figure 8.13: DDR Clock Definition 315

List of Figures

Figure 8.14: Data to Clock Timing Definitions.....316
Figure 9.1: Layout recommendation 318

List of Tables

Table 4.1: Interface selection 30
Table 4.2: Pin connection based on different interface 31
Table 4.3: Data types for processor-sourced packets....58
Table 4.4: Shows the error report bit definitions.....65
Table 4.5: The complete set of peripheral-to-processor data types. 66
Table 4.6: List of supported MDDI packet 73
Table 4.7: Operation mode list 81
Table 5.1: Addresses counter range....82
Table 5.2: Memory map of 480RGB x 864 resolution 83
Table 5.3: Memory map of 480RGB x 854 resolution 84
Table 5.4: Memory map of 480RGB x 800 resolution 85
Table 5.5: Memory map of 480RGB x 640 resolution 86
Table 5.6: Memory map of 360RGB x640 resolution 87
Table 5.7: Memory map of 480RGB x 720 resolution 88
Table 5.8: 480RGB x 864 resolution (SRAM assignment) 91
Table 5.9: 480RGB x 854 resolution (SRAM assignment) 92
Table 5.10: 480RGB x 800 resolution (SRAM assignment) 93
Table 5.11: 480RGB x 640 resolution (SRAM assignment) 94
Table 5.12: 360RGB x 640 resolution (SRAM assignment) 95
Table 5.13: 480RGB x 720 resolution (SRAM assignment) 96
Table 5.14: AC characteristics of tearing effect signal 101
Table 5.15: Look-up tables-1....104
Table 5.16: Look-up tables-2....105
Table 5.17: Look-up tables-3....106
Table 5.18: Look-up tables-4....107
Table 5.19: Look-up tables-5....108
Table 5.20: Look-up tables-6....109
Table 5.21: Gamma-Adjustment registers....117
Table 5.22: Offset adjustment 0~5 120
Table 5.23: Center adjustment 120
Table 5.24: VinP0 121
Table 5.25: VinP1 122
Table 5.26: VinP2 123
Table 5.27: VinP14 124
Table 5.28: VinP15 125
Table 5.29: VinP16 126
Table 5.30: VinP5 128
Table 5.31: VinP11 130
Table 5.32: VinP3 131
Table 5.33: VinP4 132
Table 5.34: VinP6 132
Table 5.35: VinP7 133
Table 5.36: VinP8 133
Table 5.37: VinP9 134
Table 5.38: VinP10 134
Table 5.39: VinP12 135
Table 5.40: VinP13 135
Table 5.41: VinN0 136
Table 5.42: VinN1 137
Table 5.43: VinN2 138
Table 5.44: VinN14 139
Table 5.45: VinN15 140
Table 5.46: VinN16 141
Table 5.47: VinN5 143
Table 5.48: VinN11 145

Table 5.49: VinN3 146
Table 5.50: VinN4 147
Table 5.51: VinN6 147
Table 5.52: VinN7 148
Table 5.53: VinN8 148
Table 5.54: VinN9 149
Table 5.55: VinN10 149
Table 5.56: VinN12 150
Table 5.57: VinN13 150
Table 5.58: Voltage calculation formula of 64-grayscale voltage (positive polarity) 152
Table 5.59: Voltage calculation formula of 64-grayscale voltage (negative polarity) 154
Table 5.60: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity) 157
Table 5.61 Characteristics of output or bi-directional (I/O) pins 158
Table 5.62 Characteristics of input pins 158
Table 5.63 CABC timing table 168
Table 5.64: OTP Programming sequence 174
Table 7.1: Adoptability of component 295
Table 8.1: Absolute maximum rating 296
Table 8.2: ESD protection level 296
Table 8.3: DC characteristic 297
Table 8.4: DBI Type A interface characteristics 298
Table 8.5: DBI Type B interface characteristics 299
Table 8.6: DBI Type C interface characteristics 300
Table 8.7: DPI interface characteristics 301
Table 8.8 Vertical Timings for RGB I/F 302
Table 8.9 Horizontal Timings for RGB I/F 303
Table 8.10: Reset timing 304
Table 8.11: LP Transmitter DC Specifications 311
Table 8.12: LP Transmitter AC Specifications 311
Table 8.13: HS Receiver DC Specifications 312
Table 8.14: HS Receiver AC Specifications 312
Table 8.15: LP Receiver DC Specifications 313
Table 8.16: LP Receiver AC Specifications 313
Table 8.17: Contention Detector DC Specifications 314
Table 8.18: HS Data Transmission Timing Parameters 315
Table 8.19: Data to Clock Timing Specifications 317
Table 10.1: Maximum layout resistance 319

1. General Description

This document describes Himax's HX8369-A02 supports WVGA resolution driving controller. The HX8369-A02 is designed to provide a single-chip solution that combines a source driver, power supply circuit to drive a TFT dot matrix LCD with 480RGBx864 dots at maximum.

The HX8369-A02 can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8369-A02 also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8369-A02 supports several interface modes, including MPU MIPI DBI Type A/Type B interface mode, MIPI DPI/DBI Type C interface mode, MIPI DSI (Display Serial Interface) interface mode and MDDI (Mobile Display Digital Interface) interface mode. The interface mode is selected by the external hardware pins BS3~0.

The HX8369-A02 is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

2.1 Display

- Single chip solution for a WVGA GIP (Gate In Panel) type TFT LCD display
- Resolution:
  - 480RGB x 864
  - 480RGB x 854
  - 480RGB x 800
  - 480RGB x 640
  - 480RGB x 720
  - 360RGB x 640
- Display color modes
  - Full color mode:
    - 16.7M colours (24-bit 8(R):8(G):8(B))
  - Reduce color mode:
    - 262k colours (18-bit 6(R):6(G):6(B))
    - 65k colours (16-bit 5(R):6(G):5(B))
    - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

2.2 Display module

- Support 1440 source channel outputs
- Internal level shifter for GIP gate control
- Supports 1-dot / 2-dot / column / Zig-Zag inversion
- Gamma correction (1 preset gamma curve)
- On module VCOM control (-2 to 0V common electrode output voltage range)
- On module DC/DC converter
  - VSP=4.7 to 5.7V
  - VSN=-5.7 to -4.7V
  - Positive source output voltage level: VSPR=3.5V to 5V
  - Negative source output voltage level: VSNR=-5V to -3.5V
  - Positive gate driver output voltage level: VGH=+9V to +20V
  - Negative gate driver output voltage level: VGL=-6V to -13.5V
  - GIP most negative reference voltage: LVGL=VGL –VDD3
  - VCOM=-2.0V to 0V, a step=16mV
- Frame memory area 480 (H) x 864 (V) x 24-bit

2.3 Display / Control interface

- Display interface types supported
  - MPU mode
    - MIPI-DBI Type B (80 System) interface (16- / 18- / 24-bit bus)
    - MIPI-DBI Type A (68 System) interface (16- / 18- bit bus)
    - MIPI-DBI Type C (Serial data transfer interface) interface
  - MIPI-DSI (Display Serial Interface) interface
    - Support DSI Version 1.01
    - Support D-PHY version 0.90
  - MDDI (Mobile Display Digital Interface) interface
    - Support VESA Mobile Display Digital Interface Standard Version 1.2
  - RGB mode
    - 16 bit/pixel R(5), G(6), B(5)
    - 18 bit/pixel R(6), G(6), B(6)
    - 24 bit/pixel R(8), G(8), B(8)

2.4 Input power

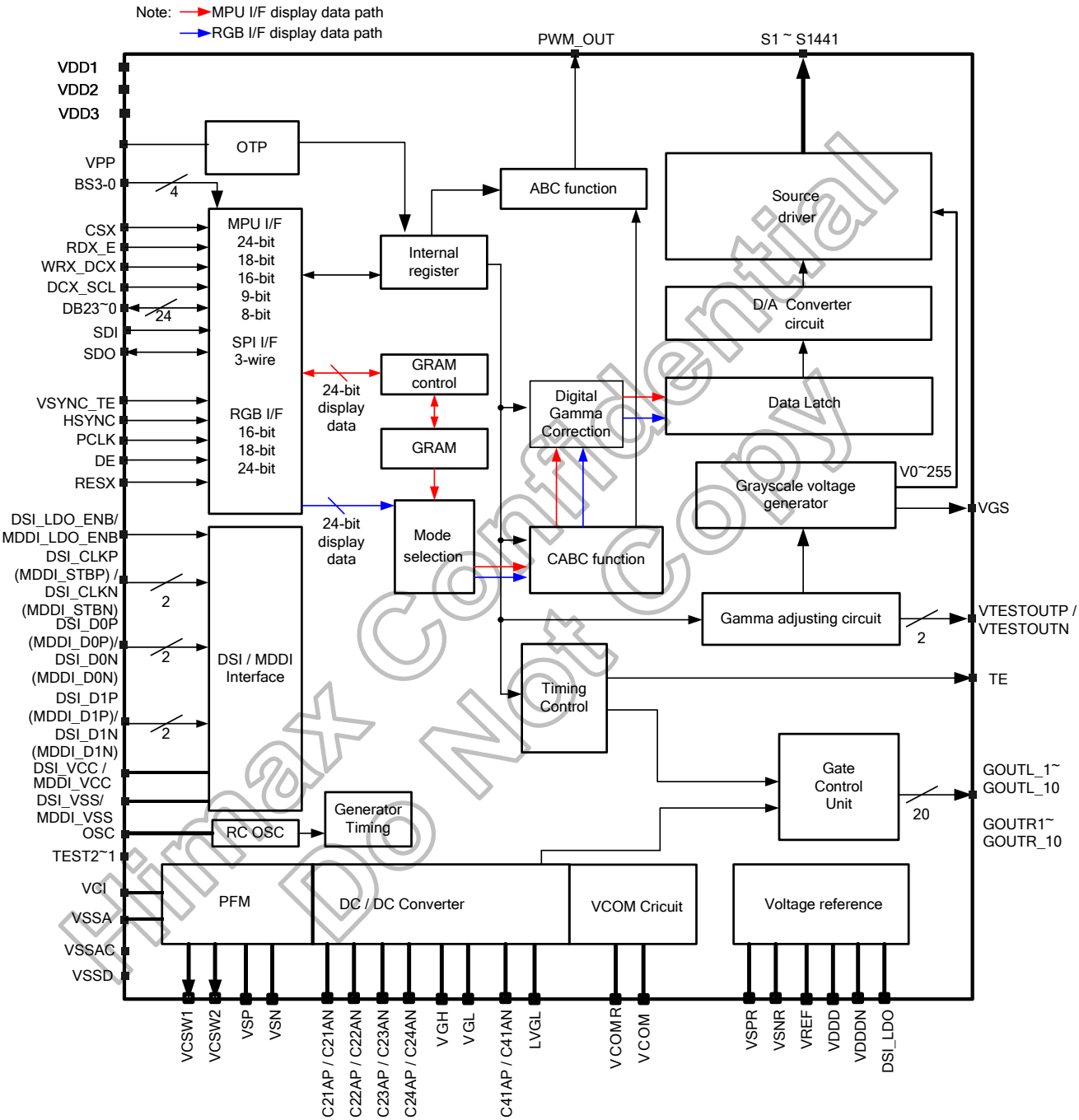
- I/O and interface power supply (VDD1): 1.65V to 3.3V
- Analog power supply (VDD2): 2.3V to 4.8V
- Logic power supply (VDD3): 2.3V to 4.8V
- DSI power supply (DSI_VCC): 1.65V to 3.3V
- MDDI power supply (DSI_VCC): 2.3V to 3.3V
- OTP programming voltage (VPP): 7.5V ± 0.2V

2.5 Miscellaneous

- Partial display mode
- Software programmable color depth mode
- Oscillator for display clock generation
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Optimized layout for COG assembly
- Temperature range: -40 to +85 ℃
- HBM ESD (Human Body Mode)>2KV, MM(Machine Mode)>±200V and Latch up>±200mA
- Support inversion mode
- DC/DC converter for source
- Support DC COM driving
- VCOM voltage generator
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 3 times MTP for VCOM setting ,ID setting
- Support CABC (Content Adaptive Brightness Control) function
- Support DGC (Digital Gamma Correction) function

3. Device Overview

3.1 Block diagram



3.2 Pin description

<table>
<tr><th colspan="5">Host interface pins</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin no.</th><th>Connected with</th><th>Description</th></tr>
<tr><td>BS3 ~ BS0</td><td>I</td><td>4</td><td>VSSD / VDD1</td><td>Select the MPU interface mode as listed below:
<table>
<tr><th>BS3</th><th>BS2</th><th>BS1</th><th>BS0</th><th>MPU interface mode</th><th>DB pins</th><th>Display mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>DBI TYPE-A 8-bit (CLK-E)</td><td>DB23-DB8: Unused, DB7-DB0: Data</td><td>Type 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>DBI TYPE-A 9-bit (CLK-E)</td><td>DB23-DB9:Unused, DB8-DB0: Data</td><td>Type 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>DBI TYPE-A 16-bit (CLK-E)</td><td>DB23-DB16: Unused, DB15-DB0: Data</td><td>Type 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>DBI TYPE-A 18-bit (CLK-E)</td><td>DB23-DB18: Unused, DB17-DB0: Data</td><td>Type 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>DBI TYPE-B 8-bit</td><td>DB23-DB8: Unused DB7-DB0: Data</td><td>Type 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>DBI TYPE-B 9-bit</td><td>DB23-DB9:Unused, DB8-DB0: Data</td><td>Type 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>DBI TYPE-B 16-bit</td><td>DB23-DB16: Unused, DB15-DB0: Data</td><td>Type 1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>DBI TYPE-B 18-bit</td><td>DB23-DB18: Unused, DB17-DB0: Data</td><td>Type 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>DSI (Command mode)</td><td>DSI_CLKP, DSI_CLKN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N</td><td>Type 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3-wire serial + MDDI interface + external R (note 1)</td><td>MDDI _STBP, MDDI _STBN, MDDI _D0P, MDDI _D0N, MDDI _D1P, MDDI _D1N,</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>DBI TYPE-B 24-bit</td><td>DB23-DB0: Data</td><td>Type 1</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>3-wire serial + MDDI interface + internal R (note 1)</td><td>MDDI _STBP, MDDI _STBN, MDDI _D0P, MDDI _D0N, MDDI _D1P, MDDI _D1N,</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>DSI (Video mode)</td><td>DSI_CLKP, DSI_CLKN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N</td><td>Type 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>DPI/DBI TYPE-C Option 1</td><td>SDI/SDO, DB23-DB0</td><td>Type 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>DPI/DBI TYPE-C Option 2</td><td>SDI/SDO, DB23-DB0</td><td>Type 3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>DPI/DBI TYPE-C Option 3</td><td>SDI/SDO, DB23-DB0</td><td>Type 3</td></tr>
</table>
Pixel format (RGB565 / RGB666 / RGB888) is selected by DCS command (0x3Ah)
Note 1: 3-wire serial Interface only active on MDDI / Hibernation mode(1-lane only). Must be connected to VSSD or VDD1.</td></tr>
<tr><td>CSX</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.
If this pin is not used, please connect it to VSSD or VDD1.</td></tr>
<tr><td>RESX</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or VDD1).</td></tr>
<tr><td>RDX_E</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-A: 0: Read/Write disable, 1: Read / Write enable.
DBI Type-B: Serves as a read signal and read data at the low level.
If not use, let it open or connected to VDD1.</td></tr>
<tr><td>DCX_SCL</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-A/B: Data / Command Selection pin
DBI Type-C: it servers as SCL (Serial Clock)
If not use, let it open or connected to VDD1.</td></tr>
</table>

<table>
<tr><td>WRX_DCX</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B mode: Serves as a write signal and write data at the low level.
DBI Type-A mode: 0: Read/Write disable, 1: Read / Write enable.
If not use, let it open or connected to VDD1.</td></tr>
<tr><td>DB23~0</td><td>I/O</td><td>24</td><td>MPU</td><td>DBI type interface:
<table>
<tr><td>Data bus</td><td>Used</td><td>Unused</td></tr>
<tr><td>8-bit bus</td><td>DB7-0</td><td>DB23-8</td></tr>
<tr><td>9-bit bus</td><td>DB8-0</td><td>DB23-9</td></tr>
<tr><td>16-bit bus</td><td>DB15-0</td><td>DB23-16</td></tr>
<tr><td>18-bit bus</td><td>DB17-0</td><td>DB23-18</td></tr>
<tr><td>24-bit bus</td><td>DB23-0</td><td>-</td></tr>
</table>
DPI type interface:
<table>
<tr><td>Data bus</td><td>Used</td><td>Unused</td></tr>
<tr><td>16-bit bus</td><td>DB21-17,
DB13-8,
DB5-1</td><td>DB23-22,
DB16-14,
DB7-6, DB0</td></tr>
<tr><td>18-bit bus</td><td>DB21-16,
DB13-8,
DB5-0</td><td>DB23-22,
DB15-14,
DB7-6</td></tr>
<tr><td>24-bit bus</td><td>DB23-0</td><td>-</td></tr>
</table>
Let the unused pins open for each mode.</td></tr>
<tr><td>SDO</td><td>O</td><td>1</td><td>MPU</td><td>Serial data output. Let it to open in MPU interface mode.</td></tr>
<tr><td>SDI</td><td>I</td><td>1</td><td>MPU</td><td>Serial data input pin in serial interface operation.</td></tr>
<tr><td colspan="5">Clock input and RGB interface</td></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Line synchronizing signal.
Must be connected to VSSD or VDD1 if not used.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data enable signal in RGB I/F mode. Has to be fixed to VSSD level in MPU interface mode.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Serves VS signal pin on RGB interface. (Input pad).
Must be connected to VSSD or VDD1 if not used.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td>Dot clock signal.
Must be connected to VSSD or VDD1 if not used.</td></tr>
<tr><td colspan="5">Source driver output pins</td></tr>
<tr><td>S1 to S1441</td><td>O</td><td>1441</td><td>LCD</td><td>Output voltages applied to the liquid crystal.
<table>
<tr><td>RGB resolution</td><td>Source channels</td></tr>
<tr><td>360RGB</td><td>S1 ~ S540, S901 ~ S1440</td></tr>
<tr><td>480RGB</td><td>S1 to S1440</td></tr>
<tr><td>480RGB+Z inversion</td><td>S1 to S1441</td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td>1</td><td>MPU</td><td>Serves TE (Tearing Effect) pin on MPU interface.</td></tr>
<tr><td colspan="5">GIP control singal and bias voltage</td></tr>
<tr><td>CGOUT1_L
CGOUT2_L
CGOUT3_L
CGOUT4_L
CGOUT5_L
CGOUT6_L
CGOUT7_L
CGOUT8_L
CGOUT9_L
CGOUT10_L</td><td>O</td><td>14</td><td>GIP</td><td>Signals for right side GIP on panel view (Left side in IC bump view),
Unused pins should be left open.</td></tr>
<tr><td>CGOUT1_R
CGOUT2_R
CGOUT3_R
CGOUT4_R
CGOUT5_R
CGOUT6_R
CGOUT7_R
CGOUT8_R
CGOUT9_R
CGOUT10_R</td><td>O</td><td>14</td><td>GIP</td><td>Signals for Right side GIP on panel view (Right side in IC bump view),
Unused pins should be left open.</td></tr>
<tr><td>VBIAS</td><td>O</td><td>2</td><td>GIP</td><td>Bias voltage for some special GIP circuits. If not used, leave this pin open.</td></tr>
</table>

<table>
<tr><td colspan="6">Power supply pins</td></tr>
<tr><td>PCCS0 ~ PCCS1</td><td>I</td><td>2</td><td>VSSD / VDD3</td><td colspan="2">Select the VSP/VSN bumping method as listed below:
<table>
<tr><th>PCCS1</th><th>PCCS0</th><th>Driving mode</th></tr>
<tr><td>0</td><td>0</td><td>Setting invalid</td></tr>
<tr><td>0</td><td>1</td><td>Setting invalid</td></tr>
<tr><td>1</td><td>0</td><td>PFM one Inductor Mode (Type C)</td></tr>
<tr><td>1</td><td>1</td><td>Charge Bump Mode(Use HX5186-A)</td></tr>
</table>
Must be connected to VSSD or VDD3.</td></tr>
<tr><td>VDD1</td><td>I</td><td>5</td><td>Power supply</td><td colspan="2">A power supply for the I/O circuit. VDD1=1.65 to 3.3V</td></tr>
<tr><td>VDD2</td><td>I</td><td>6</td><td>Power supply</td><td colspan="2">A power supply for the analog power. VDD2=2.3 to 4.8V
VDD2 input level should be same as VDD3 input level to avoid the level-mismatching at internal level shifter circuit.</td></tr>
<tr><td>VDD3</td><td>I</td><td>6</td><td>Power supply</td><td colspan="2">A power supply for the logic power, DC/DC converter VDD3=2.3 to 4.8V.</td></tr>
<tr><td>VSSA</td><td>P</td><td>6</td><td>Power supply</td><td colspan="2">Analoge ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.</td></tr>
<tr><td>VSSAC</td><td>P</td><td>2</td><td>Power supply</td><td colspan="2">Analoge ground. Must connect to VSSA on the FPC.</td></tr>
<tr><td>VSSD</td><td>P</td><td>16</td><td>Power supply</td><td colspan="2">Ground for the internal logic. VSSD=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.</td></tr>
<tr><td>VPP</td><td>I</td><td>2</td><td>Power supply</td><td colspan="2">External high voltage pin used in OTP mode and operates at 7.5V.
If not used, let it open.</td></tr>
<tr><td colspan="6">Output Pins of Power and reference voltage</td></tr>
<tr><td>VSP</td><td>I</td><td>7</td><td>Stabilizing capacitor</td><td colspan="2">Input voltage from the set-up circuit (4.7V to 5.5V). it is generated from VDD3.</td></tr>
<tr><td>VSN</td><td>I</td><td>6</td><td>Stabilizing capacitor</td><td colspan="2">Input voltage from the set-up circuit (-4.7V to -5.5V). it is generated from VDD3.</td></tr>
<tr><td>VSPC</td><td>I</td><td>1</td><td>VSP</td><td colspan="2">Positive boosting reference voltage input.</td></tr>
<tr><td>VSNC</td><td>I</td><td>1</td><td>VSN</td><td colspan="2">Negative boosting reference voltage input.</td></tr>
<tr><td>VSPR</td><td>O</td><td>2</td><td>Stabilizing capacitor</td><td colspan="2">Positive regulated voltage output (3.5V to VSP - 0.5)</td></tr>
<tr><td>VSNR</td><td>O</td><td>2</td><td>Stabilizing capacitor</td><td colspan="2">Positive regulated voltage output (-3.5V to VSN + 0.5)</td></tr>
<tr><td>VDDD</td><td>O</td><td>19</td><td>Stabilizing capacitor</td><td colspan="2">Internal logic voltage output</td></tr>
<tr><td>VDDDN</td><td>O</td><td>5</td><td>Stabilizing capacitor</td><td colspan="2">Internal logic voltage output (-2.5V fixed)</td></tr>
<tr><td>VREF</td><td>O</td><td>2</td><td>Stabilizing capacitor</td><td colspan="2">Reference voltage from internal band gap circuit. The tolerance of VREF voltage is ± 3 % .(1.8V fixed)</td></tr>
<tr><td>VGH</td><td>O</td><td>10</td><td>Stabilizing capacitor</td><td colspan="2">Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGH.</td></tr>
<tr><td>VGL</td><td>O</td><td>10</td><td>Stabilizing capacitor</td><td colspan="2">Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSA and VGL.</td></tr>
<tr><td>LVGL</td><td>O</td><td>15</td><td>Stabilizing capacitor</td><td colspan="2">Most negative voltage for some special GIP circuits. If not used, connect to VGL.</td></tr>
<tr><td>VCOM</td><td>O</td><td>14</td><td>Stabilizing capacitor</td><td colspan="2">The power supply of common voltage in DC com driving. The voltage range is set between -2V to 0V. It must be connected a stabilizing capacitor 2.2u to VSSD.</td></tr>
<tr><td>VCOMR</td><td>I</td><td>1</td><td>Input</td><td colspan="2">The input pad of external VCOM voltage.</td></tr>
<tr><td colspan="6">DC/DC pumping</td></tr>
<tr><td>C21AP, C21AN
C22AP, C22AN</td><td>I/O</td><td>16</td><td>Step-up Capacitor</td><td colspan="2">Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage.</td></tr>
<tr><td>C23AP, C23AN
C24AP, C24AN</td><td>I/O</td><td>16</td><td>Step-up Capacitor</td><td colspan="2">Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage.</td></tr>
<tr><td>C41AP, C41AN</td><td>I/O</td><td>6</td><td>Step-up Capacitor</td><td colspan="2">Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the LVGL voltage.</td></tr>
<tr><td>VCSW1</td><td>O</td><td>4</td><td>-</td><td colspan="2">Boosting control output1, it needs to connect to the gate pin of NMOS on external DC/DC converter circuit. (0 to VDD3)</td></tr>
<tr><td>VCSW2</td><td>O</td><td>4</td><td>-</td><td colspan="2">Boosting control output2, it needs to connect to the gate pin of PMOS on external DC/DC converter circuit. (0 to VDD3)</td></tr>
</table>

CABC & ABC & Ambient light sensor				
CABC_PWM_OUT	**O**	**1**	**-**	Backlight on/fff control pin. If use CABC function, the pin can connect to external LED driver IC. The output voltage range=0 to VDD1.
Test Pins				
OSC	**I**	**1**	**Open**	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.(weak pull low)
TEST1	**I**	**1**	**Open**	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
TEST2	**I**	**1**	**Open**	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
VTESTOUTP	**O**	**1**	**Open**	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
VTESTOUTN	**O**	**1**	**Open**	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMYR1 **DUMMYR2**	**-**	**2**	**Open**	Dummy pads. Available for measuring the COG contact resistance. They are short-circuited within the chip.
DUMMY17~1	**-**	**17**	**Open**	Not used. Let it open.
IOGNDDUM	**-**	**3**	**Open**	Dummy pad. Connect to grand internally.
MIPI-DSI interface parts				
DSI_D0P, **DSI_D0N**	**I/O**	**6**	**DSI Host**	MIPI-DSI Data differential signal input pins. (Data lane 0) If not used, please let it connected to VSSD.
DSI_CP, **DSI_CN**	**I**	**6**	**DSI Host**	MIPI-DSI CLOCK differential signal input pins. If not used, please let it connected to VSSD.
DSI_D1P, **DSI_D1N**	**I**	**6**	**DSI Host**	MIPI-DSI Data differential signal input pins. (Data lane 1) If not used, please let it connected to VSSD.
DSI_VCC	**P**	**5**	**Power Supply**	Power supply for the MIPI DSI analog power.DSI_VCC=1.65V to 3.3V
DSI_VSS	**P**	**9**	**Ground**	MIPI DSI analogy ground. DSI_VSS=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
DSI_LDO	**O**	**2**	**Capacitor**	DSI: DSI regulator output pin. (1.2V to 1.3V) Connect to a stabilizing capacitor between DSI_VSS and DSI_LDO If not used, please open these pins.
DSI_LDO_ENB	**I**	**1**	**Input**	DSI I/F: Control signal of DSI_LDO. The default setting of DSI_LDO_ENB is Low. High: Disable the DSI_LDO. Low: Enable the DSI_LDO. It must be connected to VDD1 or VSSD. (latch type)
MDDI interface parts				
MDDI_STBP, **MDDI _STBN**	**-**	**6**	**High Speed Interface Host**	High Speed Interface clock differential signal input pins. When BS[3:0]=1001(MDDI interface + external R), please connect to a terminal resistance (100Ω) between MDDI_STBP and MDDI_STBN. If not used, please let it connected to VSSD.
MDDI _D0P, **MDDI _D0N**	**-**	**6**	**High Speed Interface Host**	High Speed Interface Data differential signal input pins (Data lane 0). When BS[3:0]=1001(MDDI interface + external R), please connect to a terminal resistance (100Ω) between MDDI_D0P and MDDI_D0N. If not used, please let it connected to VSSD.
MDDI _D1P, **MDDI _D1N**	**-**	**6**	**High Speed Interface Host**	High Speed Interface Data differential signal input pins. (Data lane 1) When BS[3:0]=1001(MDDI interface + external R), please connect to a terminal resistance (100Ω) between MDDI_D1P and MDDI_D1N. If not used, please let it connected to VSSD.
MDDI _VCC	**P**	**5**	**Power Supply or Capacitor**	High Speed Interface I/O power supply pin, 2.3V to 3.3V.
MDDI _VSS	**P**	**9**	**Ground**	High Speed Interface I/O ground pin.
MDDI _LDO	**O**	**2**	**Capacitor**	High Speed Interface regulator output pin. Connect to a stabilizing capacitor between MDDI_VSS and MDDI_LDO. If not used, please open these pins.
MDDI_LDO_ENB	**I**	**1**	**Input**	MDDI I/F: Control signal of MDDI_LDO. The default setting of MDDI_LDO_ENB is Low. High: Disable the MDDI _LDO. Low: Enable the MDDI _LDO. It must be connected to VDD1 or VSSD. (latch type)

3.3 Pin assignment

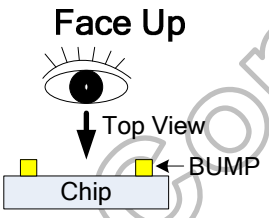
- Chip Size : 22430 x 1701 um
  (Include scribe line = 80 um)
- Chip thickness: 250 um ± 25 um

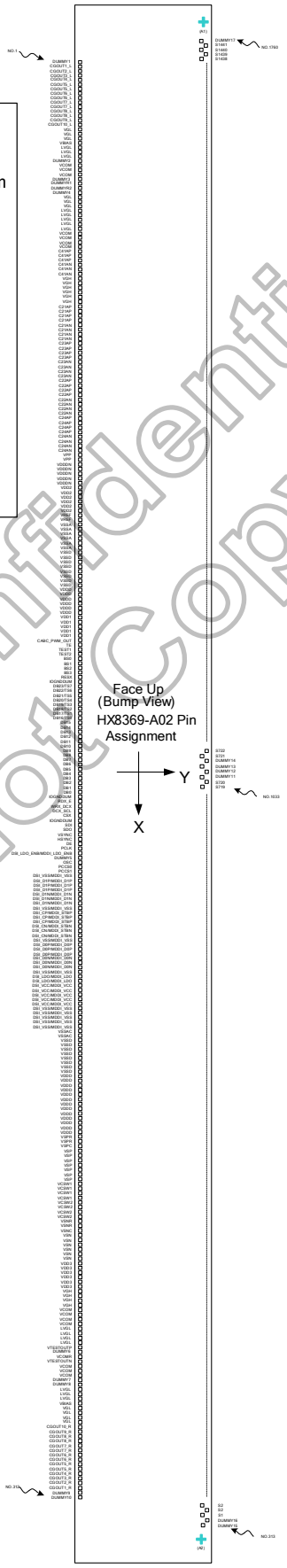
. Pad Location:PAD Center
. Coordinate Origin:Chip Center
. Au Bump Size:

1. 50 um x 80 um
   Input:
   No.1 ~ No.312

2. 15 um x 95 um
   Staggered LCD output side
   No.313 ~ No.1760

- The chip size includes the core size seal ring size, and scribe line size
- Au bump pitch:Refer to Pad Coordinate
- Au bump height : 12 um ± 3 um
- Numbers in the figure corresponds to pad coordinate numbers





3.4 PAD coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY1	-10885	-672	61	C21AN	-6685	-672	121	VDDD	-2485	-672	181	DSI_D1P / MDDI_D1P	1715	-672
2	CGOUT1_L	-10815	-672	62	C21AN	-6615	-672	122	VDD1	-2415	-672	182	DSI_D1N / MDDI_D1N	1785	-672
3	CGOUT2_L	-10745	-672	63	C23AP	-6545	-672	123	VDD1	-2345	-672	183	DSI_D1N / MDDI_D1N	1855	-672
4	CGOUT3_L	-10675	-672	64	C23AP	-6475	-672	124	VDD1	-2275	-672	184	DSI_D1N / MDDI_D1N	1925	-672
5	CGOUT4_L	-10605	-672	65	C23AP	-6405	-672	125	VDD1	-2205	-672	185	DSI_VSS / MDDI_VSS	1995	-672
6	CGOUT5_L	-10535	-672	66	C23AP	-6335	-672	126	VDD1	-2135	-672	186	DSI_CP / MDDI_STBP	2065	-672
7	CGOUT5_L	-10465	-672	67	C23AN	-6265	-672	127	CABC_PWM_OUT	-2065	-672	187	DSI_CP / MDDI_STBP	2135	-672
8	CGOUT6_L	-10395	-672	68	C23AN	-6195	-672	128	TE	-1995	-672	188	DSI_CP / MDDI_STBP	2205	-672
9	CGOUT6_L	-10325	-672	69	C23AN	-6125	-672	129	TEST1	-1925	-672	189	DSI_CN / MDDI_STBN	2275	-672
10	CGOUT7_L	-10255	-672	70	C23AN	-6055	-672	130	TEST2	-1855	-672	190	DSI_CN / MDDI_STBN	2345	-672
11	CGOUT7_L	-10185	-672	71	C22AP	-5985	-672	131	BS0	-1785	-672	191	DSI_CN / MDDI_STBN	2415	-672
12	CGOUT8_L	-10115	-672	72	C22AP	-5915	-672	132	BS1	-1715	-672	192	DSI_VSS / MDDI_VSS	2485	-672
13	CGOUT8_L	-10045	-672	73	C22AP	-5845	-672	133	BS2	-1645	-672	193	DSI_D0P / MDDI_D0P	2555	-672
14	CGOUT9_L	-9975	-672	74	C22AP	-5775	-672	134	BS3	-1575	-672	194	DSI_D0P / MDDI_D0P	2625	-672
15	CGOUT10_L	-9905	-672	75	C22AN	-5705	-672	135	RESX	-1505	-672	195	DSI_D0P / MDDI_D0P	2695	-672
16	VGL	-9835	-672	76	C22AN	-5635	-672	136	IOGNDDUM	-1435	-672	196	DSI_D0N / MDDI_D0N	2765	-672
17	VGL	-9765	-672	77	C22AN	-5565	-672	137	DB23	-1365	-672	197	DSI_D0N / MDDI_D0N	2835	-672
18	VGL	-9695	-672	78	C22AN	-5495	-672	138	DB22	-1295	-672	198	DSI_D0N / MDDI_D0N	2905	-672
19	VBIAS	-9625	-672	79	C24AP	-5425	-672	139	DB21	-1225	-672	199	DSI_VSS / MDDI_VSS	2975	-672
20	LVGL	-9555	-672	80	C24AP	-5355	-672	140	DB20	-1155	-672	200	DSI_LDO / MDDI_LDO	3045	-672
21	LVGL	-9485	-672	81	C24AP	-5285	-672	141	DB19	-1085	-672	201	DSI_LDO / MDDI_LDO	3115	-672
22	LVGL	-9415	-672	82	C24AP	-5215	-672	142	DB18	-1015	-672	202	DSI_VCC / MDDI_VCC	3185	-672
23	DUMMY2	-9345	-672	83	C24AN	-5145	-672	143	DB17	-945	-672	203	DSI_VCC / MDDI_VCC	3255	-672
24	VCOM	-9275	-672	84	C24AN	-5075	-672	144	DB16	-875	-672	204	DSI_VCC / MDDI_VCC	3325	-672
25	VCOM	-9205	-672	85	C24AN	-5005	-672	145	DB15	-805	-672	205	DSI_VCC / MDDI_VCC	3395	-672
26	VCOM	-9135	-672	86	C24AN	-4935	-672	146	DB14	-735	-672	206	DSI_VCC / MDDI_VCC	3465	-672
27	DUMMY3	-9065	-672	87	VPP	-4865	-672	147	DB13	-665	-672	207	DSI_VSS / MDDI_VSS	3535	-672
28	DUMMYR1	-8995	-672	88	VPP	-4795	-672	148	DB12	-595	-672	208	DSI_VSS / MDDI_VSS	3605	-672
29	DUMMYR2	-8925	-672	89	VDDDN	-4725	-672	149	DB11	-525	-672	209	DSI_VSS / MDDI_VSS	3675	-672
30	DUMMY4	-8855	-672	90	VDDDN	-4655	-672	150	DB10	-455	-672	210	DSI_VSS / MDDI_VSS	3745	-672
31	VGL	-8785	-672	91	VDDDN	-4585	-672	151	DB9	-385	-672	211	DSI_VSS / MDDI_VSS	3815	-672
32	VGL	-8715	-672	92	VDDDN	-4515	-672	152	DB8	-315	-672	212	VSSAC	3885	-672
33	VGL	-8645	-672	93	VDDDN	-4445	-672	153	DB7	-245	-672	213	VSSAC	3955	-672
34	LVGL	-8575	-672	94	VDD2	-4375	-672	154	DB6	-175	-672	214	VSSD	4025	-672
35	LVGL	-8505	-672	95	VDD2	-4305	-672	155	DB5	-105	-672	215	VSSD	4095	-672
36	LVGL	-8435	-672	96	VDD2	-4235	-672	156	DB4	-35	-672	216	VSSD	4165	-672
37	LVGL	-8365	-672	97	VDD2	-4165	-672	157	DB3	35	-672	217	VSSD	4235	-672
38	LVGL	-8295	-672	98	VDD2	-4095	-672	158	DB2	105	-672	218	VSSD	4305	-672
39	VCOM	-8225	-672	99	VDD2	-4025	-672	159	DB1	175	-672	219	VSSD	4375	-672
40	VCOM	-8155	-672	100	VREF	-3955	-672	160	DB0	245	-672	220	VSSD	4445	-672
41	VCOM	-8085	-672	101	VREF	-3885	-672	161	IOGNDDUM	315	-672	221	VSSD	4515	-672
42	VCOM	-8015	-672	102	VSSA	-3815	-672	162	RDX_E	385	-672	222	VDDD	4585	-672
43	C41AP	-7945	-672	103	VSSA	-3745	-672	163	WRX_DCX	455	-672	223	VDDD	4655	-672
44	C41AP	-7875	-672	104	VSSA	-3675	-672	164	DCX_SCL	525	-672	224	VDDD	4725	-672
45	C41AP	-7805	-672	105	VSSA	-3605	-672	165	CSX	595	-672	225	VDDD	4795	-672
46	C41AN	-7735	-672	106	VSSA	-3535	-672	166	IOGNDDUM	665	-672	226	VDDD	4865	-672
47	C41AN	-7665	-672	107	VSSA	-3465	-672	167	SDI	735	-672	227	VDDD	4935	-672
48	C41AN	-7595	-672	108	VSSD	-3395	-672	168	SDO	805	-672	228	VDDD	5005	-672
49	VGH	-7525	-672	109	VSSD	-3325	-672	169	VSYNC	875	-672	229	VDDD	5075	-672
50	VGH	-7455	-672	110	VSSD	-3255	-672	170	HSYNC	945	-672	230	VDDD	5145	-672
51	VGH	-7385	-672	111	VSSD	-3185	-672	171	DE	1015	-672	231	VDDD	5215	-672
52	VGH	-7315	-672	112	VSSD	-3115	-672	172	PCLK	1085	-672	232	VDDD	5285	-672
53	VGH	-7245	-672	113	VSSD	-3045	-672	173	DSI_LDO_ENB	1155	-672	233	VDDD	5355	-672
54	VGH	-7175	-672	114	VSSD	-2975	-672	174	DUMMY5	1225	-672	234	VDDD	5425	-672
55	C21AP	-7105	-672	115	VSSD	-2905	-672	175	OSC	1295	-672	235	VSPR	5495	-672
56	C21AP	-7035	-672	116	VDDD	-2835	-672	176	PCCS0	1365	-672	236	VSPR	5565	-672
57	C21AP	-6965	-672	117	VDDD	-2765	-672	177	PCCS1	1435	-672	237	VSPC	5635	-672
58	C21AP	-6895	-672	118	VDDD	-2695	-672	178	DSI_VSS / MDDI_VSS	1505	-672	238	VSP	5705	-672
59	C21AN	-6825	-672	119	VDDD	-2625	-672	179	DSI_D1P / MDDI_D1P	1575	-672	239	VSP	5775	-672
60	C21AN	-6755	-672	120	VDDD	-2555	-672	180	DSI_D1P / MDDI_D1P	1645	-672	240	VSP	5845	-672

No.	Name	X	Y
241	VSP	5915	-672
242	VSP	5985	-672
243	VSP	6055	-672
244	VSP	6125	-672
245	VCSW1	6195	-672
246	VCSW1	6265	-672
247	VCSW1	6335	-672
248	VCSW1	6405	-672
249	VCSW2	6475	-672
250	VCSW2	6545	-672
251	VCSW2	6615	-672
252	VCSW2	6685	-672
253	VSNR	6755	-672
254	VSNR	6825	-672
255	VSNC	6895	-672
256	VSN	6965	-672
257	VSN	7035	-672
258	VSN	7105	-672
259	VSN	7175	-672
260	VSN	7245	-672
261	VSN	7315	-672
262	VDD3	7385	-672
263	VDD3	7455	-672
264	VDD3	7525	-672
265	VDD3	7595	-672
266	VDD3	7665	-672
267	VDD3	7735	-672
268	VGH	7805	-672
269	VGH	7875	-672
270	VGH	7945	-672
271	VGH	8015	-672
272	VCOM	8085	-672
273	VCOM	8155	-672
274	VCOM	8225	-672
275	VCOM	8295	-672
276	LVGL	8365	-672
277	LVGL	8435	-672
278	LVGL	8505	-672
279	LVGL	8575	-672
280	VTESTOUTP	8645	-672
281	DUMMY6	8715	-672
282	VCOMR	8785	-672
283	VTESTOUTN	8855	-672
284	VCOM	8925	-672
285	VCOM	8995	-672
286	VCOM	9065	-672
287	DUMMY7	9135	-672
288	DUMMY8	9205	-672
289	LVGL	9275	-672
290	LVGL	9345	-672
291	LVGL	9415	-672
292	VBIAS	9485	-672
293	VGL	9555	-672
294	VGL	9625	-672
295	VGL	9695	-672
296	VGL	9765	-672
297	CGOUT10_R	9835	-672
298	CGOUT9_R	9905	-672
299	CGOUT8_R	9975	-672
300	CGOUT8_R	10045	-672
301	CGOUT7_R	10115	-672
302	CGOUT7_R	10185	-672
303	CGOUT6_R	10255	-672
304	CGOUT6_R	10325	-672
305	CGOUT5_R	10395	-672
306	CGOUT5_R	10465	-672
307	CGOUT4_R	10535	-672
308	CGOUT3_R	10605	-672
309	CGOUT2_R	10675	-672
310	CGOUT1_R	10745	-672
311	DUMMY9	10815	-672
312	DUMMY10	10885	-672
313	DUMMY15	10950	500
314	DUMMY16	10935	613
315	S1	10920	500
316	S2	10905	613
317	S3	10890	500
318	S4	10875	613
319	S5	10860	500
320	S6	10845	613
321	S7	10830	500
322	S8	10815	613
323	S9	10800	500
324	S10	10785	613
325	S11	10770	500
326	S12	10755	613
327	S13	10740	500
328	S14	10725	613
329	S15	10710	500
330	S16	10695	613
331	S17	10680	500
332	S18	10665	613
333	S19	10650	500
334	S20	10635	613
335	S21	10620	500
336	S22	10605	613
337	S23	10590	500
338	S24	10575	613
339	S25	10560	500
340	S26	10545	613
341	S27	10530	500
342	S28	10515	613
343	S29	10500	500
344	S30	10485	613
345	S31	10470	500
346	S32	10455	613
347	S33	10440	500
348	S34	10425	613
349	S35	10410	500
350	S36	10395	613
351	S37	10380	500
352	S38	10365	613
353	S39	10350	500
354	S40	10335	613
355	S41	10320	500
356	S42	10305	613
357	S43	10290	500
358	S44	10275	613
359	S45	10260	500
360	S46	10245	613
361	S47	10230	500
362	S48	10215	613
363	S49	10200	500
364	S50	10185	613
365	S51	10170	500
366	S52	10155	613
367	S53	10140	500
368	S54	10125	613
369	S55	10110	500
370	S56	10095	613
371	S57	10080	500
372	S58	10065	613
373	S59	10050	500
374	S60	10035	613
375	S61	10020	500
376	S62	10005	613
377	S63	9990	500
378	S64	9975	613
379	S65	9960	500
380	S66	9945	613
381	S67	9930	500
382	S68	9915	613
383	S69	9900	500
384	S70	9885	613
385	S71	9870	500
386	S72	9855	613
387	S73	9840	500
388	S74	9825	613
389	S75	9810	500
390	S76	9795	613
391	S77	9780	500
392	S78	9765	613
393	S79	9750	500
394	S80	9735	613
395	S81	9720	500
396	S82	9705	613
397	S83	9690	500
398	S84	9675	613
399	S85	9660	500
400	S86	9645	613
401	S87	9630	500
402	S88	9615	613
403	S89	9600	500
404	S90	9585	613
405	S91	9570	500
406	S92	9555	613
407	S93	9540	500
408	S94	9525	613
409	S95	9510	500
410	S96	9495	613
411	S97	9480	500
412	S98	9465	613
413	S99	9450	500
414	S100	9435	613
415	S101	9420	500
416	S102	9405	613
417	S103	9390	500
418	S104	9375	613
419	S105	9360	500
420	S106	9345	613
421	S107	9330	500
422	S108	9315	613
423	S109	9300	500
424	S110	9285	613
425	S111	9270	500
426	S112	9255	613
427	S113	9240	500
428	S114	9225	613
429	S115	9210	500
430	S116	9195	613
431	S117	9180	500
432	S118	9165	613
433	S119	9150	500
434	S120	9135	613
435	S121	9120	500
436	S122	9105	613
437	S123	9090	500
438	S124	9075	613
439	S125	9060	500
440	S126	9045	613
441	S127	9030	500
442	S128	9015	613
443	S129	9000	500
444	S130	8985	613
445	S131	8970	500
446	S132	8955	613
447	S133	8940	500
448	S134	8925	613
449	S135	8910	500
450	S136	8895	613
451	S137	8880	500
452	S138	8865	613
453	S139	8850	500
454	S140	8835	613
455	S141	8820	500
456	S142	8805	613
457	S143	8790	500
458	S144	8775	613
459	S145	8760	500
460	S146	8745	613
461	S147	8730	500
462	S148	8715	613
463	S149	8700	500
464	S150	8685	613
465	S151	8670	500
466	S152	8655	613
467	S153	8640	500
468	S154	8625	613
469	S155	8610	500
470	S156	8595	613
471	S157	8580	500
472	S158	8565	613
473	S159	8550	500
474	S160	8535	613
475	S161	8520	500
476	S162	8505	613
477	S163	8490	500
478	S164	8475	613
479	S165	8460	500
480	S166	8445	613

No.	Name	X	Y
481	S167	8430	500
482	S168	8415	613
483	S169	8400	500
484	S170	8385	613
485	S171	8370	500
486	S172	8355	613
487	S173	8340	500
488	S174	8325	613
489	S175	8310	500
490	S176	8295	613
491	S177	8280	500
492	S178	8265	613
493	S179	8250	500
494	S180	8235	613
495	S181	8220	500
496	S182	8205	613
497	S183	8190	500
498	S184	8175	613
499	S185	8160	500
500	S186	8145	613
501	S187	8130	500
502	S188	8115	613
503	S189	8100	500
504	S190	8085	613
505	S191	8070	500
506	S192	8055	613
507	S193	8040	500
508	S194	8025	613
509	S195	8010	500
510	S196	7995	613
511	S197	7980	500
512	S198	7965	613
513	S199	7950	500
514	S200	7935	613
515	S201	7920	500
516	S202	7905	613
517	S203	7890	500
518	S204	7875	613
519	S205	7860	500
520	S206	7845	613
521	S207	7830	500
522	S208	7815	613
523	S209	7800	500
524	S210	7785	613
525	S211	7770	500
526	S212	7755	613
527	S213	7740	500
528	S214	7725	613
529	S215	7710	500
530	S216	7695	613
531	S217	7680	500
532	S218	7665	613
533	S219	7650	500
534	S220	7635	613
535	S221	7620	500
536	S222	7605	613
537	S223	7590	500
538	S224	7575	613
539	S225	7560	500
540	S226	7545	613

No.	Name	X	Y
541	S227	7530	500
542	S228	7515	613
543	S229	7500	500
544	S230	7485	613
545	S231	7470	500
546	S232	7455	613
547	S233	7440	500
548	S234	7425	613
549	S235	7410	500
550	S236	7395	613
551	S237	7380	500
552	S238	7365	613
553	S239	7350	500
554	S240	7335	613
555	S241	7320	500
556	S242	7305	613
557	S243	7290	500
558	S244	7275	613
559	S245	7260	500
560	S246	7245	613
561	S247	7230	500
562	S248	7215	613
563	S249	7200	500
564	S250	7185	613
565	S251	7170	500
566	S252	7155	613
567	S253	7140	500
568	S254	7125	613
569	S255	7110	500
570	S256	7095	613
571	S257	7080	500
572	S258	7065	613
573	S259	7050	500
574	S260	7035	613
575	S261	7020	500
576	S262	7005	613
577	S263	6990	500
578	S264	6975	613
579	S265	6960	500
580	S266	6945	613
581	S267	6930	500
582	S268	6915	613
583	S269	6900	500
584	S270	6885	613
585	S271	6870	500
586	S272	6855	613
587	S273	6840	500
588	S274	6825	613
589	S275	6810	500
590	S276	6795	613
591	S277	6780	500
592	S278	6765	613
593	S279	6750	500
594	S280	6735	613
595	S281	6720	500
596	S282	6705	613
597	S283	6690	500
598	S284	6675	613
599	S285	6660	500
600	S286	6645	613

No.	Name	X	Y
601	S287	6630	500
602	S288	6615	613
603	S289	6600	500
604	S290	6585	613
605	S291	6570	500
606	S292	6555	613
607	S293	6540	500
608	S294	6525	613
609	S295	6510	500
610	S296	6495	613
611	S297	6480	500
612	S298	6465	613
613	S299	6450	500
614	S300	6435	613
615	S301	6420	500
616	S302	6405	613
617	S303	6390	500
618	S304	6375	613
619	S305	6360	500
620	S306	6345	613
621	S307	6330	500
622	S308	6315	613
623	S309	6300	500
624	S310	6285	613
625	S311	6270	500
626	S312	6255	613
627	S313	6240	500
628	S314	6225	613
629	S315	6210	500
630	S316	6195	613
631	S317	6180	500
632	S318	6165	613
633	S319	6150	500
634	S320	6135	613
635	S321	6120	500
636	S322	6105	613
637	S323	6090	500
638	S324	6075	613
639	S325	6060	500
640	S326	6045	613
641	S327	6030	500
642	S328	6015	613
643	S329	6000	500
644	S330	5985	613
645	S331	5970	500
646	S332	5955	613
647	S333	5940	500
648	S334	5925	613
649	S335	5910	500
650	S336	5895	613
651	S337	5880	500
652	S338	5865	613
653	S339	5850	500
654	S340	5835	613
655	S341	5820	500
656	S342	5805	613
657	S343	5790	500
658	S344	5775	613
659	S345	5760	500
660	S346	5745	613

No.	Name	X	Y
661	S347	5730	500
662	S348	5715	613
663	S349	5700	500
664	S350	5685	613
665	S351	5670	500
666	S352	5655	613
667	S353	5640	500
668	S354	5625	613
669	S355	5610	500
670	S356	5595	613
671	S357	5580	500
672	S358	5565	613
673	S359	5550	500
674	S360	5535	613
675	S361	5520	500
676	S362	5505	613
677	S363	5490	500
678	S364	5475	613
679	S365	5460	500
680	S366	5445	613
681	S367	5430	500
682	S368	5415	613
683	S369	5400	500
684	S370	5385	613
685	S371	5370	500
686	S372	5355	613
687	S373	5340	500
688	S374	5325	613
689	S375	5310	500
690	S376	5295	613
691	S377	5280	500
692	S378	5265	613
693	S379	5250	500
694	S380	5235	613
695	S381	5220	500
696	S382	5205	613
697	S383	5190	500
698	S384	5175	613
699	S385	5160	500
700	S386	5145	613
701	S387	5130	500
702	S388	5115	613
703	S389	5100	500
704	S390	5085	613
705	S391	5070	500
706	S392	5055	613
707	S393	5040	500
708	S394	5025	613
709	S395	5010	500
710	S396	4995	613
711	S397	4980	500
712	S398	4965	613
713	S399	4950	500
714	S400	4935	613
715	S401	4920	500
716	S402	4905	613
717	S403	4890	500
718	S404	4875	613
719	S405	4860	500
720	S406	4845	613

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
721	S407	4830	500	781	S467	3930	500	841	S527	3030	500	901	S587	2130	500
722	S408	4815	613	782	S468	3915	613	842	S528	3015	613	902	S588	2115	613
723	S409	4800	500	783	S469	3900	500	843	S529	3000	500	903	S589	2100	500
724	S410	4785	613	784	S470	3885	613	844	S530	2985	613	904	S590	2085	613
725	S411	4770	500	785	S471	3870	500	845	S531	2970	500	905	S591	2070	500
726	S412	4755	613	786	S472	3855	613	846	S532	2955	613	906	S592	2055	613
727	S413	4740	500	787	S473	3840	500	847	S533	2940	500	907	S593	2040	500
728	S414	4725	613	788	S474	3825	613	848	S534	2925	613	908	S594	2025	613
729	S415	4710	500	789	S475	3810	500	849	S535	2910	500	909	S595	2010	500
730	S416	4695	613	790	S476	3795	613	850	S536	2895	613	910	S596	1995	613
731	S417	4680	500	791	S477	3780	500	851	S537	2880	500	911	S597	1980	500
732	S418	4665	613	792	S478	3765	613	852	S538	2865	613	912	S598	1965	613
733	S419	4650	500	793	S479	3750	500	853	S539	2850	500	913	S599	1950	500
734	S420	4635	613	794	S480	3735	613	854	S540	2835	613	914	S600	1935	613
735	S421	4620	500	795	S481	3720	500	855	S541	2820	500	915	S601	1920	500
736	S422	4605	613	796	S482	3705	613	856	S542	2805	613	916	S602	1905	613
737	S423	4590	500	797	S483	3690	500	857	S543	2790	500	917	S603	1890	500
738	S424	4575	613	798	S484	3675	613	858	S544	2775	613	918	S604	1875	613
739	S425	4560	500	799	S485	3660	500	859	S545	2760	500	919	S605	1860	500
740	S426	4545	613	800	S486	3645	613	860	S546	2745	613	920	S606	1845	613
741	S427	4530	500	801	S487	3630	500	861	S547	2730	500	921	S607	1830	500
742	S428	4515	613	802	S488	3615	613	862	S548	2715	613	922	S608	1815	613
743	S429	4500	500	803	S489	3600	500	863	S549	2700	500	923	S609	1800	500
744	S430	4485	613	804	S490	3585	613	864	S550	2685	613	924	S610	1785	613
745	S431	4470	500	805	S491	3570	500	865	S551	2670	500	925	S611	1770	500
746	S432	4455	613	806	S492	3555	613	866	S552	2655	613	926	S612	1755	613
747	S433	4440	500	807	S493	3540	500	867	S553	2640	500	927	S613	1740	500
748	S434	4425	613	808	S494	3525	613	868	S554	2625	613	928	S614	1725	613
749	S435	4410	500	809	S495	3510	500	869	S555	2610	500	929	S615	1710	500
750	S436	4395	613	810	S496	3495	613	870	S556	2595	613	930	S616	1695	613
751	S437	4380	500	811	S497	3480	500	871	S557	2580	500	931	S617	1680	500
752	S438	4365	613	812	S498	3465	613	872	S558	2565	613	932	S618	1665	613
753	S439	4350	500	813	S499	3450	500	873	S559	2550	500	933	S619	1650	500
754	S440	4335	613	814	S500	3435	613	874	S560	2535	613	934	S620	1635	613
755	S441	4320	500	815	S501	3420	500	875	S561	2520	500	935	S621	1620	500
756	S442	4305	613	816	S502	3405	613	876	S562	2505	613	936	S622	1605	613
757	S443	4290	500	817	S503	3390	500	877	S563	2490	500	937	S623	1590	500
758	S444	4275	613	818	S504	3375	613	878	S564	2475	613	938	S624	1575	613
759	S445	4260	500	819	S505	3360	500	879	S565	2460	500	939	S625	1560	500
760	S446	4245	613	820	S506	3345	613	880	S566	2445	613	940	S626	1545	613
761	S447	4230	500	821	S507	3330	500	881	S567	2430	500	941	S627	1530	500
762	S448	4215	613	822	S508	3315	613	882	S568	2415	613	942	S628	1515	613
763	S449	4200	500	823	S509	3300	500	883	S569	2400	500	943	S629	1500	500
764	S450	4185	613	824	S510	3285	613	884	S570	2385	613	944	S630	1485	613
765	S451	4170	500	825	S511	3270	500	885	S571	2370	500	945	S631	1470	500
766	S452	4155	613	826	S512	3255	613	886	S572	2355	613	946	S632	1455	613
767	S453	4140	500	827	S513	3240	500	887	S573	2340	500	947	S633	1440	500
768	S454	4125	613	828	S514	3225	613	888	S574	2325	613	948	S634	1425	613
769	S455	4110	500	829	S515	3210	500	889	S575	2310	500	949	S635	1410	500
770	S456	4095	613	830	S516	3195	613	890	S576	2295	613	950	S636	1395	613
771	S457	4080	500	831	S517	3180	500	891	S577	2280	500	951	S637	1380	500
772	S458	4065	613	832	S518	3165	613	892	S578	2265	613	952	S638	1365	613
773	S459	4050	500	833	S519	3150	500	893	S579	2250	500	953	S639	1350	500
774	S460	4035	613	834	S520	3135	613	894	S580	2235	613	954	S640	1335	613
775	S461	4020	500	835	S521	3120	500	895	S581	2220	500	955	S641	1320	500
776	S462	4005	613	836	S522	3105	613	896	S582	2205	613	956	S642	1305	613
777	S463	3990	500	837	S523	3090	500	897	S583	2190	500	957	S643	1290	500
778	S464	3975	613	838	S524	3075	613	898	S584	2175	613	958	S644	1275	613
779	S465	3960	500	839	S525	3060	500	899	S585	2160	500	959	S645	1260	500
780	S466	3945	613	840	S526	3045	613	900	S586	2145	613	960	S646	1245	613

No.	Name	X	Y
961	S647	1230	500
962	S648	1215	613
963	S649	1200	500
964	S650	1185	613
965	S651	1170	500
966	S652	1155	613
967	S653	1140	500
968	S654	1125	613
969	S655	1110	500
970	S656	1095	613
971	S657	1080	500
972	S658	1065	613
973	S659	1050	500
974	S660	1035	613
975	S661	1020	500
976	S662	1005	613
977	S663	990	500
978	S664	975	613
979	S665	960	500
980	S666	945	613
981	S667	930	500
982	S668	915	613
983	S669	900	500
984	S670	885	613
985	S671	870	500
986	S672	855	613
987	S673	840	500
988	S674	825	613
989	S675	810	500
990	S676	795	613
991	S677	780	500
992	S678	765	613
993	S679	750	500
994	S680	735	613
995	S681	720	500
996	S682	705	613
997	S683	690	500
998	S684	675	613
999	S685	660	500
1000	S686	645	613
1001	S687	630	500
1002	S688	615	613
1003	S689	600	500
1004	S690	585	613
1005	S691	570	500
1006	S692	555	613
1007	S693	540	500
1008	S694	525	613
1009	S695	510	500
1010	S696	495	613
1011	S697	480	500
1012	S698	465	613
1013	S699	450	500
1014	S700	435	613
1015	S701	420	500
1016	S702	405	613
1017	S703	390	500
1018	S704	375	613
1019	S705	360	500
1020	S706	345	613

No.	Name	X	Y
1021	S707	330	500
1022	S708	315	613
1023	S709	300	500
1024	S710	285	613
1025	S711	270	500
1026	S712	255	613
1027	S713	240	500
1028	S714	225	613
1029	S715	210	500
1030	S716	195	613
1031	S717	180	500
1032	S718	165	613
1033	S719	150	500
1034	S720	135	613
1035	DUMMY11	90	613
1036	DUMMY12	30	613
1037	DUMMY13	-30	613
1038	DUMMY14	-90	613
1039	S721	-135	613
1040	S722	-150	500
1041	S723	-165	613
1042	S724	-180	500
1043	S725	-195	613
1044	S726	-210	500
1045	S727	-225	613
1046	S728	-240	500
1047	S729	-255	613
1048	S730	-270	500
1049	S731	-285	613
1050	S732	-300	500
1051	S733	-315	613
1052	S734	-330	500
1053	S735	-345	613
1054	S736	-360	500
1055	S737	-375	613
1056	S738	-390	500
1057	S739	-405	613
1058	S740	-420	500
1059	S741	-435	613
1060	S742	-450	500
1061	S743	-465	613
1062	S744	-480	500
1063	S745	-495	613
1064	S746	-510	500
1065	S747	-525	613
1066	S748	-540	500
1067	S749	-555	613
1068	S750	-570	500
1069	S751	-585	613
1070	S752	-600	500
1071	S753	-615	613
1072	S754	-630	500
1073	S755	-645	613
1074	S756	-660	500
1075	S757	-675	613
1076	S758	-690	500
1077	S759	-705	613
1078	S760	-720	500
1079	S761	-735	613
1080	S762	-750	500

No.	Name	X	Y
1081	S763	-765	613
1082	S764	-780	500
1083	S765	-795	613
1084	S766	-810	500
1085	S767	-825	613
1086	S768	-840	500
1087	S769	-855	613
1088	S770	-870	500
1089	S771	-885	613
1090	S772	-900	500
1091	S773	-915	613
1092	S774	-930	500
1093	S775	-945	613
1094	S776	-960	500
1095	S777	-975	613
1096	S778	-990	500
1097	S779	-1005	613
1098	S780	-1020	500
1099	S781	-1035	613
1100	S782	-1050	500
1101	S783	-1065	613
1102	S784	-1080	500
1103	S785	-1095	613
1104	S786	-1110	500
1105	S787	-1125	613
1106	S788	-1140	500
1107	S789	-1155	613
1108	S790	-1170	500
1109	S791	-1185	613
1110	S792	-1200	500
1111	S793	-1215	613
1112	S794	-1230	500
1113	S795	-1245	613
1114	S796	-1260	500
1115	S797	-1275	613
1116	S798	-1290	500
1117	S799	-1305	613
1118	S800	-1320	500
1119	S801	-1335	613
1120	S802	-1350	500
1121	S803	-1365	613
1122	S804	-1380	500
1123	S805	-1395	613
1124	S806	-1410	500
1125	S807	-1425	613
1126	S808	-1440	500
1127	S809	-1455	613
1128	S810	-1470	500
1129	S811	-1485	613
1130	S812	-1500	500
1131	S813	-1515	613
1132	S814	-1530	500
1133	S815	-1545	613
1134	S816	-1560	500
1135	S817	-1575	613
1136	S818	-1590	500
1137	S819	-1605	613
1138	S820	-1620	500
1139	S821	-1635	613
1140	S822	-1650	500

No.	Name	X	Y
1141	S823	-1665	613
1142	S824	-1680	500
1143	S825	-1695	613
1144	S826	-1710	500
1145	S827	-1725	613
1146	S828	-1740	500
1147	S829	-1755	613
1148	S830	-1770	500
1149	S831	-1785	613
1150	S832	-1800	500
1151	S833	-1815	613
1152	S834	-1830	500
1153	S835	-1845	613
1154	S836	-1860	500
1155	S837	-1875	613
1156	S838	-1890	500
1157	S839	-1905	613
1158	S840	-1920	500
1159	S841	-1935	613
1160	S842	-1950	500
1161	S843	-1965	613
1162	S844	-1980	500
1163	S845	-1995	613
1164	S846	-2010	500
1165	S847	-2025	613
1166	S848	-2040	500
1167	S849	-2055	613
1168	S850	-2070	500
1169	S851	-2085	613
1170	S852	-2100	500
1171	S853	-2115	613
1172	S854	-2130	500
1173	S855	-2145	613
1174	S856	-2160	500
1175	S857	-2175	613
1176	S858	-2190	500
1177	S859	-2205	613
1178	S860	-2220	500
1179	S861	-2235	613
1180	S862	-2250	500
1181	S863	-2265	613
1182	S864	-2280	500
1183	S865	-2295	613
1184	S866	-2310	500
1185	S867	-2325	613
1186	S868	-2340	500
1187	S869	-2355	613
1188	S870	-2370	500
1189	S871	-2385	613
1190	S872	-2400	500
1191	S873	-2415	613
1192	S874	-2430	500
1193	S875	-2445	613
1194	S876	-2460	500
1195	S877	-2475	613
1196	S878	-2490	500
1197	S879	-2505	613
1198	S880	-2520	500
1199	S881	-2535	613
1200	S882	-2550	500

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1201	S883	-2565	613	1261	S943	-3465	613	1321	S1003	-4365	613	1381	S1063	-5265	613
1202	S884	-2580	500	1262	S944	-3480	500	1322	S1004	-4380	500	1382	S1064	-5280	500
1203	S885	-2595	613	1263	S945	-3495	613	1323	S1005	-4395	613	1383	S1065	-5295	613
1204	S886	-2610	500	1264	S946	-3510	500	1324	S1006	-4410	500	1384	S1066	-5310	500
1205	S887	-2625	613	1265	S947	-3525	613	1325	S1007	-4425	613	1385	S1067	-5325	613
1206	S888	-2640	500	1266	S948	-3540	500	1326	S1008	-4440	500	1386	S1068	-5340	500
1207	S889	-2655	613	1267	S949	-3555	613	1327	S1009	-4455	613	1387	S1069	-5355	613
1208	S890	-2670	500	1268	S950	-3570	500	1328	S1010	-4470	500	1388	S1070	-5370	500
1209	S891	-2685	613	1269	S951	-3585	613	1329	S1011	-4485	613	1389	S1071	-5385	613
1210	S892	-2700	500	1270	S952	-3600	500	1330	S1012	-4500	500	1390	S1072	-5400	500
1211	S893	-2715	613	1271	S953	-3615	613	1331	S1013	-4515	613	1391	S1073	-5415	613
1212	S894	-2730	500	1272	S954	-3630	500	1332	S1014	-4530	500	1392	S1074	-5430	500
1213	S895	-2745	613	1273	S955	-3645	613	1333	S1015	-4545	613	1393	S1075	-5445	613
1214	S896	-2760	500	1274	S956	-3660	500	1334	S1016	-4560	500	1394	S1076	-5460	500
1215	S897	-2775	613	1275	S957	-3675	613	1335	S1017	-4575	613	1395	S1077	-5475	613
1216	S898	-2790	500	1276	S958	-3690	500	1336	S1018	-4590	500	1396	S1078	-5490	500
1217	S899	-2805	613	1277	S959	-3705	613	1337	S1019	-4605	613	1397	S1079	-5505	613
1218	S900	-2820	500	1278	S960	-3720	500	1338	S1020	-4620	500	1398	S1080	-5520	500
1219	S901	-2835	613	1279	S961	-3735	613	1339	S1021	-4635	613	1399	S1081	-5535	613
1220	S902	-2850	500	1280	S962	-3750	500	1340	S1022	-4650	500	1400	S1082	-5550	500
1221	S903	-2865	613	1281	S963	-3765	613	1341	S1023	-4665	613	1401	S1083	-5565	613
1222	S904	-2880	500	1282	S964	-3780	500	1342	S1024	-4680	500	1402	S1084	-5580	500
1223	S905	-2895	613	1283	S965	-3795	613	1343	S1025	-4695	613	1403	S1085	-5595	613
1224	S906	-2910	500	1284	S966	-3810	500	1344	S1026	-4710	500	1404	S1086	-5610	500
1225	S907	-2925	613	1285	S967	-3825	613	1345	S1027	-4725	613	1405	S1087	-5625	613
1226	S908	-2940	500	1286	S968	-3840	500	1346	S1028	-4740	500	1406	S1088	-5640	500
1227	S909	-2955	613	1287	S969	-3855	613	1347	S1029	-4755	613	1407	S1089	-5655	613
1228	S910	-2970	500	1288	S970	-3870	500	1348	S1030	-4770	500	1408	S1090	-5670	500
1229	S911	-2985	613	1289	S971	-3885	613	1349	S1031	-4785	613	1409	S1091	-5685	613
1230	S912	-3000	500	1290	S972	-3900	500	1350	S1032	-4800	500	1410	S1092	-5700	500
1231	S913	-3015	613	1291	S973	-3915	613	1351	S1033	-4815	613	1411	S1093	-5715	613
1232	S914	-3030	500	1292	S974	-3930	500	1352	S1034	-4830	500	1412	S1094	-5730	500
1233	S915	-3045	613	1293	S975	-3945	613	1353	S1035	-4845	613	1413	S1095	-5745	613
1234	S916	-3060	500	1294	S976	-3960	500	1354	S1036	-4860	500	1414	S1096	-5760	500
1235	S917	-3075	613	1295	S977	-3975	613	1355	S1037	-4875	613	1415	S1097	-5775	613
1236	S918	-3090	500	1296	S978	-3990	500	1356	S1038	-4890	500	1416	S1098	-5790	500
1237	S919	-3105	613	1297	S979	-4005	613	1357	S1039	-4905	613	1417	S1099	-5805	613
1238	S920	-3120	500	1298	S980	-4020	500	1358	S1040	-4920	500	1418	S1100	-5820	500
1239	S921	-3135	613	1299	S981	-4035	613	1359	S1041	-4935	613	1419	S1101	-5835	613
1240	S922	-3150	500	1300	S982	-4050	500	1360	S1042	-4950	500	1420	S1102	-5850	500
1241	S923	-3165	613	1301	S983	-4065	613	1361	S1043	-4965	613	1421	S1103	-5865	613
1242	S924	-3180	500	1302	S984	-4080	500	1362	S1044	-4980	500	1422	S1104	-5880	500
1243	S925	-3195	613	1303	S985	-4095	613	1363	S1045	-4995	613	1423	S1105	-5895	613
1244	S926	-3210	500	1304	S986	-4110	500	1364	S1046	-5010	500	1424	S1106	-5910	500
1245	S927	-3225	613	1305	S987	-4125	613	1365	S1047	-5025	613	1425	S1107	-5925	613
1246	S928	-3240	500	1306	S988	-4140	500	1366	S1048	-5040	500	1426	S1108	-5940	500
1247	S929	-3255	613	1307	S989	-4155	613	1367	S1049	-5055	613	1427	S1109	-5955	613
1248	S930	-3270	500	1308	S990	-4170	500	1368	S1050	-5070	500	1428	S1110	-5970	500
1249	S931	-3285	613	1309	S991	-4185	613	1369	S1051	-5085	613	1429	S1111	-5985	613
1250	S932	-3300	500	1310	S992	-4200	500	1370	S1052	-5100	500	1430	S1112	-6000	500
1251	S933	-3315	613	1311	S993	-4215	613	1371	S1053	-5115	613	1431	S1113	-6015	613
1252	S934	-3330	500	1312	S994	-4230	500	1372	S1054	-5130	500	1432	S1114	-6030	500
1253	S935	-3345	613	1313	S995	-4245	613	1373	S1055	-5145	613	1433	S1115	-6045	613
1254	S936	-3360	500	1314	S996	-4260	500	1374	S1056	-5160	500	1434	S1116	-6060	500
1255	S937	-3375	613	1315	S997	-4275	613	1375	S1057	-5175	613	1435	S1117	-6075	613
1256	S938	-3390	500	1316	S998	-4290	500	1376	S1058	-5190	500	1436	S1118	-6090	500
1257	S939	-3405	613	1317	S999	-4305	613	1377	S1059	-5205	613	1437	S1119	-6105	613
1258	S940	-3420	500	1318	S1000	-4320	500	1378	S1060	-5220	500	1438	S1120	-6120	500
1259	S941	-3435	613	1319	S1001	-4335	613	1379	S1061	-5235	613	1439	S1121	-6135	613
1260	S942	-3450	500	1320	S1002	-4350	500	1380	S1062	-5250	500	1440	S1122	-6150	500

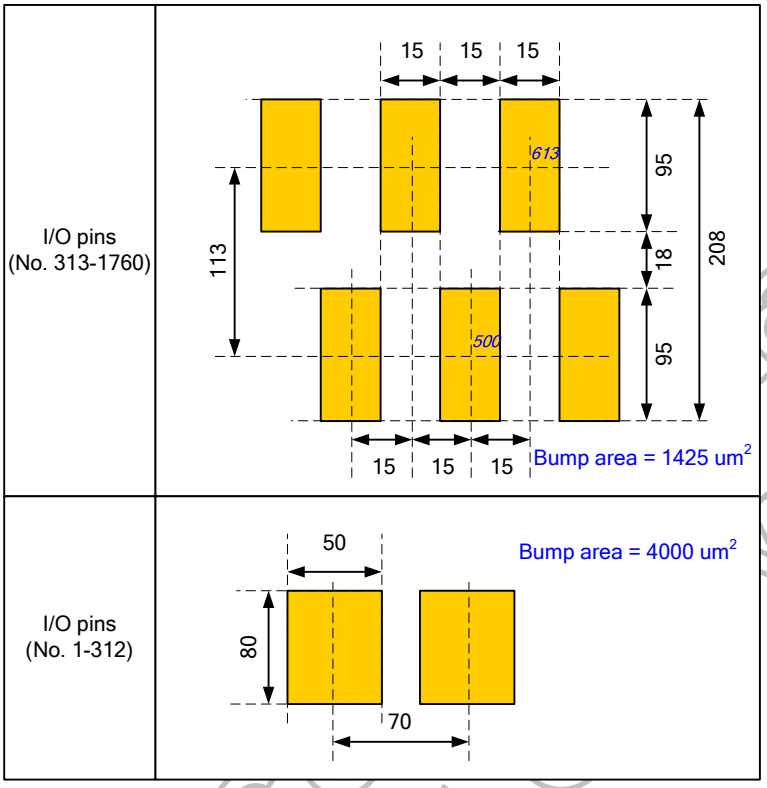
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1441	S1123	-6165	613	1501	S1183	-7065	613	1561	S1243	-7965	613	1621	S1303	-8865	613
1442	S1124	-6180	500	1502	S1184	-7080	500	1562	S1244	-7980	500	1622	S1304	-8880	500
1443	S1125	-6195	613	1503	S1185	-7095	613	1563	S1245	-7995	613	1623	S1305	-8895	613
1444	S1126	-6210	500	1504	S1186	-7110	500	1564	S1246	-8010	500	1624	S1306	-8910	500
1445	S1127	-6225	613	1505	S1187	-7125	613	1565	S1247	-8025	613	1625	S1307	-8925	613
1446	S1128	-6240	500	1506	S1188	-7140	500	1566	S1248	-8040	500	1626	S1308	-8940	500
1447	S1129	-6255	613	1507	S1189	-7155	613	1567	S1249	-8055	613	1627	S1309	-8955	613
1448	S1130	-6270	500	1508	S1190	-7170	500	1568	S1250	-8070	500	1628	S1310	-8970	500
1449	S1131	-6285	613	1509	S1191	-7185	613	1569	S1251	-8085	613	1629	S1311	-8985	613
1450	S1132	-6300	500	1510	S1192	-7200	500	1570	S1252	-8100	500	1630	S1312	-9000	500
1451	S1133	-6315	613	1511	S1193	-7215	613	1571	S1253	-8115	613	1631	S1313	-9015	613
1452	S1134	-6330	500	1512	S1194	-7230	500	1572	S1254	-8130	500	1632	S1314	-9030	500
1453	S1135	-6345	613	1513	S1195	-7245	613	1573	S1255	-8145	613	1633	S1315	-9045	613
1454	S1136	-6360	500	1514	S1196	-7260	500	1574	S1256	-8160	500	1634	S1316	-9060	500
1455	S1137	-6375	613	1515	S1197	-7275	613	1575	S1257	-8175	613	1635	S1317	-9075	613
1456	S1138	-6390	500	1516	S1198	-7290	500	1576	S1258	-8190	500	1636	S1318	-9090	500
1457	S1139	-6405	613	1517	S1199	-7305	613	1577	S1259	-8205	613	1637	S1319	-9105	613
1458	S1140	-6420	500	1518	S1200	-7320	500	1578	S1260	-8220	500	1638	S1320	-9120	500
1459	S1141	-6435	613	1519	S1201	-7335	613	1579	S1261	-8235	613	1639	S1321	-9135	613
1460	S1142	-6450	500	1520	S1202	-7350	500	1580	S1262	-8250	500	1640	S1322	-9150	500
1461	S1143	-6465	613	1521	S1203	-7365	613	1581	S1263	-8265	613	1641	S1323	-9165	613
1462	S1144	-6480	500	1522	S1204	-7380	500	1582	S1264	-8280	500	1642	S1324	-9180	500
1463	S1145	-6495	613	1523	S1205	-7395	613	1583	S1265	-8295	613	1643	S1325	-9195	613
1464	S1146	-6510	500	1524	S1206	-7410	500	1584	S1266	-8310	500	1644	S1326	-9210	500
1465	S1147	-6525	613	1525	S1207	-7425	613	1585	S1267	-8325	613	1645	S1327	-9225	613
1466	S1148	-6540	500	1526	S1208	-7440	500	1586	S1268	-8340	500	1646	S1328	-9240	500
1467	S1149	-6555	613	1527	S1209	-7455	613	1587	S1269	-8355	613	1647	S1329	-9255	613
1468	S1150	-6570	500	1528	S1210	-7470	500	1588	S1270	-8370	500	1648	S1330	-9270	500
1469	S1151	-6585	613	1529	S1211	-7485	613	1589	S1271	-8385	613	1649	S1331	-9285	613
1470	S1152	-6600	500	1530	S1212	-7500	500	1590	S1272	-8400	500	1650	S1332	-9300	500
1471	S1153	-6615	613	1531	S1213	-7515	613	1591	S1273	-8415	613	1651	S1333	-9315	613
1472	S1154	-6630	500	1532	S1214	-7530	500	1592	S1274	-8430	500	1652	S1334	-9330	500
1473	S1155	-6645	613	1533	S1215	-7545	613	1593	S1275	-8445	613	1653	S1335	-9345	613
1474	S1156	-6660	500	1534	S1216	-7560	500	1594	S1276	-8460	500	1654	S1336	-9360	500
1475	S1157	-6675	613	1535	S1217	-7575	613	1595	S1277	-8475	613	1655	S1337	-9375	613
1476	S1158	-6690	500	1536	S1218	-7590	500	1596	S1278	-8490	500	1656	S1338	-9390	500
1477	S1159	-6705	613	1537	S1219	-7605	613	1597	S1279	-8505	613	1657	S1339	-9405	613
1478	S1160	-6720	500	1538	S1220	-7620	500	1598	S1280	-8520	500	1658	S1340	-9420	500
1479	S1161	-6735	613	1539	S1221	-7635	613	1599	S1281	-8535	613	1659	S1341	-9435	613
1480	S1162	-6750	500	1540	S1222	-7650	500	1600	S1282	-8550	500	1660	S1342	-9450	500
1481	S1163	-6765	613	1541	S1223	-7665	613	1601	S1283	-8565	613	1661	S1343	-9465	613
1482	S1164	-6780	500	1542	S1224	-7680	500	1602	S1284	-8580	500	1662	S1344	-9480	500
1483	S1165	-6795	613	1543	S1225	-7695	613	1603	S1285	-8595	613	1663	S1345	-9495	613
1484	S1166	-6810	500	1544	S1226	-7710	500	1604	S1286	-8610	500	1664	S1346	-9510	500
1485	S1167	-6825	613	1545	S1227	-7725	613	1605	S1287	-8625	613	1665	S1347	-9525	613
1486	S1168	-6840	500	1546	S1228	-7740	500	1606	S1288	-8640	500	1666	S1348	-9540	500
1487	S1169	-6855	613	1547	S1229	-7755	613	1607	S1289	-8655	613	1667	S1349	-9555	613
1488	S1170	-6870	500	1548	S1230	-7770	500	1608	S1290	-8670	500	1668	S1350	-9570	500
1489	S1171	-6885	613	1549	S1231	-7785	613	1609	S1291	-8685	613	1669	S1351	-9585	613
1490	S1172	-6900	500	1550	S1232	-7800	500	1610	S1292	-8700	500	1670	S1352	-9600	500
1491	S1173	-6915	613	1551	S1233	-7815	613	1611	S1293	-8715	613	1671	S1353	-9615	613
1492	S1174	-6930	500	1552	S1234	-7830	500	1612	S1294	-8730	500	1672	S1354	-9630	500
1493	S1175	-6945	613	1553	S1235	-7845	613	1613	S1295	-8745	613	1673	S1355	-9645	613
1494	S1176	-6960	500	1554	S1236	-7860	500	1614	S1296	-8760	500	1674	S1356	-9660	500
1495	S1177	-6975	613	1555	S1237	-7875	613	1615	S1297	-8775	613	1675	S1357	-9675	613
1496	S1178	-6990	500	1556	S1238	-7890	500	1616	S1298	-8790	500	1676	S1358	-9690	500
1497	S1179	-7005	613	1557	S1239	-7905	613	1617	S1299	-8805	613	1677	S1359	-9705	613
1498	S1180	-7020	500	1558	S1240	-7920	500	1618	S1300	-8820	500	1678	S1360	-9720	500
1499	S1181	-7035	613	1559	S1241	-7935	613	1619	S1301	-8835	613	1679	S1361	-9735	613
1500	S1182	-7050	500	1560	S1242	-7950	500	1620	S1302	-8850	500	1680	S1362	-9750	500

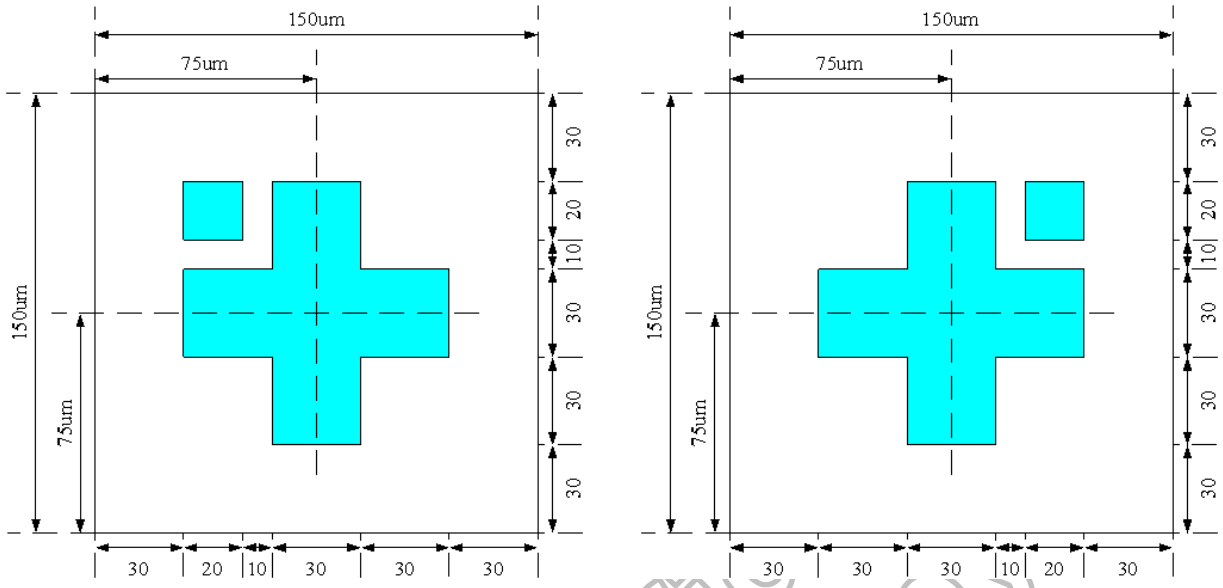
No.	Name	X	Y
1681	S1363	-9765	613
1682	S1364	-9780	500
1683	S1365	-9795	613
1684	S1366	-9810	500
1685	S1367	-9825	613
1686	S1368	-9840	500
1687	S1369	-9855	613
1688	S1370	-9870	500
1689	S1371	-9885	613
1690	S1372	-9900	500
1691	S1373	-9915	613
1692	S1374	-9930	500
1693	S1375	-9945	613
1694	S1376	-9960	500
1695	S1377	-9975	613
1696	S1378	-9990	500
1697	S1379	-10005	613
1698	S1380	-10020	500
1699	S1381	-10035	613
1700	S1382	-10050	500
1701	S1383	-10065	613
1702	S1384	-10080	500
1703	S1385	-10095	613
1704	S1386	-10110	500
1705	S1387	-10125	613
1706	S1388	-10140	500
1707	S1389	-10155	613
1708	S1390	-10170	500
1709	S1391	-10185	613
1710	S1392	-10200	500
1711	S1393	-10215	613
1712	S1394	-10230	500
1713	S1395	-10245	613
1714	S1396	-10260	500
1715	S1397	-10275	613
1716	S1398	-10290	500
1717	S1399	-10305	613
1718	S1400	-10320	500
1719	S1401	-10335	613
1720	S1402	-10350	500
1721	S1403	-10365	613
1722	S1404	-10380	500
1723	S1405	-10395	613
1724	S1406	-10410	500
1725	S1407	-10425	613
1726	S1408	-10440	500
1727	S1409	-10455	613
1728	S1410	-10470	500
1729	S1411	-10485	613
1730	S1412	-10500	500
1731	S1413	-10515	613
1732	S1414	-10530	500
1733	S1415	-10545	613
1734	S1416	-10560	500
1735	S1417	-10575	613
1736	S1418	-10590	500
1737	S1419	-10605	613
1738	S1420	-10620	500
1739	S1421	-10635	613
1740	S1422	-10650	500

No.	Name	X	Y
1741	S1423	-10665	613
1742	S1424	-10680	500
1743	S1425	-10695	613
1744	S1426	-10710	500
1745	S1427	-10725	613
1746	S1428	-10740	500
1747	S1429	-10755	613
1748	S1430	-10770	500
1749	S1431	-10785	613
1750	S1432	-10800	500
1751	S1433	-10815	613
1752	S1434	-10830	500
1753	S1435	-10845	613
1754	S1436	-10860	500
1755	S1437	-10875	613
1756	S1438	-10890	500
1757	S1439	-10905	613
1758	S1440	-10920	500
1759	S1441 (for Zig-Zag)	-10935	613
1760	Dummy17	-10950	500

Alignment mark	X	Y
A1	-11060	600
A2	11060	600

3.4.1 Bump arrangement





4. Interface

4.1 System interface

The HX8369-A02 supports MDDI (Mobile Display Digital Interface) and MIPI interfaces: DBI (Display Bus Interface), DPI (Display Pixel Interface), DSI (Display Serial Interface). Where DBI supports (16-/9-/8-bit interface) Parallel Interface (Type A, Type B) and Serial interface (Type C). The interface mode can be selected by BS3-0 pins setting as show in Table 4.1.

BS3	BS2	BS1	BS0	Interface	Display data	Display mode
0	0	0	0	DBI TYPE-A 8-bit (CLK-E)	GRAM	Type 1
0	0	0	1	DBI TYPE-A 9-bit (CLK-E)	GRAM	Type 1
0	0	1	0	DBI TYPE-A 16-bit (CLK-E)	GRAM	Type 1
0	0	1	1	DBI TYPE-A 18-bit (CLK-E)	GRAM	Type 1
0	1	0	0	DBI TYPE-B 8-bit	GRAM	Type 1
0	1	0	1	DBI TYPE-B 9-bit	GRAM	Type 1
0	1	1	0	DBI TYPE-B 16-bit	GRAM	Type 1
0	1	1	1	DBI TYPE-B 18-bit	GRAM	Type 1
1	0	0	0	DSI (Command mode)	GRAM	Type 1
1	0	0	1	MDDI (3-wire serial + MDDI + external R)	GRAM	-
1	0	1	0	DBI TYPE-B 24-bit	GRAM	Type 1
1	0	1	1	MDDI (3-wire serial + MDDI + internal R)	GRAM	-
1	1	0	0	DSI (Video mode)	DSI I/F	Type 3
1	1	0	1	DPI / DBI TYPE-C Option 1	DPI / GRAM	Type 3
1	1	1	0	DPI / DBI TYPE-C Option 2	DPI / GRAM	Type 3
1	1	1	1	DPI / DBI TYPE-C Option 3	DPI / GRAM	Type 3

Table 4.1: Interface selection

The HX8369-A02 includes an index register (IR), which is stored the index data of internal control register and GRAM. When DCX="L", the command via DBI interface write into register. When DCX="H", GRAM data via R2Ch register can be written through data bus. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM.

When data is read from the GRAM to the MPU, it is first read from GRAM to the read-data latch and then data is read to MPU through the read-data latch in next read operation. Therefore, the read data in data bus in first read operation is invalid, and the read data in data bus in second and the following read operation is valid.

Interface	RDX_E	WRX_DCX	DCX_SCL	D23–D0 or other input pin
DBI Type C 3-wire serial interface + DPI interface	Unused	Unused	SCL	DB23–DB0: 24-bit data bus DB21–DB16, DB13-DB8, DB5-DB0: 18-bit data bus DB21–DB17, DB13-DB8, DB5-DB1: 16-bit data bus SDI/SDO
DBI Type A 8-bit parallel	E	RW	DCX	DB23–DB8: Unused, DB7–DB0: 8-bit data bus
DBI Type A 9-bit parallel	E	RW	DCX	DB23–DB9: Unused, DB8–DB0: 9-bit data bus
DBI Type A 16-bit parallel	E	RW	DCX	DB23–DB16: Unused, DB15–DB0: 16-bit data bus
DBI Type A 18-bit parallel	E	RW	DCX	DB23–DB18: Unused, DB17–DB0: 18-bit data bus
DBI Type C 4-wire serial interface + DPI interface	Unused	DCX	SCL	DB23–DB0: 24-bit data bus DB21–DB16, DB13-DB8, DB5-DB0: 18-bit data bus DB21–DB17, DB13-DB8, DB5-DB1: 16-bit data bus SDI/SDO
DBI Type B 8-bit parallel	RDX	WRX	DCX	DB23–DB8: Unused, D7–D0: 8-bit data bus
DBI Type B 9-bit parallel	RDX	WRX	DCX	DB23–DB9: Unused, DB8–DB0: 9-bit data bus
DBI Type B 16-bit parallel	RDX	WRX	DCX	DB23–DB16: Unused, DB15–DB0: 16-bit data bus
DBI Type B 18-bit parallel	RDX	WRX	DCX	DB23–DB18: Unused, DB17–DB0: 18-bit data bus
DBI Type B 24-bit parallel	RDX	WRX	DCX	DB23–DB0: 24-bit data bus
DSI (Display Serial Interface)	Unused	Unused	Unused	DSI_CP, DSI_CN, DSI_D0P, DSI_D0N, DSI_D1P, DSI_D1N,
MDDI (Mobile Display Digital Interface)	Unused	Unused	Unused	MDDI_STBP, MDDI_STBN, MDDI_D0P, MDDI_D0N, MDDI_D1P, MDDI_D1N

Table 4.2: Pin connection based on different interface

4.1.1 MIPI DBI-A / DBI-B interface

The selection of DBI interface is by BS3 pin. When this pin is low state (VSSD), the interface is use DBI system. And use BS2 to BS0 pins to selsect DBI interfacr mode. The parallel interface timing diagram is described in Figure 4.1 to Figure 4.4.

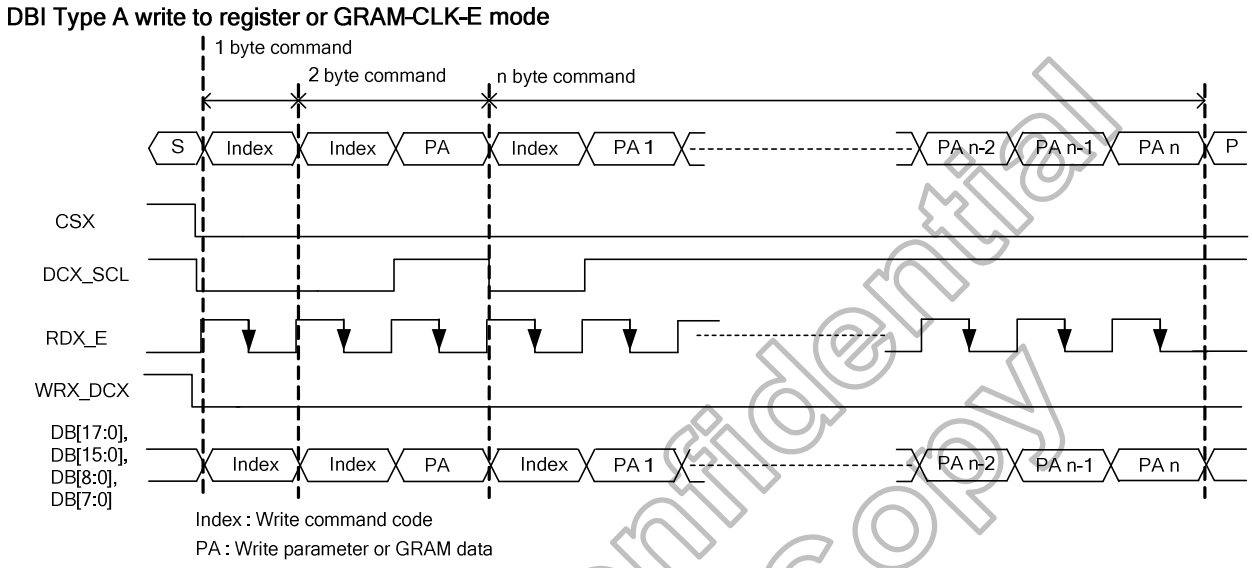


Figure 4.1: DBI-A system interface protocol, write to register or GRAM

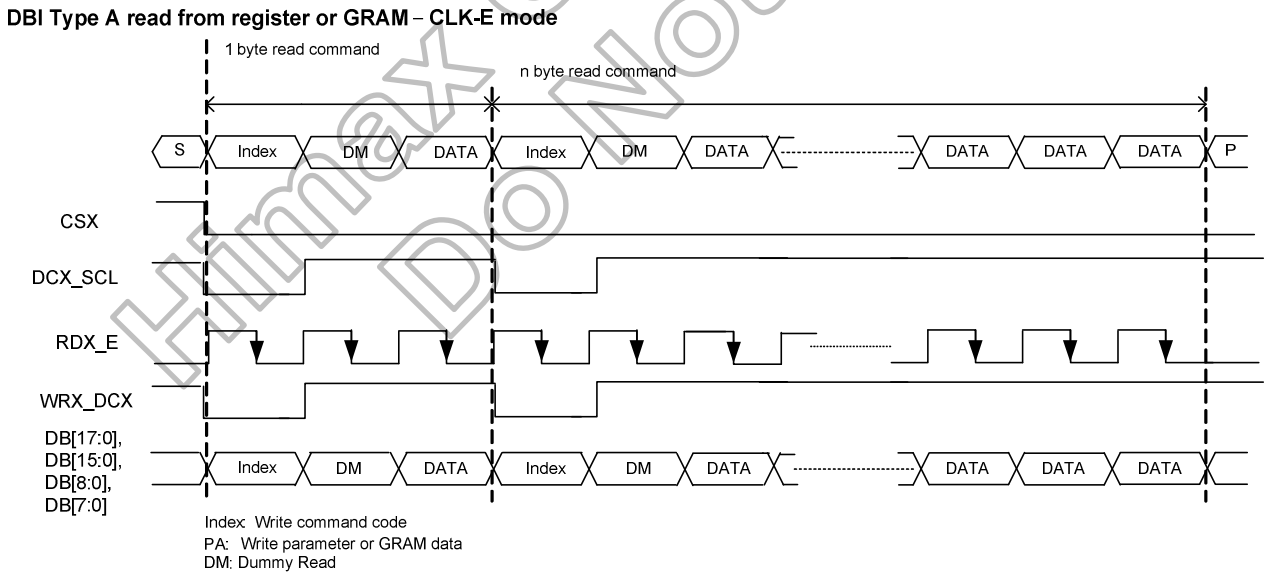


Figure 4.2: DBI-A system interface protocol, read from register or GRAM

DBI Type B write to register or GRAM

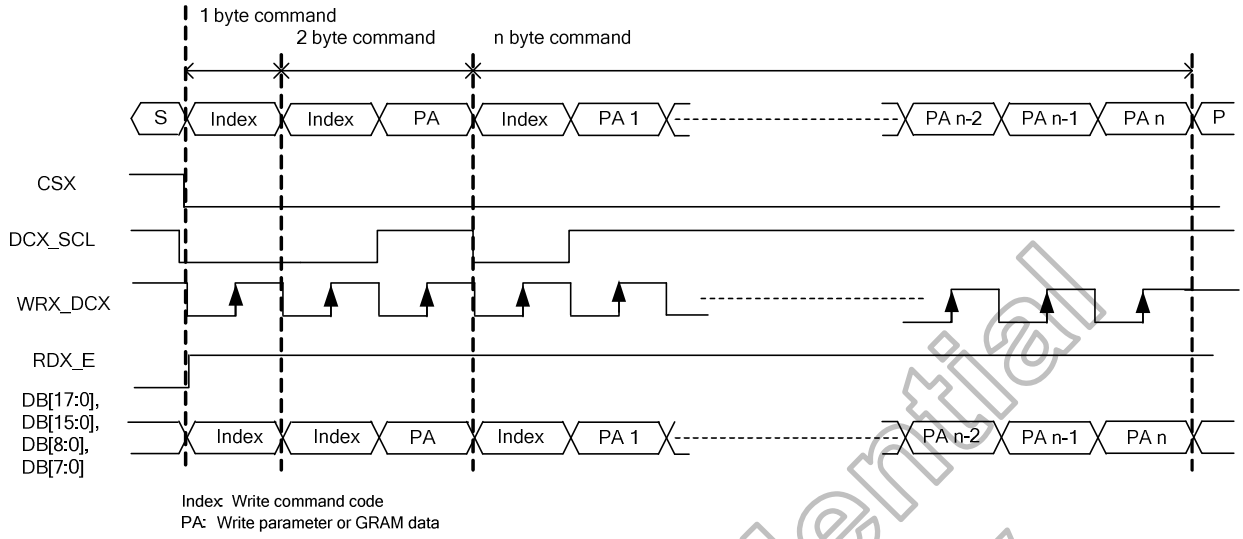


Figure 4.3: DBI-B system interface protocol, write to register or GRAM

DBI Type B read from register or GRAM

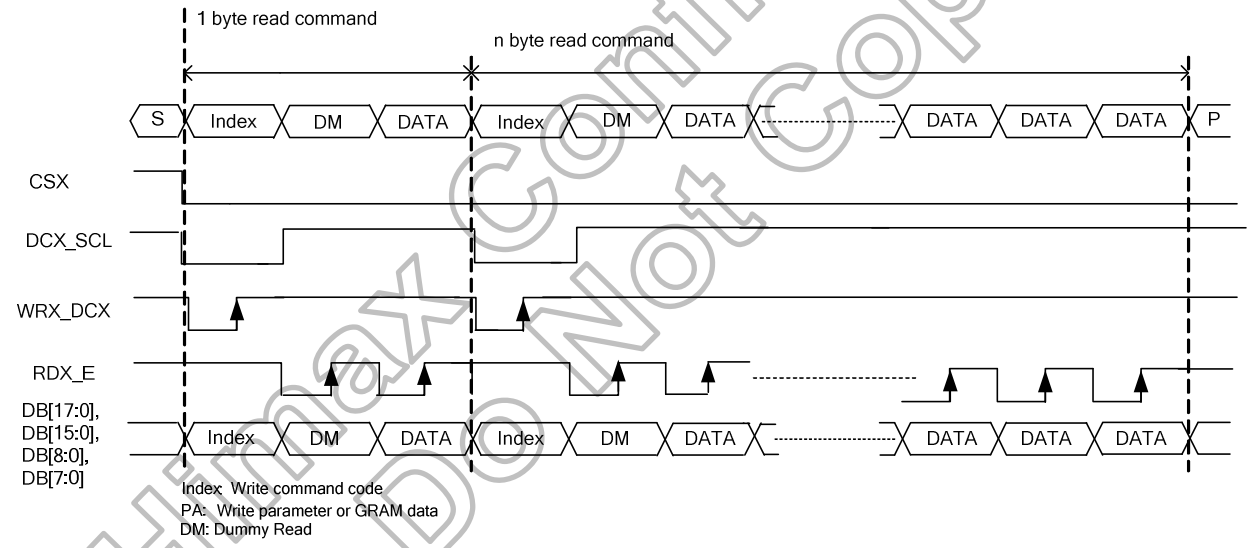


Figure 4.4: DBI-B system interface protocol, read from register or GRAM

4.1.1.1 24-bit parallel bus system interface

The DBI-B system 24-bit bus parallel data transfer can be used by setting “BS3-0” pins to “1010”. The Figure 4.5 is the example of interface with 18-bit DBI-A / DBI-B microcomputer system interface.

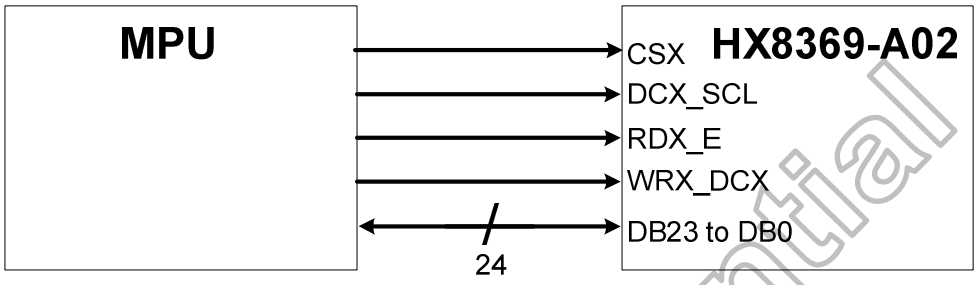


Figure 4.5 Example of DBI-B system 18-bit parallel bus interface

There are one type data format to write display data at 24-bit bus Interface. See Figure 4.6.

16.7M Color Data	DCX	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																								-
1st write	1	R17	R16	R15	R14	R13	R12	R11	R10	G17	G16	G15	G14	G13	G12	G11	G10	B17	B16	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	R27	R26	R15	R24	R23	R22	R21	R20	G17	G26	G25	G24	G23	G22	G21	G20	B27	B26	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

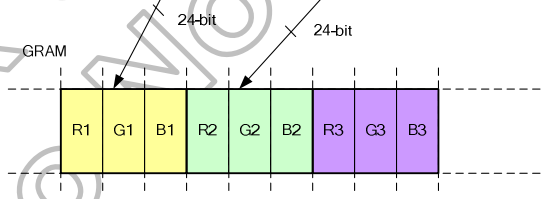


Figure 4.6: Write data for RGB 8-8-8 (16.7M colours) bit Input in 24-bit parallel interface

4.1.1.2 18-bit parallel bus system interface

The DBI-A system 18-bit bus parallel data transfer can be used by setting “BS3-0” pins to “0011”. And the DBI-B system 18-bit bus parallel data transfer can be used by setting “BS3-0”pins to “0111”. The Figure 4.7 is the example of interface with 18-bit DBI-A / DBI-B microcomputer system interface.

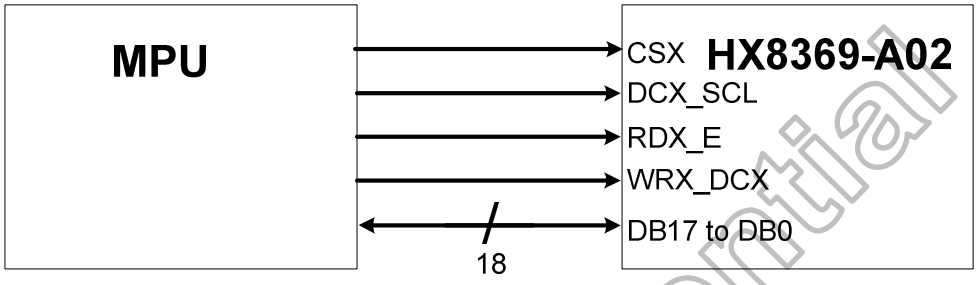


Figure 4.7: Example of DBI-A- / DBI-B system 18-bit parallel bus interface

There are three types data format to write display data at 18-bit bus Interface. See Figure 4.8 to Figure 4.10. Under this type, the data format can select as 16- / 18- / 24-bit by register R3Ah. (set_pixel_format)

65k Color Data	DCX	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																		-
1st write	1	x	x	R14	R13	R12	R11	R10	G15	G14	G13	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	x	x	R24	R23	R22	R21	R20	G25	G24	G23	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

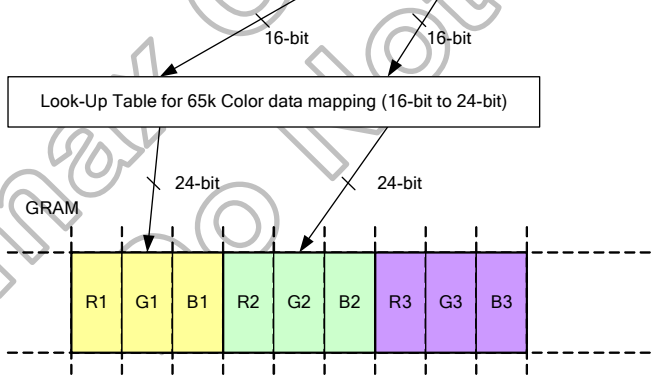


Figure 4.8: Write data for RGB 5-6-5 (65k colours) bit input in 18-bit parallel interface

262k Color Data	DCX	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																		-
1st write	1	R15	R14	R13	R12	R11	R10	G15	G14	G13	G12	G11	G10	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	R25	R24	R23	R22	R21	R20	G25	G24	G23	G22	G21	G20	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

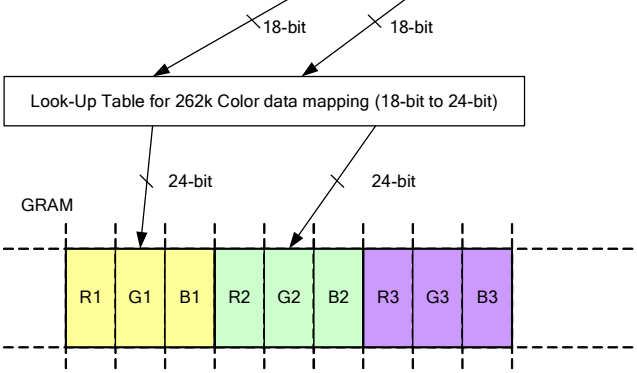
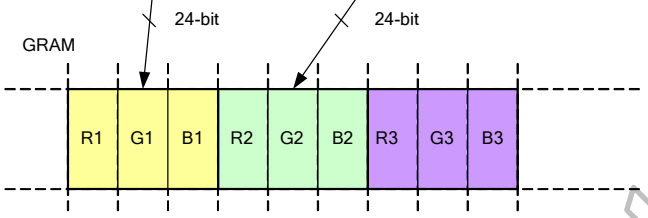
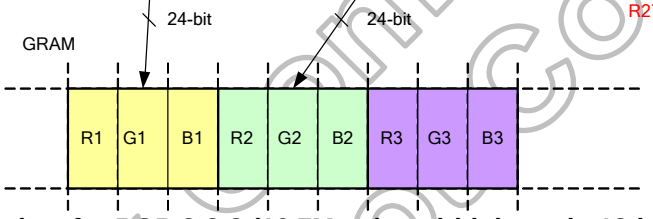


Figure 4.9: Write data for RGB 6-6-6(262k colours) bit input in 18-bit parallel interface

16.7M Color Data	DCX	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																		-
1st write	1	R17	R16	R15	R14	R13	R12	R11	R10	x	x	G17	G16	G15	G14	G13	G12	G11	G10	1st pixel (R1/G1/B1)
2nd write	1	B17	B16	B15	B14	B13	B12	B11	B10	x	x	R27	R26	R25	R24	R23	R22	R21	R20	x
3rd write	1	G27	G26	G25	G24	G23	G22	G21	G20	x	x	B27	B26	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)



16.7M Color Data	DCX	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																		-
1st write	1	R17	R16	R15	R14	R13	R12	R11	R10	x	x	G17	G16	G15	G14	G13	G12	G11	G10	1st pixel (R1/G1/B1)
2nd write	1	B17	B16	B15	B14	B13	B12	B11	B10	x	x	R27	R26	R25	R24	R23	R22	R21	R20	-
-	0	The other command																		-
MEMWR	0	GRAM Write command code																		-
1st write	1	R27	R26	R25	R24	R23	R22	R21	R20	x	x	G27	G26	G25	G24	G23	G22	G21	G20	2nd pixel (R2/G2/B2)
2nd write	1	B27	B26	B25	B24	B23	B22	B21	B20	x	x	R37	R36	R35	R34	R33	R32	R31	R30	-
3rd write	1	G37	G36	G35	G34	G33	G32	G31	G30	x	x	B37	B36	B35	B34	B33	B32	B31	B30	3rd pixel (R3/G3/B3)



R27 ~ R20 will be neglected and are not used

Figure 4.10: Write data for RGB 8-8-8 (16.7M colours) bit input in 18-bit parallel interface

4.1.1.3 16-bit parallel bus system interface

The DBI-A system 16-bit bus parallel data transfer can be used by setting “BS3-0” pins to “0010”. And the DBI-B system 16-bit bus parallel data transfer can be used by setting “BS3-0” pins to “0110”. The Figure 4.11 is the example of interface with 16-bit DBI-A / DBI-B microcomputer system interface.

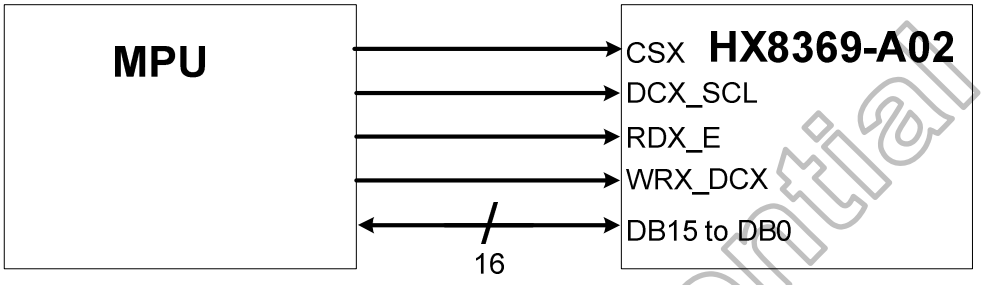


Figure 4.11: Example of DBI-A- / DBI-B system 16-bit bus interface

There are three types data format to write display data at 16-bit bus Interface. See Figure 4.12 to Figure 4. 14. Under this type, the data format can select as 16- / 18- / 24-bit by register R3Ah. (set_pixel_format)

65k Color Data	DCX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																-
1st write	1	R14	R13	R12	R11	R10	G15	G14	G13	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	R24	R23	R22	R21	R20	G25	G24	G23	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

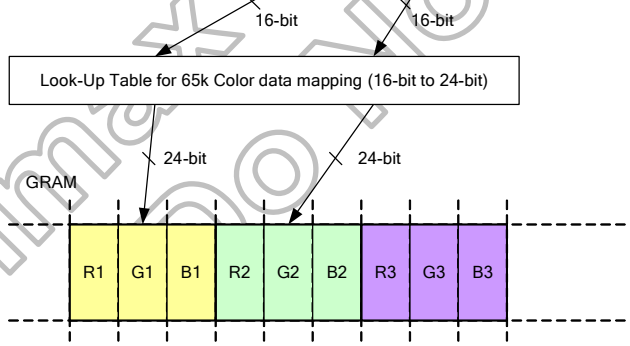


Figure 4.12: Write data for RGB 5-6-5 (65k colours) bit input in 16-bit parallel interface

262K Color Data	DCX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																-
1st write	1	R15	R14	R13	R12	R11	R10	x	x	G15	G14	G13	G12	G11	G10	x	x	1st pixel (R1/G1/B1)
2nd write	1	B15	B14	B13	B12	B11	B10	x	x	R25	R24	R23	R22	R21	R20	x	x	-
3rd write	1	G25	G24	G23	G22	G21	G20	x	x	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

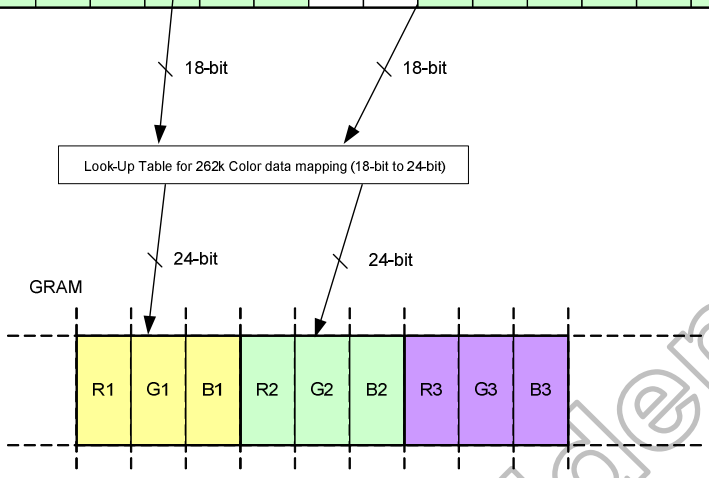


Figure 4.13: Write data for RGB 6-6-6 (262k colours) bit input in 16-bit parallel interface

16.7M Color Data	DCX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code																-
1st write	1	R17	R16	R15	R14	R13	R12	R11	R10	G17	G16	G15	G14	G13	G12	G11	G10	1st pixel (R1/G1/B1)
2nd write	1	B17	B16	B15	B14	B13	B12	B11	B10	R27	R26	R25	R24	R23	R22	R21	R20	-
3rd write	1	G27	G26	G25	G24	G23	G22	G21	G20	B27	B26	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

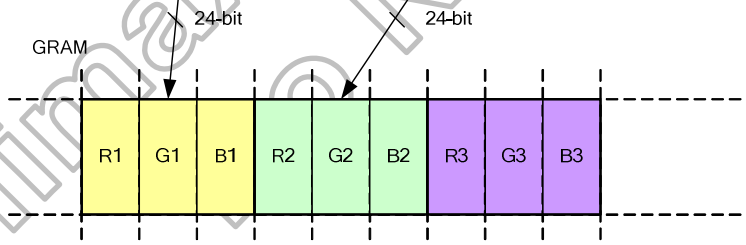


Figure 4.14: Write data for RGB 8-8-8-bit (16.7M colours) input in 16-bit parallel interface

4.1.1.4 9-bit parallel bus system interface

The DBI-A system 9-bit bus parallel data transfer can be used by setting “BS3-0” pins to “0001”. And the DBI-B system 9-bit bus parallel data transfer can be used by setting “BS3-0” pins to “0101”. The Figure 4.15 is the example of interface with 9-bit DBI-A / DBI-B microcomputer system interface.

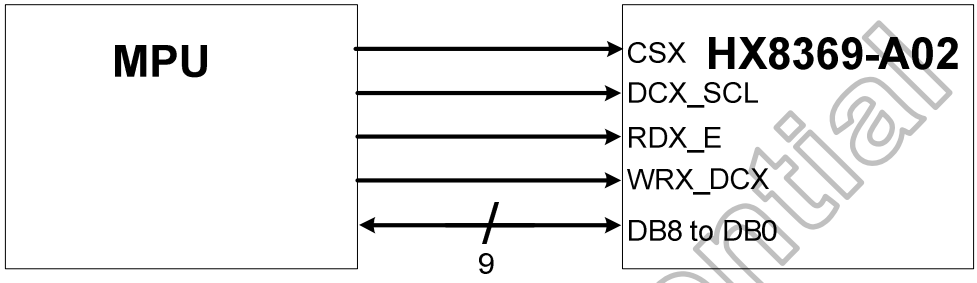


Figure 4.15: Example of DBI-A- / DBI-B- system 9-bit bus interface

There are three types data format to write display data at 9-bit bus Interface. See Figure 4.16 to Figure 4. 18. Under this type, the data format can select as 16-/18-/ 24-bit by register R3Ah. (set_pixel_format)

65k Color Data	DCX	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code									-
1st write	1	x	R14	R13	R12	R11	R10	G15	G14	G13	-
2nd write	1	x	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
3rd write	1	x	R24	R23	R22	R21	R20	G25	G24	G23	-
4th write	1	x	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

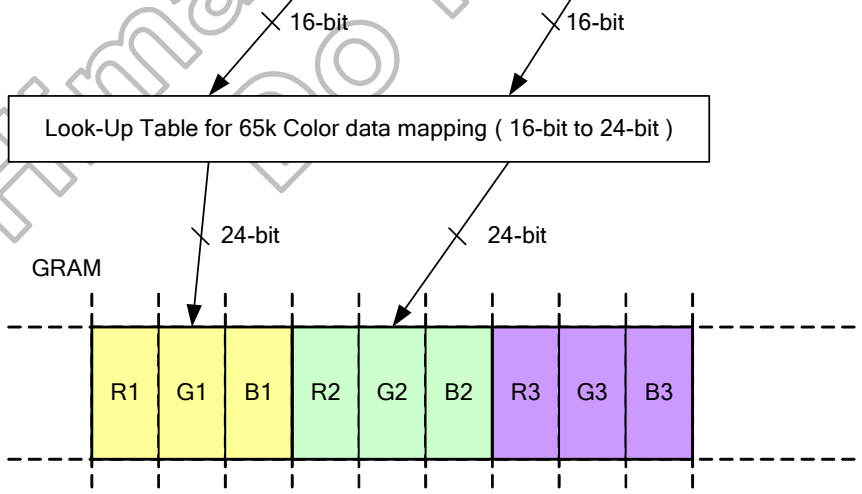


Figure 4.16: Write data for RGB 5-6-5(65k colours) bit input in 9-bit parallel interface

262k Color Data	DCX	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code									-
1st write	1	R15	R14	R13	R12	R11	R10	G15	G14	G13	-
2nd write	1	G12	G11	G10	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
3rd write	1	R25	R24	R23	R22	R21	R20	G25	G24	G23	-
4th write	1	G22	G21	G20	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

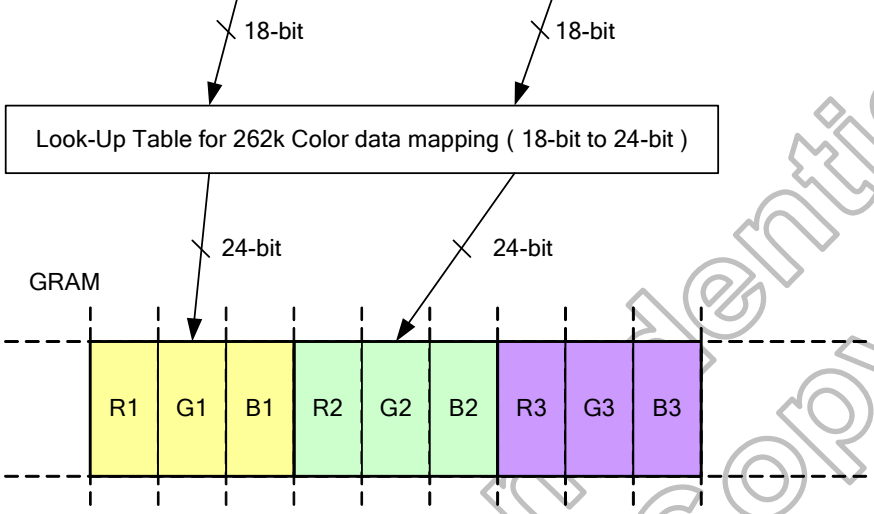


Figure 4.17: Write data for RGB 6-6-6-bit (262k colours) input in 9-bit parallel interface

16.7M Color Data	DCX	D8	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code									-
1st write	1	R17	R16	R15	R14	R13	R12	R11	R10	x	-
2nd write	1	G17	G16	G15	G14	G13	G12	G11	G10	x	-
3rd write	1	B17	B16	B15	B14	B13	B12	B11	B10	x	1st pixel (R1/G1/B1)
4th write	1	R27	R26	R25	R24	R23	R22	R21	R20	x	-
5th write	1	G27	G26	G25	G24	G23	G22	G21	G20	x	-
6th write	1	B27	B26	B25	B24	B23	B22	B21	B20	x	2nd pixel (R2/G2/B2)

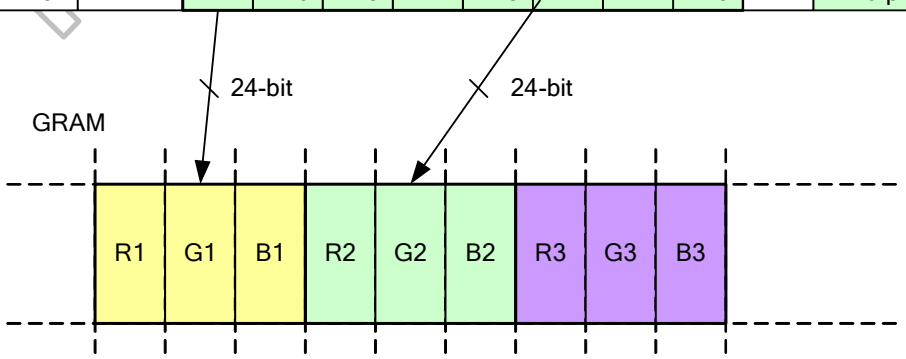


Figure 4.18: Write data for RGB 8-8-8-bit (16.7 M colours) input in 9-bit parallel interface

4.1.1.5 8-bit parallel bus system interface

The DBI-A system 8-bit bus parallel data transfer can be used by setting “BS3-0” pins to “0000”. And the DBI-B system 8-bit bus parallel data transfer can be used by setting “BS3-0” pins to “0100”. The Figure 4.19 is the example of interface with 8-bit DBI-A / DBI-B microcomputer system interface.

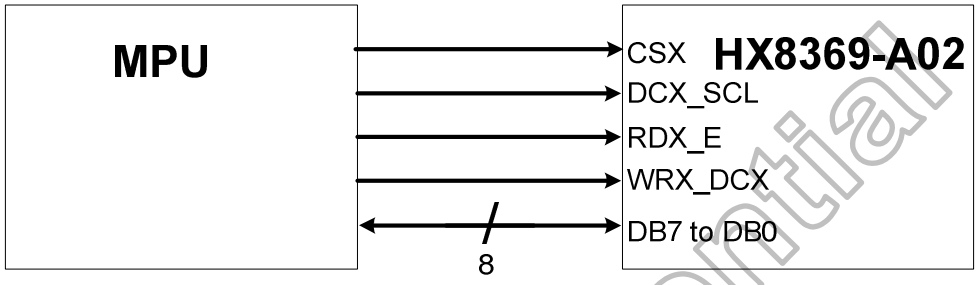


Figure 4.19: Example of DBI-A- / DBI-B-system 8-bit bus interface

There are three types data format to write display data at 8-bit bus Interface. See Figure 4. 20 to Figure 4. 22. Under this type, the data format can select as 16-/18-/ 24-bit by register R3Ah. (set_pixel_format)

65k Color Data	DCX	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R14	R13	R12	R11	R10	G15	G14	G13	-
2nd write	1	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
3rd write	1	R24	R23	R22	R21	R20	G25	G24	G23	-
4th write	1	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

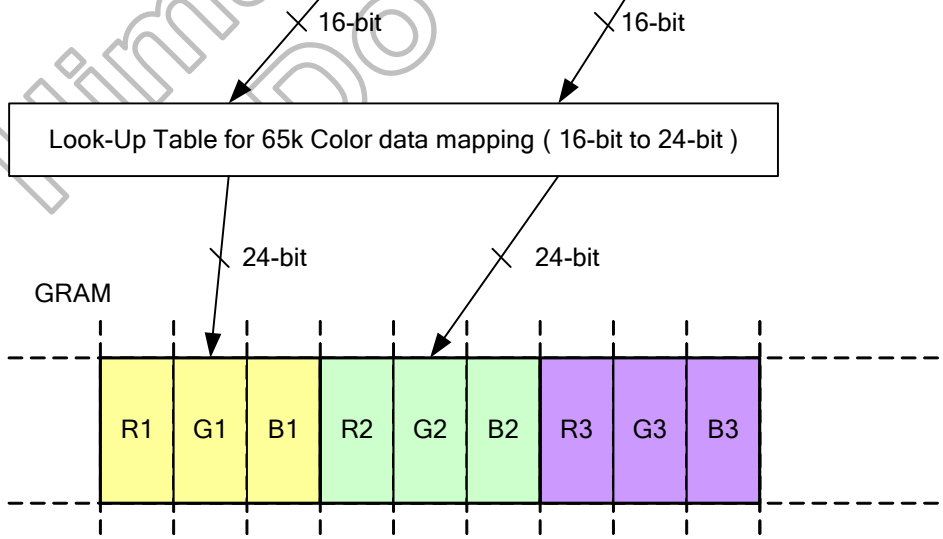


Figure 4.20: Write data for RGB 5-6-5 (65k colours) bit input in 8-bit parallel interface

262k Color Data	DCX	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R15	R14	R13	R12	R11	R10	x	x	-
2nd write	1	G15	G14	G13	G12	G11	G10	x	x	-
3rd write	1	B15	B14	B13	B12	B11	B10	x	x	1st pixel (R1/G1/B1)
4th write	1	R25	R24	R23	R22	R21	R20	x	x	-
5th write	1	G25	G24	G23	G22	G21	G20	x	x	-
6th write	1	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

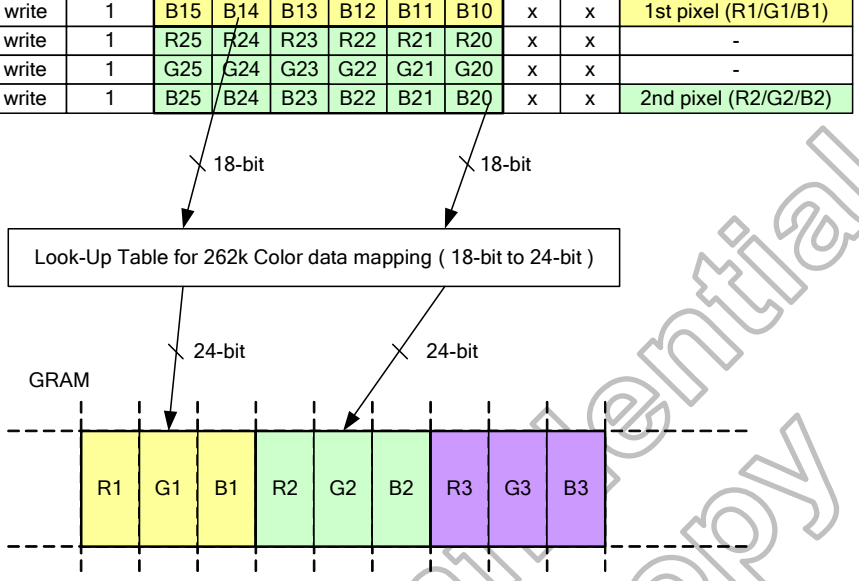


Figure 4.21: Write data for RGB 6-6-6-bit (262k colours) input in 8-bit parallel interface

16.7M Color Data	DCX	D7	D6	D5	D4	D3	D2	D1	D0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R17	R16	R15	R14	R13	R12	R11	R10	-
2nd write	1	G17	G16	G15	G14	G13	G12	G11	G10	-
3rd write	1	B17	B16	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
4th write	1	R27	R26	R25	R24	R23	R22	R21	R20	-
5th write	1	G27	G26	G25	G24	G23	G22	G21	G20	-
6th write	1	B27	B26	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

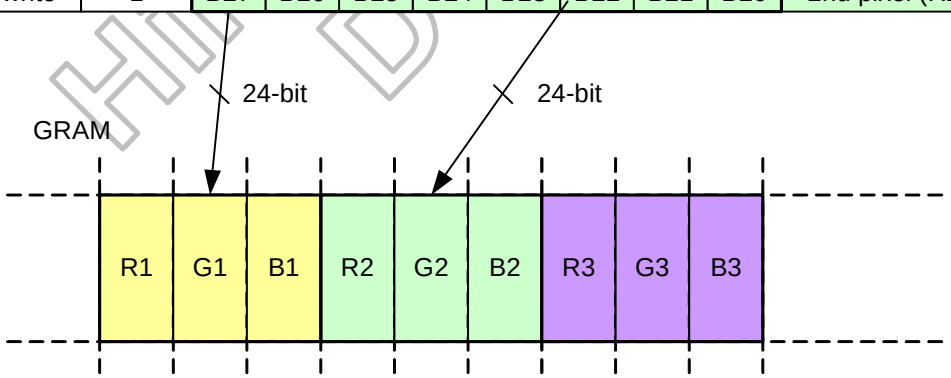


Figure 4.22: Write data for RGB 8-8-8-bit (16.7 M colours) input in 8-bit parallel interface

4.2 Serial data transfer interface (MIPI DBI-C)

The HX8369-A02 supports three type serial data transfer interface, the interface selection by setting BS3-0 pins. The BS3-0 set “1101” is select 3-wire option 1 serial bus. The BS3-0 set “1110” is select 3-wire option 2 serial bus. The BS3-0 is set “1111” when select 4-wire option 3 serial bus.

The 3-wire serial bus is use: chip select line (CSX), serial input/output data (SDI and SDO) and the serial transfer clock line (DCX_SCL).The 4-wire serial bus is use: chip select line (CSX), data/command select (WRX_DCX), serial input/output data (SDI and SDO) and the serial transfer clock line (DCX_SCL).

4.2.1.1 Serial data write mode

The 3-pin serial data packet contains a control bit D/CX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control signal D/CX is transferred by WRX_DCX pin. If DCX is low, the transmission byte is command byte. If D/CX is high, the transmission byte is stored in to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDI and SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. Where 3-wire serial write format include two types (8-/16-bit) is according command code.

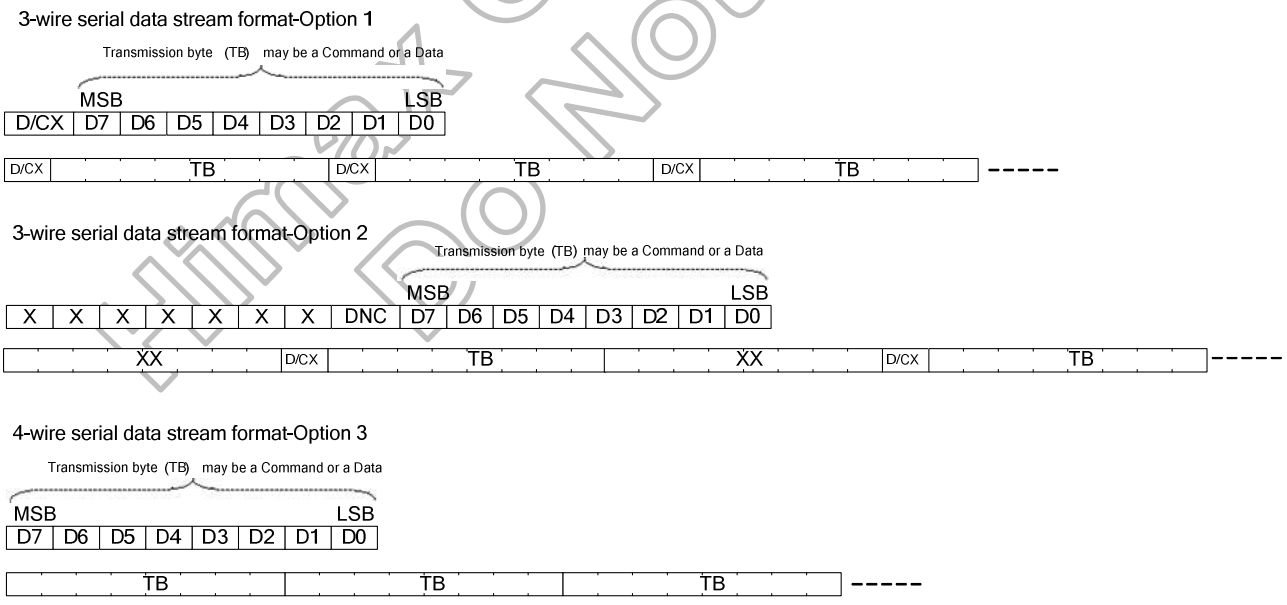
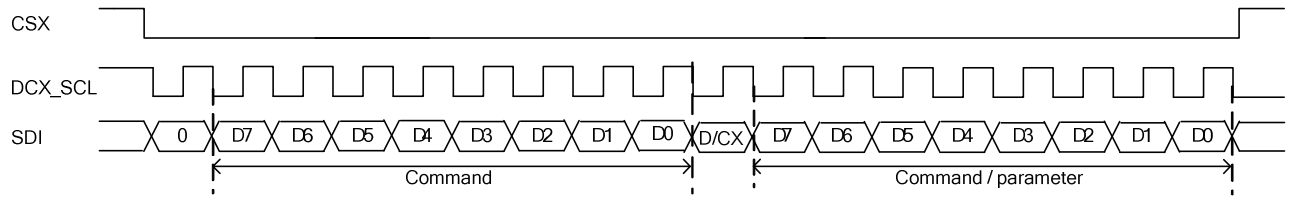
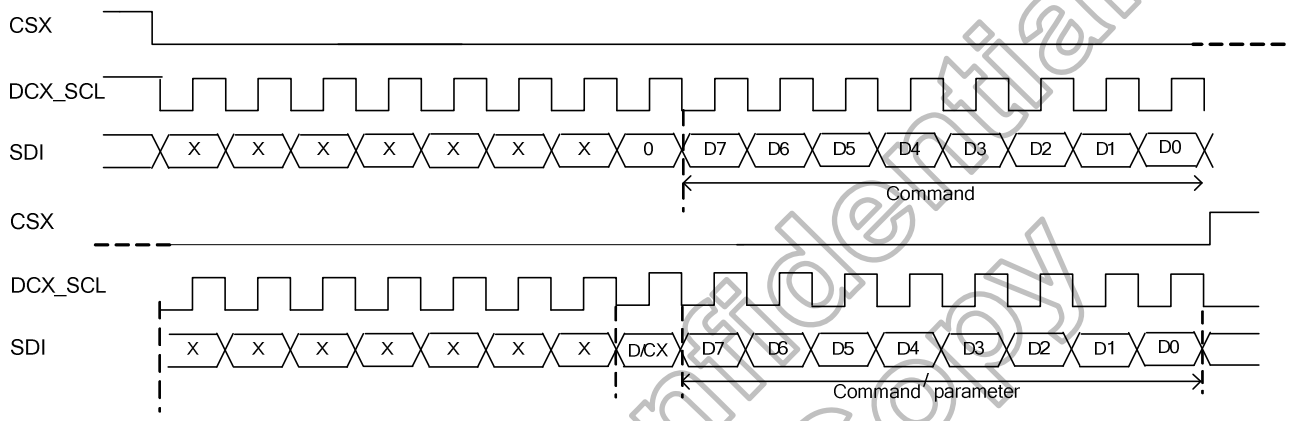


Figure 4.23: Serial data stream, write mode

DBI Type C: Interface protocol-Option 1 (3-wire)



DBI Type C: Interface protocol-Option 2 (3-wire)



DBI Type C: Interface protocol Option 3 (4-wire)

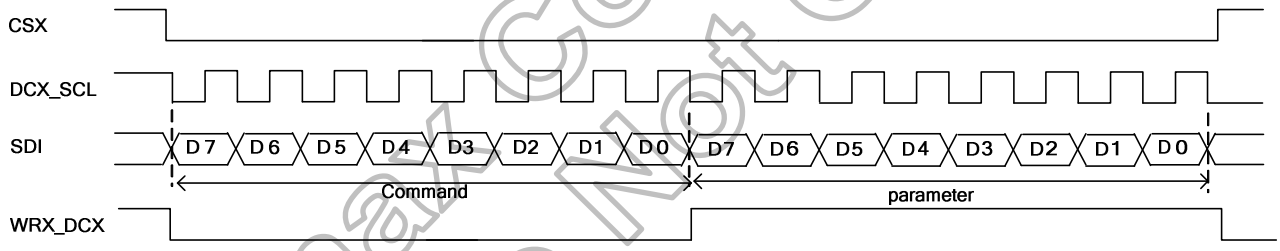


Figure 4.24: DBI Type C: Serial interface protocol 3-wire/4-wire, write mode

4.2.1.2 Serial data read mode

The micro-controller first has to send a command and then the following byte is transmitted in the opposite direction. The 3-wire serial read data format which just needs 8-bit.

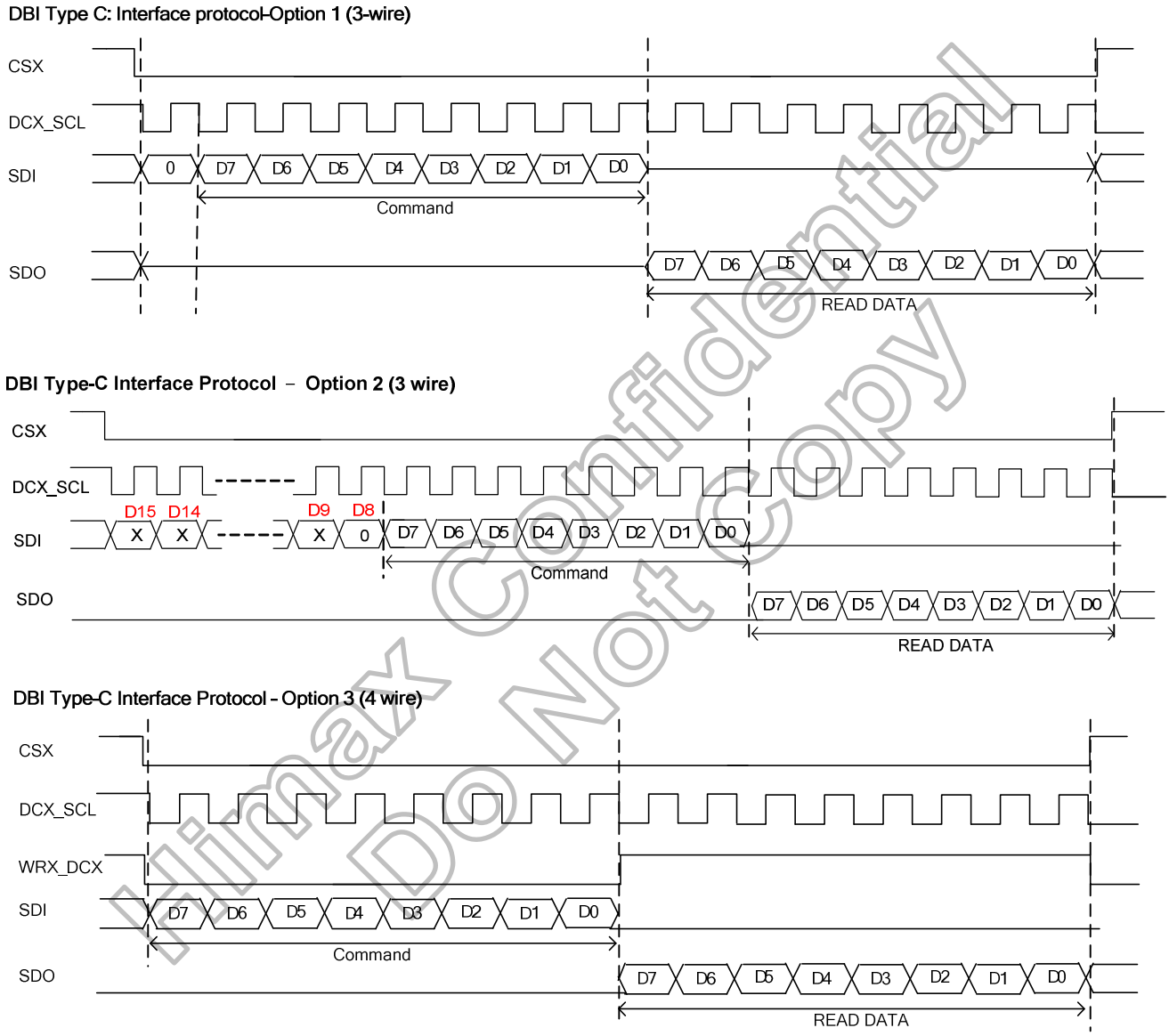


Figure 4.25: Type C:Serial interface protocol 3-wire/4-wire read mode

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

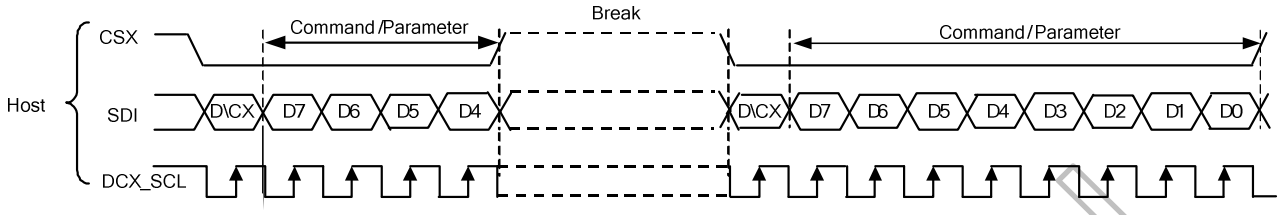
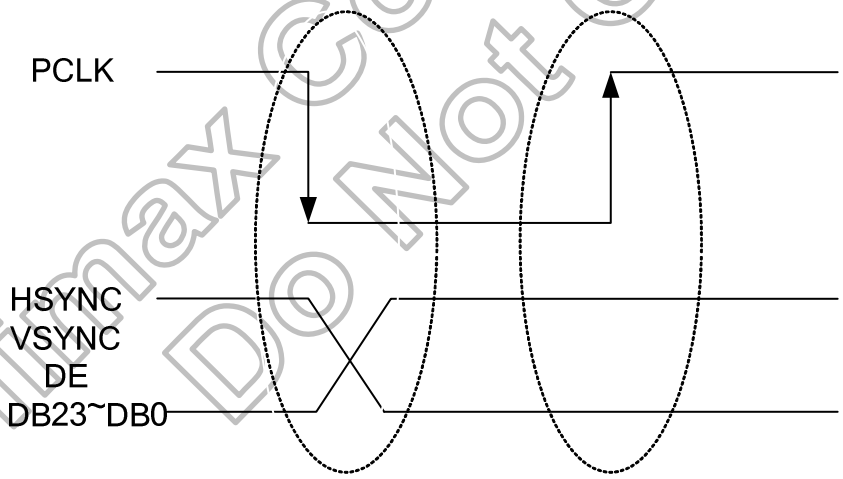


Figure 4.26: Display module data transfer recovery

4.2.2 MIPI DPI interface (Display Pixel Interface)

The HX8369-A02 uses 16 or 18-bit or 24-bit parallel RGB interface which includes: HS, VSYNC, DE, PCLK, DB23~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB23~DB0– lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In– mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative (“-“, “0”, low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative (“-“, “0”, low) active and its state is read to the display module by a rising edge of the PCLK- line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is positive (“+”, “1”, high) active and its state is read to the display module by a rising edge of the PCLK-line. DB23~DB0 (24 bit: R7-R0, G7-G0 and B7-B0; 18 bit: R5- R0, G5-G0 and B5-B0; 16 bit: R4- R0, G5-G0 and B4-B0) are used to tell what is the information of the image that is transferred on the display (when DE=1 and there is a rising edge of PCLK). DB23~DB0– lines can be set to “0” (low) or “1” (high). These lines are read by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.



Note: PCLK is an unsynchronized signal (It can be stopped).

Figure 4.27: PCLK cycle

4.2.2.1 General timing diagram

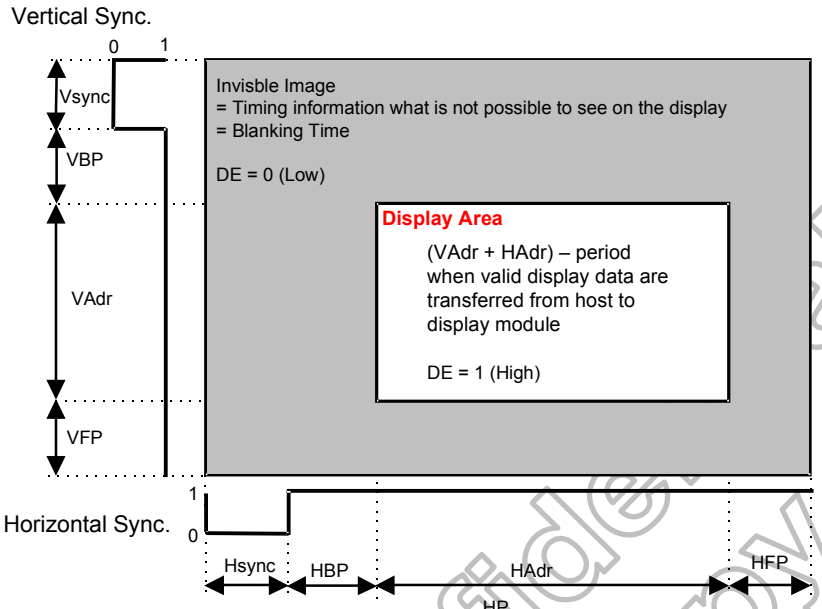


Figure 4.28: General timing diagram

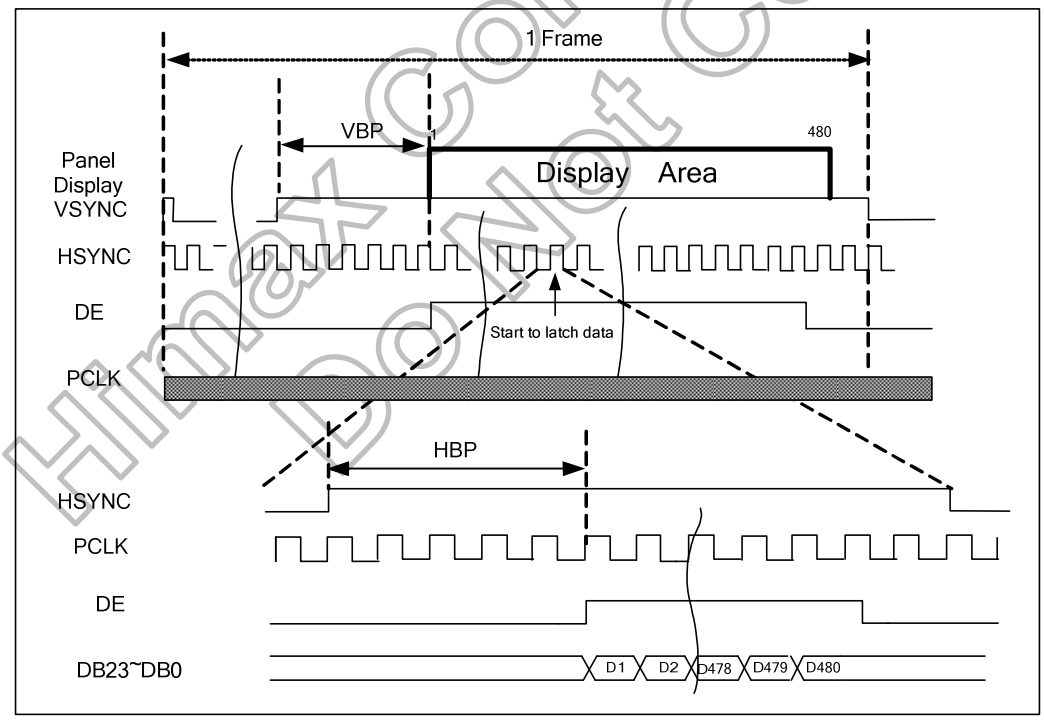


Figure 4.29: DPI (480RGB x 864) timing diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

The MIPI DPI interface includes two types which are 16-/18-/24-bit data format by register 3Ah (set_pixel_format) to select.

DPI interface displaying moving pictures can be selected to rewrite into the GRAM or not through GRAM. The selection is set by register DM[1:0] and RM.

RM The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation.

RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting.

RM	Interface for RAM access
0	DBI Interface (CPU)
1	DPI Interface (RGB)

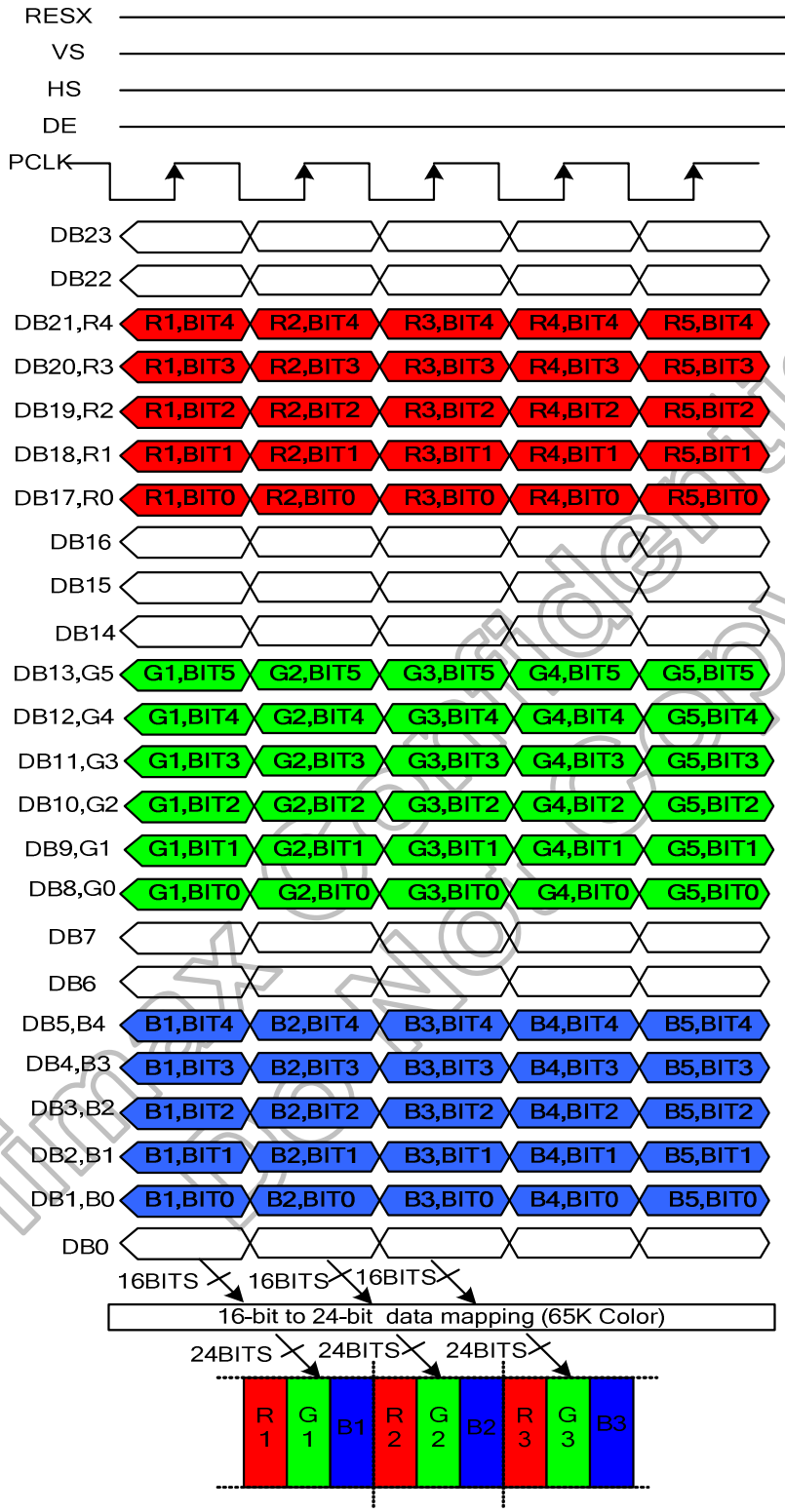
DM[1:0] The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal.
Note that switching between VSYNC and DPI operation is prohibited.

DM 1	DM 0	Display Mode
0	0	Internal oscillation clock
0	1	DPI signal (VSYNC+HSYNC)
1	0	VSYNC signal only
1	1	RGB data bypass GRAM mode

Operation Mode	Frame Memory Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal clock operation (displaying still pictures)	MPU interface (RM=0)	Internal clock operation (DM[1:0]=00)
RGB interface : capture mode 1 (displaying moving pictures)	RGB interface (RM=1)	RGB interface : VS & HS (DM[1:0]=01)
RGB interface : capture mode 2 (rewriting still pictures while displaying moving pictures)	MPU interface (RM=0)	RGB interface : VS & HS (DM[1:0]=01)
RGB interface : through mode (displaying moving pictures)	Bypass frame memory	RGB interface : VS & HS (DM[1:0]=11)
Internal clock operation RGB data format	RGB interface (RM=1)	Internal clock operation (DM[1:0]=00)

Note: RGB interface capture mode is only for 24-bit / pixel color order.

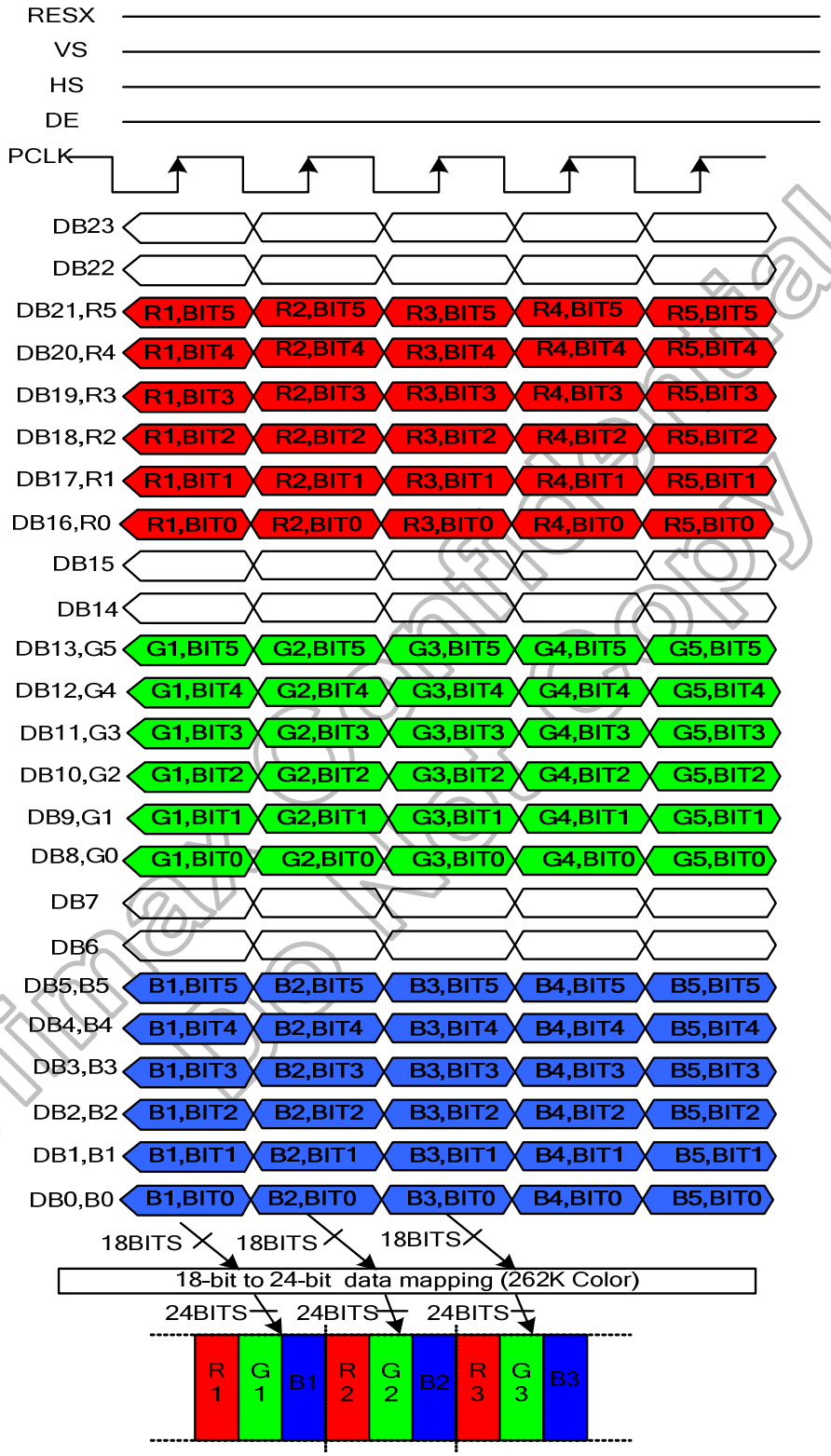
4.2.2.2 16-bit / pixel color order on the DPI I/F



Note: The data order is shown as follows, MSB=DB23, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data. Un-used pin DB23, DB22, DB16, DB15, DB14, DB7, DB6 and DB0 are set to open.

Figure 4.30: 16-bit / pixel 65K colours order on the DPI I/F

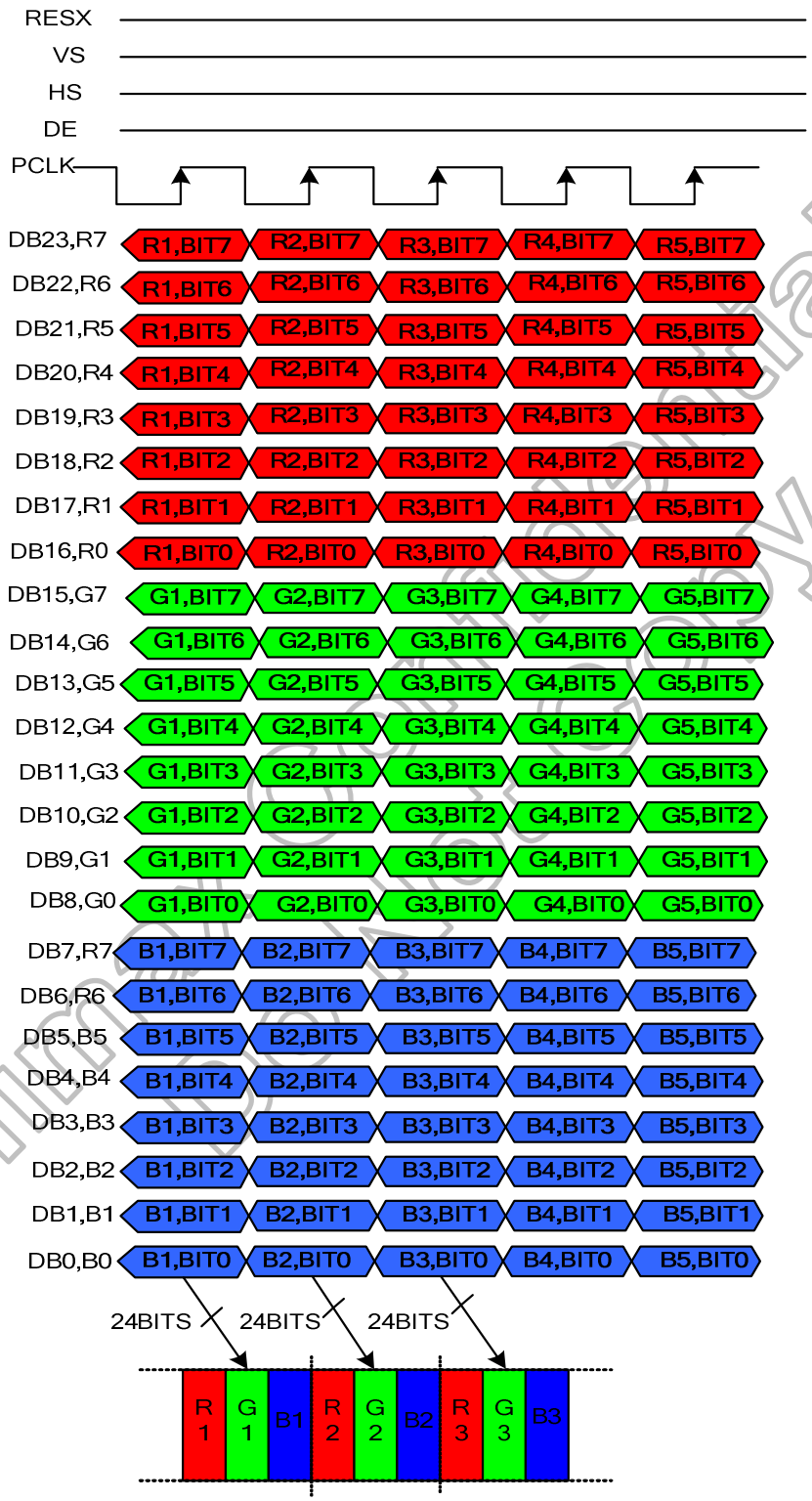
4.2.2.3 18-bit / pixel color order on the DPI I/F



Note: The Data order is shown as follows, MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data. Un-used pin DB23, DB22, DB15, DB14, DB7 and DB6 are set to open.

Figure 4.31: 18-bit / pixel: 262k colours order on the DPI I/F

4.2.2.4 24-bit / pixel color order on the RGB I/F



Note: The Data order is shown as follows, MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green and Blue data.

Figure 4.32: 24-bit / pixel color order on the RGB I/F

4.2.3 DSI system interface

The selection of interface is by BS(3-0) =”1000 “ or “1100”, the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.33 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that. DSI-compliant peripherals support Command Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display.

Command Mode refers to operation in which transactions primarily take the form of sending Commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

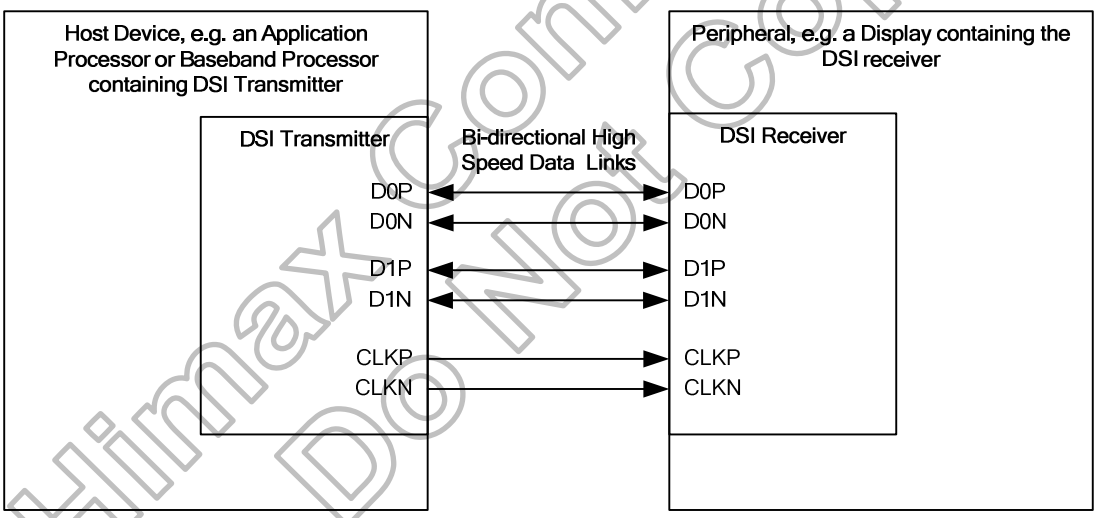


Figure 4.33: DSI transmitter and receiver interface

Please refer to “**DRAFT MIPI Alliance Standard for DSI**” for DSI detailed specifications.

4.2.3.1 DSI layer definitions

According Figure 4.34 DSI transmitter and Receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four types: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

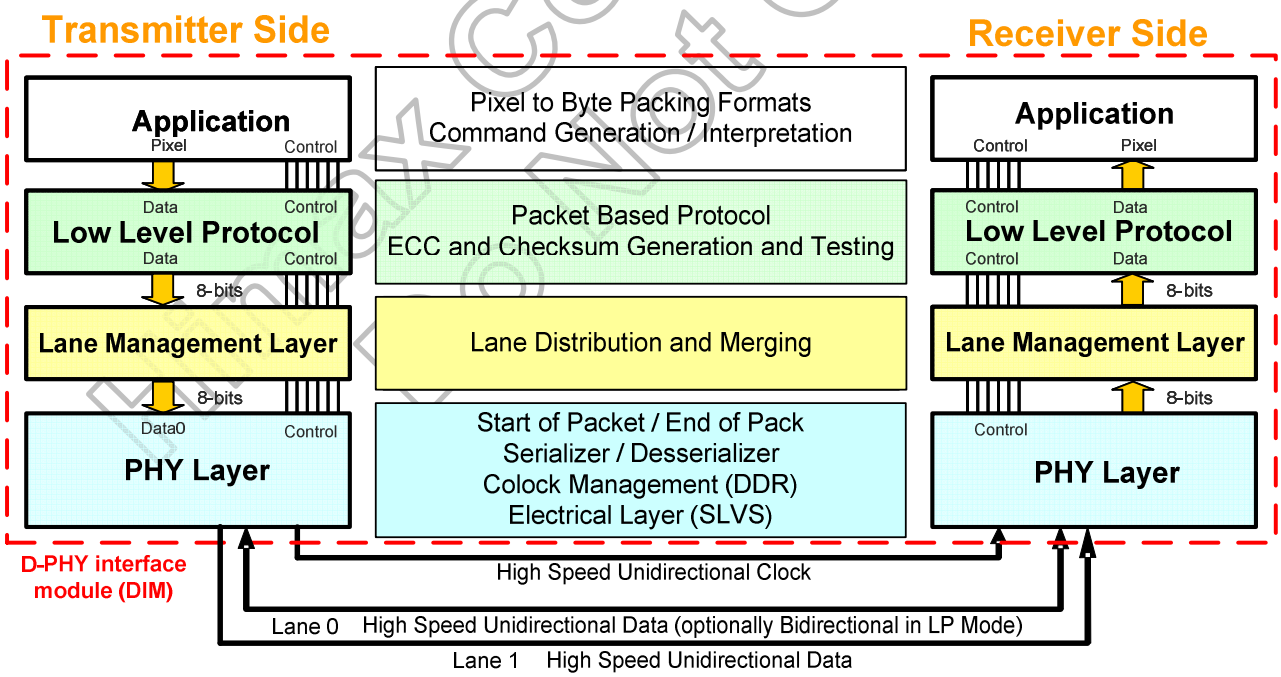
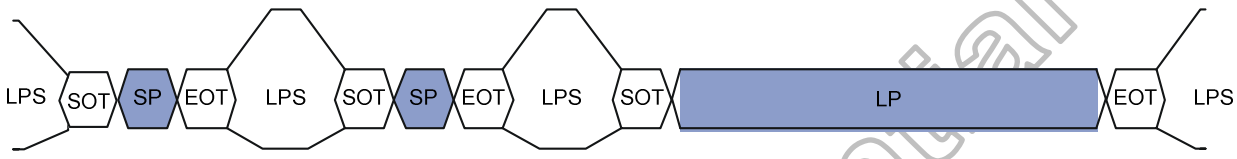


Figure 4.34: DSI transmitter and receiver interface

4.2.3.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 4.35 illustrates multiple HS Transmission packets.

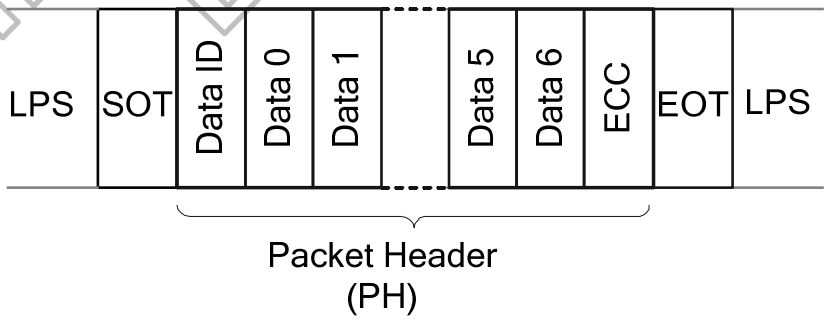


LPS：Low power state
SOT：Start of Transmission
SP：Short Packet
LP：Long Packet
EOT：End of Transmission

Figure 4.35: Multiple HS transmission packets

The packet includes two types which are Long packet and short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the length of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Short packets specify the payload length using the Data Type field and are from two to nine bytes in length. Short packet is used for most Command Mode commands and associated parameters. Where short packets format include an 8-bit Data ID followed by zero to seven bytes and an 8-bit ECC. Figure 4.36 shows the structure of the Short packet.

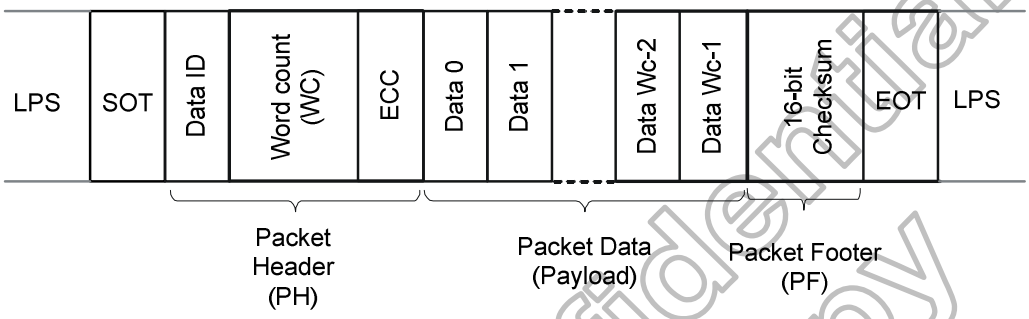


DI(Data ID)：Contain Virtual Channel Identifier and Data Type.
ECC(Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

Figure 4.36: Structure of the short packet

Long packets specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,541 bytes in length. Long packets permit transmission of large blocks of pixel or other data.. Figure 4.37 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where 65,541 bytes = (2^{16}-1) + 4 bytes PH + 2 bytes PF



DI (Data ID)：Contain Virtual Channel Identifier and Data Type.
WC (Word Count)：The receiver use WC to define packet end.
ECC (Error Correction Code)：The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF(Packet Footer)：Mean 16-bit Checksum.

Figure 4.37: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.38 the shows format of Data ID.

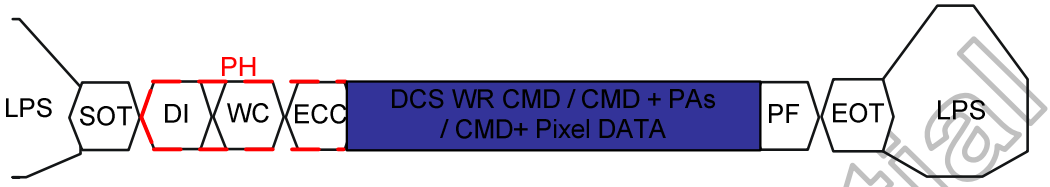
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)		DT (Data Type)					

DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Figure 4.38: The format of data ID.

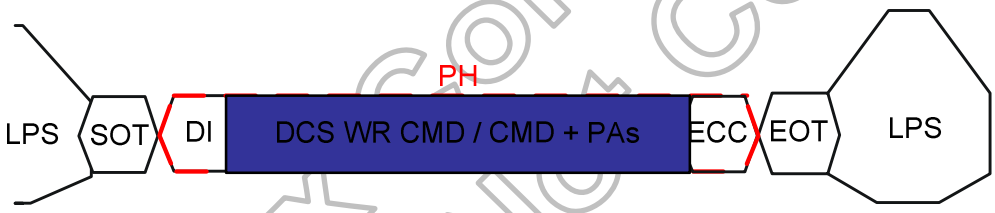
Due to Data Type (DT) mean format of transmission type, Figure 4.39 show Short- / Long-packet transmission command sequence.

Long packet write Command / Parameters / Pixel Datas



DI ➔ Write suitable Data type.
WC ➔ Write number of Payload Data.
Ex: One CMD write, WC setting as 1.
CMD + PAs write, WC setting as number of (CMD+PAs).
CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Short packet write Command / Parameters



DI ➔ Write suitable Data type.
Ex: One CMD write, DI + DCS WR CMD
CMD + PAs write, DI + DCS WR CMD + PAs

Figure 4.39: show Short- / Long-packet transmission command sequence

4.2.3.3 Processor to peripheral direction packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.3 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
22h	10 0010	Shut Down Peripheral Command	Short
32h	11 0010	Turn On Peripheral Command	Short
05h	000101	DCS WRITE, no parameter	Short
15h	010101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format (This project is not use)	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 4.3: Data types for processor-sourced packets

Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h	V Sync start, Start of VSA pulse.	4 bytes (DI+Data0+Data1+ECC)
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	
Note: V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.		

Display status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	4 bytes (DI+Data0+Data1+ECC)
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	
Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.		

Color mode status (Color Mode On, Color Mode Off)		
Data type, hex	**Function description**	**Number of bytes**
05h and 15h	DCS Short Write command, 0 or 1 parameter, Data Types = 00 0101(05h), 01 0101 (15h), Respectively.	4 bytes (DI+Data0+Data1+ECC)
NOTE: (1) For write part, If DCS Short Write command, followed by BTA, the peripheral shall respond with **ACK** when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with **Acknowledge with Error Report**.		

For example: 05h DCS WRITE for no parameter command set.

05h	CMD	0	ECC

Ex. 05h, 29h, 00, 1Ch — Display On(29h)

For example: 15h DCS WRITE for only one parameter command set.

15h	CMD	Par	ECC

Ex. 15h, 36h, 08h, 11h — MADCTL(36h)-BGR bit=1

DCS command setting		
Data type, hex	**Function description**	**Number of bytes**
06h	DCS Read command, the returned data may be of Short or Long packet format.	4 bytes (DI+Data0+Data1+ECC)
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

NOTE: (1) When use DCS Read Command, the **Set Max Return Packet Size** command will limit the size of returning packets.

(2) The peripheral shall respond to DCS Read Command Request in one of the following ways:

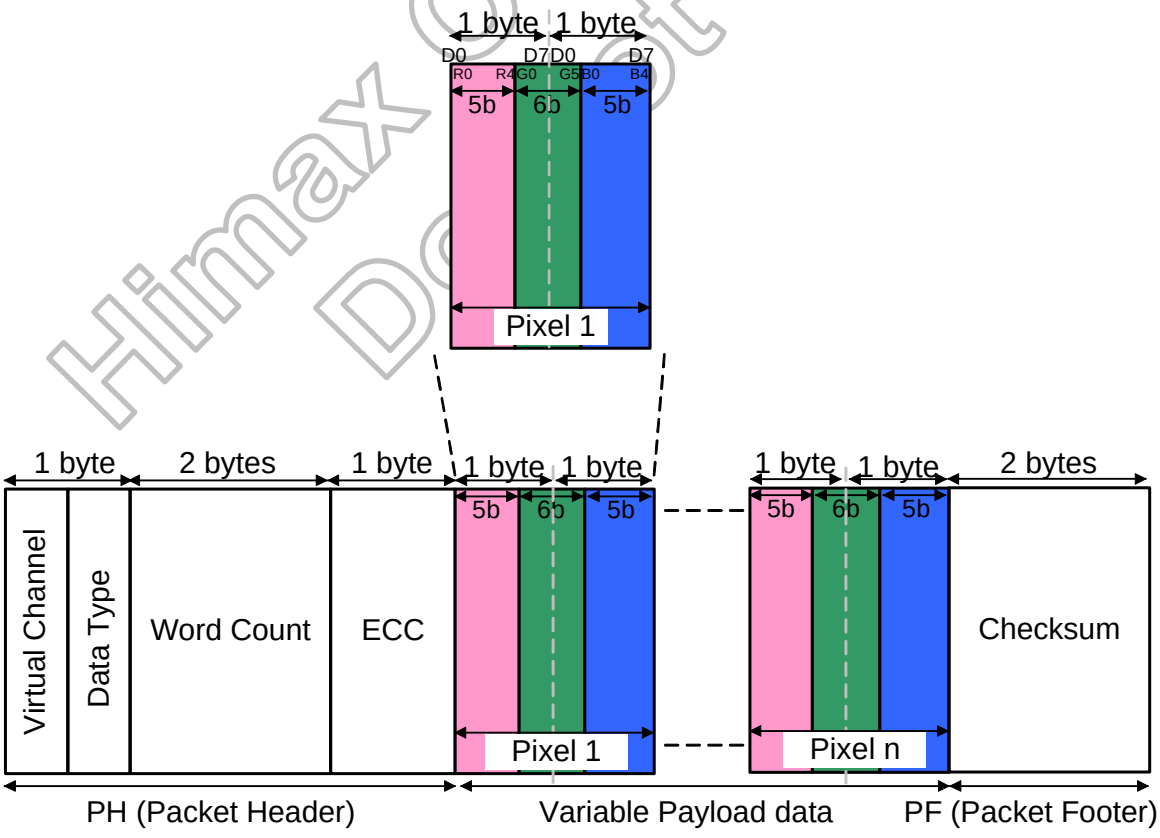
- ◆ If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- ◆ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.

(3) **One byte <= Length of payload DATA <= 2^{WC}-1**

Return packet size setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + WC + ECC)
Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.		

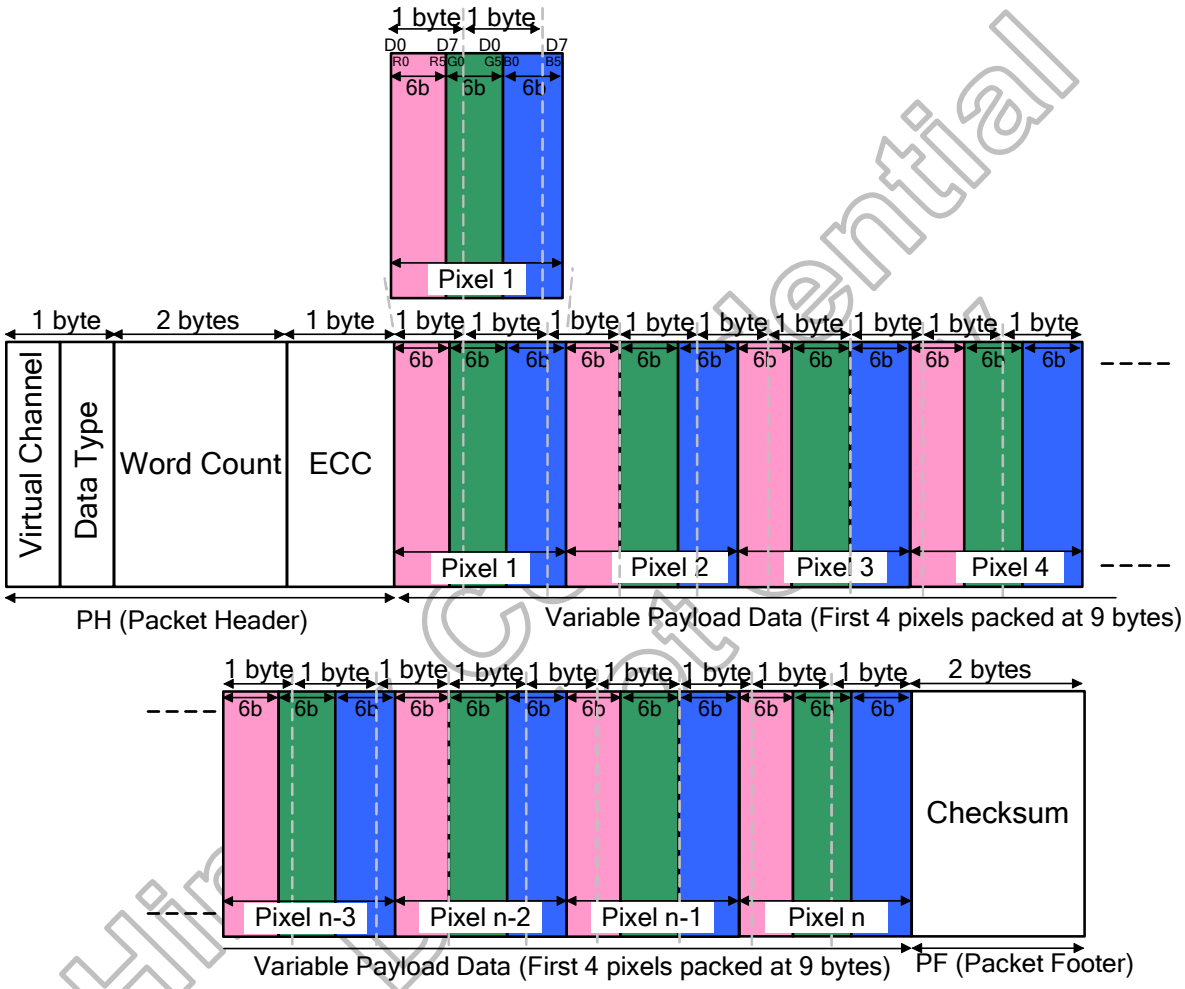
Variable data packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
19h	Blanking packet is used to convey blanking timing information in a Long packet.	
Note: (1) When **Null Packet**, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data. (2) When **Blanking packet**, the packet represents a period between active scan lines of a Video Mode display,		

Data stream format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



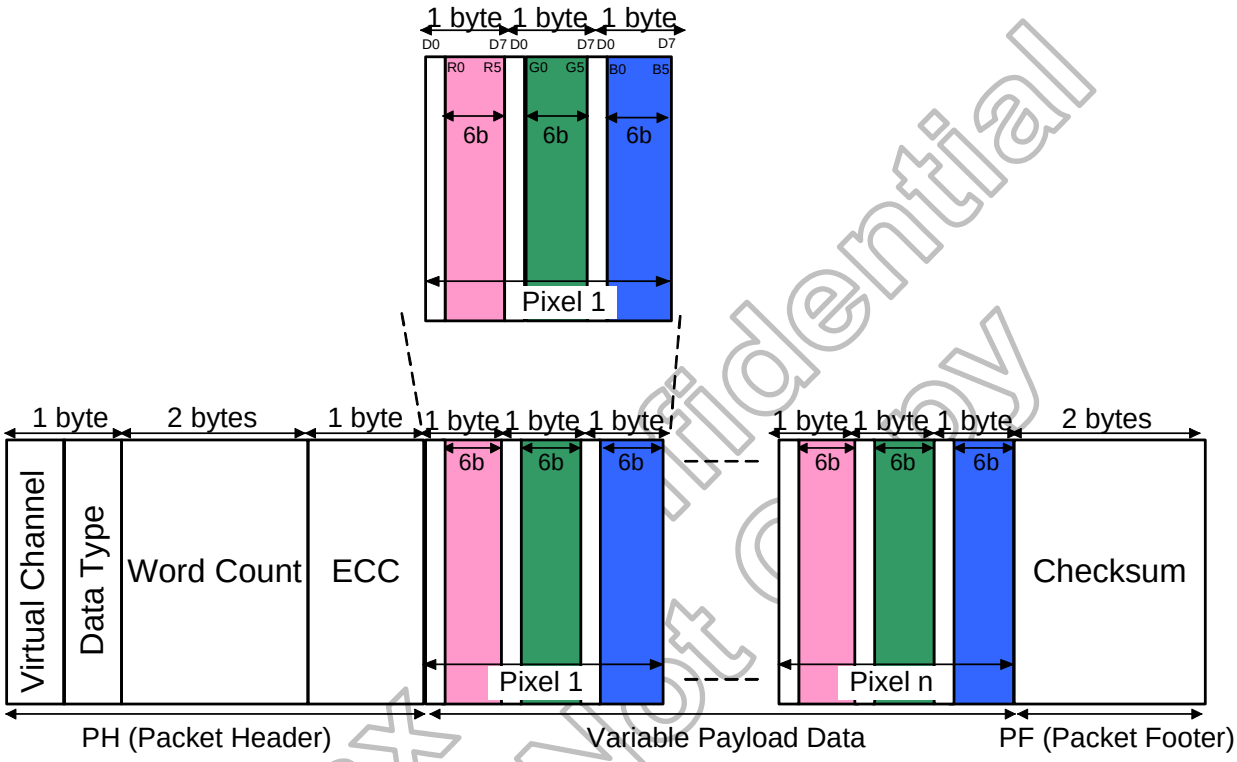
Note: Within a color component, the "LSB is sent first, the MSB last ".

Data stream format		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



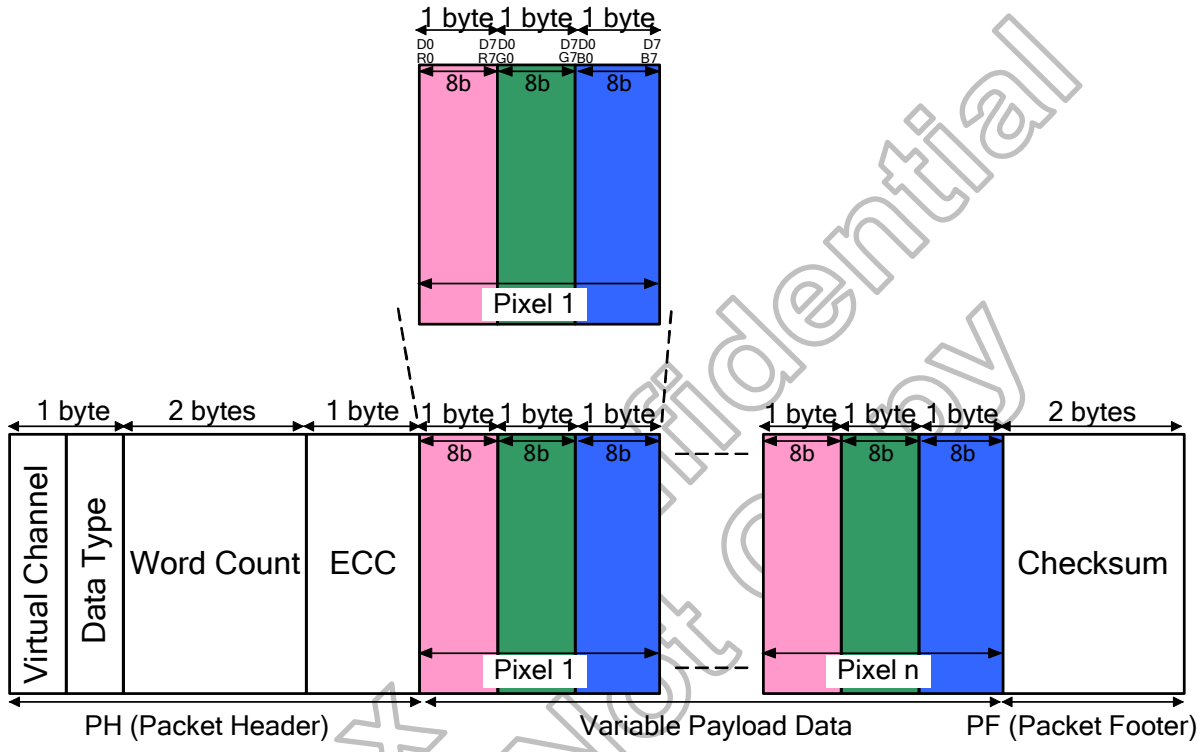
Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a “clean start” for the next line.

Data stream format		
Data type, hex	**Function description**	**Number of bytes**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is “(6 bits) red, (6 bits) green and (6 bits) blue”.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Packed pixel stream, 24-bit format		
Data type, hex	**Function description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)



Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

4.2.3.4 Peripheral to processor (reverse direction)

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets may use ECC and Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

A. Tearing Effect is a Trigger message sent to convey display timing information to the host processor. Trigger messages ate signal byte packets sent by a peripheral's PHY layer in response to a signal form the DSI protocol layer.
B. Acknowledge is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication.
C. Acknowledge and Error Report is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
D. Response to Read Request may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain under form.

A. Following a **non-Read command** in which no error was detected, the peripheral shall respond with Acknowledge.
B. Following a **Read request** in which no error was detected, the peripheral shall send the requested READ data.
C. Following a **Read request in which the ECC error** was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report*)* packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
D. Following a **non-Read command in which the ECC error** was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report*)* packet, the Error Report shall have the ECC Error flag set.
E. Following any command in which **SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid** was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

Which,

A. “Acknowledge” includes 2 bytes which are DI (VC + Acknowledge Data Type) and ECC.
B. “Acknowledge with Error Report” include 4 bytes which are DI, 2 bytes Error report and ECC.
C. “Response to Read Request” contains 2 types which are Short packet and long packet.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.4 shows the Error Report Bit Definitions. And Table 4.5 list complete set of peripheral-to-processor Data Types.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	reserved
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	LP-TX Timeout Error
6	reserved
7	reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	reserved
14	reserved
15	reserved

Table 4.4: Shows the error report bit definitions.

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
1Ch	01 1100	DCS Long READ Response	Long
Others (00h→3Fh)		Reserved	-

Table 4.5: The complete set of peripheral-to-processor data types.

Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes
Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error→Acknowledge with error report, Without error→ Acknowledge.		

DCS Read types		
Data type, hex	**Function description**	**Number of bytes**
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
Note: If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.		

4.2.4 MDDI Interface (Mobile Display Digital Interface)

4.2.4.1 Introduction of MDDI

The HX8369-A02 support MDDI, which is a differential serial interface with high-speed、low voltage swing characteristics. Both command and display image data can be transferred by MDDI. The devices connected by Data and STB link are host and client part.

Host transfer data to client in “forward” direction, client transfer data to host in “reverse” direction. The Data line is Dual direction, both command and image data are all send through the Data line. The STB line send strobe signal from host to client.

Data transferred in MDDI link are encoded as packet type.

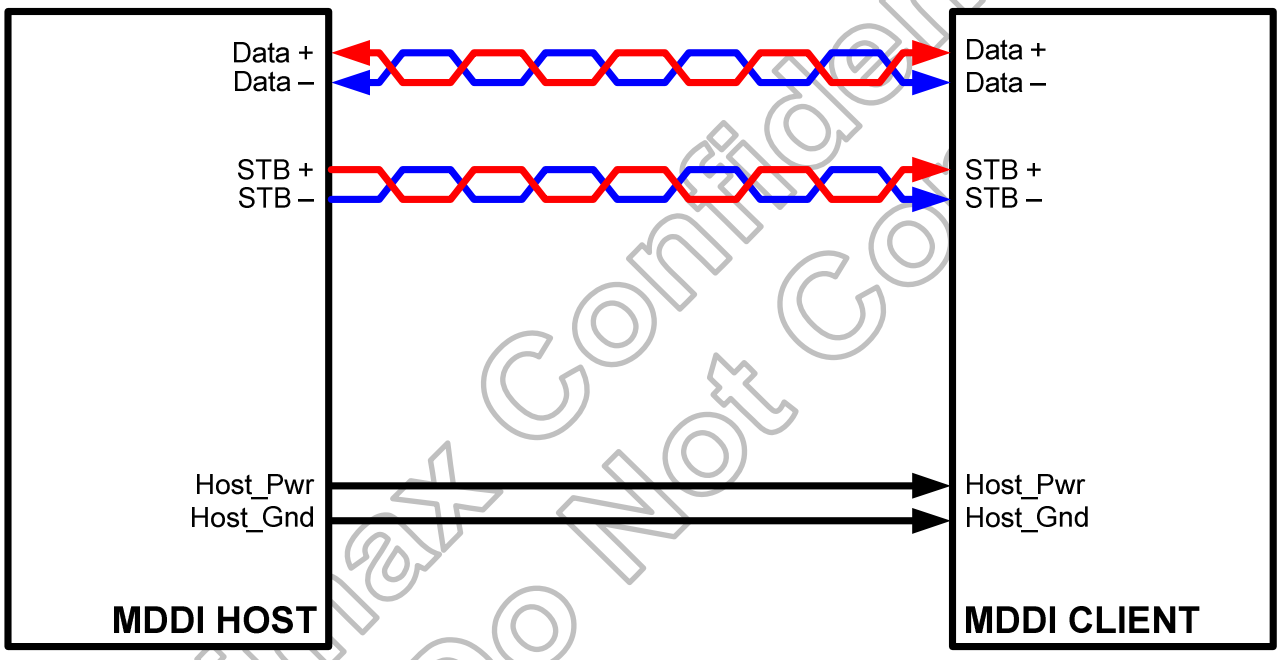


Figure 4.40: Physical connection of MDDI host and client

4.2.5 Terminology

The devices connected by the MDDI link are called the host and client. Data going from the host to the client travels in the ***forward*** direction, and data from the client to the host travels in the ***reverse*** direction.

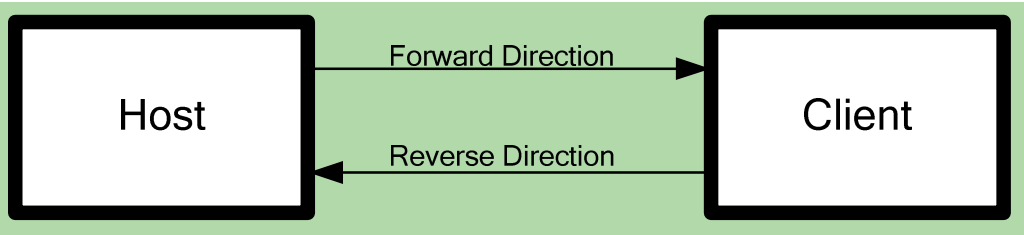


Figure 4.41: MDDI terminology

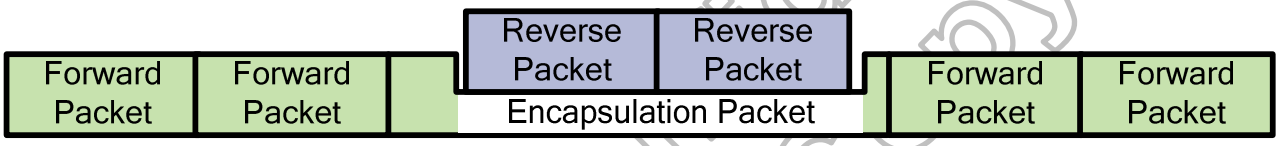


Figure 4.42: Example of Bi-directional MDDI communication

4.2.6 Order of data transmission

All fields are transmitted with the LSB first and the MSB transmitted last. Parameters that are more than one byte in length are transmitted in little-endian format, i.e. the least significant byte first. The data fields of each packet are transmitted in the exact order that they are defined in the subsequent sections below, with the first field listed being transmitted first, and the last field described being transmitted last.

MDDI_Data0 is always aligned with bit 0 of bytes transmitted on the interface in any mode: Type 1, Type 2, Type 3, or Type 4.

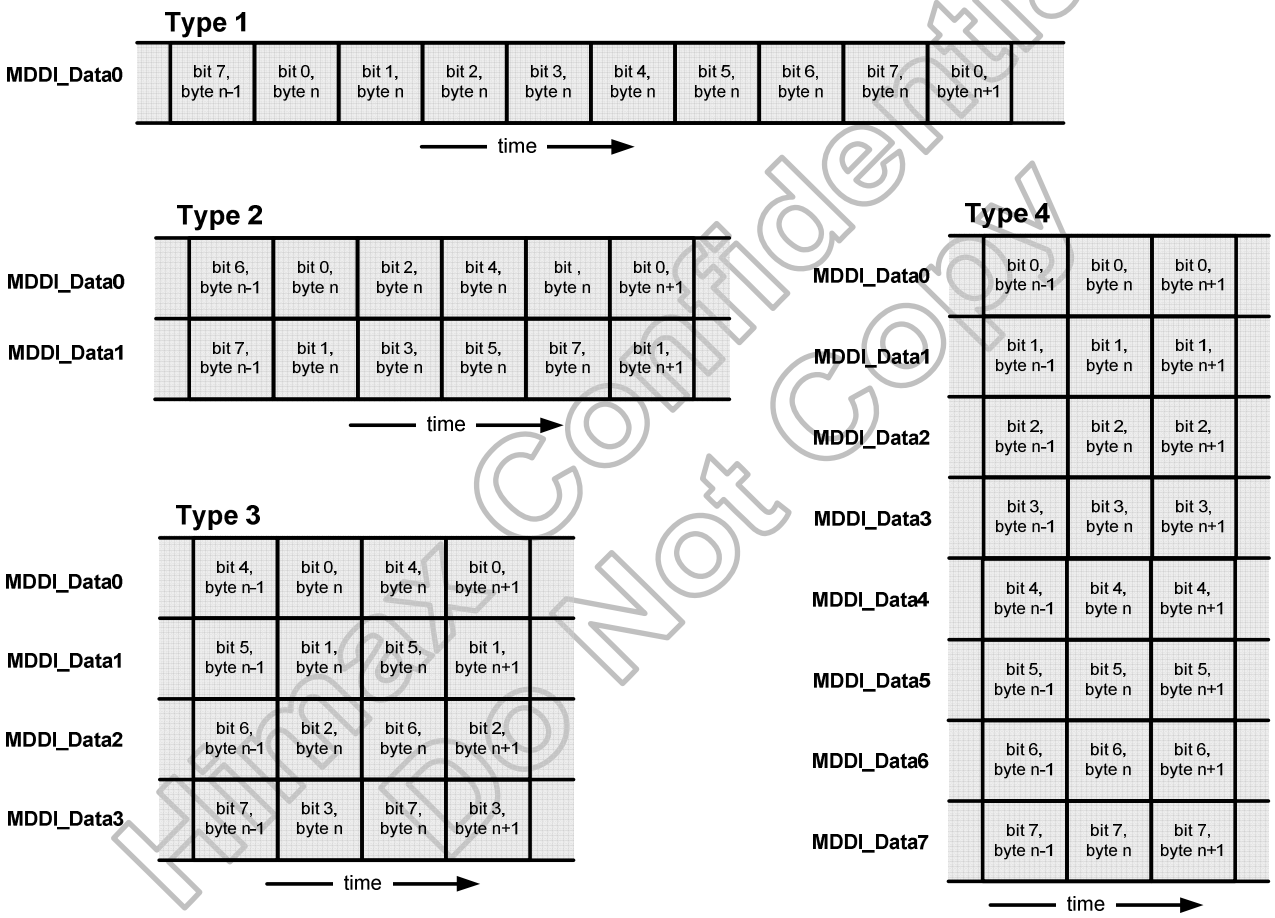


Figure 4.43: Transmission bit ordering for each type

4.2.7 Data-STB encoding

Data is encoded using a DATA-STB format. DATA is carried over a bi-directional differential cable, while STB is carried over a unidirectional differential cable driven only by the host. Figure 4.44 illustrates how the data sequence “1110001011” is transmitted by using DATA-STB encoding.

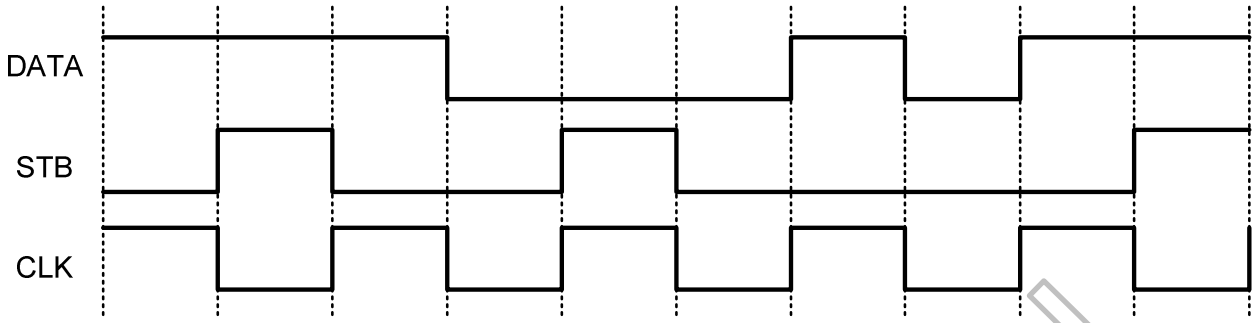


Figure 4.44: Data-STB encoding

Figure 4.45 shows a sample circuit to generate DATA and STB from input data, and then decodes the DATA and STB to the Output Data.

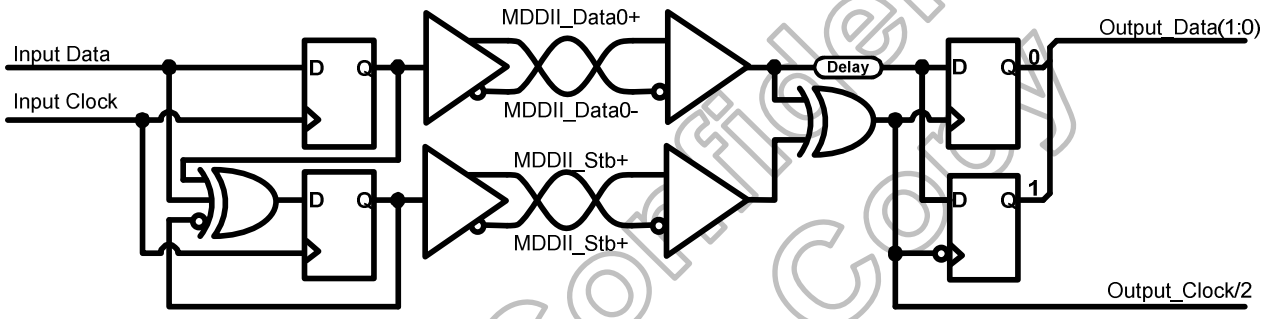


Figure 4.45: Data / STB generation & recovery circuit

4.2.7.1 MDDI data / STB

The data (MDP/MDN) and STB (MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

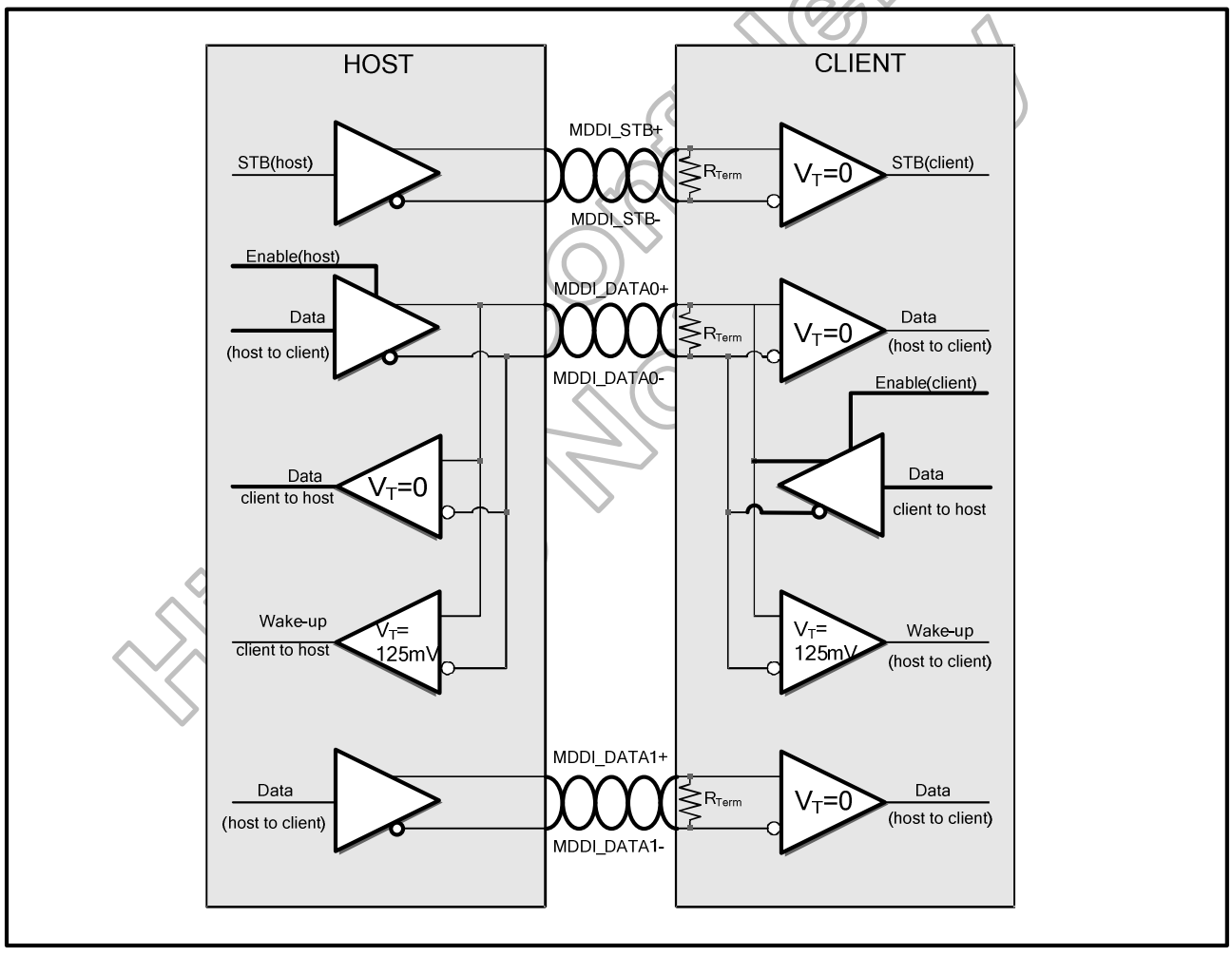


Figure 4.46: Differential connection between host and client

4.2.7.2 MDDI packet

Data transmission over the MDDI link is grouped into packets. Several packets format is supported in HX8369-A02. Most packets are in forward direction, transferred from host to client; reverse encapsulation packet is in reverse direction, transferred from MDDI client to host. A number of packets, started by sub-frame header packet, construct one sub frame.

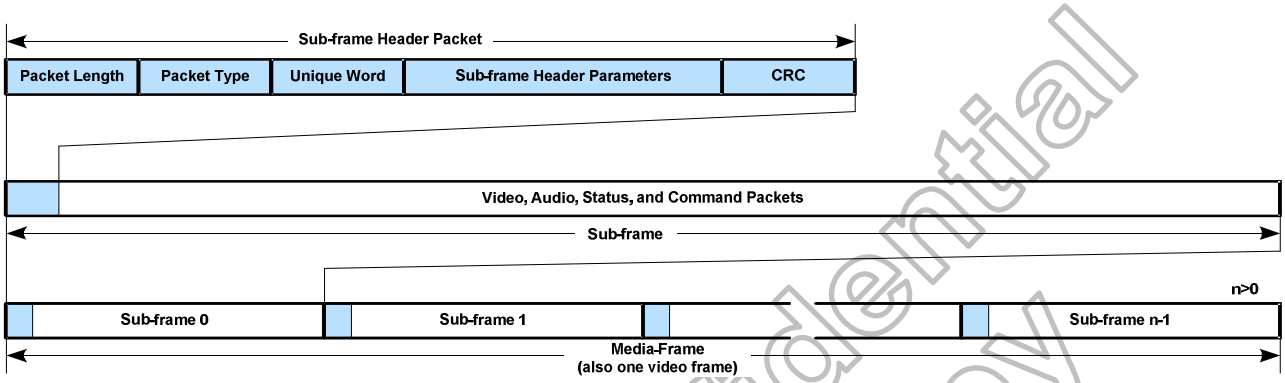
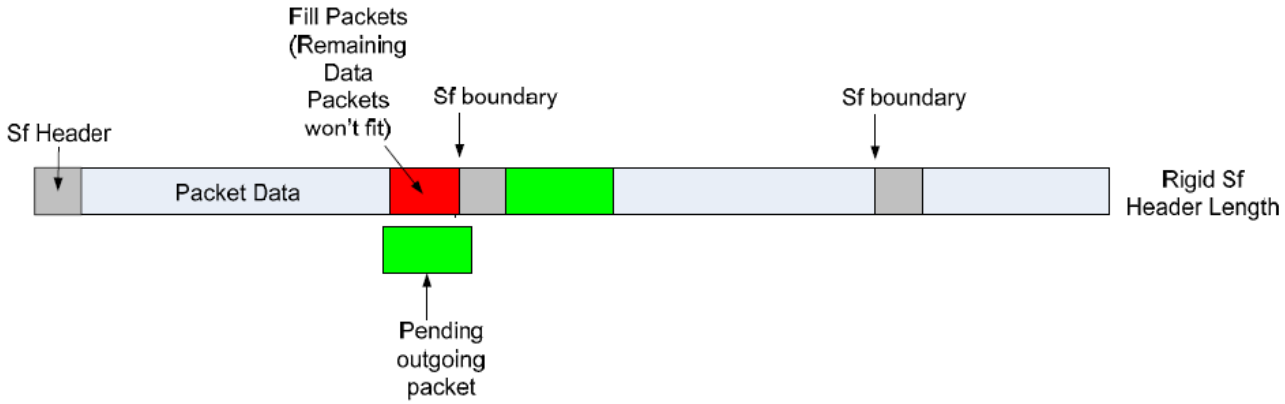


Figure 4.47 MDDI packet structure

Refer to MDDI frame structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frames make up a media-frame.

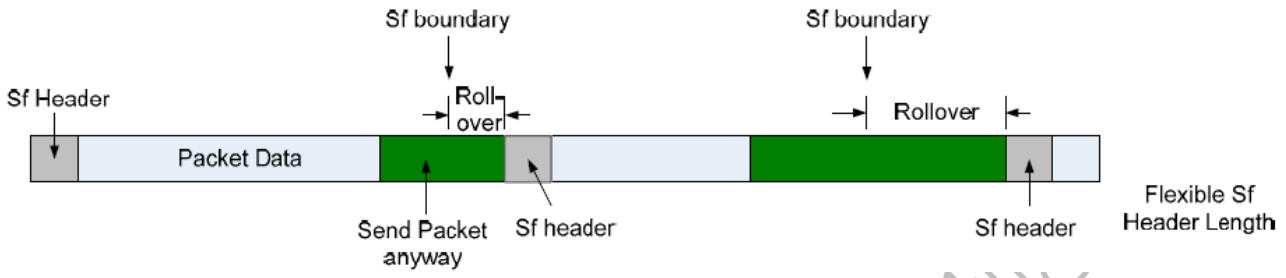
The length of sub-frame has three mode Fixed, Flexible and Unlimited.

Fixed sub-frame length means the total byte in a sub-frame will meet the value which defined in the sub-frame header packet in front of a sub-frame.

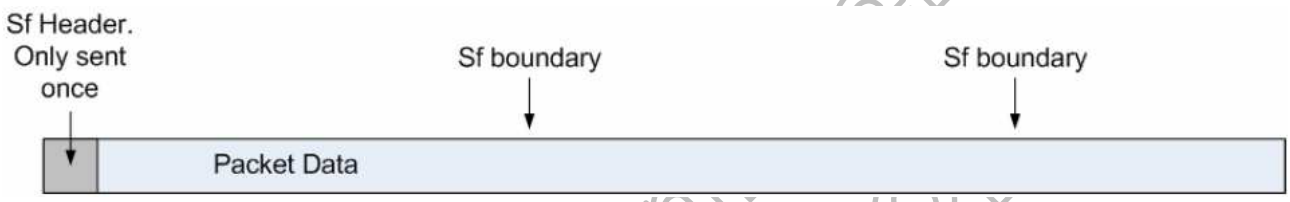


In flexible sub-frame When a packet is requested to be transmitted, it will never be blocked. This may cause a packet to cross a sub-frame boundary. The host therefore must maintain the sub-frame timing within its core to keep track of sub-frames that havelengths greater than the target length, to then transmit a matched number and length of sub-frames that are

less than the target sub-frame length to ensure an average sub-frame length that matches the target length.



hibernation to help the client sync up with the unique word pattern. The MDDI host is allowed to transmit a sub-frame at any time if it wishes, however it is not required.



HX8369-A02 support these packets, which described in the table below.

Packet	Function	Direction
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Windowless Video stream packet	Video data transfer	Forward
Flexible Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Enhanced Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Client request and status packet	Information about client status	Reverse
Forward Link Skew Calibration Packet	Use to Calibrate the delay skew	Forward
Perform Type Handoff Packet	Change operate Type	Forward
Link shutdown packet	End of frame	Forward

Table 4.6: List of supported MDDI packet

Sub-frame header packet

Packet Length	Packet type =0x3bffh	Unique word =0x005a	Reserved 1	Sub-frame length	Protocol Version	Sub-frame Count	Media-frame Count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length	:	total number of bytes in the packet not including the packet length field, always 20
packet type	:	packet type, 0x3bffh for sub-frame header packet
unique word	:	link packet type to form a 32-bit unique word for good autocorrelation.
reserved 1	:	not used(all zero)
sub-frame length	:	In fixed Sub-Frame mode, this value specifies number of bytes per sub-frame. In the Flexible Sub-Frame mode ,this value represents the target length. In the unlimited Sub-Frame mode, the value is set to zero
	:	All zero define the length of the sub-frame is undefined.
protocol version	:	set all zero
sub-frame count	:	specifies number of sub-frame header packet.
media frame count	:	specifies number of media frame
CRC	:	error check

Register access packet

Packet Length	Packet type =146	bClient ID	Read/Write Info	Register Address	Parameter CRC	Register Data list	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	P_length-14 bytes	4 bytes

packet length	:	total number of bytes in the packet not including the packet length field
packet type	:	packet type, 146(decimal) for register access packet
bClient ID	:	set all zero
Read/Write Info	:	when write value to register, bit[15:14] = “00”
		when request data from register, bit[15:14]=“10”
		when data from client, bit[15:14] = “11”
		bit[13:0] : A 14-bit unsigned integer that specifies the number of 32-bit register Data List items to be transferred in the Register Data List field
register address	:	Register address is set written here.
parameter CRC	:	To error check from packet length to register address
register data list	:	A list of 4-byte register data values.

Video stream packet

Packet Length	Packet type =16	bClient ID	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom dedge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length - 26 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 16 (decimal) for register access packet
bClient ID : set all zero
video data format descriptor : bits[15:13]=010, raw RGB format (fixed value)
bit[12]=1,only packed type is available (fixed value)
bits[11:0]=number of bits per pixel,
bits[11:8]=for Red,bits[7:4]=for Green,bits[3:0]=for Blue
pixel data attributes : bits[1:0]=11, displayed both eyes (fixed value)
: others are all zero
X left edge : X coordinate of the left edge of the active window filled by the Pixel Data field.
X top edge : Y coordinate of the top edge of the active window filled by the Pixel Data field
X right edge : X coordinate of the right edge of the active window filled by the Pixel Data field.
Y bottom edge : Y coordinate of the bottom edge of the active window filled by the Pixel Data field.
X start : X coordinate of the first pixel in the Pixel Data field below
Y start : X coordinate of the first pixel in the Pixel Data field below
Pixel count : Write number of pixel
Patameter CRC : To error check from packet length to pixel count
pixel data : pixel data info. Number of pixel data must not be over 65509
pixel data CRC : To pixel data error check.

Windowless video stream packet

Packet Length	Packet type =22	bClient ID	video data format descriptor	pixel data attributes	pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	packet length - 14 bytes	2 bytes

packet length : total number of bytes in the packet not including the packet length field
packet type : packet type, 22 (decimal) for register access packet
bClient ID : set all zero
video data format descriptor : bits[15:13]=010, raw RGB format (fixed value)
bit[12]=1,only packed type is available (fixed value)
bits[11:0]=number of bits per pixel,
bits[11:8]=for Red,bits[7:4]=for Green,bits[3:0]=for Blue
pixel data attributes : bits[1:0]=11, displayed both eyes (fixed value)
others are all zero
Pixel count : Write number of pixel
Patameter CRC : To error check from packet length to pixel count
pixel data : pixel data info. Number of pixel data must not be over 65509
pixel data CRC : To pixel data error check.

Flexible video stream packet

Packet Length	Packet type =20	bClient ID	Field Present Flags	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom dedge	X start	Y start
2 bytes	2 bytes	2 bytes		2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length – present header bytes	2 bytes

packet length	**:**	**total number of bytes in the packet not including the packet length fie**
packet type	**:**	**packet type, 16 (decimal) for register access packet**
bClient ID	**:**	**set all zero**
Field Present Flags	**:**	**A value of '1' for each bit indicates that the field is present in the packet. A value of '0' for the bit indicates that the field is not present. o Bit 0 indicates the presence of the Video Data Format Descriptor field. o Bit 1 indicates the presence of the Pixel Data Attributes field. o Bit 2 indicates the presence of the X Left Edge field. o Bit 3 indicates the presence of the Y Top Edge field. o Bit 4 indicates the presence of the X Right Edge field. o Bit 5 indicates the presence of the Y Bottom Edge field. o Bit 6 indicates the presence of the X Start field. o Bit 7 indicates the presence of the Y Start field. o Bit 8 indicates the presence of the Pixel Count field. o Bits [15:9] must be set to '0'.**
video data format descriptor	**:**	**bits[15:13]=010, raw RGB format (fixed value) bit[12]=1,only packed type is available (fixed value) bits[11:0]=number of bits per pixel, bits[11:8]=for Red,bits[7:4]=for Green,bits[3:0]=for Blue**
pixel data attributes	**:**	**bits[1:0]=11, displayed both eyes (fixed value) others are all zero**
X left edge	**:**	**X coordinate of the left edge of the active window filled by the Pixel D**
X top edge	**:**	**Y coordinate of the top edge of the active window filled by the Pixel D**
X right edge	**:**	**X coordinate of the right edge of the active window filled by the Pixel**
Y bottom edge	**:**	**Y coordinate of the bottom edge of the active window filled by the Pix**
X start	**:**	**X coordinate of the first pixel in the Pixel Data field below**
Y start	**:**	**X coordinate of the first pixel in the Pixel Data field below**
Pixel count	**:**	**Write number of pixel**
Patameter CRC	**:**	**To error check from packet length to pixel count**
pixel data	**:**	**pixel data info. Number of pixel data must not be over 65509**
pixel data CRC	**:**	**To pixel data error check.**

Perform type handoff packet

Packet Length	Packet type =77	Interface Type	Reserved1	Delay filler	CRC
2 bytes	2 bytes	1 byte	1 byte	Packet Length – 6 bytes	2 bytes

packet length	:	total number of bytes in the packet not including the packet length field
packet type	:	packet type, 77(decimal) for perform type handoff packet
interface type	:	contain the new type to be used. Bit[2:0], define the forward link 1: handoff to type1 2: handoff to type2 others: not used. Bit[5:3], define the reverse link 1: handoff to type1 others not used bit[7:6], set all zero.
Reserved1	:	Set all zero
delay filler	:	Set all zero Forward link is Type1, Delay filler is 16byte Forward link is Type2, Delay filler is 32byte
CRC	:	To error check

Forward link skew calibration pack

Packet Length	Packet type =83	hClient ID	CRC	All Zero1	Calibration Data Sequence	All Zero2
2 bytes	2 bytes	2 bytes	2 bytes	8 bytes	Packet Length - 22 bytes	8 bytes

packet length	:	total number of bytes in the packet not including the packet length field
packet type	:	packet type, 83(decimal) for perform type handoff packet
hClient ID	:	contain the new type to be used.
CRC	:	To error check
All Zero 1	:	Set all zero
Calibration Data Sequence	:	a data sequence that causes the MDDI_Data signals to toggle at every data period. o Type 1 – (64 byte data sequence) AAh, AAh … or 55h, 55h… o Type 2 – (128 byte data sequence) CCh, CCh … or 33h, 33h…
All Zero 2		Set all zero

Filler packet

Packet Length	Packet type =0	filler bytes (all zero)	CRC
2 bytes	2 bytes	packet length – 4 bytes	2 bytes

packet length total number of bytes in the packet not including the packet length field
packet type packet type, 0 (decimal) for register access packet
filler bytes set to all zero (The size is under packet length available)
CRC To error check

Link shutdown packet

Packet Length	Packet type =69	CRC	All zeros
2 bytes	2 bytes	2 bytes	16 bytes

packet length total number of bytes in the packet not including the packet length field
packet type packet type, 16 (decimal) for register access packet
CRC To error check
All zeros write all zero (size is 16 bytes, because MDDI for HX8369-A is type 1)

Fixed Value

For more information about MDDI packet refer to VESA MDDI spec.

4.2.7.3 Hibernation / Wake up

HX8369-A02 MDDI provides the hibernation mode to reduce the power consumption. The MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force the MDDI link into hibernation frequently to reduce power consumption. In hibernation mode, hi-speed drivers and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

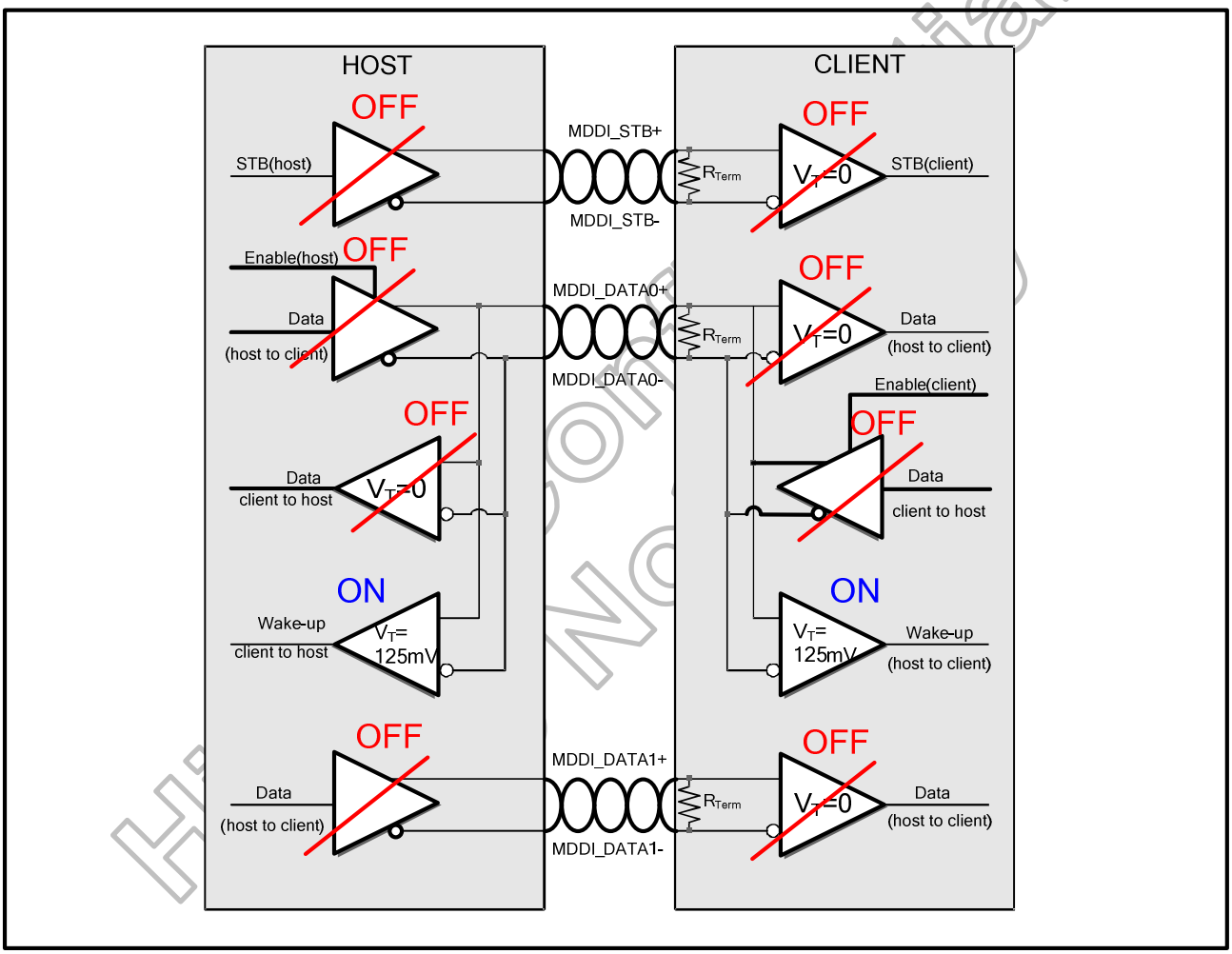


Figure 4.48: MDDI Transceiver / Receiver state in hibernation

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulses can be detected using low-speed line receivers that consume only a fraction of the current as the differential receivers required to receive the signals at the maximum link operating speed.

4.2.7.4 MDDI link wakeup sequence

Figure below provide a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The labeled events are：

Host-Initiated Wake-up

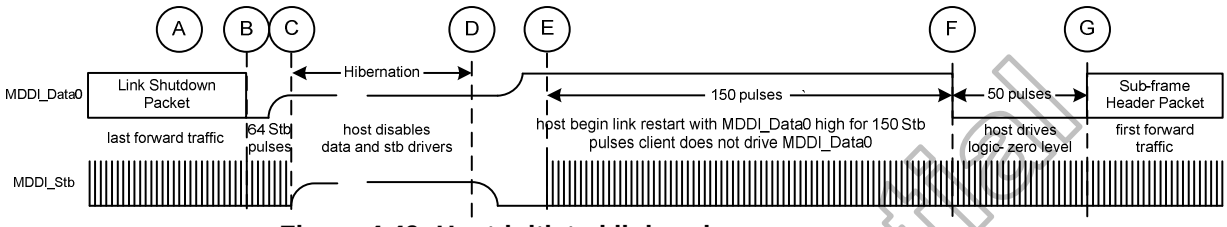


Figure 4.49: Host-initiated link wakeup sequence

An example of a typical client-initiated service request event with no contention is illustrated in below figure. The labeled events are：

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.
B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device. Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC. It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.
C. The host enters the low-power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state. It is also allowable for MDDI_Stb to be driven to a logic-zero level or to continue toggling during hibernation. The client is also in the low-power hibernation state.
D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.
E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level. The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.
F. The host drives MDDI_Data0 to a logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at a logic-zero level for 40 MDDI_Stb cycles.
G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet. Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

4.2.7.5 MDDI operation mode

The MDDI Link provides six operation modes, the mode flow is illustrated as below.

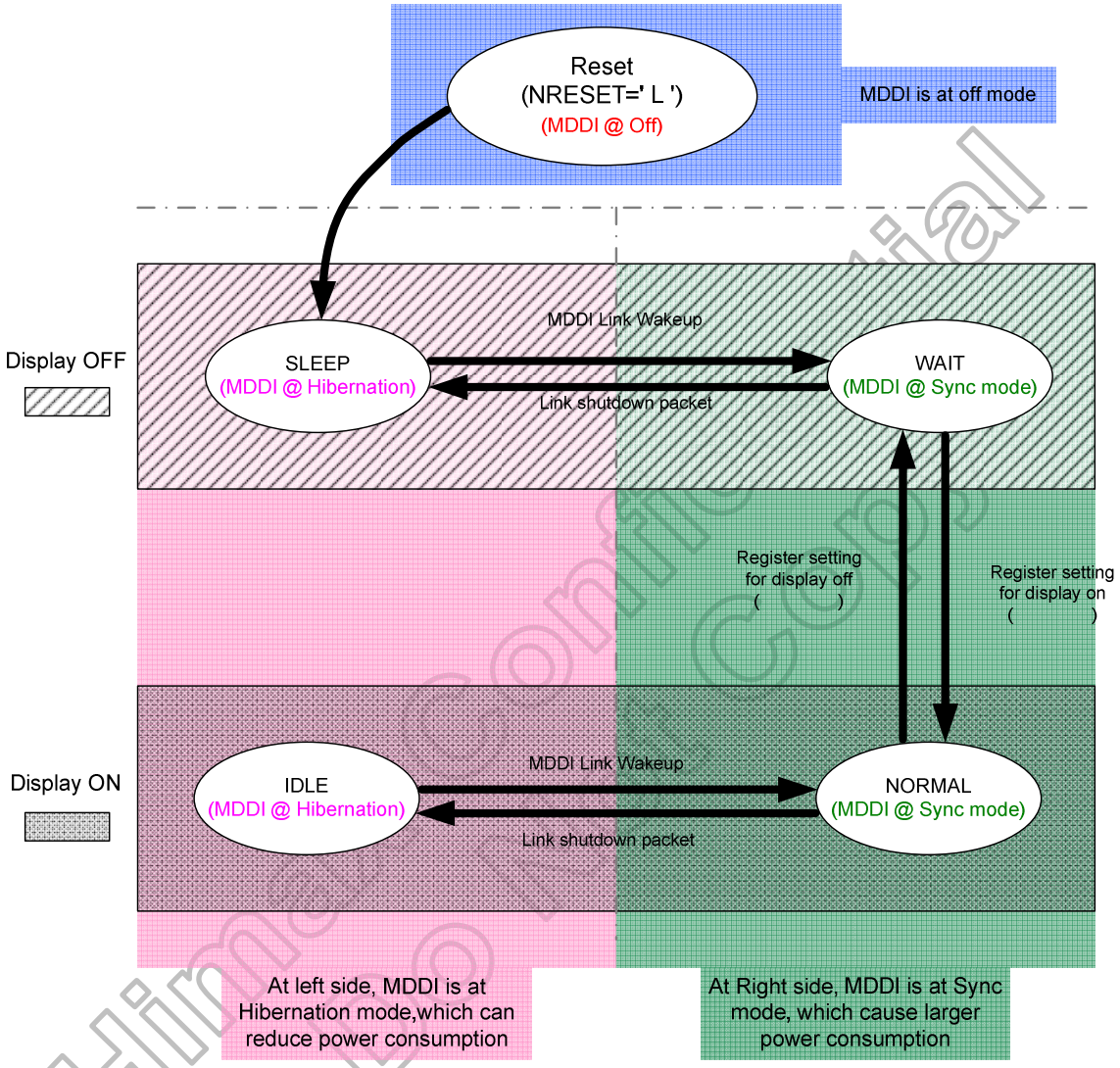


Figure 4.50: MDDI operation mode

The MDDI link provides five operation modes that are listed in the Table 4.7.

Function	RESET	SLEEP	WAIT	NORMAL	IDLE
MDDI hibernation receiver	OFF	ON	OFF	OFF	ON
MDDI normal receiver or normal driver	OFF	OFF	ON	ON	OFF
Register and RAM access	Disable	Disable	Enable	Enable	Disable
Internal oscillator(OSC)	OFF	OFF	ON/OFF (1)	ON(2)	ON(2)
Booster(VSP,VSN,VGH,VGL)	OFF	OFF	OFF	ON	ON
Regulator (VCOM,VSPR,VSNR)	OFF	OFF	OFF	ON	ON

Note: (1) While OSC_EN = 0 is defined the operation as OFF, and OSC_EN = 1 is ON.
(2) Do not set OSC_EN = 1 in Normal mode, If OSC stopped, indication also stops.

Table 4.7: Operation mode list

5. Function Description

5.1 Display data GRAM

HX8369-A02 support the display data RAM that stores display dots and consists of 9,953,280 bits (480x864x24 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

5.2 Address counter (AC)

The HX8369-A02 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

RES_SEL2	RES_SEL 1	RES_SEL 0	MV	X range	Y range	Panel resolution
0	0	0	0	0~479d.	0~863d.	480RGBX864 dot
			1	0~863d.	0~479d.	
0	0	1	0	0~479d..	0~853d.	480RGBX854 dot
			1	0~853d.	0~479d.	
0	1	0	0	0~479d.	0~799d.	480RGBX800 dot
			1	0~799d.	0~479d.	
0	1	1	0	0~479d.	0~639d.	480RGBX640 dot
			1	0~639d.	0~479d.	
1	0	0	0	0~359d.	0~639d.	360 RGBX640 dot
			1	0~639d.	0~359d.	
1	0	1	0	0~479d.	0~719d.	480RGBX720 dot
			1	0~719d.	0~479d.	

Table 5.1: Addresses counter range

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

5.3 Source, gate and memory map

5.3.1 480RGB x 864 resolution

R36h: B5=0

Source Out		S1	S2	S3	S4	S5	S6	---	S1435	S1436	S1437	S1438	S1439	S1440		
		RGB=0	RGB=1		RGB=0	RGB=1			RGB=0	RGB=1		RGB=0	RGB=1			
RA															SA	
MY=0	MY=1														ML=0	ML=1
0	863	R0 7-0	G0 7-0	B0 7-0	R1 7-0	G1 7-0	B1 7-0	---	R478 7-0	G478 7-0	B478 7-0	R479 7-0	G479 7-0	B479 7-0	0	863
1	862							---							1	862
2	861							---							2	861
3	860							---							3	860
4	859							---							4	859
5	858							---							5	858
6	857							---							6	857
7	856							---							7	856
8	855							---							8	855
9	854							---							9	854
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
856	7							---							856	7
857	6							---							857	6
858	5							---							858	5
859	4							---							859	4
860	3							---							860	3
861	2							---							861	2
862	1							---							862	1
863	0							---							863	0
CA	MX=0	0			1			---	478			479				
	MX=1	479			478			---	1			0				

Note:RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB=Red,Green and Blue pixel position change

Table 5.2: Memory map of 480RGB x 864 resolution

5.3.2 480RGB x 854 resolution

R36h: B5=0

Source Out		S1	S2	S3	S4	S5	S6	---	S1435	S1436	S1437	S1438	S1439	S1440		
		RGB=0	RGB=1		RGB=0	RGB=1			RGB=0	RGB=1		RGB=0	RGB=1			
RA															SA	
MY=0	MY=1														ML=0	ML=1
0	853	R0 7-0	G0 7-0	B0 7-0	R1 7-0	G1 7-0	B1 7-0	---	R478 7-0	G478 7-0	B478 7-0	R479 7-0	G479 7-0	B479 7-0	0	853
1	852							---							1	852
2	851							---							2	851
3	850							---							3	850
4	849							---							4	849
5	848							---							5	848
6	847							---							6	847
7	846							---							7	846
8	845							---							8	845
9	844							---							9	844
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
846	7							---							846	7
847	6							---							847	6
848	5							---							848	5
849	4							---							849	4
850	3							---							850	3
851	2							---							851	2
852	1							---							852	1
853	0							---							853	0
CA	MX=0	0			1			---	478			479				
	MX=1	479			478			---	1			0				

Note:RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB=Red,Green and Blue pixel position change

Table 5.3: Memory map of 480RGB x 854 resolution

5.3.3 480RGB x 800 resolution

R36h: B5=0

Source Out		S1	S2	S3	S4	S5	S6	---	S1435	S1436	S1437	S1438	S1439	S1440		
		RGB=0	RGB=1		RGB=0	RGB=1			RGB=0	RGB=1		RGB=0	RGB=1			
RA															SA	
MY=0	MY=1														ML=0	ML=1
0	799	R0 7-0	G0 7-0	B0 7-0	R1 7-0	G1 7-0	B1 7-0	---	R478 7-0	G478 7-0	B478 7-0	R479 7-0	G479 7-0	B479 7-0	0	799
1	798							---							1	798
2	797							---							2	797
3	796							---							3	796
4	795							---							4	795
5	794							---							5	794
6	793							---							6	793
7	792							---							7	792
8	791							---							8	791
9	790							---							9	790
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
792	7							---							792	7
793	6							---							793	6
794	5							---							794	5
795	4							---							795	4
796	3							---							796	3
797	2							---							797	2
798	1							---							798	1
799	0							---							799	0
CA	MX=0	0			1			---	478			479				
	MX=1	479			478			---	1			0				

Note:RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB=Red,Green and Blue pixel position change

Table 5.4: Memory map of 480RGB x 800 resolution

5.3.4 480RGB x 640 resolution

R36h: B5=0

Source Out		S1	S2	S3	S4	S5	S6	---	S1435	S1436	S1437	S1438	S1439	S1440		
		RGB=0	RGB=1		RGB=0	RGB=1			RGB=0	RGB=1		RGB=0	RGB=1			
RA															SA	
MY=0	MY=1														ML=0	ML=1
0	639	R0 7-0	G0 7-0	B0 7-0	R1 7-0	G1 7-0	B1 7-0	---	R478 7-0	G478 7-0	B478 7-0	R479 7-0	G479 7-0	B479 7-0	0	639
1	638							---							1	638
2	637							---							2	637
3	636							---							3	636
4	635							---							4	635
5	634							---							5	634
6	633							---							6	633
7	632							---							7	632
8	631							---							8	631
9	630							---							9	630
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
632	7							---							632	7
633	6							---							633	6
634	5							---							634	5
635	4							---							635	4
636	3							---							636	3
637	2							---							637	2
638	1							---							638	1
639	0							---							639	0
CA	MX=0	0			1			---	478			479				
	MX=1	479			478			---	1			0				

Note:RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB=Red,Green and Blue pixel position change

Table 5.5: Memory map of 480RGB x 640 resolution

5.3.5 360RGB x 640 resolution

R36h: B5=0

Source Out		S1	S2	S3	S4	S5	S6	---	S1435	S1436	S1437	S1438	S1439	S1440		
		RGB=0	RGB=1		RGB=0	RGB=1			RGB=0	RGB=1		RGB=0	RGB=1			
RA															SA	
MY=0	MY=1														ML=0	ML=1
0	639	R0 7-0	G0 7-0	B0 7-0	R1 7-0	G1 7-0	B1 7-0	---	R358 7-0	G358 7-0	B358 7-0	R359 7-0	G359 7-0	B359 7-0	0	639
1	638							---							1	638
2	637							---							2	637
3	636							---							3	636
4	635							---							4	635
5	634							---							5	634
6	633							---							6	633
7	632							---							7	632
8	631							---							8	631
9	630							---							9	630
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
632	7							---							632	7
633	6							---							633	6
634	5							---							634	5
635	4							---							635	4
636	3							---							636	3
637	2							---							637	2
638	1							---							638	1
639	0							---							639	0
CA	MX=0	0			1			---	358			359				
	MX=1	359			358			---	1			0				

Note:RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB=Red,Green and Blue pixel position change

Table 5.6: Memory map of 360RGB x640 resolution

5.3.6 480RGB x 720 resolution

R36h: B5=0

Source Out		S1	S2	S3	S4	S5	S6	---	S1435	S1436	S1437	S1438	S1439	S1440		
		RGB=0	RGB=1		RGB=0	RGB=1			RGB=0	RGB=1		RGB=0	RGB=1			
RA															SA	
MY=0	MY=1														ML=0	ML=1
0	719	R0 7-0	G0 7-0	B0 7-0	R1 7-0	G1 7-0	B1 7-0	---	R478 7-0	G478 7-0	B478 7-0	R479 7-0	G479 7-0	B479 7-0	0	719
1	718							---							1	718
2	717							---							2	717
3	716							---							3	716
4	715							---							4	715
5	714							---							5	714
6	713							---							6	713
7	712							---							7	712
8	711							---							8	711
9	710							---							9	710
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
712	7							---							712	7
713	6							---							713	6
714	5							---							714	5
715	4							---							715	4
716	3							---							716	3
717	2							---							717	2
718	1							---							718	1
719	0							---							719	0
CA	MX=0	0			1			---	478			479				
	MX=1	479			478			---	1			0				

Note:RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB=Red,Green and Blue pixel position change

Table 5.7: Memory map of 480RGB x 720 resolution

5.4 MCU to memory write / read direction

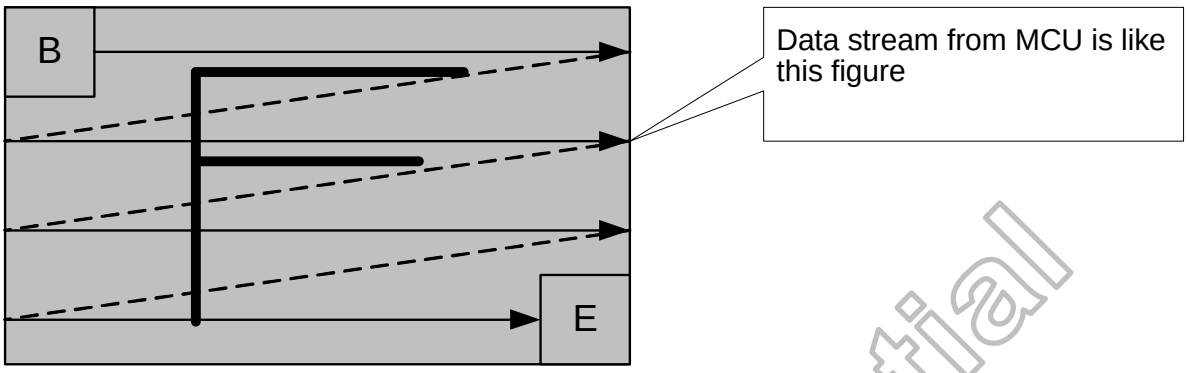


Figure 5.1: MCU to Memory write / read direction

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by "Memory Access Control" Command, Bits MY, MX, MV as described below.

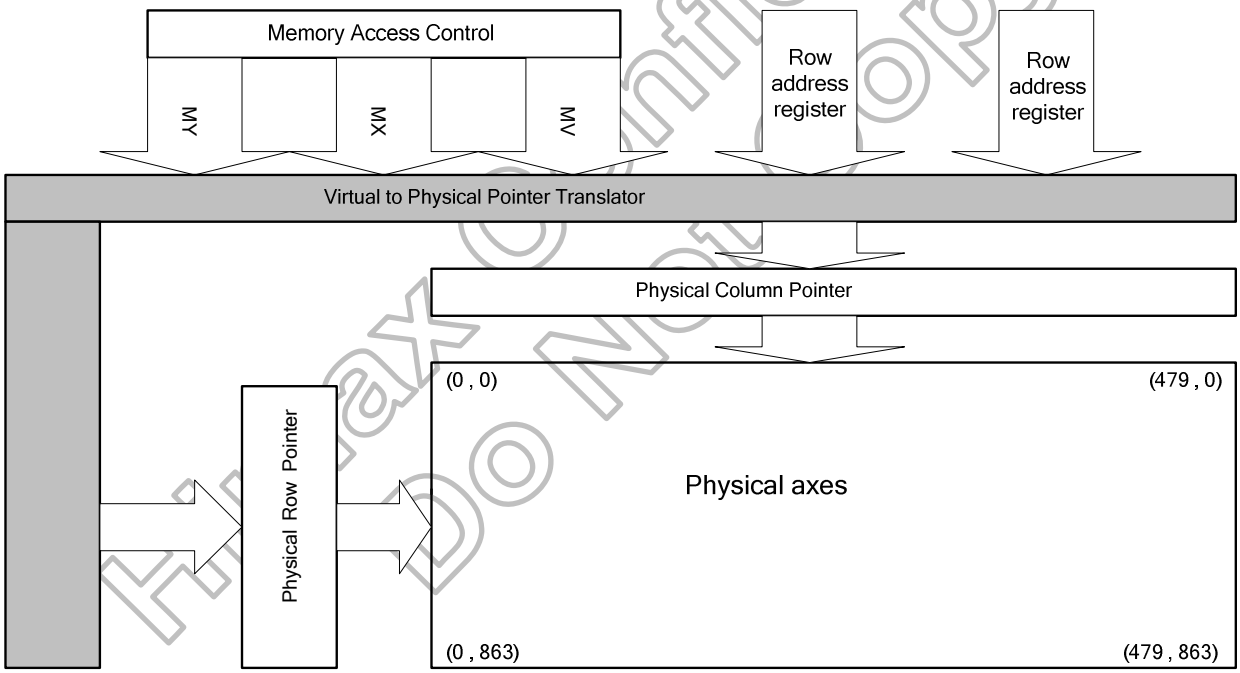


Figure 5.2: MY, MX, MV setting of 480RGB x 864 dot

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (863-Physical Row Pointer) with SC
0	1	0	Direct to (479-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (479-Physical Column Pointer)	Direct to (863-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (863-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (479-Physical Column Pointer)
1	1	1	Direct to (863-Physical Row Pointer)	Direct to (479-Physical Column Pointer)

Figure 5.3: MY, MX, MV setting of 480RGB x 864 dot

The following figure depicts the update method set by MV, MX and MY bit.

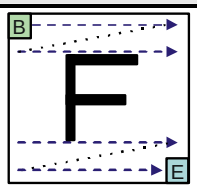
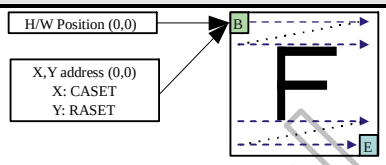
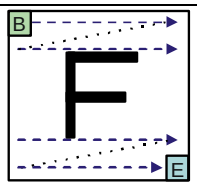
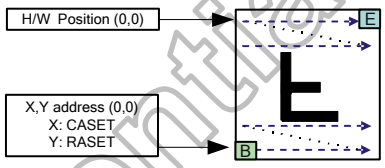
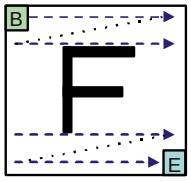
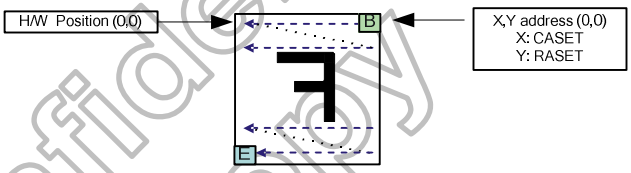
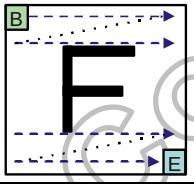
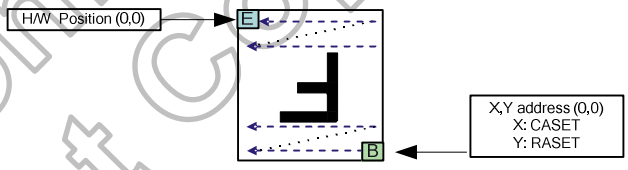
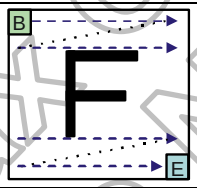
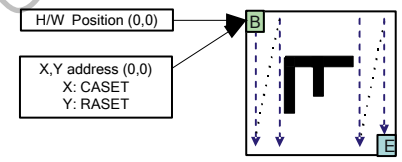
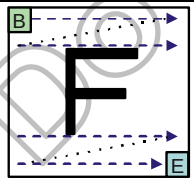
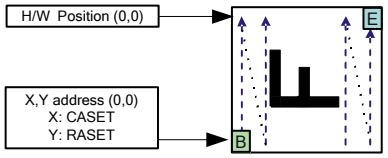
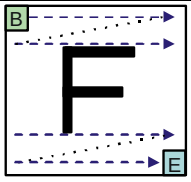
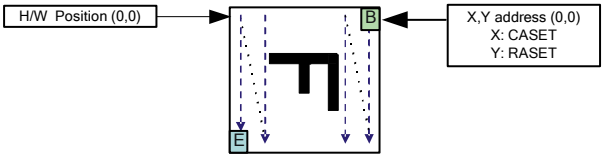
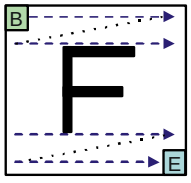
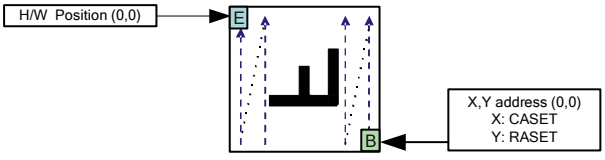
Display Data Direction	Memory Access Control			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 5.4: Address direction settings

5.5 Fully display, partial display, vertical scrolling display

5.5.1 Fully display

Example: (1) 480RGBx864 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x1DFh (R2Ah) and SP=0x000h, EP=0x35Fh (R2Bh), ML=0.

GRAM	000h DB---DB 23 ---0	001h DB---DB 23 ---0	---------	1DEh DB---DB 23 ---0	1DFh DB---DB 23 ---0
000h	000000H	000001H	---------	0001DEH	0001DFH
001h	001000H	001001H	---------	0011DEH	0011DFH
002h	002000H	002001H	---------	0021DEH	0021DFH
003h	003000H	003001H	---------	0031DEH	0031DFH
004h	004000H	004001H	---------	0041DEH	0041DFH
005h	005000H	005001H	---------	0051DEH	0051DFH
⋮	⋮	⋮	---------	⋮	⋮
35Ah	35A000H	35A001H	---------	35A1DEH	35A1DFH
35Bh	35B000H	35B001H	---------	35B1DEH	35B1DFH
35Ch	35C000H	35C001H	---------	35C1DEH	35C1DFH
35Dh	35D000H	35D001H	---------	35D1DEH	35D1DFH
35Eh	35E000H	35E001H	---------	35E1DEH	35E1DFH
35Fh	35F000H	35F001H	---------	35F1DEH	35F1DFH

Table 5.8: 480RGB x 864 resolution (SRAM assignment)

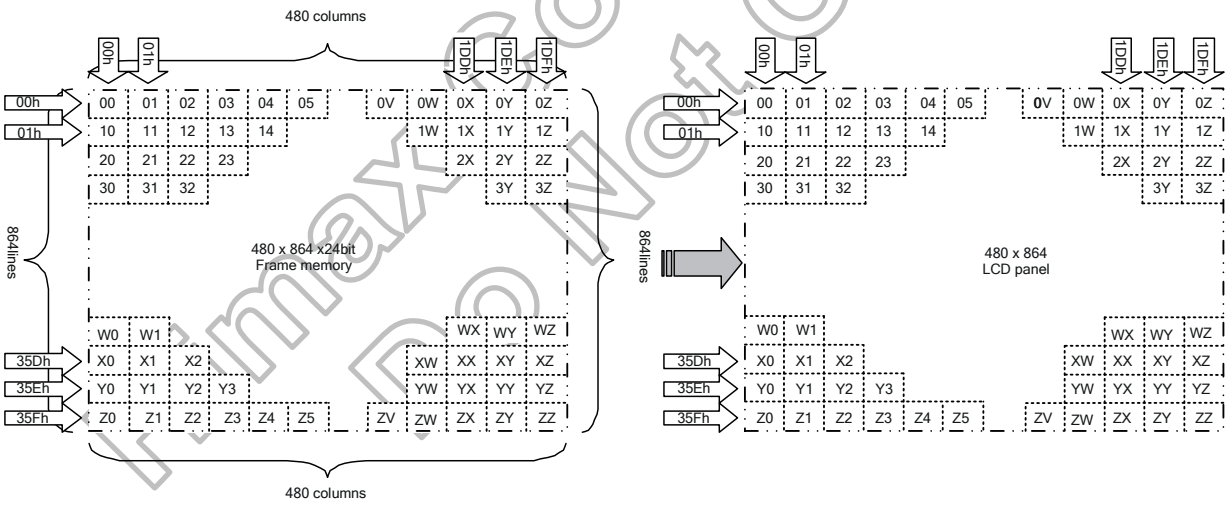


Figure 5.5: 480RGB x 864 resolution

Example: (1) 480RGBx854 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x1DFh (R2Ah) and SP=0x000h, EP=0x355h (R2Bh), ML=0.

GRAM	000h	001h	---	1DEh	1DFh
	DB---DB 23 ---0	DB---DB 23 ---0	---	DB---DB 23 ---0	DB---DB 23 ---0
000h	000000H	000001H	---	0001DEH	0001DFH
001h	001000H	001001H	---	0011DEH	0011DFH
002h	002000H	002001H	---	0021DEH	0021DFH
003h	003000H	003001H	---	0031DEH	0031DFH
004h	004000H	004001H	---	0041DEH	0041DFH
005h	005000H	005001H	---	0051DEH	0051DFH
⋮	⋮	⋮	---	⋮	⋮
350h	350000H	350001H	---	3501DEH	3501DFH
351h	351000H	351001H	---	3511DEH	3511DFH
352h	352000H	352001H	---	3521DEH	3521DFH
353h	353000H	353001H	---	3531DEH	3531DFH
354h	354000H	354001H	---	3541DEH	3541DFH
355h	355000H	355001H	---	3551DEH	3551DFH

Table 5.9: 480RGB x 854 resolution (SRAM assignment)

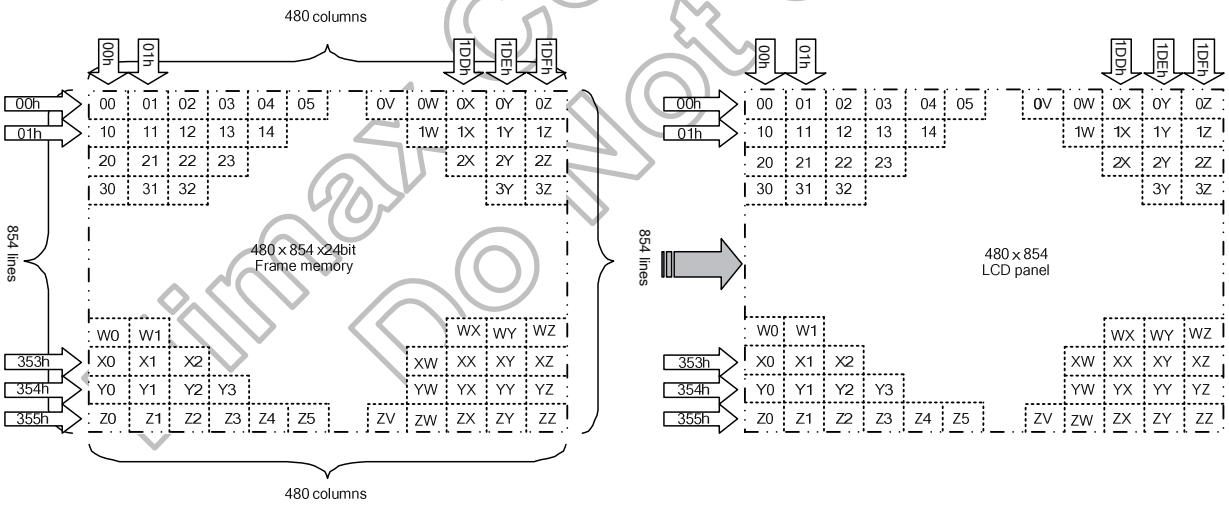


Figure 5.6: 480RGB x 854 resolution

Example: (1) 480RGBx800 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x1DFh (R2Ah) and SP=0x000h, EP=0x31Fh (R2Bh), ML=0.

GRAM	000h DB---DB 23 ---0	001h DB---DB 23 ---0	---------	1DEh DB---DB 23 ---0	1DFh DB---DB 23 ---0
000h	000000H	000001H	---------	0001DEH	0001DFH
001h	001000H	001001H	---------	0011DEH	0011DFH
002h	002000H	002001H	---------	0021DEH	0021DFH
003h	003000H	003001H	---------	0031DEH	0031DFH
004h	004000H	004001H	---------	0041DEH	0041DFH
005h	005000H	005001H	---------	0051DEH	0051DFH
⋮	⋮	⋮	---------	⋮	⋮
31Ah	31A000H	31A001H	---------	31A1DEH	31A1DFH
31Bh	31B000H	31B001H	---------	31B1DEH	31B1DFH
31Ch	31C000H	31C001H	---------	31C1DEH	31C1DFH
31Dh	31D000H	31D001H	---------	31D1DEH	31D1DFH
31Eh	31E000H	31E001H	---------	31E1DEH	31E1DFH
31Fh	31F000H	31F001H	---------	31F1DEH	31F1DFH

Table 5.10: 480RGB x 800 resolution (SRAM assignment)

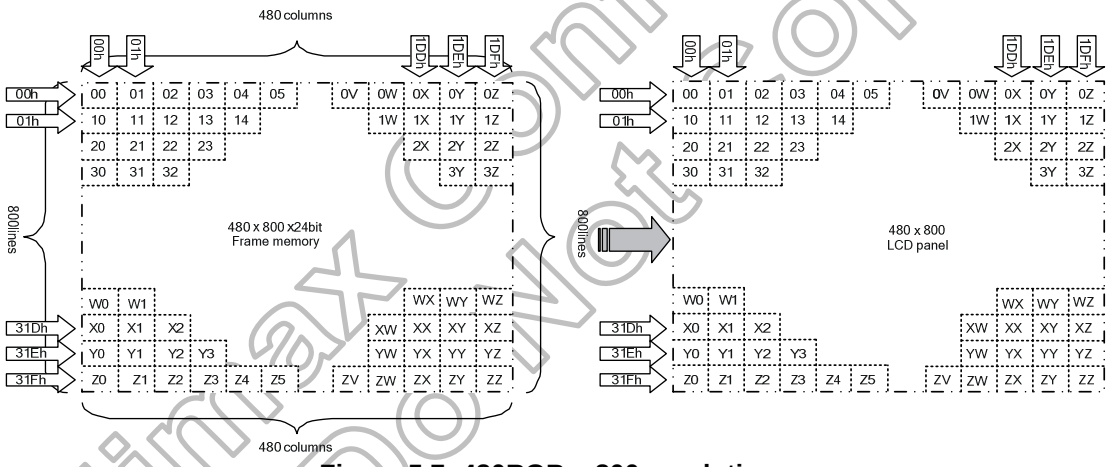


Figure 5.7: 480RGB x 800 resolution

Example: (1) 480RGBx640 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x1DFh (R2Ah) and SP=0x000h, EP=0x27Fh (R2Bh), ML=0.

GRAM	000h DB---DB 23 ---0	001h DB---DB 23 ---0	---------	1DEh DB---DB 23 ---0	1DFh DB---DB 23 ---0
000h	000000H	000001H	---------	0001DEH	0001DFH
001h	001000H	001001H	---------	0011DEH	0011DFH
002h	002000H	002001H	---------	0021DEH	0021DFH
003h	003000H	003001H	---------	0031DEH	0031DFH
004h	004000H	004001H	---------	0041DEH	0041DFH
005h	005000H	005001H	---------	0051DEH	0051DFH
⋮	⋮	⋮	---------	⋮	⋮
27Ah	27A000H	27A001H	---------	27A1DEH	27A1DFH
27Bh	27B000H	27B001H	---------	27B1DEH	27B1DFH
27Ch	27C000H	27C001H	---------	27C1DEH	27C1DFH
27Dh	27D000H	27D001H	---------	27D1DEH	27D1DFH
27Eh	27E000H	27E001H	---------	27E1DEH	27E1DFH
27Fh	27F000H	27F001H	---------	27F1DEH	27F1DFH

Table 5.11: 480RGB x 640 resolution (SRAM assignment)

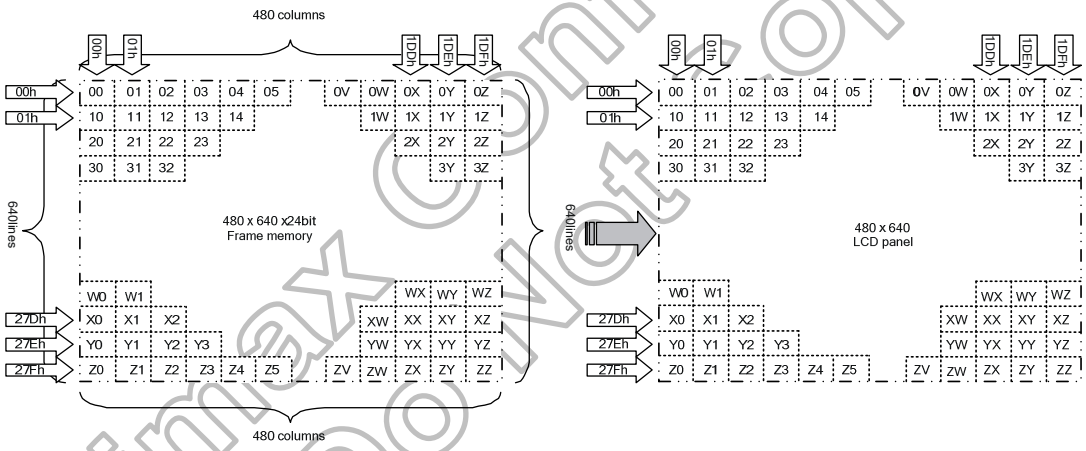


Figure 5.8: 480RGB x 640 resolution

Example: (1) 360RGBx640 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x167h (R2Ah) and SP=0x000h, EP=0x27Fh (R2Bh), ML=0.

GRAM	000h DB---DB 23 ---0	001h DB---DB 23 ---0	--------- ---------	166h DB---DB 23 ---0	167h DB---DB 23 ---0
000h	000000H	000001H	---------	000166H	000167H
001h	001000H	001001H	---------	001166H	001167H
002h	002000H	002001H	---------	002166H	002167H
003h	003000H	003001H	---------	003166H	003167H
004h	004000H	004001H	---------	004166H	004167H
005h	005000H	005001H	---------	005166H	005167H
⋮	⋮	⋮	---------	⋮	⋮
27Ah	27A000H	27A001H	---------	27A166H	27A167H
27Bh	27B000H	27B001H	---------	27B166H	27B167H
27Ch	27C000H	27C001H	---------	27C166H	27C167H
27Dh	27D000H	27D001H	---------	27D166H	27D167H
27Eh	27E000H	27E001H	---------	27E166H	27E167H
27Fh	27F000H	27F001H	---------	27F166H	27F167H

Table 5.12: 360RGB x 640 resolution (SRAM assignment)

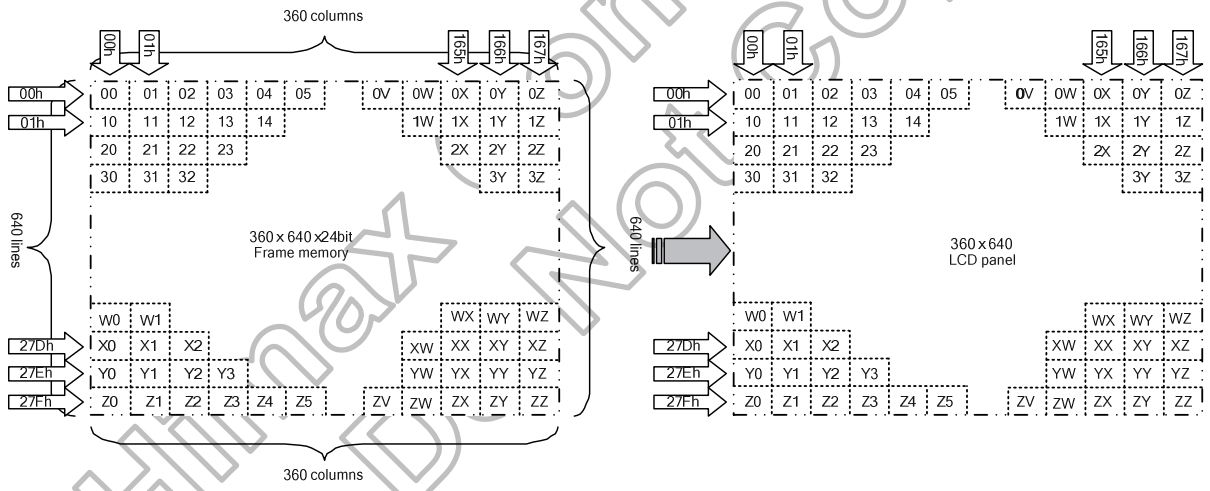


Figure 5.9: 360RGB x 640 resolution

Example: (1) 480RGBx720 dot display mode.
(2) NORON (Normal Display Mode On) instruction (R13h).
(3) SC=0x000h, EC=0x1DFh (R2Ah) and SP=0x000h, EP=0x2CFh (R2Bh), ML=0.

GRAM	000h DB---DB 23 ---0	001h DB---DB 23 ---0	---------	1DEh DB---DB 23 ---0	1DFh DB---DB 23 ---0
000h	000000H	000001H	---------	0001DEH	0001DFH
001h	001000H	001001H	---------	0011DEH	0011DFH
002h	002000H	002001H	---------	0021DEH	0021DFH
003h	003000H	003001H	---------	0031DEH	0031DFH
004h	004000H	004001H	---------	0041DEH	0041DFH
005h	005000H	005001H	---------	0051DEH	0051DFH
⋮	⋮	⋮	---------	⋮	⋮
2CAh	2CA000H	2CA001H	---------	2CA1DEH	2CA1DFH
2CBh	2CB000H	2CB001H	---------	2CB1DEH	2CB1DFH
2CCh	2CC000H	2CC001H	---------	2CC1DEH	2CC1DFH
2CDh	2CD000H	2CD001H	---------	2CD1DEH	2CD1DFH
2CEh	2CE000H	2CE001H	---------	2CE1DEH	2CE1DFH
2CFh	2CF000H	2CF001H	---------	2CF1DEH	2CF1DFH

Table 5.13: 480RGB x 720 resolution (SRAM assignment)

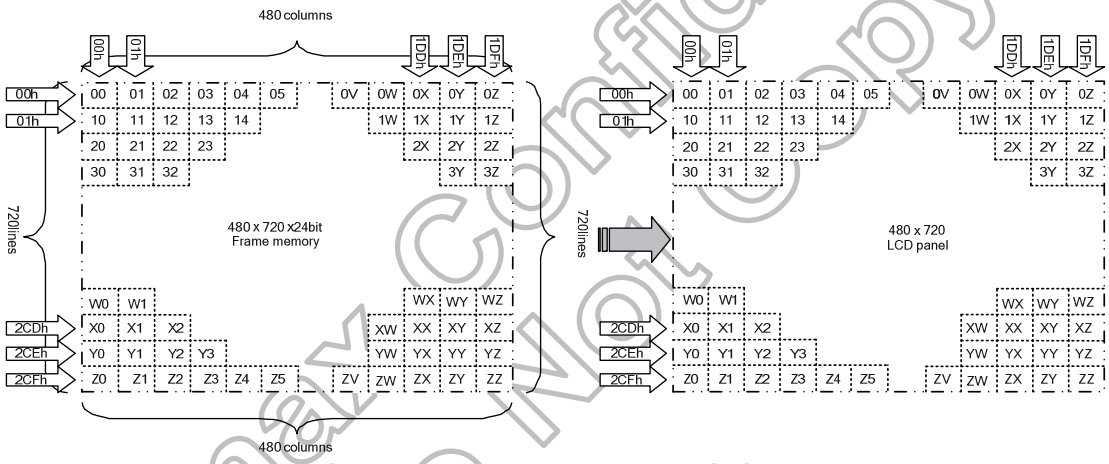


Figure 5.10: 480RGB x 720 resolution

5.5.2 Vertical scrolling display

The vertical scrolling display is specified by VSCRDEF instruction (R33h) and VSCRSADD instruction (R37h).

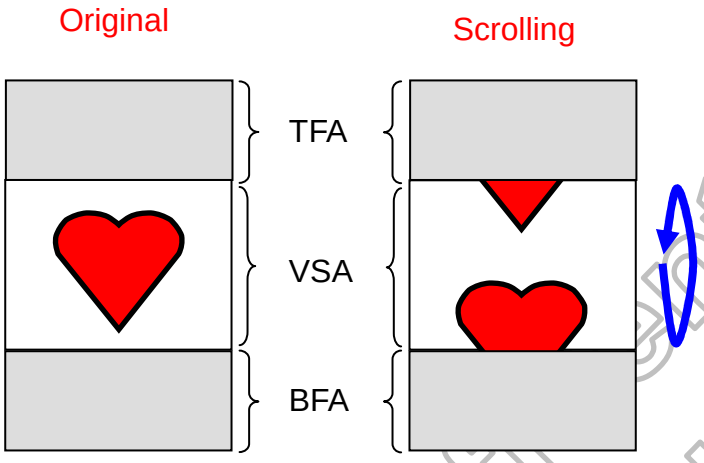


Figure 5.11: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=Panel total scan lines. In this case, scrolling is applied as shown below.

5.5.2.1 Example: 480RGB X 864

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=864. In this case, scrolling is applied as shown below.

Example (1) TFA=2, VSA=862, BFA=0 when MADCTL B4=0

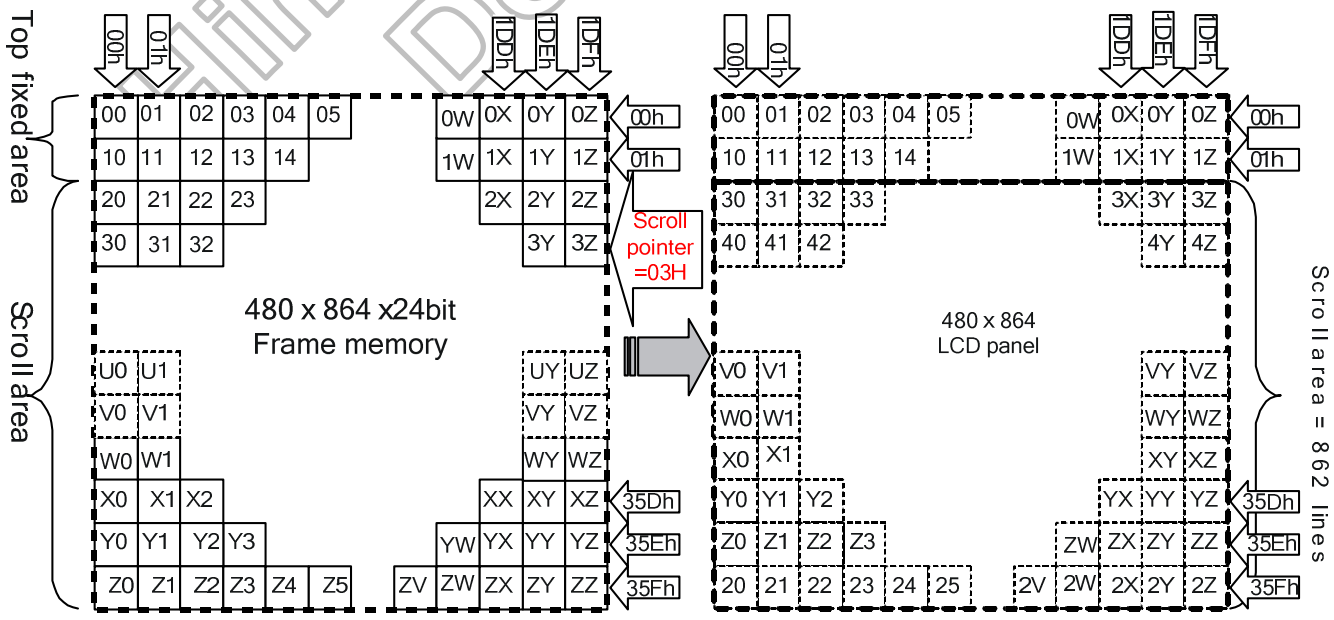


Figure 5.12: Memory map of vertical scrolling 1

Example (2) TFA=2, VSA=860, BFA=2 when MADCTL B4=0

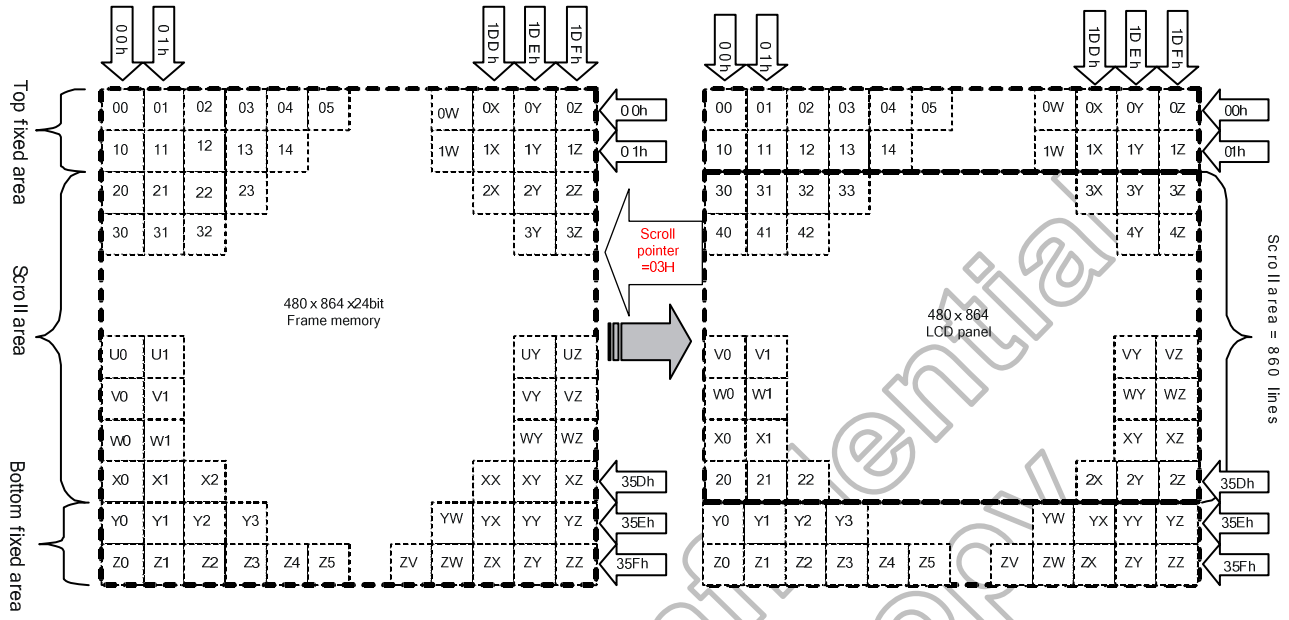


Figure 5.13: Memory map of vertical scrolling 2

5.5.2.2 Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

Case 1: TFA + VSA + BFA≠864
Do not set TFA + VSA + BFA≠864. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=864 (Scrolling)
Example (1) When TFA=0, VSA=864, BFA=0 and VSCRSADD=40.MADCTL parameter B4="0"

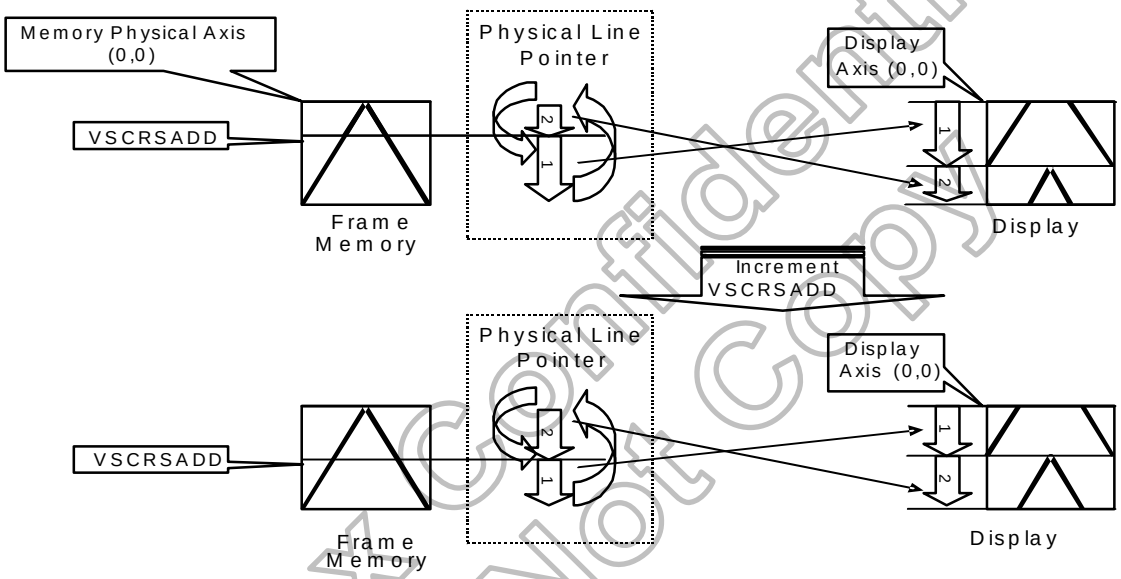


Figure 5.14: Vertical scroll example 1

Example (2) TFA=30, VSA=834, BFA=0 and VSCRSADD =80. MADCTRL parameter B4="1"

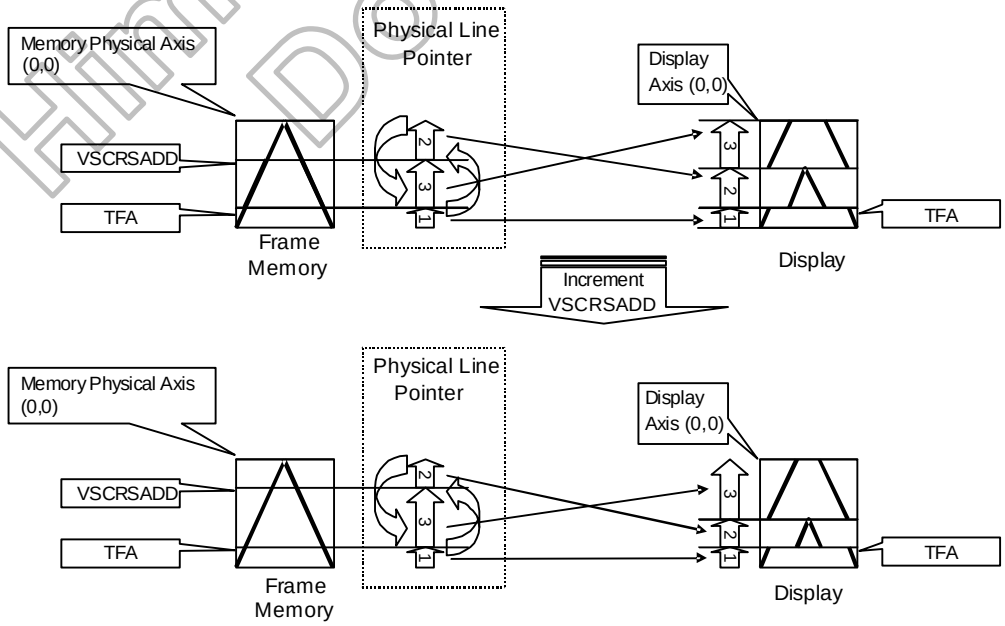


Figure 5.15: Vertical scroll example 2

5.5.3 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

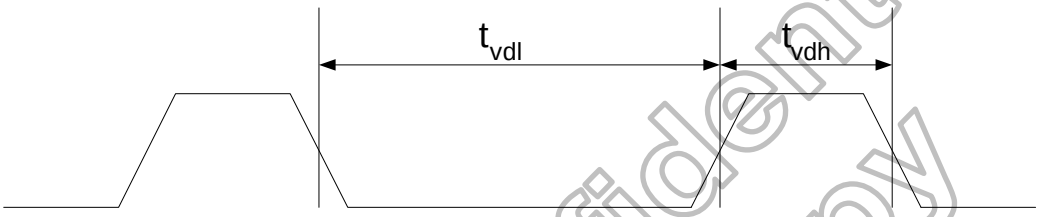


Figure 5.16: Tearing effect output line–mode 1

tvdh=The LCD display is not updated from the Frame Memory
tvdl=The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and N H-sync pulses per field.
N: If RES_SEL [2:0] set to = 3'b000, the resolution is 480 RGB X 864, the N=864.

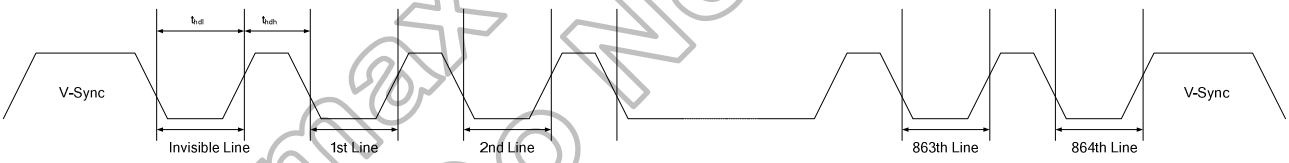
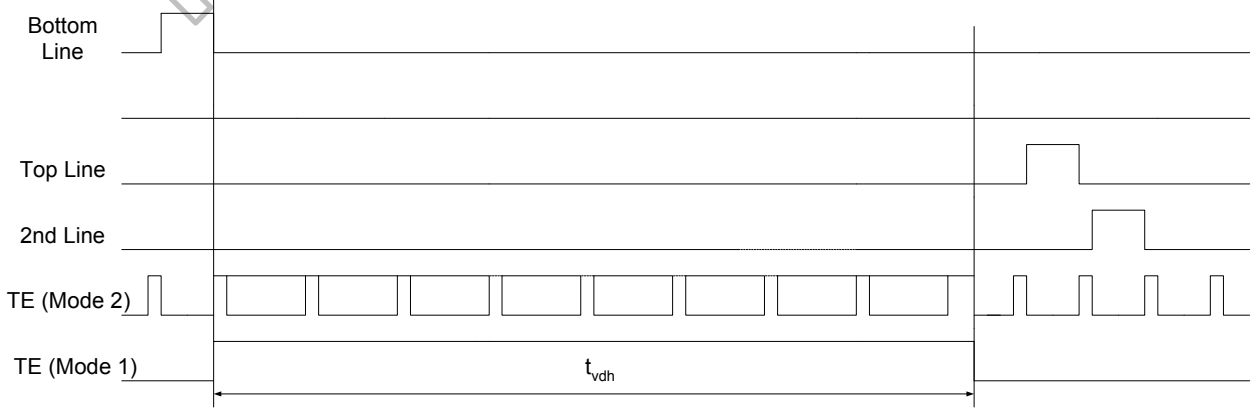


Figure 5.17: Tearing effect output line–mode 2

thdh=The LCD display is not updated from the Frame Memory
thdl=The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

Figure 5.18: Tearing effect output line–timing diagrm

5.5.3.1 Tearing effect line timing

The Tearing Effect signal is described below:

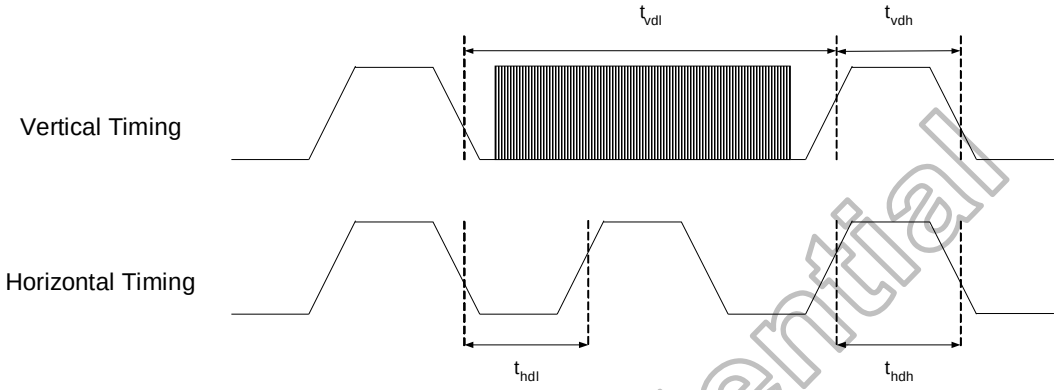


Figure 5.19: Tearing effect output line –tearing effect line timing

Idle Mode Off (Resolution 480x800 RGB, Frame Rate = 60.5 Hz)

Symbol	Parameter	Min.	Max.	Unit
tvdl	Vertical Timing Low Duration	15	-	ms
tvdh	Vertical Timing High Duration	1000	-	us
thdl	Horizontal Timing Low Duration	18	-	us
thdh	Horizontal Timing High Duration	0.13	500	us
tr	Rise time	-	15	ns
tf	Fall time	-	15	ns

Note: The timings in Table 5.13 apply when MADCTL ML=0 and ML=1

Table 5.14: AC characteristics of tearing effect signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

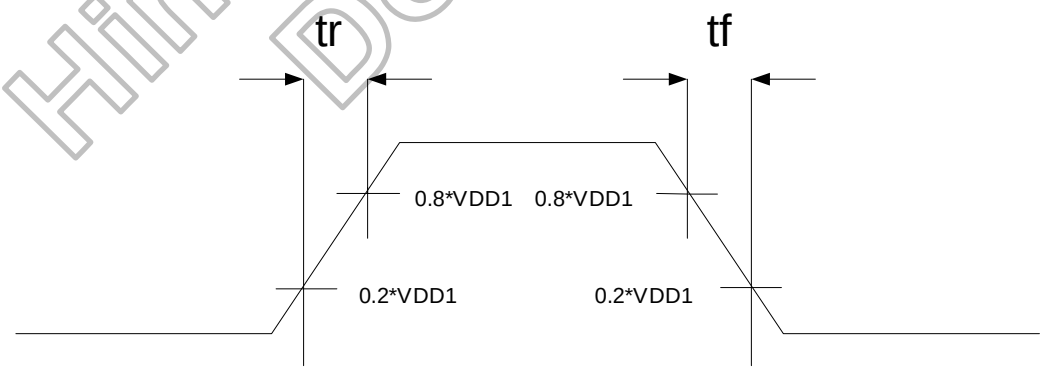


Figure 5.20: Tearing effect output line–definition of tf, tr

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect.

Example 1: MPU write is faster than panel read.

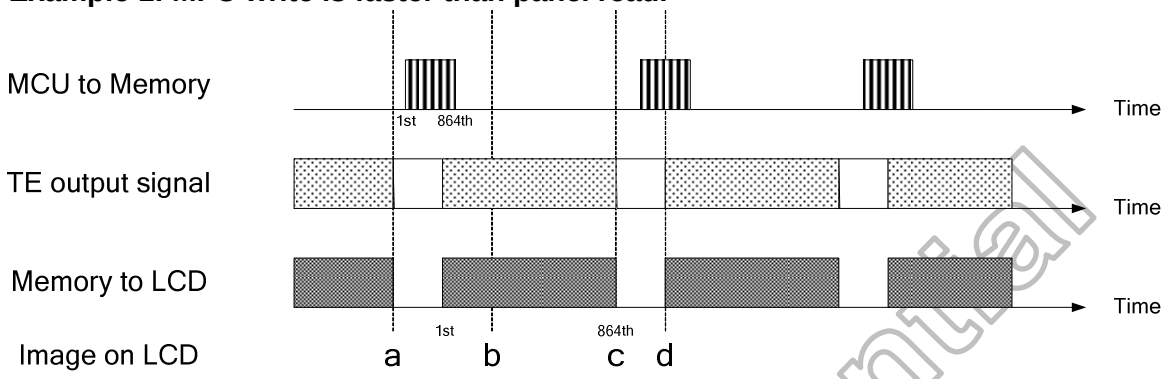


Figure 5.21: Tearing effect output line–example 1 (Timing)

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

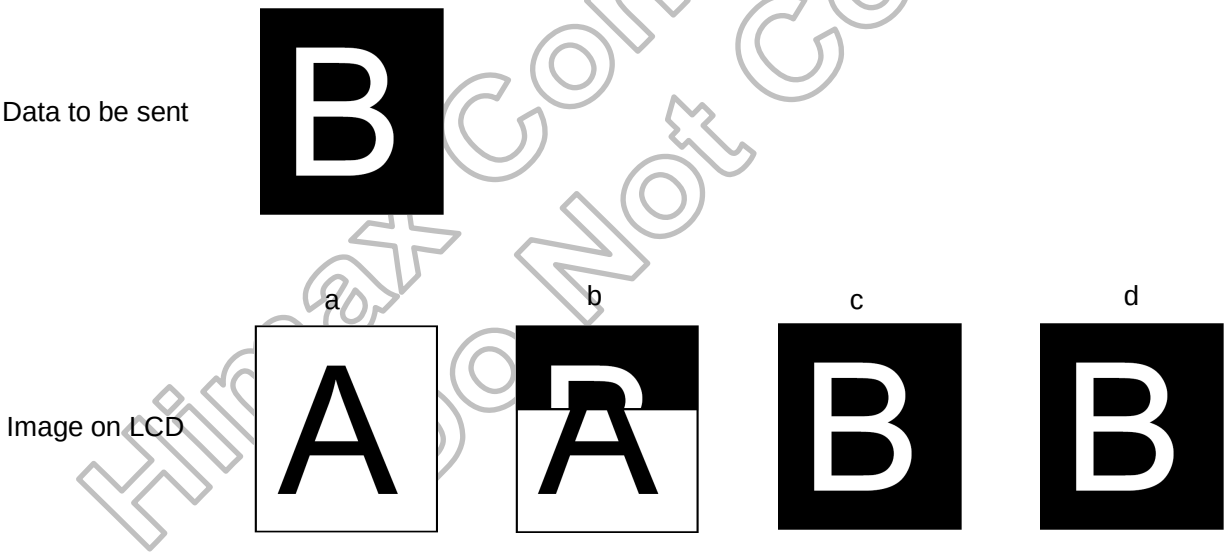


Figure 5.22: Tearing effect output line–example 1 (Image)

Example 2: MPU write is slower than panel read.

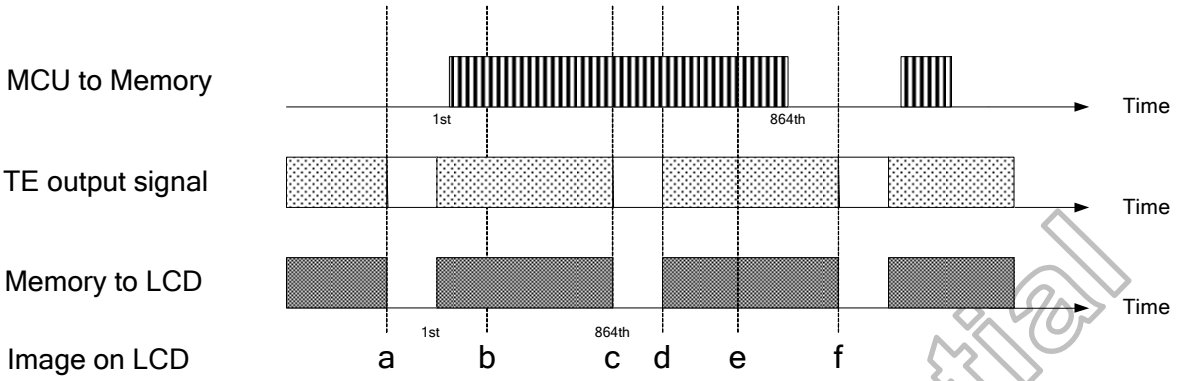


Figure 5.23: Tearing effect output line–example 2 (Timing)

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.

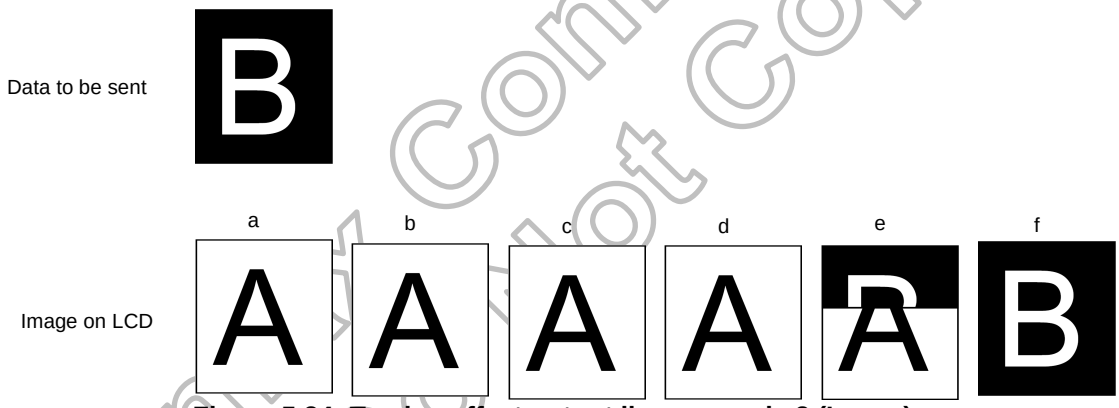


Figure 5.24: Tearing effect output line–example 2 (Image)

5.6 Color depth conversion

5.6.1 Color depth conversion Look-up tables

R input (5-bit) 16-bit / pixel mode 65,536 colours	R input (6-bit) 18-bit / pixel mode 262,144 colours	R output (8-bit) 24-bit / pixel mode 16,777,216 colours	RGBSET Parameter
00000	000000	R_{007} $R_{006}R_{005}$ $R_{004}R_{003}R_{002}R_{001}R_{000}$	1
00001	000001	$R_{017}R_{016}R_{015}R_{014}R_{013}R_{012}R_{011}R_{010}$	2
00010	000010	$R_{027}R_{026}R_{025}R_{024}R_{023}R_{022}R_{021}R_{020}$	3
00011	000011	$R_{037}R_{036}R_{035}R_{034}R_{033}R_{032}R_{031}R_{030}$	4
00100	000100	$R_{047}R_{046}R_{045}R_{044}R_{043}R_{042}R_{041}R_{040}$	5
00101	000101	$R_{057}R_{056}R_{055}R_{054}R_{053}R_{052}R_{051}R_{050}$	6
00110	000110	$R_{067}R_{066}R_{065}R_{064}R_{063}R_{062}R_{061}R_{060}$	7
00111	000111	$R_{077}R_{076}R_{075}R_{074}R_{073}R_{072}R_{071}R_{070}$	8
01000	001000	$R_{087}R_{086}R_{085}R_{084}R_{083}R_{082}R_{081}R_{080}$	9
01001	001001	$R_{097}R_{096}R_{095}R_{094}R_{093}R_{092}R_{091}R_{090}$	10
01010	001010	$R_{107}R_{106}R_{105}R_{104}R_{103}R_{102}R_{101}R_{100}$	11
01011	001011	$R_{117}R_{116}R_{115}R_{114}R_{113}R_{112}R_{111}R_{110}$	12
01100	001100	$R_{127}R_{126}R_{125}R_{124}R_{123}R_{122}R_{121}R_{120}$	13
01101	001101	$R_{137}R_{136}R_{135}R_{134}R_{133}R_{132}R_{131}R_{130}$	14
01110	001110	$R_{147}R_{146}R_{145}R_{144}R_{143}R_{142}R_{141}R_{140}$	15
01111	001111	$R_{157}R_{156}R_{155}R_{154}R_{153}R_{152}R_{151}R_{150}$	16
10000	010000	R_{167} $R_{166}R_{165}$ $R_{164}R_{163}R_{162}R_{161}R_{160}$	17
10001	010001	$R_{177}R_{176}R_{175}R_{174}R_{173}R_{172}R_{171}R_{170}$	18
10010	010010	$R_{187}R_{186}R_{185}R_{184}R_{183}R_{182}R_{181}R_{180}$	19
10011	010011	$R_{197}R_{196}R_{195}R_{194}R_{193}R_{192}R_{191}R_{190}$	20
10100	010100	$R_{207}R_{206}R_{205}R_{204}R_{203}R_{202}R_{201}R_{200}$	21
10101	010101	$R_{217}R_{216}R_{215}R_{214}R_{213}R_{212}R_{211}R_{210}$	22
10110	010110	$R_{227}R_{226}R_{225}R_{224}R_{223}R_{222}R_{221}R_{220}$	23
10111	010111	$R_{237}R_{236}R_{235}R_{234}R_{233}R_{232}R_{231}R_{230}$	24
11000	011000	$R_{247}R_{246}R_{245}R_{244}R_{243}R_{242}R_{241}R_{240}$	25
11001	011001	$R_{257}R_{256}R_{255}R_{254}R_{253}R_{252}R_{251}R_{250}$	26
11010	011010	$R_{267}R_{266}R_{265}R_{264}R_{263}R_{262}R_{261}R_{260}$	27
11011	011011	$R_{277}R_{276}R_{275}R_{274}R_{273}R_{272}R_{271}R_{270}$	28
11100	011100	$R_{287}R_{286}R_{285}R_{284}R_{283}R_{282}R_{281}R_{280}$	29
11101	011101	$R_{297}R_{296}R_{295}R_{294}R_{293}R_{292}R_{291}R_{290}$	30
11110	011110	$R_{307}R_{306}R_{305}R_{304}R_{303}R_{302}R_{301}R_{300}$	31
11111	011111	$R_{317}R_{316}R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$	32

Table 5.15: Look-up tables-1

R input (5-bit) 16-bit / pixel mode 65,536 colours	R input (6-bit) 18-bit / pixel mode 262,144 colours	R output (8-bit) 24-bit / pixel mode 16,777,216 colours	RGBSET Parameter
No Input	100000	R_{327} $R_{326}R_{325}$ $R_{324}R_{323}R_{322}R_{321}R_{320}$	33
No Input	100001	$R_{337}R_{336}R_{335}R_{334}R_{333}R_{332}R_{331}R_{330}$	34
No Input	100010	$R_{347}R_{346}R_{345}R_{344}R_{343}R_{342}R_{341}R_{340}$	35
No Input	100011	$R_{357}R_{356}R_{355}R_{354}R_{353}R_{352}R_{351}R_{350}$	36
No Input	100100	$R_{367}R_{366}R_{365}R_{364}R_{363}R_{362}R_{361}R_{360}$	37
No Input	100101	$R_{377}R_{376}R_{375}R_{374}R_{373}R_{372}R_{371}R_{370}$	38
No Input	100110	$R_{387}R_{386}R_{385}R_{384}R_{383}R_{382}R_{381}R_{380}$	39
No Input	100111	$R_{397}R_{396}R_{395}R_{394}R_{393}R_{392}R_{391}R_{390}$	40
No Input	101000	$R_{407}R_{406}R_{405}R_{404}R_{403}R_{402}R_{401}R_{400}$	41
No Input	101001	$R_{417}R_{416}R_{415}R_{414}R_{413}R_{412}R_{411}R_{410}$	42
No Input	101010	$R_{427}R_{426}R_{425}R_{424}R_{423}R_{422}R_{421}R_{420}$	43
No Input	101011	$R_{437}R_{436}R_{435}R_{434}R_{433}R_{432}R_{431}R_{430}$	44
No Input	101100	$R_{447}R_{446}R_{445}R_{444}R_{443}R_{442}R_{441}R_{440}$	45
No Input	101101	$R_{457}R_{456}R_{455}R_{454}R_{453}R_{452}R_{451}R_{450}$	46
No Input	101110	$R_{467}R_{466}R_{465}R_{464}R_{463}R_{462}R_{461}R_{460}$	47
No Input	101111	$R_{477}R_{476}R_{475}R_{474}R_{473}R_{472}R_{471}R_{470}$	48
No Input	110000	R_{487} $R_{486}R_{485}$ $R_{484}R_{483}R_{482}R_{481}R_{480}$	49
No Input	110001	$R_{497}R_{496}R_{495}R_{494}R_{493}R_{492}R_{491}R_{490}$	50
No Input	110010	$R_{507}R_{506}R_{505}R_{504}R_{503}R_{502}R_{501}R_{500}$	51
No Input	110011	$R_{517}R_{516}R_{515}R_{514}R_{513}R_{512}R_{511}R_{510}$	52
No Input	110100	$R_{527}R_{526}R_{525}R_{524}R_{523}R_{522}R_{521}R_{520}$	53
No Input	110101	$R_{537}R_{536}R_{535}R_{534}R_{533}R_{532}R_{531}R_{530}$	54
No Input	110110	$R_{547}R_{546}R_{545}R_{544}R_{543}R_{542}R_{541}R_{540}$	55
No Input	110111	$R_{557}R_{556}R_{555}R_{554}R_{553}R_{552}R_{551}R_{550}$	56
No Input	111000	$R_{567}R_{566}R_{565}R_{564}R_{563}R_{562}R_{561}R_{560}$	57
No Input	111001	$R_{577}R_{576}R_{575}R_{574}R_{573}R_{572}R_{571}R_{570}$	58
No Input	111010	$R_{587}R_{586}R_{585}R_{584}R_{583}R_{582}R_{581}R_{580}$	59
No Input	111011	$R_{597}R_{596}R_{595}R_{594}R_{593}R_{592}R_{591}R_{590}$	60
No Input	111100	$R_{607}R_{606}R_{605}R_{604}R_{603}R_{602}R_{601}R_{600}$	61
No Input	111101	$R_{617}R_{616}R_{615}R_{614}R_{613}R_{612}R_{611}R_{610}$	62
No Input	111110	$R_{627}R_{626}R_{625}R_{624}R_{623}R_{622}R_{621}R_{620}$	63
No Input	111111	$R_{637}R_{636}R_{635}R_{634}R_{633}R_{632}R_{631}R_{630}$	64

Table 5.16: Look-up tables-2

G input (5-bit) 16-bit / pixel mode 65,536 colours	G input (6-bit) 18-bit / pixel mode 262,144 colours	G output (8-bit) 24-bit / pixel mode 16,777,216 colours	RGBSET Parameter
000000	000000	G_{007} $G_{006}G_{005}$ $G_{004}G_{003}G_{002}G_{001}G_{000}$	65
000001	000001	$G_{017}G_{016}G_{015}G_{014}G_{013}G_{012}G_{011}G_{010}$	66
000010	000010	$G_{027}G_{026}G_{025}G_{024}G_{023}G_{022}G_{021}G_{020}$	67
000011	000011	$G_{037}G_{036}G_{035}G_{034}G_{033}G_{032}G_{031}G_{030}$	68
000100	000100	$G_{047}G_{046}G_{045}G_{044}G_{043}G_{042}G_{041}G_{040}$	69
000101	000101	$G_{057}G_{056}G_{055}G_{054}G_{053}G_{052}G_{051}G_{050}$	70
000110	000110	$G_{067}G_{066}G_{065}G_{064}G_{063}G_{062}G_{061}G_{060}$	71
000111	000111	$G_{077}G_{076}G_{075}G_{074}G_{073}G_{072}G_{071}G_{070}$	72
001000	001000	$G_{087}G_{086}G_{085}G_{084}G_{083}G_{082}G_{081}G_{080}$	73
001001	001001	$G_{097}G_{096}G_{095}G_{094}G_{093}G_{092}G_{091}G_{090}$	74
001010	001010	$G_{107}G_{106}G_{105}G_{104}G_{103}G_{102}G_{101}G_{100}$	75
001011	001011	$G_{117}G_{116}G_{115}G_{114}G_{113}G_{112}G_{111}G_{110}$	76
001100	001100	$G_{127}G_{126}G_{125}G_{124}G_{123}G_{122}G_{121}G_{120}$	77
001101	001101	$G_{137}G_{136}G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$	78
001110	001110	$G_{147}G_{146}G_{145}G_{144}G_{143}G_{142}G_{141}G_{140}$	79
001111	001111	$G_{157}G_{156}G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$	80
010000	010000	G_{167} $G_{166}G_{165}$ $G_{164}G_{163}G_{162}G_{161}G_{160}$	81
010001	010001	$G_{177}G_{176}G_{175}G_{174}G_{173}G_{172}G_{171}G_{170}$	82
010010	010010	$G_{187}G_{186}G_{185}G_{184}G_{183}G_{182}G_{181}G_{180}$	83
010011	010011	$G_{197}G_{196}G_{195}G_{194}G_{193}G_{192}G_{191}G_{190}$	84
010100	010100	$G_{207}G_{206}G_{205}G_{204}G_{203}G_{202}G_{201}G_{200}$	85
010101	010101	$G_{217}G_{216}G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$	86
010110	010110	$G_{227}G_{226}G_{225}G_{224}G_{223}G_{222}G_{221}G_{220}$	87
010111	010111	$G_{237}G_{236}G_{235}G_{234}G_{233}G_{232}G_{231}G_{230}$	88
011000	011000	$G_{247}G_{246}G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$	89
011001	011001	$G_{257}G_{256}G_{255}G_{254}G_{253}G_{252}G_{251}G_{250}$	90
011010	011010	$G_{267}G_{266}G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$	91
011011	011011	$G_{277}G_{276}G_{275}G_{274}G_{273}G_{272}G_{271}G_{270}$	92
011100	011100	$G_{287}G_{286}G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$	93
011101	011101	$G_{297}G_{296}G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$	94
011110	011110	$G_{307}G_{306}G_{305}G_{304}G_{303}G_{302}G_{301}G_{300}$	95
011111	011111	$G_{317}G_{316}G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$	96

Table 5.17: Look-up tables-3

G input (5-bit) 16-bit / pixel mode 65,536 colours	G input (6-bit) 18-bit / pixel mode 262,144 colours	G output (8-bit) 24-bit / pixel mode 16,777,216 colours	RGBSET Parameter
100000	100000	G_{327} $G_{326}G_{325}$ $G_{324}G_{323}G_{322}G_{321}G_{320}$	97
100001	100001	$G_{337}G_{336}G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$	98
100010	100010	$G_{347}G_{346}G_{345}G_{344}G_{343}G_{342}G_{341}G_{340}$	99
100011	100011	$G_{357}G_{356}G_{355}G_{354}G_{353}G_{352}G_{351}G_{350}$	100
100100	100100	$G_{367}G_{366}G_{365}G_{364}G_{363}G_{362}G_{361}G_{360}$	101
100101	100101	$G_{377}G_{376}G_{375}G_{374}G_{373}G_{372}G_{371}G_{370}$	102
100110	100110	$G_{387}G_{386}G_{385}G_{384}G_{383}G_{382}G_{381}G_{380}$	103
100111	100111	$G_{397}G_{396}G_{395}G_{394}G_{393}G_{392}G_{391}G_{390}$	104
101000	101000	$G_{407}G_{406}G_{405}G_{404}G_{403}G_{402}G_{401}G_{400}$	105
101001	101001	$G_{417}G_{416}G_{415}G_{414}G_{413}G_{412}G_{411}G_{410}$	106
101010	101010	$G_{427}G_{426}G_{425}G_{424}G_{423}G_{422}G_{421}G_{420}$	107
101011	101011	$G_{437}G_{436}G_{435}G_{434}G_{433}G_{432}G_{431}G_{430}$	108
101100	101100	$G_{447}G_{446}G_{445}G_{444}G_{443}G_{442}G_{441}G_{440}$	109
101101	101101	$G_{457}G_{456}G_{455}G_{454}G_{453}G_{452}G_{451}G_{450}$	110
101110	101110	$G_{467}G_{466}G_{465}G_{464}G_{463}G_{462}G_{461}G_{460}$	111
101111	101111	$G_{477}G_{476}G_{475}G_{474}G_{473}G_{472}G_{471}G_{470}$	112
110000	110000	G_{487} $G_{486}G_{485}$ $G_{484}G_{483}G_{482}G_{481}G_{480}$	113
110001	110001	$G_{497}G_{496}G_{495}G_{494}G_{493}G_{492}G_{491}G_{490}$	114
110010	110010	$G_{507}G_{506}G_{505}G_{504}G_{503}G_{502}G_{501}G_{500}$	115
110011	110011	$G_{517}G_{516}G_{515}G_{514}G_{513}G_{512}G_{511}G_{510}$	116
110100	110100	$G_{527}G_{526}G_{525}G_{524}G_{523}G_{522}G_{521}G_{520}$	117
110101	110101	$G_{537}G_{536}G_{535}G_{534}G_{533}G_{532}G_{531}G_{530}$	118
110110	110110	$G_{547}G_{546}G_{545}G_{544}G_{543}G_{542}G_{541}G_{540}$	119
110111	110111	$G_{557}G_{556}G_{555}G_{554}G_{553}G_{552}G_{551}G_{550}$	120
111000	111000	$G_{567}G_{566}G_{565}G_{564}G_{563}G_{562}G_{561}G_{560}$	121
111001	111001	$G_{577}G_{576}G_{575}G_{574}G_{573}G_{572}G_{571}G_{570}$	122
111010	111010	$G_{587}G_{586}G_{585}G_{584}G_{583}G_{582}G_{581}G_{580}$	123
111011	111011	$G_{597}G_{596}G_{595}G_{594}G_{593}G_{592}G_{591}G_{590}$	124
111100	111100	$G_{607}G_{606}G_{605}G_{604}G_{603}G_{602}G_{601}G_{600}$	125
111101	111101	$G_{617}G_{616}G_{615}G_{614}G_{613}G_{612}G_{611}G_{610}$	126
111110	111110	$G_{627}G_{626}G_{625}G_{624}G_{623}G_{622}G_{621}G_{620}$	127
111111	111111	$G_{637}G_{636}G_{635}G_{634}G_{633}G_{632}G_{631}G_{630}$	128

Table 5.18: Look-up tables-4

B input (5-bit) 16-bit / pixel mode 65,536 colours	B input (6-bit) 18-bit / pixel mode 262,144 colours	B output (8-bit) 24-bit / pixel mode 16,777,216 colours	RGBSET Parameter
00000	000000	B_{007} $B_{006}B_{005}$ $B_{004}B_{003}B_{002}B_{001}B_{000}$	129
00001	000001	$B_{017}B_{016}B_{015}B_{014}B_{013}B_{012}B_{011}B_{010}$	130
00010	000010	$B_{027}B_{026}B_{025}B_{024}B_{023}B_{022}B_{021}B_{020}$	131
00011	000011	$B_{037}B_{036}B_{035}B_{034}B_{033}B_{032}B_{031}B_{030}$	132
00100	000100	$B_{047}B_{046}B_{045}B_{044}B_{043}B_{042}B_{041}B_{040}$	133
00101	000101	$B_{057}B_{056}B_{055}B_{054}B_{053}B_{052}B_{051}B_{050}$	134
00110	000110	$B_{067}B_{066}B_{065}B_{064}B_{063}B_{062}B_{061}B_{060}$	135
00111	000111	$B_{077}B_{076}B_{075}B_{074}B_{073}B_{072}B_{071}B_{070}$	136
01000	001000	$B_{087}B_{086}B_{085}B_{084}B_{083}B_{082}B_{081}B_{080}$	137
01001	001001	$B_{097}B_{096}B_{095}B_{094}B_{093}B_{092}B_{091}B_{090}$	138
01010	001010	$B_{107}B_{106}B_{105}B_{104}B_{103}B_{102}B_{101}B_{100}$	139
01011	001011	$B_{117}B_{116}B_{115}B_{114}B_{113}B_{112}B_{111}B_{110}$	140
01100	001100	$B_{127}B_{126}B_{125}B_{124}B_{123}B_{122}B_{121}B_{120}$	141
01101	001101	$B_{137}B_{136}B_{135}B_{134}B_{133}B_{132}B_{131}B_{130}$	142
01110	001110	$B_{147}B_{146}B_{145}B_{144}B_{143}B_{142}B_{141}B_{140}$	143
01111	001111	$B_{157}B_{156}B_{155}B_{154}B_{153}B_{152}B_{151}B_{150}$	144
10000	010000	B_{167} $B_{166}B_{165}$ $B_{164}B_{163}B_{162}B_{161}B_{160}$	145
10001	010001	$B_{177}B_{176}B_{175}B_{174}B_{173}B_{172}B_{171}B_{170}$	146
10010	010010	$B_{187}B_{186}B_{185}B_{184}B_{183}B_{182}B_{181}B_{180}$	147
10011	010011	$B_{197}B_{196}B_{195}B_{194}B_{193}B_{192}B_{191}B_{190}$	148
10100	010100	$B_{207}B_{206}B_{205}B_{204}B_{203}B_{202}B_{201}B_{200}$	149
10101	010101	$B_{217}B_{216}B_{215}B_{214}B_{213}B_{212}B_{211}B_{210}$	150
10110	010110	$B_{227}B_{226}B_{225}B_{224}B_{223}B_{222}B_{221}B_{220}$	151
10111	010111	$B_{237}B_{236}B_{235}B_{234}B_{233}B_{232}B_{231}B_{230}$	152
11000	011000	$B_{247}B_{246}B_{245}B_{244}B_{243}B_{242}B_{241}B_{240}$	153
11001	011001	$B_{257}B_{256}B_{255}B_{254}B_{253}B_{252}B_{251}B_{250}$	154
11010	011010	$B_{267}B_{266}B_{265}B_{264}B_{263}B_{262}B_{261}B_{260}$	155
11011	011011	$B_{277}B_{276}B_{275}B_{274}B_{273}B_{272}B_{271}B_{270}$	156
11100	011100	$B_{287}B_{286}B_{285}B_{284}B_{283}B_{282}B_{281}B_{280}$	157
11101	011101	$B_{297}B_{296}B_{295}B_{294}B_{293}B_{292}B_{291}B_{290}$	158
11110	011110	$B_{307}B_{306}B_{305}B_{304}B_{303}B_{302}B_{301}B_{300}$	159
11111	011111	$B_{317}B_{316}B_{315}B_{314}B_{313}B_{312}B_{311}B_{310}$	160

Table 5.19: Look-up tables-5

B input (5-bit) 16-bit / pixel mode 65,536 colours	B input (6-bit) 18-bit / pixel mode 262,144 colours	B output (8-bit) 24-bit / pixel mode 16,777,216 colours	RGBSET Parameter
No Input	100000	B_{327} $B_{326}B_{325}$ $B_{324}B_{323}B_{322}B_{321}B_{320}$	161
No Input	100001	$B_{337}B_{336}B_{335}B_{334}B_{333}B_{332}B_{331}B_{330}$	162
No Input	100010	$B_{347}B_{346}B_{345}B_{344}B_{343}B_{342}B_{341}B_{340}$	163
No Input	100011	$B_{357}B_{356}B_{355}B_{354}B_{353}B_{352}B_{351}B_{350}$	164
No Input	100100	$B_{367}B_{366}B_{365}B_{364}B_{363}B_{362}B_{361}B_{360}$	165
No Input	100101	$B_{377}B_{376}B_{375}B_{374}B_{373}B_{372}B_{371}B_{370}$	166
No Input	100110	$B_{387}B_{386}B_{385}B_{384}B_{383}B_{382}B_{381}B_{380}$	167
No Input	100111	$B_{397}B_{396}B_{395}B_{394}B_{393}B_{392}B_{391}B_{390}$	168
No Input	101000	$B_{407}B_{406}B_{405}B_{404}B_{403}B_{402}B_{401}B_{400}$	169
No Input	101001	$B_{417}B_{416}B_{415}B_{414}B_{413}B_{412}B_{411}B_{410}$	170
No Input	101010	$B_{427}B_{426}B_{425}B_{424}B_{423}B_{422}B_{421}B_{420}$	171
No Input	101011	$B_{437}B_{436}B_{435}B_{434}B_{433}B_{432}B_{431}B_{430}$	172
No Input	101100	$B_{447}B_{446}B_{445}B_{444}B_{443}B_{442}B_{441}B_{440}$	173
No Input	101101	$B_{457}B_{456}B_{455}B_{454}B_{453}B_{452}B_{451}B_{450}$	174
No Input	101110	$B_{467}B_{466}B_{465}B_{464}B_{463}B_{462}B_{461}B_{460}$	175
No Input	101111	$B_{477}B_{476}B_{475}B_{474}B_{473}B_{472}B_{471}B_{470}$	176
No Input	110000	B_{487} $B_{486}B_{485}$ $B_{484}B_{483}B_{482}B_{481}B_{480}$	177
No Input	110001	$B_{497}B_{496}B_{495}B_{494}B_{493}B_{492}B_{491}B_{490}$	178
No Input	110010	$B_{507}B_{506}B_{505}B_{504}B_{503}B_{502}B_{501}B_{500}$	179
No Input	110011	$B_{517}B_{516}B_{515}B_{514}B_{513}B_{512}B_{511}B_{510}$	180
No Input	110100	$B_{527}B_{526}B_{525}B_{524}B_{523}B_{522}B_{521}B_{520}$	181
No Input	110101	$B_{537}B_{536}B_{535}B_{534}B_{533}B_{532}B_{531}B_{530}$	182
No Input	110110	$B_{547}B_{546}B_{545}B_{544}B_{543}B_{542}B_{541}B_{540}$	183
No Input	110111	$B_{557}B_{556}B_{555}B_{554}B_{553}B_{552}B_{551}B_{550}$	184
No Input	111000	$B_{567}B_{566}B_{565}B_{564}B_{563}B_{562}B_{561}B_{560}$	185
No Input	111001	$B_{577}B_{576}B_{575}B_{574}B_{573}B_{572}B_{571}B_{570}$	186
No Input	111010	$B_{587}B_{586}B_{585}B_{584}B_{583}B_{582}B_{581}B_{580}$	187
No Input	111011	$B_{597}B_{596}B_{595}B_{594}B_{593}B_{592}B_{591}B_{590}$	188
No Input	111100	$B_{607}B_{606}B_{605}B_{604}B_{603}B_{602}B_{601}B_{600}$	189
No Input	111101	$B_{617}B_{616}B_{615}B_{614}B_{613}B_{612}B_{611}B_{610}$	190
No Input	111110	$B_{627}B_{626}B_{625}B_{624}B_{623}B_{622}B_{621}B_{620}$	191
No Input	111111	$B_{637}B_{636}B_{635}B_{634}B_{633}B_{632}B_{631}B_{630}$	192

Table 5.20: Look-up tables-6

5.7 Oscillator

The HX8369-A02 can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the UADJ[3:0] internal register. Please refer to OSC control register (RB0h). The default frequency is 15MHz.

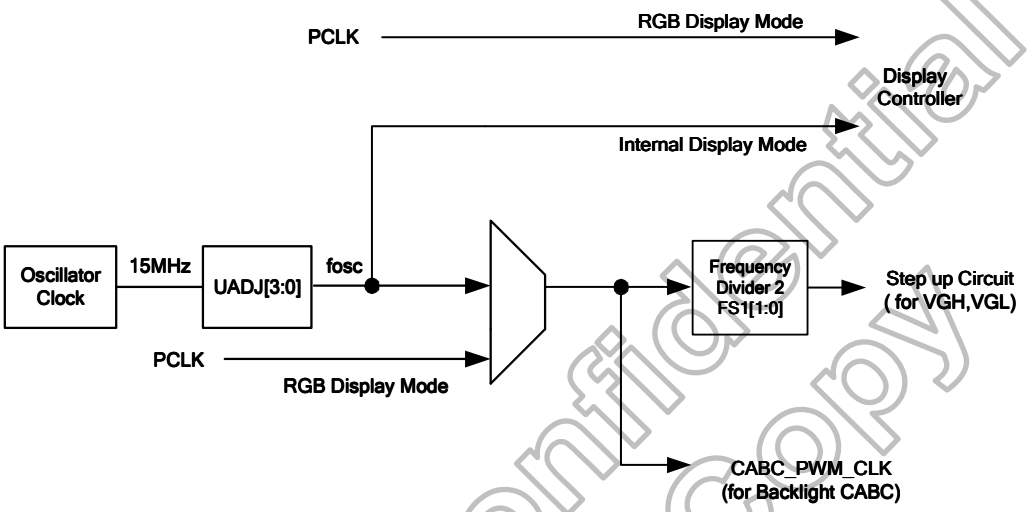
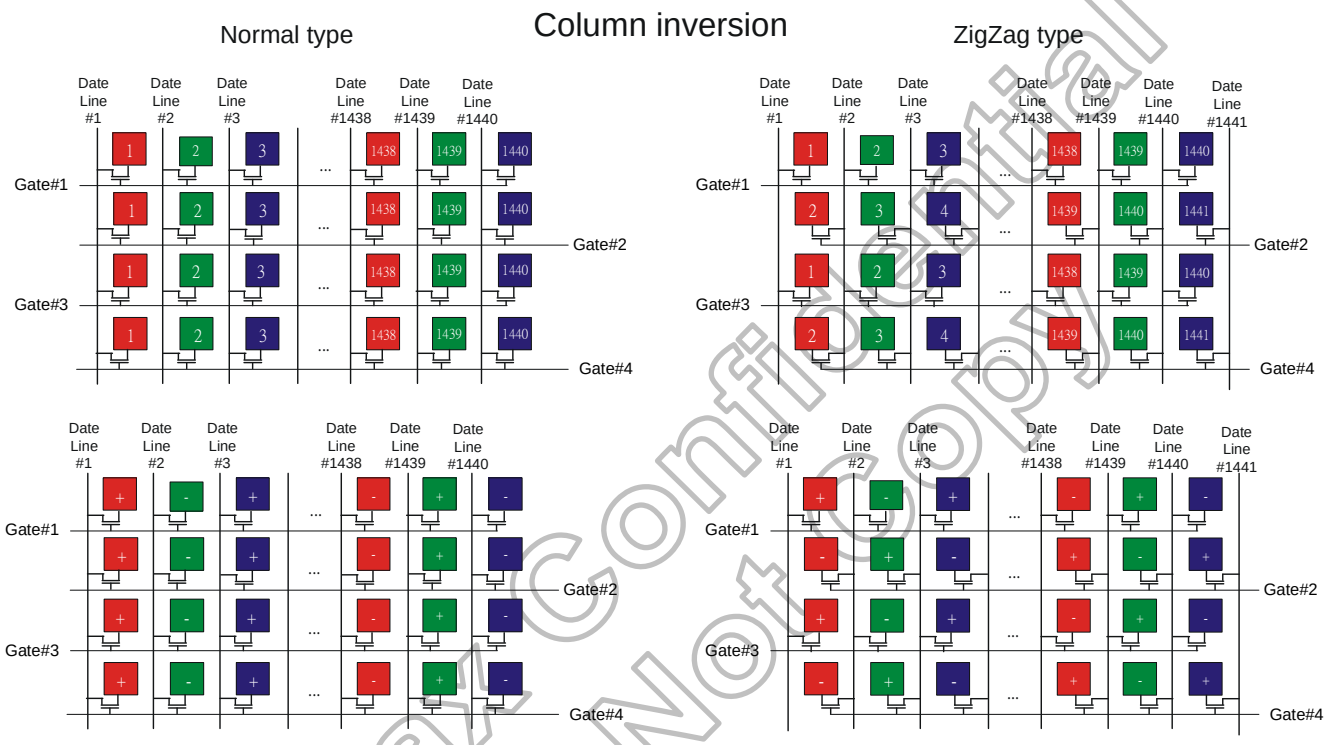


Figure 5.25: OSC aritecture

5.8 Source driver

The HX8369-A02 contains a 1440 channels of source driver (normal S1~S1440; Zig-zag S1~S1441) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 1440 channels and generates corresponding gray scale voltage output, which can realize a 16.7M colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.



5.9 LCD power generation scheme

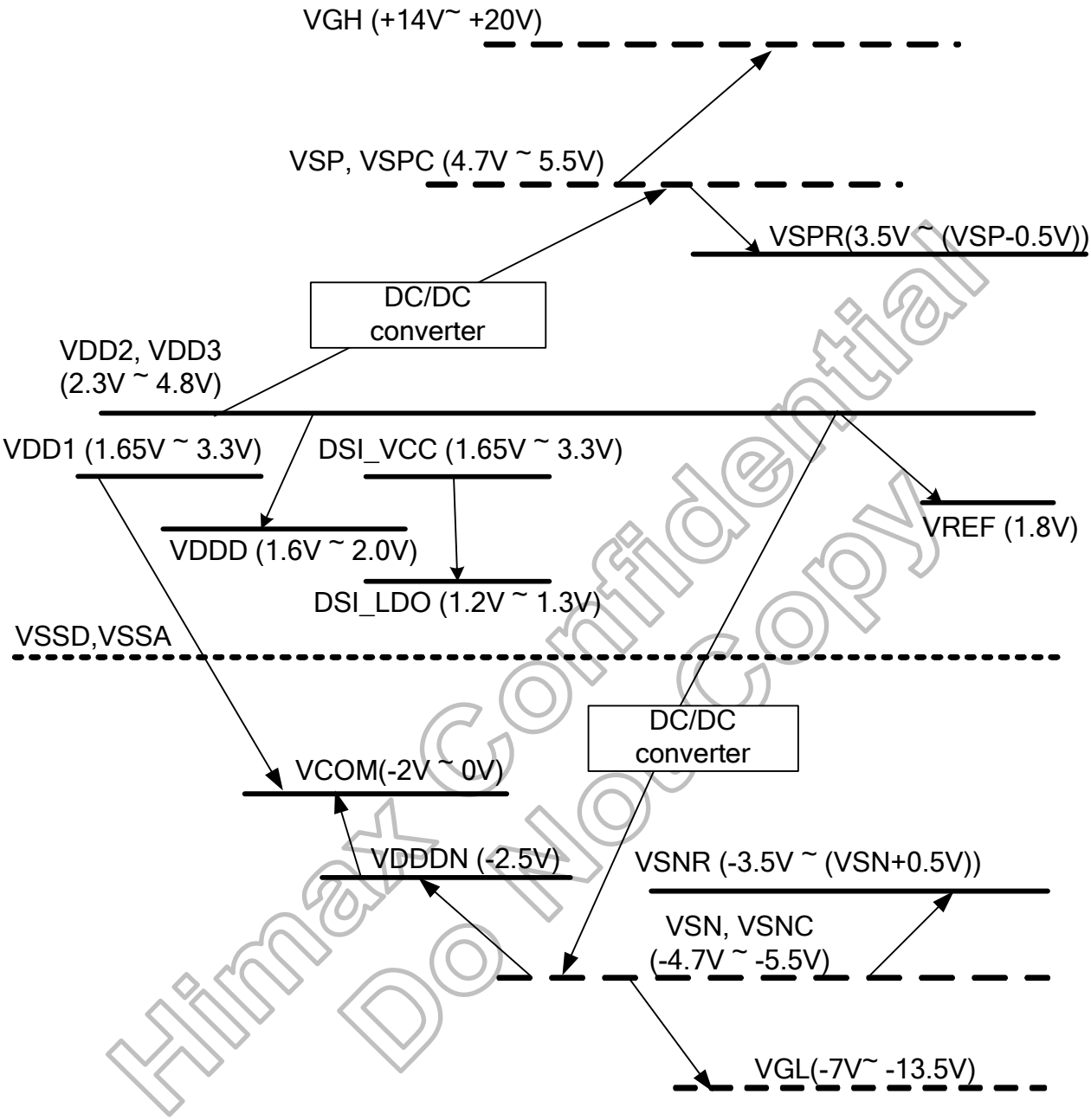


Figure 5.26: LCD power generation scheme

5.10 DC/DC converter circuit

5.10.1 Use PFM DC/DC converter

The PFM DC-DC converter generates the high voltage level VSP/VSN required for source drivers. HX8369-A02 contains sub-circuits of the PFM boost converter, including a precision 1.8V reference voltage, comparator, PFM controlling logic, and the output buffer. The boost converter uses a external power transistor to provide maximum efficiency and to minimize the number of external components. The output voltage of the boost converter can be set from 4.7 to 5.5 (VSP) and -4.7 to -5.5V (VSN)

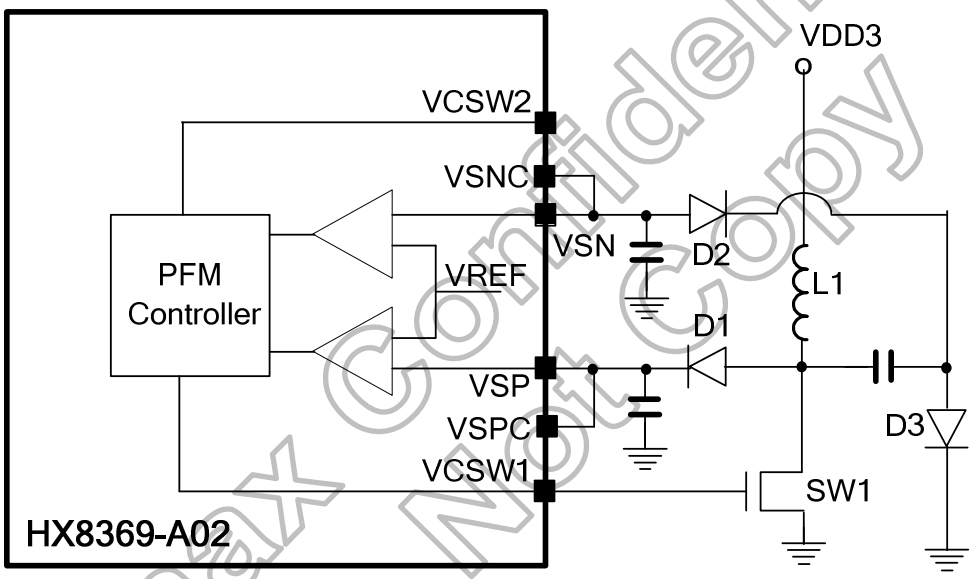


Figure 5.27: DC/DC converter circuit (PFM Type C)–PCCS=10

5.10.2 Use HX5186-A

The HX5186-A is highly efficient switching voltage generator circuits that generate the high voltage level VSP/VSN required for source drivers. HX8369-A02 contains Charge Pump Controller for HX5186-A, including a comparator for VSP/VSN feedback control. HX5186-A can provide maximum efficiency and use minimum number of external components. The output voltage of the boost converter can be set from 4.7 to 5.5 (VSP) and -4.7 to -5.5V (VSN)

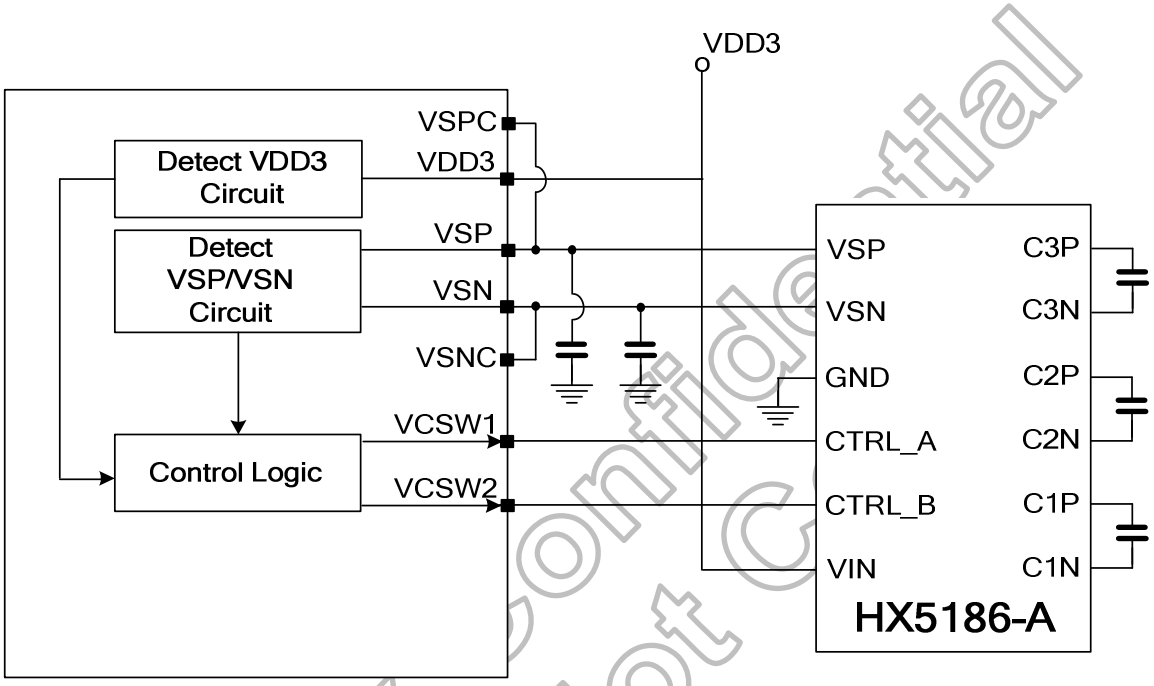


Figure 5.28: DC/DC converter circuit (HX5186-A)

5.11Idle display

The HX8369-A02 supports an idle display mode. The grayscale level to be used is V0 and V64 with R7, G7, B7 decoding, and the other levels (V1-V63) are halted to reduce power consumption. In idle display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

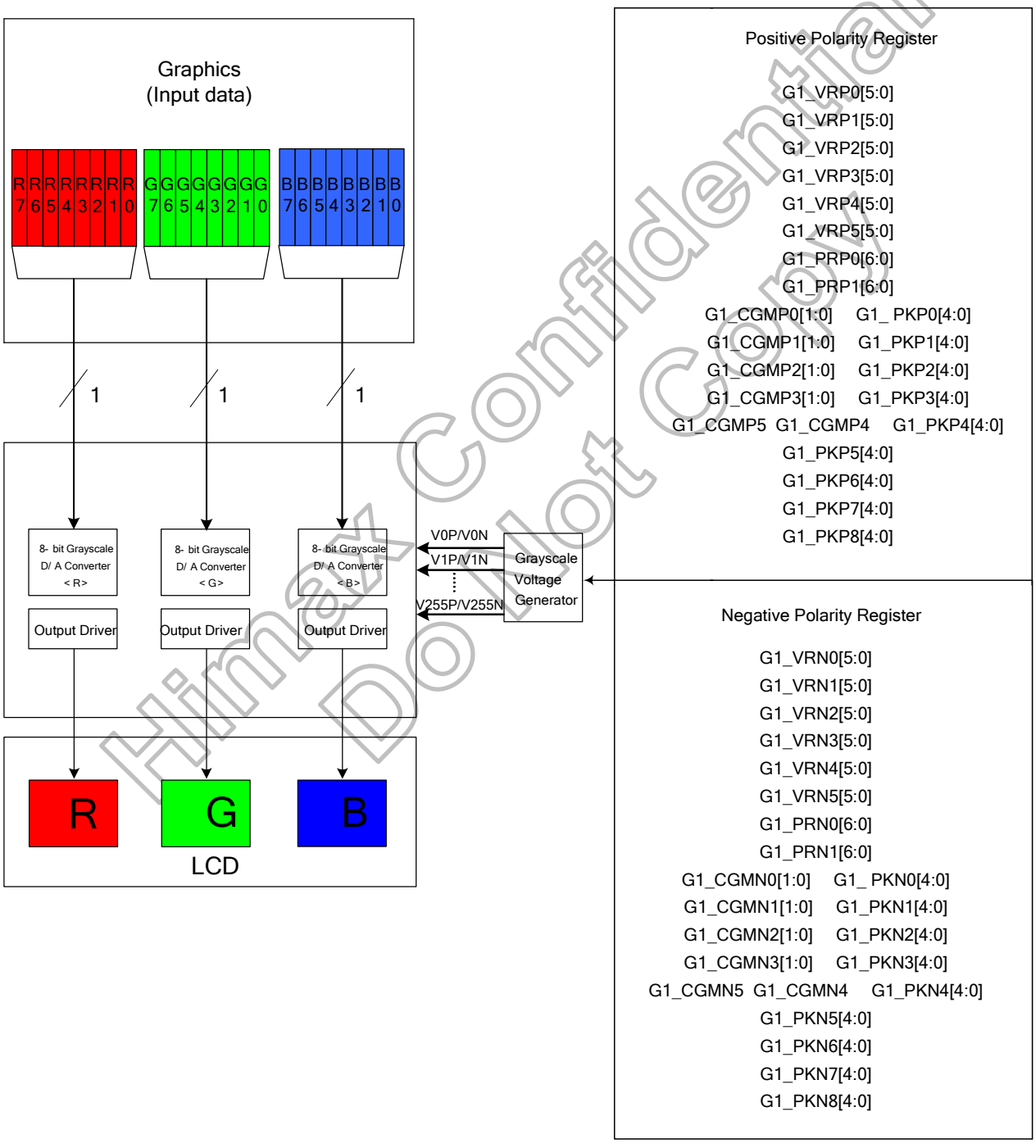


Figure 5.29: Idle mode grayscale control

5.12Gamma characteristic correction function

The HX8369-A02 incorporates gamma adjustment function for the 16,777,216-color display (256 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 512 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

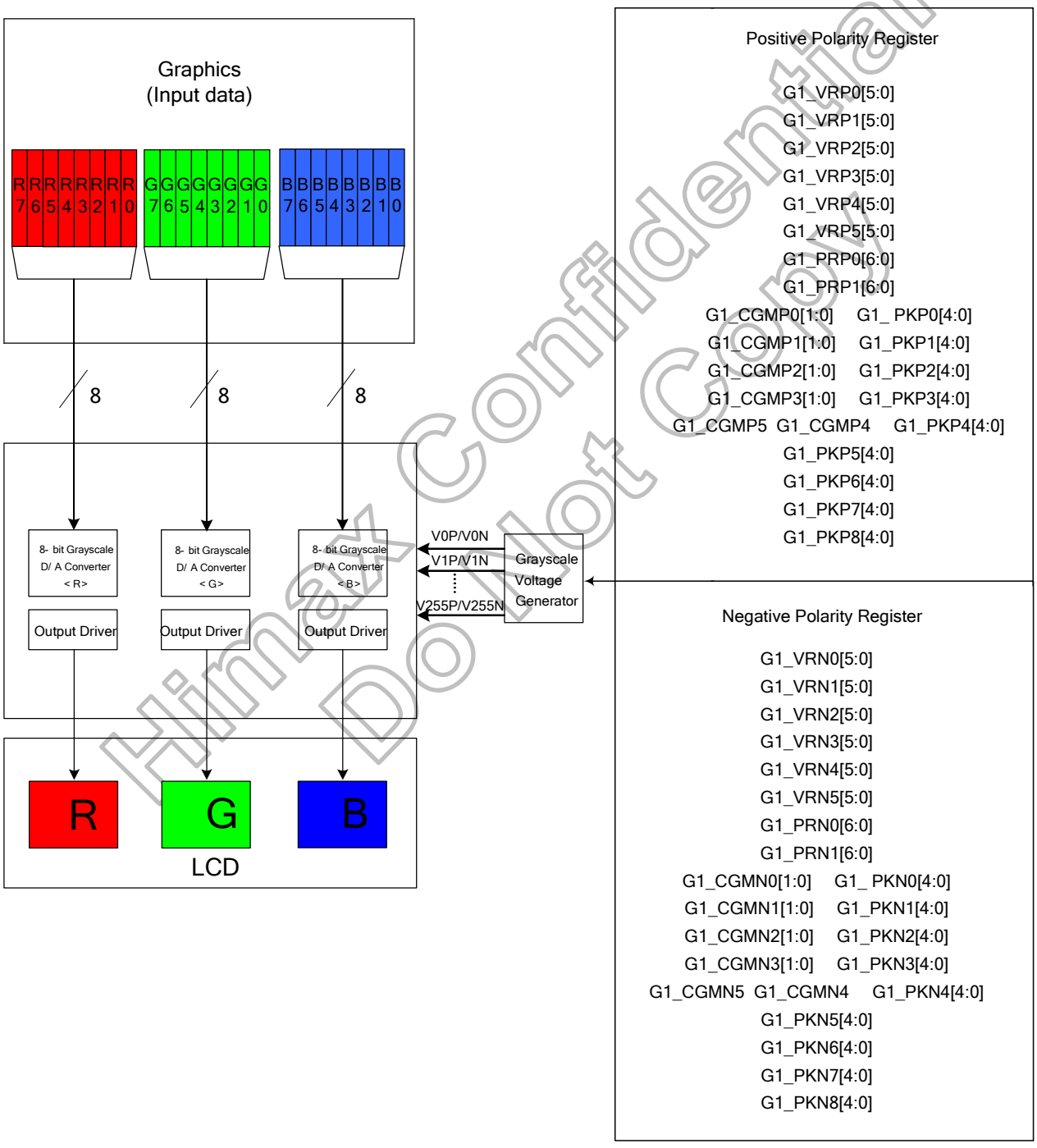


Figure 5.30: Grayscale control

Gamma-Characteristics adjustment register

This HX8369-A02 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

(1) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 88 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output (Vg(P/N)3, 7, 19, 25, 32, 38, 44, 56, 60).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
	PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

Table 5.21: Gamma-Adjustment registers

Gamma resister stream and 8 to 1 selector

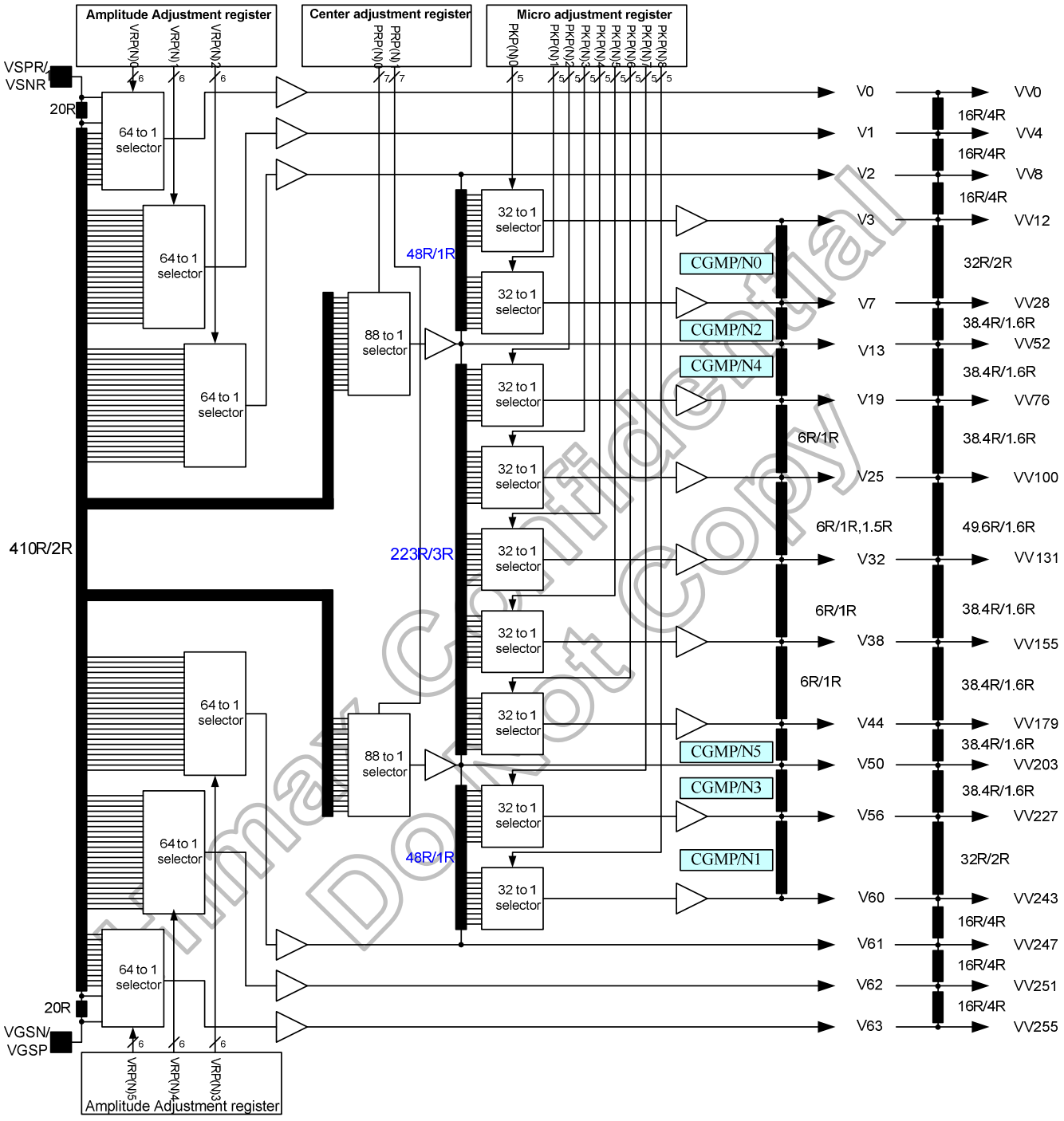
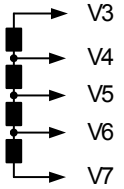
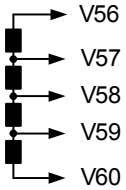


Figure 5.31: Gamma resister stream and gamma reference voltage

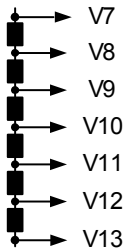
CGMP/N0	0	1	2	3
	1R	3R	3.5R	3.5R
	1R	2.5R	2.5R	2.5R
	1R	2R	1.8R	2R
	1R	2R	1.5R	2R



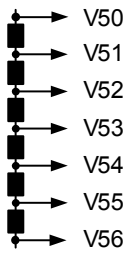
CGMP/N1	0	1	2	3
	1R	2R	1.5R	2R
	1R	2R	1.8R	2R
	1R	2.5R	2.5R	2.5R
	1R	3R	3.5R	3.5R



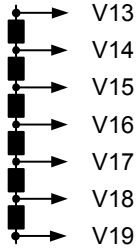
CGMP/N2	0	1	2	3
	1R	3R	4R	4.5R
	1R	3R	3R	4R
	1R	2.5R	3R	3R
	1R	2.5R	3R	3R
	1R	2.5R	2.5R	2.5R
	1R	2.5R	2.5R	2.5R



CGMP/N3	0	1	2	3
	1R	2.5R	2.5R	2.5R
	1R	2.5R	2.5R	2.5R
	1R	2.5R	3R	3R
	1R	2.5R	3R	3R
	1R	3R	3R	4R
	1R	3R	4R	4.5R



CGMP/N4	0	1
	1R	1.5R
	1R	1R
	1R	1R
	1R	1R
	1R	1R
	1R	1R



CGMP/N5	0	1
	1R	1R
	1R	1R
	1R	1R
	1R	1R
	1R	1R
	1R	1.5R

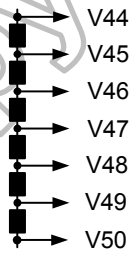


Figure 5.32: Gamma resister stream

Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0
000000	0R
000001	20R
000010	22R
000011	24R
•	•
•	•
011101	76R
011110	78R
011111	80R
100000	82R
100001	84R
100010	86R
•	•
•	•
111101	140R
111110	142R
111111	144R

Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
000011	6R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	126R

Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R
000001	2R
000010	4R
•	•
•	•
011101	58R
011110	60R
011111	62R
100000	64R
100001	66R
100010	68R
•	•
•	•
111100	120R
111101	122R
111110	124R
111111	144R

Table 5.22: Offset adjustment 0~5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1010101	170R
1010110	172R
1010111	174R

Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R
0000001	2R
0000010	4R
•	•
•	•
1010101	170R
1010110	172R
1010111	174R

Table 5.23: Center adjustment

The grayscale levels are determined by the following formulas:

Reference voltage	Macro adjustment value	VinP0 formula
VinP0	VRP0 5-0 = 000000	VSPR
	VRP0 5-0 = 000001	((450R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000010	((450R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000011	((450R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000100	((450R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000101	((450R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000110	((450R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000111	((450R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001000	((450R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001001	((450R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001010	((450R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001011	((450R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001100	((450R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001101	((450R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001110	((450R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001111	((450R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010000	((450R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010001	((450R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010010	((450R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010011	((450R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010100	((450R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010101	((450R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010110	((450R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010111	((450R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011000	((450R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011001	((450R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011010	((450R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011011	((450R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011100	((450R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011101	((450R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011110	((450R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011111	((450R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100000	((450R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100001	((450R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100010	((450R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100011	((450R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100100	((450R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100101	((450R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100110	((450R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100111	((450R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101000	((450R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101001	((450R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101010	((450R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101011	((450R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101100	((450R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101101	((450R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101110	((450R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101111	((450R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110000	((450R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110001	((450R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110010	((450R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110011	((450R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110100	((450R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110101	((450R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110110	((450R - 126R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110111	((450R - 128R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111000	((450R - 130R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111001	((450R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111010	((450R - 134R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111011	((450R - 136R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111100	((450R - 138R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111101	((450R - 140R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111110	((450R - 142R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111111	((450R - 144R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.24: VinP0

Reference voltage	Macro adjustment value	VinP1 formula
VinP1	VRP1 5-0 = 000000	(430R / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000001	((430R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000010	((430R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000011	((430R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000100	((430R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000101	((430R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000110	((430R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000111	((430R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001000	((430R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001001	((430R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001010	((430R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001011	((430R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001100	((430R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001101	((430R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001110	((430R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001111	((430R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010000	((430R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010001	((430R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010010	((430R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010011	((430R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010100	((430R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010101	((430R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010110	((430R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010111	((430R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011000	((430R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011001	((430R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011010	((430R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011011	((430R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011100	((430R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011101	((430R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011110	((430R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011111	((430R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100000	((430R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100001	((430R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100010	((430R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100011	((430R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100100	((430R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100101	((430R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100110	((430R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100111	((430R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101000	((430R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101001	((430R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101010	((430R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101011	((430R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101100	((430R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101101	((430R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101110	((430R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101111	((430R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110000	((430R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110001	((430R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110010	((430R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110011	((430R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110100	((430R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110101	((430R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110110	((430R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110111	((430R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111000	((430R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111001	((430R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111010	((430R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111011	((430R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111100	((430R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111101	((430R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111110	((430R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111111	((430R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.25: VinP1

Reference voltage	Macro adjustment value	VinP2 formula
VinP2	VRP2 5-0 = 000000	(420R / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000001	((420R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000010	((420R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000011	((420R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000100	((420R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000101	((420R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000110	((420R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000111	((420R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001000	((420R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001001	((420R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001010	((420R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001011	((420R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001100	((420R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001101	((420R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001110	((420R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001111	((420R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010000	((420R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010001	((420R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010010	((420R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010011	((420R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010100	((420R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010101	((420R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010110	((420R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010111	((420R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011000	((420R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011001	((420R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011010	((420R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011011	((420R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011100	((420R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011101	((420R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011110	((420R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011111	((420R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100000	((420R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100001	((420R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100010	((420R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100011	((420R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100100	((420R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100101	((420R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100110	((420R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100111	((420R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101000	((420R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101001	((420R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101010	((420R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101011	((420R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101100	((420R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101101	((420R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101110	((420R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101111	((420R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110000	((420R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110001	((420R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110010	((420R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110011	((420R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110100	((420R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110101	((420R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110110	((420R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110111	((420R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111000	((420R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111001	((420R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111010	((420R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111011	((420R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111100	((420R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111101	((420R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111110	((420R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111111	((420R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.26: VinP2

Reference voltage	Macro adjustment value	VinP14 formula
VinP14	VRP3 5-0 = 000000	(156R / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000001	((156R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000010	((156R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000011	((156R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000100	((156R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000101	((156R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000110	((156R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 000111	((156R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001000	((156R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001001	((156R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001010	((156R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001011	((156R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001100	((156R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001101	((156R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001110	((156R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 001111	((156R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010000	((156R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010001	((156R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010010	((156R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010011	((156R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010100	((156R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010101	((156R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010110	((156R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 010111	((156R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011000	((156R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011001	((156R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011010	((156R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011011	((156R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011100	((156R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011101	((156R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011110	((156R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 011111	((156R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100000	((156R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100001	((156R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100010	((156R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100011	((156R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100100	((156R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100101	((156R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100110	((156R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 100111	((156R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101000	((156R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101001	((156R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101010	((156R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101011	((156R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101100	((156R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101101	((156R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101110	((156R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 101111	((156R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110000	((156R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110001	((156R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110010	((156R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110011	((156R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110100	((156R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110101	((156R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110110	((156R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 110111	((156R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111000	((156R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111001	((156R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111010	((156R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111011	((156R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111100	((156R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111101	((156R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111110	((156R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP3 5-0 = 111111	((156R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.27: VinP14

Reference voltage	Macro adjustment value	VinP15 formula
VinP15	VRP4 5-0 = 000000	(146R / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000001	((146R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000010	((146R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000011	((146R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000100	((146R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000101	((146R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000110	((146R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000111	((146R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001000	((146R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001001	((146R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001010	((146R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001011	((146R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001100	((146R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001101	((146R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001110	((146R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001111	((146R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010000	((146R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010001	((146R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010010	((146R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010011	((146R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010100	((146R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010101	((146R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010110	((146R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010111	((146R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011000	((146R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011001	((146R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011010	((146R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011011	((146R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011100	((146R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011101	((146R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011110	((146R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011111	((146R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100000	((146R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100001	((146R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100010	((146R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100011	((146R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100100	((146R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100101	((146R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100110	((146R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100111	((146R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101000	((146R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101001	((146R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101010	((146R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101011	((146R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101100	((146R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101101	((146R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101110	((146R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101111	((146R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110000	((146R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110001	((146R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110010	((146R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110011	((146R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110100	((146R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110101	((146R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110110	((146R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110111	((146R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111000	((146R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111001	((146R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111010	((146R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111011	((146R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111100	((146R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111101	((146R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111110	((146R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111111	((146R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.28: VinP15

Reference voltage	Macro adjustment value	VinP16 formula
VinP16	VRP5 5-0 = 000000	(144R / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000001	((144R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000010	((144R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000011	((144R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000100	((144R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000101	((144R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000110	((144R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 000111	((144R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001000	((144R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001001	((144R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001010	((144R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001011	((144R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001100	((144R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001101	((144R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001110	((144R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 001111	((144R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010000	((144R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010001	((144R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010010	((144R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010011	((144R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010100	((144R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010101	((144R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010110	((144R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 010111	((144R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011000	((144R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011001	((144R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011010	((144R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011011	((144R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011100	((144R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011101	((144R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011110	((144R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 011111	((144R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100000	((144R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100001	((144R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100010	((144R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100011	((144R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100100	((144R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100101	((144R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100110	((144R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 100111	((144R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101000	((144R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101001	((144R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101010	((144R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101011	((144R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101100	((144R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101101	((144R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101110	((144R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 101111	((144R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110000	((144R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110001	((144R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110010	((144R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110011	((144R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110100	((144R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110101	((144R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110110	((144R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 110111	((144R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111000	((144R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111001	((144R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111010	((144R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111011	((144R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111100	((144R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111101	((144R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111110	((144R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP5 5-0 = 111111	VGSP

Table 5.29: VinP16

Reference voltage	Macro adjustment value	VinP5 formula
VinP5	PRP0 6-0 = 0000000	(350R / 450R) (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000001	((350R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000010	((350R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000011	((350R – 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000100	((350R – 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000101	((350R – 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000110	((350R – 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000111	((350R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001000	((350R – 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001001	((350R – 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001010	((350R – 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001011	((350R – 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001100	((350R – 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001101	((350R – 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001110	((350R – 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001111	((350R – 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010000	((350R – 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010001	((350R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010010	((350R – 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010011	((350R – 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010100	((350R – 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010101	((350R – 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010110	((350R – 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010111	((350R – 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011000	((350R – 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011001	((350R – 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011010	((350R – 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011011	((350R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011100	((350R – 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011101	((350R – 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011110	((350R – 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011111	((350R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100000	((350R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100001	((350R – 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100010	((350R – 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100011	((350R – 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100100	((350R – 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100101	((350R – 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100110	((350R – 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100111	((350R – 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101000	((350R – 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101001	((350R – 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101010	((350R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101011	((350R – 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101100	((350R – 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101101	((350R – 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101110	((350R – 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101111	((350R – 94R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110000	((350R – 96R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110001	((350R – 98R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110010	((350R – 100R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110011	((350R – 102R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110100	((350R – 104R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110101	((350R – 106R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110110	((350R – 108R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0110111	((350R – 110R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111000	((350R – 112R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111001	((350R – 114R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111010	((350R – 116R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111011	((350R – 118R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111100	((350R – 120R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111101	((350R – 122R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111110	((350R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0111111	((350R – 126R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000000	((350R – 128R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000001	((350R – 130R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000010	((350R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000011	((350R – 134R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000100	((350R – 136R) / 450R) * (VSPR - VGSP) + VGSP

	PRP0 6-0 = 1000101	((350R – 138R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000110	((350R – 140R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1000111	((350R – 142R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001000	((350R – 144R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001001	((350R – 146R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001010	((350R – 148R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001011	((350R – 150R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001100	((350R - 152R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001101	((350R – 154R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001110	((350R – 156R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1001111	((350R – 158R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010000	((350R – 160R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010001	((350R – 162R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010010	((350R – 164R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010011	((350R – 166R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010100	((350R – 168R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010101	((350R – 170R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010110	((350R – 172R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1010111	((350R - 174R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 1011000	inhibit
	PRP0 6-0 = 1011001	inhibit
	PRP0 6-0 = 1011010	inhibit
	PRP0 6-0 = 1011011	inhibit
	PRP0 6-0 = 1011100	inhibit
	PRP0 6-0 = 1011101	inhibit
	PRP0 6-0 = 1011110	inhibit
	PRP0 6-0 = 1011111	inhibit
	PRP0 6-0 = 1100000	inhibit
	PRP0 6-0 = 1100001	inhibit
	PRP0 6-0 = 1100010	inhibit
	PRP0 6-0 = 1100011	inhibit
	PRP0 6-0 = 1100100	inhibit
	PRP0 6-0 = 1100101	inhibit
	PRP0 6-0 = 1100110	inhibit
	PRP0 6-0 = 1100111	inhibit
	PRP0 6-0 = 1101000	inhibit
	PRP0 6-0 = 1101001	inhibit
	PRP0 6-0 = 1101010	inhibit
	PRP0 6-0 = 1101011	inhibit
	PRP0 6-0 = 1101100	inhibit
	PRP0 6-0 = 1101101	inhibit
	PRP0 6-0 = 1101110	inhibit
	PRP0 6-0 = 1101111	inhibit
	PRP0 6-0 = 1110000	inhibit
	PRP0 6-0 = 1110001	inhibit
	PRP0 6-0 = 1110010	inhibit
	PRP0 6-0 = 1110011	inhibit
	PRP0 6-0 = 1110100	inhibit
	PRP0 6-0 = 1110101	inhibit
	PRP0 6-0 = 1110110	inhibit
	PRP0 6-0 = 1110111	inhibit
	PRP0 6-0 = 1111000	inhibit
	PRP0 6-0 = 1111001	inhibit
	PRP0 6-0 = 1111010	inhibit
	PRP0 6-0 = 1111011	inhibit
	PRP0 6-0 = 1111100	inhibit
	PRP0 6-0 = 1111101	inhibit
	PRP0 6-0 = 1111110	inhibit
	PRP0 6-0 = 1111111	inhibit

Table 5.30: VinP5

Reference voltage	Macro adjustment value	VinP11 formula
VinP11	PRP1 6-0 = 0000000	(274R / 450R) (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000001	((274R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000010	((274R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000011	((274R – 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000100	((274R – 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000101	((274R – 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000110	((274R – 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000111	((274R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001000	((274R – 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001001	((274R – 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001010	((274R – 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001011	((274R – 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001100	((274R – 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001101	((274R – 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001110	((274R – 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001111	((274R – 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010000	((274R – 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010001	((274R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010010	((274R – 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010011	((274R – 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010100	((274R – 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010101	((274R – 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010110	((274R – 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010111	((274R – 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011000	((274R – 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011001	((274R – 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011010	((274R – 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011011	((274R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011100	((274R – 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011101	((274R – 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011110	((274R – 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011111	((274R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100000	((274R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100001	((274R – 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100010	((274R – 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100011	((274R – 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100100	((274R – 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100101	((274R – 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100110	((274R – 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100111	((274R – 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101000	((274R – 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101001	((274R – 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101010	((274R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101011	((274R – 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101100	((274R – 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101101	((274R – 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101110	((274R – 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101111	((274R – 94R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110000	((274R – 96R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110001	((274R – 98R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110010	((274R – 100R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110011	((274R – 102R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110100	((274R – 104R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110101	((274R – 106R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110110	((274R – 108R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110111	((274R – 110R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111000	((274R – 112R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111001	((274R – 114R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111010	((274R – 116R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111011	((274R – 118R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111100	((274R – 120R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111101	((274R – 122R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111110	((274R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111111	((274R – 126R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000000	((274R – 128R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000001	((274R – 130R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000010	((274R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000011	((274R - 134R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000100	((274R – 136R) / 450R) * (VSPR - VGSP) + VGSP

	PRP1 6-0 = 1000101	((274R – 138R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000110	((274R – 140R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000111	((274R – 142R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001000	((274R – 144R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001001	((274R – 146R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001010	((274R – 148R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001011	((274R – 150R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001100	((274R - 152R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001101	((274R – 154R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001110	((274R – 156R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1001111	((274R – 158R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010000	((274R – 160R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010001	((274R – 162R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010010	((274R – 164R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010011	((274R – 166R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010100	((274R – 168R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010101	((274R – 170R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010110	((274R – 172R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1010111	((274R - 174R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1011000	inhibit
	PRP1 6-0 = 1011001	inhibit
	PRP1 6-0 = 1011010	inhibit
	PRP1 6-0 = 1011011	inhibit
	PRP1 6-0 = 1011100	inhibit
	PRP1 6-0 = 1011101	inhibit
	PRP1 6-0 = 1011110	inhibit
	PRP1 6-0 = 1011111	inhibit
	PRP1 6-0 = 1100000	inhibit
	PRP1 6-0 = 1100001	inhibit
	PRP1 6-0 = 1100010	inhibit
	PRP1 6-0 = 1100011	inhibit
	PRP1 6-0 = 1100100	inhibit
	PRP1 6-0 = 1100101	inhibit
	PRP1 6-0 = 1100110	inhibit
	PRP1 6-0 = 1100111	inhibit
	PRP1 6-0 = 1101000	inhibit
	PRP1 6-0 = 1101001	inhibit
	PRP1 6-0 = 1101010	inhibit
	PRP1 6-0 = 1101011	inhibit
	PRP1 6-0 = 1101100	inhibit
	PRP1 6-0 = 1101101	inhibit
	PRP1 6-0 = 1101110	inhibit
	PRP1 6-0 = 1101111	inhibit
	PRP1 6-0 = 1110000	inhibit
	PRP1 6-0 = 1110001	inhibit
	PRP1 6-0 = 1110010	inhibit
	PRP1 6-0 = 1110011	inhibit
	PRP1 6-0 = 1110100	inhibit
	PRP1 6-0 = 1110101	inhibit
	PRP1 6-0 = 1110110	inhibit
	PRP1 6-0 = 1110111	inhibit
	PRP1 6-0 = 1111000	inhibit
	PRP1 6-0 = 1111001	inhibit
	PRP1 6-0 = 1111010	inhibit
	PRP1 6-0 = 1111011	inhibit
	PRP1 6-0 = 1111100	inhibit
	PRP1 6-0 = 1111101	inhibit
	PRP1 6-0 = 1111110	inhibit
	PRP1 6-0 = 1111111	inhibit

Table 5.31: VinP11

Reference voltage	Macro adjustment value	VinP3 formula
VinP3	PKP0 4-0 = 00000	(47R / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00001	((47R – 1R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00010	((47R – 2R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00011	((47R – 3R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00100	((47R – 4R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00101	((47R – 5R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00110	((47R – 6R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 00111	((47R – 7R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01000	((47R – 8R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01001	((47R – 9R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01010	((47R - 10R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01011	((47R - 11R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01100	((47R - 12R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01101	((47R - 13R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01110	((47R - 14R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 01111	((47R - 15R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10000	((47R - 16R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10001	((47R - 17R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10010	((47R - 18R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10011	((47R - 19R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10100	((47R - 20R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10101	((47R - 21R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10110	((47R - 22R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 10111	((47R - 23R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11000	((47R - 24R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11001	((47R - 25R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11010	((47R - 26R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11011	((47R - 27R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11100	((47R - 28R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11101	((47R - 29R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11110	((47R - 30R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP0 4-0 = 11111	((47R - 31R) / 48R) * (VinP2 - VinP5) + VinP5

Table 5.32: VinP3

Reference voltage	Macro adjustment value	VinP4 formula
VinP4	PKP1 4-0 = 00000	(32R / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00001	((32R - 1R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00010	((32R - 2R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00011	((32R - 3R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00100	((32R - 4R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00101	((32R - 5R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00110	((32R - 6R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 00111	((32R - 7R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01000	((32R - 8R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01001	((32R - 9R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01010	((32R - 10R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01011	((32R - 11R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01100	((32R - 12R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01101	((32R - 13R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01110	((32R - 14R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 01111	((32R - 15R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10000	((32R - 16R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10001	((32R - 17R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10010	((32R - 18R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10011	((32R - 19R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10100	((32R - 20R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10101	((32R - 21R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10110	((32R - 22R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 10111	((32R - 23R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11000	((32R - 24R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11001	((32R - 25R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11010	((32R - 26R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11011	((32R - 27R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11100	((32R - 28R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11101	((32R - 29R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11110	((32R - 30R) / 48R) * (VinP2 - VinP5) + VinP5
	PKP1 4-0 = 11111	((32R - 31R) / 48R) * (VinP2 - VinP5) + VinP5

Table 5.33: VinP4

Reference voltage	Macro adjustment value	VinP6 formula
VinP6	PKP2 4-0 = 00000	(220R / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00001	((220R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00010	((220R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00011	((220R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00100	((220R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00101	((220R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00110	((220R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 00111	((220R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01000	((220R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01001	((220R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01010	((220R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01011	((220R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01100	((220R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01101	((220R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01110	((220R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 01111	((220R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10000	((220R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10001	((220R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10010	((220R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10011	((220R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10100	((220R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10101	((220R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10110	((220R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 10111	((220R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11000	((220R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11001	((220R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11010	((220R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11011	((220R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11100	((220R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11101	((220R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11110	((220R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP2 4-0 = 11111	((220R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.34: VinP6

Reference voltage	Macro adjustment value	VinP7 formula
VinP7	PKP3 4-0 = 00000	(193R / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00001	((193R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00010	((193R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00011	((193R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00100	((193R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00101	((193R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00110	((193R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 00111	((193R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01000	((193R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01001	((193R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01010	((193R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01011	((193R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01100	((193R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01101	((193R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01110	((193R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 01111	((193R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10000	((193R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10001	((193R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10010	((193R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10011	((193R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10100	((193R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10101	((193R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10110	((193R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 10111	((193R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11000	((193R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11001	((193R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11010	((193R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11011	((193R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11100	((193R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11101	((193R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11110	((193R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP3 4-0 = 11111	((193R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.35: VinP7

Reference voltage	Macro adjustment value	VinP8 formula
VinP8	PKP4 4-0 = 00000	(158R / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00001	((158R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00010	((158R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00011	((158R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00100	((158R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00101	((158R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00110	((158R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 00111	((158R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01000	((158R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01001	((158R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01010	((158R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01011	((158R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01100	((158R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01101	((158R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01110	((158R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 01111	((158R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10000	((158R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10001	((158R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10010	((158R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10011	((158R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10100	((158R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10101	((158R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10110	((158R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 10111	((158R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11000	((158R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11001	((158R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11010	((158R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11011	((158R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11100	((158R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11101	((158R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11110	((158R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP4 4-0 = 11111	((158R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.36: VinP8

Reference voltage	Macro adjustment value	VinP9 formula
VinP9	PKP5 4-0 = 00000	(123R / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00001	((123R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00010	((123R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00011	((123R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00100	((123R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00101	((123R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00110	((123R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 00111	((123R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01000	((123R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01001	((123R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01010	((123R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01011	((123R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01100	((123R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01101	((123R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01110	((123R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 01111	((123R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10000	((123R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10001	((123R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10010	((123R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10011	((123R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10100	((123R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10101	((123R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10110	((123R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 10111	((123R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11000	((123R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11001	((123R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11010	((123R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11011	((123R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11100	((123R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11101	((123R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11110	((123R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP5 4-0 = 11111	((123R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.37: VinP9

Reference voltage	Macro adjustment value	VinP10 formula
VinP10	PKP6 4-0 = 00000	(96R / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00001	((96R - 3R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00010	((96R - 6R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00011	((96R - 9R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00100	((96R - 12R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00101	((96R - 15R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00110	((96R - 18R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 00111	((96R - 21R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01000	((96R - 24R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01001	((96R - 27R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01010	((96R - 30R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01011	((96R - 33R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01100	((96R - 36R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01101	((96R - 39R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01110	((96R - 42R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 01111	((96R - 45R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10000	((96R - 48R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10001	((96R - 51R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10010	((96R - 54R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10011	((96R - 57R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10100	((96R - 60R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10101	((96R - 63R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10110	((96R - 66R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 10111	((96R - 69R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11000	((96R - 72R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11001	((96R - 75R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11010	((96R - 78R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11011	((96R - 81R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11100	((96R - 84R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11101	((96R - 87R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11110	((96R - 90R) / 223R) * (VinP5 - VinP11) + VinP11
	PKP6 4-0 = 11111	((96R - 93R) / 223R) * (VinP5 - VinP11) + VinP11

Table 5.38: VinP10

Reference voltage	Macro adjustment value	VinP12 formula
VinP12	PKP7 4-0 = 00000	(47R / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00001	((47R - 1R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00010	((47R - 2R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00011	((47R - 3R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00100	((47R - 4R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00101	((47R - 5R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00110	((47R - 6R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 00111	((47R - 7R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01000	((47R - 8R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01001	((47R - 9R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01010	((47R - 10R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01011	((47R - 11R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01100	((47R - 12R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01101	((47R - 13R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01110	((47R - 14R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 01111	((47R - 15R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10000	((47R - 16R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10001	((47R - 17R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10010	((47R - 18R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10011	((47R - 19R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10100	((47R - 20R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10101	((47R - 21R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10110	((47R - 22R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 10111	((47R - 23R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11000	((47R - 24R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11001	((47R - 25R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11010	((47R - 26R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11011	((47R - 27R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11100	((47R - 28R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11101	((47R - 29R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11110	((47R - 30R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP7 4-0 = 11111	((47R - 31R) / 48R) * (VinP11 - VinP14) + VinP14

Table 5.39: VinP12

Reference voltage	Macro adjustment value	VinP13 formula
VinP13	PKP8 4-0 = 00000	(32R / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00001	((32R - 1R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00010	((32R - 2R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00011	((32R - 3R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00100	((32R - 4R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00101	((32R - 5R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00110	((32R - 6R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 00111	((32R - 7R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01000	((32R - 8R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01001	((32R - 9R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01010	((32R - 10R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01011	((32R - 11R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01100	((32R - 12R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01101	((32R - 13R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01110	((32R - 14R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 01111	((32R - 15R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10000	((32R - 16R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10001	((32R - 17R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10010	((32R - 18R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10011	((32R - 19R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10100	((32R - 20R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10101	((32R - 21R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10110	((32R - 22R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 10111	((32R - 23R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11000	((32R - 24R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11001	((32R - 25R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11010	((32R - 26R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11011	((32R - 27R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11100	((32R - 28R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11101	((32R - 29R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11110	((32R - 30R) / 48R) * (VinP11 - VinP14) + VinP14
	PKP8 4-0 = 11111	((32R - 31R) / 48R) * (VinP11 - VinP14) + VinP14

Table 5.40: VinP13

Reference voltage	Macro adjustment value	VinN0 formula
VinN0	VRN0 5-0 = 000000	VSNR
	VRN0 5-0 = 000001	((450R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000010	((450R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000011	((450R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000100	((450R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000101	((450R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000110	((450R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000111	((450R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001000	((450R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001001	((450R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001010	((450R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001011	((450R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001100	((450R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001101	((450R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001110	((450R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001111	((450R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010000	((450R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010001	((450R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010010	((450R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010011	((450R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010100	((450R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010101	((450R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010110	((450R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010111	((450R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011000	((450R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011001	((450R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011010	((450R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011011	((450R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011100	((450R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011101	((450R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011110	((450R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011111	((450R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100000	((450R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100001	((450R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100010	((450R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100011	((450R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100100	((450R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100101	((450R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100110	((450R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100111	((450R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101000	((450R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101001	((450R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101010	((450R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101011	((450R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101100	((450R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101101	((450R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101110	((450R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101111	((450R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110000	((450R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110001	((450R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110010	((450R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110011	((450R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110100	((450R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110101	((450R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110110	((450R - 126R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110111	((450R - 128R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111000	((450R - 130R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111001	((450R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111010	((450R - 134R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111011	((450R - 136R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111100	((450R - 138R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111101	((450R - 140R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111110	((450R - 142R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111111	((450R - 144R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.41: VinN0

Reference voltage	Macro adjustment value	VinN1 formula
VinN1	VRN1 5-0 = 000000	(430R / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000001	((430R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000010	((430R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000011	((430R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000100	((430R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000101	((430R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000110	((430R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000111	((430R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001000	((430R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001001	((430R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001010	((430R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001011	((430R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001100	((430R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001101	((430R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001110	((430R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001111	((430R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010000	((430R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010001	((430R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010010	((430R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010011	((430R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010100	((430R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010101	((430R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010110	((430R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010111	((430R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011000	((430R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011001	((430R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011010	((430R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011011	((430R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011100	((430R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011101	((430R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011110	((430R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011111	((430R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100000	((430R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100001	((430R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100010	((430R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100011	((430R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100100	((430R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100101	((430R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100110	((430R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100111	((430R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101000	((430R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101001	((430R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101010	((430R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101011	((430R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101100	((430R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101101	((430R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101110	((430R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101111	((430R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110000	((430R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110001	((430R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110010	((430R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110011	((430R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110100	((430R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110101	((430R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110110	((430R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110111	((430R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111000	((430R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111001	((430R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111010	((430R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111011	((430R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111100	((430R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111101	((430R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111110	((430R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111111	((430R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.42: VinN1

Reference voltage	Macro adjustment value	VinN2 formula
VinN2	VRN2 5-0 = 000000	(420R / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000001	((420R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000010	((420R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000011	((420R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000100	((420R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000101	((420R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000110	((420R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000111	((420R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001000	((420R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001001	((420R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001010	((420R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001011	((420R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001100	((420R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001101	((420R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001110	((420R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001111	((420R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010000	((420R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010001	((420R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010010	((420R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010011	((420R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010100	((420R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010101	((420R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010110	((420R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010111	((420R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011000	((420R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011001	((420R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011010	((420R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011011	((420R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011100	((420R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011101	((420R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011110	((420R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011111	((420R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100000	((420R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100001	((420R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100010	((420R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100011	((420R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100100	((420R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100101	((420R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100110	((420R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100111	((420R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101000	((420R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101001	((420R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101010	((420R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101011	((420R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101100	((420R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101101	((420R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101110	((420R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101111	((420R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110000	((420R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110001	((420R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110010	((420R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110011	((420R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110100	((420R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110101	((420R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110110	((420R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110111	((420R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111000	((420R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111001	((420R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111010	((420R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111011	((420R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111100	((420R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111101	((420R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111110	((420R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111111	((420R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.43: VinN2

Reference voltage	Macro adjustment value	VinN14 formula
VinN14	VRN3 5-0 = 000000	(156R / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000001	((156R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000010	((156R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000011	((156R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000100	((156R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000101	((156R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000110	((156R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000111	((156R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001000	((156R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001001	((156R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001010	((156R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001011	((156R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001100	((156R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001101	((156R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001110	((156R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001111	((156R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010000	((156R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010001	((156R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010010	((156R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010011	((156R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010100	((156R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010101	((156R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010110	((156R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010111	((156R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011000	((156R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011001	((156R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011010	((156R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011011	((156R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011100	((156R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011101	((156R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011110	((156R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011111	((156R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100000	((156R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100001	((156R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100010	((156R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100011	((156R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100100	((156R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100101	((156R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100110	((156R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100111	((156R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101000	((156R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101001	((156R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101010	((156R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101011	((156R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101100	((156R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101101	((156R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101110	((156R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101111	((156R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110000	((156R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110001	((156R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110010	((156R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110011	((156R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110100	((156R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110101	((156R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110110	((156R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110111	((156R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111000	((156R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111001	((156R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111010	((156R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111011	((156R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111100	((156R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111101	((156R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111110	((156R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111111	((156R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.44: VinN14

Reference voltage	Macro adjustment value	VinN15 formula
VinN15	VRN4 5-0 = 000000	(146R / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000001	((146R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000010	((146R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000011	((146R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000100	((146R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000101	((146R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000110	((146R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000111	((146R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001000	((146R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001001	((146R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001010	((146R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001011	((146R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001100	((146R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001101	((146R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001110	((146R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001111	((146R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010000	((146R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010001	((146R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010010	((146R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010011	((146R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010100	((146R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010101	((146R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010110	((146R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010111	((146R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011000	((146R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011001	((146R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011010	((146R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011011	((146R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011100	((146R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011101	((146R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011110	((146R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011111	((146R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100000	((146R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100001	((146R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100010	((146R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100011	((146R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100100	((146R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100101	((146R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100110	((146R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100111	((146R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101000	((146R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101001	((146R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101010	((146R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101011	((146R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101100	((146R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101101	((146R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101110	((146R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101111	((146R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110000	((146R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110001	((146R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110010	((146R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110011	((146R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110100	((146R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110101	((146R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110110	((146R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110111	((146R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111000	((146R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111001	((146R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111010	((146R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111011	((146R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111100	((146R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111101	((146R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111110	((146R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111111	((146R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.45: VinN15

Reference voltage	Macro adjustment value	VinN16 formula
VinN16	VRN5 5-0 = 000000	(144R / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000001	((144R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000010	((144R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000011	((144R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000100	((144R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000101	((144R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000110	((144R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 000111	((144R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001000	((144R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001001	((144R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001010	((144R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001011	((144R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001100	((144R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001101	((144R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001110	((144R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 001111	((144R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010000	((144R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010001	((144R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010010	((144R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010011	((144R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010100	((144R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010101	((144R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010110	((144R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 010111	((144R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011000	((144R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011001	((144R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011010	((144R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011011	((144R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011100	((144R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011101	((144R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011110	((144R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 011111	((144R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100000	((144R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100001	((144R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100010	((144R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100011	((144R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100100	((144R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100101	((144R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100110	((144R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 100111	((144R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101000	((144R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101001	((144R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101010	((144R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101011	((144R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101100	((144R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101101	((144R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101110	((144R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 101111	((144R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110000	((144R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110001	((144R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110010	((144R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110011	((144R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110100	((144R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110101	((144R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110110	((144R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 110111	((144R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111000	((144R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111001	((144R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111010	((144R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111011	((144R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111100	((144R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111101	((144R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111110	((144R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN5 5-0 = 111111	VGSN

Table 5.46: VinN16

Reference voltage	Macro adjustment value	VinN5 formula
VinN5	PRN0 6-0 = 0000000	(350R / 450R) (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000001	((350R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000010	((350R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000011	((350R – 6R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000100	((350R – 8R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000101	((350R – 10R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000110	((350R – 12R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0000111	((350R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001000	((350R – 16R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001001	((350R – 18R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001010	((350R – 20R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001011	((350R – 22R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001100	((350R – 24R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001101	((350R – 26R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001110	((350R – 28R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0001111	((350R – 30R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010000	((350R – 32R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010001	((350R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010010	((350R – 36R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010011	((350R – 38R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010100	((350R – 40R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010101	((350R – 42R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010110	((350R – 44R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0010111	((350R – 46R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011000	((350R – 48R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011001	((350R – 50R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011010	((350R – 52R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011011	((350R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011100	((350R – 56R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011101	((350R – 58R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011110	((350R – 60R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0011111	((350R – 62R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100000	((350R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100001	((350R – 66R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100010	((350R – 68R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100011	((350R – 70R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100100	((350R – 72R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100101	((350R – 74R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100110	((350R – 76R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0100111	((350R – 78R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101000	((350R – 80R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101001	((350R – 82R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101010	((350R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101011	((350R – 86R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101100	((350R – 88R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101101	((350R – 90R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101110	((350R – 92R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0101111	((350R – 94R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110000	((350R – 96R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110001	((350R – 98R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110010	((350R – 100R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110011	((350R – 102R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110100	((350R – 104R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110101	((350R – 106R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110110	((350R – 108R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0110111	((350R – 110R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111000	((350R – 112R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111001	((350R – 114R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111010	((350R – 116R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111011	((350R – 118R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111100	((350R – 120R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111101	((350R – 122R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111110	((350R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 0111111	((350R – 126R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000000	((350R – 128R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000001	((350R – 130R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000010	((350R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000011	((350R – 134R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000100	((350R – 136R) / 450R) * (VSNR - VGSN) + VGSN

	PRN0 6-0 = 1000101	((350R – 138R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000110	((350R – 140R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1000111	((350R – 142R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001000	((350R – 144R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001001	((350R – 146R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001010	((350R – 148R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001011	((350R – 150R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001100	((350R - 152R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001101	((350R – 154R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001110	((350R – 156R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1001111	((350R – 158R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010000	((350R – 160R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010001	((350R – 162R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010010	((350R – 164R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010011	((350R – 166R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010100	((350R – 168R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010101	((350R – 170R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010110	((350R – 172R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1010111	((350R - 174R) / 450R) * (VSNR - VGSN) + VGSN
	PRN0 6-0 = 1011000	inhibit
	PRN0 6-0 = 1011001	inhibit
	PRN0 6-0 = 1011010	inhibit
	PRN0 6-0 = 1011011	inhibit
	PRN0 6-0 = 1011100	inhibit
	PRN0 6-0 = 1011101	inhibit
	PRN0 6-0 = 1011110	inhibit
	PRN0 6-0 = 1011111	inhibit
	PRN0 6-0 = 1100000	inhibit
	PRN0 6-0 = 1100001	inhibit
	PRN0 6-0 = 1100010	inhibit
	PRN0 6-0 = 1100011	inhibit
	PRN0 6-0 = 1100100	inhibit
	PRN0 6-0 = 1100101	inhibit
	PRN0 6-0 = 1100110	inhibit
	PRN0 6-0 = 1100111	inhibit
	PRN0 6-0 = 1101000	inhibit
	PRN0 6-0 = 1101001	inhibit
	PRN0 6-0 = 1101010	inhibit
	PRN0 6-0 = 1101011	inhibit
	PRN0 6-0 = 1101100	inhibit
	PRN0 6-0 = 1101101	inhibit
	PRN0 6-0 = 1101110	inhibit
	PRN0 6-0 = 1101111	inhibit
	PRN0 6-0 = 1110000	inhibit
	PRN0 6-0 = 1110001	inhibit
	PRN0 6-0 = 1110010	inhibit
	PRN0 6-0 = 1110011	inhibit
	PRN0 6-0 = 1110100	inhibit
	PRN0 6-0 = 1110101	inhibit
	PRN0 6-0 = 1110110	inhibit
	PRN0 6-0 = 1110111	inhibit
	PRN0 6-0 = 1111000	inhibit
	PRN0 6-0 = 1111001	inhibit
	PRN0 6-0 = 1111010	inhibit
	PRN0 6-0 = 1111011	inhibit
	PRN0 6-0 = 1111100	inhibit
	PRN0 6-0 = 1111101	inhibit
	PRN0 6-0 = 1111110	inhibit
	PRN0 6-0 = 1111111	inhibit

Table 5.47: VinN5

Reference voltage	Macro adjustment value	VinN11 formula
VinN11	PRN1 6-0 = 0000000	(274R / 450R) (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000001	((274R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000010	((274R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000011	((274R – 6R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000100	((274R – 8R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000101	((274R – 10R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000110	((274R – 12R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000111	((274R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001000	((274R – 16R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001001	((274R – 18R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001010	((274R – 20R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001011	((274R – 22R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001100	((274R – 24R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001101	((274R – 26R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001110	((274R – 28R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001111	((274R – 30R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010000	((274R – 32R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010001	((274R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010010	((274R – 36R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010011	((274R – 38R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010100	((274R – 40R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010101	((274R – 42R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010110	((274R – 44R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010111	((274R – 46R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011000	((274R – 48R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011001	((274R – 50R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011010	((274R – 52R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011011	((274R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011100	((274R – 56R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011101	((274R – 58R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011110	((274R – 60R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011111	((274R – 62R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100000	((274R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100001	((274R – 66R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100010	((274R – 68R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100011	((274R – 70R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100100	((274R – 72R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100101	((274R – 74R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100110	((274R – 76R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100111	((274R – 78R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101000	((274R – 80R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101001	((274R – 82R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101010	((274R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101011	((274R – 86R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101100	((274R – 88R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101101	((274R – 90R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101110	((274R – 92R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101111	((274R – 94R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110000	((274R – 96R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110001	((274R – 98R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110010	((274R – 100R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110011	((274R – 102R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110100	((274R – 104R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110101	((274R – 106R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110110	((274R – 108R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110111	((274R – 110R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111000	((274R – 112R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111001	((274R – 114R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111010	((274R – 116R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111011	((274R – 118R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111100	((274R – 120R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111101	((274R – 122R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111110	((274R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111111	((274R – 126R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000000	((274R – 128R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000001	((274R – 130R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000010	((274R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000011	((274R – 134R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000100	((274R – 136R) / 450R) * (VSNR - VGSN) + VGSN

	PRN1 6-0 = 1000101	((274R – 138R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000110	((274R – 140R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000111	((274R – 142R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001000	((274R – 144R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001001	((274R – 146R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001010	((274R – 148R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001011	((274R – 150R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001100	((274R - 152R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001101	((274R – 154R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001110	((274R – 156R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1001111	((274R – 158R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010000	((274R – 160R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010001	((274R – 162R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010010	((274R – 164R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010011	((274R – 166R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010100	((274R – 168R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010101	((274R – 170R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010110	((274R – 172R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1010111	((274R - 174R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1011000	inhibit
	PRN1 6-0 = 1011001	inhibit
	PRN1 6-0 = 1011010	inhibit
	PRN1 6-0 = 1011011	inhibit
	PRN1 6-0 = 1011100	inhibit
	PRN1 6-0 = 1011101	inhibit
	PRN1 6-0 = 1011110	inhibit
	PRN1 6-0 = 1011111	inhibit
	PRN1 6-0 = 1100000	inhibit
	PRN1 6-0 = 1100001	inhibit
	PRN1 6-0 = 1100010	inhibit
	PRN1 6-0 = 1100011	inhibit
	PRN1 6-0 = 1100100	inhibit
	PRN1 6-0 = 1100101	inhibit
	PRN1 6-0 = 1100110	inhibit
	PRN1 6-0 = 1100111	inhibit
	PRN1 6-0 = 1101000	inhibit
	PRN1 6-0 = 1101001	inhibit
	PRN1 6-0 = 1101010	inhibit
	PRN1 6-0 = 1101011	inhibit
	PRN1 6-0 = 1101100	inhibit
	PRN1 6-0 = 1101101	inhibit
	PRN1 6-0 = 1101110	inhibit
	PRN1 6-0 = 1101111	inhibit
	PRN1 6-0 = 1110000	inhibit
	PRN1 6-0 = 1110001	inhibit
	PRN1 6-0 = 1110010	inhibit
	PRN1 6-0 = 1110011	inhibit
	PRN1 6-0 = 1110100	inhibit
	PRN1 6-0 = 1110101	inhibit
	PRN1 6-0 = 1110110	inhibit
	PRN1 6-0 = 1110111	inhibit
	PRN1 6-0 = 1111000	inhibit
	PRN1 6-0 = 1111001	inhibit
	PRN1 6-0 = 1111010	inhibit
	PRN1 6-0 = 1111011	inhibit
	PRN1 6-0 = 1111100	inhibit
	PRN1 6-0 = 1111101	inhibit
	PRN1 6-0 = 1111110	inhibit
	PRN1 6-0 = 1111111	inhibit

Table 5.48: VinN11

Reference voltage	Macro adjustment value	VinN3 formula
VinN3	PKN0 4-0 = 00000	(47R / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00001	((47R – 1R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00010	((47R – 2R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00011	((47R – 3R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00100	((47R – 4R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00101	((47R – 5R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00110	((47R – 6R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 00111	((47R – 7R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01000	((47R – 8R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01001	((47R – 9R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01010	((47R - 10R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01011	((47R - 11R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01100	((47R - 12R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01101	((47R - 13R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01110	((47R - 14R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 01111	((47R - 15R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10000	((47R - 16R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10001	((47R - 17R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10010	((47R - 18R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10011	((47R - 19R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10100	((47R - 20R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10101	((47R - 21R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10110	((47R - 22R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 10111	((47R - 23R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11000	((47R - 24R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11001	((47R - 25R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11010	((47R - 26R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11011	((47R - 27R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11100	((47R - 28R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11101	((47R - 29R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11110	((47R - 30R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN0 4-0 = 11111	((47R - 31R) / 48R) * (VinN2 - VinN5) + VinN5

Table 5.49: VinN3

Reference voltage	Macro adjustment value	VinN4 formula
VinN4	PKN1 4-0 = 00000	(32R / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00001	((32R - 1R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00010	((32R - 2R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00011	((32R - 3R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00100	((32R - 4R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00101	((32R - 5R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00110	((32R - 6R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 00111	((32R - 7R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01000	((32R - 8R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01001	((32R - 9R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01010	((32R - 10R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01011	((32R - 11R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01100	((32R - 12R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01101	((32R - 13R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01110	((32R - 14R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 01111	((32R - 15R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10000	((32R - 16R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10001	((32R - 17R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10010	((32R - 18R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10011	((32R - 19R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10100	((32R - 20R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10101	((32R - 21R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10110	((32R - 22R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 10111	((32R - 23R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11000	((32R - 24R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11001	((32R - 25R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11010	((32R - 26R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11011	((32R - 27R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11100	((32R - 28R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11101	((32R - 29R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11110	((32R - 30R) / 48R) * (VinN2 - VinN5) + VinN5
	PKN1 4-0 = 11111	((32R - 31R) / 48R) * (VinN2 - VinN5) + VinN5

Table 5.50: VinN4

Reference voltage	Macro adjustment value	VinN6 formula
VinN6	PKN2 4-0 = 00000	(220R / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00001	((220R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00010	((220R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00011	((220R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00100	((220R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00101	((220R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00110	((220R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 00111	((220R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01000	((220R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01001	((220R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01010	((220R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01011	((220R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01100	((220R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01101	((220R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01110	((220R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 01111	((220R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10000	((220R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10001	((220R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10010	((220R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10011	((220R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10100	((220R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10101	((220R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10110	((220R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 10111	((220R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11000	((220R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11001	((220R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11010	((220R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11011	((220R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11100	((220R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11101	((220R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11110	((220R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN2 4-0 = 11111	((220R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.51: VinN6

Reference voltage	Macro adjustment value	VinN7 formula
VinN7	PKN3 4-0 = 00000	(193R / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00001	((193R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00010	((193R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00011	((193R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00100	((193R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00101	((193R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00110	((193R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 00111	((193R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01000	((193R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01001	((193R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01010	((193R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01011	((193R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01100	((193R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01101	((193R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01110	((193R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 01111	((193R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10000	((193R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10001	((193R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10010	((193R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10011	((193R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10100	((193R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10101	((193R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10110	((193R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 10111	((193R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11000	((193R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11001	((193R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11010	((193R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11011	((193R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11100	((193R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11101	((193R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11110	((193R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN3 4-0 = 11111	((193R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.52: VinN7

Reference voltage	Macro adjustment value	VinN8 formula
VinN8	PKN4 4-0 = 00000	(158R / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00001	((158R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00010	((158R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00011	((158R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00100	((158R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00101	((158R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00110	((158R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 00111	((158R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01000	((158R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01001	((158R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01010	((158R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01011	((158R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01100	((158R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01101	((158R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01110	((158R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 01111	((158R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10000	((158R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10001	((158R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10010	((158R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10011	((158R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10100	((158R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10101	((158R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10110	((158R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 10111	((158R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11000	((158R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11001	((158R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11010	((158R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11011	((158R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11100	((158R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11101	((158R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11110	((158R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN4 4-0 = 11111	((158R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.53: VinN8

Reference voltage	Macro adjustment value	VinN9 formula
VinN9	PKN5 4-0 = 00000	(123R / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00001	((123R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00010	((123R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00011	((123R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00100	((123R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00101	((123R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00110	((123R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 00111	((123R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01000	((123R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01001	((123R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01010	((123R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01011	((123R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01100	((123R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01101	((123R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01110	((123R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 01111	((123R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10000	((123R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10001	((123R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10010	((123R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10011	((123R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10100	((123R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10101	((123R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10110	((123R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 10111	((123R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11000	((123R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11001	((123R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11010	((123R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11011	((123R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11100	((123R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11101	((123R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11110	((123R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN5 4-0 = 11111	((123R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.54: VinN9

Reference voltage	Macro adjustment value	VinN10 formula
VinN10	PKN6 4-0 = 00000	(96R / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00001	((96R - 3R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00010	((96R - 6R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00011	((96R - 9R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00100	((96R - 12R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00101	((96R - 15R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00110	((96R - 18R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 00111	((96R - 21R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01000	((96R - 24R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01001	((96R - 27R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01010	((96R - 30R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01011	((96R - 33R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01100	((96R - 36R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01101	((96R - 39R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01110	((96R - 42R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 01111	((96R - 45R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10000	((96R - 48R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10001	((96R - 51R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10010	((96R - 54R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10011	((96R - 57R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10100	((96R - 60R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10101	((96R - 63R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10110	((96R - 66R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 10111	((96R - 69R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11000	((96R - 72R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11001	((96R - 75R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11010	((96R - 78R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11011	((96R - 81R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11100	((96R - 84R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11101	((96R - 87R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11110	((96R - 90R) / 223R) * (VinN5 - VinN11) + VinN11
	PKN6 4-0 = 11111	((96R - 93R) / 223R) * (VinN5 - VinN11) + VinN11

Table 5.55: VinN10

Reference voltage	Macro adjustment value	VinN12 formula
VinN12	PKN7 4-0 = 00000	(47R / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00001	((47R - 1R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00010	((47R - 2R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00011	((47R - 3R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00100	((47R - 4R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00101	((47R - 5R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00110	((47R - 6R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 00111	((47R - 7R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01000	((47R - 8R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01001	((47R - 9R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01010	((47R - 10R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01011	((47R - 11R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01100	((47R - 12R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01101	((47R - 13R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01110	((47R - 14R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 01111	((47R - 15R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10000	((47R - 16R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10001	((47R - 17R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10010	((47R - 18R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10011	((47R - 19R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10100	((47R - 20R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10101	((47R - 21R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10110	((47R - 22R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 10111	((47R - 23R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11000	((47R - 24R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11001	((47R - 25R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11010	((47R - 26R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11011	((47R - 27R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11100	((47R - 28R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11101	((47R - 29R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11110	((47R - 30R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN7 4-0 = 11111	((47R - 31R) / 48R) * (VinN11 - VinN14) + VinN14

Table 5.56: VinN12

Reference voltage	Macro adjustment value	VinN13 formula
VinN13	PKN8 4-0 = 00000	(32R / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00001	((32R - 1R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00010	((32R - 2R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00011	((32R - 3R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00100	((32R - 4R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00101	((32R - 5R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00110	((32R - 6R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 00111	((32R - 7R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01000	((32R - 8R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01001	((32R - 9R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01010	((32R - 10R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01011	((32R - 11R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01100	((32R - 12R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01101	((32R - 13R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01110	((32R - 14R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 01111	((32R - 15R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10000	((32R - 16R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10001	((32R - 17R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10010	((32R - 18R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10011	((32R - 19R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10100	((32R - 20R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10101	((32R - 21R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10110	((32R - 22R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 10111	((32R - 23R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11000	((32R - 24R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11001	((32R - 25R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11010	((32R - 26R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11011	((32R - 27R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11100	((32R - 28R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11101	((32R - 29R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11110	((32R - 30R) / 48R) * (VinN11 - VinN14) + VinN14
	PKN8 4-0 = 11111	((32R - 31R) / 48R) * (VinN11 - VinN14) + VinN14

Table 5.57: VinN13

Grayscale voltage	Formula
V0	VinP0
V1	VinP1
V2	VinP2
V3	VinP3
V4	CGMP0=0 = VinP3 - (VinP3 - VinP4)*(1R/4R) CGMP0=1 = VinP3 - (VinP3 - VinP4)*(3R/9.5R) CGMP0=2 = VinP3 - (VinP3 - VinP4)*(3.5R/9.3R) CGMP0=3 = VinP3 - (VinP3 - VinP4)*(3.5R/10R)
V5	CGMP0=0 = VinP3 - (VinP3 - VinP4)*(2R/4R) CGMP0=1 = VinP3 - (VinP3 - VinP4)*(5.5R/9.5R) CGMP0=2 = VinP3 - (VinP3 - VinP4)*(6R/9.3R) CGMP0=3 = VinP3 - (VinP3 - VinP4)*(6R/10R)
V6	CGMP0=0 = VinP3 - (VinP3 - VinP4)*(3R/4R) CGMP0=1 = VinP3 - (VinP3 - VinP4)*(7.5R/9.5R) CGMP0=2 = VinP3 - (VinP3 - VinP4)*(7.8R/9.3R) CGMP0=3= VinP3 - (VinP3 - VinP4)*(8R/10R)
V7	VinP4
V8	CGMP2=0 = VinP4 - (VinP4 - VinP5)*(1R/6R) CGMP2=1 = VinP4 - (VinP4 - VinP5)*(3R/16R) CGMP2=2 = VinP4 - (VinP4 - VinP5)*(4R/18R) CGMP2=3 = VinP4 - (VinP4 - VinP5)*(4.5R/19.5R)
V9	CGMP2=0 = VinP4 - (VinP4 - VinP5)*(2R/6R) CGMP2=1 = VinP4 - (VinP4 - VinP5)*(6R/16R) CGMP2=2 = VinP4 - (VinP4 - VinP5)*(7R/18R) CGMP2=3 = VinP4 - (VinP4 - VinP5)*(8.5R/19.5R)
V10	CGMP2=0 = VinP4 - (VinP4 - VinP5)*(3R/6R) CGMP2=1 = VinP4 - (VinP4 - VinP5)*(8.5R/16R) CGMP2=2 = VinP4 - (VinP4 - VinP5)*(10R/18R) CGMP2=3 = VinP4 - (VinP4 - VinP5)*(11.5R/19.5R)
V11	CGMP2=0 = VinP4 - (VinP4 - VinP5)*(4R/6R) CGMP2=1 = VinP4 - (VinP4 - VinP5)*(11R/16R) CGMP2=2 = VinP4 - (VinP4 - VinP5)*(13R/18R) CGMP2=3 = VinP4 - (VinP4 - VinP5)*(14.5R/19.5R)
V12	CGMP2=0 = VinP4 - (VinP4 - VinP5)*(5R/6R) CGMP2=1 = VinP4 - (VinP4 - VinP5)*(13.5R/16R) CGMP2=2 = VinP4 - (VinP4 - VinP5)*(15.5R/18R) CGMP2=3 = VinP4 - (VinP4 - VinP5)*(17R/19.5R)
V13	VinP5
V14	CGMP4=0 =VinP5 - (VinP5 - VinP6)*(1R/6R) CGMP4=1 =VinP5 - (VinP5 - VinP6)*(1.5R/6.5R)
V15	CGMP4=0 =VinP5 - (VinP5 - VinP6)*(2R/6R) CGMP4=1 =VinP5 - (VinP5 - VinP6)*(2.5R/6.5R)
V16	CGMP4=0 =VinP5 - (VinP5 - VinP6)*(3R/6R) CGMP4=1 =VinP5 - (VinP5 - VinP6)*(3.5R/6.5R)
V17	CGMP4=0 =VinP5 - (VinP5 - VinP6)*(4R/6R) CGMP4=1 =VinP5 - (VinP5 - VinP6)*(4.5R/6.5R)
V18	CGMP4=0 =VinP5 - (VinP5 - VinP6)*(5R/6R) CGMP4=1 =VinP5 - (VinP5 - VinP6)*(5.5R/6.5R)
V19	VinP6
V20	VinP6 - (VinP6 - VinP7)*(1R/6R)
V21	VinP6 - (VinP6 - VinP7)*(2R/6R)
V22	VinP6 - (VinP6 - VinP7)*(3R/6R)
V23	VinP6 - (VinP6 - VinP7)*(4R/6R)
V24	VinP6 - (VinP6 - VinP7)*(5R/6R)
V25	VinP7
V26	VinP7 - (VinP7 - VinP8)*(1R/7.5R)
V27	VinP7 - (VinP7 - VinP8)*(2R/7.5R)
V28	VinP7 - (VinP7 - VinP8)*(3R/7.5R)
V29	VinP7 - (VinP7 - VinP8)*(4R/7.5R)
V30	VinP7 - (VinP7 - VinP8)*(5R/7.5R)
V31	VinP7 - (VinP7 - VinP8)*(6R/7.5R)
V32	VinP8
V33	VinP8 - (VinP8 - VinP9)*(1R/6R)
V34	VinP8 - (VinP8 - VinP9)*(2R/6R)
V35	VinP8 - (VinP8 - VinP9)*(3R/6R)
V36	VinP8 - (VinP8 - VinP9)*(4R/6R)
V37	VinP8 - (VinP8 - VinP9)*(5R/6R)
V38	VinP9
V39	VinP9 - (VinP9 - VinP10)*(1R/6R)
V40	VinP9 - (VinP9 - VinP10)*(2R/6R)
V41	VinP9 - (VinP9 - VinP10)*(3R/6R)
V42	VinP9 - (VinP9 - VinP10)*(4R/6R)
V43	VinP9 - (VinP9 - VinP10)*(5R/6R)
V44	VinP10
V45	CGMP5=0 =VinP10 - (VinP10 - VinP11)*(1R/6R) CGMP5=1 =VinP10 - (VinP10 - VinP11)*(1R/6.5R)
V46	CGMP5=0 =VinP10 - (VinP10 - VinP11)*(2R/6R) CGMP5=1 =VinP10 - (VinP10 - VinP11)*(2R/6.5R)
V47	CGMP5=0 =VinP10 - (VinP10 - VinP11)*(3R/6R) CGMP5=1 =VinP10 - (VinP10 - VinP11)*(3R/6.5R)
V48	CGMP5=0 =VinP10 - (VinP10 - VinP11)*(4R/6R) CGMP5=1 =VinP10 - (VinP10 - VinP11)*(4R/6.5R)
V49	CGMP5=0 =VinP10 - (VinP10 - VinP11)*(5R/6R) CGMP5=1 =VinP10 - (VinP10 - VinP11)*(5R/6.5R)

Grayscale voltage	Formula
V50	VinP11
V51	CGMP3=0 = VinP11 - (VinP11 - VinP12)*(1R/6R) CGMP3=1 = VinP11 - (VinP11 - VinP12)*(2.5R/16R) CGMP3=2 = VinP11 - (VinP11 - VinP12)*(2.5R/18R) CGMP3=3 = VinP11 - (VinP11 - VinP12)* (2.5R/19.5R)
V52	CGMP3=0 = VinP11 - (VinP11- VinP12)*(2R/6R) CGMP3=1 = VinP11 - (VinP11 - VinP12)*(5R/16R) CGMP3=2 = VinP11 - (VinP11 - VinP12)*(5R/18R) CGMP3=3 = VinP11 - (VinP11 - VinP12)*(5R/19.5R)
V53	CGMP3=0 = VinP11 - (VinP11 - VinP12)*(3R/6R) CGMP3=1 = VinP11 - (VinP11 - VinP12)*(7.5R/16R) CGMP3=2 = VinP11 - (VinP11 - VinP12)*(8R/18R) CGMP3=3 = VinP11 - (VinP11 - VinP12)*(8R/19.5R)
V54	CGMP3=0 = VinP11 - (VinP11 - VinP12)*(4R/6R) CGMP3=1 = VinP11 - (VinP11 - VinP12)*(10R/16R) CGMP3=2 = VinP11 - (VinP11 - VinP12)*(11R/18R) CGMP3=3 = VinP11 - (VinP11 - VinP12)* (11R/19.5R)
V55	CGMP3=0 = VinP11 - (VinP11- VinP12)*(5R/6R) CGMP3=1 = VinP11 - (VinP11 - VinP12)*(13R/16R) CGMP3=2 = VinP11 - (VinP11 - VinP12)*(14R/18R) CGMP3=3 = VinP11 - (VinP11 - VinP12)* (15R/19.5R)

Grayscale voltage	Formula
V56	VinP12
V57	CGMP1=0 = VinP12 - (VinP12 – VinP13)*(1R/4R) CGMP1=1 = VinP12 - (VinP12 – VinP13)*(2R/9.5R) CGMP1=2 = VinP12 - (VinP12 – VinP13)*(1.5R/9.3R) CGMP1=3 = VinP12 - (VinP12 – VinP13)*(2R/10R)
V58	CGMP1=0 = VinP12 - (VinP12 – VinP13)*(2R/4R) CGMP1=1 = VinP12 - (VinP12 – VinP13)*(4R/9.5R) CGMP1=2 = VinP12 - (VinP12 – VinP13)*(3.3R/9.3R) CGMP1=3 = VinP12 - (VinP12 – VinP13)*(4R/10R)
V59	CGMP1=0 = VinP12 - (VinP12 – VinP13)*(3R/4R) CGMP1=1 = VinP12 - (VinP12 – VinP13)*(6.5R/9.5R) CGMP1=2 = VinP12 - (VinP12 – VinP13)*(5.8R/9.3R) CGMP1=3= VinP12 - (VinP12 – VinP13)*(6.5R/10R)
V60	VinP13
V61	VinP14
V62	VinP15
V63	VinP16

Table 5.58: Voltage calculation formula of 64-grayscale voltage (positive polarity)

Grayscale voltage	Formula
V0	VinN0
V1	VinN1
V2	VinN2
V3	VinN3
V4	CGMN0=0 = VinN3 - (VinN3 - VinN4)*(1R/4R) CGMN0=1 = VinN3 - (VinN3 - VinN4)*(3R/9.5R) CGMN0=2 = VinN3 - (VinN3 - VinN4)*(3.5R/9.3R) CGMN0=3 = VinN3 - (VinN3 - VinN4)*(3.5R/10R)
V5	CGMN0=0 = VinN3 - (VinN3 - VinN4)*(2R/4R) CGMN0=1 = VinN3 - (VinN3 - VinN4)*(5.5R/9.5R) CGMN0=2 = VinN3 - (VinN3 - VinN4)*(6R/9.3R) CGMN0=3 = VinN3 - (VinN3 - VinN4)*(6R/10R)
V6	CGMN0=0 = VinN3 - (VinN3 - VinN4)*(3R/4R) CGMN0=1 = VinN3 - (VinN3 - VinN4)*(7.5R/9.5R) CGMN0=2 = VinN3 - (VinN3 - VinN4)*(7.8R/9.3R) CGMN0=3= VinN3 - (VinN3 - VinN4)*(8R/10R)
V7	VinN4
V8	CGMN2=0 = VinN4 - (VinN4 - VinN5)*(1R/6R) CGMN2=1 = VinN4 - (VinN4 - VinN5)*(3R/16R) CGMN2=2 = VinN4 - (VinN4 - VinN5)*(4R/18R) CGMN2=3 = VinN4 - (VinN4 - VinN5)*(4.5R/19.5R)
V9	CGMN2=0 = VinN4 - (VinN4 - VinN5)*(2R/6R) CGMN2=1 = VinN4 - (VinN4 - VinN5)*(6R/16R) CGMN2=2 = VinN4 - (VinN4 - VinN5)*(7R/18R) CGMN2=3 = VinN4 - (VinN4 - VinN5)*(8.5R/19.5R)
V10	CGMN2=0 = VinN4 - (VinN4 - VinN5)*(3R/6R) CGMN2=1 = VinN4 - (VinN4 - VinN5)*(8.5R/16R) CGMN2=2 = VinN4 - (VinN4 - VinN5)*(10R/18R) CGMN2=3 = VinN4 - (VinN4 - VinN5)*(11.5R/19.5R)
V11	CGMN2=0 = VinN4 - (VinN4 - VinN5)*(4R/6R) CGMN2=1 = VinN4 - (VinN4 - VinN5)*(11R/16R) CGMN2=2 = VinN4 - (VinN4 - VinN5)*(13R/18R) CGMN2=3 = VinN4 - (VinN4 - VinN5)*(14.5R/19.5R)
V12	CGMN2=0 = VinN4 - (VinN4 - VinN5)*(5R/6R) CGMN2=1 = VinN4 - (VinN4 - VinN5)*(13.5R/16R) CGMN2=2 = VinN4 - (VinN4 - VinN5)*(15.5R/18R) CGMN2=3 = VinN4 - (VinN4 - VinN5)*(17R/19.5R)
V13	VinN5
V14	CGMN4=0 =VinN5 - (VinN5 - VinN6)*(1R/6R) CGMN4=1 =VinN5 - (VinN5 - VinN6)*(1.5R/6.5R)
V15	CGMN4=0 =VinN5 - (VinN5 - VinN6)*(2R/6R) CGMN4=1 =VinN5 - (VinN5 - VinN6)*(2.5R/6.5R)

Grayscale voltage	Formula
V16	CGMN4=0 =VinN5 - (VinN5 - VinN6)*(3R/6R) CGMN4=1 =VinN5 - (VinN5 - VinN6)*(3.5R/6.5R)
V17	CGMN4=0 =VinN5 - (VinN5 - VinN6)*(4R/6R) CGMN4=1 =VinN5 - (VinN5 - VinN6)*(4.5R/6.5R)
V18	CGMN4=0 =VinN5 - (VinN5 - VinN6)*(5R/6R) CGMN4=1 =VinN5 - (VinN5 - VinN6)*(5.5R/6.5R)
V19	VinN6
V20	VinN6 - (VinN6 - VinN7)*(1R/6R)
V21	VinN6 - (VinN6 - VinN7)*(2R/6R)
V22	VinN6 - (VinN6 - VinN7)*(3R/6R)
V23	VinN6 - (VinN6 - VinN7)*(4R/6R)
V24	VinN6 - (VinN6 - VinN7)*(5R/6R)
V25	VinP7
V26	VinP7 - (VinP7 - VinP8)*(1R/7.5R)
V27	VinP7 - (VinP7 - VinP8)*(2R/7.5R)
V28	VinP7 - (VinP7 - VinP8)*(3R/7.5R)
V29	VinP7 - (VinP7 - VinP8)*(4R/7.5R)
V30	VinP7 - (VinP7 - VinP8)*(5R/7.5R)
V31	VinP7 - (VinP7 - VinP8)*(6R/7.5R)
V32	VinP8
V33	VinP8 - (VinP8 - VinP9)*(1R/6R)
V34	VinP8 - (VinP8 - VinP9)*(2R/6R)
V35	VinP8 - (VinP8 - VinP9)*(3R/6R)
V36	VinP8 - (VinP8 - VinP9)*(4R/6R)
V37	VinP8 - (VinP8 - VinP9)*(5R/6R)
V38	VinN9
V39	VinN9 - (VinN9 - VinN10)*(1R/6R)
V40	VinN9 - (VinN9 - VinN10)*(2R/6R)
V41	VinN9 - (VinN9 - VinN10)*(3R/6R)
V42	VinN9 - (VinN9 - VinN10)*(4R/6R)
V43	VinN9 - (VinN9 - VinN10)*(5R/6R)
V44	VinN10
V45	CGMN5=0 =VinN10 - (VinN10 - VinN11)*(1R/6R) CGMN5=1 =VinN10 - (VinN10 - VinN11)*(1R/6.5R)
V46	CGMN5=0 =VinN10 - (VinN10 - VinN11)*(2R/6R) CGMN5=1 =VinN10 - (VinN10 - VinN11)*(2R/6.5R)
V47	CGMN5=0 =VinN10 - (VinN10 - VinN11)*(3R/6R) CGMN5=1 =VinN10 - (VinN10 - VinN11)*(3R/6.5R)
V48	CGMN5=0 =VinN10 - (VinN10 - VinN11)*(4R/6R) CGMN5=1 =VinN10 - (VinN10 - VinN11)*(4R/6.5R)
V49	CGMN5=0 =VinN10 - (VinN10 - VinN11)*(5R/6R) CGMN5=1 =VinN10 - (VinN10 - VinN11)*(5R/6.5R)

Grayscale voltage	Formula
V50	VinN11
V51	CGMN3=0 = VinN11 - (VinN11 - VinN12)*(1R/6R) CGMN3=1 = VinN11 - (VinN11 - VinN12)*(2.5R/16R) CGMN3=2 = VinN11 - (VinN11 - VinN12)*(2.5R/18R) CGMN3=3 = VinN11 - (VinN11 - VinN12)*(2.5R/19.5R)
V52	CGMN3=0 = VinN11 - (VinN11- VinN12)*(2R/6R) CGMN3=1 = VinN11 - (VinN11 - VinN12)*(5R/16R) CGMN3=2 = VinN11 - (VinN11 - VinN12)*(5R/18R) CGMN3=3 = VinN11 - (VinN11 - VinN12)*(5R/19.5R)
V53	CGMN3=0 = VinN11 - (VinN11 - VinN12)*(3R/6R) CGMN3=1 = VinN11 - (VinN11 - VinN12)*(7.5R/16R) CGMN3=2 = VinN11 - (VinN11 - VinN12)*(8R/18R) CGMN3=3 = VinN11 - (VinN11 - VinN12)*(8R/19.5R)
V54	CGMN3=0 = VinN11 - (VinN11 - VinN12)*(4R/6R) CGMN3=1 = VinN11 - (VinN11 - VinN12)*(10R/16R) CGMN3=2 = VinN11 - (VinN11 - VinN12)*(11R/18R) CGMN3=3 = VinN11 - (VinN11 - VinN12)*(11R/19.5R)
V55	CGMN3=0 = VinN11 - (VinN11- VinN12)*(5R/6R) CGMN3=1 = VinN11 - (VinN11 - VinN12)*(13R/16R) CGMN3=2 = VinN11 - (VinN11 - VinN12)*(14R/18R) CGMN3=3 = VinN11 - (VinN11 - VinN12)*(15R/19.5R)

Grayscale voltage	Formula
V56	VinN12
V57	CGMN1=0 = VinN12 - (VinN12 – VinN13)*(1R/4R) CGMN1=1 = VinN12 - (VinN12 – VinN13)*(2R/9.5R) CGMN1=2 = VinN12 - (VinN12 – VinN13)*(1.5R/9.3R) CGMN1=3 = VinN12 - (VinN12 – VinN13)*(2R/10R)
V58	CGMN1=0 = VinN12 - (VinN12 – VinN13)*(2R/4R) CGMN1=1 = VinN12 - (VinN12 – VinN13)*(4R/9.5R) CGMN1=2 = VinN12 - (VinN12 – VinN13)*(3.3R/9.3R) CGMN1=3 = VinN12 - (VinN12 – VinN13)*(4R/10R)
V59	CGMN1=0 = VinN12 - (VinN12 – VinN13)*(3R/4R) CGMN1=1 = VinN12 - (VinN12 – VinN13)*(6.5R/9.5R) CGMN1=2 = VinN12 - (VinN12 – VinN13)*(5.8R/9.3R) CGMN1=3= VinN12 - (VinN12 – VinN13)*(6.5R/10R)
V60	VinN13
V61	VinN14
V62	VinN15
V63	VinN16

Table 5.59: Voltage calculation formula of 64-grayscale voltage (negative polarity)

Grayscale voltage	Formula
VV0	V0
VV1	V0 - (V0 - V1)*(4R/16R)
VV2	V0 - (V0 - V1)*(8R/16R)
VV3	V0 - (V0 - V1)*(12R/16R)
VV4	V1
VV5	V1 - (V1 - V2)*(4R/16R)
VV6	V1 - (V1 - V2)*(8R/16R)
VV7	V1 - (V1 - V2)*(12R/16R)
VV8	V2
VV9	V2 - (V2 - V3)*(4R/16R)
VV10	V2 - (V2 - V3)*(8R/16R)
VV11	V2 - (V2 - V3)*(12R/16R)
VV12	V3
VV13	V3 - (V3 - V4)*(2R/8R)
VV14	V3 - (V3 - V4)*(4R/8R)
VV15	V3 - (V3 - V4)*(6R/8R)
VV16	V4
VV17	V4 - (V4 - V5)*(2R/8R)
VV18	V4 - (V4 - V5)*(4R/8R)
VV19	V4 - (V4 - V5)*(6R/8R)
VV20	V5
VV21	V5 - (V5 - V6)*(2R/8R)
VV22	V5 - (V5 - V6)*(4R/8R)
VV23	V5 - (V5 - V6)*(6R/8R)
VV24	V6
VV25	V6 - (V6 - V7)*(2R/8R)
VV26	V6 - (V6 - V7)*(4R/8R)
VV27	V6 - (V6 - V7)*(6R/8R)
VV28	V7
VV29	V7 - (V7 - V8)*(1.6R/6.4R)
VV30	V7 - (V7 - V8)*(3.2R/6.4R)
VV31	V7 - (V7 - V8)*(4.8R/6.4R)
VV32	V8
VV33	V8 - (V8 - V9)*(1.6R/6.4R)
VV34	V8 - (V8 - V9)*(3.2R/6.4R)
VV35	V8 - (V8 - V9)*(4.8R/6.4R)
VV36	V9
VV37	V9 - (V9 - V10)*(1.6R/6.4R)
VV38	V9 - (V9 - V10)*(3.2R/6.4R)
VV39	V9 - (V9 - V10)*(4.8R/6.4R)
VV40	V10
VV41	V10 - (V10 - V11)*(1.6R/6.4R)
VV42	V10 - (V10 - V11)*(3.2R/6.4R)
VV43	V10 - (V10 - V11)*(4.8R/6.4R)

Grayscale voltage	Formula
VV44	V11
VV45	V11 - (V11 - V12)*(1.6R/6.4R)
VV46	V11 - (V11 - V12)*(3.2R/6.4R)
VV47	V11 - (V11 - V12)*(4.8R/6.4R)
VV48	V12
VV49	V12 - (V12 - V13)*(1.6R/6.4R)
VV50	V12 - (V12 - V13)*(3.2R/6.4R)
VV51	V12 - (V12 - V13)*(4.8R/6.4R)
VV52	V13
VV53	V13 - (V13 - V14)*(1.6R/6.4R)
VV54	V13 - (V13 - V14)*(3.2R/6.4R)
VV55	V13 - (V13 - V14)*(4.8R/6.4R)
VV56	V14
VV57	V14 - (V14 - V15)*(1.6R/6.4R)
VV58	V14 - (V14 - V15)*(3.2R/6.4R)
VV59	V14 - (V14 - V15)*(4.8R/6.4R)
VV60	V15
VV61	V15 - (V15 - V16)*(1.6R/6.4R)
VV62	V15 - (V15 - V16)*(3.2R/6.4R)
VV63	V15 - (V15 - V16)*(4.8R/6.4R)
VV64	V16
VV65	V16 - (V16 - V17)*(1.6R/6.4R)
VV66	V16 - (V16 - V17)*(3.2R/6.4R)
VV67	V16 - (V16 - V17)*(4.8R/6.4R)
VV68	V17
VV69	V17 - (V17 - V18)*(1.6R/6.4R)
VV70	V17 - (V17 - V18)*(3.2R/6.4R)
VV71	V17 - (V17 - V18)*(4.8R/6.4R)
VV72	V18
VV73	V18 - (V18 - V19)*(1.6R/6.4R)
VV74	V18 - (V18 - V19)*(3.2R/6.4R)
VV75	V18 - (V18 - V19)*(4.8R/6.4R)
VV76	V19
VV77	V19 - (V19 - V20)*(1.6R/6.4R)
VV78	V19 - (V19 - V20)*(3.2R/6.4R)
VV79	V19 - (V19 - V20)*(4.8R/6.4R)
VV80	V20
VV81	V20 - (V20 - V21)*(1.6R/6.4R)
VV82	V20 - (V20 - V21)*(3.2R/6.4R)
VV83	V20 - (V20 - V21)*(4.8R/6.4R)
VV84	V21
VV85	V21 - (V21 - V22)*(1.6R/6.4R)
VV86	V21 - (V21 - V22)*(3.2R/6.4R)
VV87	V21 - (V21 - V22)*(4.8R/6.4R)

Grayscale voltage	Formula
VV88	V22
VV89	V22 - (V22 - V23)*(1.6R/6.4R)
VV90	V22 - (V22 - V23)*(3.2R/6.4R)
VV91	V22 - (V22 - V23)*(4.8R/6.4R)
VV92	V23
VV93	V23 - (V23 - V24)*(1.6R/6.4R)
VV94	V23 - (V23 - V24)*(3.2R/6.4R)
VV95	V23 - (V23 - V24)*(4.8R/6.4R)
VV96	V24
VV97	V24 - (V24 - V25)*(1.6R/6.4R)
VV98	V24 - (V24 - V25)*(3.2R/6.4R)
VV99	V24 - (V24 - V25)*(4.8R/6.4R)
VV100	V25
VV101	V25 - (V25 - V26)*(1.6R/6.4R)
VV102	V25 - (V25 - V26)*(3.2R/6.4R)
VV103	V25 - (V25 - V26)*(4.8R/6.4R)
VV104	V26
VV105	V26 - (V26 - V27)*(1.6R/6.4R)
VV106	V26 - (V26 - V27)*(3.2R/6.4R)
VV107	V26 - (V26 - V27)*(4.8R/6.4R)
VV108	V27
VV109	V27 - (V27 - V28)*(1.6R/6.4R)
VV110	V27 - (V27 - V28)*(3.2R/6.4R)
VV111	V27 - (V27 - V28)*(4.8R/6.4R)
VV112	V28
VV113	V28 - (V28 - V29)*(1.6R/6.4R)
VV114	V28 - (V28 - V29)*(3.2R/6.4R)
VV115	V28 - (V28 - V29)*(4.8R/6.4R)
VV116	V29
VV117	V29 - (V29 - V30)*(1.6R/6.4R)
VV118	V29 - (V29 - V30)*(3.2R/6.4R)
VV119	V29 - (V29 - V30)*(4.8R/6.4R)
VV120	V30
VV121	V30 - (V30 - V31)*(1.6R/6.4R)
VV122	V30 - (V30 - V31)*(3.2R/6.4R)
VV123	V30 - (V30 - V31)*(4.8R/6.4R)
VV124	V31
VV125	V31 - (V31 - V32)*(1.6R/11.2R)
VV126	V31 - (V31 - V32)*(3.2R/11.2R)
VV127	V31 - (V31 - V32)*(4.8R/11.2R)
VV128	V31 - (V31 - V32)*(6.4R/11.2R)
VV129	V31 - (V31 - V32)*(8R/11.2R)
VV130	V31 - (V31 - V32)*(9.6R/11.2R)
VV131	V32

Grayscale voltage	Formula
VV132	V32 - (V32 - V33)*(1.6R/6.4R)
VV133	V32 - (V32 - V33)*(3.2R/6.4R)
VV134	V32 - (V32 - V33)*(4.8R/6.4R)
VV135	V33
VV136	V33 - (V33 - V34)*(1.6R/6.4R)
VV137	V33 - (V33 - V34)*(3.2R/6.4R)
VV138	V33 - (V33 - V34)*(4.8R/6.4R)
VV139	V34
VV140	V34 - (V34 - V35)*(1.6R/6.4R)
VV141	V34 - (V34 - V35)*(3.2R/6.4R)
VV142	V34 - (V34 - V35)*(4.8R/6.4R)
VV143	V35
VV144	V35 - (V35 - V36)*(1.6R/6.4R)
VV145	V35 - (V35 - V36)*(3.2R/6.4R)
VV146	V35 - (V35 - V36)*(4.8R/6.4R)
VV147	V36
VV148	V36 - (V36 - V37)*(1.6R/6.4R)
VV149	V36 - (V36 - V37)*(3.2R/6.4R)
VV150	V36 - (V36 - V37)*(4.8R/6.4R)
VV151	V37
VV152	V37 - (V37 - V38)*(1.6R/6.4R)
VV153	V37 - (V37 - V38)*(3.2R/6.4R)
VV154	V37 - (V37 - V38)*(4.8R/6.4R)
VV155	V38
VV156	V38 - (V38 - V39)*(1.6R/6.4R)
VV157	V38 - (V38 - V39)*(3.2R/6.4R)
VV158	V38 - (V38 - V39)*(4.8R/6.4R)
VV159	V39
VV160	V39 - (V39 - V40)*(1.6R/6.4R)
VV161	V39 - (V39 - V40)*(3.2R/6.4R)
VV162	V39 - (V39 - V40)*(4.8R/6.4R)
VV163	V40
VV164	V40 - (V40 - V41)*(1.6R/6.4R)
VV165	V40 - (V40 - V41)*(3.2R/6.4R)
VV166	V40 - (V40 - V41)*(4.8R/6.4R)
VV167	V41
VV168	V41 - (V41 - V42)*(1.6R/6.4R)
VV169	V41 - (V41 - V42)*(3.2R/6.4R)
VV170	V41 - (V41 - V42)*(4.8R/6.4R)
VV171	V42
VV172	V42 - (V42 - V43)*(1.6R/6.4R)
VV173	V42 - (V42 - V43)*(3.2R/6.4R)
VV174	V42 - (V42 - V43)*(4.8R/6.4R)
VV175	V43

Grayscale voltage	Formula
VV176	V43 - (V43 - V44)*(1.6R/6.4R)
VV177	V43 - (V43 - V44)*(3.2R/6.4R)
VV178	V43 - (V43 - V44)*(4.8R/6.4R)
VV179	V44
VV180	V44 - (V44 - V45)*(1.6R/6.4R)
VV181	V44 - (V44 - V45)*(3.2R/6.4R)
VV182	V44 - (V44 - V45)*(4.8R/6.4R)
VV183	V45
VV184	V45 - (V45 - V46)*(1.6R/6.4R)
VV185	V45 - (V45 - V46)*(3.2R/6.4R)
VV186	V45 - (V45 - V46)*(4.8R/6.4R)
VV187	V46
VV188	V46 - (V46 - V47)*(1.6R/6.4R)
VV189	V46 - (V46 - V47)*(3.2R/6.4R)
VV190	V46 - (V46 - V47)*(4.8R/6.4R)
VV191	V47
VV192	V47 - (V47 - V48)*(1.6R/6.4R)
VV193	V47 - (V47 - V48)*(3.2R/6.4R)
VV194	V47 - (V47 - V48)*(4.8R/6.4R)
VV195	V48
VV196	V48 - (V48 - V49)*(1.6R/6.4R)
VV197	V48 - (V48 - V49)*(3.2R/6.4R)
VV198	V48 - (V48 - V49)*(4.8R/6.4R)
VV199	V49
VV200	V49 - (V49 - V50)*(1.6R/6.4R)
VV201	V49 - (V49 - V50)*(3.2R/6.4R)
VV202	V49 - (V49 - V50)*(4.8R/6.4R)
VV203	V50
VV204	V50 - (V50 - V51)*(1.6R/6.4R)
VV205	V50 - (V50 - V51)*(3.2R/6.4R)
VV206	V50 - (V50 - V51)*(4.8R/6.4R)
VV207	V51
VV208	V51 - (V51 - V52)*(1.6R/6.4R)
VV209	V51 - (V51 - V52)*(3.2R/6.4R)
VV210	V51 - (V51 - V52)*(4.8R/6.4R)
VV211	V52
VV212	V52 - (V52 - V53)*(1.6R/6.4R)
VV213	V52 - (V52 - V53)*(3.2R/6.4R)
VV214	V52 - (V52 - V53)*(4.8R/6.4R)
VV215	V53

Grayscale voltage	Formula
VV216	V53 - (V53 - V54)*(1.6R/6.4R)
VV217	V53 - (V53 - V54)*(3.2R/6.4R)
VV218	V53 - (V53 - V54)*(4.8R/6.4R)
VV219	V54
VV220	V54 - (V54 - V55)*(1.6R/6.4R)
VV221	V54 - (V54 - V55)*(3.2R/6.4R)
VV222	V54 - (V54 - V55)*(4.8R/6.4R)
VV223	V55
VV224	V55 - (V55 - V56)*(1.6R/6.4R)
VV225	V55 - (V55 - V56)*(3.2R/6.4R)
VV226	V55 - (V55 - V56)*(4.8R/6.4R)
VV227	V56
VV228	V56 - (V56 - V57)*(2R/8R)
VV229	V56 - (V56 - V57)*(4R/8R)
VV230	V56 - (V56 - V57)*(6R/8R)
VV231	V57
VV232	V57 - (V57 - V58)*(2R/8R)
VV233	V57 - (V57 - V58)*(4R/8R)
VV234	V57 - (V57 - V58)*(6R/8R)
VV235	V58
VV236	V58 - (V58 - V59)*(2R/8R)
VV237	V58 - (V58 - V59)*(4R/8R)
VV238	V58 - (V58 - V59)*(6R/8R)
VV239	V59
VV240	V59 - (V59 - V60)*(2R/8R)
VV241	V59 - (V59 - V60)*(4R/8R)
VV242	V59 - (V59 - V60)*(6R/8R)
VV243	V60
VV244	V60 - (V60 - V61)*(4R/16R)
VV245	V60 - (V60 - V61)*(8R/16R)
VV246	V60 - (V60 - V61)*(12R/16R)
VV247	V61
VV248	V61 - (V61 - V62)*(4R/16R)
VV249	V61 - (V61 - V62)*(8R/16R)
VV250	V61 - (V61 - V62)*(12R/16R)
VV251	V62
VV252	V62 - (V62 - V63)*(4R/16R)
VV253	V62 - (V62 - V63)*(8R/16R)
VV254	V62 - (V62 - V63)*(12R/16R)
VV255	V63

Table 5.60: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity)

5.13Characteristics of I/O

5.13.1 Output or bi-directional (I/O) pins

Output or bi-directional pins	After power on	After hardware reset	After software reset
TE	Low	Low	Low
DB23 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CABC_PWM_OUT	Low	Low	Low

Table 5.61 Characteristics of output or bi-directional (I/O) pins

5.13.2 Input pins

Input pins	During power on process	After power on	After hardware reset	After software reset	During power off process
RESX	Setion.5.18	Input valid	Input valid	Input valid	Setion.5.18
CSX	Input valid	Input valid	Input valid	Input valid	Input valid
DCX_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
WRX_DCX	Input valid	Input valid	Input valid	Input valid	Input valid
RDX_E	Input valid	Input valid	Input valid	Input valid	Input valid
DB23 to DB0 SDI	Input valid	Input valid	Input valid	Input valid	Input valid
HSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
PCLK	Input valid	Input valid	Input valid	Input valid	Input valid
DE	Input valid	Input valid	Input valid	Input valid	Input valid
OSC, BS3, BS2, BS1, BS0,	Input valid	Input valid	Input valid	Input valid	Input valid
TEST2-1	Low	Low	Low	Low	Low

Table 5.62 Characteristics of input pins

5.14GIP control singal

HX8369-A02 is a single chip solution for a WVGA GIP (Gate In Panel) type TFT LCD display. There are many GIP/ASG type TFT panels that correspond to different GIP timing. Therefore, the GIP setting must be setup to the correct GIP/ASG timing for the normal display. The GIP timing adjustment is related to register 0xD5h SETGIP.

The GIP control signals (GOUT[1~10]_L and GOUT[1~10]_R) is for panel used. The assignment of each panel type is specified on the application note. Regarding the GIP/ASG timing, please refer to HX8369-A02 application note.

5.15Sleep Out –command and self-diagnostic functions of the display module

5.15.1 Register loading detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1).
The flow chart for this internal function is following:

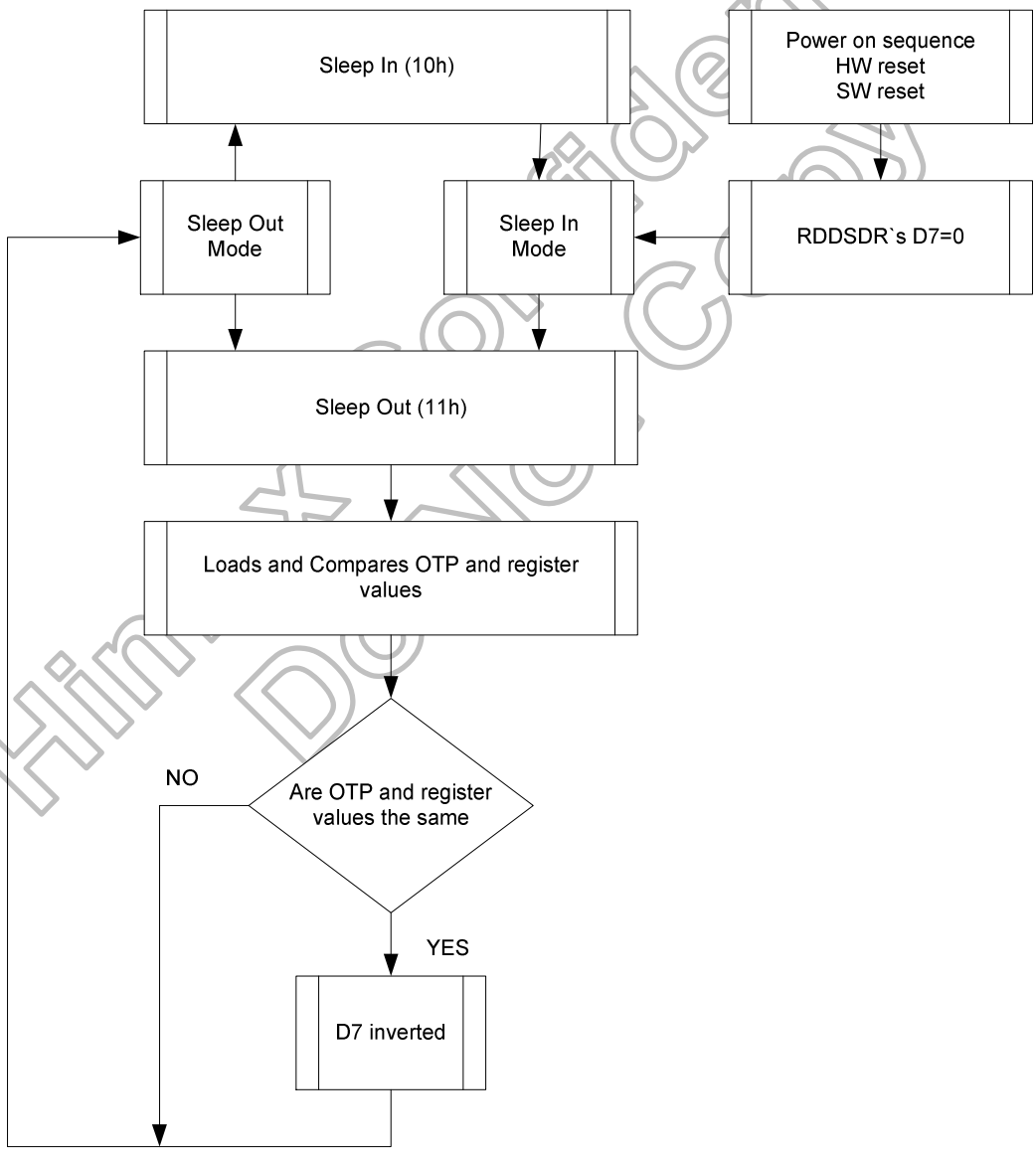
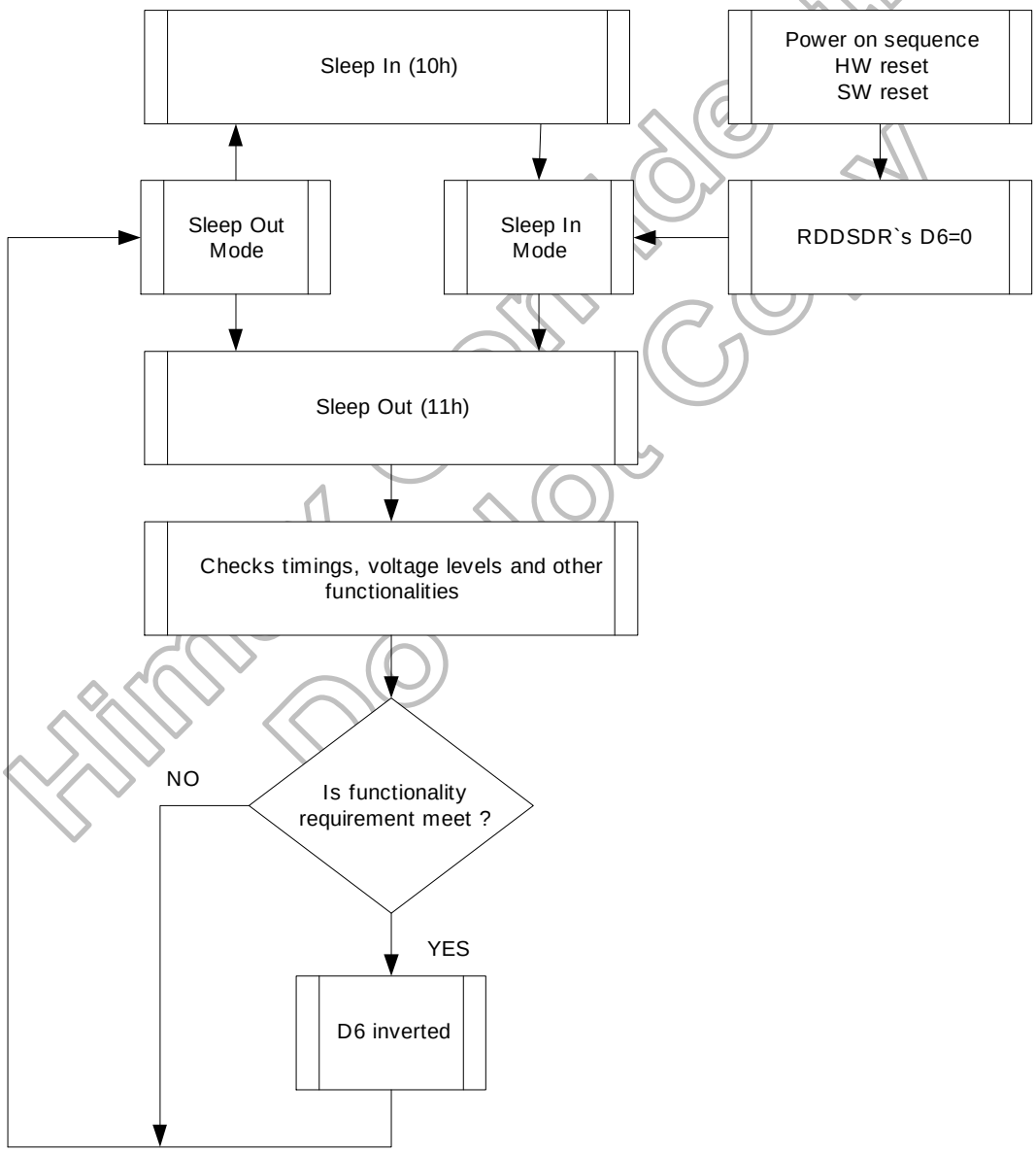


Figure 5.33: Sleep out flow chart–command and self-diagnostic functions

5.15.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.
The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In–mode toSleep Out -mode, before there is possible to check if Customer’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5.34: Sleep out flow chart internal function detection

5.16 Power on/off sequence

VDD1, VDD2 and VDD3 can be applied in any order. VDD1, VDD2 and VDD3 can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VDD1 and VDD2 must be powered down minimum 120msec after RESX has been released. During power off, if LCD is in the Sleep In mode, VDD1, VDD2 and VDD3 can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.16.1 and 5.16.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

5.16.1 Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

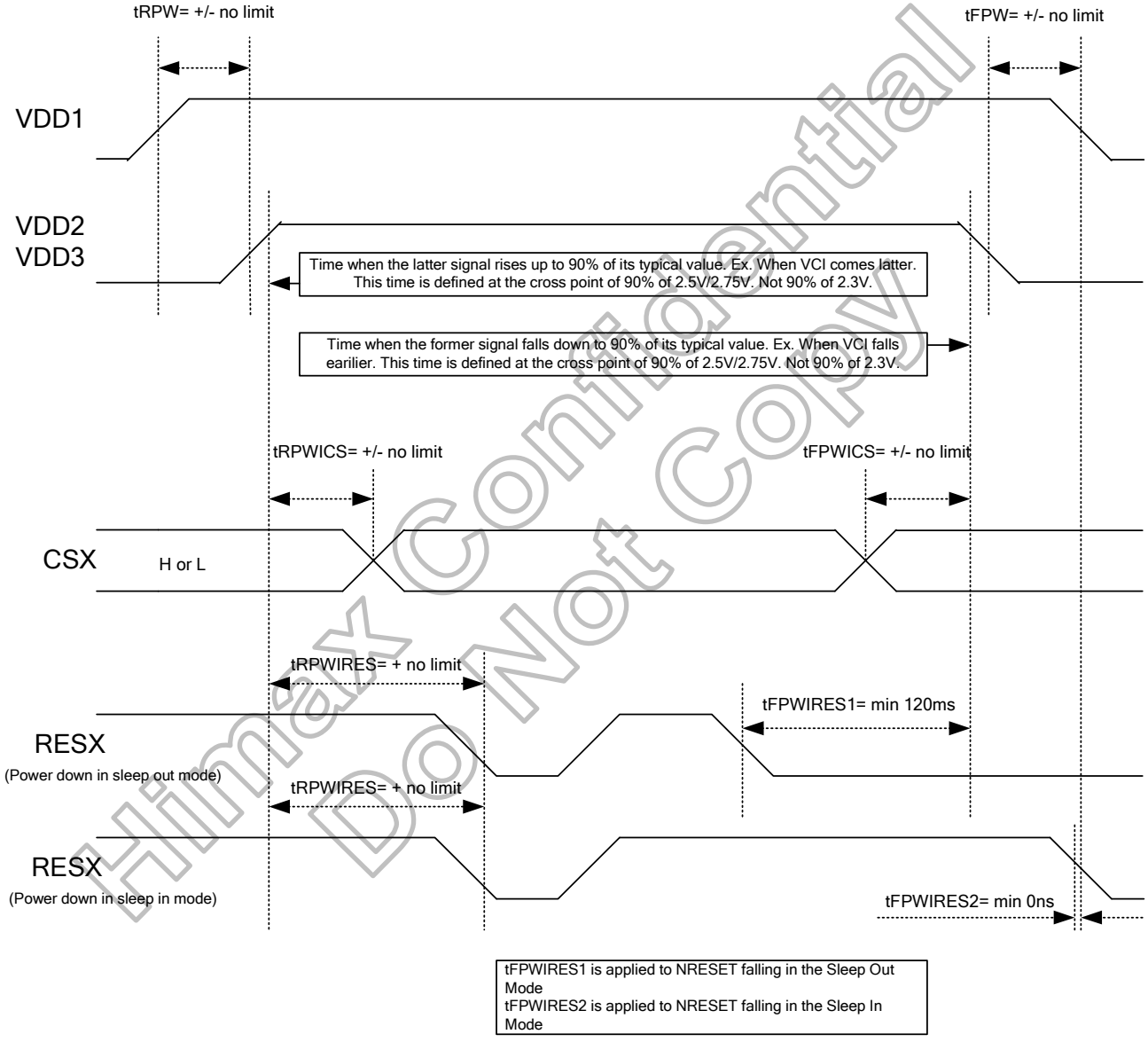


Figure 5.35: Case 1: RESX line is held high or unstable by host at power on

5.16.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.

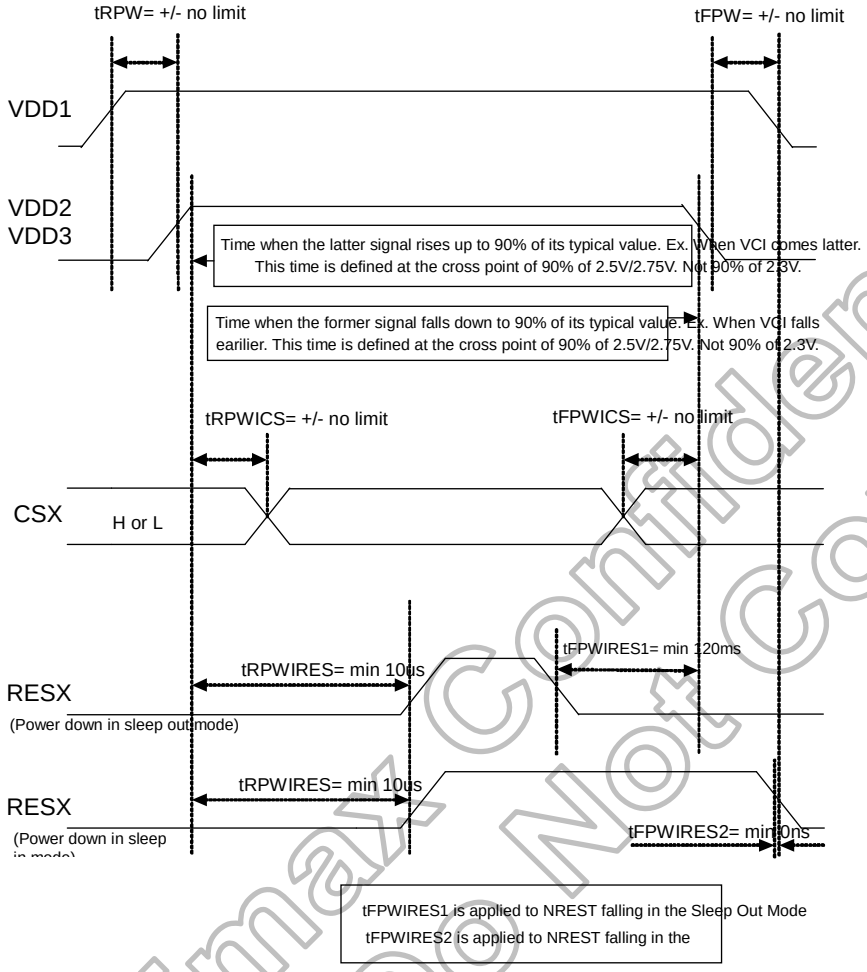
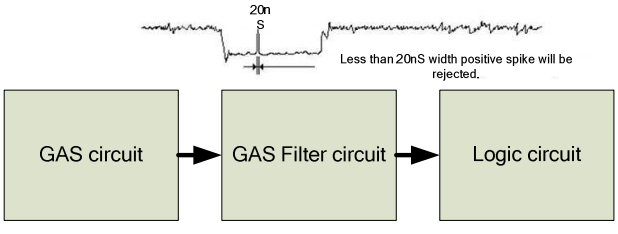


Figure 5.36: Case 2: RESX line is held low by host at power on

5.17 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

Note: HX8369-A02 is support the noise reject filter (20ns) to reject spike or noise.



5.18Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

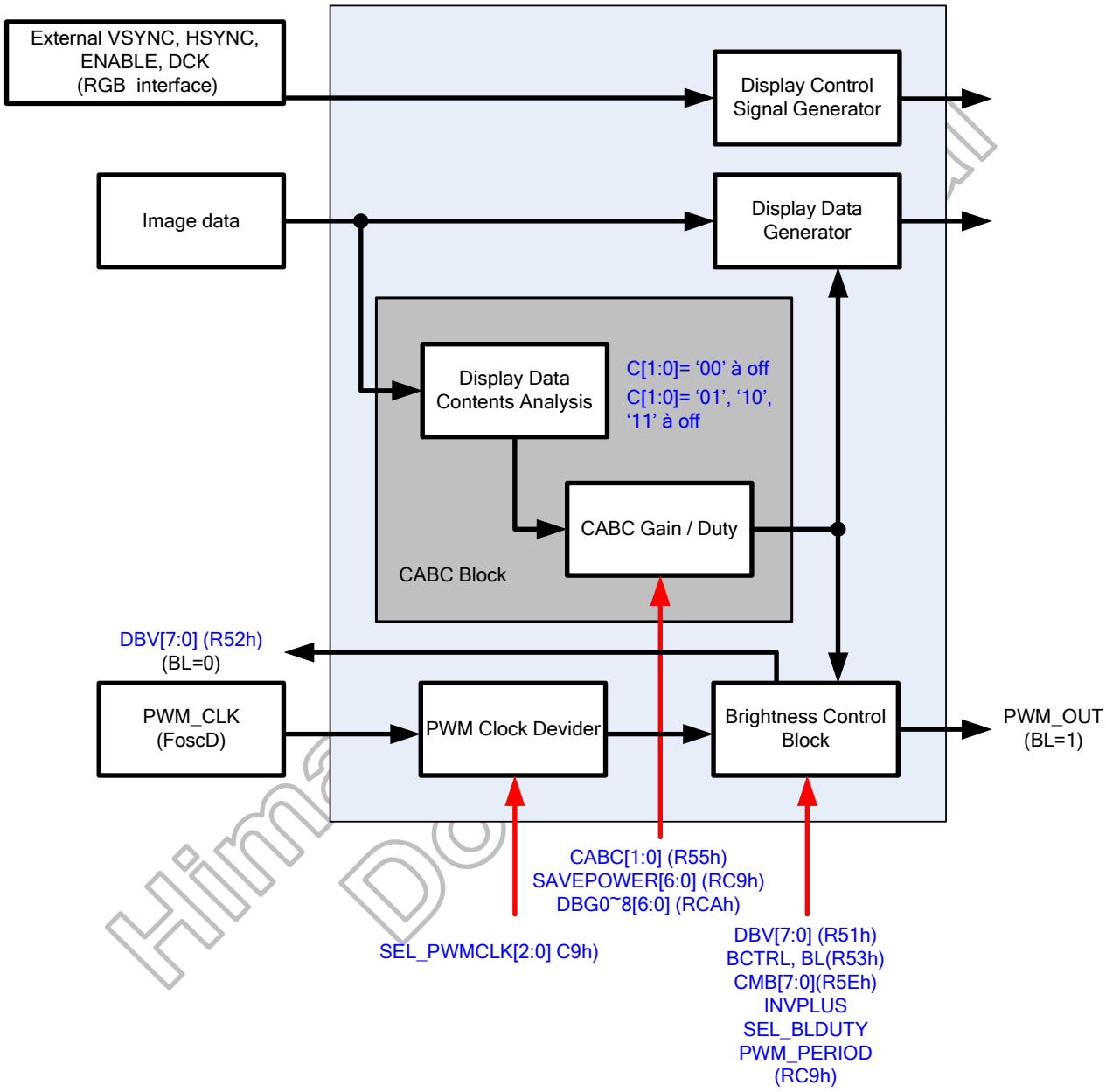
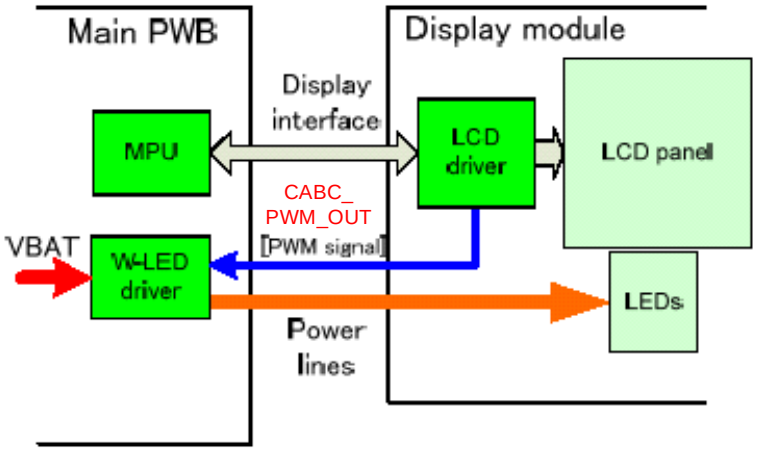


Figure 5.37: CABC block diagram

5.18.1 Module architectures

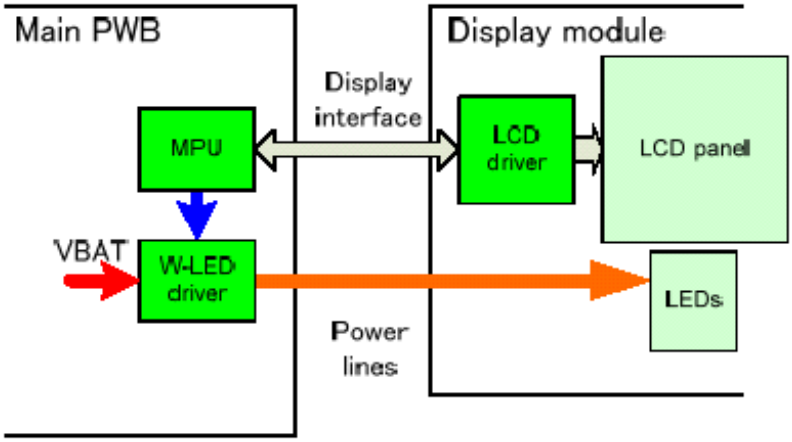
HX8369-A02 can support two module architectures for CABC operation. The BL bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



1. **BL** =`1` of R53h
2. LED backlight brightness for the display is controlled by external output "CABC_PWM_OUT" .

- Architecture II



1. **BL** =`0` of R53h
2. LED backlight brightness data for the display is read with DBV[7:0] bits of R52h.
3. Read commands R53h should be synchronized with V-sync.

Figure 5.38: Module architecture

5.18.2 CABC block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/ “CABC duty” table. Every DBGx[6:0] has 33 gain/duty value setting.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGxx[6:0].

Please note that : Duty (valid level period (LED on) / one complete period)=1/ gain.

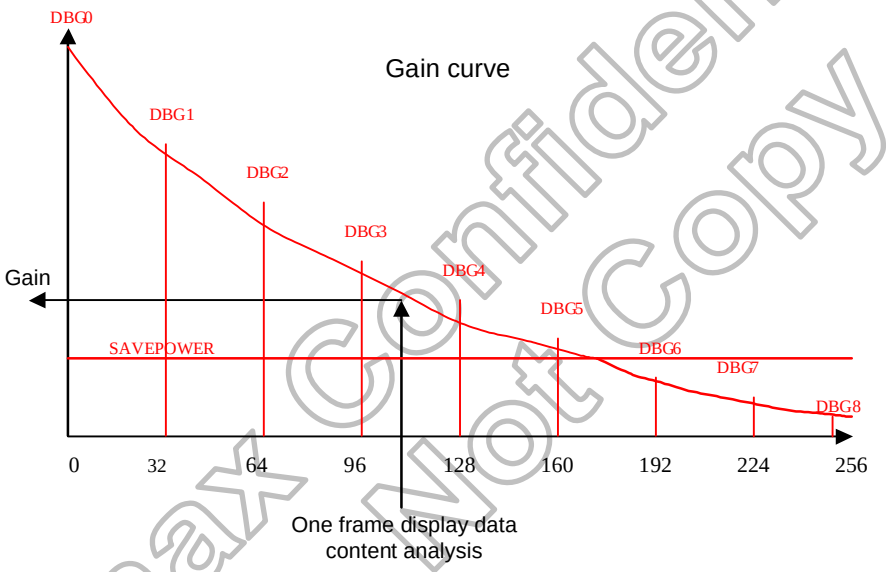


Figure 5.39: CABC gain / CABC duty generation

For power saving of backlight module, there are SAVEPOWER[6:0] bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain / duty after one-frame display data contents analysis is smaller(gain) / larger(duty) than SAVEPOWER[6:0] bits setting, the CABC block will output CABC gain / duty equal to SAVEPOWER[6:0] and ignore the result of display data contents analysis.

5.18.3 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as (DBV[7:0])/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period=2.95 ms, and DBV[7:0](R51h)='228DEC' and CABC duty is 74%. Then CABC_PWM_OUT duty=(228) / 255 x 74.42%≡66.54%. Correspond to the CABC_PWM_OUT period=2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT =0.99ms.

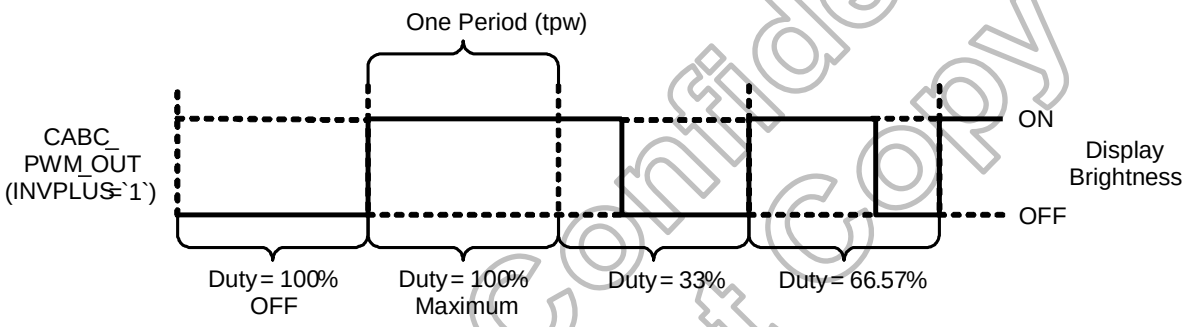


Figure 5.40: CABC_PWM_OUT output duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

Table 5.63 CABC timing table

Note1: The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.
Note2: The pulse width range by setting CABC related registers is locate between 0.0333ms to 8.33ms.

When Architecture II module is used (BL='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0](R51h) will be read a value as 169DEC ((169)/255≡ 66.27%).

5.18.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (CMB[7:0] bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=’0’ of R53h), CABC minimum brightness setting is ignored. “CMB[7:0], Read CABC minimum brightness (R5Fh)“ always read the setting value of “CMB[7:0], Write CABC minimum brightness (R5Eh)”

5.19 OTP programing

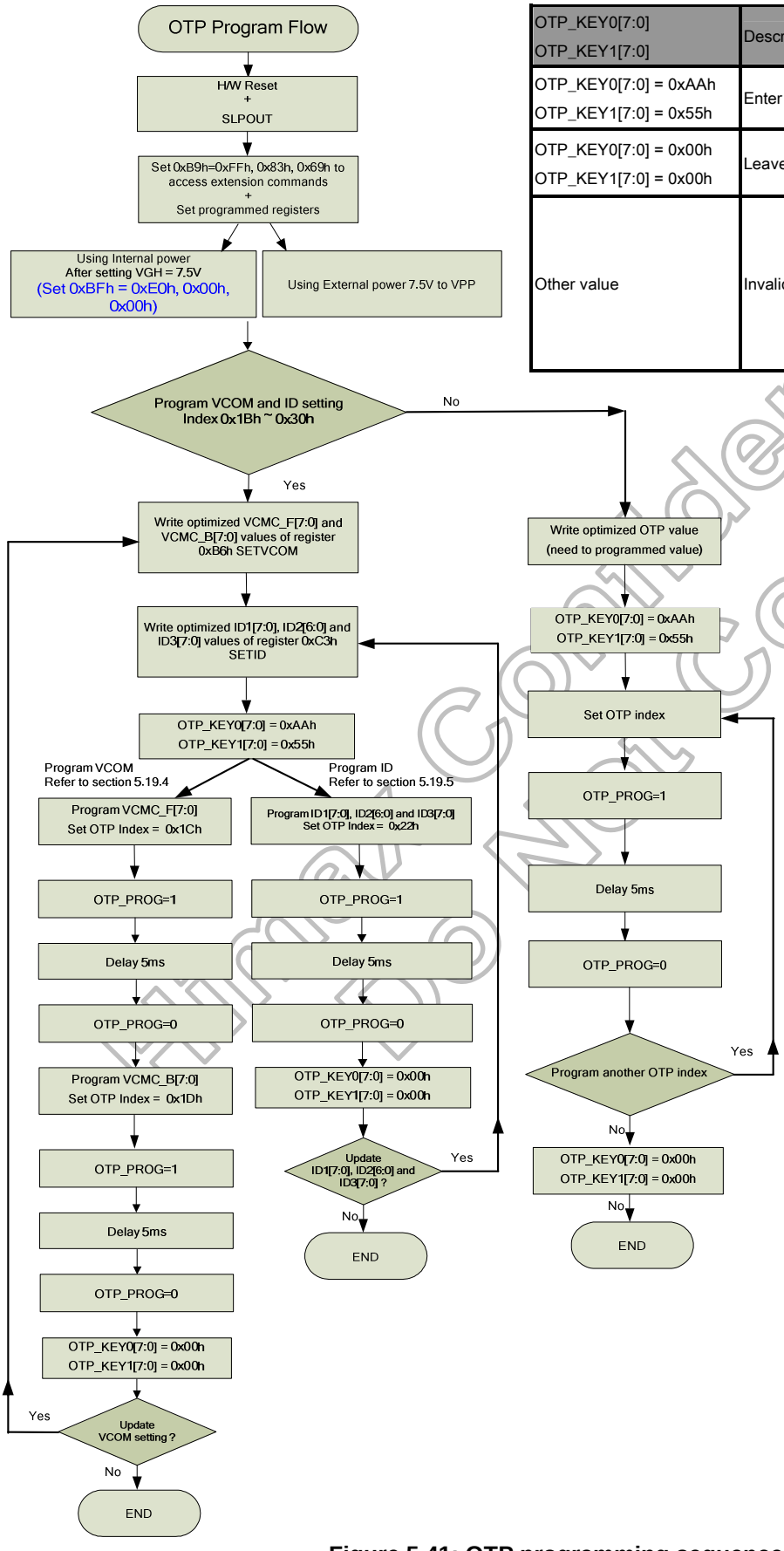
5.19.1 OTP table

OTP_INDEX (HEX)	Ref. Command	B7	B6	B5	B4	B3	B2	B1	B0
00	SETOSC (B0h)	NVALID0	-	-	-	UADJ[3:0]			
1B	SETVCOM (B6h)	NVALID_VCMF1	NVALID_VCMF2	NVALID_VCMF3	NVALID_VCMB1	NVALID_VCMB2	NVALID_VCMB3	-	-
1C		VCMC_F1[7:0]							
1D		VCMC_B1[7:0]							
1E		VCMC_F2[7:0]							
1F		VCMC_B2[7:0]							
20		VCMC_F3[7:0]							
21		VCMC_B3[7:0]							
22	SETID (C3h)	ID1_1[7:0]							
23		NVALID_ID1	ID2_1[6:0]						
24		ID3_1[7:0]							
25		ID1_2[7:0]							
26		NVALID_ID2	ID2_2[6:0]						
27		ID3_2[7:0]							
28		ID1_3[7:0]							
29		NVALID_ID3	ID2_3[6:0]						
2A		ID3_3[7:0]							
2B		ID1_4[7:0]							
2C		NVALID_ID4	ID2_4[6:0]						
2D		ID3_4[7:0]							
2E		ID1_5[7:0]							
2F		NVALID_ID5	ID2_5[6:0]						
30		ID3_5[7:0]							
31	SETPOWER (B1h)	NVALID8	FS1[2:0]			-	AP[2:0]		
32		-	-	-	-	BT[3:0]			
33		DT[1:0]		-	-	DCDIV[3:0]			
34		-	-	-	BTP[4:0]				
35		-	-	-	BTN[4:0]				
36		VRHP[7:0]							
37		VRHN[7:0]							
38		-	-	VRMP[5:0]					
39		-	-	VRMN[5:0]					
3A		-	-	DD_TU	VPNL_EN	-	VBS[2:0]		
3B		-	DC86_DIV3	DC86_DIV2	DC86_DIV1	DC86_DIV0	XDK1	XDK0	AUTO_XDK
3C		-	DTPS[2:0]			-	DTNS[2:0]		
3D		A_DC[1:0]		A_DTP[2:0]			A_DTN[2:0]		
3E		B_DC[1:0]		B_DTP[2:0]			B_DTN[2:0]		
3F		C_DC[1:0]		C_DTP[2:0]			C_DTN[2:0]		
40		D_DC[1:0]		D_DTP[2:0]			D_DTN[2:0]		
41		E_DC[1:0]		E_DTP[2:0]			E_DTN[2:0]		
42	SETCYC (B4h)	NVALID9	-	-	-	NW_PE[1:0]		NW[1:0]	
43		SON[7:0]							
44		SOFF[7:0]							
45		EQS[7:0]							
46		EQON[7:0]							
47	SETPANEL (CCh)	NVALID10	VPL	HPL	EPL	SS_PANEL	DPL	REV_PANEL	BGR_PANEL
48	SETDISP (B2h)	NVALID11	RES_SEL[2:0]			RM	DFR	DM[1:0]	
49		BP [7:0]							
4A		FP [7:0]							
4B		SAP[3:0]				-	-	-	-
4C		GEN_ON[7:0]							
4D		GEN_OFF[7:0]							
4E		RTN[7:0]							
4F		-	-	-	-	TEI[3:0]			

50		-	-	-	-	-	-	TEP[9:8]
51		TEP[7:0]						
52		BP_PE [7:0]						
53		FP_PE [7:0]						
54		RTN_PE[7:0]						
78		NVALID_GV0	-	G1_VRP0[5:0]				
79		-	-	G1_VRP1[5:0]				
7A		-	-	G1_VRP2[5:0]				
7B		-	-	G1_VRP3[5:0]				
7C		-	-	G1_VRP4[5:0]				
7D		-	-	G1_VRP5[5:0]				
7E		-	G1_PRP0[6:0]					
7F		-	G1_PRP1[6:0]					
80		G1_CGMP0[1:0]		-	G1_ PKP0[4:0]			
81		G1_CGMP1[1:0]		-	G1_PKP1[4:0]			
82		G1_CGMP2[1:0]		-	G1_PKP2[4:0]			
83		G1_CGMP3[1:0]		-	G1_PKP3[4:0]			
84		G1_CGMP5	G1_CGMP4	-	G1_PKP4[4:0]			
85		-	-	-	G1_PKP5[4:0]			
86		-	-	-	G1_PKP6[4:0]			
87		-	-	-	G1_PKP7[4:0]			
88	SETGAMMA (E0h) (GC0)	-	-	-	G1_PKP8[4:0]			
89		-	-	G1_VRN0[5:0]				
8A		-	-	G1_VRN1[5:0]				
8B		-	-	G1_VRN2[5:0]				
8C		-	-	G1_VRN3[5:0]				
8D		-	-	G1_VRN4[5:0]				
8E		-	-	G1_VRN5[5:0]				
8F		-	G1_PRN0[6:0]					
90		-	G1_PRN1[6:0]					
91		G1_CGMN0[1:0]		-	G1_PKN0[4:0]			
92		G1_CGMN1[1:0]		-	G1_PKN1[4:0]			
93		G1_CGMN2[1:0]		-	G1_PKN2[4:0]			
94		G1_CGMN3[1:0]		-	G1_PKN3[4:0]			
95		G1_CGMN5	G1_CGMN4	-	G1_PKN4[4:0]			
96		-	-	-	G1_PKN5[4:0]			
97		-	-	-	G1_PKN6[4:0]			
98		-	-	-	G1_PKN7[4:0]			
99		-	-	-	G1_PKN8[4:0]			
9A	SETGIP(D5h)	NVALID13	-	-	-	SHR_0[11:8]		
9B		SHR_0[7:0]						
9C		-	-	-	-	SHR_1[11:8]		
9D		SHR_1[7:0]						
9E		SPD[7:0]						
9F		CHR[7:0]						
A0		CON[7:0]						
A1		COFF[7:0]						
A2		SHP[3:0]				SCP[3:0]		
A3		CHP[3:0]				CCP[3:0]		
A4		SOS_1[3:0]				SOS_0[3:0]		
A5		SOS_3[3:0]				SOS_2[3:0]		
A6		COS_1[3:0]				COS_0[3:0]		
A7		COS_3[3:0]				COS_2[3:0]		
A8		COS_5[3:0]				COS_4[3:0]		
A9		COS_7[3:0]				COS_6[3:0]		
AA		SOS_1_ML[3:0]				SOS_0_ML[3:0]		
AB		SOS_3_ML[3:0]				SOS_2_ML[3:0]		
AC		COS_1_ML[3:0]				COS_0_ML[3:0]		
AD		COS_3_ML[3:0]				COS_2_ML[3:0]		

AE		COS_5_ML[3:0]				COS_4_ML[3:0]			
AF		COS_7_ML[3:0]				COS_6_ML[3:0]			
B0		-	-	GTO[5:0]					
B1		GNO[7:0]							
B2		EQ_DELAY[7:0]							
B3		GIP_OPT[7:0]							
100	SETDGCLUT (C1h)	NVALID16	-	-	-	-	-	DITH_OPT	DGC_EN
101		D1[7:0]							
102		D2[7:0]							
• • •		Dn[7:0]							
17D		D125[7:0]							
17E		D126[7:0]							

5.19.2 OTP programming flow



OTP_KEY0[7:0] OTP_KEY1[7:0]	Description	Note
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode	
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode	
Other value	Invalid	1. If HX8369-A02 operate on OTP program mode, then keep on OTP program mode. 2. If HX8369-A02 operate on non-OTP program mode, then keep on non-OTP program mode.

Figure 5.41: OTP programming sequence

5.19.3 Programming sequence

Step	Operation
1	Power on and reset the module.
2	SLPOUT and set 0xB9h = 0xFFh, 0x83h, 0x69h to access the extension commands.
3	Set VGH power to 7.5V for OTP programming state for using internal power mode. Or using the external power 7.5V to VPP.
4	Write optimized values to related registers.
5	Set OTP_KEY1[7:0] (RE9h)=0xAAh and OTP_KEY1[7:0] (RE9h)=0x55h to enter OTP program mode.
6	Specify OTP_index, please refer to the OTP table.
7	Set OTP_Mask=0x00h, programming the entire bit of one parameter.
8	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.
9	Wait 5 ms (**Note 1**)
10	Set OTP_PROG=0, OTP_index programming action done.
11	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (5). Otherwise, set OTP_KEY1[7:0] (RE9h)=0x00h and OTP_KEY1[7:0] (RE9h)=0x00h to leave OTP program mode and power off the module and remove the external power on VPP pin.

Note1: When do the OTP programming process, it must be added 5ms delay time after setting OTP_PROG=1.

Table 5.64: OTP Programming sequence

5.19.4 OTP Programming example of VCOM setting VCMC_F and VCMC_B

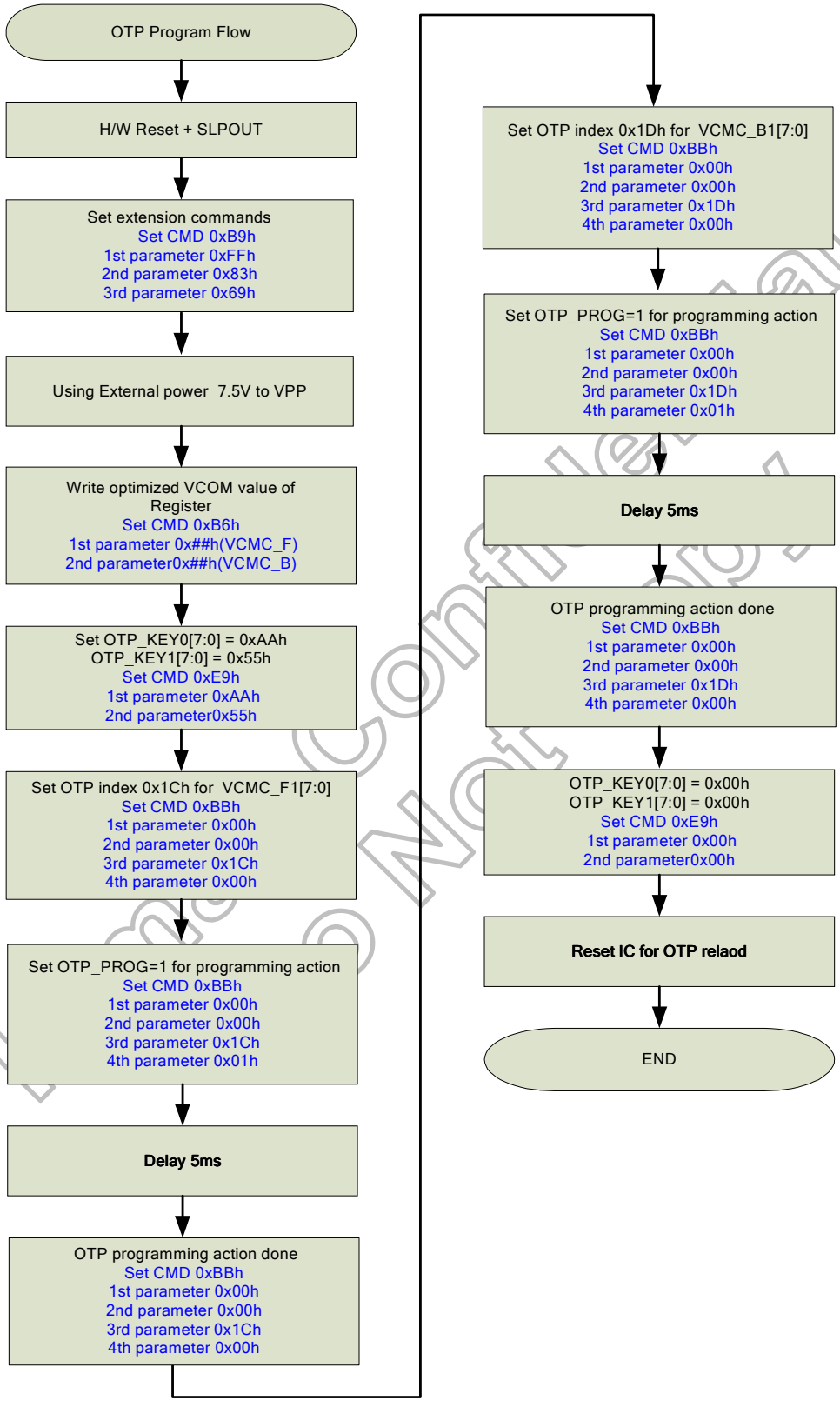


Figure 5.42: OTP programming sequence example 1.

5.19.5 OTP Programming example of ID1, ID2 and ID3

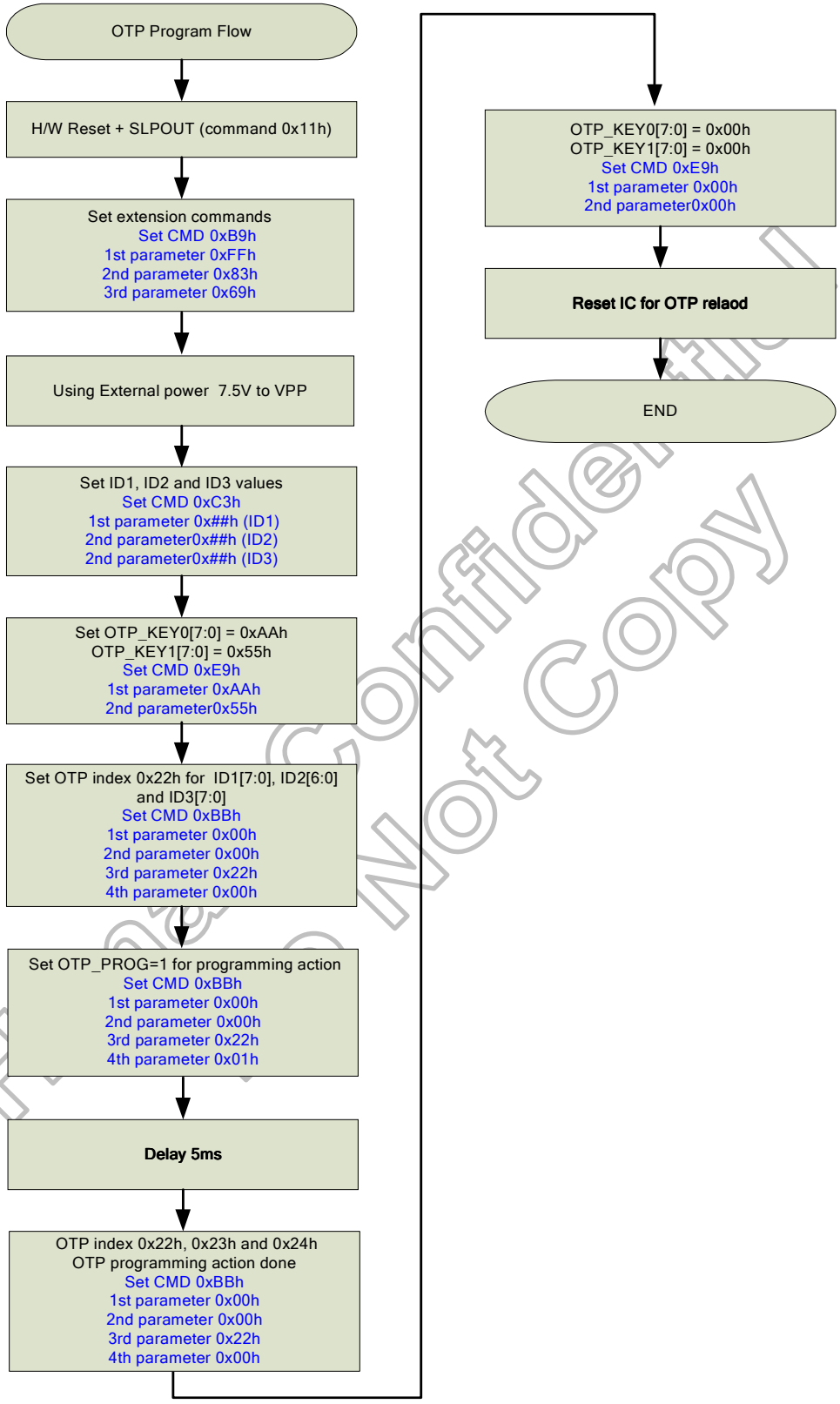
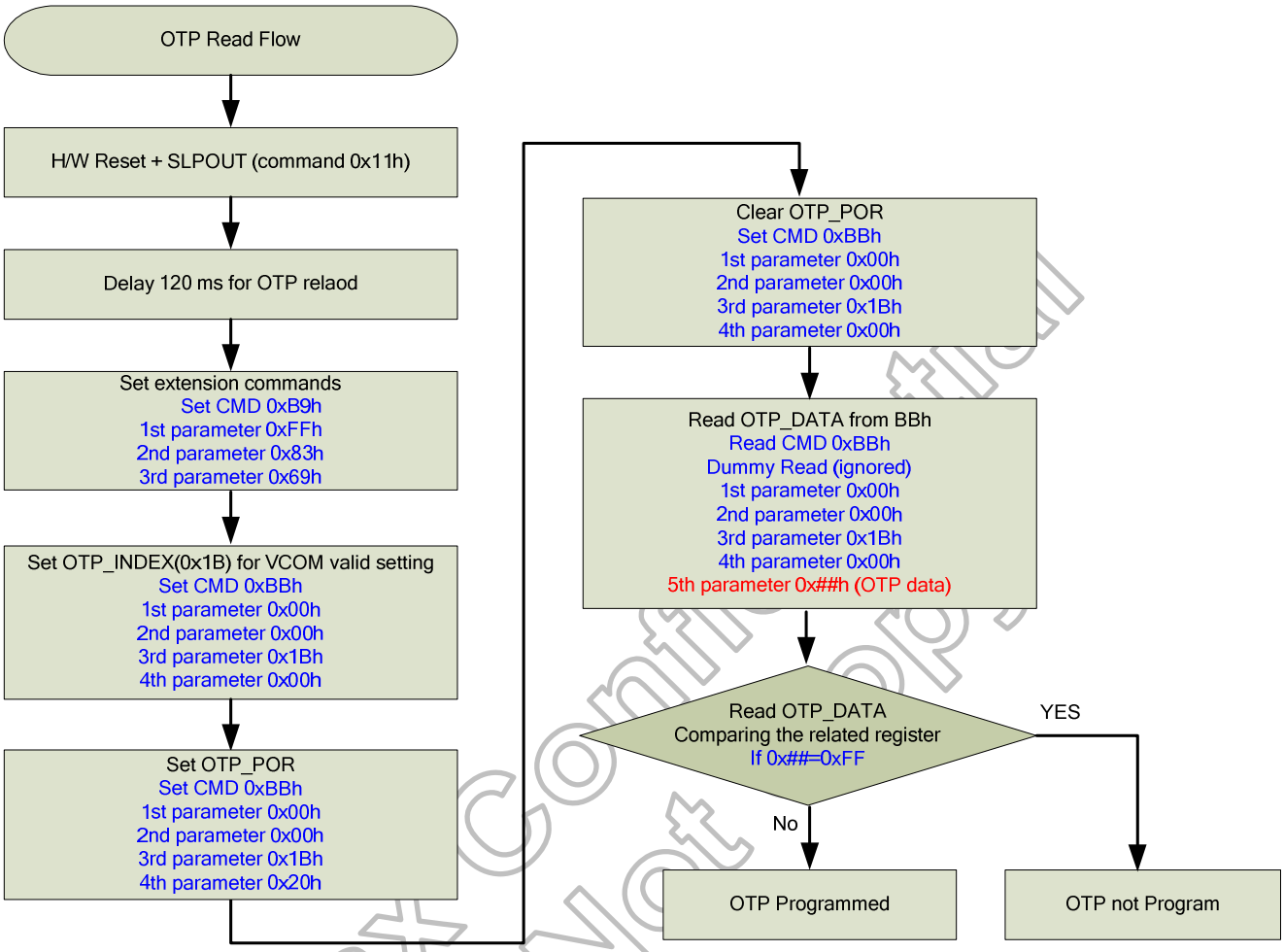


Figure 5.43: OTP programming sequence example 2.

5.19.6 OTP read example of 0x1Bh (VCOM setting re-load)



OTP_index 0x1Bh	value	1st VCOM OTP	2nd VCOM OTP	3rd VCOM OTP
D7 NVALID_VCMF1	1	0	0	0
D6 NVALID_VCMF2	1	1	0	0
D5 NVALID_VCMF3	1	1	1	0
D4 NVALID_VCMB1	1	0	0	0
D3 NVALID_VCMB2	1	1	0	0
D2 NVALID_VCMB3	1	1	1	0
0x1Bh value	0xFFh	0x6Fh	0x27h	0x03h
Reload OTP index	Default	0x1Ch and 0x1Dh	0x1Eh and 0x1Fh	0x20h and 0x21h

Figure 5.44: OTP programming sequence index 0x1Bh read flow.

5.19.7 OTP read example of VCMC_F1

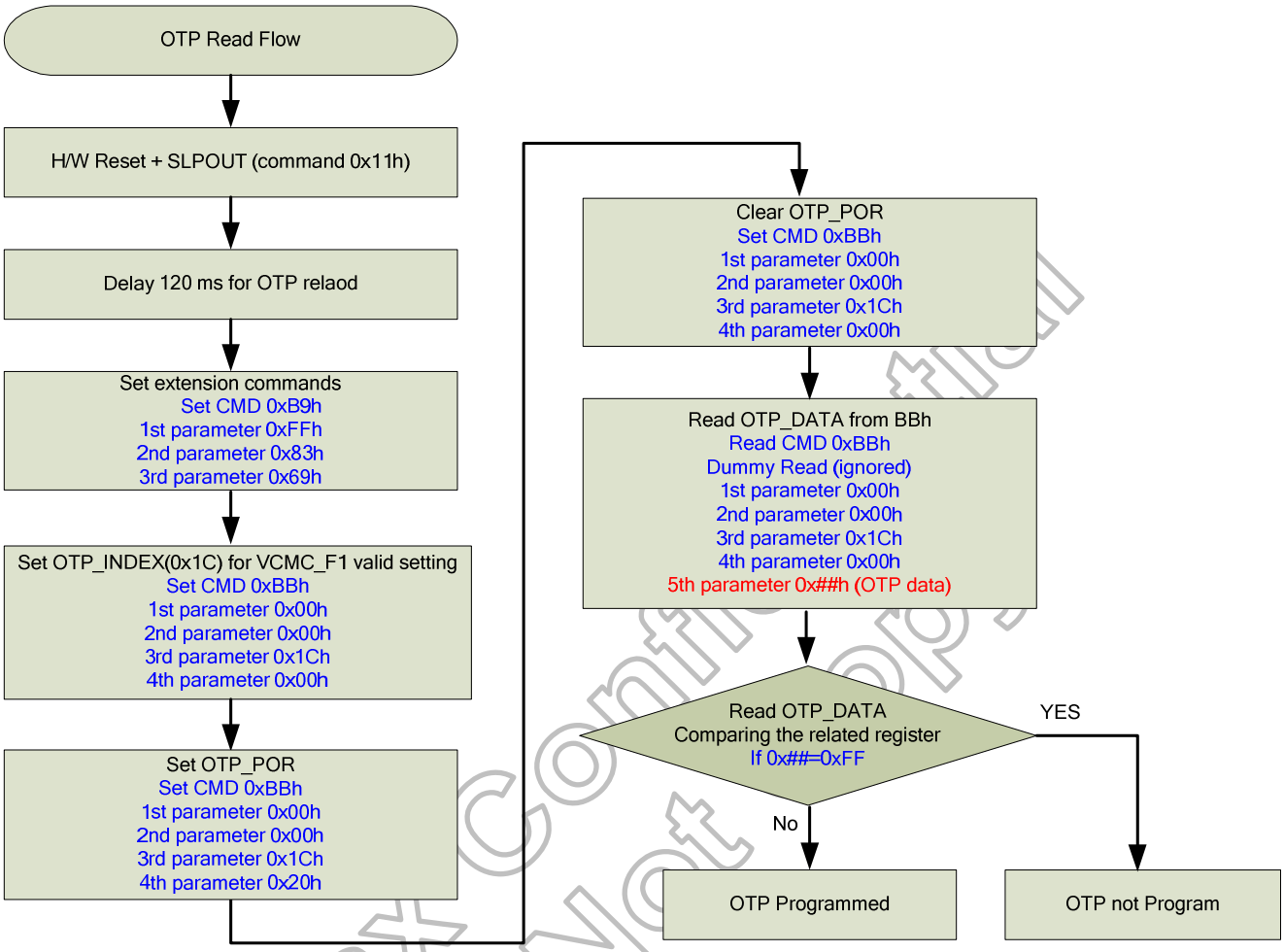


Figure 5.45: OTP programming sequence read flow.

6. Command

6.1 Command list

6.1.1 Standard command

(Hex)	Operation code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	RGB
00	NOP	0	1	↑	0	0	0	0	0	0	0	0	No Operation	-	Yes
01	SWRESET	0	1	↑	0	0	0	0	0	0	0	1	Software Reset	-	Yes
05	RDNUMPE	0	1	↑	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error	-	-
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	P[7:0]								-	-	-
06	RDRED	0	1	↑	0	0	0	0	0	1	1	0	Read Red Colour	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	R7	R6	R5	R4	R3	R2	R1	R0	xx	-	-
07	RDGREEN	0	1	↑	0	0	0	0	0	1	1	1	Read Green Colour	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	G7	G6	G5	G4	G3	G2	G1	G0	xx	-	-
08	RDBLUE	0	1	↑	0	0	0	0	1	0	0	0	Read Blue Colour	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	B7	B6	B5	B4	B3	B2	B1	B0	xx	-	-
0A	RDDPM	0	1	↑	0	0	0	0	1	0	1	0	Read display power mode	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	D7	D6	D5	D4	D3	D2	0	0	-	-	-
0B	RDDMADCTL	0	1	↑	0	0	0	0	1	0	1	1	Read display MADCTL	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	D7	D6	D5	D4	D3	D2	0	0	-	-	-
0C	RDDCOLMOD	0	1	↑	0	0	0	0	1	1	0	0	Read display pixel format	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	-	D6	D5	D4	-	D2	D1	D0	-	-	-
0D	RDDIM	0	1	↑	0	0	0	0	1	1	0	1	Read display image mode	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	D7	D6	D5	0	0	D2	D1	D0	-	-	-
0E	RDDSM	0	1	↑	0	0	0	0	1	1	1	0	Read display signal mode	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	D7	D6	0	0	0	0	0	0	-	-	-
0F	RDDSDR	0	1	↑	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-	Yes
		1	↑	1	x	x	x	x	x	x	x	x	Dummy read	-	-
		1	↑	1	D7	D6	D5	D4	0	0	0	0	-	-	-

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	RGB
10	SLPIN	0	1	↑	0	0	0	1	0	0	0	0	Sleep In	-	Yes
11	SLPOUT	0	1	↑	0	0	0	1	0	0	0	1	Sleep Out	-	Yes
12	PTLON	0	1	↑	0	0	0	1	0	0	1	0	Partial Mode On	-	No
13	NORON	0	1	↑	0	0	0	1	0	0	1	1	Normal display mode on	-	No
20	INVOFF	0	1	↑	0	0	1	0	0	0	0	0	Display inversion off	-	No
21	INVON	0	1	↑	0	0	1	0	0	0	0	1	Display inversion on	-	No
26	GAMSET	0	1	↑	0	0	1	0	0	1	1	0	Gamma set	-	Yes
		1	1	↑	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-	-	
28	DISPOFF	0	1	↑	0	0	1	0	1	0	0	0	Display off	-	Yes
29	DISPON	0	1	↑	0	0	1	0	1	0	0	1	Display on	-	Yes
2A	CASET	0	1	↑	0	0	1	0	1	0	1	0	Column Address Set	-	No
		1	1	↑	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Column address start	-	-
		1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Column address start	-	-
		1	1	↑	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Column address end	-	-
		1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Column address end	-	-
2B	PASET	0	1	↑	0	0	1	0	1	0	1	1	Row address set	-	No
		1	1	↑	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Row address start	-	-
		1	1	↑	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Row address start	-	-
		1	1	↑	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Row address end	-	-
		1	1	↑	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	Row address end	-	-
2C	RAMWR	0	1	↑	0	0	1	0	1	1	0	0	Memory Write	-	No
		1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	Write data		
		1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Write data	-	
		1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	Write data	-	
2D	RGBSET	0	1	↑	0	0	1	0	1	1	0	1	Color Set	-	Yes
		1	1	↑	R007	R006	R005	R004	R003	R002	R001	R000	Red tone	-	-
		1	1	↑	Rnn7	Rnn6	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	Red tone	-	-
		1	1	↑	R637	R636	R635	R634	R633	R632	R631	R630	Red tone	-	-
		1	1	↑	G007	G006	G005	G004	G003	G002	G001	G000	Green tone	-	-
		1	1	↑	Gnn7	Gnn6	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	Green tone	-	-
		1	1	↑	G637	G636	G635	G634	G633	G632	G631	G630	Green tone	-	-
		1	1	↑	B007	B006	B005	B004	B003	B002	B001	B000	Blue tone	-	-
		1	1	↑	Bnn7	Bnn6	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	Blue tone	-	-
		1	1	↑	B637	B636	B635	B634	B633	B632	B631	B630	Blue tone	-	-
2E	RAMRD	0	1	↑	0	0	1	0	1	1	1	0	Memory read	-	No
		1	↑	1	X	X	X	X	X	X	X	X	Dummy read	-	-
		1	↑	1	D17	D16	D15	D14	D13	D12	D11	D10	Read data	-	-
		1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	Read data	-	-
		1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-	-
30	PLTAR	0	1	↑	0	0	1	1	0	0	0	0	Partial Area	-	No
		1	1	↑	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	Start row	-	-
		1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	Start row	-	-
		1	1	↑	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	End row	-	-
		1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	End row	-	-

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	RGB
33	VSCRDEF	0	1	↑	0	0	1	1	0	0	1	1	Vertical scrolling definition	-	No
		1	1	↑	TFA[15:8]								-	-	-
		1	1	↑	TFA[7:0]								-	-	-
		1	1	↑	VSA[15:8]								-	-	-
		1	1	↑	VSA[7:0]								-	-	-
		1	1	↑	BFA[15:8]								-	-	-
		1	1	↑	BFA[7:0]								-	-	-
34	TEOFF	0	1	↑	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	-	No
35	TEON	0	1	↑	0	0	1	1	0	1	0	1	Tearing Effect Line ON	-	No
		1	1	↑	X	X	X	X	X	X	X	M	-	-	-
36	MADCTL	0	1	↑	0	0	1	1	0	1	1	0	Memory Access Control	-	Yes
		1	1	↑	B7	B6	B5	B4	B3	B2	X	X	-	-	-
37	VSCRSADD	0	1	↑	0	0	1	1	0	1	1	1	Vertical scrolling start address	-	No
		1	1	↑	VSP[15:8]								-	-	-
		1	1	↑	VSP[7:0]								-	-	-
38	IDMOFF	0	1	↑	0	0	1	1	1	0	0	0	Idle mode off	-	No
39	IDMON	0	1	↑	0	0	1	1	1	0	0	1	Idle mode on	-	No
3A	COLMOD	0	1	↑	0	0	1	1	1	0	1	0	-	-	Yes
		1	1	↑	X	D6	D5	D4	X	D2	D1	D0	-	-	-
3C	RAMWRCON	0	1	↑	0	0	1	1	1	1	0	0	Memory write	-	No
		1	1	↑	D17	D16	D15	D14	D13	D12	D11	D10	-	-	-
		1	1	↑	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	-	-	-
		1	1	↑	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-	-
3E	RAMRDCON	0	1	↑	0	0	1	1	1	1	1	0	Memory read	-	No
		1	↑	1	X	X	X	X	X	X	X	X	Dummy read	-	-
		1	↑	1	D17	D16	D15	D14	D13	D12	D11	D10	-	-	-
		1	↑	1	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	-	-	-
		1	↑	1	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	-	-	-
44	TESL	0	1	↑	0	1	0	0	0	1	0	0	TESL	-	Yes
		1	1	↑	TELINE[15:8](8'b0)								-	-	-
		1	1	↑	TELINE[7:0](8'b0)								-	-	-
45	GETSCAN	0	1	↑	0	1	0	0	0	1	0	1	Reture the current scanline SLN[15:0]	-	No
		1	1	↑	SLN[15:8]								-	-	-
		1	1	↑	SLN[7:0]								-	-	-
51	WRDISBV	0	1	↑	0	1	0	1	0	0	0	1	Write Display Brightness	-	Yes
		1	1	↑	DBV[7:0]								-	-	-
52	RDDISBV	0	1	↑	0	1	0	1	0	0	1	0	Read Display Brightness Value	-	Yes
		1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read	-	-
		1	↑	1	DBV[7:0]								-	-	-
53	WRCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Write CTRL Display	-	Yes
		1	1	↑	xx	xx	BCTRL	xx	DD	BL	xx	xx		-	-
54	RDCTRLD	0	1	↑	0	1	0	1	0	0	1	1	Read Control Value Display	-	Yes
		1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read	-	-
		1	↑	1	0	0	BCTRL	0	DD	BL	0	0	-	-	-
55	WRCABC	0	1	↑	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	-	Yes
		1	1	↑	xx	xx	xx	xx	xx	xx	CABC[1:0]		-	-	-
56	RDCABC	0	1	↑	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	-	Yes
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-	-
		1	↑	1	0	0	0	0	0	0	C1	C0	-	-	-

(Hex)	Operation Code	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	RGB
5E	WRCABCMB	0	1	↑	0	1	0	1	1	1	1	0	Write CABC minimum brightness	-	Yes
		1	1	↑	CMB[7:0]								-	-	-
5F	RDCABCMB	0	1	↑	0	1	0	1	1	1	1	1	Read CABC minimum brightness	-	Yes
		1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	Dummy read	-	-
		1	↑	1	CMB[7:0]								-	-	-
68	RDABCSDR	0	1	↑	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	-	Yes
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	-	-	-
		1	↑	1	D[7:6]		0	0	0	0	0	0	-	-	-
DA	RDID1	0	↑	1	1	1	0	1	1	0	1	0	Read ID1	-	Yes
		1	1	↑	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-	-
		1	1	↑	module's manufacturer[7:0]								-	-	-
DB	RDID2	0	↑	1	1	1	0	1	1	0	1	1	Read ID2	-	Yes
		1	1	↑	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-	-
		1	1	↑	1	LCD module/driver version [6:0]							-	-	-
DC	RDID3	0	↑	1	1	1	0	1	1	1	0	0	Read ID3	-	Yes
		1	1	↑	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-	-
		1	1	↑	LCD module/driver ID[7:0]								-	-	-
A1	Read_DDB_start	0	1	↑	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-	Yes
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
A8	Read_DDB_continue	0	1	↑	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-	Yes
		1	↑	1	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-
		1	↑	1	x	x	x	x	x	x	x	x	-	-	-

Note: (1) Undefined commands are treated as NOP (00h) command.
(2) B0h to D8h and E0h to FFh are for factory use of display supplier.

6.1.2 User define command list table

User define command list is available only set “SETEXC” command.

(Hex)	Operation Code	DCX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
B0	SETOSC	0	1	↑	1	0	1	1	0	0	0	0	Set Internal oscillator	-
		1	1	↑	-	-	-	-	-	-	-	OSC_EN	-	**(00h)**
		1	1	↑	-	-	-	-	UADJ[3:0]				-	**(0Bh)**
B1	SETPOWER	0	1	↑	1	0	1	1	0	0	0	1	Set power related setting	-
		1	1	↑	VBIAS_EN	VSN_EN	VSP_EN	VGL_EN	VGH_EN	LVGL_EN	VDDDN_HZ	STB	-	**(01h)**
		1	1	↑	-	-	-	-	-	-	-	DSTB	-	**(00h)**
		1	1	↑	-	FS1[2:0]			-	AP[2:0]			-	**(34h)**
		1	1	↑	-	-	-	-	BT[3:0]				-	**(07h)**
		1	1	↑	DT[1:0]		-	-	DCDIV[3:0]				-	**(00h)**
		1	1	↑	-	-	-	BTP[4:0]					-	**(0Eh)**
		1	1	↑	-	-	-	BTN[4:0]					-	**(0Eh)**
		1	1	↑	VRHP[7:0]								-	**(21h)**
		1	1	↑	VRHN[7:0]								-	**(29h)**
		1	1	↑	-	-	VRMP[5:0]						-	**(19h)**
		1	1	↑	-	-	VRMN[5:0]						-	**(19h)**
		1	1	↑	-	-	DD_TU	VPNL_EN	-	VBS[2:0]			-	**(07h)**
		1	1	↑	-	DC86_DIV3	DC86_DIV2	DC86_DIV1	DC86_DIV0	XDK1	XDK0	AUTO_XDK	-	**(22h)**
		1	1	↑	-	DTPS[2:0]			-	DTNS[2:0]			-	**(01h)**
		1	1	↑	A_DC[1:0]		A_DTP[2:0]			A_DTN[2:0]			-	**(E6h)**
		1	1	↑	B_DC[1:0]		B_DTP[2:0]			B_DTN[2:0]			-	**(E6h)**
		1	1	↑	C_DC[1:0]		C_DTP[2:0]			C_DTN[2:0]			-	**(E6h)**
		1	1	↑	D_DC[1:0]		D_DTP[2:0]			D_DTN[2:0]			-	**(E6h)**
		1	1	↑	E_DC[1:0]		E_DTP[2:0]			E_DTN[2:0]			-	**(E6h)**
B2	SETDISP	0	1	↑	1	0	1	1	0	0	1	0	Set display related register	-
		1	1	↑	-	-	-	-	-	-	D[1:0]		-	**(00h)**
		1	1	↑	-	RES_SEL[2:0]			RM	DFR	DM[1:0](1)		-	**(10h)**
		1	1	↑	BP [7:0]								-	**(03h)**
		1	1	↑	FP [7:0]								-	**(03h)**
		1	1	↑	SAP[3:0]				-	-	-	-	-	**(70h)**
		1	1	↑	GEN_ON[7:0]								-	**(00h)**
		1	1	↑	GEN_OFF[7:0]								-	**(FFh)**
		1	1	↑	RTN[7:0]								-	**(00h)**
		1	1	↑	-	-	-	-	TEI[3:0]				-	**(00h)**
		1	1	↑	-	-	-	-	-	-	TEP[9:8]		-	**(00h)**
		1	1	↑	TEP[7:0]								-	**(00h)**
		1	1	↑	BP_PE [7:0]								-	**(03h)**
		1	1	↑	FP_PE [7:0]								-	**(03h)**
		1	1	↑	RTN_PE[7:0]								-	**(03h)**
		1	1	↑	-	-	-	-	-	-	-	GON	-	**(01h)**
-	-	-	-	-	**Note:** (1) When BS[3:0]=1101, 1110, 1111 DM[1:0] default =11 Other condition, DM[1:0] default =00								-	**-**
B3	SETRGBIF	0	1	↑	1	0	1	1	0	0	1	1	Set RGB interface related register)	-
		1	1	↑	-	-	-	-	DPL	HSPL	VSPL	EPL		**(01h)**
B4	SETCYC	0	1	↑	1	0	1	0	0	1	0	0	Set Display waveform cycles	-
		1	1	↑	-	-	-	-	NW_PE[1:0]		NW[1:0]		-	**(00h)**
		1	1	↑	SON[7:0]								-	**(0Fh)**
		1	1	↑	SOFF[7:0]								-	**(82h)**
		1	1	↑	EQS[7:0]								-	**(0Ch)**
		1	1	↑	EQON[7:0]								-	**(03h)**

B6	SETVCOM (OTPx3)	0	1	↑	1	0	1	1	0	1	1	0	Set VCOM Voltage	-
		1	1	↑	VCMC_F[7:0]								-	**(5Eh)**
		1	1	↑	VCMC_B[7:0]									**(5Eh)**
B9	SETEXTC	0	1	↑	1	0	1	1	1	0	0	1	Set extended command set	-
		1	1	↑	EXTC1[7:0]								-	**(00h/FFh)**
		1	1	↑	EXTC2[7:0]								-	**(00h/83h)**
		1	1	↑	EXTC3[7:0]								-	**(00h/69h)**
BA	SETMIPI	0	1	↑	1	0	1	1	1	0	1	0	Set MIPI Control	
		1	1	↑	DPHYCMD0[7:0]								-	**(00h)**
		1	1	↑	DPHYCMD1[7:0]								-	**(A0h)**
		1	1	↑	DPHYCMD2[7:0]								-	**(C6h)**
		1	1	↑	DSICMD0[7:0]								-	**(00h)**
		1	1	↑	DSICMD1[7:0]								-	**(0Ah)**
		1	1	↑	DSICMD2[7:0]								-	**(00h)**
		1	1	↑	DSICMD3[7:0]								-	**(10h)**
		1	1	↑	DPHYOTP0[7:0]								-	**(30h)**
		1	1	↑	DPHYOTP1[7:0]								-	**(6Fh)**
		1	1	↑	DPHYOTP2[7:0]								-	**(02h)**
		1	1	↑	DSIOTP0[7:0]								-	**(10h)**
		1	1	↑	DSIOTP1[7:0]								-	**(18h)**
		1	1	↑	-	DSI_INITRDY	-	-	-	-	-	-		(40h)
BB	SETOTP	0	1	↑	1	0	1	1	1	0	1	1	Set OTP	-
		1	1	↑	OTP_MASK[7:0]								-	**(00h)**
		1	1	↑	-	-	-	-	-	-	-	OTP_INDEX[8]	-	**(01h)**
		1	1	↑	OTP_INDEX[7:0]								-	**(FFh)**
		1	1	↑	OTP_LOAD_DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]		VPP_SEL	OTP_PROG	-	**(00h)**
		1	1	↑	OTP_DATA[7:0]								OTP read / write	**(xxh)**
C1	SETDGCLUT	0	1	↑	1	1	0	0	0	0	0	1	Set DGC LUT	-
		1	1	↑	-	-	-	-	-	-	DITH_OPT	DGC_EN	-	-
		1	1	↑	D1[7:0]								-	-
		1	1	↑	Dn[7:0]								-	-
		1	1	↑	D126[7:0]								-	-
C3	SETID (OTPx5)	0	1	↑	1	1	0	0	0	0	1	1	Set ID	-
		1	1	↑	ID1[7:0]								-	**(00h)**
		1	1	↑	0	ID2[6:0]							-	**(00h)**
		1	1	↑	ID3[7:0]								-	**(00h)**
+C9	SETCABC	0	1	↑	1	1	0	0	1	0	0	1	Set CABC Control	
		1	1	↑	-	-	EN_DIM_MIX	EN_COST_MEAN	EN_COST	EN_NLN_GAIN	EN_JUDGE	EN_TEMP		**(3Eh)**
		1	1	↑	CABC_DD	SAVEPOWER[6:0]								**(00h)**
		1	1	↑	MEAN_OFFSET[7:0]									**(00h)**
		1	1	↑	-	-	-	-	CABC_FLM[3:0]					**(01h)**
		1	1	↑	-	SEL_PWMCLK[2:0]			SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY		**(2Fh)**
		1	1	↑	PWM_PERIOD[7:0]									**(2Bh)**
		1	1	↑	-	DIM_FRAME[6:0]								**(1Eh)**
		1	1	↑	CABC_STEP[7:0]									**(1Eh)**
		1	1	↑	CABC_CLKEN[7:0]									**(00h)**
CC	SETPANEL	0	1	↑	1	1	0	0	1	1	0	0	Set panel related register	
		1	1	↑	-	-	-	-	SS_PANEL	-	REV_PANE	BGR_PANEL	-	**(02h)**
D5	SETGIP	0	1	↑	1	1	0	1	0	1	0	1	SET GIP control	
		1	1	↑	-	-	-	-	SHR_0[11:8]				-	**(00h)**
		1	1	↑	SHR_0[7:0]								-	**(02h)**
		1	1	↑	-	-	-	-	SHR_1[11:8]				-	**(00h)**
		1	1	↑	SHR_1[7:0]								-	**(01h)**
		1	1	↑	SPD[7:0]								-	**(02h)**

		1	1	↑	CHR[7:0]								-	**(03h)**
		1	1	↑	CON[7:0]								-	**(20h)**
		1	1	↑	COFF[7:0]								-	**(6Ch)**
		1	1	↑	SHP[3:0]				SCP[3:0]				-	**(03h)**
		1	1	↑	CHP[3:0]				CCP[3:0]				-	**(03h)**
		1	1	↑	SOS_1[3:0]				SOS_0[3:0]				-	**(00h)**
		1	1	↑	SOS_3[3:0]				SOS_2[3:0]				-	**(00h)**
		1	1	↑	COS_1[3:0]				COS_0[3:0]				-	**(60h)**
		1	1	↑	COS_3[3:0]				COS_2[3:0]				-	**(04h)**
		1	1	↑	COS_5[3:0]				COS_4[3:0]				-	**(71h)**
		1	1	↑	COS_7[3:0]				COS_6[3:0]				-	**(75h)**
		1	1	↑	SOS_1_ML[3:0]				SOS_0_ML[3:0]				-	**(00h)**
		1	1	↑	SOS_3_ML[3:0]				SOS_2_ML[3:0]				-	**(00h)**
		1	1	↑	COS_1_ML[3:0]				COS_0_ML[3:0]				-	**(51h)**
		1	1	↑	COS_3_ML[3:0]				COS_2_ML[3:0]				-	**(57h)**
		1	1	↑	COS_5_ML[3:0]				COS_4_ML[3:0]				-	**(40h)**
		1	1	↑	COS_7_ML[3:0]				COS_6_ML[3:0]				-	**(46h)**
		1	1	↑	-	-	GTO[5:0]						-	**(01h)**
		1	1	↑	GNO[7:0]								-	**(0Ch)**
		1	1	↑	EQ_DELAY[7:0]								-	**(0Ch)**
		1	1	↑	GIP_OPT[7:0]								-	**(00h)**
D8	SETTPSNR	0	1	↑	1	1	0	1	1	0	0	1	Set the Temp Senor control	
		1	1	↑	-	-	-	TSRAW[4:0]					(read only)	
		1	1	↑	-	-	-	TS_OS2[4:0]					-	**(12h)**
		1	1	↑	BT_P2[3:0]				BT_P1[3:0]				-	**(74h)**
		1	1	↑	BT_P4[3:0]				BT_P3[3:0]				-	**(A7h)**
		1	1	↑	-	-	-	D0[4:0]					-	**(0Ch)**
		1	1	↑	TS_G[2:0]			I0[4:0]					-	**(6Ah)**
		1	1	↑	-	TS_OS1[4:3]		D1[4:0]					-	**(57h)**
		1	1	↑	TS_OS1[2:0]			I1[4:0]					-	**(55h)**
		1	1	↑	PORE	RER[1:0]		D2[4:0]					-	**(17h)**
		1	1	↑	-	TF_ON	TSON	I2[4:0]					-	**(55h)**
E0	SETGAMMA (OTPx1)	0	1	↑	1	1	1	0	0	0	0	0	Set Gamma Curve Related Setting	-
		1	1	↑	-	-	G1_VRP0[5:0]						-	**(00h)**
		1	1	↑	-	-	G1_VRP1[5:0]						-	**(18h)**
		1	1	↑	-	-	G1_VRP2[5:0]						-	**(1Fh)**
		1	1	↑	-	-	G1_VRP3[5:0]						-	**(3Fh)**
		1	1	↑	-	-	G1_VRP4[5:0]						-	**(3Fh)**
		1	1	↑	-	-	G1_VRP5[5:0]						-	**(3Fh)**
		1	1	↑	-	G1_PRP0[6:0]							-	**(33h)**
		1	1	↑	-	G1_PRP1[6:0]							-	**(57h)**
		1	1	↑	G1_CGMP0[1:0]		-	G1_ PKP0[4:0]					-	**(07h)**
		1	1	↑	G1_CGMP1[1:0]		-	G1_PKP1[4:0]					-	**(0Dh)**
		1	1	↑	G1_CGMP2[1:0]		-	G1_PKP2[4:0]					-	**(0Fh)**
		1	1	↑	G1_CGMP3[1:0]		-	G1_PKP3[4:0]					-	**(13h)**
		1	1	↑	G1_CGMP5	G1_CGMP4	-	G1_PKP4[4:0]					-	**(16h)**
		1	1	↑	-	-	-	G1_PKP5[4:0]					-	**(14h)**
		1	1	↑	-	-	-	G1_PKP6[4:0]					-	**(16h)**
		1	1	↑	-	-	-	G1_PKP7[4:0]					-	**(18h)**
		1	1	↑	-	-	-	G1_PKP8[4:0]					-	**(1Fh)**
		1	1	↑	-	-	G1_VRN0[5:0]						-	**(00h)**
		1	1	↑	-	-	G1_VRN1[5:0]						-	**(18h)**
		1	1	↑	-	-	G1_VRN2[5:0]						-	**(1Fh)**
		1	1	↑	-	-	G1_VRN3[5:0]						-	**(3Fh)**
		1	1	↑	-	-	G1_VRN4[5:0]						-	**(3Fh)**
		1	1	↑	-	-	G1_VRN5[5:0]						-	**(3Fh)**
		1	1	↑	-	G1_PRN0[6:0]							-	**(33h)**
		1	1	↑	-	G1_PRN1[6:0]							-	**(57h)**
		1	1	↑	G1_CGMN0[1:0]		-	G1_PKN0[4:0]					-	**(07h)**

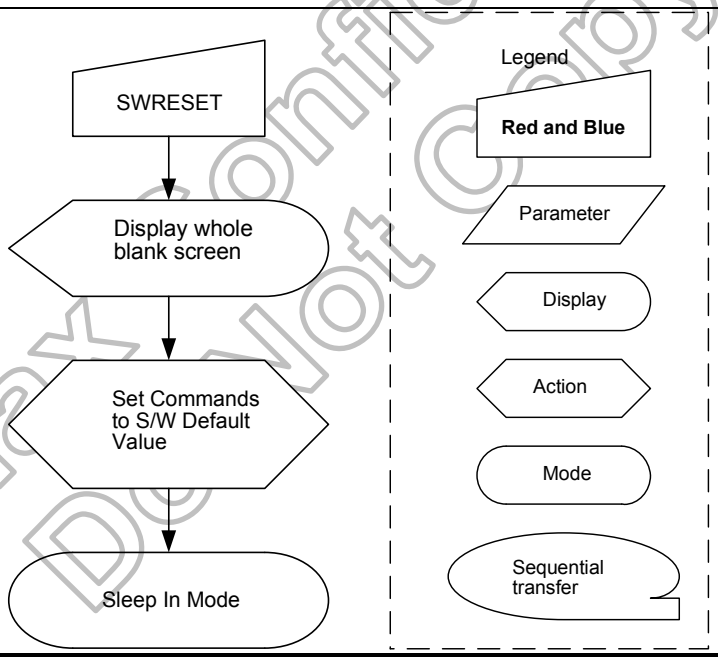
		1	1	↑	G1_CGMN1[1:0]		-	G1_PKN1[4:0]						-	**(0Dh)**
		1	1	↑	G1_CGMN2[1:0]		-	G1_PKN2[4:0]						-	**(0Fh)**
		1	1	↑	G1_CGMN3[1:0]		-	G1_PKN3[4:0]						-	**(13h)**
		1	1	↑	G1_CGMN5	G1_CGMN4	-	G1_PKN4[4:0]						-	**(16h)**
		1	1	↑	-	-	-	G1_PKN5[4:0]						-	**(14h)**
		1	1	↑	-	-	-	G1_PKN6[4:0]						-	**(16h)**
		1	1	↑	-	-	-	G1_PKN7[4:0]						-	**(18h)**
		1	1	↑	-	-	-	G1_PKN8[4:0]						-	**(1Fh)**
E9	SETOTPKEY	0	1	↑	1	1	1	0	1	0	0	1		-	-
		1	1	↑	OTP_KEY0[7:0]									-	**(00h/AAh)**
		1	1	↑	OTP_KEY1[7:0]									-	**(00h/55h)**
F4	GETHXID	0	1	↑	1	1	1	1	0	1	0	0		-	-
		1	↑	1	Himax ID[7:0]									-	**(69h)**
		1	↑	1	Version[7:0]										**(02h)**
FD	SETCNCD/ GETCNCD	0	1	↑	1	1	1	1	1	1	0	1		Set/Get Continue Command	-
		1	1	↑	WR_CMD_CN[7:0]									-	-
FE	SET READ INDEX	0	1	↑	1	1	1	1	1	1	1	0		SET READ Command Address	-
		1	1	↑	CMD_ADD[7:0]									-	**(00h)**
FF	GETSPIREAD	0	1	↑	1	1	1	1	1	1	1	1		Read Command Data	-
		1	↑	1	CMD_DATA1[7:0]									-	-
		1	↑	1	.									-	-
		1	↑	1	CMD_DATAN[7:0]									-	-

6.2 Command description

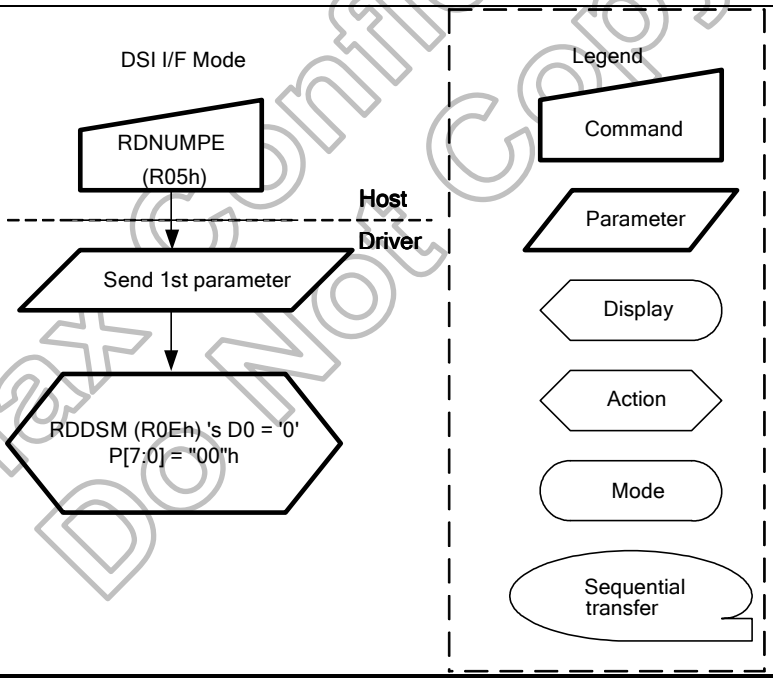
6.2.1 NOP (00h)

00H	NOP (No Operation)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.												
Restriction	-												
Register Availability	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
Default	N/A												
Flow Chart	-												

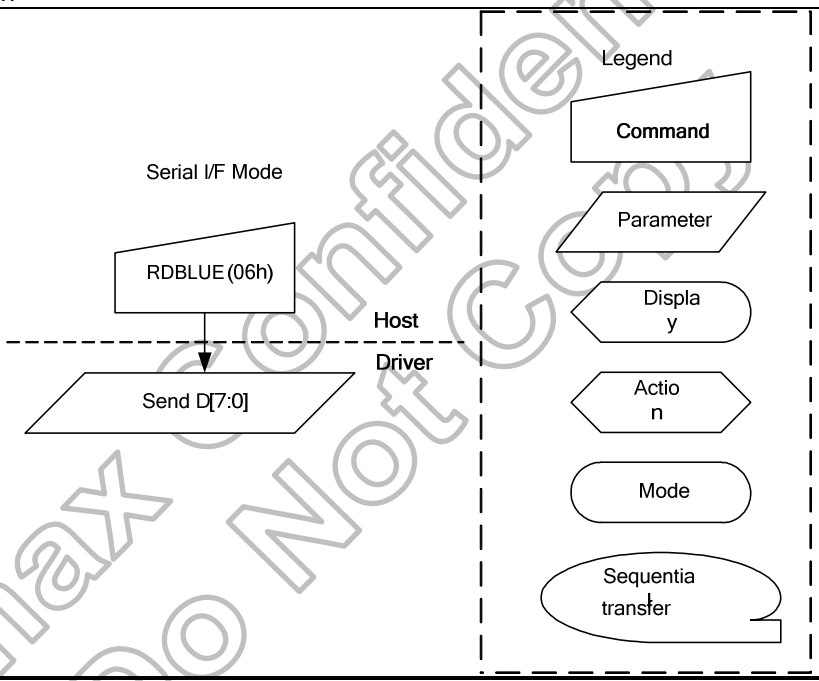
6.2.2 Software reset (01h)

01H	SWRESET (Software Reset)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command It will be necessary to wait 5msec before sending new command following software reset.												
Restriction	The display module loads all display supplier's factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability	Status								Availability				
	Normal Mode On, Idle Mode Off, Sleep Out								Yes				
	Normal Mode On, Idle Mode On, Sleep Out								Yes				
	Partial Mode On, Idle Mode Off, Sleep Out								Yes				
	Partial Mode On, Idle Mode On, Sleep Out								Yes				
Default	N/A												
Flow Chart													

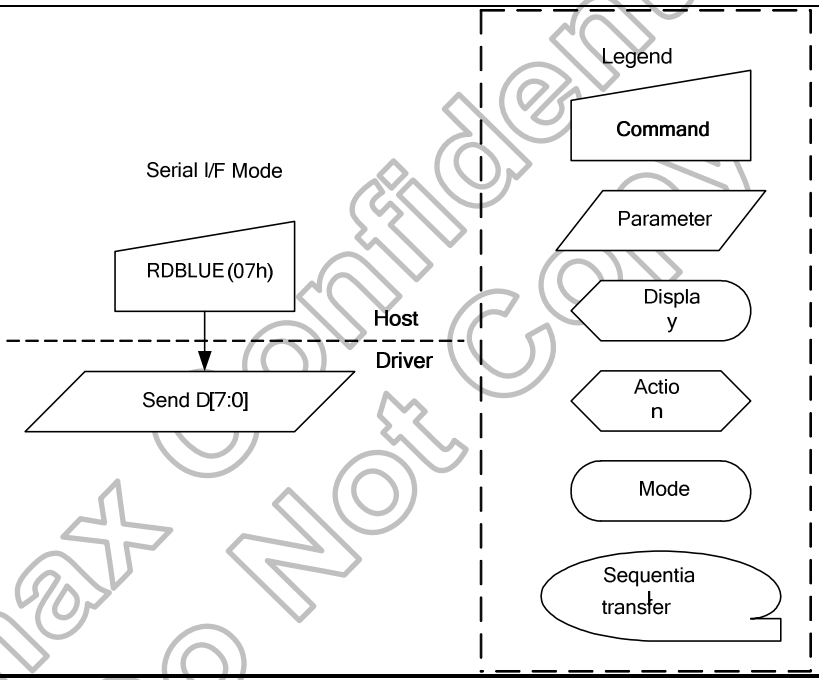
6.2.3 RDNUMPE: Read number of the parity errors (05h)

05H	RDNUMPE (Read Number of the Parity Errors)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	0	1	05
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	P7	P6	P5	P4	P3	P2	P1	P0	xx
Description	The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the errors. P[7] is set to '1' if there is overflow with P[6..0] bits. P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (The read function is completed).												
Restriction	SETEXTC turn on to enable this command												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	P[7:0] = 0x00h												
Flow Chart													

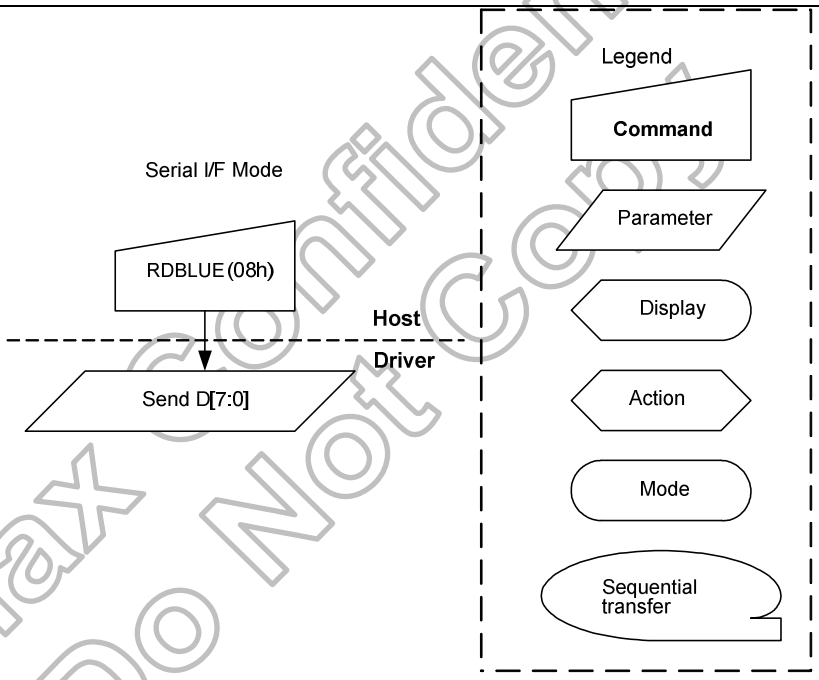
6.2.4 Get_red_channel (06h)

06H	RDRED (Read Red Colour)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	1	0	06
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	R7	R6	R5	R4	R3	R2	R1	R0	xx
Description	The first parameter is telling red colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes												
Default	R[7:0] = 0x00h												
Flow Chart													

6.2.5 Get_green_channel (07h)

07H	RDGREEN (Read Green Colour)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	0	1	1	1	07
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	G7	G6	G5	G4	G3	G2	G1	G0	xx
Description	The first parameter is telling green colour value of the first pixel of the frame when there is used DPI I/F. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes												
Default	G[7:0] = 0x00h												
Flow Chart													

6.2.6 Get_blue_channel (08h)

08H	RDBLUE (Read Blue Colour)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	0	0	08
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	B7	B6	B5	B4	B3	B2	B1	B0	xx
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	B[7:0] = 0x00h												
Flow Chart													

6.2.7 Get_power_mode (0Ah)

0AH	RDDPM (Read Display Power Mode)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	1	0	0A
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Not Defined	Set to '0'
D6	Idle Mode On/Off	-
D5	Partial Mode On/Off	-
D4	Sleep In/Out	-
D3	Display Normal Mode On/Off	-
D2	Display On/Off	-
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bits D7 for future use and are set to '0'.
Bit D6 – Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.
Bit D5 – Partial Mode On/Off
'0' = Partial Mode Off.
'1' = Partial Mode On.
Bit D4 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D3 – Display Normal Mode On/Off
'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.
Bit D2 – Display On/Off
'0' = Display is Off.
'1' = Display is On.

Restrictions

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

D[7:0] = 0x08h

6.2.8 Read display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	0	1	1	0B
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	-
D6	Column Address Order	-
D5	Page/Column Order	-
D4	Line Address Order	-
D3	RGB/BGR Order	-
D2	Display Data Latch Order	-
D1	Reserved	Set to '0'
D0	Reserved	Set to '0'

Bit D7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7='0').
'1' = Bottom to Top (When MADCTL B7='1').
Bit D6 – Column Address Order
'0' = Left to Right (When MADCTL B6='0').
'1' = Right to Left (When MADCTL B6='1').
Bit D5 – Page/Column Order
'0' = Normal (When MADCTL B5='0').
'1' = Roration (When MADCTL B5='1').
Note: For Bits D7 to D5, also refer to Section 5.3 MCU to memory write/read direction.
Bit D4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4='0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4='1').
Bit D3 – RGB/BGR Order
'0' = RGB (When MADCTL B3='0').
'1' = BGR (When MADCTL B3='1').
Note: For Bits D4 and D3 also refer to Section 6.2.31 Set_address_mode (36h).
Bit D2 – Display Data Latch Data Order
'0' = LCD Refresh Left to Right (When MADCTL B2='0').
'1' = LCD Refresh Right to Left (When MADCTL B2='1').

Restrictions

-

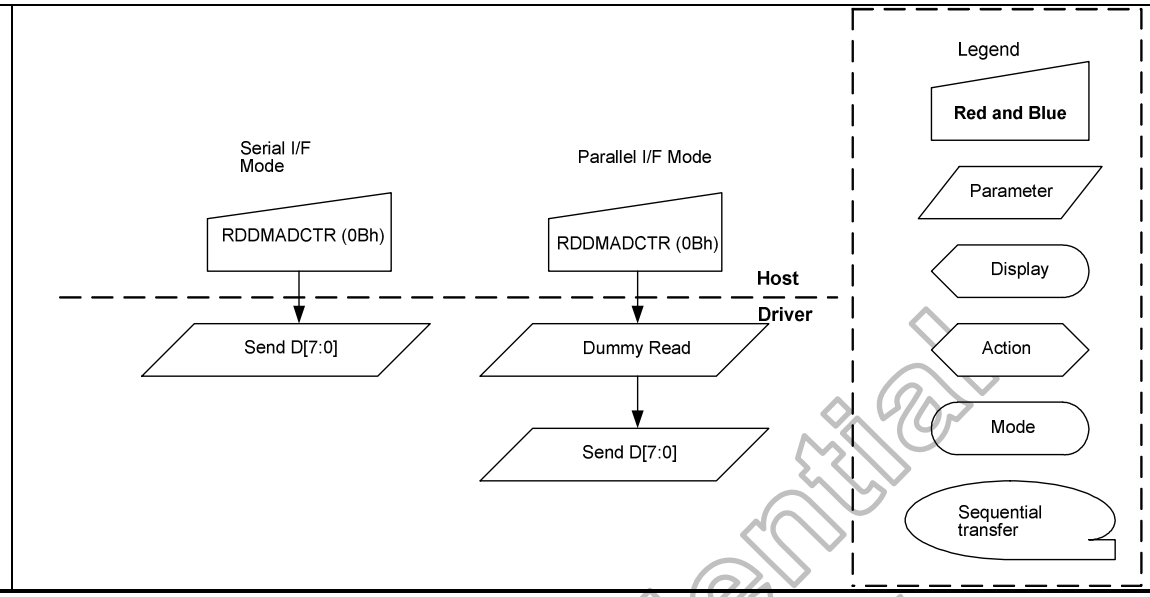
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

D[7:0] = 0x00h

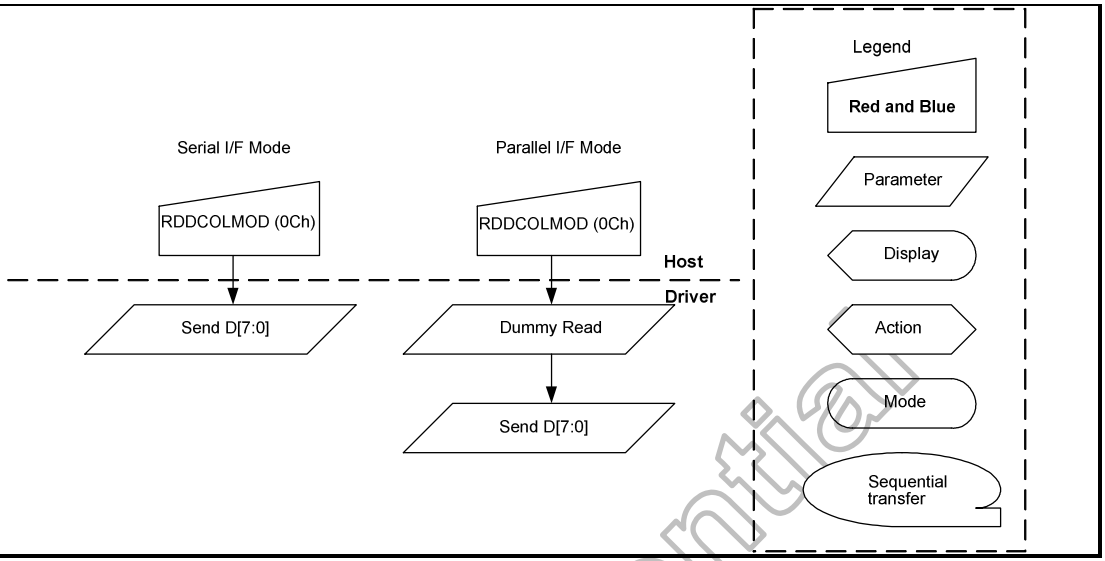
Flow Chart



6.2.9 Get_pixel_format (0Ch)

<table>
<tr><th rowspan="2">0CH</th><th colspan="13">RDDCOLMOD (Read Display COLMOD)</th></tr>
<tr><th>D/CX</th><th>RDX</th><th>WRX</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0C</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>Dummy read</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>-</td><td>D6</td><td>D5</td><td>D4</td><td>-</td><td>D2</td><td>D1</td><td>D0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>Reserved</td><td>Set to ‘0’</td></tr>
<tr><td>D6</td><td rowspan="3">DPI Interface Pixel format</td><td>-</td></tr>
<tr><td>D5</td><td>-</td></tr>
<tr><td>D4</td><td>-</td></tr>
<tr><td>D3</td><td>Reserved</td><td>Set to ‘0’</td></tr>
<tr><td>D2</td><td rowspan="3">DBI Interface Pixel format</td><td>-</td></tr>
<tr><td>D1</td><td>-</td></tr>
<tr><td>D0</td><td>-</td></tr>
</table>
Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition
Bits D2, D1, D0 – DBI Interface Colour Pixel Format Definition.
For Setting pixel format, see section 6.2.35 Set_pixel_format (3Ah)”.
<table>
<tr><th rowspan="2">Interface Colour Format</th><th>D6</th><th>D5</th><th>D4</th></tr>
<tr><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 bit/pixel</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 bit/pixel</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>24 bit/pixel</td><td>1</td><td>1</td><td>1</td></tr>
</table>
If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined.</td></tr>
<tr><td>Restrictions</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">D[7:0] = 0x07h</td></tr>
</table>

Flow Chart



6.2.10 Get_display_mode (0Dh)

0DH	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	0	1	0D
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	D5	0	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:
Bit D7 – Vertical Scrolling On/Off
'0' = Vertical Scrolling is Off.
'1' = Vertical Scrolling is On.
Bit D6 – Horizontal Scrolling Status
This bit is not applicable for this project, so it is set to '0'
Bit D5 – Inversion On/Off
'0' = Inversion is Off.
'1' = Inversion is On.
Bit D4, D4 – Reserved
Bits D2, D1, D0 – Gamma Curve Selection

Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Restrictions

-

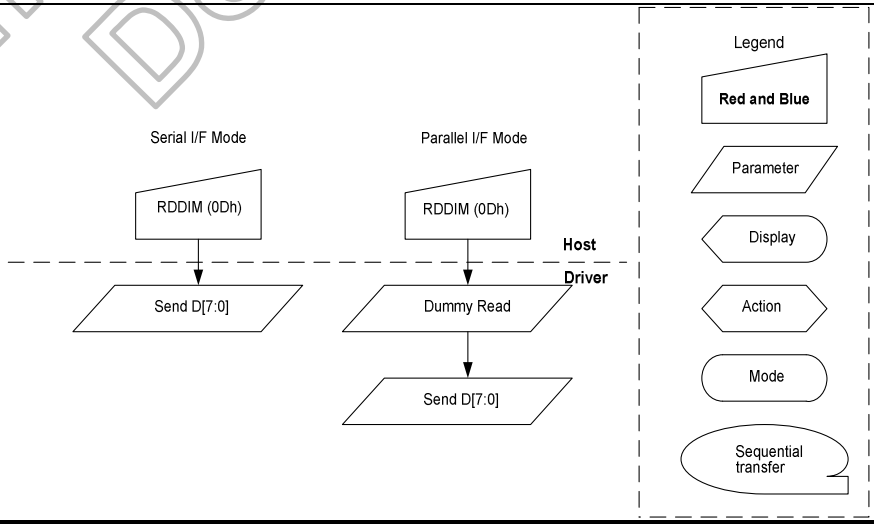
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

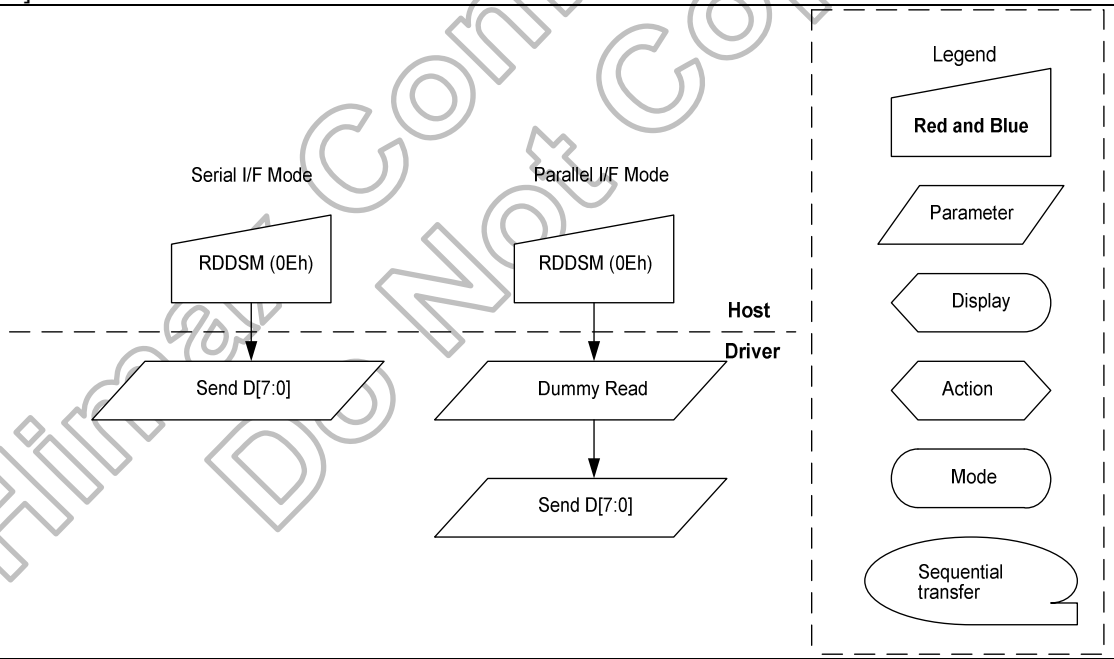
Default

D[7:0] = 0x00h

Flow Chart



6.2.11 Get_signal_mode (0Eh)

0EH	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	0	0E
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	D7	D6	0	0	0	0	0	0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 5.5.3 for mode definitions. '0' = Mode 1. '1' = Mode 2. D5 are D0 – are for future use and are set to '0'.												
Restrictions	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	D[7:0] = 0x00h												
Flow Chart													

6.2.12 Get_diagnostic_result (0Fh)

0FH	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	0	1	1	1	1	0F
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	1	1	-	D7	D6	D5	D4	0	0	0	0	xx

Description

The display module returns the self-diagnostic results following a Sleep Out command. See section 5.15 for a description of the status results.
Bit D7 – Register Loading Detection
Bit D6 – Functionality Detection
Bit D5 – Chip Attachment Detection
Set to '0' if feature unimplemented.
Bit D4 – Display Glass Break Detection
Set to '0' if feature unimplemented.
Bits D[3:0] – Reserved
Set to '0'.

Restrictions

-

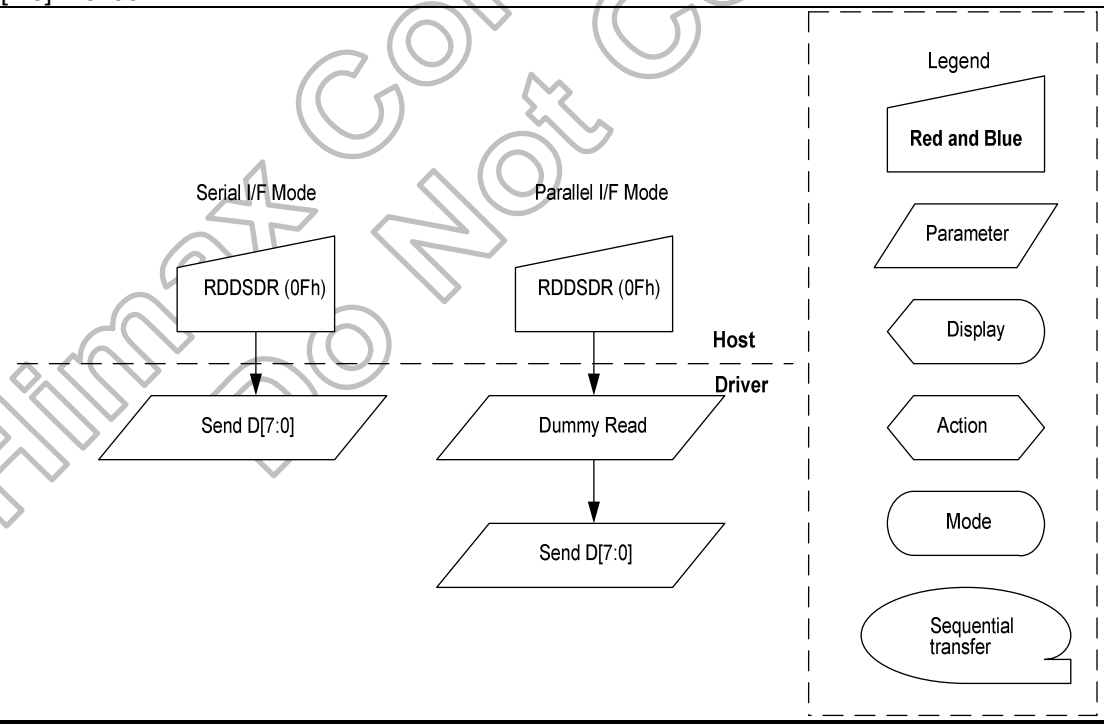
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

D[7:0] = 0x00h

Flow Chart

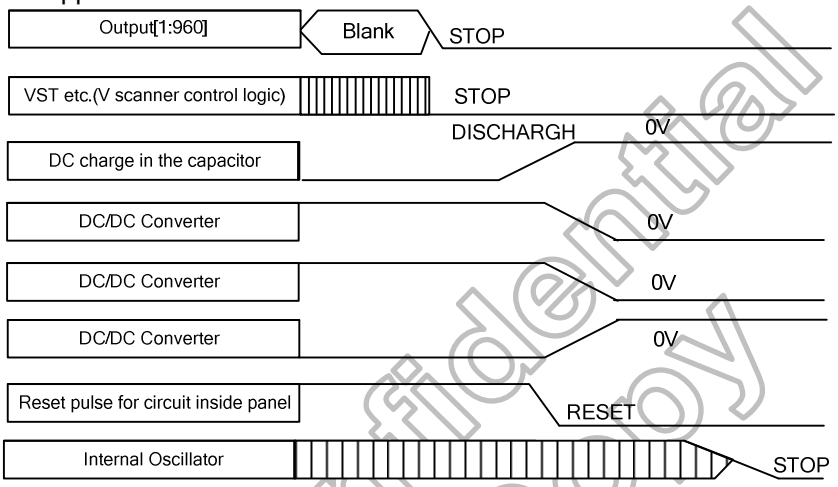


6.2.13 Enter_sleep_mode (10h)

10H	SLPIN (Sleep In)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	0	10
Parameter	NO PARAMETER												

Description

This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.



MCU interface and memory are still working and the memory keeps its contents.

Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

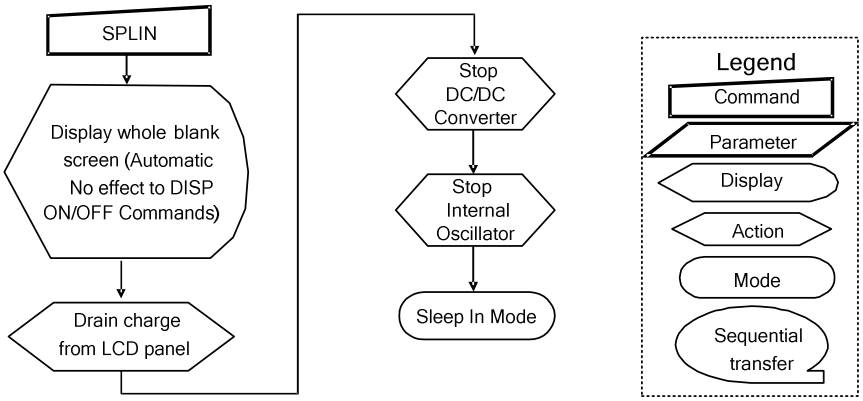
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

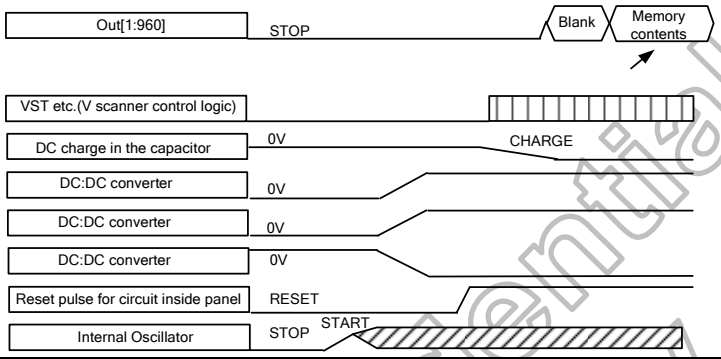
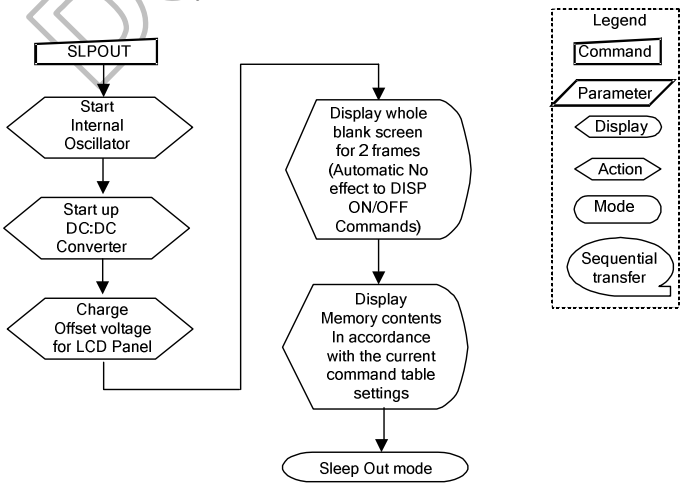
N/A

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



6.2.14 Exit_sleep_omde (11h)

11H	SLPOUT (Sleep Out)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started. 												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to alit 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	N/A												
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued. 												

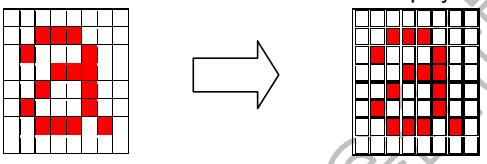
6.2.15 Enter_partial_mode (12h)

12H	PTLON (Partial Mode On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER												
Description	This command turns on partial mode The partial mode window is described by the “Set_partial_area” command (30H). To leave Partial mode, the “Enter_norma_mode” command (13H) should be written.												
Restrictions	This command has no effect when Partial mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	N/A												
Flow Chart	See Partial Area (30h)												

6.2.16 Enter_normal_mode (13h)

13H	NORON (Normal Display Mode On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	0	1	0	0	1	1	13
Parameter	NO PARAMETER												
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off.												
Restriction	This command has no effect when Normal Display mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In or Booster Off / Yes												
Default	N/A												
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.												

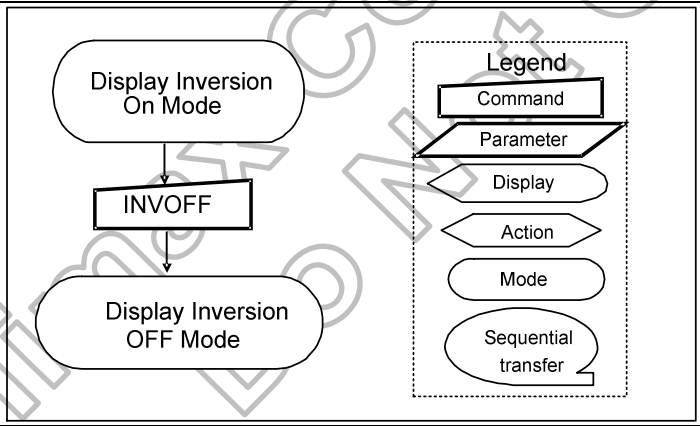
6.2.17 Exit_inversion_mode (20h)

20H	INVOFF (Display Inversion Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	No parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Memory (Example) Display 												
Restriction	This command has no effect when module is already in inversion off mode.												

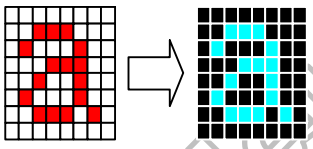
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default: N/A

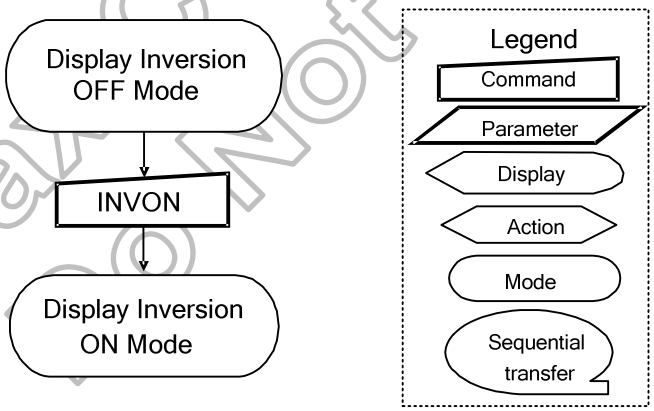
Flow Chart



6.2.18 Enter_inversion_mode (21h)

21H	INVON (Display Inversion On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER												
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in inversion on mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	N/A
Flow Chart	

6.2.19 Set_gamma_curve (26h)

26H	GAMSET (Gamma Set)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	1	1	0	26
Parameter	1	1	↑	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	1..08

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC[7..0]	Parameter	Curve selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

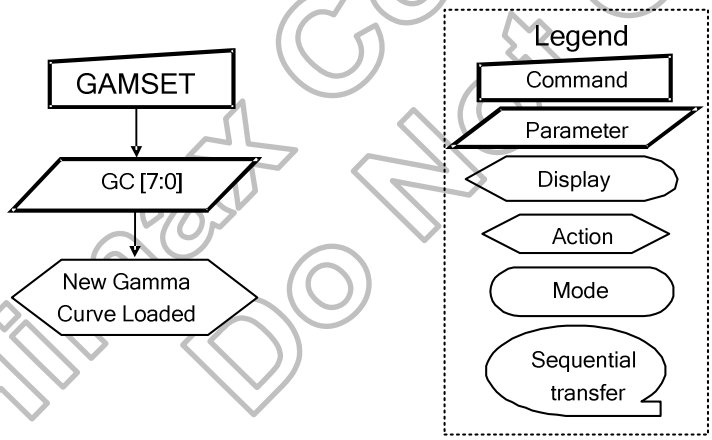
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

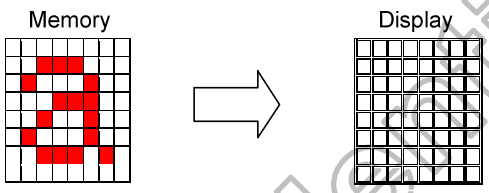
Default

GC[7:0] = 0x01h

Flow Chart



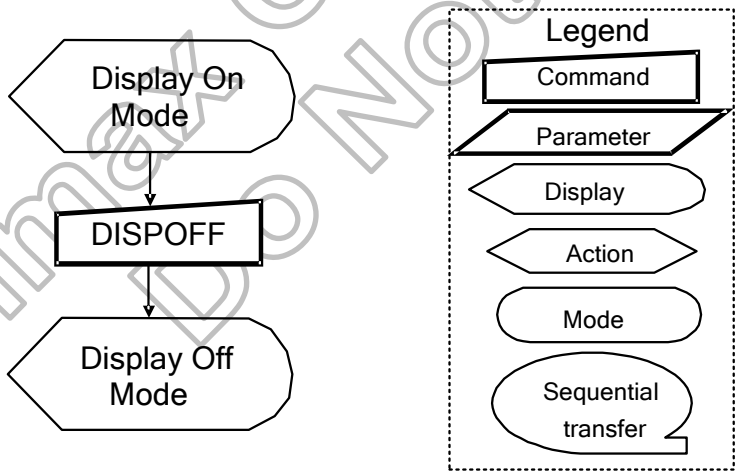
6.2.20 Set_display_off (28h)

28H	DISPOFF (Display Off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. Example 												
Restriction	This command has no effect when module is already in display off mode.												

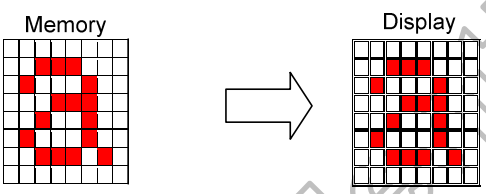
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default: N/A

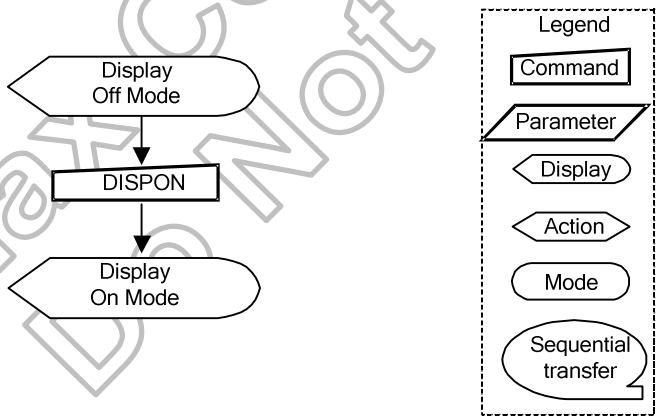
Flow Chart



6.2.21 Set_display_on (29h)

29H	DISPON (Display On)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) 												
Restriction	This command has no effect when module is already in display on mode.												

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

Default	N/A
Flow Chart	

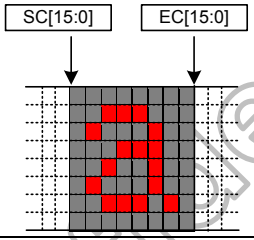
6.2.22 Set_clumn_address (2Ah)

2AH	CASET (Column Address Set)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	1	0	2A
1st parameter	1	1	↑	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	00..
2nd parameter	1	1	↑	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Note 1
3rd parameter	1	1	↑	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	00 ..
4th parameter	1	1	↑	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Note 1

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)



Restriction

SC[15:0] always must be equal to or less than EC[15:0]
Note 1: When SC[15:0] or EC[15:0] is greater than horizontal line (when MADCTL's B5=0) or vertical line (when MADCTL's B5=1), data of out of range will be ignored.

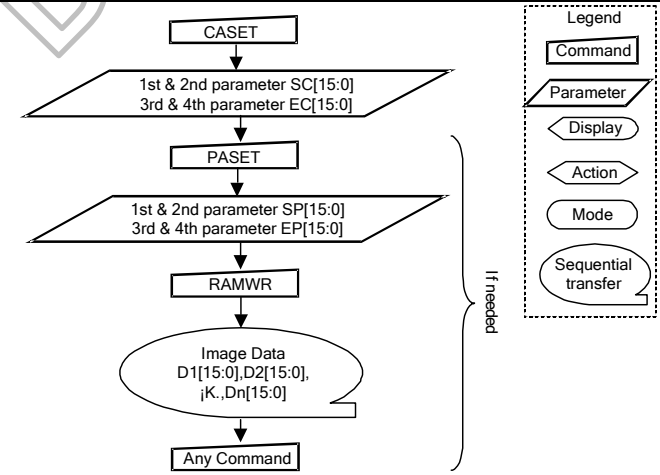
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

RES_SEL[2:0]=000, Resoultion 480RGBx864: SC[15:0] = 0x0000h, EC[15:0] = 0x01DFh
RES_SEL[2:0]=001, Resoultion 480RGBx854: SC[15:0] = 0x0000h, EC[15:0] = 0x01DFh
RES_SEL[2:0]=010, Resoultion 480RGBx800: SC[15:0] = 0x0000h, EC[15:0] = 0x01DFh
RES_SEL[2:0]=011, Resoultion 480RGBx640: SC[15:0] = 0x0000h, EC[15:0] = 0x01DFh
RES_SEL[2:0]=100, Resoultion 360RGBx640: SC[15:0] = 0x0000h, EC[15:0] = 0x0167h
RES_SEL[2:0]=101, Resoultion 480RGBx720: SC[15:0] = 0x0000h, EC[15:0] = 0x01DFh

Flow Chart



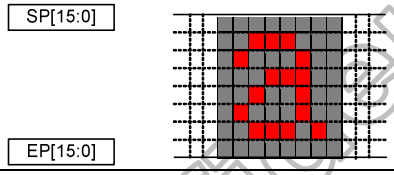
6.2.23 Set_page_address (2Bh)

2BH	PASET (Page Address Set)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	0	1	1	2B
1st parameter	1	1	↑	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	00 ..
2nd parameter	1	1	↑	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Note 1
3rd parameter	1	1	↑	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	00 .. Note 1
4th parameter	1	1	↑	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]
Note 1: When SP[15:0] or EP[15:0] is greater than vertical line (When MADCTL's B5=0) or horizontal line (When MADCTL's B5=1), data of out of range will be ignored.

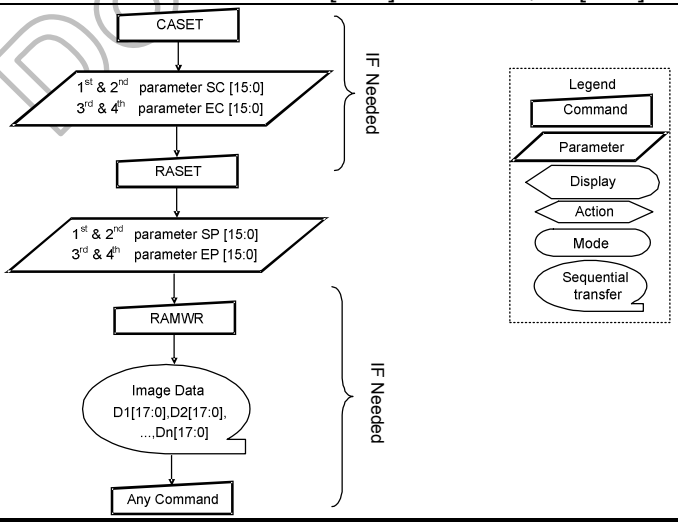
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

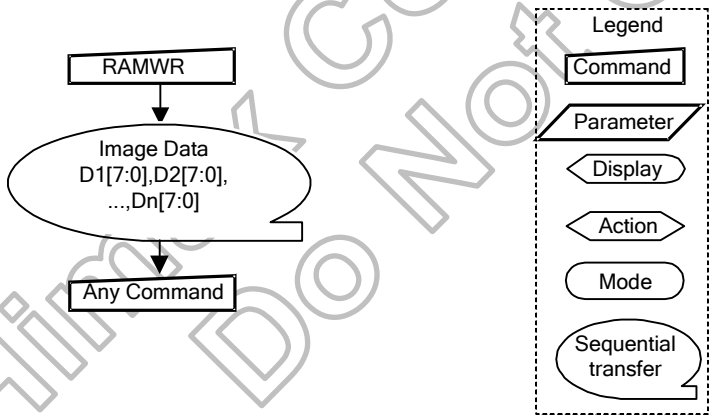
Default

RES_SEL[2:0]=000, Resoultion 480RGBx864: SP[15:0] = 0x0000h, EP[15:0] = 0x035Fh
RES_SEL[2:0]=001, Resoultion 480RGBx854: SP[15:0] = 0x0000h, EP[15:0] = 0x0355h
RES_SEL[2:0]=010, Resoultion 480RGBx800: SP[15:0] = 0x0000h, EP[15:0] = 0x031Fh
RES_SEL[2:0]=011, Resoultion 480RGBx640: SP[15:0] = 0x0000h, EP[15:0] = 0x027Fh
RES_SEL[2:0]=100, Resoultion 360RGBx640: SP[15:0] = 0x0000h, EP[15:0] = 0x027Fh
RES_SEL[2:0]=101, Resoultion 480RGBx720: SP[15:0] = 0x0000h, EP[15:0] = 0x02CFh

Flow Chart



6.2.24 Write_memory_start (2Ch)

2CH	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	1	0	0	2C
1st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address and set_page_address commands. The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.												
Restriction	In all colour modes, there is no restriction on length of parameters.												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes												
Default	Contents of memory is set randomly and not cleared.												
Flow Chart													

6.2.25 Colour Set (2Dh)

2DH	COLSET (Colour Set)												
	DNC	NRD	NWR	D8~D15	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	1	0	1	2D
1st parameter	1	1	↑	-	R007	R006	R005	R004	R003	R002	R001	R000	00..FF
:	1	1	↑	-	Rnn7	Rnn6	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	00..FF
64th parameter	1	1	↑	-	R637	R636	R635	R634	R633	R632	R631	R630	00..FF
65th parameter	1	1	↑	-	G007	G006	G005	G004	G003	G002	G001	G000	00..FF
:	1	1	↑	-	Gnn7	Gnn6	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	00..FF
128th parameter	1	1	↑	-	G637	G636	G635	G634	G633	G632	G631	G630	00..FF
129th parameter	1	1	↑	-	B007	B006	B005	B004	B003	B002	B001	B000	00..FF
:	1	1	↑	-	Bnn7	Bnn6	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	00..FF
192nd parameter	1	1	↑	-	B637	B636	B635	B634	B633	B632	B631	B630	00..FF
Description	This command is used to define the LUT for 18bit to 24bit, 16bit-to-24bit colour depth conversions colour depth conversions. 192bytes must be written to the LUT regardless of the colour mode. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.												
Restriction	This command is needed to be set in write_data for RGB 5-6-5 (65K colours) and RGB 6-6-6 (262K colours) pixel format. The default for command Colour Set (2Dh) is 0x00h. The colour depth conversion must be followed the below tables. Once write data is RGB 5-6-5 (65K colours), the set pixel format 0x3A=0x05h command must be set and using the 16bit-to-24bit colour depth conversion.												

R-G-B=5-6-5	RGBSET parameter	24- bit /pixel mode	LUT 24-bit /pixel value	Input 16-bit /pixel
R	1	R00[7:0]	00000000	00000
	2	R01[7:0]	00001000	00001
	3	R02[7:0]	00010000	00010
	..	..	..	..
	..	..	..	..
	30	R29[7:0]	11101111	11101
	31	R30[7:0]	11110111	11110
	32	R31[7:0]	11111111	11111
	33	Not Used	Not Used	Not Used
	34			
	35			
	..			
	..			
	62			
	63			
	64			
G	65	G00[7:0]	00000000	000000
	66	G01[7:0]	00000100	000001
	67	G02[7:0]	00001000	000010
	..	..	..	..
	..	..	..	..
	126	G61[7:0]	11110111	111101
	127	G62[7:0]	11111011	111110
	128	G63[7:0]	11111111	111111
B	129	B00[7:0]	00000000	00000
	130	B01[7:0]	00001000	00001
	131	B02[7:0]	00010000	00010
	..	..	..	..
	..	..	..	..
	158	B29[7:0]	11101111	11101
	159	B30[7:0]	11110111	11110
	160	B31[7:0]	11111111	11111
	161	Not Used	Not Used	Not Used
	162			
	163			

	..			
	..			
	190			
	191			
	192			

Once write data is RGB 5-6-5 (65K colours), the set pixel format 0x3A=0x06h command must be set and using the 18bit-to-24bit colour depth conversion.

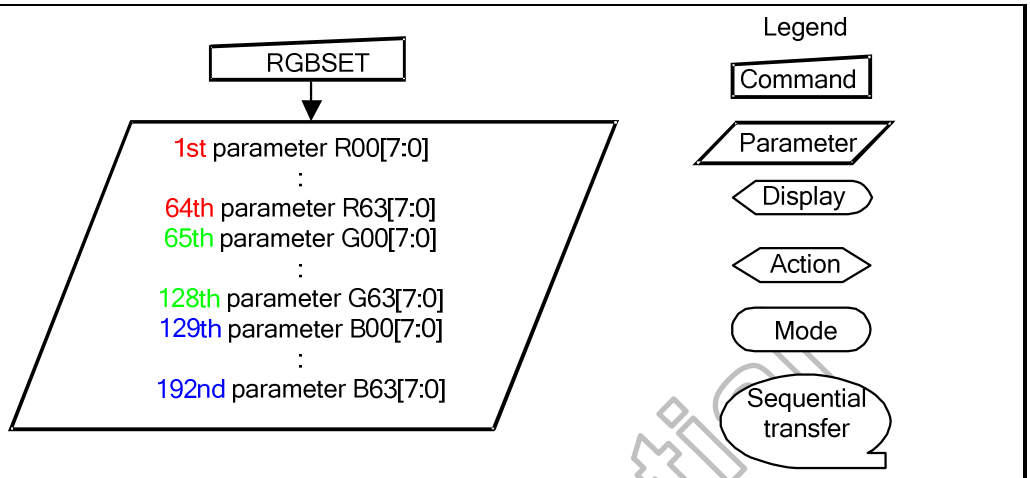
R-G-B=6-6-6	RGBSET parameter	24- bit /pixel mode	LUT 24-bit /pixel value	Input 18-bit /pixel
R	1	R00[7:0]	00000000	000000
	2	R01[7:0]	00000100	000001
	3	R02[7:0]	00001000	000010
	..	..	..	..
	..	..	..	..
	62	R61[7:0]	11110111	111101
	63	R62[7:0]	11111011	111110
	64	R63[7:0]	11111111	111111
G	65	G00[7:0]	00000000	000000
	66	G01[7:0]	00000100	000001
	67	G02[7:0]	00001000	000010
	..	..	..	..
	..	..	..	..
	126	G61[7:0]	11110111	111101
	127	G62[7:0]	11111011	111110
	128	G63[7:0]	11111111	111111
B	129	B00[7:0]	00000000	000000
	130	B01[7:0]	00000100	000001
	131	B02[7:0]	00001000	000010
	..	..	..	..
	..	..	..	..
	190	B61[7:0]	11110111	111101
	191	B62[7:0]	11111011	111110
	192	B63[7:0]	11111111	111111

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
S/W Reset	Contents of the look-up table protected
H/W Reset	R00[7:0]~R63[7:0] =0x00h G00[7:0]~G63[7:0] =0x00h B00[7:0]~B63[7:0] =0x00h

Flow Chart	

6.2.26 Raed_memory_start (2Eh)

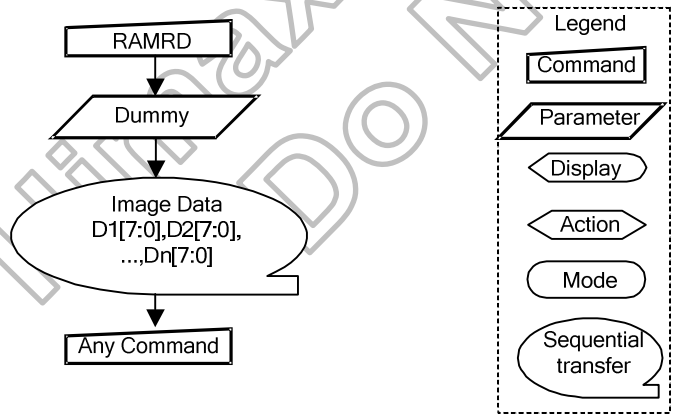
2EH	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	-	X	X	X	X	X	X	X	X	Dummy read
2nd parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
(n+1)th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands. The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.												
Restriction	In all colour modes, the Frame Read is always 24bit so there is no restriction on length of parameters. Note – Memory Read is only possible via the Parallel Interface.												

Register Availability

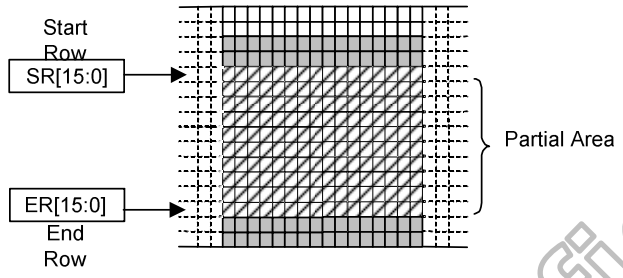
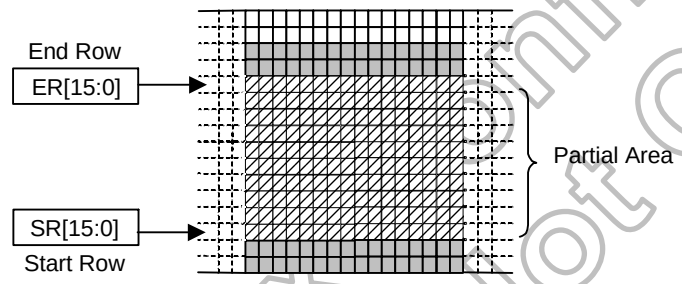
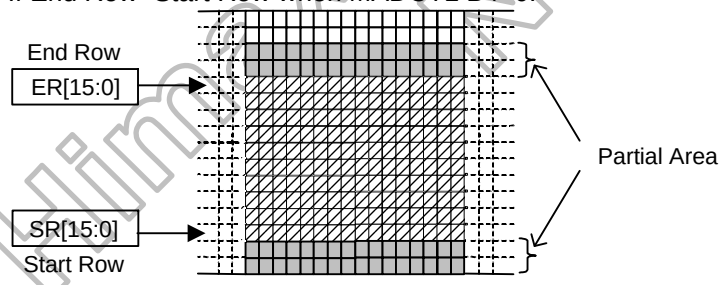
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default: Contents of memory is set randomly and not cleared.

Flow Chart

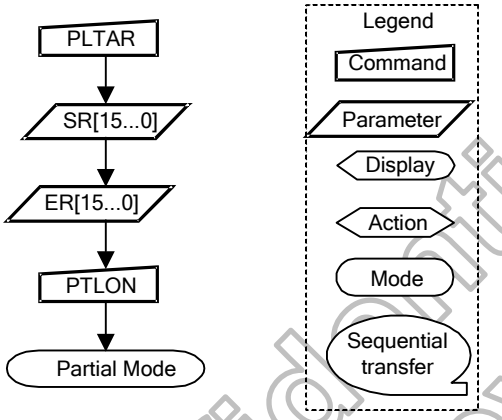
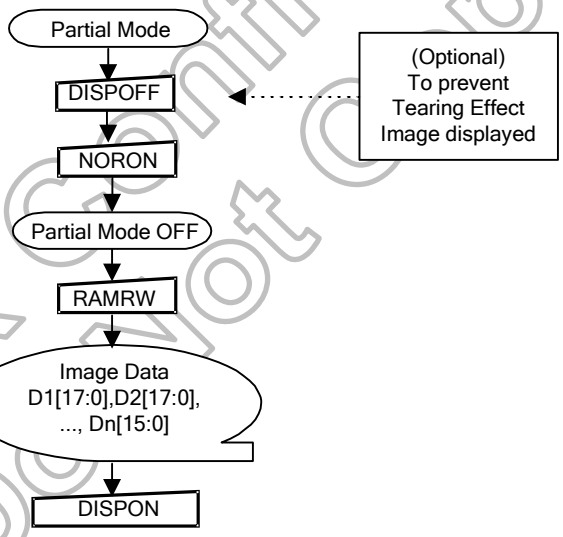


6.2.27 Set_partial_area (30h)

30H	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	0	0	0	30
1st parameter	1	1	↑	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	xx
2nd parameter	1	1	↑	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	xx
3rd parameter	1	1	↑	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	xx
4th parameter	1	1	↑	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	xx
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  If End Row>Start Row when MADCTL B4=1:-  If End Row<Start Row when MADCTL B4=0:-  If End Row = Start Row then the Partial Area will be one row deep.												
Restriction	SR[15..0] and ER[15..0] cannot be greater than horizontal line number.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

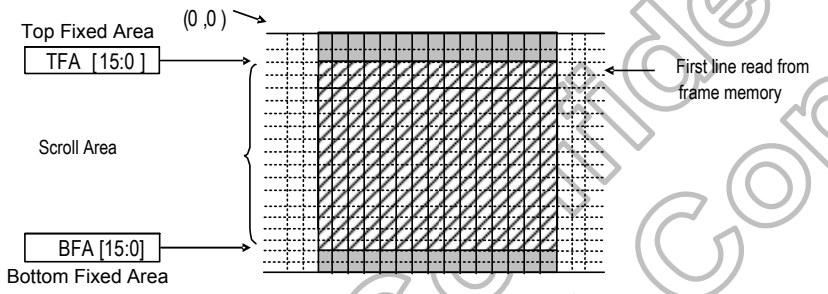
Default	RES_SEL[2:0]=000, Resoultion 480RGBx864: SR[15:0] = 0x0000h, ER[15:0] = 0x035Fh RES_SEL[2:0]=001, Resoultion 480RGBx854: SR[15:0] = 0x0000h, ER[15:0] = 0x0355h RES_SEL[2:0]=010, Resoultion 480RGBx800: SR[15:0] = 0x0000h, ER[15:0] = 0x031Fh RES_SEL[2:0]=011, Resoultion 480RGBx640: SR[15:0] = 0x0000h, ER[15:0] = 0x027Fh RES_SEL[2:0]=100, Resoultion 360RGBx640: SR[15:0] = 0x0000h, ER[15:0] = 0x027Fh RES_SEL[2:0]=101, Resoultion 480RGBx720: SR[15:0] = 0x0000h, ER[15:0] = 0x02CFh
Flow Chart	1. To Enter Partial Mode:-  2. To Leave Partial Mode 

6.2.28 Set_scroll_area (33h)

33H	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	0	1	1	33
1st parameter	1	1	↑	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	xx
2nd parameter	1	1	↑	-	TFA7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA1	TFA0	xx
3rd parameter	1	1	↑	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8	xx
4th parameter	1	1	↑	-	VSA7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA1	VSA0	xx
5th parameter	1	1	↑	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	xx
6th parameter	1	1	↑	-	BFA7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA1	BFA0	xx

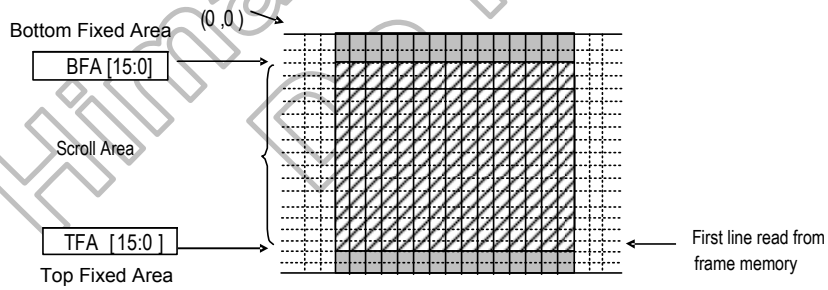
Description

This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0, the 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



When MADCTL B4=1

The 1st & 2nd parameter TFA[15..0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15..0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15..0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



Restriction

The condition is (TFA+VSA+BFA)= Vertical line number, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

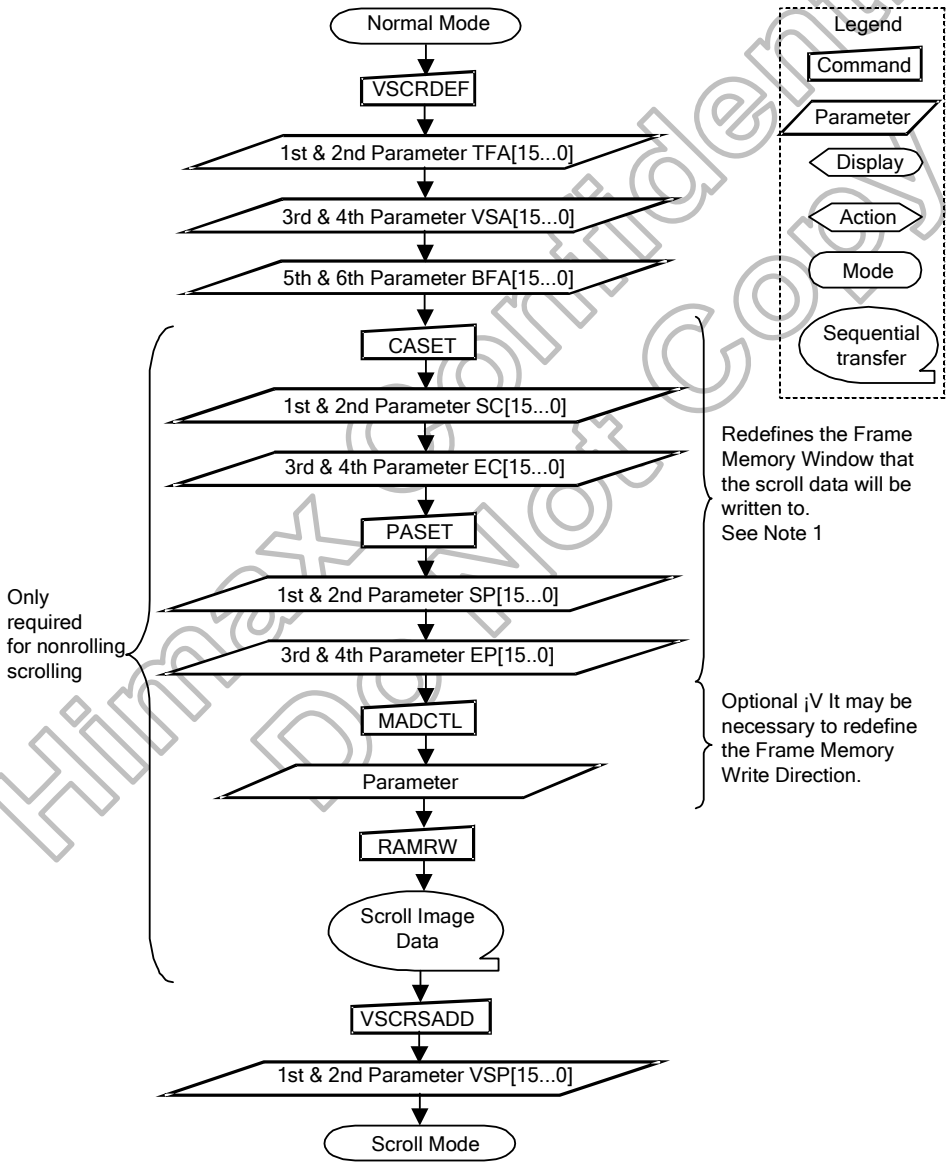
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value		
RES_SEL[2:0]=000, 480RGBx864	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0360h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=001, 480RGBx854	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0356h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=010, 480RGBx800	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0320h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=011, 480RGBx640	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0280h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=100, 360RGBx640	TFA[15..0]= 0x0000h	VSA[15..0]= 0x0280h	BFA[15..0]= 0x0000h
RES_SEL[2:0]=101,	TFA[15..0]= 0x0000h	VSA[15..0]= 0x02D0h	BFA[15..0]= 0x0000h

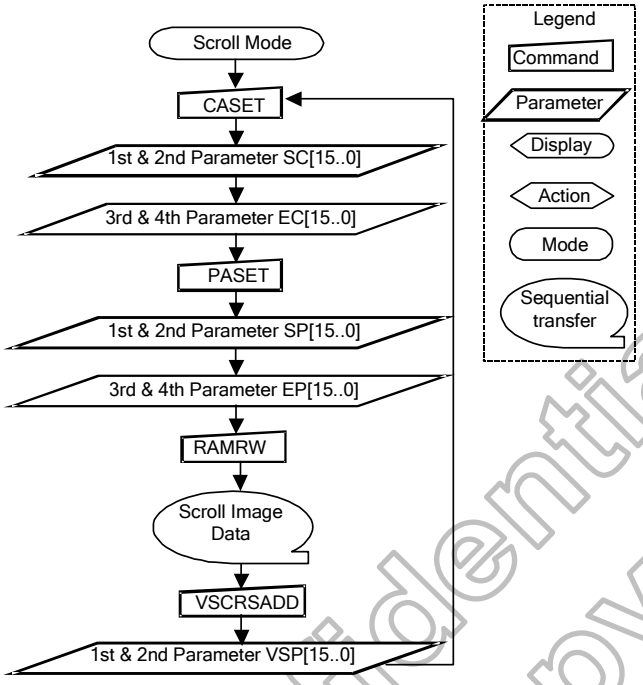
Flow Charts

1.To enter Vertical Scroll Mode:

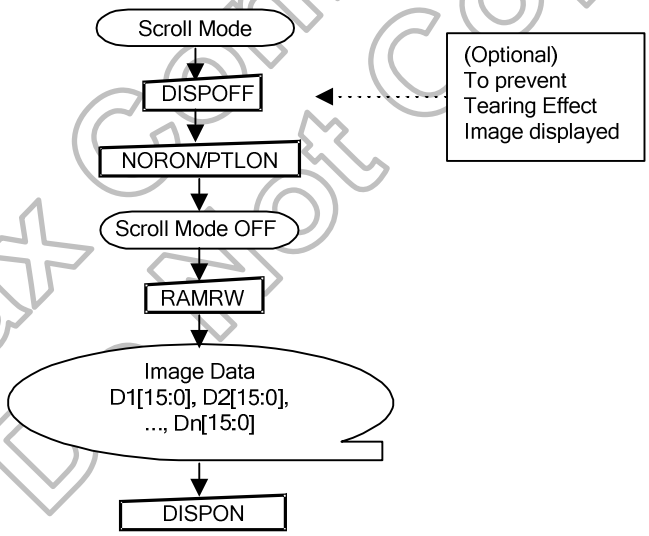


Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:

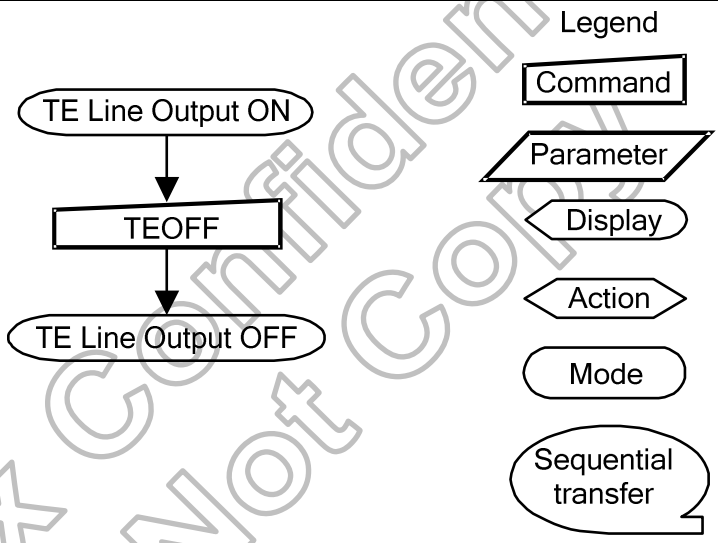


3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

6.2.29 Tearing effect line off (34h)

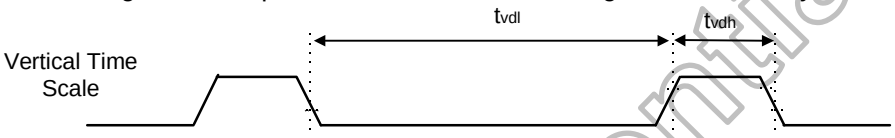
34H	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	OFF												
Flow Chart													

6.2.30 Set_tear_on (35h)

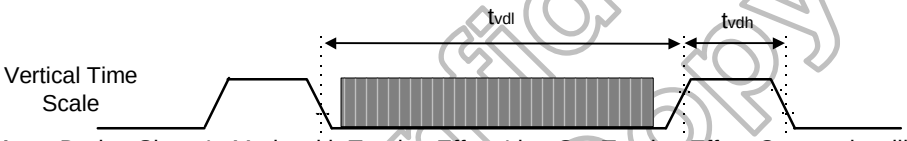
35H	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	-	X	X	X	X	X	X	X	M	xx

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal
line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).
When M=0:
The Tearing Effect Output line consists of V-Blanking information only:



When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

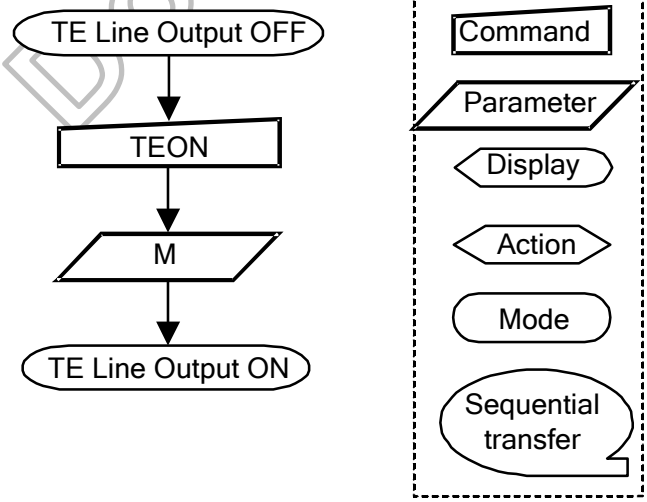
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

OFF

Flow Chart



6.2.31 Set_address_mode (36h)

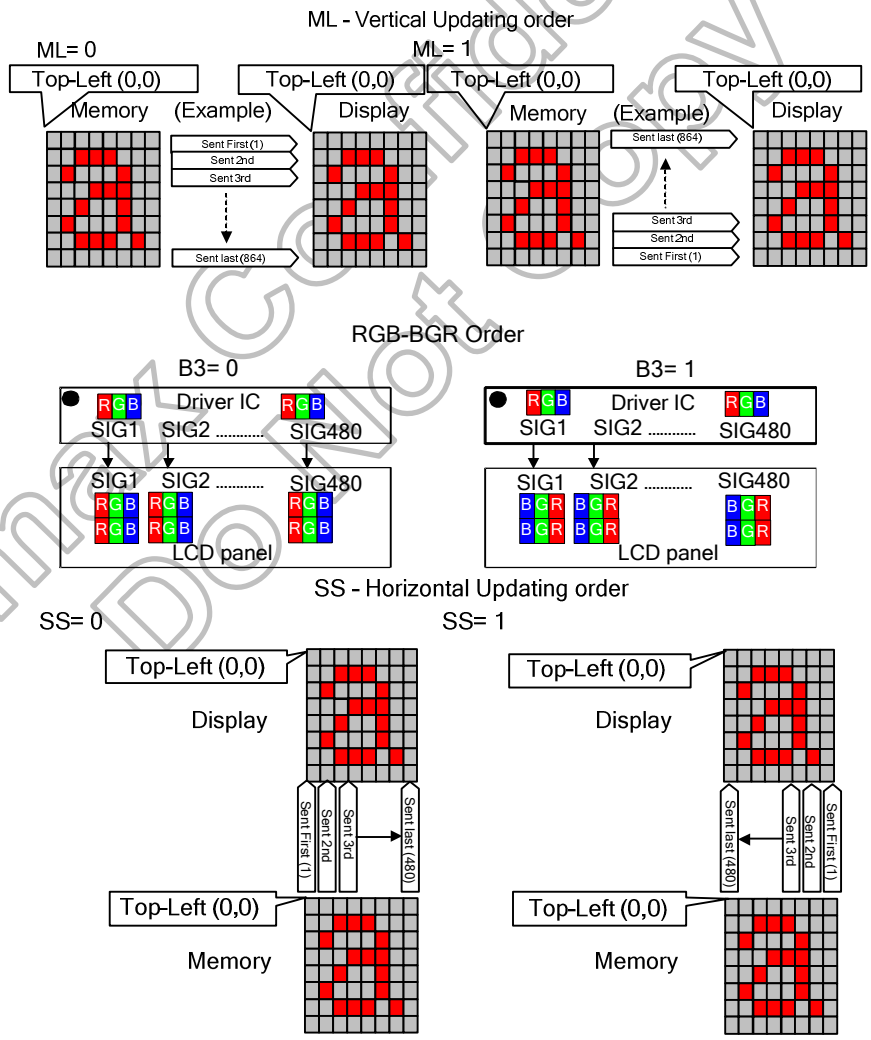
36H	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	0	36
1st parameter	1	1	↑	-	B7	B6	B5	B4	B3	B2	X	X	XX

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit Assignment

BIT	NAME	DESCRIPTION
B7	PAGE ADDRESS ORDER (MY)	These 3 bits controls MCU to memory write/read direction.
B6	COLUMN ADDRESS ORDER (MX)	
B5	PAGE/COLUMN SELECTION (MV)	
B4	Vertical ORDER (ML)	LCD vertical refresh direction control
B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)
B2	Horizontal ORDER (SS)	LCD horizontal refresh direction control



Note: Top-Left (0,0) means a physical memory location.
Bit D1 – Switching Between Segment Output and RAM
Bit D0 – Switching Between Common Output and RAM

Restriction: -

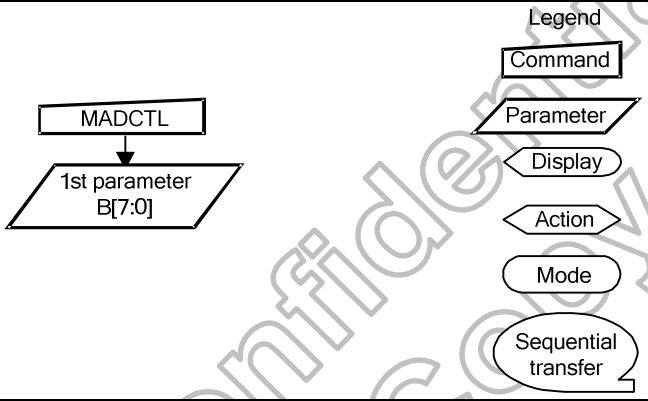
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value
Power On Sequence	B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0
S/W Reset	No Change

Flow Chart



6.2.32 Set_scroll_start (37h)

37H	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	-	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	00. 13F
2nd parameter	1	1	↑	-	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	

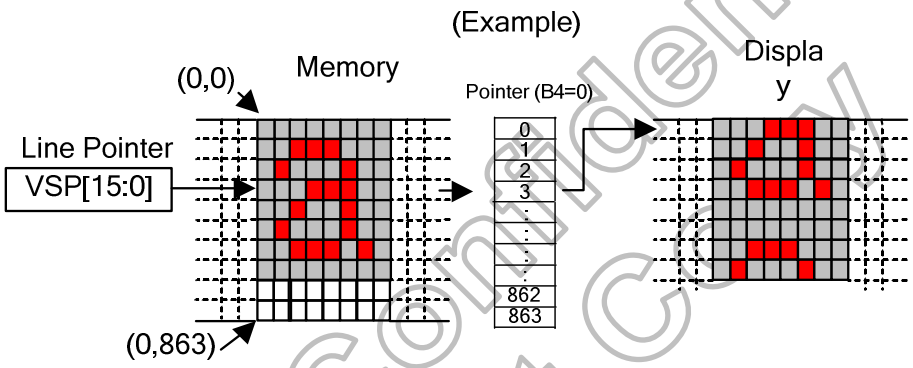
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

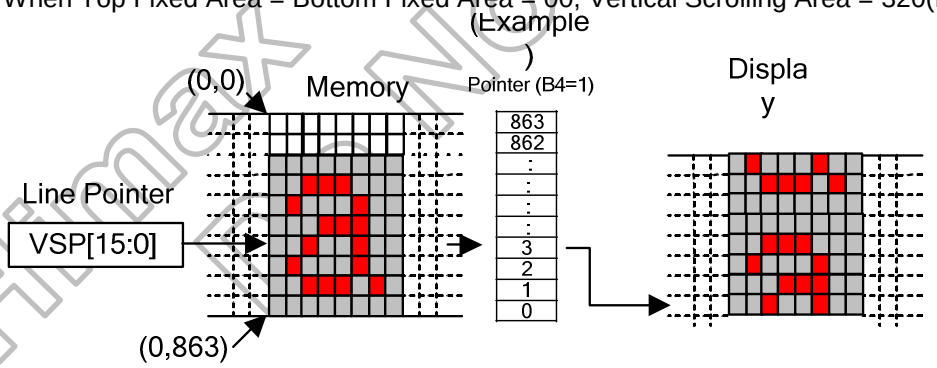
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 864(DM=10) and



When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320(DM=10) and



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	No
Partial Mode On, Idle Mode On, Sleep Out	No

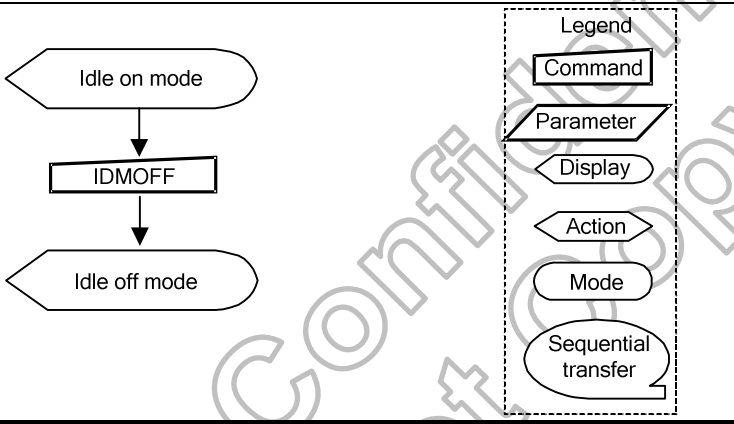
Default

VSP[15:0]= 0x0000h

Flow Chart

See Vertical Scrolling Definition (33h) description.

6.2.33 Idle mode off (38h)

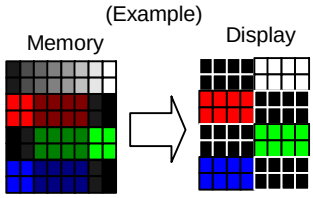
38H	IDMOFF (Idle mode off)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colours.												
Restriction	This command has no effect when module is already in idle off mode.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	Idle mode is OFF.												
Flow Chart													

6.2.34 Enter_Idle_mode (39h)

39H	IDMON (Idle mode on)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.



Memory contents vs. Display Colour

	R7 - R0	G7 - G0	B7 - B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magent	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X=don't care

Restriction

This command has no effect when module is already in idle on mode.

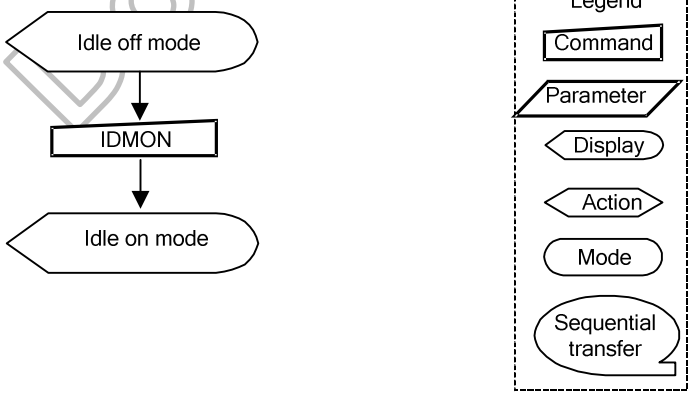
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Idle mode is OFF.

Flow Chart



6.2.35 Set_pixel_format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	0	1	0	3A
1st parameter	1	1	↑	-	X	D6	D5	D4	X	D2	D1	D0	XX

Description

This command is used to define the format of RGB picture data.
D6~D4 : DPI Pixel format Definition.
D2~D0 : DBI Pixel format Definition.
The formats are shown in the table:

Pixel Format	D6/D2	D5/D1	D4/D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

If a particular interface, enter DBI or DPI, is not used then the correspondind bits in the parameter returned from the display module undefined.

Restriction

There is no visible effect until the Frame Memory is written to.

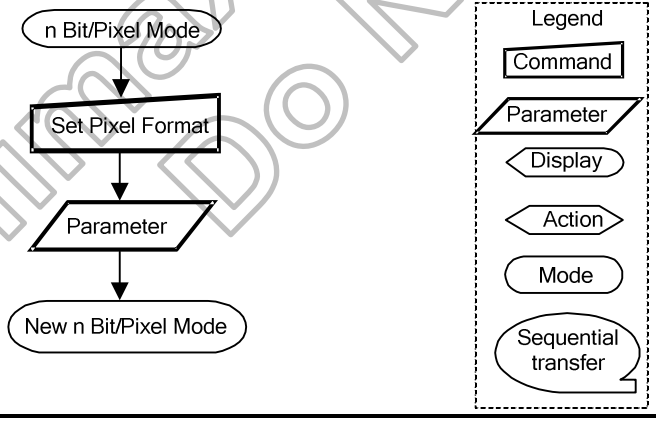
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value
Power On Sequence	24 Bit/Pixel

Flow Chart



6.2.36 Write_memory_contiune (3Ch)

3CH	Write_memory_contiune												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	0	0	3C
1st parameter	1	1	↑	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	1	↑	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
Nth parameter	1	1	↑	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF

Description

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. Sending any other command can stop frame Write.
If set_address_mode B5 = 0:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.
If set_address_mode B5 = 1:
Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Restriction

In all colour modes, there is no restriction on length of parameters.

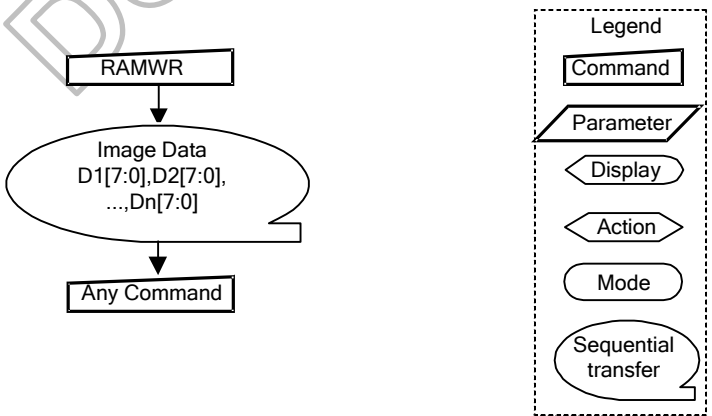
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is set randomly

Flow Chart



6.2.37 Raed_memory_continue (3Eh)

3EH	Raed_memory_continue												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	1	1	1	0	3E
1st parameter	1	↑	1	-	X	X	X	X	X	X	X	X	Dummy read
2nd parameter	1	↑	1	-	D17	D16	D15	D14	D13	D12	D11	D10	00..FF
:	1	↑	1	-	Dx7	Dx6	Dx5	Dx4	Dx3	Dx2	Dx1	Dx0	00..FF
(n+1)th parameter	1	↑	1	-	Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0	00..FF
Description	This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command. If set_address_mode B5=0: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If set_address_mode B5=1: Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.												
Restriction	Regardless of the color mode set in set_pixel_format, the pixel format returned by read_memory_continue is always 24-bit so there is no restriction on the length of data. A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.												

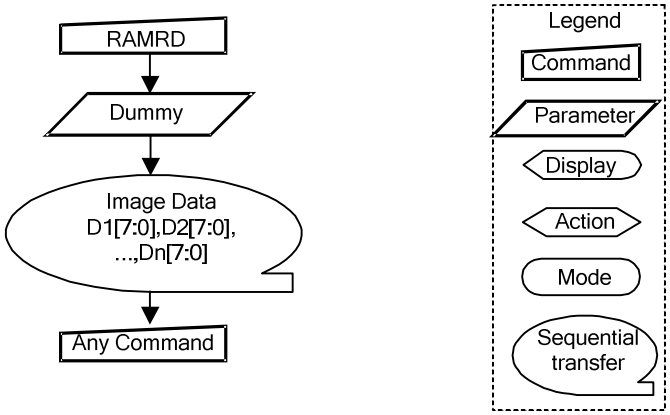
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

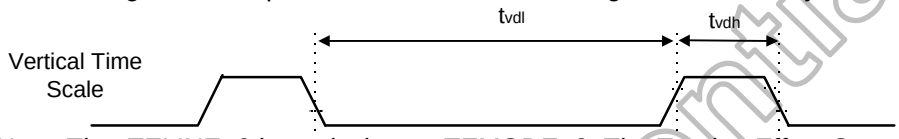
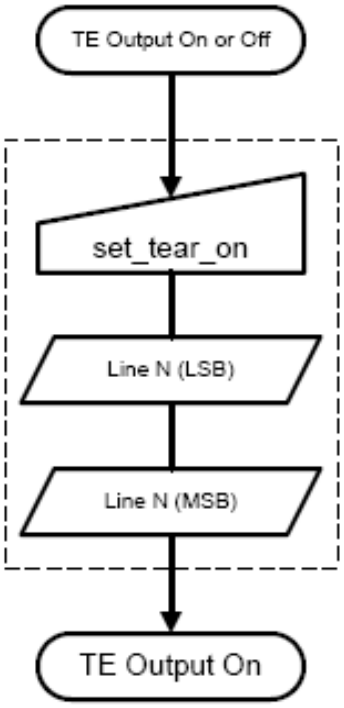
Default

Status	Default value
Power On Sequence	Contents of memory is set randomly

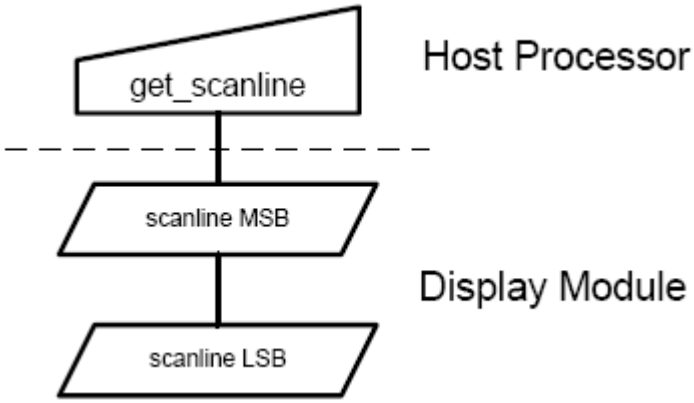
Flow Chart



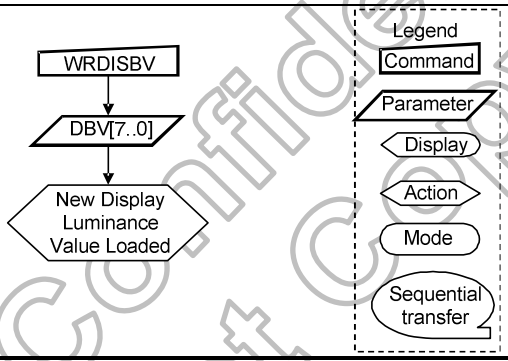
6.2.38 Set tear scan lines (44h)

44H	TESL (Tear Effect Scan Lines)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44
1st parameter	1	1	↑	-	TELINE[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	TELINE[7:0](8'b0)								00..FF
Description	This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reacfes line TELINE. The TE signal is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. The Tearing Effect Output line consists of V-Blanking information only:  Note: That TELINE=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.												
Restriction	The command has no effect when Tearing Effect output is already ON.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	TELINE[15:0]=0x0000h												
Flow Chart	 												

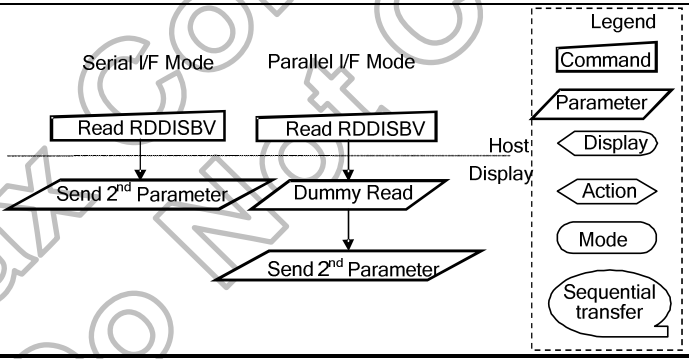
6.2.39 Get the current scanline(45h)

45H	GETSCAN (Get the current scanline)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	0	0	1	0	1	45
1st parameter	1	1	↑	-	SLN[15:8](8'b0)								00..FF
2nd parameter	1	1	↑	-	SLN[7:0](8'b0)								00..FF
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes												
Default	SLN[15:0]= 0x0000h												
Flow Chart													

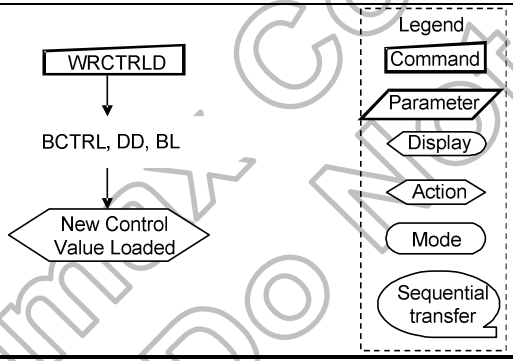
6.2.40 Write display brightness (51h)

51H	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	0	1	51
1st parameter	1	1	↑	-	DBV[7:0]								00 .. FF
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “5.18.3 Brightness Control Block”.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	DBV[7:0]= 0x00h												
Flow Chart													

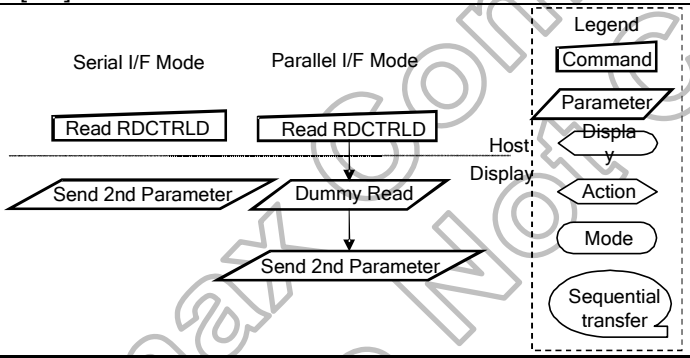
6.2.41 Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	0	52
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read
2nd parameter	1	↑	1	-	DBV[7:0]								xx
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display modulespecification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapters: “5.18.3 Brightness Control Block”, and “6.2.40 Write Display Brightness (51h)” DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is ‘0’ when bit BCTRL of “6.2.42 Write CTRL Display (53h)” command is ‘0’. DBV[7:0] is manual set brightness specified with “6.2.42 Write CTRL Display (53h)” command when bit BCTRL is ‘1’. When bit BCTRL of “6.2.42 Write CTRL Display (53h)” command is ‘1’ and bit C1/C0 of “6.2.44 Write Content Adaptive Brightness Control (55h)” are ‘0’, DBV[7:0] output is the brightness value specified with “6.2.40 Write Display Brightness (51h)” command.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	DBV[7:0]= 0x00h												
Flow Chart													

6.2.42 Write CTRL display (53h)

53H	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	0	1	1	53
1st parameter	1	1	↑	-	xx	xx	BCTRL	xx	DD	BL	xx	xx	00 .. FF
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don’t care.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0]= 0x00h												
Flow Chart													

6.2.43 Read CTRL value display (54h)

54H	RDCTRLD (Read Control Value Display)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	0	0	54
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd arameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	xx
Description	This command returns ambient light and brightness control values, see chapter: "6.2.42 Write CTRL Display (53h)". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0]= 0x00h												
Flow Chart													

6.2.44 Write content adaptive brightness control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	0	1	55
1st parameter	1	1	↑	-	xx	xx	xx	xx	xx	xx	CABC[1:0]		xx

Description

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.18 Content Adaptive Brightness Control (CABC)".

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

X = Don't care.

Restriction

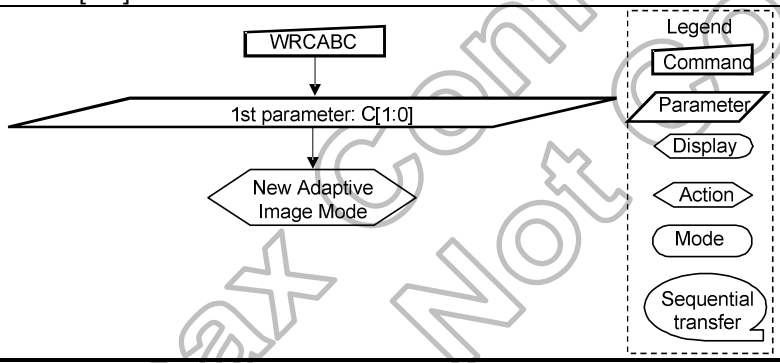
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

CABC[1:0] = 00

Flow Chart



6.2.45 Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	0	1	1	0	56
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read
2nd parameter	1	↑	1	-	0	0	0	0	0	0	C1	C0	xx

Description

This command is used to set parameters for image content based adaptive brightness control functionality.
There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.18 Content Adaptive Brightness Control (CABC)".

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

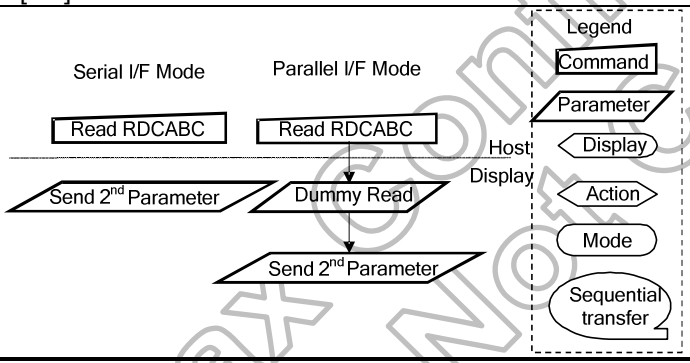
Restriction

Register Availability

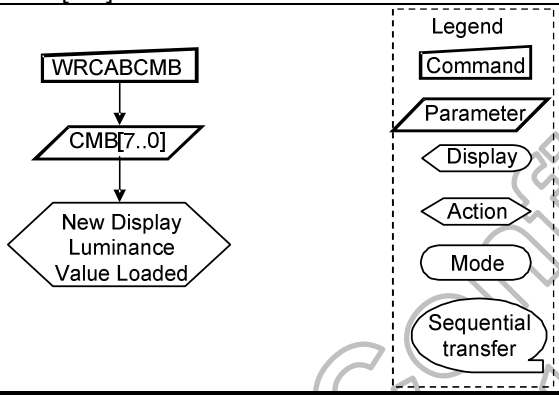
Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default: C[1:0] = 00

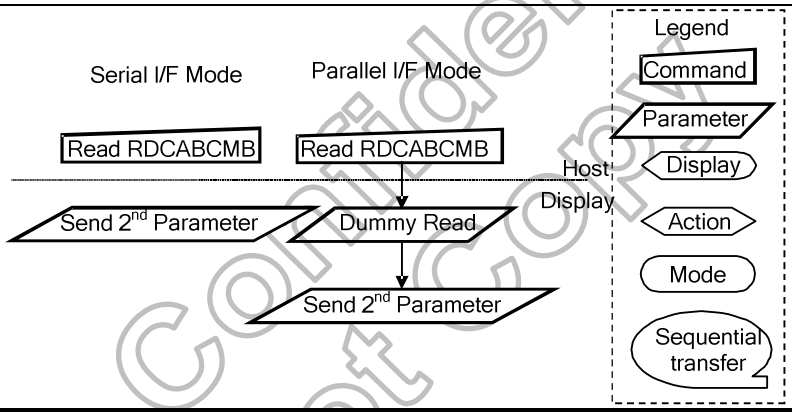
Flow Chart



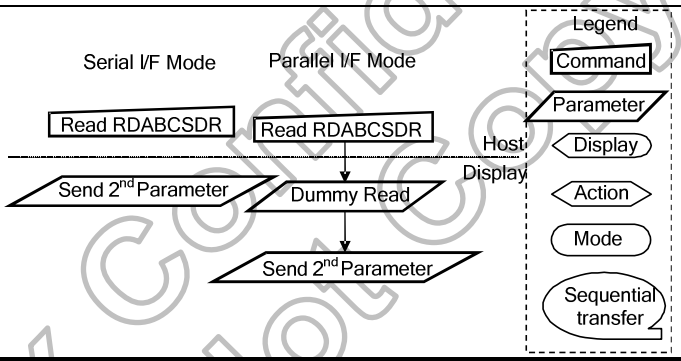
6.2.46 Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	0	5E
1st parameter	1	1	1	-	CMB[7:0]								00 .. FF
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter “5.18.4 Minimum brightness setting of CABC function”.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	CMB[7:0] = 0x00h												
Flow Chart													

6.2.47 Read CABC minimum brightness (5Fh)

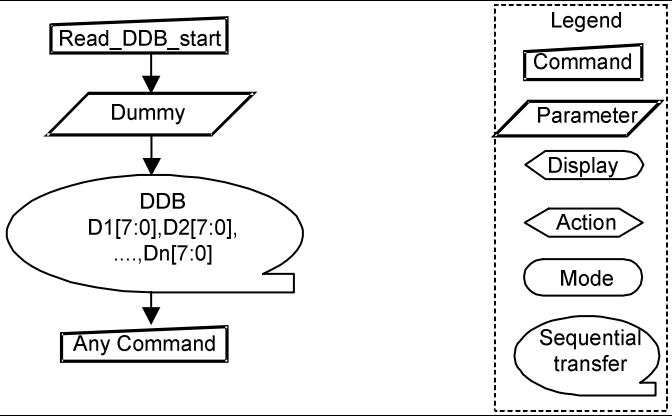
5FH	RDCABCMB (Read CABC minimum brightness)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	0	1	1	1	1	1	5F
1st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX
2nd parameter	1	↑	1	-	CMB[7:0]								XX
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter “5.18.4 Minimum brightness setting of CABC function”. CMB[7:0] is CABC minimum brightness specified with “6.2.46 Write CABC minimum brightness (5Eh)” command.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	CMB[7:0] = 0x00h												
Flow Chart													

6.2.48 Read automatic brightness control self-diagnostic result (68h)

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	1	1	0	1	0	0	0	68
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	D[7:6]		0	0	0	0	0	0	xx
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below: ● Bit D7 – Register Loading Detection See section “5.15.1 Register loading Detection”. ● Bit D6 – Functionality Detection See section “5.15.2 Functionality Detection “. ● Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’.												
Restriction	-												
Register Availability	Status: Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes												
Default	D[7:0] = 0x00h												
Flow Chart													

6.2.49 Read_DDB_start (A1h)

A1H	Read_DDB_start												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	0	0	0	1	A1
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	X	Dummy read
2nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Nth parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Description	This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data. The format of returned data is as follows: Parameter 2: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 3: MS (most significant) byte of Supplier ID. Parameter 4: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example. Parameter 5: MS (most significant) byte of Supplier Elective Data Parameter 6: single-byte *Escape or Exit Code* (EEC). The code is interpreted as follows: - FFh - Exit code – there is no more data in the Descriptor Block - 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard) - Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in *MIPI Alliance Standard for Device Descriptor Block (DDB)*. DDBs may contain many more data fields providing information about the peripheral. In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the bus turn-around token. The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command. The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB. Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.												
Restrictions	-												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes												
Default	D[7:0] = 0x00h												

Flow Chart	

6.2.50 Read_DDB_continue (A8h)

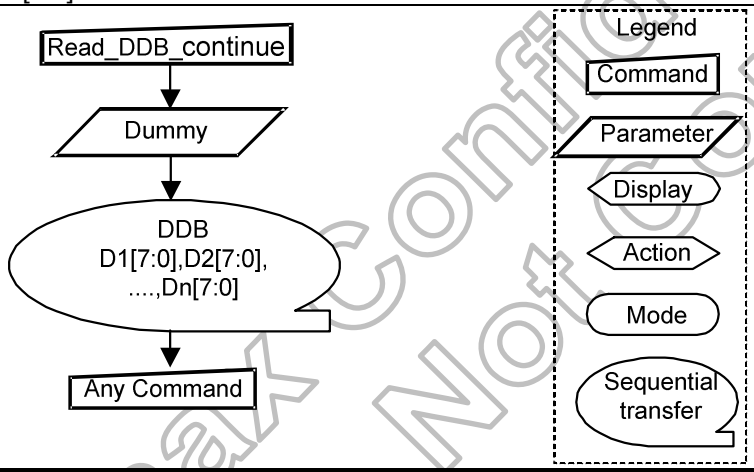
A8H	Read_DDB_continue												
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	1	0	0	0	A8
1st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read
2nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Nth parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.												
Restrictions	-												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default: D[7:0] = 0x00h

Flow Chart



6.2.51 Read ID1 (DAh)

DAH	RDID1 (Read ID1)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	0	1	0	DA
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	-	module's manufacturer[7:0]								xx
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.												
Restriction	-												

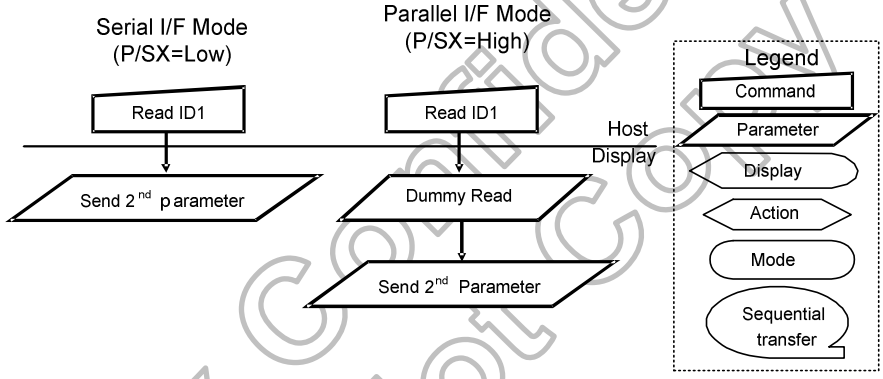
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

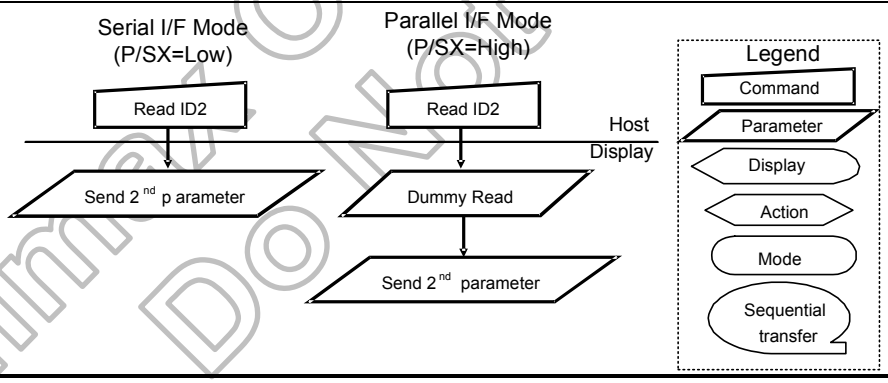
Default

Default value	OTP value
ID1[7:0]=0x00h	Define by customer

Flow Chart



6.2.52 Read ID2 (DBh)

<table>
<tr><th rowspan="2">DBH</th><th colspan="13">RDID2 (Read ID2)</th></tr>
<tr><th>DNC</th><th>NRD</th><th>NWR</th><th>D15~D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DB</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td>-</td><td colspan="7">LCD module/driver version [6:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:
<table>
<tr><th>ID Byte Value V[7:0]</th><th>Version</th><th>Changes</th></tr>
<tr><td>80h</td><td></td><td></td></tr>
<tr><td>81h</td><td></td><td></td></tr>
<tr><td>82h</td><td></td><td></td></tr>
<tr><td>83h</td><td></td><td></td></tr>
<tr><td>84h</td><td></td><td></td></tr>
<tr><td>85h</td><td></td><td></td></tr>
</table>
X= Don't care</td></tr>
<tr><td>Restrictions</td><td colspan="13">-</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Default value</th><th>OTP value</th></tr>
<tr><td>ID2[6:0]=0x00h</td><td>Define by customer</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.53 Read ID3 (DCh)

DCH	RDID3 (Read ID3)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd parameter	1	↑	1	-	LCD module/driver ID[7:0]								xx
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.												
Restrictions	-												

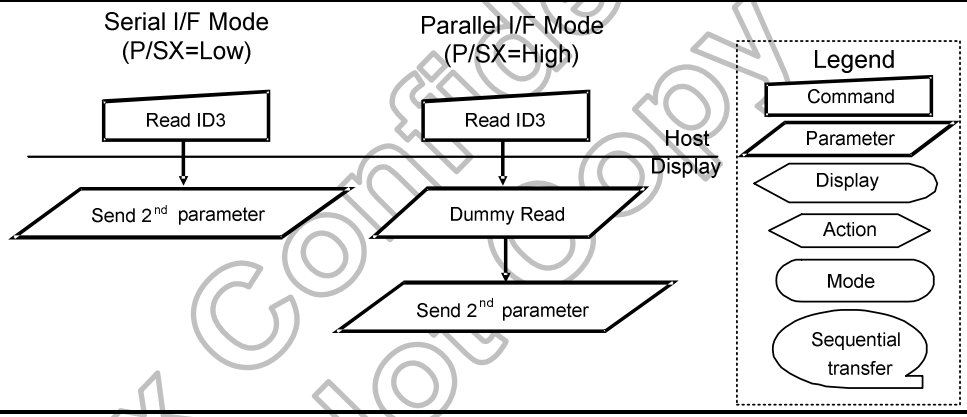
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Default value	OTP value
ID3[7:0]=0x00h	Define by customer

Flow Chart



6.2.54 SETOSC: Set internal oscillator (B0h)

B0H	SETOSC(Set Internal Oscillator)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	OSC_EN	-
2nd parameter	1	1	↑	-	-	-	-	-	UADJ[3:0]				-

Description

This command is used to set internal oscillator related setting
OSC_EN: Enable internal oscillator, High active.
UADJ[3:0]: For User to adjust OSC frequency, default is 15 MHZ.

UADJ				Internal oscillator frequency
0	0	0	0	28.0%
0	0	0	1	34.8%
0	0	1	0	41.5%
0	0	1	1	48.1%
0	1	0	0	54.7%
0	1	0	1	61.3%
0	1	1	0	67.8%
0	1	1	1	74.4%
1	0	0	0	80.6%
1	0	0	1	87.2%
1	0	1	0	93.5%
1	0	1	1	**100.0%**
1	1	0	0	106.4%
1	1	0	1	112.7%
1	1	1	0	119.4%
1	1	1	1	125.8%

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	OSC_EN=0, UADJ[3:0]= 1011	UADJ[3:0]

6.2.55 SETPOWER: Set power (B1h)

B1H	SETPOWER(Set power related setting)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	0	0	1	B1
1st parameter	1	1	↑	-	VBIAS_EN	VSN_EN	VSP_EN	VGL_EN	VGH_EN	LVGL_EN	VDDDN_HZ	STB	-
2nd parameter	1	1	↑	-	-	-	-	-	-	-	-	DSTB	-
3rd parameter	1	1	↑	-	-	FS1[2:0]			-	AP[2:0]			-
4th parameter	1	1	↑	-	-	-	-	-	BT[3:0]				-
5th parameter	1	1	↑	-	DT[1:0]		-	-	DCDIV[3:0]				-
6th parameter	1	1	↑	-	-	-	-	BTP[4:0]					-
7th parameter	1	1	↑	-	-	-	-	BTN[4:0]					-
8th parameter	1	1	↑	-	VRHP[7:0]								-
9th parameter	1	1	↑	-	VRHN[7:0]								-
10th parameter	1	1	↑	-	-	-	VRMP[5:0]						-
11th parameter	1	1	↑	-	-	-	VRMN[5:0]						-
12th parameter	1	1	↑	-	-	-	DD_TU	VPNL_EN	-	VBS[2:0]			-
13th parameter	1	1	↑	-	-	DC86_DIV[3:0]				XDK1	XDK0	AUTO_XDK	-
14th parameter	1	1	↑	-	-	DTPS[2:0]			-	DTNS[2:0]			-
15th parameter	1	1	↑	-	A_DC[1:0]		A_DTP[2:0]			A_DTN[2:0]			-
16th parameter	1	1	↑	-	B_DC[1:0]		B_DTP[2:0]			B_DTN[2:0]			-
17th parameter	1	1	↑	-	C_DC[1:0]		C_DTP[2:0]			C_DTN[2:0]			-
18th parameter	1	1	↑	-	D_DC[1:0]		D_DTP[2:0]			D_DTN[2:0]			-
19th parameter	1	1	↑	-	E_DC[1:0]		E_DTP[2:0]			E_DTN[2:0]			-

Description

This command is used to set related setting of power.

DSTB: When DSTB = "1", the HX8369-A02 into the deep_standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed.

1. Exit the Standby mode (DSTB = "0")

In the deep standby mode, the GRAM data and register content may be lost. For preventing this, they have to reset again after the deep standby mode cancel.

STB: When SLP = "1", the HX8369-A02 enters the standby mode, where all display operation stops, suspend all the internal operations. But the internal R-C oscillator stop or not is determined by OSC_EN bit. To minimize the standby power, please set OSC_EN to 0. During the standby mode, only the following process can be executed.

a. Exit the Standby (Sleep) mode (SLP = "0")
b. Enable or disable the oscillation
c. Software reset

VSP_EN: ON/OFF the operation of VSP circuit.

VSP_EN	Operation of VSP DC/DC circuit
0	OFF
1	ON

VSN_EN: ON/OFF the operation of VSN circuit.

VSN_EN	Operation of VSN DC/DC circuit
0	OFF
1	ON

VGH_EN: ON/OFF the operation of VGH charge bump circuit.

VGH_EN	Operation of VGH charge bump circuit
0	OFF
1	ON

VGL_EN	Operation of VGL charge bump circuit
0	OFF
1	ON

LVGL_EN : ON/OFF the operation of LVGL charge bump circuit.

LVGL_EN	Operation of LVGL charge bump circuit
0	OFF
1	ON

BT3	BT2	BT1	BT0	VGH	VGL
0	0	0	0	2*(VSP-VSN)	VDDDN-1*(VSP-VSN)
0	0	0	1	2*(VSP-VSN)	-1*(VSP-VSN)
0	0	1	0	2*(VSP-VSN)	VDD3-1*(VSP-VSN)
0	0	1	1	(VSP-VSN)+(VDD3-VSN)	VDDDN-1*(VSP-VSN)
0	1	0	0	(VSP-VSN)+(VDD3-VSN)	-1*(VSP-VSN)
0	1	0	1	(VSP-VSN)+(VDD3-VSN)	VDD3-1*(VSP-VSN)
0	1	1	0	(VSP-VSN)+(VSP-VSSD)	VDDDN-1*(VSP-VSN)
0	1	1	1	(VSP-VSN)+(VSP-VSSD)	-1*(VSP-VSN)
1	0	0	0	(VSP-VSN)+(VSP-VSSD)	VDD3-1*(VSP-VSN)
1	0	0	1	(VDD3-VSN)+(VSP-VSSD)	VDDDN-1*(VSP-VSN)
1	0	1	0	(VDD3-VSN)+(VSP-VSSD)	-1*(VSP-VSN)
1	0	1	1	(VDD3-VSN)+(VSP-VSSD)	VDD3-1*(VSP-VSN)
1	1	0	0	(VSP-VSN)	VDDDN-1*(VSP-VSN)
1	1	0	1	(VSP-VSN)	-1*(VSP-VSN)
1	1	1	0	(VSP-VSN)	VDD3-1*(VSP-VSN)
1	1	1	1	2*(VSP-VSSD)	-2*(VSP-VSSD)

FS1[2:0]: Set the operating frequency of the step-up circuit for VGH and VGL voltage generation.

FS12	FS11	FS10	Operation Frequency of Step-up Circuit
0	0	0	Inhibit
0	0	1	Fosc/64
0	1	0	Fosc/128
0	1	1	Fosc/256
1	0	0	Fosc/512
1	0	1	Fosc/1024
1	1	0	Fosc/2048
1	1	1	Fosc/4096

VDDDN_HZ: Choose external or internal VDDDN power.

VDDDN_HZ=0, VDDDN= -2.5V.
VDDDN_HZ=1, VDDDN output HZ. (For external VDDDN.)

DCDIV[3:0]: Set the normal operate frequency of DC/DC converter circuit during normal mode.
For PFM circuit: Set the operate frequency of DC/DC converter circuit for PFM design.
(PCCS[1:0]=00, PCCS[1:0]=01, PCCS[1:0]=10)

DCDIV3	DCDIV2	DCDIV1	DCDIV0	Normal operate frequency of DC/DC converter
0	0	0	0	Fosc / 1
0	0	0	1	Fosc / 2
0	0	1	0	Fosc / 3
0	0	1	1	Fosc / 4
0	1	0	0	Fosc / 5
0	1	0	1	Fosc / 6
0	1	1	0	Fosc / 7
0	1	1	1	Fosc / 8
1	0	0	0	Fosc / 1
1	0	0	1	Fosc / 2
1	0	1	0	Fosc / 3
1	0	1	1	Fosc / 4
1	1	0	0	Fosc / 5
1	1	0	1	Fosc / 6
1	1	1	0	Fosc / 7

1	1	1	1	Fosc / 8

DT[1:0]: Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence on (ms)
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

DTPS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).
1 duty cycle = 1 M clock

DTPS2	DTPS1	DTPS0	soft start operating duty cycle of DC/DC circuit circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTNS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).
1 duty cycle = 1 M clock

DTNS2	DTNS1	DTNS0	soft start operating duty cycle of DC/DC circuit circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

BTP[4:0]: Switch the output factor for DC/DC circuit for VSP voltage generation. The LCD drive voltage level VSP can be selected according to the characteristic of liquid crystal which panel used.

BTP4	BTP3	BTP2	BTP1	BTP0	VSP
0	0	0	0	0	3.01
0	0	0	0	1	3.15
0	0	0	1	0	3.29
0	0	0	1	1	3.46
0	0	1	0	0	3.60
0	0	1	0	1	3.74
0	0	1	1	0	3.91
0	0	1	1	1	4.05
0	1	0	0	0	4.19
0	1	0	0	1	4.36
0	1	0	1	0	4.50
0	1	0	1	1	4.64
0	1	1	0	0	4.81
0	1	1	0	1	4.95
0	1	1	1	0	5.09
0	1	1	1	1	5.26
1	0	0	0	0	5.40
1	0	0	0	1	5.54
1	0	0	1	0	5.71

1	0	0	1	1	Inhibit
. . . . .					Inhibit
1	1	1	1	1	Inhibit

BTN[4:0]: Switch the output factor of DC/DC circuit for VSN voltage generation. The LCD drive voltage level VSN can be selected according to the characteristic of liquid crystal which panel used.

While using PFM type-C or HX5186-A mode (PCCS1-0 = 10, PCCS1-0 = 11), VSN is followed the BTP[4:0] setting.
PFM mode type-C : VSN = -VSP + 0.6V
Using HX5186-A charge Pump mode : VSN = -VSP

AP[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop (inhibit)
0	0	1	0.5μA
0	1	0	1μA
0	1	1	1.5μA
1	0	0	2μA
1	0	1	2.5μA
1	1	0	3μA
1	1	1	3.5μA

VRHP[7:0]: VSPR regulator output control setting for source data output driving.

VRHP[7:0]								VSPR
0	0	0	0	0	0	0	0	3.488
0	0	0	0	0	0	0	1	3.516
0	0	0	0	0	0	1	0	3.544
0	0	0	0	0	0	1	1	3.572
0	0	0	0	0	1	0	0	3.600
0	0	0	0	0	1	0	1	3.628
0	0	0	0	0	1	1	0	3.656
0	0	0	0	0	1	1	1	3.684
0	0	0	0	1	0	0	0	3.713
0	0	0	0	1	0	0	1	3.741
0	0	0	0	1	0	1	0	3.769
0	0	0	0	1	0	1	1	3.797
0	0	0	0	1	1	0	0	3.825
0	0	0	0	1	1	0	1	3.853
0	0	0	0	1	1	1	0	3.881
0	0	0	0	1	1	1	1	3.909
0	0	0	1	0	0	0	0	3.938
0	0	0	1	0	0	0	1	3.966
0	0	0	1	0	0	1	0	3.994
0	0	0	1	0	0	1	1	4.022
0	0	0	1	0	1	0	0	4.050
0	0	0	1	0	1	0	1	4.078
0	0	0	1	0	1	1	0	4.106
0	0	0	1	0	1	1	1	4.134
0	0	0	1	1	0	0	0	4.163
0	0	0	1	1	0	0	1	4.191
0	0	0	1	1	0	1	0	4.219
0	0	0	1	1	0	1	1	4.247
0	0	0	1	1	1	0	0	4.275
0	0	0	1	1	1	0	1	4.303
0	0	0	1	1	1	1	0	4.331
0	0	0	1	1	1	1	1	4.359
0	0	1	0	0	0	0	0	4.388

0	0	1	0	0	0	0	1	4.416
0	0	1	0	0	0	1	0	4.444
0	0	1	0	0	0	1	1	4.472
0	0	1	0	0	1	0	0	4.500
0	0	1	0	0	1	0	1	4.528
0	0	1	0	0	1	1	0	4.556
0	0	1	0	0	1	1	1	4.584
0	0	1	0	1	0	0	0	4.613
0	0	1	0	1	0	0	1	4.641
0	0	1	0	1	0	1	0	4.669
0	0	1	0	1	0	1	1	4.697
0	0	1	0	1	1	0	0	4.725
0	0	1	0	1	1	0	1	4.753
0	0	1	0	1	1	1	0	4.781
0	0	1	0	1	1	1	1	4.809
0	0	1	1	0	0	0	0	4.838
0	0	1	1	0	0	0	1	4.866
0	0	1	1	0	0	1	0	4.894
0	0	1	1	0	0	1	1	4.922
0	0	1	1	0	1	0	0	4.950
0	0	1	1	0	1	0	1	4.978
0	0	1	1	0	1	1	0	5.006
0	0	1	1	0	1	1	1	5.034
0	0	1	1	1	0	0	0	5.063
0	0	1	1	1	0	0	1	5.091
0	0	1	1	1	0	1	0	5.119
00111011 ~ 01111110								Inhibit
0	1	1	1	1	1	1	1	VSP
10000000 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	HZ

VRHN[7:0]: VSNR regulator output control setting for source data output driving.

VRHN[7:0]								VSNR
0	0	0	0	0	0	0	0	-3.263
0	0	0	0	0	0	0	1	-3.291
0	0	0	0	0	0	1	0	-3.319
0	0	0	0	0	0	1	1	-3.347
0	0	0	0	0	1	0	0	-3.375
0	0	0	0	0	1	0	1	-3.403
0	0	0	0	0	1	1	0	-3.431
0	0	0	0	0	1	1	1	-3.459
0	0	0	0	1	0	0	0	-3.488
0	0	0	0	1	0	0	1	-3.516
0	0	0	0	1	0	1	0	-3.544
0	0	0	0	1	0	1	1	-3.572
0	0	0	0	1	1	0	0	-3.600
0	0	0	0	1	1	0	1	-3.628
0	0	0	0	1	1	1	0	-3.656
0	0	0	0	1	1	1	1	-3.684
0	0	0	1	0	0	0	0	-3.713
0	0	0	1	0	0	0	1	-3.741
0	0	0	1	0	0	1	0	-3.769
0	0	0	1	0	0	1	1	-3.797
0	0	0	1	0	1	0	0	-3.825
0	0	0	1	0	1	0	1	-3.853
0	0	0	1	0	1	1	0	-3.881
0	0	0	1	0	1	1	1	-3.909
0	0	0	1	1	0	0	0	-3.938
0	0	0	1	1	0	0	1	-3.966
0	0	0	1	1	0	1	0	-3.994
0	0	0	1	1	0	1	1	-4.022
0	0	0	1	1	1	0	0	-4.050
0	0	0	1	1	1	0	1	-4.078
0	0	0	1	1	1	1	0	-4.106

0	0	0	1	1	1	1	1	-4.134
0	0	1	0	0	0	0	0	-4.163
0	0	1	0	0	0	0	1	-4.191
0	0	1	0	0	0	1	0	-4.219
0	0	1	0	0	0	1	1	-4.247
0	0	1	0	0	1	0	0	-4.275
0	0	1	0	0	1	0	1	-4.303
0	0	1	0	0	1	1	0	-4.331
0	0	1	0	0	1	1	1	-4.359
0	0	1	0	1	0	0	0	-4.388
0	0	1	0	1	0	0	1	-4.416
0	0	1	0	1	0	1	0	-4.444
0	0	1	0	1	0	1	1	-4.472
0	0	1	0	1	1	0	0	-4.500
0	0	1	0	1	1	0	1	-4.528
0	0	1	0	1	1	1	0	-4.556
0	0	1	0	1	1	1	1	-4.584
0	0	1	1	0	0	0	0	-4.613
0	0	1	1	0	0	0	1	-4.641
0	0	1	1	0	0	1	0	-4.669
0	0	1	1	0	0	1	1	-4.697
0	0	1	1	0	1	0	0	-4.725
0	0	1	1	0	1	0	1	-4.753
0	0	1	1	0	1	1	0	-4.781
0	0	1	1	0	1	1	1	-4.809
0	0	1	1	1	0	0	0	-4.838
0	0	1	1	1	0	0	1	-4.866
0	0	1	1	1	0	1	0	-4.894
0	0	1	1	1	0	1	1	-4.922
0	0	1	1	1	1	0	0	-4.950
0	0	1	1	1	1	0	1	-4.978
0	0	1	1	1	1	1	0	-5.006
0	0	1	1	1	1	1	1	-5.034
0	1	0	0	0	0	0	0	-5.063
0	1	0	0	0	0	0	1	-5.091
0	1	0	0	0	0	1	0	-5.119
01000011 ~ 01111110								Inhibit
0	1	1	1	1	1	1	1	VSN
10000000 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	HZ

VRMP[5:0]: The positive polarity gamma amplitude voltage setting (VSPR-VGSP).

VRMP[5:0]						VSPR-VGSP
0	0	0	0	0	0	2.588
0	0	0	0	0	1	2.644
0	0	0	0	1	0	2.700
0	0	0	0	1	1	2.756
0	0	0	1	0	0	2.813
0	0	0	1	0	1	2.869
0	0	0	1	1	0	2.925
0	0	0	1	1	1	2.981
0	0	1	0	0	0	3.038
0	0	1	0	0	1	3.094
0	0	1	0	1	0	3.150
0	0	1	0	1	1	3.206
0	0	1	1	0	0	3.263
0	0	1	1	0	1	3.319
0	0	1	1	1	0	3.375
0	0	1	1	1	1	3.431
0	1	0	0	0	0	3.488
0	1	0	0	0	1	3.544
0	1	0	0	1	0	3.600
0	1	0	0	1	1	3.656
0	1	0	1	0	0	3.713
0	1	0	1	0	1	3.769

0	1	0	1	1	0	3.825
0	1	0	1	1	1	3.881
0	1	1	0	0	0	3.938
0	1	1	0	0	1	3.994
0	1	1	0	1	0	4.050
0	1	1	0	1	1	4.106
0	1	1	1	0	0	4.163
0	1	1	1	0	1	4.219
0	1	1	1	1	0	4.275
0	1	1	1	1	1	4.331
1	0	0	0	0	0	4.388
1	0	0	0	0	1	4.444
1	0	0	0	1	0	4.500
1	0	0	0	1	1	4.556
1	0	0	1	0	0	4.613
1	0	0	1	0	1	4.669
1	0	0	1	1	0	4.725
1	0	0	1	1	1	4.781
1	0	1	0	0	0	4.838
1	0	1	0	0	1	4.894
1	0	1	0	1	0	4.950
1	0	1	0	1	1	5.006
1	0	1	1	0	0	5.063
1	0	1	1	0	1	5.119
1	0	1	1	1	0	Inhibit
			. . . . .			Inhibit
1	1	1	1	1	0	Inhibit
1	1	1	1	1	1	VSPR(VGSP=VSSA)

VRMN[5:0]: The negitive polarity gamma amplitude voltage setting (VSNR-VGSN).

VRMN[5:0]						VSNR-VGSN
0	0	0	0	0	0	-2.588
0	0	0	0	0	1	-2.644
0	0	0	0	1	0	-2.700
0	0	0	0	1	1	-2.756
0	0	0	1	0	0	-2.813
0	0	0	1	0	1	-2.869
0	0	0	1	1	0	-2.925
0	0	0	1	1	1	-2.981
0	0	1	0	0	0	-3.038
0	0	1	0	0	1	-3.094
0	0	1	0	1	0	-3.150
0	0	1	0	1	1	-3.206
0	0	1	1	0	0	-3.263
0	0	1	1	0	1	-3.319
0	0	1	1	1	0	-3.375
0	0	1	1	1	1	-3.431
0	1	0	0	0	0	-3.488
0	1	0	0	0	1	-3.544
0	1	0	0	1	0	-3.600
0	1	0	0	1	1	-3.656
0	1	0	1	0	0	-3.713
0	1	0	1	0	1	-3.769
0	1	0	1	1	0	-3.825
0	1	0	1	1	1	-3.881
0	1	1	0	0	0	-3.938
0	1	1	0	0	1	-3.994
0	1	1	0	1	0	-4.050
0	1	1	0	1	1	-4.106
0	1	1	1	0	0	-4.163
0	1	1	1	0	1	-4.219
0	1	1	1	1	0	-4.275
0	1	1	1	1	1	-4.331
1	0	0	0	0	0	-4.388
1	0	0	0	0	1	-4.444

1	0	0	0	1	0	-4.500
1	0	0	0	1	1	-4.556
1	0	0	1	0	0	-4.613
1	0	0	1	0	1	-4.669
1	0	0	1	1	0	-4.725
1	0	0	1	1	1	-4.781
1	0	1	0	0	0	-4.838
1	0	1	0	0	1	-4.894
1	0	1	0	1	0	-4.950
1	0	1	0	1	1	-5.006
1	0	1	1	0	0	-5.063
1	0	1	1	0	1	-5.119
1	0	1	1	1	0	Inhibit
. . . . .						Inhibit
1	1	1	1	1	0	Inhibit
1	1	1	1	1	1	VSNR(VGSN=VSSA)

VBS[2:0]: Set the VBIAS level.

VBS2	VBS1	VBS0	VBIAS
0	0	0	Inhibit
0	0	1	4.68
0	1	0	4.50
0	1	1	4.32
1	0	0	4.14
1	0	1	3.96
1	1	0	3.78
1	1	1	3.60

DC86_DIV[3:0]: Frequency for Charge Pump Mode (HX5186-A)

DC86_DIV[3:0]	Frequency - Charge Pump Mode (HX5186-A)
0000	Fosc/2
0001	Fosc/4
0010	Fosc/8
0011	Fosc/16
0100	Fosc/24
0101	Fosc/32
0110	Fosc/40
0111	Fosc/48
1000	Fosc/56
1001	Fosc/64
1010	Fosc/72
1011	Fosc/80
1100	Fosc/88
1101	Fosc/96
1110	Fosc/104
1111	Fosc/112

XDK[1:0]: Setting HX5186-A

XDK[1]	XDK[0]	HX5186-A or Internal-Charge Pump
0	0	X1.5 Pump
0	1	x2 Pump
1	0	X3 Pump
1	1	Inhibited

AUTO_XDK: Auto XDK function enable, when using HX5186-A.

Auto_XDK=1	Hx5186-A
VDD3 x 1.5 > VSPtarget	X1.5
VDD3 x 2 > VSPtarget	X2
VDD3 x 2 < VSPtarget	X3
Auto_XDK=0	Depend on XDK[2:0]

DD_TU: In-house function, and not open.

VPNL_EN: Enable VPNL function.

<table>
<tr><td></td><td></td></tr>
<tr><td>Restriction</td><td>SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default value</th><th>OTP value</th></tr>
<tr><td>Power On Sequence
S/W Reset
H/W Reset</td><td>VBIAS_EN=0, VSN_EN=0,
VSP_EN=0,
VGL_EN=0, VGH_EN=0, LVGL_EN=0,
VDDDN_HZ=0, STB=1, DSTB=0,
FS1[2:0]=011, AP[2:0]=100,
BT[3:0]=111, DT[1:0] =00,
DCDIV[3:0]=0000, BTP[4:0]=01110,
BTN[4:0]=01110, VRHP[7:0]=0x21h,
VRHN[7:0]=0x29h, VRMP[5:0]=0x19h,
VRMN[5:0]=0x19h,
DD_TU= 0, VPNL_EN=0,
VBS[2:0]=111, DC86_DIV[3:0]=0111,
XDK1=0, XDK0=1, AUTO_XDK=0,
DTPS[2:0]=000, DTNS[2:0]=001,
A_DC[1:0]=11, A_DTP[2:0]=100,
A_DTN[2:0]=110,
B_DC[1:0]=11, B_DTP[2:0]=100,
B_DTN[2:0]=110,
C_DC[1:0]=11, C_DTP[2:0]=100,
C_DTN[2:0]=110,
D_DC[1:0]=11, D_DTP[2:0]=100,
D_DTN[2:0]=110,
E_DC[1:0]=11, E_DTP[2:0]=100,
E_DTN[2:0]=110,</td><td>FS1[2:0], AP[2:0], BT[3:0],
DT[1:0], DCDIV[3:0],
BTP[4:0], BTN[4:0],
VRHP[7:0], VRHN[7:0],
VRMP[5:0], VRMN[5:0],
DD_TU, VPNL_EN,
VBS[2:0], DC86_DIV[3:0],
XDK1, XDK0, AUTO_XDK,
DTPS[2:0], DTNS[2:0],
A_DC[1:0], A_DTP[2:0],
A_DTN[2:0].
B_DC[1:0], B_DTP[2:0],
B_DTN[2:0],
C_DC[1:0], C_DTP[2:0],
C_DTN[2:0],
D_DC[1:0], D_DTP[2:0],
D_DTN[2:0],
E_DC[1:0], E_DTP[2:0],
E_DTN[2:0],</td></tr>
</table>
</td></tr>
</table>

6.2.56 SETDISP: Set display related register (B2h)

B2H	SETDISP(Set display related register)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	0	1	0	B2
1st parameter	1	1	↑	-	-	-	-	-	-	-	D[1:0]		
2nd parameter	1	1	↑	-	-	RES_SEL[2:0]			RM	DFR	DM[1:0]		
3rd parameter	1	1	↑	-	BP [7:0]								
4th parameter	1	1	↑		FP [7:0]								
5th parameter	1	1	↑	-	SAP[3:0]				-	-	-	-	
6th parameter	1	1	↑	-	GEN_ON[7:0]								
7th parameter	1	1	↑	-	GEN_OFF[7:0]								
8th parameter	1	1	↑	-	RTN[7:0]								
9th parameter	1	1	↑	-	-	-	-	-	TEI[3:0]				
10th parameter	1	1	↑	-	-	-	-	-	-	-	TEP[9:8]		
11th parameter	1	1	↑	-	TEP[7:0]								
12th parameter	1	1	↑	-	BP_PE[7:0]								
13th parameter	1	1	↑	-	FP_PE[7:0]								
14th parameter	1	1	↑	-	RTN_PE[7:0]								
15th parameter	1	1	↑	-	-	-	-	-	-	-	-	GON	

Description

This command is used to set display related register

D1–0:

D1	D0	Source Output	HX8369-A02 Internal Display Operations
0	0	VSSD	Halt
0	1	Inhibit	Inhibit
1	0	V255	Operate
1	1	Display	Operate

RES_SEL[2:0]: Resolution selection.

RES_SEL 2	RES_SEL 1	RES_SEL 0	Resolution
0	0	0	480RGBX864
0	0	1	480RGBX854
0	1	0	480RGBX800
0	1	1	480RGBX640
1	0	0	360 RGBX640
1	0	1	480RGBX720
1	1	0	Setting disable
1	1	1	Setting disable

RM The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation.
RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting.

RM	Interface for RAM Access
0	DBI Interface (CPU)
1	DPI Interface (RGB)

DM[1:0] The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal (VSYNC+HSYNC).
Note that switching between VSYNC and DPI operation is prohibited.

DM 1	DM 0	Display Mode
0	0	Internal oscillation clock
0	1	DPI signal (VSYNC+HSYNC)
1	0	VSYNC signal
1	1	RGB data bypass GRAM mode

FP[7:0]: Specify the amount of scan line for front porch (FP).
BP[7:0] : Specify the amount of scan line for back porch(BP).
FP_PE[7:0]: Specify the amount of scan line for front porch (FP) on partial idle mode.
BP_PE[7:0] : Specify the amount of scan line for back porch(BP) on partial idle mode.

FP[7:0] / FP_PE[7:0] BP[7:0] / BP_PE[7:0]	Number of FP Line	Number of BP Line
8h'00	Inhibited	
8h'01	3 lines	
8h'02	4 lines	
8h'03	5 lines	
8h'04	6 lines	
8h'05	7 lines	
• • •	• • •	
8h'FB	253 lines	
8h'FC	254 lines	
8h'FD	255 lines	
8h'FE	256 lines	
8h'FF	257 lines	

SAP3	SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
0	0	0	0	0.5u
0	0	0	1	1u
0	0	1	0	1.5u
0	0	1	1	2u
0	1	0	0	2.5u
0	1	0	1	3u
0	1	1	0	3.5u
0	1	1	1	4u
• • • • • • • • • • • • • • • •				
1	1	1	1	8u

GEN_ON[7:0]: Gamma OP turned on timing and in-house function not open.

GEN_OFF[7:0]: Gamma OP turned off timing and in-house function not open.

RTN[7:0]: A cycle time of line width, in-house function not open.
RTN_PE[7:0]: A cycle time of line width on partial idle mode, in-house function not open.

RTN[7:0]/ RTN_PE[7:0]	Clock per Line
8h'00	275 clocks
8h'01	(275 + 1x2) 277 clocks
8h'02	(275 + 2x2) 279 clocks
8h'03	(275 + 3x2) 281 clocks
• • •	• • •
8'hFD	(275 + 253x2) 781 clocks
8'hFE	(275 + 254x2) 783 clocks
8'hFF	(275 + 255x2) 785 clocks

TEI[3:0]: Sets the output interval of TE signal according to the display data rewrite cycle and data transfer rate.

TEI3	TEI2	TEI1	TEI0	Output Interval
0	0	0	0	1 frame
0	0	0	1	2 frames
0	0	1	0	3 frames
• • • • • • •				• •
1	1	1	0	15 frames
1	1	1	1	16 frames

DFR: The bit is used in the Frame Memory access and Display operation. In-house function and not open.

TEP[9:0]: Sets the output position of frame cycle signal. TE can be used as the trigger signal for frame synchronous write operation.
Make sure the setting restriction 9'h000 ≤ TEP[9:0] ≤ BP+Number of Line +FP.

TEP[9:0]	Output position
10'h000	0th line
10'h001	1st line
10'h002	2nd line
10'h003	3rd line
• • •	• • •
10'h35D	861th line
10'h35E	862th line
10'h35F	863th line

GON: Controlling the GIP signals On/Off register.
GON =1, the GIP signals are On for normal operation.
GON =0, the GIP signals are OFF and set as GND.

Restrictions: SETEXTC turn on to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	D[1:0]=00, RES_SEL[2:0]=001, RM=0, DFR=0, DM[1:0]=00 BP[7:0]=0x03h, FP[7:0]=0x03h, SAP[3:0]=0111, GEN_ON=0x00h, GEN_OFF=0xFFh, RTN[7:0]=0x00h, TEI[3:0] =0000,TEP[9:0] =0x000h, BP_PE[7:0]=0x03h, FP_PE[7:0]=0x03h, RTN_PE[7:0]=0x00h, GON=1	RES_SEL[2:0], RM, DFR, DM[1:0] BP[7:0], FP[7:0], SAP[3:0], GEN_ON, GEN_OFF, RTN[7:0], TEI[3:0], TEP[9:0], BP_PE[7:0], FP_PE[7:0], RTN_PE[7:0]

6.2.57 SETRGBIF: Set RGB interface related register (B3h)

B3H	SETRGBIF(Set RGB interface related register)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	0	1	1	B3
1st parameter	1	1	↑	-	-	-	-	-	DPL	HSPL	VSPL	EPL	-

Description

This command is used to set RGB interface related register.
EPL: Specify the polarity of DE pin in RGB interface mode.

EPL	DE pin	Display
0	0	Enable
0	1	Disable
1	0	Disable
1	1	Enable

VSPL: The polarity of VS pin. When VSPL=0, the VS pin is Low active. When VSPL=1, the VS pin is High active.
HSPL: The polarity of HS pin. When HSPL=0, the HS pin is Low active. When HSPL=1, the HS pin is High active.
DPL: The polarity of PCLK pin. When DPL=0, the data is read on the rising edge of PCLK signal. When DPL=1, the data is read on the falling edge of PCLK signal.

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	DPL=0,HSPL=0,VSPL=0,EPL=1	DPL,HSPL,VSPL,EPL

6.2.58 SETCYC: Set display waveform cycle (B4h)

B4H	SETCYC(Set display waveform cycles)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	0	0	1	0	0	B4
1st parameter	1	1	↑	-	-	-	-	-	NW_PE[1:0]		NW[1:0]		-
2nd parameter	1	1	↑	-	SON[7:0]								-
3rd parameter	1	1	↑	-	SOFF[7:0]								-
4th parameter	1	1	↑	-	EQS[7:0]								-
5th parameter	1	1	↑	-	EQON[7:0]								-

Description

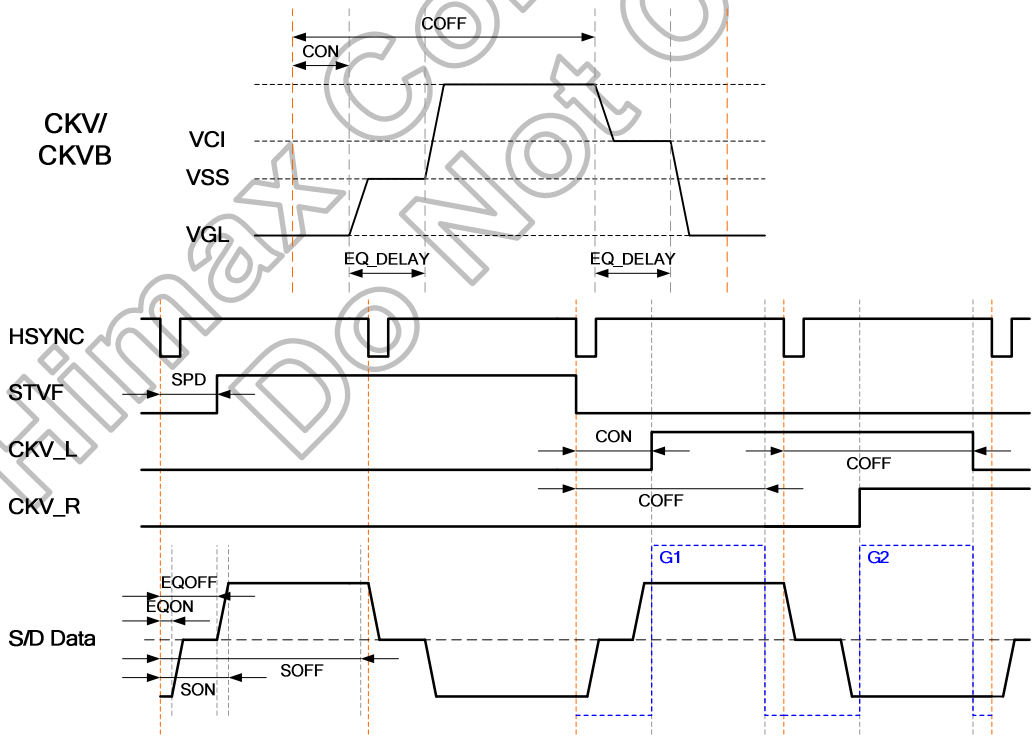
This command is used to get setting of display waveform cycles.

NW[1:0]: Inversion type setting.

NW1	NW0	Inversion type
0	0	Column inversion
0	1	1-dot inversion
1	0	2-dot inversion
1	1	Zig-zag inversion

NW_PE[1:0]: Inversion type setting on partial idle mode.

NW_PE1	NW_PE0	Inversion type
0	0	Column inversion
0	1	1-dot inversion
1	0	2-dot inversion
1	1	Zig-zag inversion



SOFF > SON > EQOFF > EQON
SOFF > COFF

SON[7:0]: Specify the valid source output start time.

SON [7:0]								Source output start time
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 OSC clock cycle
0	0	0	0	0	0	1	0	2 OSC clock cycle
0	0	0	0	0	0	1	1	3 OSC clock cycle
0	0	0	0	0	1	0	0	4 OSC clock cycle

				• • • • •				• • • • •
0	0	0	0	1	1	1	1	15 OSC clock cycle
				• • • • •				• • • • •
1	1	1	1	1	0	1	0	250 OSC clock cycle
1	1	1	1	1	0	1	1	251 OSC clock cycle
1	1	1	1	1	1	0	0	252 OSC clock cycle
1	1	1	1	1	1	0	1	253 OSC clock cycle
1	1	1	1	1	1	1	0	254 OSC clock cycle
1	1	1	1	1	1	1	1	255 OSC clock cycle

SOFF[7:0]: Specify the valid source output end time.

SOFF [7:0]								Source output end time
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 OSC clock cycle
0	0	0	0	0	0	1	0	2 OSC clock cycle
0	0	0	0	0	0	1	1	3 OSC clock cycle
0	0	0	0	0	1	0	0	4 OSC clock cycle
				• • • • •				• • • • •
1	0	0	0	0	0	1	0	130 OSC clock cycle
				• • • • •				• • • • •
1	1	1	1	1	0	1	0	250 OSC clock cycle
1	1	1	1	1	0	1	1	251 OSC clock cycle
1	1	1	1	1	1	0	0	252 OSC clock cycle
1	1	1	1	1	1	0	1	253 OSC clock cycle
1	1	1	1	1	1	1	0	254 OSC clock cycle
1	1	1	1	1	1	1	1	255 OSC clock cycle

EQON[7:0]: Specify the valid Equalize output start time.
(Please note that the EQON[7:0] ≤ EQS[7:0]-1)

EQON [7:0]								Gate output start time
0	0	0	0	0	0	0	0	Inhibit
0	0	0	0	0	0	0	1	1 OSC clock cycle
0	0	0	0	0	0	1	0	2 OSC clock cycle
0	0	0	0	0	0	1	1	3 OSC clock cycle
0	0	0	0	0	1	0	0	4 OSC clock cycle
				• • • • •				• • • • •
0	0	0	0	1	1	0	0	12 OSC clock cycle
				• • • • •				• • • • •
1	1	1	1	1	0	1	0	250 OSC clock cycle
1	1	1	1	1	0	1	1	251 OSC clock cycle
1	1	1	1	1	1	0	0	252 OSC clock cycle
1	1	1	1	1	1	0	1	253 OSC clock cycle
1	1	1	1	1	1	1	0	254 OSC clock cycle
1	1	1	1	1	1	1	1	255 OSC clock cycle

EQS[7:0]: Specify the Equalize time of source output. (Please note that the EQS[7:0] ≤ SON-1).

EQS [7:0]								Equalize time of source output
0	0	0	0	0	0	0	0	Equalize function off
0	0	0	0	0	0	0	1	1 OSC clock cycle
0	0	0	0	0	0	1	0	2 OSC clock cycle
0	0	0	0	0	0	1	1	3 OSC clock cycle
0	0	0	0	0	1	0	0	4 OSC clock cycle
0	0	0	0	0	1	0	1	5 OSC clock cycle
0	0	0	0	0	1	1	0	6 OSC clock cycle
				• • • • •				• • • • •
1	1	1	1	1	0	1	0	250 OSC clock cycle
1	1	1	1	1	0	1	1	251 OSC clock cycle

	1	1	1	1	1	1	0	0	252 OSC clock cycle
	1	1	1	1	1	1	0	1	253 OSC clock cycle
	1	1	1	1	1	1	1	0	254 OSC clock cycle
	1	1	1	1	1	1	1	1	255 OSC clock cycle

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	NW_PE[1:0]=00,NW[1:0]=00, SON[7:0]=0x0Fh,SOFF[7:0]=0x82h, EQS[7:0]=0x0Ch, EQON[7:0]=0x03h	NW_PE[1:0], NW[1:0], SON[7:0], SOFF[7:0], EQS[7:0], EQON[7:0]

6.2.59 SETVCOM: Set VCOM voltage (B6h)

B6 H	SETVCOM (Set VCOM Voltage)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	0	1	1	0	B6
1st parameter	1	1	↑	-	VCMC_F[7:0]								-
2nd parameter	1	1	↑	-	VCMC_B[7:0]								-

Description

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage.

VCMC_F[7:0]: DC VCOM voltage setting for forward scan.
VCMC_B[7:0]: DC VCOM voltage setting for backward scan.

VCMC_F[7:0] / VCMC_B[7:0]								VCOM (V)
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	-2
0	0	0	0	0	0	0	1	-1.984
0	0	0	0	0	0	1	0	-1.968
0	0	0	0	0	0	1	1	-1.952
0	0	0	0	0	1	0	0	-1.936
0	0	0	0	0	1	0	1	-1.92
0	0	0	0	0	1	1	0	-1.904
0	0	0	0	0	1	1	1	-1.888
0	0	0	0	1	0	0	0	-1.872
0	0	0	0	1	0	0	1	-1.856
0	0	0	0	1	0	1	0	-1.84
0	0	0	0	1	0	1	1	-1.824
0	0	0	0	1	1	0	0	-1.808
0	0	0	0	1	1	0	1	-1.792
0	0	0	0	1	1	1	0	-1.776
0	0	0	0	1	1	1	1	-1.76
0	0	0	1	0	0	0	0	-1.744
0	0	0	1	0	0	0	1	-1.728
0	0	0	1	0	0	1	0	-1.712
0	0	0	1	0	0	1	1	-1.696
0	0	0	1	0	1	0	0	-1.68
0	0	0	1	0	1	0	1	-1.664
0	0	0	1	0	1	1	0	-1.648
0	0	0	1	0	1	1	1	-1.632
0	0	0	1	1	0	0	0	-1.616
0	0	0	1	1	0	0	1	-1.6
0	0	0	1	1	0	1	0	-1.584
0	0	0	1	1	0	1	1	-1.568
0	0	0	1	1	1	0	0	-1.552
0	0	0	1	1	1	0	1	-1.536
0	0	0	1	1	1	1	0	-1.52
0	0	0	1	1	1	1	1	-1.504
0	0	1	0	0	0	0	0	-1.488
0	0	1	0	0	0	0	1	-1.472
0	0	1	0	0	0	1	0	-1.456
0	0	1	0	0	0	1	1	-1.44
0	0	1	0	0	1	0	0	-1.424
0	0	1	0	0	1	0	1	-1.408
0	0	1	0	0	1	1	0	-1.392
0	0	1	0	0	1	1	1	-1.376
0	0	1	0	1	0	0	0	-1.36
0	0	1	0	1	0	0	1	-1.344
0	0	1	0	1	0	1	0	-1.328
0	0	1	0	1	0	1	1	-1.312
0	0	1	0	1	1	0	0	-1.296

		0	0	1	0	1	1	0	1	-1.28
		0	0	1	0	1	1	1	0	-1.264
		0	0	1	0	1	1	1	1	-1.248
		0	0	1	1	0	0	0	0	-1.232
		0	0	1	1	0	0	0	1	-1.216
		0	0	1	1	0	0	1	0	-1.2
		0	0	1	1	0	0	1	1	-1.184
		0	0	1	1	0	1	0	0	-1.168
		0	0	1	1	0	1	0	1	-1.152
		0	0	1	1	0	1	1	0	-1.136
		0	0	1	1	0	1	1	1	-1.12
		0	0	1	1	1	0	0	0	-1.104
		0	0	1	1	1	0	0	1	-1.088
		0	0	1	1	1	0	1	0	-1.072
		0	0	1	1	1	0	1	1	-1.056
		0	0	1	1	1	1	0	0	-1.04
		0	0	1	1	1	1	0	1	-1.024
		0	0	1	1	1	1	1	0	-1.008
		0	0	1	1	1	1	1	1	-0.992
		0	1	0	0	0	0	0	0	-0.976
		0	1	0	0	0	0	0	1	-0.96
		0	1	0	0	0	0	1	0	-0.944
		0	1	0	0	0	0	1	1	-0.928
		0	1	0	0	0	1	0	0	-0.912
		0	1	0	0	0	1	0	1	-0.896
		0	1	0	0	0	1	1	0	-0.88
		0	1	0	0	0	1	1	1	-0.864
		0	1	0	0	1	0	0	0	-0.848
		0	1	0	0	1	0	0	1	-0.832
		0	1	0	0	1	0	1	0	-0.816
		0	1	0	0	1	0	1	1	-0.8
		0	1	0	0	1	1	0	0	-0.784
		0	1	0	0	1	1	0	1	-0.768
		0	1	0	0	1	1	1	0	-0.752
		0	1	0	0	1	1	1	1	-0.736
		0	1	0	1	0	0	0	0	-0.72
		0	1	0	1	0	0	0	1	-0.704
		0	1	0	1	0	0	1	0	-0.688
		0	1	0	1	0	0	1	1	-0.672
		0	1	0	1	0	1	0	0	-0.656
		0	1	0	1	0	1	0	1	-0.64
		0	1	0	1	0	1	1	0	-0.624
		0	1	0	1	0	1	1	1	-0.608
		0	1	0	1	1	0	0	0	-0.592
		0	1	0	1	1	0	0	1	-0.576
		0	1	0	1	1	0	1	0	-0.56
		0	1	0	1	1	0	1	1	-0.544
		0	1	0	1	1	1	0	0	-0.528
		0	1	0	1	1	1	0	1	-0.512
		0	1	0	1	1	1	1	0	-0.496
		0	1	0	1	1	1	1	1	-0.48
		0	1	1	0	0	0	0	0	-0.464
		0	1	1	0	0	0	0	1	-0.448
		0	1	1	0	0	0	1	0	-0.432
		0	1	1	0	0	0	1	1	-0.416
		0	1	1	0	0	1	0	0	-0.4
		0	1	1	0	0	1	0	1	-0.384
		0	1	1	0	0	1	1	0	-0.368

0	1	1	0	0	1	1	1	-0.352
0	1	1	0	1	0	0	0	-0.336
0	1	1	0	1	0	0	1	-0.32
0	1	1	0	1	0	1	0	-0.304
0	1	1	0	1	0	1	1	-0.288
0	1	1	0	1	1	0	0	-0.272
0	1	1	0	1	1	0	1	-0.256
0	1	1	0	1	1	1	0	-0.24
0	1	1	0	1	1	1	1	-0.224
0	1	1	1	0	0	0	0	-0.208
0	1	1	1	0	0	0	1	-0.192
0	1	1	1	0	0	1	0	-0.176
0	1	1	1	0	0	1	1	-0.16
0	1	1	1	0	1	0	0	-0.144
0	1	1	1	0	1	0	1	-0.128
0	1	1	1	0	1	1	0	-0.112
0	1	1	1	0	1	1	1	-0.096
0	1	1	1	1	0	0	0	-0.08
0	1	1	1	1	0	0	1	-0.064
0	1	1	1	1	0	1	0	-0.048
0	1	1	1	1	0	1	1	-0.032
0	1	1	1	1	1	0	0	-0.016
01111101 ~ 01111101								Inhibit
0	1	1	1	1	1	1	0	VCOMR
0	1	1	1	1	1	1	1	VSSA
10000000 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	HZ

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	VCMC_F[7:0]=0x5Eh, VCMC_B[7:0]=0x5Eh	VCMC_F[7:0], VCMC_B[7:0]

6.2.60 SETEXTC: Set extension command (B9h)

B9H	SETEXTC (Set extended command set)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	1	0	0	1	B9
1st parameter	1	1	↑	-	EXTC1[7:0](FFh)								-
2nd parameter	1	1	↑	-	EXTC2[7:0](83h)								-
3rd parameter	1	1	↑	-	EXTC3[7:0](69h)								-

Description

This command is used to set extended command set access enable.

Extend cmd	Command description
Enable	After command (B0h), must write 3 parameters (ffh,83h,69h) by order
Disable(default)	After command(B0h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (ffh,83h,69h)

Restrictions

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	EXTC1[7:0]=0x00h, EXTC2[7:0]=0x00h, EXTC3[7:0]=0x00h,	N/A

6.2.61 SETMIPI: (BAh)

BAH	SETMIPI (Set extended command set)												
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	1	0	0	1	BA
1st parameter	1	1	↑	-	DPHYCMD0[7:0]								-
2nd parameter	1	1	↑	-	DPHYCMD1[7:0]								-
3rd parameter	1	1	↑	-	DPHYCMD2[7:0]								-
4th parameter	1	1	↑	-	DSICMD0[7:0]								-
5th parameter	1	1	↑	-	DSICMD1[7:0]								-
6th parameter	1	1	↑	-	DSICMD2[7:0]								-
7th parameter	1	1	↑	-	DSICMD3[7:0]								-
8th parameter	1	1	↑	-	DPHYOTP0[7:0]								-
9th parameter	1	1	↑	-	DPHYOTP1[7:0]								-
10th parameter	1	1	↑	-	DPHYOTP2[7:0]								-
11th parameter	1	1	↑	-	DSIOTP0[7:0]								-
12th parameter	1	1	↑	-	DSIOTP1[7:0]								-
13th parameter	1	1	↑	-	-	DSI_INI TRDY	-	-	-	-	-	-	-

Description

In-house function and not open.

Command Table

Register Name	Hardware Setting
DPHYCMD0[7: 0]=0x00h	Default setting is fixed.
DPHYCMD1[7: 0]=0xA0h	Default setting is fixed.
DPHYCMD2[7: 0]=0xC6h	Default setting is fixed.

Register Name	Hardware Setting
DSICMD0[7: 0]=0x00h	Default setting is fixed.
DSICMD1[7: 0]=0x0Ah	Default setting is fixed.
DSICMD2[7: 0]=0x00h	Default setting is fixed.
DSICMD3[7: 0]=0x10h	Default setting is fixed.

In-house function and not open.

OTP Table:

Register Name	DSI OTP setting
DPHYOTP0[7:0]	Default setting is fixed.
DPHYOTP1[7:0]	Default setting is fixed.
DPHYOTP2[7:0]	Default setting is fixed.

DSI data lane number setting

DSIOTP0[7:0] (00)NW0	Data Lane Number
0x10h	One Data Lane Mode
0x11h	Two Data Lane Mode

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	DPHYCMD0[7:0]=0x00h, DPHYCMD1[7:0]=0xA0h, DPHYCMD2[7:0]=0xC6h, DSICMD0[7:0]=0x00h, DSICMD1[7:0]=0x0Ah, DSICMD2[7:0]=0x00h, DSICMD3[7:0]=0x10h, DPHYOTP0[7:0]=0x30h,	DPHYOTP0[7:0] DPHYOTP1[7:0] DPHYOTP2[7:0] DSIOTP0[7:0] DSIOTP1[7:0]

		DPHYOTP1[7:0]=0x6Fh, DPHYOTP2[7:0]=0x02h, DSIOTP0[7:0]=0x10h, DSIOTP1[7:0]=0x18h, DSI_INITRDY=1		

6.2.62 SETOTP: Set OTP (BBh)

BBH	SETOTP(Set OTP Related Setting)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	0	1	1	1	0	1	1	BB
1st parameter	1	1	↑	-	OTP_MASK[7:0] (8'b0)								-
2nd parameter	1	1	↑	-	-	-	-	-	-	-	-	OTP_INDEX[8]	
3rd parameter	1	1	↑	-	OTP_INDEX[7:0]								-
4th parameter	1	1	↑	-	OTP_LOAD_ DISABLE	OTP_TEST	OTP_POR	OTP_PWE	OTP_PTM[1:0]		VPP_SEL	OTP_PROG	-
5th parameter	1	1	↑	-	OTP_DATA[7:0]								-

Description

This command is used to set OTP Related Setting.
OTP_MASK[7:0]: Bit programming mask, if 1, means this bit can't be programmed.
OTP_INDEX[8:0]: Set index of OTP table for programming.
OTP_PWE: OTP program write enable, if 1, means OTP is able to be programmed.
OTP_PROG: When set to 1, the register content of OTP index is programmed.
OTP_LOAD_DISABLE: Normally the internal registers are auto-loaded from OTP when the SLPOUT command is received. Nevertheless, if this bit is set to 1, it will disable the auto loading function when the SLPOUT command was received. In general, this bit is used when OTP is not yet programmed.
OTP_PTM[1:0]: Not open, internal use.
VPP_SEL: When written to 1, VPP voltage is fed to OTP
OTP_DATA[7:0]: Read back the OTP index data.

Restrictions

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	OTP_MASK[7:0]=0x00h, OTP_INDEX[8:0]=0x1FFh, OTP_LOAD_ DISABLE=0, OTP_TEST=0, OTP_POR=0, OTP_PWE=0, OTP_PTM[1:0]=00, VPP_SEL=0, OTP_PROG=0, OTP_DATA[7:0]=xxh	N/A

6.2.63 SETDGCLUT: Set DGC LUT (C1h)

C1H	SETDGCLUT (Set DGC LUT)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	0	0	1	C1
1st parameter	1	1	↑	-	-	-	-	-	-	-	DITH_OPT	DGC_EN	-
2nd parameter	1	1	↑	-	D1[7:0]								-
:	1	1	↑	-	Dn[7:0]								-
127th parameter	1	1	↑	-	D126[7:0]								-

Description

This command is used to set DGC LUT.
DITH_OPT: Not open, internal use.
DGC_EN: Enable the DGC function
D1[7:0] ~ D126[7:0]:

LUT	D7	D6	D5	D4	D3	D2	D1	D0	Default
1st	R009	R008	R007	R006	R005	R004	R003	R002	00h
2nd	R019	R018	R017	R016	R015	R014	R013	R012	08h
3rd	R029	R028	R027	R026	R025	R024	R023	R022	10h
:	:	:	:	:	:	:	:	:	:
32rd	R319	R318	R317	R316	R315	R314	R313	R312	F8h
33rd	R329	R328	R327	R326	R325	R324	R323	R322	FFh
34th	R001	R000	R011	R010	R021	R020	R031	R030	00h
35th	R041	R040	R051	R050	R061	R060	R071	R070	00h
:	:	:	:	:	:	:	:	:	:
41st	R281	R280	R291	R290	R301	R300	R311	R310	00h
42nd	R321	R320	0	0	0	0	0	0	00h
43rd	G009	G008	G007	G006	G005	G004	G003	G002	00h
44th	G019	G018	G017	G016	G015	G014	G013	G012	08h
45th	G029	G028	G027	G026	G025	G024	G023	G022	10h
:	:	:	:	:	:	:	:	:	:
74th	G319	G318	G317	G316	G315	G314	G313	G312	F8h
75th	G329	G328	G327	G326	G325	G324	G323	G322	FFh
76th	G001	G000	G011	G010	G021	G020	G031	G030	00h
77th	G041	G040	G051	G050	G061	G060	G071	G070	00h
:	:	:	:	:	:	:	:	:	:
83rd	G281	G280	G291	G290	G301	G300	G311	G310	00h
84th	G321	G320	0	0	0	0	0	0	00h
85th	B009	B008	B007	B006	B005	B004	B003	B002	00h
86th	B019	B018	B017	B016	B015	B014	B013	B012	08h
87th	B029	B028	B027	B026	B025	B024	B023	B022	10h
:	:	:	:	:	:	:	:	:	:
116th	B319	B318	B317	B316	B315	B314	B313	B312	F8h
117th	B329	B328	B327	B326	B325	B324	B323	B322	FFh
118th	B001	B000	B011	B010	B021	B020	B031	B030	00h
119th	B041	B040	B051	B050	B061	B060	B071	B070	00h
:	:	:	:	:	:	:	:	:	:
125th	B281	B280	B291	B290	B301	B300	B311	B310	00h
126th	B321	B320	0	0	0	0	0	0	00h

Write D1[7:0] (R 1st), D43[7:0] (G 1st) and D85[7:0] (B 1st), but Read is from D1[7:0], D2[7:0] and D3[7:0]

Restrictions: SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Idle Mode Off, Sleep Out	Yes
Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default	Status	Default value	OTP value	
	Power On Sequence S/W Reset H/W Reset	DITH_OPT DGC_EN D1[7:0]~D126[7:0]	DITH_OPT DGC_EN D1[7:0]~D126[7:0]	

6.2.64 SETID: Set ID (C3h)

C3H	SETID (Set ID)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	0	0	1	1	C3
1st parameter	1	1	↑	-	ID1[7:0]								-
2nd parameter	1	1	↑	-	0	ID2[6:0]							-
3rd parameter	1	1	↑	-	ID3[7:0]								-
Description	This command is used to set ID (RDAh, RDBh, RDCh) value.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	ID1[7:0]=0x00h, ID2[6:0]=0x00h, ID3[7:0]=0x00h,	ID1[7:0], ID2[6:0], ID3[7:0]

6.2.65 SETCABC: Set CABC Control (C9h)

C9H	SETCABC (Set CABC Control)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	1	0	0	1	C9
1st parameter	1	1	↑	-	-	-	EN_DIM_MIX	EN_COST_MEAN	EN_COST	EN_NLN_GAIN	EN_JUDGE	EN_TEMP	-
2nd parameter	1	1	↑	-	CABC_DD	SAVEPOWER[6:0]							-
3rd parameter	1	1	↑	-	MEAN_OFFSET[7:0]								-
4th parameter	1	1	↑	-	-	-	-	-	CABC_FLM[3:0]				-
5th parameter	1	1	↑	-	-	SEL_PWMCLK[2:0]			SEL_GAIN[1:0]		INVPULS	SEL_BLDUTY	-
6th parameter	1	1	↑	-	PWM_PERIOD[7:0]								-
7th parameter	1	1	↑	-	-	DIM_FRAME[6:0]							-
8th parameter	1	1	↑	-	CABC_STEP[7:0]								-
9th parameter	1	1	↑	-	CABC_CLKEN[7:0]								-

Description

This command is used to set CABC function.

INVPULS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

SEL_BLDUTY : The backlight PWM output duty on/off control when CABC operated.
'0', The backlight PWM output duty is 100%.
'1', The backlight PWM output duty is calculated from CABC operation.

SEL_PWMCLK[2:0] : Internal PWM_CLK divider for CABC clock.

SEL_PWMCLK[2:0]			Brightness Control Clock
0	0	0	PWM_CLK / 1
0	0	1	PWM_CLK / 2
0	1	0	PWM_CLK / 4
0	1	1	PWM_CLK / 8
1	0	0	PWM_CLK / 16
1	0	1	PWM_CLK / 32
1	1	0	PWM_CLK / 64
1	1	1	PWM_CLK / 128

SEL_GAIN[1:0]: CABC gain select. Internal use and not Open. Please set to "11".

PWM_PERIOD[7:0] : The backlight PWM output period setting.
Backlight PWM output period
= 1 / (PWM_CLK / clock divider (SEL_PWMCLK[2:0])) x (255x(PWM_PERIOD[7:0])).

SAVEPOWER[6:0] : Minimum CABC gain / maximum CABC duty output select.
To define the minimum gain or maximum duty of CABC block output.
If not used, please set to"0000000".

CABC_DD: Internal use and not open.

MEAN_OFFSET[7:0]: Internal use, not open.

CABC_FLM[3:0]: CABC dimming frame number for each step.

CABC_STEP[7:0]: Internal use and not open.

CABC_CLKEN[7:0]: Internal use and not open.

<table>
<tr><td></td><td>DIM_FRAME[6:0]: Manual brightness setting dimming period.

EN_DIM_MIX: Internal use and not open. Please set to”1”.

EN_COST_MAIN: Internal use and not open. Please set to”1”.

EN_COST: Internal use and not open. Please set to”1”.

EN_NLN_GAIN: Internal use and not open. Please set to”1”.

EN_JUDGE: Internal use and not open. Please set to”1”.

EN_TEMP: Internal use and not open. Please set to”0”.</td></tr>
<tr><td>Restrictions</td><td>SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default value</th><th>OTP value</th></tr>
<tr><td>Power On Sequence
S/W Reset
H/W Reset</td><td>EN_DIM_MIX =1,
EN_COST_MEAN =1,
EN_COST =1,
EN_NLN_GAIN =1,
EN_JUDGE =1,
EN_TEMP =0,
CABC_DD =0,
SAVEPOWER[6:0] =0x00h
MEAN_OFFSET[7:0] =0x00h
CABC_FLM[3:0] = 0001,
SEL_PWMCLK[2:0] =010,
SEL_GAIN[1:0] =11,
INVPULS =1,
SEL_BLDUTY =1,
PWM_PERIOD[7:0] =0x2Bh,
DIM_FRAME[6:0] =0x1Eh,
CABC_STEP[7:0] =0x1Eh,
CABC_CLKEBN[7:0] =0x00h</td><td>SEL_PWMCLK[2:0],
SEL_GAIN[1:0],
INVPULS,
SEL_BLDUTY,
PWM_PERIOD[7:0],
DIM_FRAME[6:0],
CABC_STEP[7:0],
CABC_CLKEBN[7:0]</td></tr>
</table>
</td></tr>
</table>

6.2.66 SETPANEL (CCh)

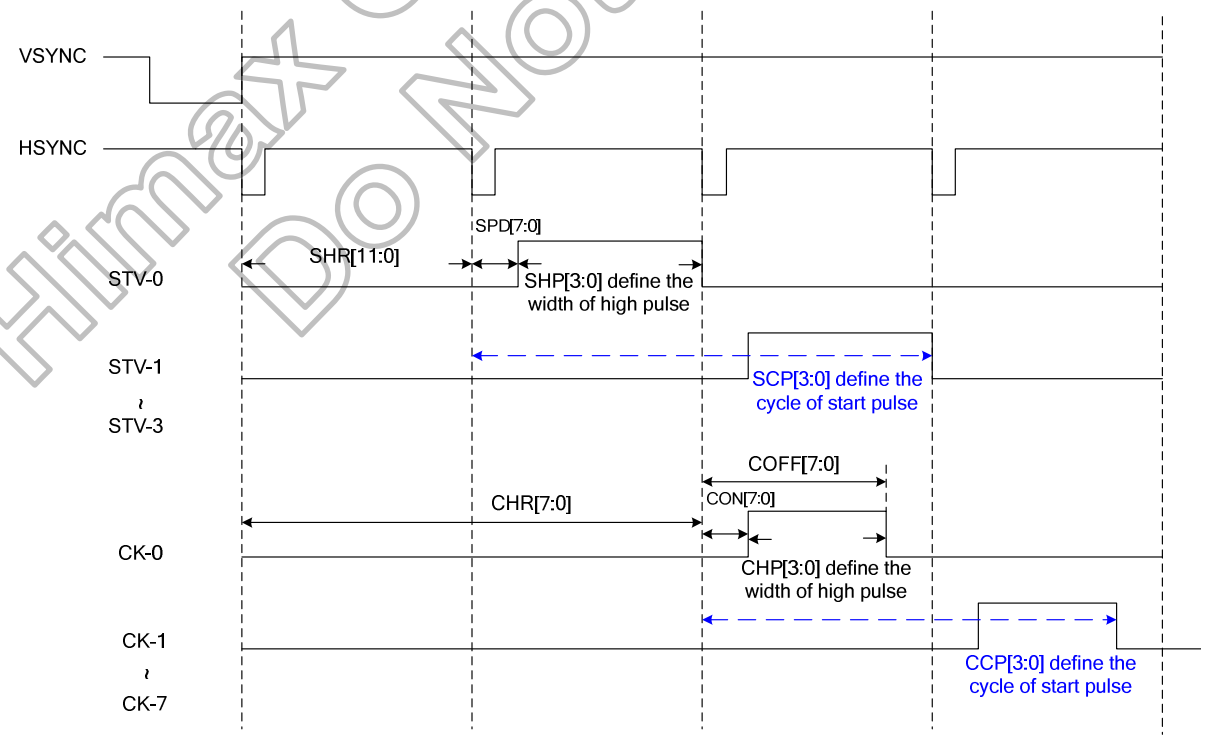
CCH	SETPANEL(Set panel related register)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	0	1	1	0	0	CC
1st parameter	1	1	↑	-	-	-	-	-	SS_PANEL	-	REV_PANEL	BGR_PANEL	-
Description0	This command is used to set setting of panel related register and make panel module meets below spec from viewpoint of user **BGR_PANEL**: The order of <R><G><B> dot color for module supplier, default value is stored in OTP. If color filter of panel is <B><G><R> type, setting BGR_PANEL = 1, if color filter of panel is <R><G><B> type, setting BGR_PANEL = 0. This bit is to make panel module look like a <R><G><B> type panel form the user viewpoint. **SS_PANEL**: Specify the shift direction of source driver output. When SS_PANEL = 0, the shift direction from S1 to S1440 When SS_PANEL = 1, the shift direction from S1440 to S1. **REV_PANEL:** Select the inversion of the display of all characters and graphics. This setting allows the display of the same data on both normally-white and normally-black panels. REV_PANEL = 0 normal-white panel REV_PANEL = 1 normal-black panel												
Restrictions	SETEXTC turn on to enable this command												
Register Availability	Status: Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes												
Default	Status: Default value: OTP value Power On Sequence / S/W Reset / H/W Reset: SS_PANEL=0, REV_PANE=1, BGR_PANEL=0: SS_PANEL, REV_PANE, BGR_PANEL												

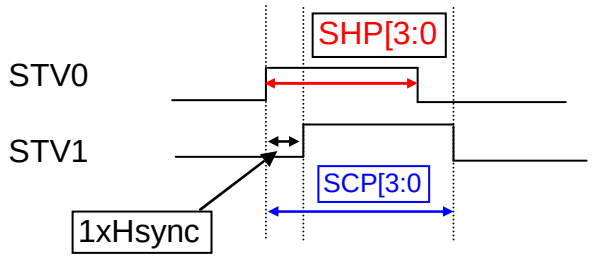
6.2.67 SETGIP (D5h)

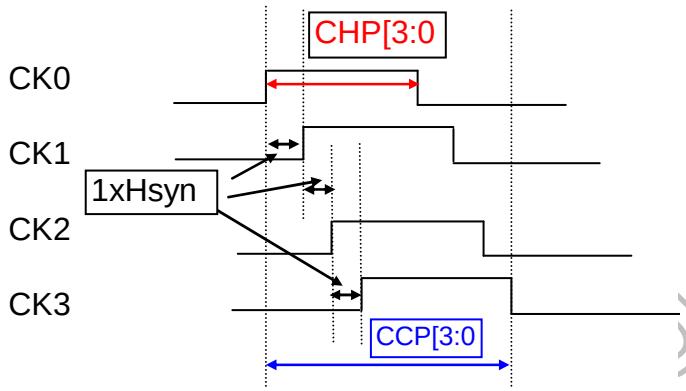
D5H	SETGIP												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	0	1	0	1	0	1	D5
1st parameter	1	1	↑	-	-	-	-	-	SHR_0[11:8]				-
2nd parameter	1	1	↑	-	SHR_0[7:0]								-
3rd parameter	1	1	↑	-	-	-	-	-	SHR_1[11:8]				-
4th parameter	1	1	↑	-	SHR_1[7:0]								-
5th parameter	1	1	↑	-	SPD[7:0]								-
6th parameter	1	1	↑	-	CHR[7:0]								-
7th parameter	1	1	↑	-	CON[7:0]								-
8th parameter	1	1	↑	-	COFF[7:0]								-
9th parameter	1	1	↑	-	SHP[3:0]				SCP[3:0]				-
10th parameter	1	1	↑	-	CHP[3:0]				CCP[3:0]				
11th parameter	1	1	↑	-	SOS_1[4:0]				SOS_0[3:0]				-
12th parameter	1	1	↑	-	SOS_3[4:0]				SOS_2[3:0]				-
13th parameter	1	1	↑	-	COS_1[4:0]				COS_0[3:0]				-
14th parameter	1	1	↑	-	COS_3[4:0]				COS_2[3:0]				-
15th parameter	1	1	↑	-	COS_5[4:0]				COS_4[3:0]				-
16th parameter	1	1	↑	-	COS_7[4:0]				COS_6[3:0]				-
17th parameter	1	1	↑	-	SOS_1_ML[3:0]				SOS_0_ML[3:0]				-
18th parameter	1	1	↑	-	SOS_3_ML[3:0]				SOS_2_ML[3:0]				-
19th parameter	1	1	↑	-	COS_1_ML[3:0]				COS_0_ML[3:0]				-
20th parameter	1	1	↑	-	COS_3_ML[3:0]				COS_2_ML[3:0]				-
21th parameter	1	1	↑	-	COS_5_ML[3:0]				COS_4_ML[3:0]				-
22th parameter	1	1	↑	-	COS_7_ML[3:0]				COS_6_ML[3:0]				-
23th parameter	1	1	↑	-	-	-	GTO[5:0]						-
24th parameter	1	1	↑	-	GNO[7:0]								-
25th parameter	1	1	↑	-	EQ_DELAY[7:0]								-
26th parameter	1	1	↑	-	GIP_OPT[7:0]								-

Description

This command is used for GIP timing output control.







SHR_0[11:0]:STV_0 Hsync Rise

SHR_0[11:0]	Start Pulse 0 Output delay
0x000h	0 x HSYNC
0x001h	1 x HSYNC
0x002h	2 x HSYNC
0x003h	3 x HSYNC
0x004h	4 x HSYNC
0x005h	5 x HSYNC
	• • • • •
0xFFEh	4094 x HSYNC
0xFFFh	4095 x HSYNC

SHR_1[11:0]:STV_1 Hsync Rise

SHR_1[11:0]	Start Pulse 1 Output delay
0x000h	0 x HSYNC
0x001h	1 x HSYNC
0x002h	2 x HSYNC
0x003h	3 x HSYNC
0x004h	4 x HSYNC
0x005h	5 x HSYNC
	• • • • •
0xFFEh	4094 x HSYNC
0xFFFh	4095 x HSYNC

SPD[7:0]: STV Pulse Delay

SPD[7:0]	Start Pulse Output delay
0x00h	0 x OSC CLK
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
0x03h	3 x OSC CLK
0x04h	4 x OSC CLK
0x05h	5 x OSC CLK
	• • • • •
0xFEh	254 x OSC CLK
0xFFh	255 x OSC CLK

CHR[7:0]: CK Hsync Rise

CHR[7:0]	Start Pulse 1 Output delay
0x00h	0 x HSYNC
0x01h	1 x HSYNC
0x02h	2 x HSYNC
0x03h	3 x HSYNC
0x004h	4 x HSYNC
0x005h	5 x HSYNC
	• • • • •
0xFEh	254 x HSYNC
0xFFh	255 x HSYNC

CON[7:0]: CK Pulse Delay

CON[7:0]	CK Pulse Output delay
0x00h	0 x OSC CLK
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
0x03h	3 x OSC CLK
0x04h	4 x OSC CLK
0x05h	5 x OSC CLK
	• • • • •
0xFEh	254 x OSC CLK
0xFFh	255 x OSC CLK

Note: Avoid CON[7:0] OSC LCK width > 1-line width

COFF[7:0]: CK Pulse width

COFF[7:0]	CK Pulse Output
0x00h	Inhibit
0x01h	1 x OSC CLK
0x02h	2 x OSC CLK
0x03h	3 x OSC CLK
0x04h	4 x OSC CLK
0x05h	5 x OSC CLK
	• • • • •
0xFEh	254 x OSC CLK
0xFFh	255 x OSC CLK

Note: COFF[7:0] value must bigger than CON[7:0] value

SHP[3:0]: Width of STV High pulse

SHP3	SHP2	SHP1	SHP0	Start Pulse Width
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
		• • • • •		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

SCP[3:0]: A Cycle of STV pulse

SCP3	SCP2	SCP1	SCP0	Start Pulse cycle
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC

		• • • • •		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

CHP[3:0]: Width of CK High pulse

CHP3	CHP2	CHP1	CHP0	CK Pulse Width
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
		• • • • •		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

CCP[3:0]: A Cycle of CK pulse

CCP3	CCP2	CCP1	CCP0	CK Pulse cycle
0	0	0	0	1 x HSYNC
0	0	0	1	2 x HSYNC
0	0	1	0	3 x HSYNC
0	0	1	1	4 x HSYNC
0	1	0	0	5 x HSYNC
0	1	0	1	6 x HSYNC
		• • • • •		
1	1	1	0	15 x HSYNC
1	1	1	1	16 x HSYNC

SOS_0[3:0] for CGOUT9_L pulse selector
SOS_1[3:0] for CGOUT10_L pulse selector
SOS_2[3:0] for CGOUT9_R pulse selector
SOS_3[3:0] for CGOUT10_R pulse selector

SOS_0/1/2/3[3]	SOS_0/1/2/3[2]	SOS_0/1/2/3[1]	SOS_0/1/2/3[0]	Signal Type
0	0	0	0	STV-0
0	0	0	1	STV-1
0	0	1	0	STV-2
0	0	1	1	STV-3
0	1	0	0	CK-0
0	1	0	1	CK-1
0	1	1	0	CK-2
0	1	1	1	CK-3
1	0	0	0	CK-4
1	0	0	1	CK-5
1	0	1	0	CK-6
1	0	1	1	CK-7
1	1	0	0	Inhibit
1	1	0	1	Inhibit
1	1	1	0	Inhibit
1	1	1	1	Inhibit

COS_0[3:0] for CGOUT5L pulse selector
COS_1[3:0] for CGOUT6L pulse selector
COS_2[3:0] for CGOUT7L pulse selector
COS_3[3:0] for CGOUT8L pulse selector
COS_4[3:0] for CGOUT5R pulse selector
COS_5[3:0] for CGOUT6R pulse selector
COS_6[3:0] for CGOUT7R pulse selector
COS_7[3:0] for CGOUT8R pulse selector

COS_0-7[3]	COS_0-7[2]	COS_0-7[1]	COS_0-7[0]	Signal Type
0	0	0	0	STV-0
0	0	0	1	STV-1
0	0	1	0	STV-2
0	0	1	1	STV-3
0	1	0	0	CK-0
0	1	0	1	CK-1
0	1	1	0	CK-2
0	1	1	1	CK-3
1	0	0	0	CK-4
1	0	0	1	CK-5
1	0	1	0	CK-6
1	0	1	1	CK-7
1	1	0	0	Inhibit
1	1	0	1	Inhibit
1	1	1	0	Inhibit
1	1	1	1	Inhibit

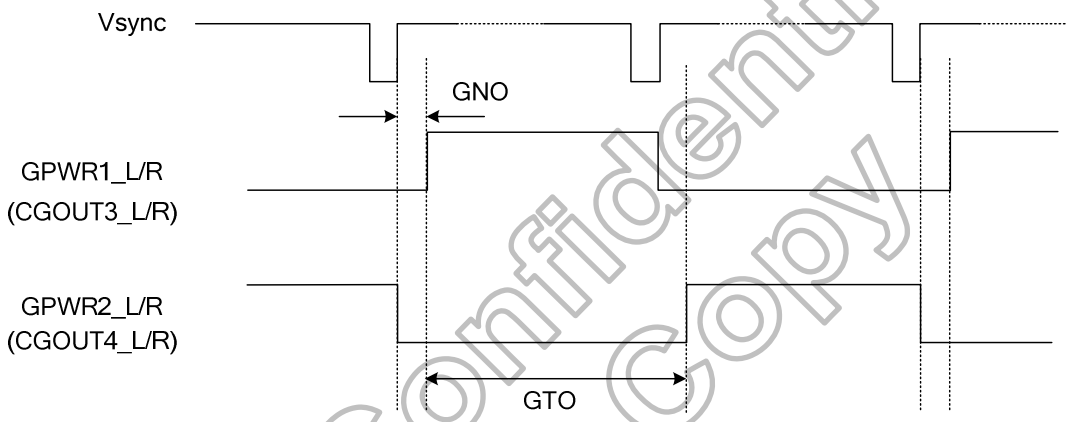
Once the R36h ML=1 the STV gate control signals are refered to the below registers:
SOS_0_ML[3:0] for CGOUT9_L pulse selector
SOS_1_ML[3:0] for CGOUT10_L pulse selector
SOS_2_ML[3:0] for CGOUT9_R pulse selector
SOS_3_ML[3:0] for CGOUT10_R pulse selector

SOS_0-3_ML[3]	SOS_0-3_ML[2]	SOS_0-3_ML[1]	SOS_0-3_ML[0]	Signal Type
0	0	0	0	STV-0
0	0	0	1	STV-1
0	0	1	0	STV-2
0	0	1	1	STV-3
0	1	0	0	CK-0
0	1	0	1	CK-1
0	1	1	0	CK-2
0	1	1	1	CK-3
1	0	0	0	CK-4
1	0	0	1	CK-5
1	0	1	0	CK-6
1	0	1	1	CK-7
1	1	0	0	Inhibit
1	1	0	1	Inhibit
1	1	1	0	Inhibit
1	1	1	1	Inhibit

Once the R36h ML=1 the CK gate control signals are refered to the below registers:
COS_0_ML[3:0] for CGOUT5L pulse selector
COS_1_ML[3:0] for CGOUT6L pulse selector
COS_2_ML[3:0] for CGOUT7L pulse selector
COS_3_ML[3:0] for CGOUT8L pulse selector
COS_4_ML[3:0] for CGOUT5R pulse selector
COS_5_ML[3:0] for CGOUT6R pulse selector
COS_6_ML[3:0] for CGOUT7R pulse selector
COS_7_ML[3:0] for CGOUT8R pulse selector

COS_0-7_ML[3]	COS_0-7_ML[2]	COS_0-7_ML[1]	COS_0-7_ML[0]	Signal Type
0	0	0	0	STV-0
0	0	0	1	STV-1
0	0	1	0	STV-2
0	0	1	1	STV-3
0	1	0	0	CK-0

0	1	0	1	CK-1
0	1	1	0	CK-2
0	1	1	1	CK-3
1	0	0	0	CK-4
1	0	0	1	CK-5
1	0	1	0	CK-6
1	0	1	1	CK-7
1	1	0	0	Inhibit
1	1	0	1	Inhibit
1	1	1	0	Inhibit
1	1	1	1	Inhibit



GTO[5:0]	GPWR toggle frequency
6'h00	64 x Frame
6'h01	1 x Frame
6'h02	2 x Frame
6'h03	3 x Frame
• • • • •	• • • • •
6'h3D	61 x Frame
6'h3E	62 x Frame
6'h3F	63 x Frame

GNO[7:0]	GPWR non-overlap timing
8'h00	0
8'h01	1 x OSC CLK
8'h02	2 x OSC CLK
8'h03	3 x OSC CLK
• • • • •	• • • • •
8'hFD	253 x OSC CLK
8'hFE	254 x OSC CLK
8'hFF	255 x OSC CLK

EQ_DELAY[7:0] is in-house function not open.

GIP_OPT[7:3] is in-hose function and not open.
GIP_OPT[2] is stv_2_time, In order to meet 2 STV pulses for BP and FP separately. It is the function of controlling the STV-0 and STV-1 pulses in the begin of a frame, and controlling the STV-2 and STV-3 pulses in the end of a frame. The pulses STV-2 and STV-3 started in position are determined by SHR_1[11:0].
GIP_OPT[1] is stv_gated, CK will be off while STV on.
GIP_OPT[0] is toggle_en, CK will toggle while porch duration.

Default	Status	Default value	OTP value	
	Power On Sequence S/W Reset H/W Reset	SHR_0[11:0]= 0x02h SHR_1[11:0]= 0x01h SPD[7:0]= 0x02h CHR[7:0]= 0x03h CON[7:0]= 0x20h COFF[7:0]= 0x6Cg SCP[3:0]= 0x03h SHP[3:0]= 0x00h CCP[3:0]= 0x03h CHP[3:0]= 0x00h SOS_0[3:0]= 0x00h SOS_1[3:0]= 0x00h SOS_2[3:0]= 0x00h SOS_3[3:0]= 0x00h COS_0[3:0]= 0x00h COS_1[3:0]= 0x06h COS_2[3:0]= 0x04h COS_3[3:0]= 0x00h COS_4[3:0]= 0x01h COS_5[3:0]= 0x07h COS_6[3:0]= 0x05h COS_7[3:0]= 0x07h SOS_0_ML[3:0]= 0x00h SOS_1_ML[3:0]= 0x00h SOS_2_ML[3:0]= 0x00h SOS_3_ML[3:0]= 0x00h COS_0_ML[3:0]= 0x01h COS_1_ML[3:0]= 0x05h COS_2_ML[3:0]= 0x07h COS_3_ML[3:0]= 0x05h COS_4_ML[3:0]= 0x00h COS_5_ML[3:0]= 0x04h COS_6_ML[3:0]= 0x06h COS_7_ML[3:0]= 0x04h GTO[5:0]= 0x01h GNO[7:0]= 0x0Ch EQ_DELAY[7:0]= 0x0Ch GIP_OPT[7:0]= 0x00h	SHR_0[11:0], SHR_1[11:0] SPD[7:0], CHR[7:0] CON[7:0], COFF[7:0] SCP[3:0], SHP[3:0] CCP[3:0], CHP[3:0] SOS_0[3:0], SOS_1[3:0] SOS_2[3:0], SOS_3[3:0] COS_0[3:0], COS_1[3:0] COS_2[3:0], COS_3[3:0] COS_4[3:0], COS_5[3:0] COS_6[3:0], COS_7[3:0] SOS_0_ML[3:0] SOS_1_ML[3:0] SOS_2_ML[3:0] SOS_3_ML[3:0] COS_0_ML[3:0] COS_1_ML[3:0] COS_2_ML[3:0] COS_3_ML[3:0] COS_4_ML[3:0] COS_5_ML[3:0] COS_6_ML[3:0] COS_7_ML[3:0] GTO[5:0], GNO[7:0] EQ_DELAY[7:0] GIP_OPT[7:0]	

6.2.68 SETGAMMA: Set gamma curve related setting (E0h)

E0H	SETGAMMAR (Set Gamma Curve Related Setting)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	0	0	0	0	0	E0
1st parameter	1	1	↑	-	-	-	G1_VRP0[5:0]						-
2nd parameter	1	1	↑	-	-	-	G1_VRP1[5:0]						-
3rd Parameter	1	1	↑	-	-	-	G1_VRP2[5:0]						-
4th Parameter	1	1	↑	-	-	-	G1_VRP3[5:0]						-
5th Parameter	1	1	↑	-	-	-	G1_VRP4[5:0]						-
6th Parameter	1	1	↑	-	-	-	G1_VRP5[5:0]						-
7th Parameter	1	1	↑	-	-	G1_PRP0[6:0]							-
8th Parameter	1	1	↑	-	-	G1_PRP1[6:0]							-
9th Parameter	1	1	↑	-	G1_CGMP0 [1:0]		-	G1_PKP0[4:0]					-
10th Parameter	1	1	↑	-	G1_CGMP1 [1:0]		-	G1_PKP1[4:0]					-
11th Parameter	1	1	↑	-	G1_CGMP2 [1:0]		-	G1_PKP2[4:0]					-
12th Parameter	1	1	↑	-	G1_CGMP3 [1:0]		-	G1_PKP3[4:0]					-
13th Parameter	1	1	↑	-	G1_CGMP5	G1_CGMP4	-	G1_PKP4[4:0]					-
14th Parameter	1	1	↑	-	-	-	-	G1_PKP5[4:0]					-
15th Parameter	1	1	↑	-	-	-	-	G1_PKP6[4:0]					-
16th Parameter	1	1	↑	-	-	-	-	G1_PKP7[4:0]					-
17th Parameter	1	1	↑	-	-	-	-	G1_PKP8[4:0]					-
18th Parameter	1	1	↑	-	-	-	G1_VRN0[5:0]						-
19th Parameter	1	1	↑	-	-	-	G1_VRN1[5:0]						-
20th Parameter	1	1	↑	-	-	-	G1_VRN2[5:0]						-
21th Parameter	1	1	↑	-	-	-	G1_VRN3[5:0]						-
22th Parameter	1	1	↑	-	-	-	G1_VRN4[5:0]						-
23th Parameter	1	1	↑	-	-	-	G1_VRN5[5:0]						-
24th Parameter	1	1	↑	-	-	G1_PRN0[6:0]							-
25th Parameter	1	1	↑	-	-	G1_PRN1[6:0]							-
26th Parameter	1	1	↑	-	G1_CGMN0 [1:0]		-	G1_PKN0[4:0]					-
27th Parameter	1	1	↑	-	G1_CGMN1 [1:0]		-	G1_PKN1[4:0]					-
28th Parameter	1	1	↑	-	G1_CGMN2 [1:0]		-	G1_PKN2[4:0]					-
29th Parameter	1	1	↑	-	G1_CGMN3 [1:0]		-	G1_PKN3[4:0]					-
30th Parameter	1	1	↑	-	G1_CGMN5	G1_CGMN4	-	G1_PKN4[4:0]					-
31th Parameter	1	1	↑	-	-	-	-	G1_PKN5[4:0]					-
32th Parameter	1	1	↑	-	-	-	-	G1_PKN6[4:0]					-
33th Parameter	1	1	↑	-	-	-	-	G1_PKN7[4:0]					-
34th Parameter	1	1	↑	-	-	-	-	G1_PKN8[4:0]					-

Description

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	G1_PRP0 6-0	G1_PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	G1_PRP1 6-0	G1_PRN1 6-0	Variable resistor (PRP/N1)for center adjustment
Macro Adjustment	G1_PKP0 4-0	G1_PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	G1_PKP1 4-0	G1_PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	G1_PKP2 4-0	G1_PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	G1_PKP3 4-0	G1_PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	G1_PKP4 4-0	G1_PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	G1_PKP5 4-0	G1_PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	G1_PKP6 4-0	G1_PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	G1_PKP7 4-0	G1_PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
	G1_PKP8 4-0	G1_PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
Offset Adjustment	G1_VRP0 5-0	G1_VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment
	G1_VRP1 5-0	G1_VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment
	G1_VRP2 5-0	G1_VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment
	G1_ VRP3 5-0	G1_VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment

	G1_VRP4 5-0	G1_VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment
	G1_VRP5 5-0	G1_VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment

G1_CGMP/N0: Select to change gamma resistor stream.
G1_CGMP/N1: Select to change gamma resistor stream.
G1_CGMP/N2: Select to change gamma resistor stream.
G1_CGMP/N3: Select to change gamma resistor stream. Please refer to Figure 5.31.
G1_CGMP/N4: Select to change gamma resistor stream. Please refer to Figure 5.31.
G1_CGMP/N5: Select to change gamma resistor stream. Please refer to Figure 5.31.

Restriction

SETEXTC turn on to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	G1_VRP0[5:0]=0x00h, G1_VRP1[5:0]=0x18h, G1_VRP2[5:0]=0x1Fh, G1_VRP3[5:0]=0x3Fh, G1_VRP4[5:0]=0x3Fh, G1_VRP5[5:0]=0x3Fh, G1_PRP0[6:0]=0x33h, G1_PRP1[6:0]=0x57h, G1_CGMP0[1:0]=00, G1_CGMP1[1:0]=00, G1_CGMP2[1:0]=00, G1_CGMP3[1:0]=00, G1_CGMP4=0, G1_CGMP5=0, G1_ PKP0[4:0]=0x07h, G1_ PKP1[4:0]=0x0Dh, G1_ PKP2[4:0]=0x0Fh, G1_ PKP3[4:0]=0x13h, G1_ PKP4[4:0]=0x16h, G1_ PKP5[4:0]=0x14h, G1_ PKP6[4:0]=0x16h, G1_ PKP7[4:0]=0x18h, G1_ PKP8[4:0]=0x1Fh, G1_VRN0[5:0]=0x00h, G1_VRN1[5:0]=0x18h, G1_VRN2[5:0]=0x1Fh, G1_VRN3[5:0]=0x3Fh, G1_VRN4[5:0]=0x3Fh, G1_VRN5[5:0]=0x3Fh, G1_ PKN0[4:0]=0x07h, G1_ PKN1[4:0]=0x0Dh, G1_ PKN2[4:0]=0x0Fh, G1_ PKN3[4:0]=0x13h, G1_ PKN4[4:0]=0x16h, G1_ PKN5[4:0]=0x14h, G1_ PKN6[4:0]=0x16h, G1_ PKN7[4:0]=0x18h, G1_ PKN8[4:0]=0x1Fh, G1_CGMN0[1:0]=00, G1_CGMN1[1:0]=00, G1_CGMN2[1:0]=00, G1_CGMN3[1:0]=00, G1_CGMN4=0, G1_CGMN5=0,	G1_VRP0[5:0], G1_VRP1[5:0], G1_VRP2[5:0], G1_VRP3[5:0], G1_VRP4[5:0], G1_VRP5[5:0], G1_PRP0[6:0], G1_PRP1[6:0], G1_CGMP0[1:0], G1_CGMP1[1:0], G1_CGMP2[1:0], G1_CGMP3[1:0], G1_CGMP4, G1_CGMP5, G1_ PKP0[4:0], G1_ PKP1[4:0], G1_ PKP2[4:0], G1_ PKP3[4:0], G1_ PKP4[4:0], G1_ PKP5[4:0], G1_ PKP6[4:0], G1_ PKP7[4:0], G1_ PKP8[4:0], G1_VRN0[5:0], G1_VRN1[5:0], G1_VRN2[5:0], G1_VRN3[5:0], G1_VRN4[5:0], G1_VRN5[5:0], G1_ PKN0[4:0], G1_ PKN1[4:0], G1_ PKN2[4:0], G1_ PKN3[4:0], G1_ PKN4[4:0], G1_ PKN5[4:0], G1_ PKN6[4:0], G1_ PKN7[4:0], G1_ PKN8[4:0], G1_CGMN0[1:0], G1_CGMN1[1:0], G1_CGMN2[1:0], G1_CGMN3[1:0], G1_CGMN4, G1_CGMN5.

6.2.69 SETOTPKEY (E9h)

<table>
<tr><th rowspan="2">E9H</th><th colspan="13">SETOTPKEY</th></tr>
<tr><th>DNC</th><th>NRD</th><th>NWR</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>E9</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td colspan="8">OTP_KEY0[7:0]</td><td>00h</td></tr>
<tr><td>2nd parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td colspan="8">OTP_KEY1[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set OTP key to enter or leave OTP program mode.
<table>
<tr><th>OTP_KEY0[7:0]
OTP_KEY1[7:0]</th><th>Description</th><th>Note</th></tr>
<tr><td>OTP_KEY0[7:0] = 0xAAh
OTP_KEY1[7:0] = 0x55h</td><td>Enter OTP program mode</td><td></td></tr>
<tr><td>OTP_KEY0[7:0] = 0x00h
OTP_KEY1[7:0] = 0x00h</td><td>Leave OTP program mode</td><td></td></tr>
<tr><td>Other value</td><td>Invalid</td><td>1. If HX8369-A02 operate on OTP program mode, Then keep on OTP program mode.
2. If HX8369-A02 operate on non-OTP program mode, Then keep on non-OTP program mode.</td></tr>
</table></td></tr>
<tr><td>Restrictions</td><td colspan="13">SETEXTC turn on to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default value</th><th>OTP value</th></tr>
<tr><td>Power On Sequence
S/W Reset
H/W Reset</td><td>OTP_KEY0[7:0]=0x00h,
OTP_KEY1[7:0]=0x00h</td><td>N/A</td></tr>
</table></td></tr>
</table>

6.2.70 GETHXID (F4h)

F4H	GETHXIC												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	1	0	1	0	0	F4
1st parameter	1	↑	1	-	Himax ID[7:0]								-
Description	This command is used to get LCD ID and version.												
Restrictions	SETEXTC turn on to enable this command.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value	OTP value
Power On Sequence S/W Reset H/W Reset	Himax ID[7:0] = 0x69h Version[7:0] = 0x02h	N/A

6.2.71 SETCNCD/GETCNCD (FDh)

<table>
<tr><th rowspan="2">FDH</th><td colspan="13">SETCNCD/GETCNCD (Set/Get Continue Command)</td></tr>
<tr><td>DNC</td><td>NRD</td><td>NWR</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>-</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>FD</td></tr>
<tr><td>1st parameter</td><td>1</td><td>1</td><td>↑</td><td>-</td><td colspan="9">WR_CMD_CN[7:0]</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">This function is use to instead of Register-Content interface mode.
The parameter for SETCNCD will continue to read from the last command address automatically.</td></tr>
<tr><td>Restrictions</td><td colspan="13">SETEXTC turn on to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default value</td><td>OTP value</td></tr><tr><td>Power On Sequence
S/W Reset
H/W Reset</td><td>N/A</td><td>N/A</td></tr></table></td></tr>
</table>

6.2.72 SET SPI READ INDEX (FEh)

FEH	SET SPI READ INDEX (Set SPI READ Command Address)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	1	1	1	1	0	FE
1st parameter	1	1	↑	-	CMD_ADD[7:0]								-
Description	SET SPI READ Command Address for User Define Command.												
Restrictions	SETEXTC turn on to enable this command												
Register Availability	Status: Idle Mode Off, Sleep Out — Availability: Yes Status: Idle Mode On, Sleep Out — Availability: Yes												
Default	Status: Power On Sequence, S/W Reset, H/W Reset — Default value: CMD_ADD[7:0]=0x00h — OTP value: N/A												

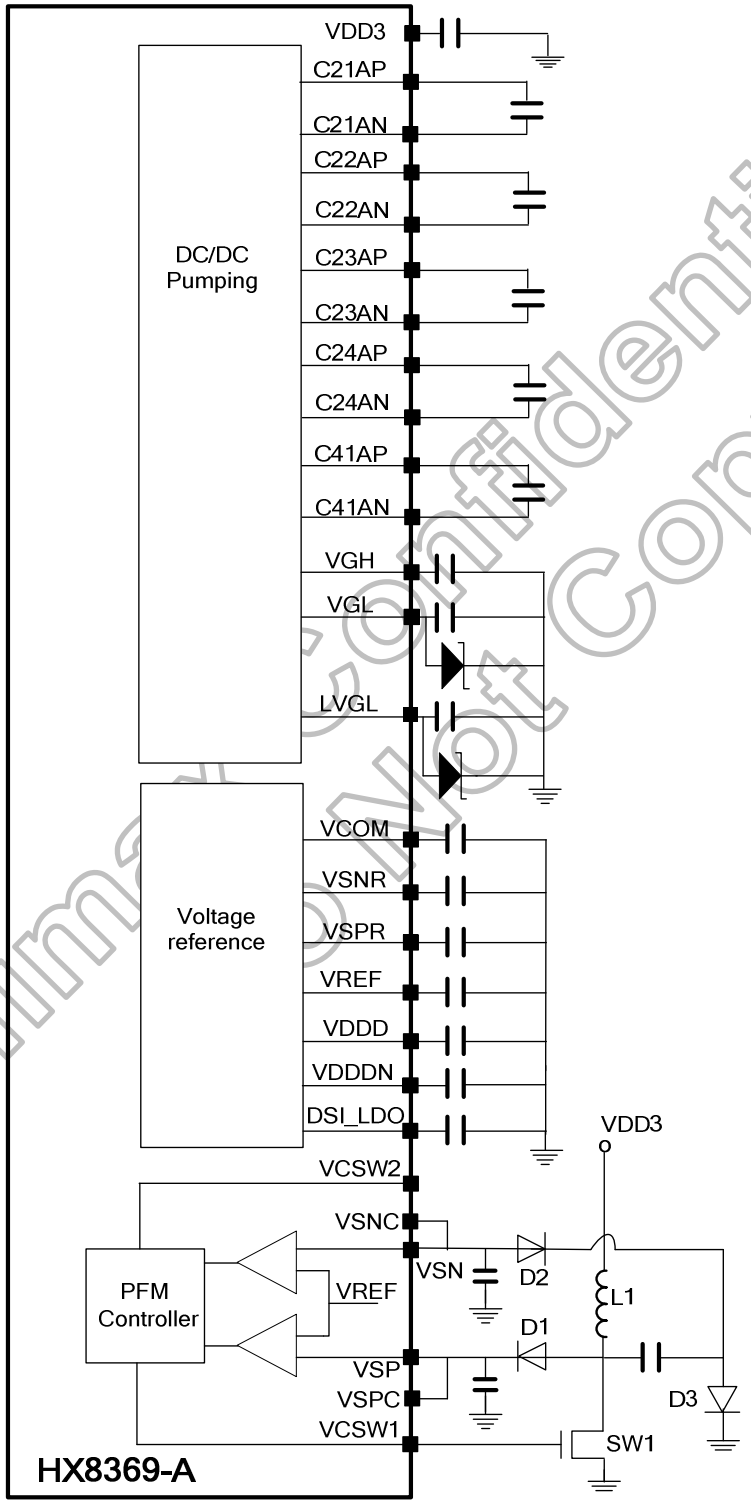
6.2.73 GETSPIREAD: Read command data (FFh)

FFH	GETMPUREAD (Read Command Data)												
	DNC	NRD	NWR	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	1	1	1	1	1	1	1	1	FF
1st parameter	1	↑	1	-	CMD_DATA1[7:0]								-
:	1	↑	1	-	:								-
nth parameter	1	↑	1	-	CMD_DATAN[7:0]								-
Description	Read SPI Command Data for User Define Command.												
Restrictions	SETEXTC turn on to enable this command.												
Register Availability	Status	Availability											
	Idle Mode Off, Sleep Out	Yes											
	Idle Mode On, Sleep Out	Yes											
	Sleep In or Booster Off	Yes											
Default	Status	Default value	OTP value										
	Power On Sequence S/W Reset H/W Reset	N/A	N/A										

7. Power Supply

7.1 Power supply setup

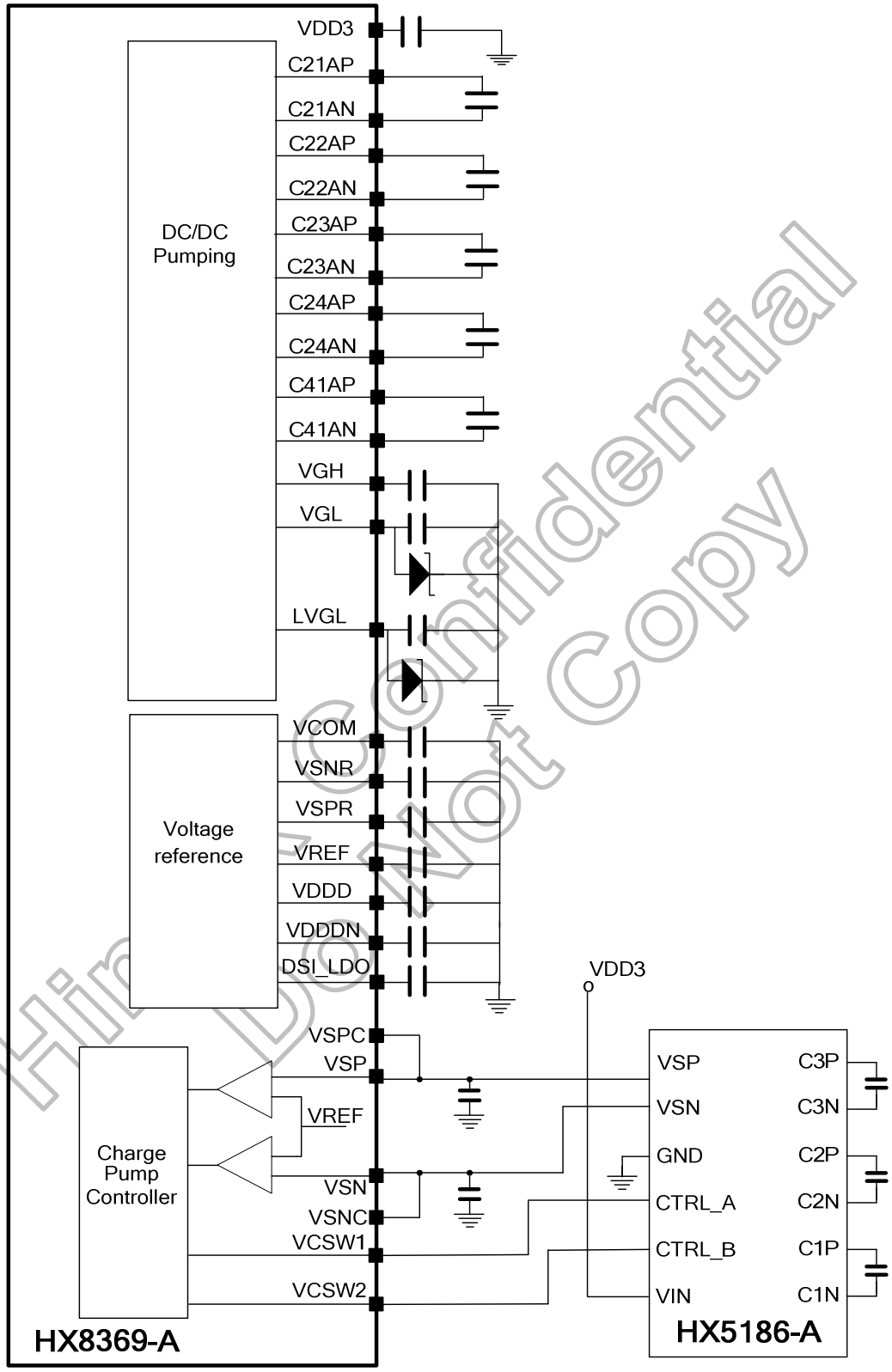
7.1.1 Architecture 1 with PFM circuit



Note: If not use LVGL, please connect the VGL and LVGL together.

Figure 7.1: Power supply with PFM circuit

7.1.2 Architecture 2 with HX5186-A



Note: If not use LVGL, please connect the VGL and LVGL together.

Figure 7.2: Power supply with HX5186-A

7.2 Voltage configuration

The HX8369-A02 has an internal power supply circuit to drive TFTLCD panel. Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
VREF	Reference voltage from internal band gap circuit	1.8V	-
VSP	DC/DC converter circuit output	4.7V ~ 5.5V	Do not exceed 6 V
VSN	DC/DC converter circuit output	-4.7V ~ -5.5V	Do not exceed 6V
VSPC	DC/DC converter circuit output	4.7V ~ 5.5V	Do not exceed 6 V
VSNC	DC/DC converter circuit output	-4.7V ~ -5.5V	Do not exceed 6V
VSPR	Reference voltage for gamma circuit	3.5V ~ (VSP – 0.5V)	Reference register
VSNR	Reference voltage for gamma circuit	-3.5V ~ (VSN + 0.5V)	Reference register
VDDDN	Logic power supply	-2.5V	-
VGH	Positive gate driver output voltage level	+9V ~ +20V	Depend on VSP and VSN
VGL	Negative gate driver output voltage level	-6V ~ -13.5V	Depend on VSP and VSN
LVGL	GIP most negative voltage level	VGL-VDD3	Depend on VSP and VSN
VCOM	VCOM DC voltage	-2V ~ 0V	-
DSI_LDO	Analog power for MIPI DSI circuit	1.2V ~ 1.3V	-

Pad Name	Connection	Typical Component Value
VCOM	Connect to Capacitor (Max 6V): VCOM ---(-)----| |--- (+)----- VSSA	2.2 µF
VGH	Connect to Capacitor (Max 25V): VGH ---(+)----| |--- (-)----- VSSA	1.0 µF
VGL	Connect to Capacitor (Max 16V): VGL ---(+)----| |--- (-)----- VSSA	1.0 µF
	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----∫◄--- (+)---- VGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)
C24AP - C24AN	Connect to Capacitor (Max 16V): C24AP ---(+)----| |--- (-)-----C24AN	1.0 µF
C23AP - C23AN	Connect to Capacitor (Max 16V): C23AP ---(+)----| |--- (-)-----C23AN	1.0 µF
C22AP - C22AN	Connect to Capacitor (Max 16V): C22AP ---(+)----| |--- (-)-----C22AN	1.0 µF
C21AP - C21AN	Connect to Capacitor (Max 16V): C21AP ---(+)----| |--- (-)-----C21AN	1.0 µF
C41AP – C41AN	Connect to Capacitor (Max 16V): C41AP ---(+)----| |--- (-)-----C41AN	1.0 µF
VSPR	Connect to Capacitor (Max 10V): VSPR ---(+)----| |--- (-)-----VSSA	1.0 µF
VSNR	Connect to Capacitor (Max 10V): VSNR ---(+)----| |--- (-)-----VSSA	1.0 µF
VDDD	Connect to Capacitor (Max 6V): VDDD ---(+)----| |--- (-)-----VSSA	1.0 µF
VDDDN	Connect to Capacitor (Max 6V): VDDDN ---(+)----| |--- (-)-----VSSA	1.0 µF
VREF	Connect to Capacitor (Max 6V): VREF ---(-)----| |--- (+)----- VSSA	1.0 µF
VSP	Connect to Capacitor (Max 10V):VSP ---(+)----| |--- (-)-----VSSA	2.2 µF
VSN	Connect to Capacitor (Max 10V):VSN ---(+)----| |--- (-)-----VSSA	2.2 µF
VDD3	Connect to Capacitor (Max 10V): VDD3 ---(+)----| |--- (-)-----VSSA	1.0 µF
DSI_LDO	Connect to Capacitor (Max 6V): DSI_LDO ---(+)----| |--- (-)----DSI_VSS	1.0 µF
LVGL	Connect to Capacitor (Max 16V): LVGL ---(-)----| |--- (+)----- VSSA	1.0 µF
	Connect to Schottky Diode(VR≥30V): VSSA ---(-)----∫◄--- (+)---- LVGL	VF < 0.4V / 20mA @ 25°C, VR ≥30V (Recommended diode: RB521S-30)

Table 7.1: Adoptability of component

8. Electrical Characteristics

8.1 Absolute maximum ratings

The absolute maximum ratings are list on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDD1~ VSSD	V	-0.3 to +3.6	Note(1),(2)
Power Supply Voltage 2	VDD2 ~ VSSA	V	-0.3 to +5.5	Note(1),(3)
Power Supply Voltage 3	VDD3 ~ VSSA	V	-0.3 to +5.5	Note(1) (4)
Power Supply Voltage 4	DSI_VCC ~ DSI_VSS	V	-0.3 to +3.6	Note(1) (5)
Power Supply Voltage 5	VSP ~ VSSA	V	-0.3 to +6.6	Note(6)
Power Supply Voltage 6	VSSA ~ VSN	V	0 to -6.6	Note(7)
Power Supply Voltage 7	VGH ~ VSSA	V	-0.3 to +25	Note(8)
Power Supply Voltage 8	VSSA ~ VGL	V	0 to -16	Note(9)
Operating Temperature	Topr	°C	-40 to +85	Note(10)
Storage Temperature	Tstg	°C	-55 to +110	Note(11)

Note: (1) VDD1, VSSD must be maintained.
(2) To make sure VDD1 ≥ VSSD.
(3) To make sure VDD2≥ VSSA.
(4) To make sure VDD3≥ VSSA.
(5) To make sure DSI_VCC ≥ DSI_VSS.
(6) To make sure VSP ≥ VSSA.
(7) To make sure VSSA ≥ VSN
(8) To make sure VGH ≥ VSSA.
(9) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(10) For die and wafer products, specified up to +85℃.
(11) This temperature specifications apply to the TCP package.

Table 8.1: Absolute maximum rating

8.2 ESD protection level

Mode	Test condition	Criteria	Standard
Human Body Model	C=100 pF, R=1.5 kΩ	±2.0KV	MIL-STD-883F Method 3015.7
Machine Model	C=200 pF, R=0.0 Ω	±200V	EIA/JEDEC JESD22-A115-A

Table 8.2: ESD protection level

8.3 DC characteristics

(VDD2=2.3 ~ 4.8V, VDD3=2.3 ~ 4.8V, VDD1=1.65~3.3V, T_A=-40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VDD1= 1.65 ~ 3.3V VDD2= 2.3 ~ 3.3V VDD3= 2.3 ~ 3.3V	0.7 V_{DD1}	-	VDD1	V
Input low voltage	V_{IL}	V		0	-	0.3 V_{DD1}	V
VPP	V_{IH}	V	VPP	7.25V	7.5V	7.75V	V
	V_{IL}	V					
Output high voltage (SDO, CABC_PWM_OUT)	V_{OH1}	V	I_{OH} = -1.0 mA	0.8 V_{DD1}	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT)	V_{OL1}	V	VDD1= 1.65 ~ 2.4V I_{OL} = 1.0 mA	0	-	0.2 V_{DD1}	V
Logic High level input current	I_{IH}	uA	VSYNC, HSYNC	-	-	1	uA
			RESX, DCX_SCL, CSX, RDX_E, WRX_DCX	-	-	1	uA
	I_{IHD}	uA	DB[23…0], SDI, DCX_SCL	-	-	1	uA
			DB[23…0]	-	-	1	uA
Logic Low level input current	I_{IL}	uA	VSYNC, HSYNC	-1	-		uA
			RESX, DCX_SCL, CSX, RDX_E, WRX_DCX	-1	-		uA
	I_{ILD}	uA	DB[23…0], SDI, DCX_SCL	-1	-		uA
			DB[17…0]	-1	-		uA
Current consumption standby mode (VDD2/VDD3-VSSD)	$I_{ST(VDD)}$	µA	VDD2/VDD3=2.8V, VDD1=1.8V T_A =25°C	-	30	80	uA
Current consumption standby mode (VDD1– VSSD)	$I_{ST(VDD1)}$	µA		-	1	-	uA
Current consumption during Deep-standby mode (VDD2/VDD3-VSSD)	$I_{DP-ST(VDD)}$	µA	VDD2/VDD3=2.8V, VDD1=1.8V T_A =25°C	-	5	-	uA
Current consumption during Deep-standby mode (VDD1– VSSD)	$I_{DP-ST(VDD1)}$	µA		-	1	-	uA

Note: 1. The VPP pin is open on normal mode and in used while OTP programming condition.
2. The GRAM data is eliminated under the Deep standby mode.

Table 8.3: DC characteristic

8.4 AC characteristics

8.4.1 DBI Type A interface characteristics

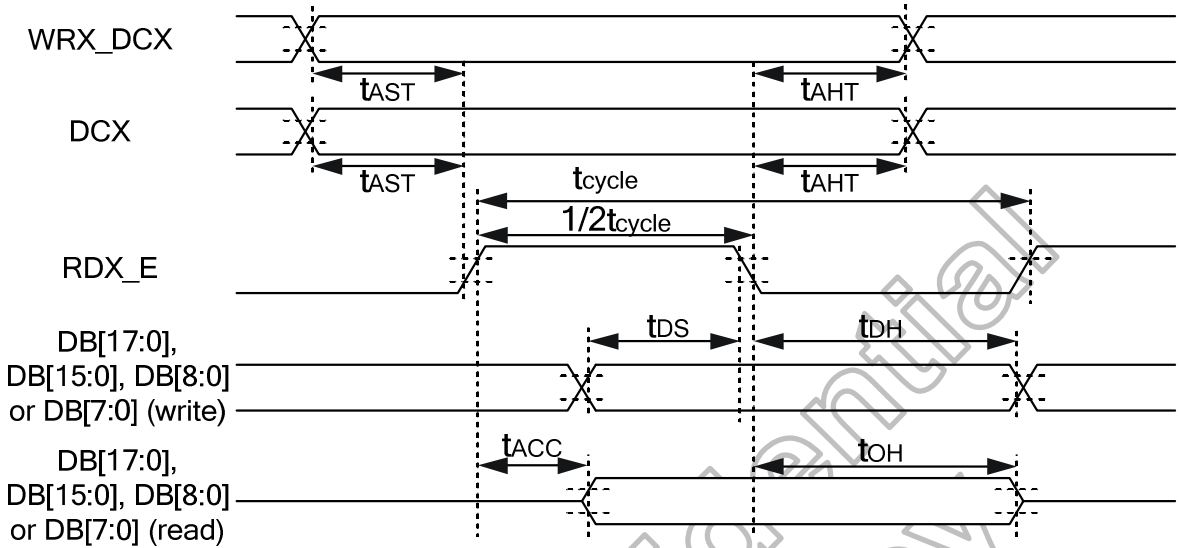


Figure 8.1: DBI Type A interface characteristics(CLK-E mode)

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
WRX_DCX or DCX_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
CSX or RDX_E	t_{cycle}	System clock cycle time read register	100	790	ns	-
		Read GRAM	350	790	ns	-
		Write register	100	790	ns	-
		Write GRAM @ SLPOUT	33	790	ns	-
		Write GRAM @ SLPIN	100	790	ns	-
DB23-DB0	t_{DS} t_{DH} t_{ACC} t_{OH}	Data setup time Data hold time Read access time Output disable time	15 25 10 10	- - - -	ns	For maximum CL=30pF For minimum CL=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.4: DBI Type A interface characteristics

8.4.2 DBI Type B interface characteristics

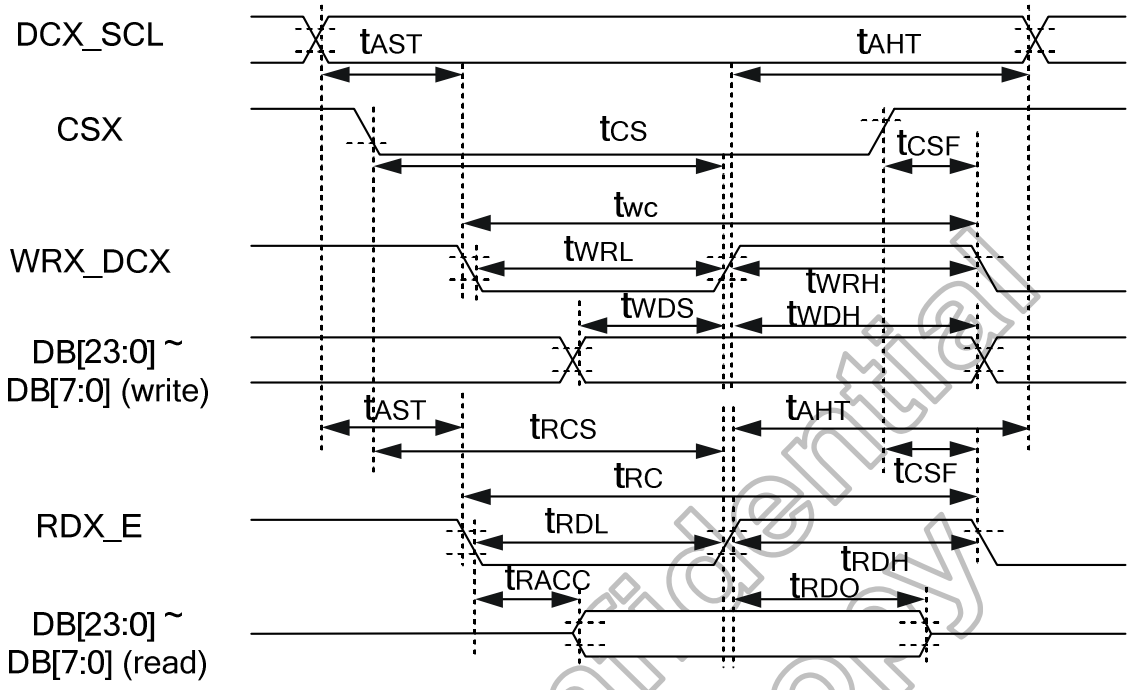


Figure 8.2: DBI Type B interface characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DCX_SCL	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
CSX	t_{CS} t_{RCS} t_{RCSFM} t_{CSF}	Chip select setup time (Write) Chip select setup time (Read ID) Chip Select setup time (Read FM) Chip select wait time (Write/Read)	20 45 355 20	- - - -	ns	-
WRX_DCX	t_{WC} t_{WC} t_{WC} t_{WRH} t_{WRL}	Write cycle (write register) Write cycle (write GRAM@SLPOUT) Write cycle (write GRAM@SLPIN) Control pulse “H” duration Control pulse “L” duration	100 33 100 15 15	790 790 790 630 160	ns	-
RDX_E	t_{RC} t_{RC} t_{RDH} t_{RDL}	Read cycle (read register) Read cycle (GRAM) Control pulse “H” duration Control pulse “L” duration	100 350 30 20	790 790 630 160	ns	-
DB23-DB0	t_{WDS} t_{WDH} t_{RACC} t_{RDO}	Data setup time Data hold time Read access time Output disable time	15 25 10 10	- - - -	ns	For maximum C_L=30pF For minimum C_L=8pF

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.5: DBI Type B interface characteristics

8.4.3 DBI Type C interface characteristics

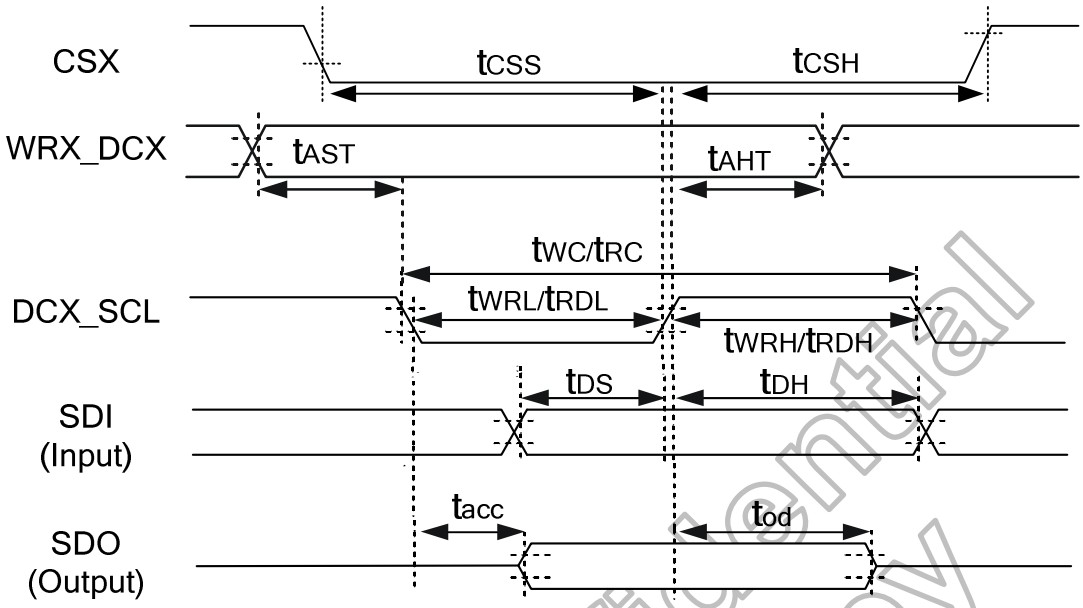


Figure 8.3: DBI Type C interface characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A = 25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS} t_{CSH}	Chip select setup time (Write) Chip select setup time (Read)	40 40	- -	ns	-
WRX_DCX	t_{AST} t_{AHT}	Address setup time Address hold time (Write/Read)	10 10	- -	ns	-
DCX_SCL (Write)	t_{WC} t_{WRH} t_{WRL}	Write cycle Control pulse “H” duration Control pulse “L” duration	100 40 40	- - -	ns	-
DCX_SCL (Read)	t_{RC} t_{RDH} t_{RDL}	Read cycle Control pulse “H” duration Control pulse “L” duration	150 60 60	- - -	ns	-
SDI/SDO (Input)	t_{DS} t_{DT}	Data setup time Data hold time	30 30	- -	ns	For maximum C_L=30pF For minimum C_L=8pF
SDI/SDO (Output)	t_{RACC} t_{OD}	Read access time Output disable time	10 10	- 50	ns	

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.6: DBI Type C interface characteristics

8.4.4 DPI interface characteristics

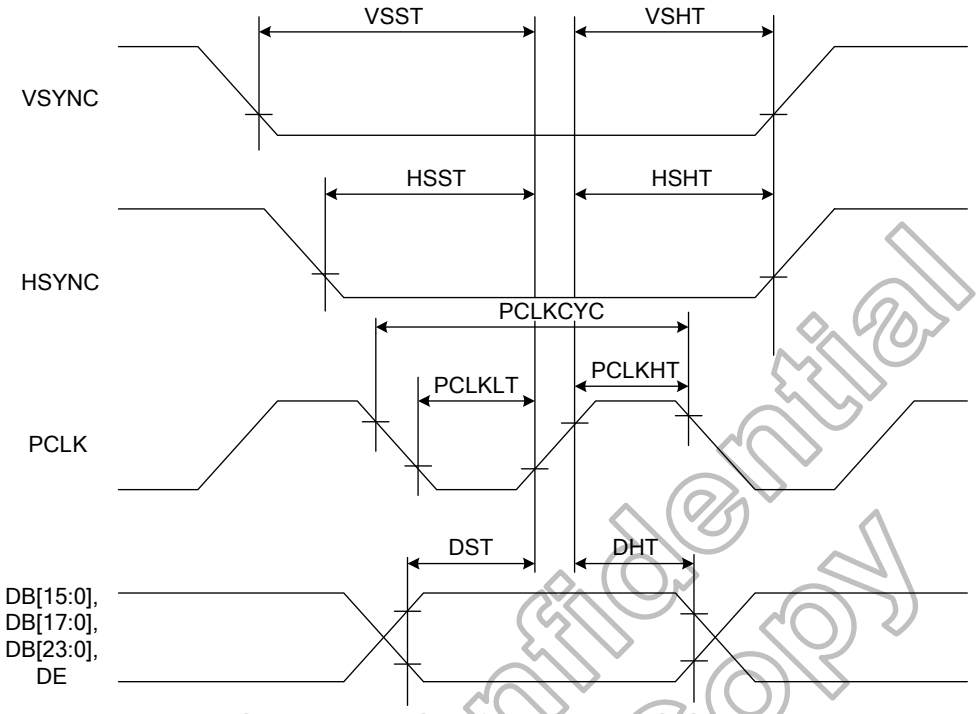


Figure 8.4: DPI interface characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	5	-	-	ns
Vertical sync. hold time	VSHT	-	5	-	-	ns
Horizontal sync. setup time	HSST	-	5	-	-	ns
Horizontal sync. hold time	HSHT	-	5	-	-	ns
Pixel clock cycle when RGB I/F is running	PCLKCYC (480x854)	VRR(3) = Min . 50 Hz Max. 70 Hz	21.6	-	34.3	MHz
			29.1	-	46.2	ns
	PCLKCYC (480x800)	VRR(3) = Min . 50 Hz Max. 70 Hz	20.3	-	32.2	MHz
			31	-	49.2	ns
	PCLKCYC (360x640)	VRR(3) = Min . 50 Hz Max. 70 Hz	12.4	-	20.3	MHz
			49.2		80.6	ns
Pixel clock low time	PCLKLT	-	5	-	-	ns
Pixel clock high time	PCLKHT	-	5	-	-	ns
Data setup time DB[23:0]	DST	-	5	-	-	ns
Data hold time DB[23:0]	DHT	-	5	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) VRR : Vertical Refresh Rate, equal to VSYNC frequency.

Table 8.7: DPI interface characteristics

Vertical Timings for RGB I/F

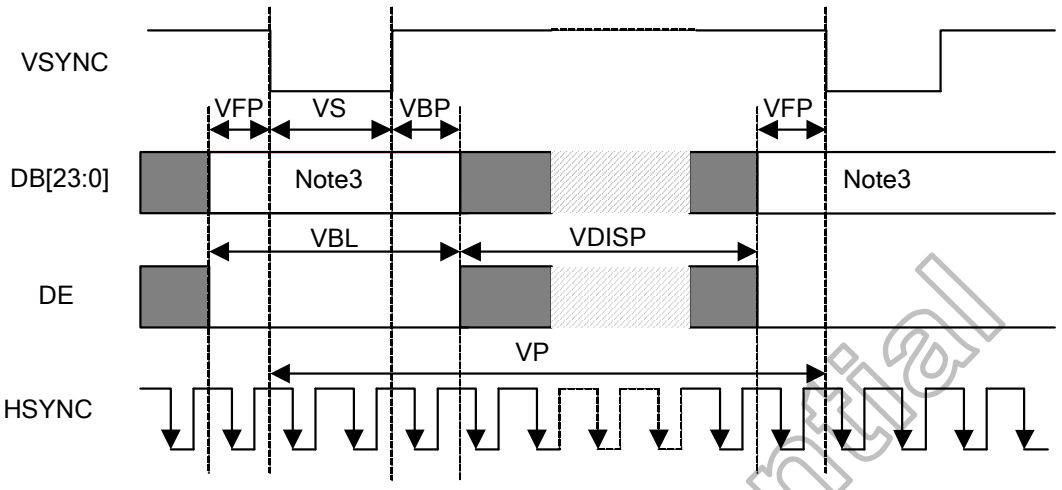


Figure 8.5: Vertical Timings for RGB I/F

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	Resolution=480x854	860			Line
		Resolution=480x800	806	-	-	Line
		Resolution=360x640	646			Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP(480x854)	-	854	-	Line
		VDISP(480x800)	-	800		
		VDISP(360x640)	-	640		
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for highstate.
(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(4) The VS and VBP pulse width are related to ASG/GIP STV and CKV timing. The STV and CKV must be set at corresponding position for LCD normal display. Also refer to setion 6.2.66 SETGIP.

Table 8.8 Vertical Timings for RGB I/F

Horizontal Timings for RGB I/F

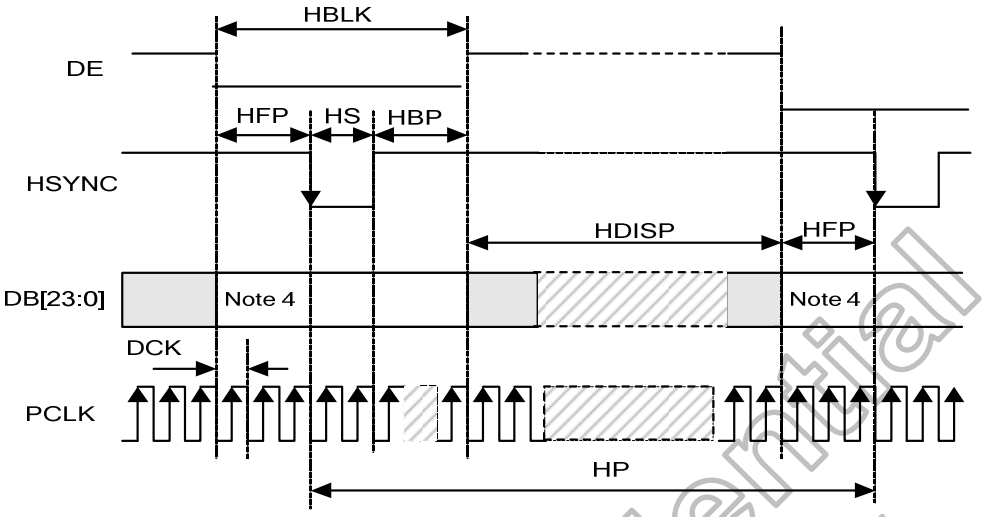


Figure 8.6: Horizontal Timing for RGB I/F

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Resolution=480x854	504	-	568	DCK
		Resolution=480x800	504	-	568	DCK
		Resolution=360x640	384	-	448	DCK
HS low pulse width	HS	-	5	-	78	DCK
Horizontal back porch	HBP	-	5	-	78	DCK
Horizontal front porch	HFP	-	5	-	78	DCK
Horizontal data start point	-	HS+HBP	19	-	83	DCK
			700	-	-	ns
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	DCK
Horizontal active area	HDISP	Resolution=480x854	-	480	-	DCK
		Resolution=480x800	-	480	-	DCK
		Resolution=360x640	-	360	-	DCK
Pixel clock frequency When RGB I/F is running	DCK (480x854)	VRR = Min. 50 Hz	21.6	-	34.3	MHz
		– Max. 70 Hz	29.1	-	46.2	ns
	DCK (480x800)	VRR = Min. 50 Hz	20.3	-	32.2	MHz
		– Max. 70 Hz	31	-	49.2	ns
	DCK (360x640)	VRR = Min. 50 Hz	12.4	-	20.3	MHz
		– Max. 70 Hz	49.2		80.6	ns

Note:(1) Signal rise and fall times are equal to or less than 20 ns.
(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.
(3) HP is multiples of eight DCK.
(4)Data lines can be set to “High” or “Low” during blanking time – Don’t care.

Table 8.9 Horizontal Timings for RGB I/F

8.4.5 Reset input timing

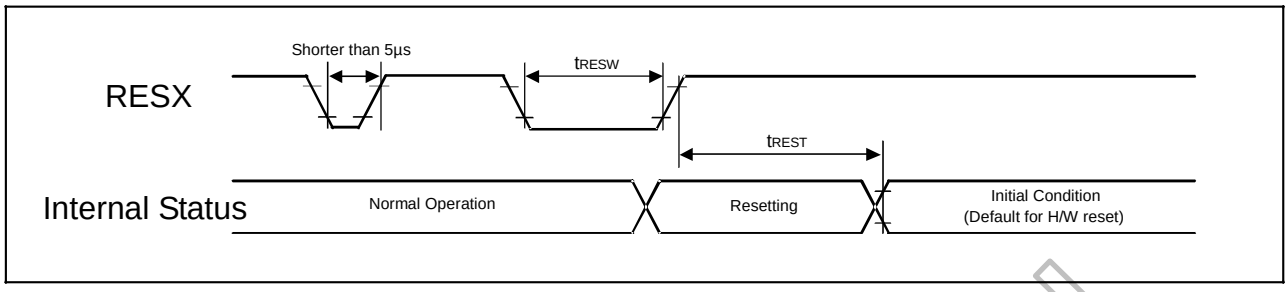


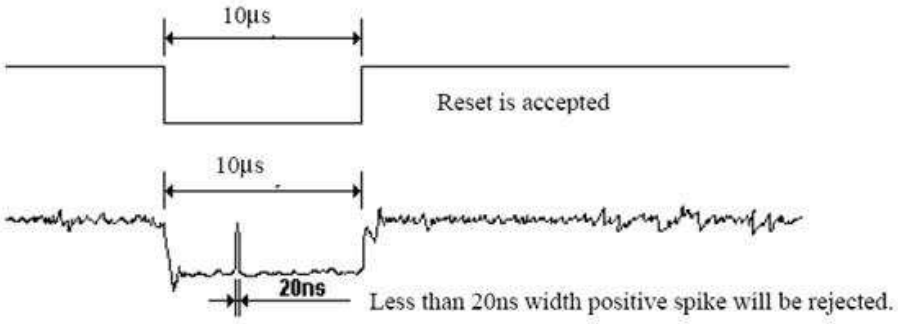
Figure 8.7: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	RESX	10	-	-	-	µs
t_{REST}	Reset complete time(2)	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µ	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.
(6) When Reset is applied during Sleep Out Mode.
(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

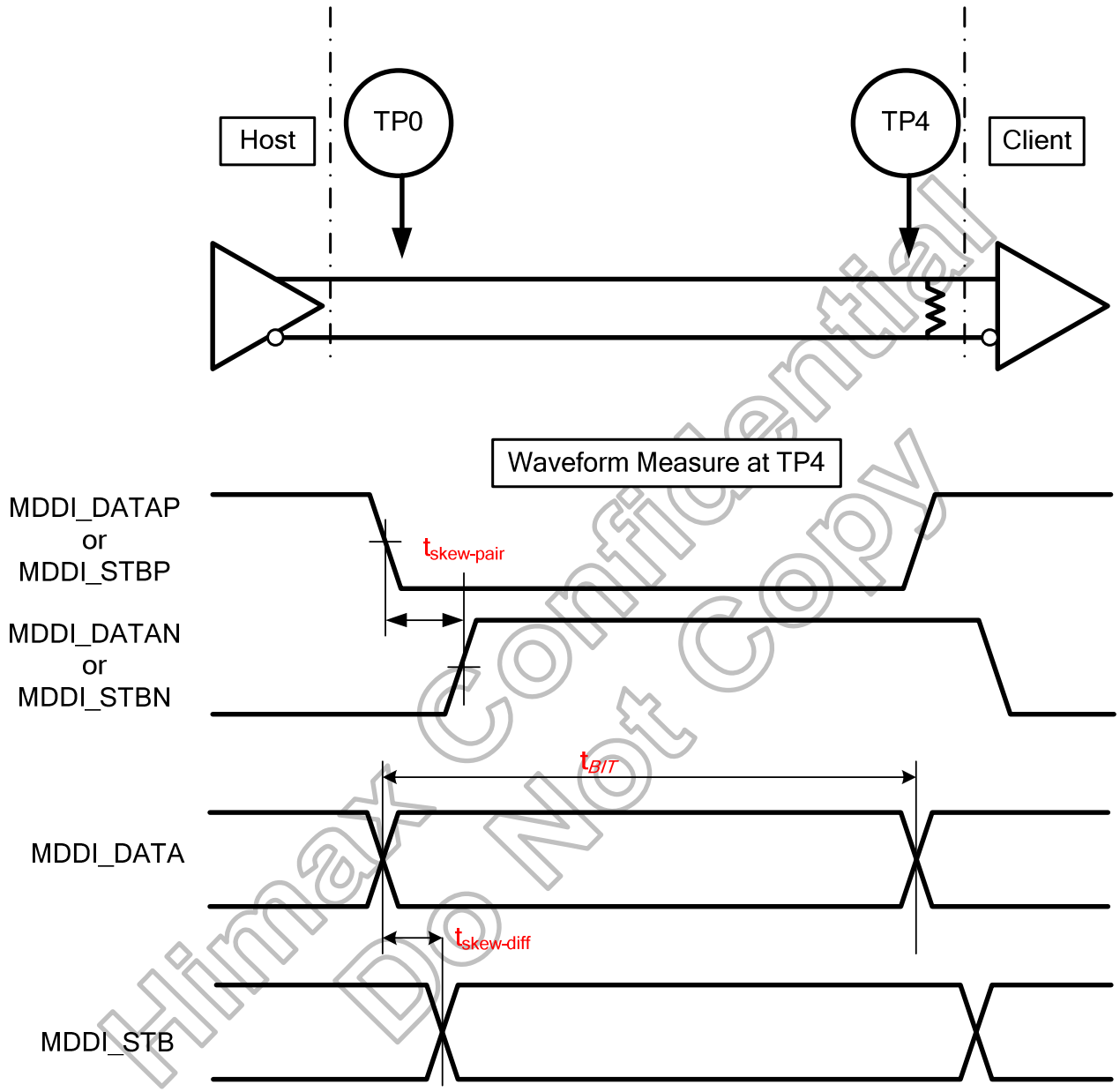
Table 8.10: Reset timing

8.4.6 MDDI electrical characteristics

8.4.6.1 DC characteristic

Parameter	Description	Min.	Typ.	Max.	Unit
V_{IT+}	Receiver differential input high threshold voltage. Above this differential voltage the input signal shall be interpreted as a logic-one level.	-	0	50	mV
V_{IT-}	Receiver differential input low threshold voltage. Below this differential voltage the input signal shall be interpreted as a logic-zero level.	-50	0	-	-
V_{IT+_hib}	Receiver differential input high threshold voltage (offset for hibernation wake-up). Above this differential voltage the input signal shall be interpreted as a logic-one level.	-	100	125	mV
V_{IT-_hib}	Receiver differential input low threshold voltage (offset for hibernation wake-up). Below this differential voltage the input signal shall be interpreted as a logic-zero level.	75	100	-	mV
$V_{Input-Range}$	Allowable receiver input voltage range with respect to client ground.	0. 5	-	1.2	V

8.4.6.2 AC characteristic

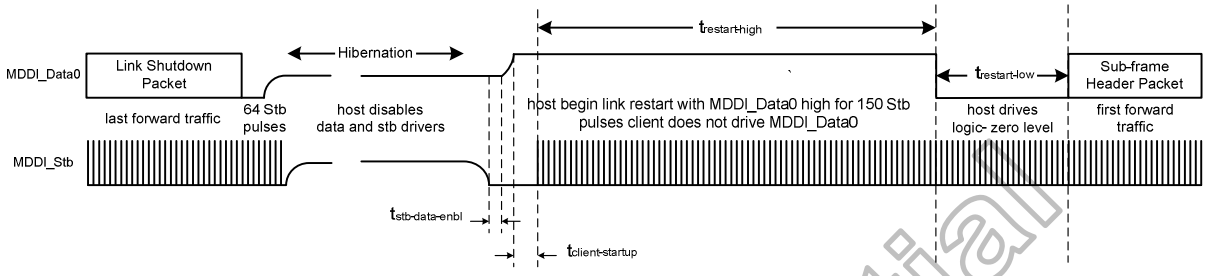


Parameter	Description	Min.	Typ.	Max.	Unit
$1/t_{BIT}$	MDDI operate speed	50	350	400	Mbps
$t_{skew-pair}$	Skew between positive and negative inputs of the differential receiver of the same differential pair (intra-pair skew)	-0.05	0	0.05	ns
$t_{skew-diff}$	Peak delay skew between one differential pair and any other differential pair	-0.45 t_{BIT}	0	0.45 t_{BIT}	ns
$t_{Rise-Fall}$	Rise/Fall time(20%-80% of swing)	200	-	Note(1)	ps

Note : The maximum rise and fall time is either 35% of the interval to transmit one bit on one differential pair or 100 nsec, hichever is smaller.

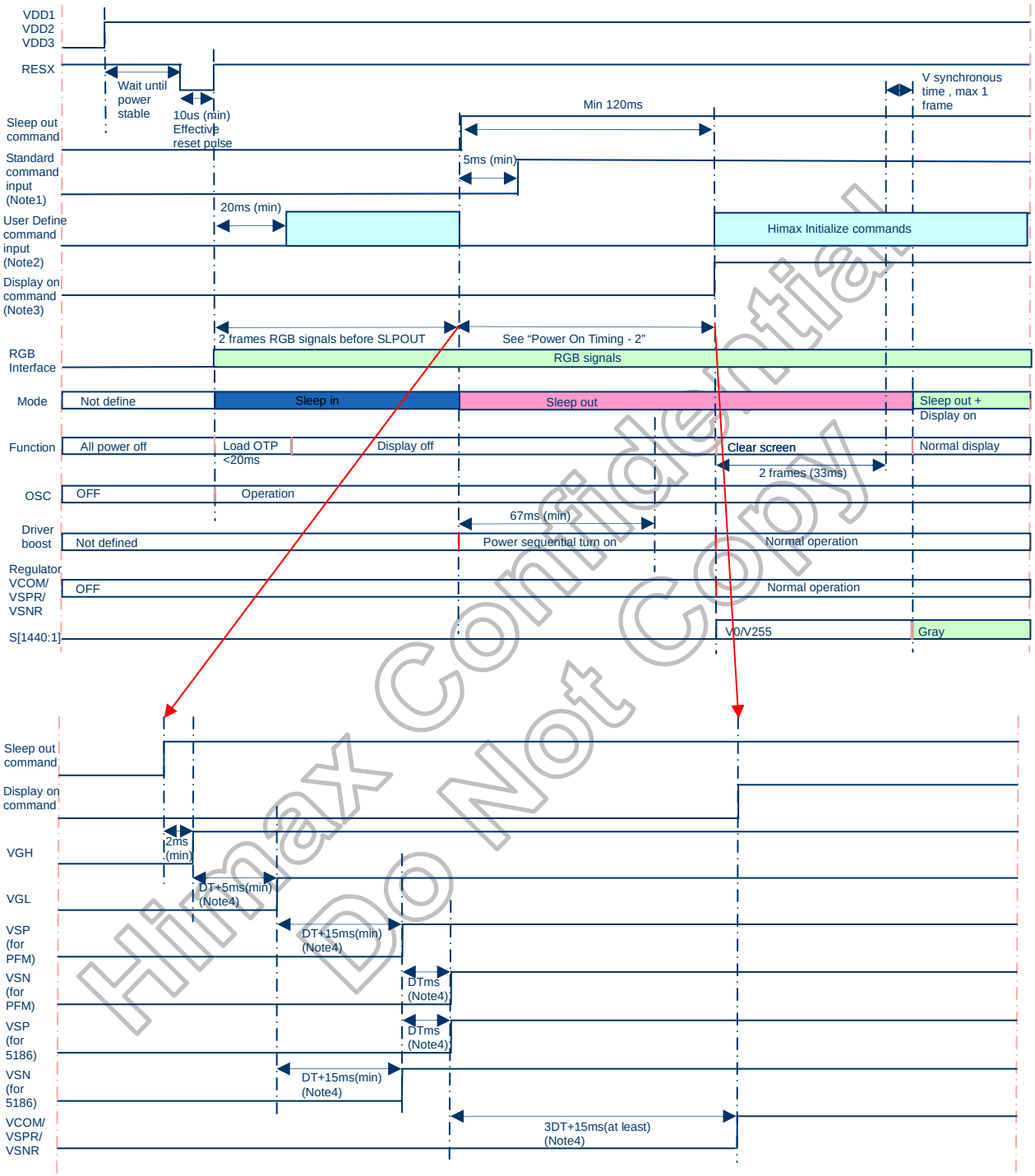
8.4.6.3 DC characteristic

Host-Initiated Wake-up



Parameter	Description	Min.	Typ.	Max.	Unit
$t_{restart-high}$	Duration of host link restart high pulse	140	150	250	Stb clock
$t_{restart-low}$	Duration of host link restart low pulse	50	50	50	Stb clock
$t_{stb-data-enbl}$	MDDI_Stb completely enabled to MDDI_Data0 enabled	0	-	-	µsec
$t_{client-startup}$	Time for host to hold MDDI_Stb at logic-zero level after MDDI_Data0 reaches logic-high level	200	-	-	nsec

8.4.7 DPI Interface Power On/Off Timing



Note1:
"Standard" command except "01h" & "10h" command must wait 5ms after "Sleep out" command then can be sent. "01h" & "10h" command must wait 100ms after "Sleep out" command then can be sent.

Note2:
"User Define" command must be sent "B9h" first then other commands can be available.

Note3:
"Display on" command must send after "User Define" command or at the same time.

Note4:

DT[1:0]:Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence on
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

Default DT=5ms

Figure 8.8 Power On Timing

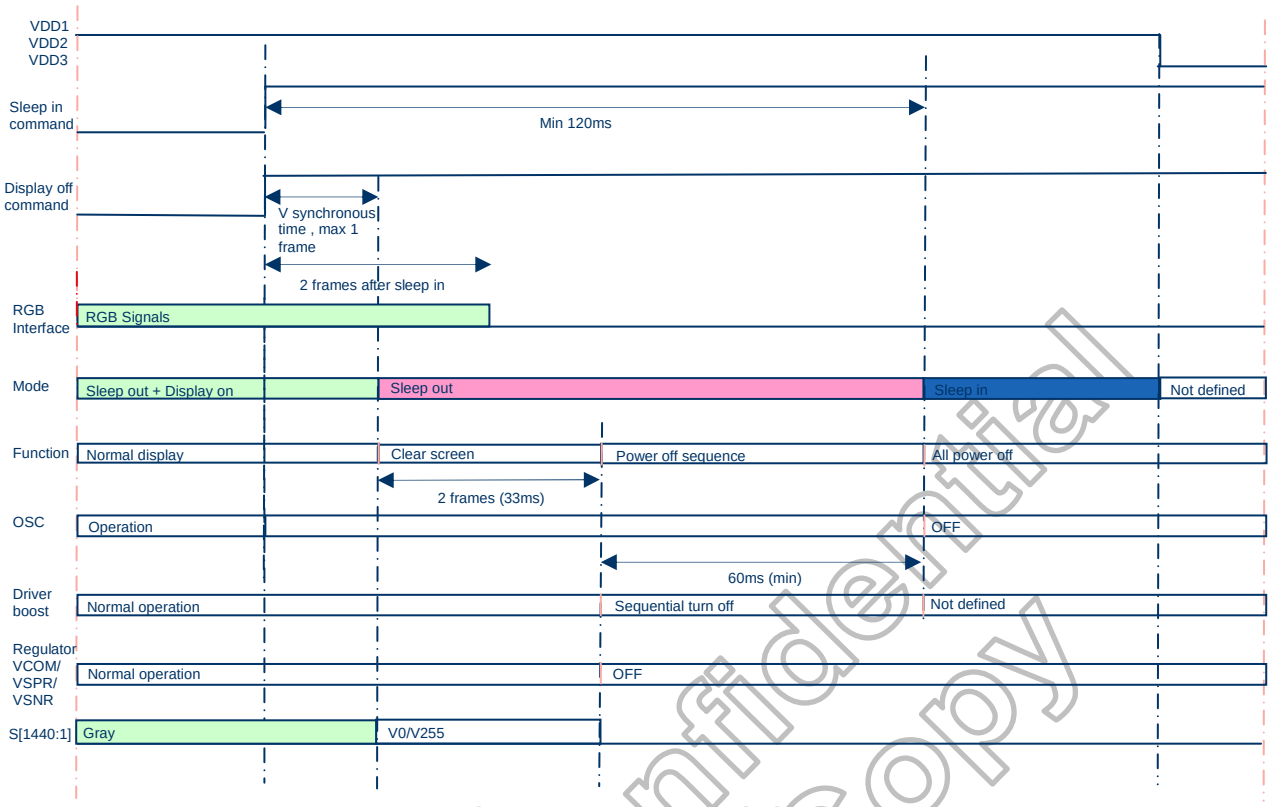


Figure 8.9 Power Off Timing

8.4.8 DSI D-PHY electrical characteristics

8.4.8.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI - PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.10 shows the complete set of electrical functions required for a fully featured PHY transceiver.

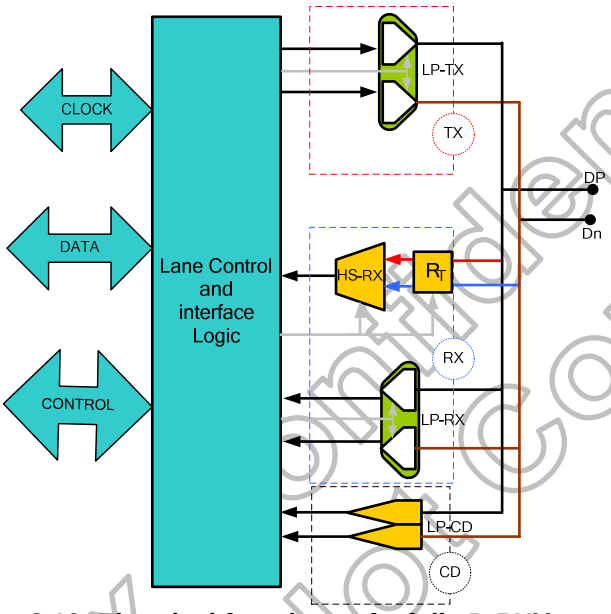


Figure 8.10: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. The Figure 8.11shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

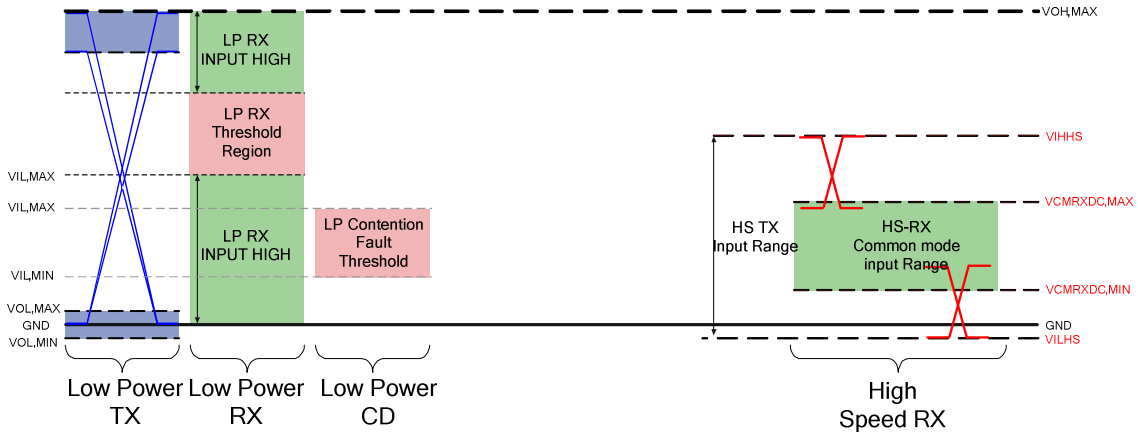


Figure 8.11: Shows both the HS and LP signal levels

8.4.8.2 The Electrical Characteristics of Low-Power Transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min	Nom	Max	Units	Note
V_{OL}	Thevenin output low level	-50		50	mV	
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
Z_{OLP}	Output impedance of LP-TX	110			Ω	1

Note: Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.11: LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
$t_{RLP}/_{tFLP}$	15%-85% rise time and fall time	-	-	25	ns	1
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	-	-	500	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	1, 3, 5, 6
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	1, 2, 3
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	1, 3, 7
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST – 700)	-	-	mV/ns	1, 8, 9
C_{LOAD}	Load capacitance	-	-	70	pF	

Note:
1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 400 mV and 930 mV.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
5. This value represents a corner point in a piecewise linear curve.
6. When the output voltage is in the range specified by $V_{PIN(absmax)}$.
7. When the output voltage is between 400 mV and 700 mV.
8. Where $V_{O,INST}$ is the instantaneous output voltage, V_{DP} or V_{DN}, in millivolts.
9. When the output voltage is between 700 mV and 930 mV.

Table 8.12: LP Transmitter AC Specifications

8.4.8.3 The Electrical Characteristics of Receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

8.4.8.4 High-Speed Receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, ZID, between the positive input pin Dp and the negative input pin Dn. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min	Nom	Max	Units	Note
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{ILHS}	Single-ended input low voltage	-40			mV	1
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{CMRXDC}	Common-mode voltage HS receive mode	70		330	mV	1, 2
Z_{ID}	Differential input impedance	80	100	125	Ω	

NOTE:
1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.13: HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz			100	mV_{PP}	1
C_{CM}	Common mode termination			60	pF	2

Note:
1. ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
2. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.14: HS Receiver AC Specifications

8.4.8.5 Low-Power Receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSPIKE. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.10 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

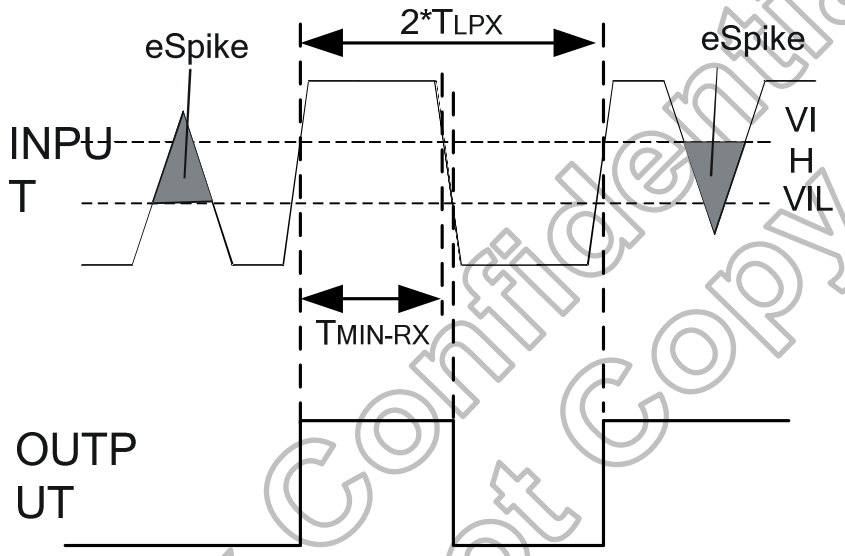


Figure 8.12: Input Glitch Rejections of Low-Power Receivers

Parameter	Description	Min	Nom	Max	Units	Note
V_{IL}	Logic 0 input threshold			550	mV	
V_{IH}	Logic 1 input threshold	880			mV	

Table 8.15: LP Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
e_{SPIKE}	Input pulse rejection			300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20			ns	4
V_{INT}	Peak-to-peak interference voltage			200	mV	
f_{INT}	Interference frequency	450			MHz	

Note:
1. Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

Table 8.16: LP Receiver AC Specifications

8.4.8.6 Line Contention Detection

Contention can be inferred from any of the following conditions:

1. An LP high fault shall be detected when the LP transmitter is driving high.

2. An LP low fault shall be detected when the LP transmitter is driving low.

Parameter	Description	Min	Nom	Max	Units	Note
V_{IHCD}	Logic 1 contention threshold	450			mV	
V_{ILCD}	Logic 0 contention threshold			200	mV	

Table 8.17: Contention Detector DC Specifications

8.4.8.7 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times.

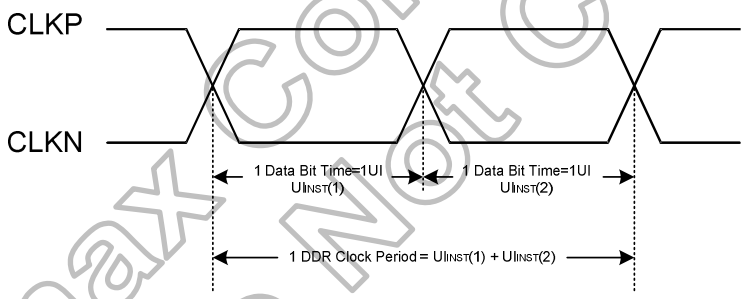


Figure 8.13: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

Parameter	Symbol	Min	Nom	Max	Unit	Note
UI instantaneous	UI_{INST}	2		12.5	ns	1, 2

Note:
1. This value corresponds to a maximum 500 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

Table 8.18: HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

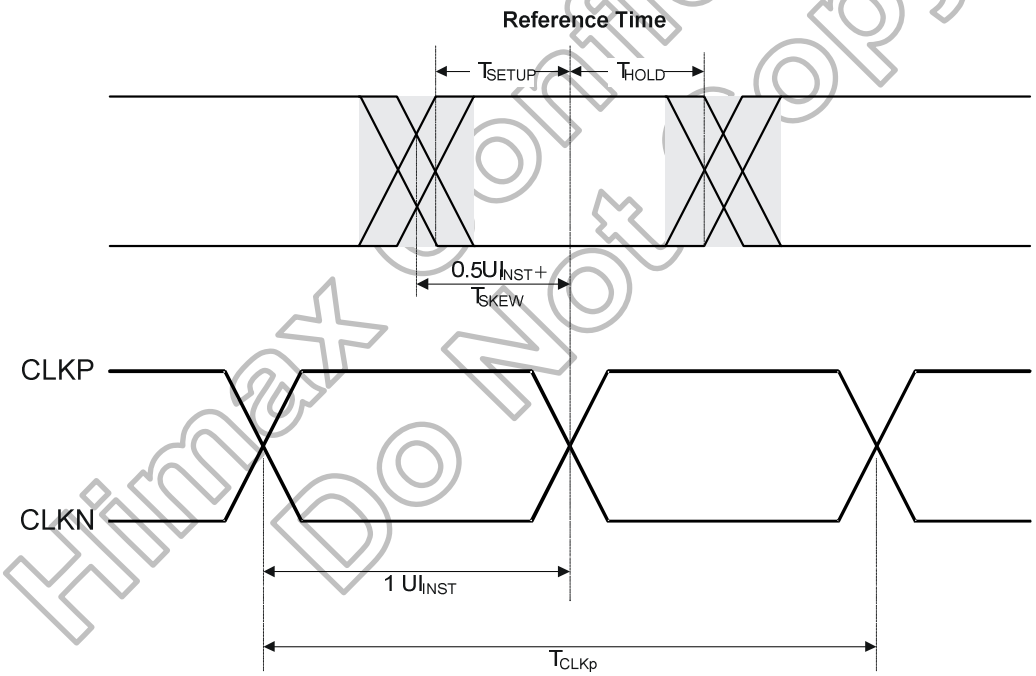


Figure 8.14: Data to Clock Timing Definitions

8.4.8.8 Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UIINST,MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, TSKEW[TX], is the allowed deviation of the data launch time to the ideal ½UIINST displaced quadrature clock edge. The setup and hold times, TSETUP[RX] and THOLD[RX], respectively, describe the timing relationships between the data and clock signals. TSETUP[RX] is the minimum time that data shall be present before a rising or falling clock edge and THOLD[RX] is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*UIINST, i.e. ±0.2*UIINST for degradation contributed by the interconnect.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15			UIINST	1
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15			UIINST	1

Note:
1. Total setup and hold window for receiver of 0.3*UI_{INST}.

Table 8.19: Data to Clock Timing Specifications

9. Layout Recommendation

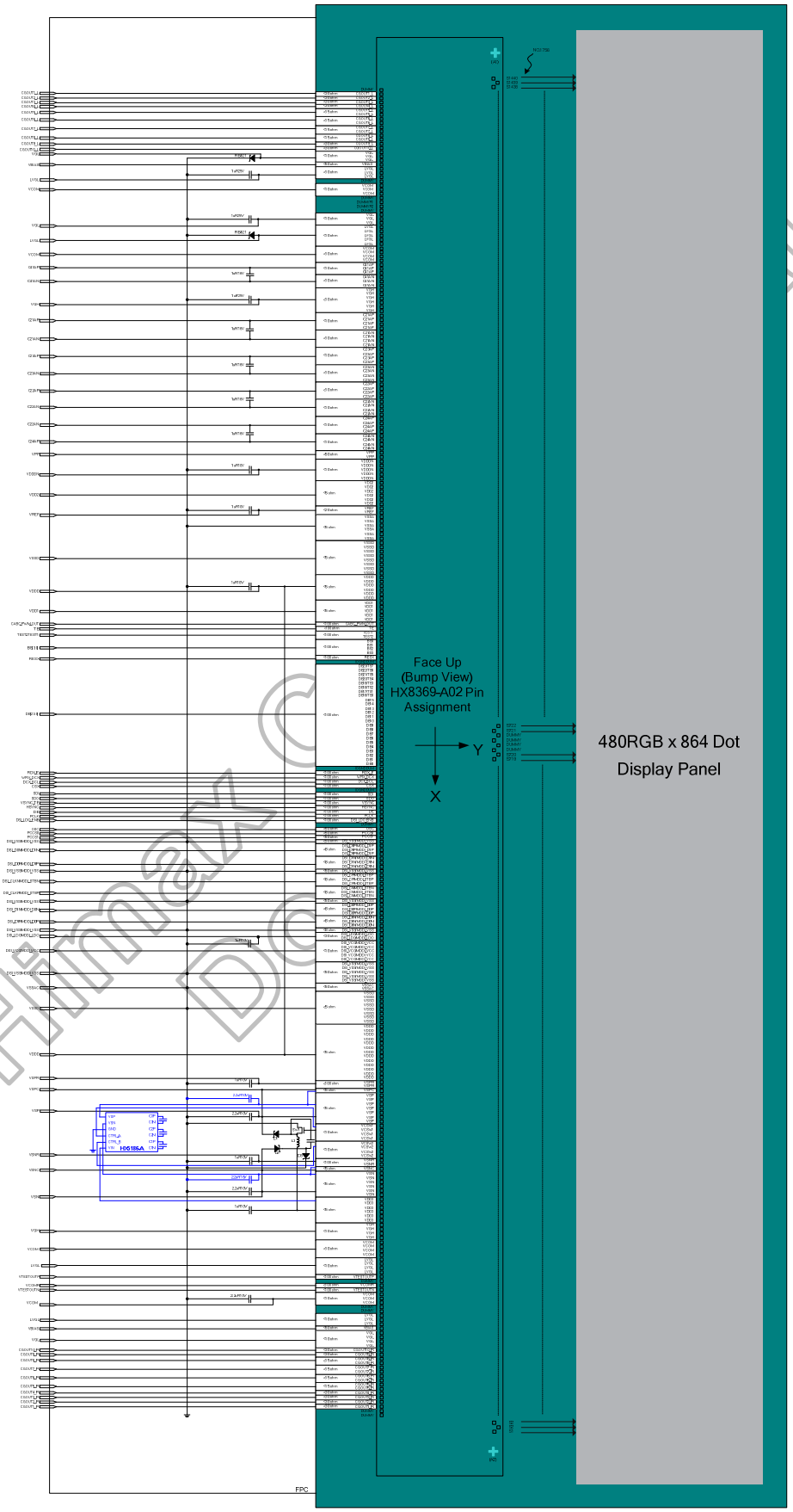


Figure 9.1: Layout recommendation

10. Maximum Layout Resistance

Name	Type	Maximum series resistance	Unit
VDD1	Power supply	10	Ω
VDD2	Power supply	20	Ω
VDD3	Power supply	10	Ω
VSSD	Power supply	10	Ω
VSSA	Power supply	10	Ω
DSI_VCC / MDDI_VCC	Power supply	10	Ω
DSI_VSS / MDDI_VSS	Power supply	10	Ω
VSSAC	Power supply	20	Ω
VPP	Input	10	Ω
PCCS0, PCCS1	Input	50	Ω
VCSW1, VCSW2	Output	30	Ω
BS[3:0]	Input	100	Ω
RDX_E, WRX_DCX, DCX_SCL, CSX, RESX	Input	100	Ω
HSYNC, VSYNC, DE, PCLK	Input	100	Ω
SDI	Input	100	Ω
SDO	Output	100	Ω
DB[23:0]	Output	100	Ω
CABC_PWM_OUT	Output	100	Ω
VCOM	Output	10	Ω
DSI_D0P / MDDI_D0P	Input + Output	8	Ω
DSI_D0N / MDDI_D0N	Input + Output	8	Ω
DSI_CLKP / MDDI_STBP	Input	8	Ω
DSI_CLKN / MDDI_STBN	Input	8	Ω
DSI_D1P / MDDI_D1P	Input	8	Ω
DSI_D1N / MDDI_D1N	Input	8	Ω
VDDD	Capacitor Connection	5	Ω
VDDDN	Capacitor Connection	50	Ω
VSP, VSN	Capacitor Connection	10	Ω
VSPC, VSNC	Capacitor Connection	50	Ω
VSPR, VSNR	Capacitor Connection	50	Ω
VREF	Capacitor Connection	20	Ω
VGL, LVGL	Capacitor Connection	10	Ω
VGH	Capacitor Connection	10	Ω
DSI_LDO/MDDI_LDO	Capacitor Connection	20	Ω
DSI_LDO_ENB	Input	100	Ω
OSC	Input	100	Ω
C21AP,C21AN,C22AP,C22AN, C23AP,C23AN,C24AP,C24AN, C41AP,C41AN,	Capacitor Connection	10	Ω
TEST[2:1]	Input	100	Ω
TE	Output	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω
VBIAS	Output	50	Ω
VCOMR	Input	100	Ω
CGOUT1~10_L CGOUT1~10_R	Output	30	Ω

Table 10.1: Maximum layout resistance

11. Ordering Information

Part No.	Package
HX8369-A02 PDxxx	PD: mean COG xxx: mean chip thickness (μm), (default: 250 μm)

12. Revision History

Version	Date	Description of Changes
01	2011/10/20	1. New setup