**Features**

- Operating voltage: 2.7V~5.2V
- Built-in RC oscillator
- External 32.768kHz crystal or 32kHz frequency source input
- 1/4 bias, 1/8 duty, frame frequency is 64Hz
- Max. 48×8 patterns, 8 commons, 48 segments
- Built-in internal resistor type bias generator
- 3-wire serial interface
- 8 kinds of time base or WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Two selection buzzer frequencies (2kHz or 4kHz)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- VLCD pin to adjust LCD operating voltage
- Cascade application
- 100-pin QFP package

**General Description**

HT1623 is a peripheral device specially designed for I/O type MCU used to expand the display capability. The max. display segment of the device are 384 patterns (48×8). It also supports serial interface, buzzer sound, watchdog timer or time base timer functions. The HT1623 is a memory mapping and multi-function LCD controller. The software configuration feature of the HT1623 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only three lines are required for the interface between the host controller and the HT1623. The HT162X series have many kinds of products that match various applications.

**Selection Table**

<table>
<thead>
<tr>
<th>HT162X</th>
<th>HT1620</th>
<th>HT1621</th>
<th>HT1622</th>
<th>HT16220</th>
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<td>√</td>
<td>√</td>
<td>—</td>
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**Block Diagram**
* The IC substrate should be connected to VDD in the PCB layout artwork.
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<th>Pad No.</th>
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Pad Description

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<th>Pad Name</th>
<th>I/O</th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>CS</td>
<td>I</td>
<td>Chip selection input with pull-high resistor. When the CS is logic high, the data and command read from or written to the HT1623 are disabled. The serial interface circuit is also reset. But if the CS is at logic low level and is input to the CS pad, the data and command transmission between the host controller and the HT1623 are all enabled.</td>
</tr>
<tr>
<td>2</td>
<td>RD</td>
<td>I</td>
<td>READ clock input with pull-high resistor. Data in the RAM of the HT1623 are clocked out on the falling edge of the RD signal. The clocked out data will appear on the data line. The host controller can use the next rising edge to latch the clocked out data.</td>
</tr>
<tr>
<td>3</td>
<td>WR</td>
<td>I</td>
<td>WRITE clock input with pull-high resistor. Data on the DATA line are latched into the HT1623 on the rising edge of the WR signal.</td>
</tr>
<tr>
<td>4</td>
<td>DATA</td>
<td>I/O</td>
<td>Serial data input or output with pull-high resistor</td>
</tr>
<tr>
<td>5</td>
<td>VSS</td>
<td>—</td>
<td>Negative power supply, ground</td>
</tr>
<tr>
<td>6</td>
<td>OSCI</td>
<td>I</td>
<td>The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.</td>
</tr>
<tr>
<td>7</td>
<td>OSCO</td>
<td>O</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>VDD</td>
<td>—</td>
<td>Positive power supply</td>
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<tr>
<td>9</td>
<td>VLCD</td>
<td>I</td>
<td>LCD operating voltage input pad.</td>
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<tr>
<td>10</td>
<td>IRQ</td>
<td>O</td>
<td>Time base or watchdog timer overflow flag, NMOS open drain output</td>
</tr>
<tr>
<td>11, 12</td>
<td>BZ, B2</td>
<td>O</td>
<td>2kHz or 4kHz tone frequency output pair</td>
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<tr>
<td>13–15</td>
<td>T1–T3</td>
<td>I</td>
<td>Not connected</td>
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<tr>
<td>16–23</td>
<td>COM0–COM7</td>
<td>O</td>
<td>LCD common outputs</td>
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<tr>
<td>24–71</td>
<td>SEG0–SEG47</td>
<td>O</td>
<td>LCD segment outputs</td>
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</table>

Absolute Maximum Ratings

Supply Voltage: \(-0.3\text{V} \text{ to } 5.5\text{V}\)  
Storage Temperature: \(-50^\circ\text{C} \text{ to } 125^\circ\text{C}\)  
Input Voltage: \(\text{VSS} = 0.3\text{V} \text{ to } \text{VDD} + 0.3\text{V}\)  
Operating Temperature: \(25^\circ\text{C} \text{ to } 75^\circ\text{C}\)

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Rev. 1.10 5 September 11, 2002
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
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<tr>
<td>VDD</td>
<td>Operating Voltage</td>
<td>3V</td>
<td>No load or LCD ON</td>
<td>On-chip RC oscillator</td>
<td>2.7</td>
<td>5.2</td>
<td>V</td>
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<td>IDD1</td>
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<td>310</td>
<td>µA</td>
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<td>No load or LCD ON</td>
<td>Crystal oscillator</td>
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<td>310</td>
<td>µA</td>
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<td>IDD11</td>
<td>Operating Current</td>
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<td>30</td>
<td>µA</td>
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<td>Operating Current</td>
<td>3V</td>
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<td>Crystal oscillator</td>
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<td>VIL</td>
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<tr>
<td>IOL1</td>
<td>BZ, BZ</td>
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<td>mA</td>
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### A.C. Characteristics

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<th>Max.</th>
<th>Unit</th>
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<td>System Clock</td>
<td>3V</td>
<td>On-chip RC oscillator</td>
<td>22</td>
<td>32</td>
<td>40</td>
<td>kHz</td>
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<td>System Clock</td>
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<td>External clock source</td>
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<td>LCD Frame Frequency</td>
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<td>External clock source</td>
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<td>LCD Frame Frequency</td>
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<td>Hz</td>
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<td>( t_{COM} )</td>
<td>LCD Common Period</td>
<td>—</td>
<td>n: Number of COM</td>
<td>—</td>
<td>n/( f_{LCD} )</td>
<td>—</td>
<td>sec</td>
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<td>Serial Data Clock (WR Pin)</td>
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<td>—</td>
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<td>kHz</td>
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<tr>
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<td>—</td>
<td>300</td>
<td>kHz</td>
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<tr>
<td>( f_{CLK2} )</td>
<td>Serial Data Clock (RD Pin)</td>
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<td>Duty cycle 50%</td>
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<td>—</td>
<td>75</td>
<td>kHz</td>
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<td>—</td>
<td>—</td>
<td>150</td>
<td>kHz</td>
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<td>( t_{CS} )</td>
<td>Serial Interface Reset Pulse Width (Figure 3)</td>
<td>—</td>
<td>CS</td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>WR, RD Input Pulse Width (Figure 1)</td>
<td>3V</td>
<td>Write mode</td>
<td>3.34</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>WR, RD Input Pulse Width (Figure 1)</td>
<td>5V</td>
<td>Read mode</td>
<td>6.67</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>WR, RD Input Pulse Width (Figure 1)</td>
<td>5V</td>
<td>Write mode</td>
<td>1.67</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>WR, RD Input Pulse Width (Figure 1)</td>
<td>5V</td>
<td>Read mode</td>
<td>3.34</td>
<td>—</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>( t_{RU} )</td>
<td>Rise/Fall Time Serial Data Clock Width (Figure 1)</td>
<td>3V</td>
<td>—</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{RU} )</td>
<td>Rise/Fall Time Serial Data Clock Width (Figure 1)</td>
<td>5V</td>
<td></td>
<td>—</td>
<td>—</td>
<td>120</td>
<td>—</td>
</tr>
<tr>
<td>( t_{SU} )</td>
<td>Setup Time DATA to WR, RD Clock Width (Figure 2)</td>
<td>3V</td>
<td>—</td>
<td>—</td>
<td>120</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SU} )</td>
<td>Setup Time DATA to WR, RD Clock Width (Figure 2)</td>
<td>5V</td>
<td></td>
<td>—</td>
<td>—</td>
<td>120</td>
<td>—</td>
</tr>
<tr>
<td>( t_{SU1} )</td>
<td>Setup Time for CS to WR, RD Clock Width (Figure 3)</td>
<td>3V</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SU1} )</td>
<td>Setup Time for CS to WR, RD Clock Width (Figure 3)</td>
<td>5V</td>
<td></td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>—</td>
</tr>
<tr>
<td>( t_{H} )</td>
<td>Hold Time for CS to WR, RD Clock Width (Figure 3)</td>
<td>3V</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{H} )</td>
<td>Hold Time for CS to WR, RD Clock Width (Figure 3)</td>
<td>5V</td>
<td></td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>—</td>
</tr>
</tbody>
</table>

---

**Figure 1**

**Figure 2**

**Figure 3**
**Functional Description**

**Display memory – RAM structure**

The static display RAM is organized into 96×4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

**Time base and watchdog timer – WDT**

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and IRQ EN/DIS are independent from each other. Once the WDT time-out occurs, the IRQ pin will remain at logic low level until the CLR WDT or the IRQ DIS command is issued.

If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

**Buzzer tone output**

A simple tone generator is implemented in the HT1623. The tone generator can output a pair of differential driving signals on the BZ and BZ which are used to generate a single tone.

**Command format**

The HT1623 can be configured by the software setting. There are two mode commands to configure the HT1623 resource and to transfer the LCD display data.

---

**RAM mapping**

<table>
<thead>
<tr>
<th>COM7</th>
<th>COM6</th>
<th>COM5</th>
<th>COM4</th>
<th>COM3</th>
<th>COM2</th>
<th>COM1</th>
<th>COM0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEG0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEG1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEG2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEG3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SEG4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>Addr</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
</tr>
</tbody>
</table>

Data 4 Bits (D3, D2, D1, D0)

---

**Timer and WDT configurations**
The following are the data mode ID and the command mode ID:

<table>
<thead>
<tr>
<th>Operation</th>
<th>Mode</th>
<th>ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>Data</td>
<td>110</td>
</tr>
<tr>
<td>WRITE</td>
<td>Data</td>
<td>101</td>
</tr>
<tr>
<td>READ-MODIFY-WRITE</td>
<td>Data</td>
<td>101</td>
</tr>
<tr>
<td>COMMAND</td>
<td>Command</td>
<td>100</td>
</tr>
</tbody>
</table>

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CS pin should be set to "1" and the previous operation mode will be reset also. The CS pin returns to "0", a new operation mode ID should be issued first.

<table>
<thead>
<tr>
<th>Name</th>
<th>Command Code</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>TONE OFF</td>
<td>0000-1000-X</td>
<td>Turn-off tone output</td>
</tr>
<tr>
<td>TONE 4K</td>
<td>010X-XXXX-X</td>
<td>Turn-on tone output, tone frequency is 4kHz</td>
</tr>
<tr>
<td>TONE 2K</td>
<td>0110-XXXX-X</td>
<td>Turn-on tone output, tone frequency is 2kHz</td>
</tr>
</tbody>
</table>

Timing Diagrams

READ mode (command code : 110)

![_timing_diagram_read_mode]

READ mode (successive address reading)

![_timing_diagram_successive_address]

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**WRITE mode (command code: 1 0 1)**

<table>
<thead>
<tr>
<th>CS</th>
<th>WR</th>
<th>DATA</th>
</tr>
</thead>
</table>
|    |    |!

**WRITE mode (successive address writing)**

<table>
<thead>
<tr>
<th>CS</th>
<th>WR</th>
<th>DATA</th>
</tr>
</thead>
</table>
|    |    |!

**READ-MODIFY-WRITE mode (command code: 1 0 1)**

<table>
<thead>
<tr>
<th>CS</th>
<th>WR</th>
<th>RD</th>
<th>DATA</th>
</tr>
</thead>
</table>
|    |    |    |!

**READ-MODIFY-WRITE mode (successive address accessing)**

<table>
<thead>
<tr>
<th>CS</th>
<th>WR</th>
<th>RD</th>
<th>DATA</th>
</tr>
</thead>
</table>
|    |    |    |!
Command mode (command code: 100)

Mode (data and command mode)
Application Circuits

Note: The connection of IRQ and RD pin can be selected depending on the requirement of the MCU. The voltage applied to VLCD pin must be lower than VDD. Adjust VR to fit LCD display, at VDD=5V, VLCD=4V, VR=15kΩ±20%. Adjust R (external pull-high resistance) to fit user’s time base clock.

Command Summary

<table>
<thead>
<tr>
<th>Name</th>
<th>ID</th>
<th>Command Code</th>
<th>D/C</th>
<th>Function</th>
<th>Def.</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>110</td>
<td>A6A5A4A3A2A1A0D0D1D2D3</td>
<td>D</td>
<td>Read data from the RAM</td>
<td></td>
</tr>
<tr>
<td>WRITE</td>
<td>101</td>
<td>A6A5A4A3A2A1A0D0D1D2D3</td>
<td>D</td>
<td>Write data to the RAM</td>
<td></td>
</tr>
<tr>
<td>READ-MODIFY-WRITE</td>
<td>101</td>
<td>A6A5A4A3A2A1A0D0D1D2D3</td>
<td>D</td>
<td>Read and Write data to the RAM</td>
<td></td>
</tr>
<tr>
<td>SYS DIS</td>
<td>100</td>
<td>0000-0000-X</td>
<td>C</td>
<td>Turn off both system oscillator and LCD bias</td>
<td>Yes</td>
</tr>
<tr>
<td>SYS EN</td>
<td>100</td>
<td>0000-0001-X</td>
<td>C</td>
<td>Turn on system oscillator</td>
<td></td>
</tr>
<tr>
<td>LCD OFF</td>
<td>100</td>
<td>0000-0010-X</td>
<td>C</td>
<td>Turn off LCD display</td>
<td>Yes</td>
</tr>
<tr>
<td>LCD ON</td>
<td>100</td>
<td>0000-0011-X</td>
<td>C</td>
<td>Turn on LCD display</td>
<td></td>
</tr>
<tr>
<td>TIMER DIS</td>
<td>100</td>
<td>0000-0100-X</td>
<td>C</td>
<td>Disable time base output</td>
<td>Yes</td>
</tr>
<tr>
<td>WDT DIS</td>
<td>100</td>
<td>0000-0101-X</td>
<td>C</td>
<td>Disable WDT time-out flag output</td>
<td>Yes</td>
</tr>
<tr>
<td>TIMER EN</td>
<td>100</td>
<td>0000-0110-X</td>
<td>C</td>
<td>Enable time base output</td>
<td></td>
</tr>
<tr>
<td>WDT EN</td>
<td>100</td>
<td>0000-0111-X</td>
<td>C</td>
<td>Enable WDT time-out flag output</td>
<td></td>
</tr>
<tr>
<td>TONE OFF</td>
<td>100</td>
<td>0000-1000-X</td>
<td>C</td>
<td>Turn off tone outputs</td>
<td></td>
</tr>
<tr>
<td>CLR TIMER</td>
<td>100</td>
<td>0000-1101-X</td>
<td>C</td>
<td>Clear the contents of the time base generator</td>
<td></td>
</tr>
<tr>
<td>CLR WDT</td>
<td>100</td>
<td>0000-1111-X</td>
<td>C</td>
<td>Clear the contents of the WDT stage</td>
<td></td>
</tr>
<tr>
<td>RC 32K</td>
<td>100</td>
<td>0001-10XX-X</td>
<td>C</td>
<td>System clock source, on-chip RC oscillator</td>
<td>Yes</td>
</tr>
<tr>
<td>EXT (XTAL) 32K</td>
<td>100</td>
<td>0001-11XX-X</td>
<td>C</td>
<td>System clock source, external 32kHz clock</td>
<td></td>
</tr>
<tr>
<td>TONE 4K</td>
<td>100</td>
<td>010X-XXXX-X</td>
<td>C</td>
<td>Tone frequency output: 4kHz</td>
<td></td>
</tr>
<tr>
<td>Name</td>
<td>ID</td>
<td>Command Code</td>
<td>D/C</td>
<td>Function</td>
<td>Def.</td>
</tr>
<tr>
<td>---------</td>
<td>----</td>
<td>--------------------</td>
<td>-----</td>
<td>-----------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>TONE 2K</td>
<td>100</td>
<td>0110-XXXX-X</td>
<td>C</td>
<td>Tone frequency output: 2kHz</td>
<td></td>
</tr>
<tr>
<td>IRQ DIS</td>
<td>100</td>
<td>100X-0XXX-X</td>
<td>C</td>
<td>Disable IRQ output</td>
<td>Yes</td>
</tr>
<tr>
<td>IRQ EN</td>
<td>100</td>
<td>100X-1XXX-X</td>
<td>C</td>
<td>Enable IRQ output</td>
<td></td>
</tr>
<tr>
<td>F1</td>
<td>100</td>
<td>101X-0000-X</td>
<td>C</td>
<td>Time base clock output: 1Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 4s</td>
<td></td>
</tr>
<tr>
<td>F2</td>
<td>100</td>
<td>101X-0001-X</td>
<td>C</td>
<td>Time base clock output: 2Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 2s</td>
<td></td>
</tr>
<tr>
<td>F4</td>
<td>100</td>
<td>101X-0010-X</td>
<td>C</td>
<td>Time base clock output: 4Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 1s</td>
<td></td>
</tr>
<tr>
<td>F8</td>
<td>100</td>
<td>101X-0011-X</td>
<td>C</td>
<td>Time base clock output: 8Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 1/2s</td>
<td></td>
</tr>
<tr>
<td>F16</td>
<td>100</td>
<td>101X-0100-X</td>
<td>C</td>
<td>Time base clock output: 16Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 1/4s</td>
<td></td>
</tr>
<tr>
<td>F32</td>
<td>100</td>
<td>101X-0101-X</td>
<td>C</td>
<td>Time base clock output: 32Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 1/8s</td>
<td></td>
</tr>
<tr>
<td>F64</td>
<td>100</td>
<td>101X-0110-X</td>
<td>C</td>
<td>Time base clock output: 64Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 1/16s</td>
<td></td>
</tr>
<tr>
<td>F128</td>
<td>100</td>
<td>101X-0111-X</td>
<td>C</td>
<td>Time base clock output: 128Hz</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The WDT time-out flag after: 1/32s</td>
<td></td>
</tr>
<tr>
<td>TEST</td>
<td>100</td>
<td>1110-0000-X</td>
<td>C</td>
<td>Test mode, user don’t use.</td>
<td></td>
</tr>
<tr>
<td>NORMAL</td>
<td>100</td>
<td>1110-0011-X</td>
<td>C</td>
<td>Normal mode</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Note: X : Don’t care
A6~A0 : RAM address
D3~D0 : RAM data
D/C : Data/Command mode
Def. : Power on reset default

All the bold forms, namely 110, 101, and 100, are mode commands. Of these, 100 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base or WDT clock frequency can be derived from an on-chip 32kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 32kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the HT1623 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1623.
Package Information
100-pin QFP (14-20) outline dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Dimensions in mm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td>A</td>
<td>18.50</td>
</tr>
<tr>
<td>B</td>
<td>13.90</td>
</tr>
<tr>
<td>C</td>
<td>24.50</td>
</tr>
<tr>
<td>D</td>
<td>19.90</td>
</tr>
<tr>
<td>E</td>
<td>—</td>
</tr>
<tr>
<td>F</td>
<td>—</td>
</tr>
<tr>
<td>G</td>
<td>2.50</td>
</tr>
<tr>
<td>H</td>
<td>—</td>
</tr>
<tr>
<td>I</td>
<td>—</td>
</tr>
<tr>
<td>J</td>
<td>1</td>
</tr>
<tr>
<td>K</td>
<td>0.10</td>
</tr>
<tr>
<td>α</td>
<td>0°</td>
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</tbody>
</table>