ILITEK
I Love Innovation

ILI9481

a-Si TFT LCD Single Chip Driver 320RGBx480 Resolution and 262K color

Datasheet

Version: V0.35
Document No.: ILI9481DS_V0.35.pdf

ILI TECHNOLOGY CORP.
8F, No. 38, Taiyuan St.,. Jhubei City, Hsinchu County 302,
Taiwan , R.O.C.
Tel.886-3-5600099; Fax.886-3-5600055
http://www.ilitek.com

Table of Contents

1. Introduction

ILI9481 is a 262,144-color single-chip SoC driver for a-TFT liquid crystal display with resolution of 320RGBx480 dots, comprising a 960-channel source driver, a 480-channel gate driver, 345,600 bytes GRAM for graphic data of 320RGBx480 dots, and power supply circuit.

The ILI9481 supports 18-/16-/9-/8-bit data bus interface (DBI) and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit RGB interface (DPI) for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9481 can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9481 also supports a function to display in 8 colors and a sleep mode, allowing for precise power control by software and these features make the ILI9481 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [320xRGB](H) x 480(V)
- Output:
  - 960 source outputs
  - 480 gate outputs
  - Common electrode output
- a-TFT LCD driver with on-chip full display RAM: 345,600 bytes
- MCU Interface
  - MIPI-DBI(Comply with MIPI DBI Version 2.00)
    Type B 16-/18- bit, 8-/9-bit
    Type C 4-line 9bit (Option 1), 8bit (Option 3)
  - 16-bits, 18-bits RGB (DPI) interface
  - MIPI DCS command sets
  - 3-pin/4-pin serial interface
- Display mode:
  - Full color mode: 262K-colors
  - Reduced color mode: 8-colors (3-bits MSB bits mode)
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
- MTP:
  - 16-bit ID1 and ID2
  - 6-bits for VCOM adjustment
- Low -power consumption architecture
  - Low operating power supplies:

- IOVcc = 1.65V ~ 3.3V (interface I/O)
- Vci = 2.5V ~ 3.3V (analog)

◆ LCD Voltage drive:

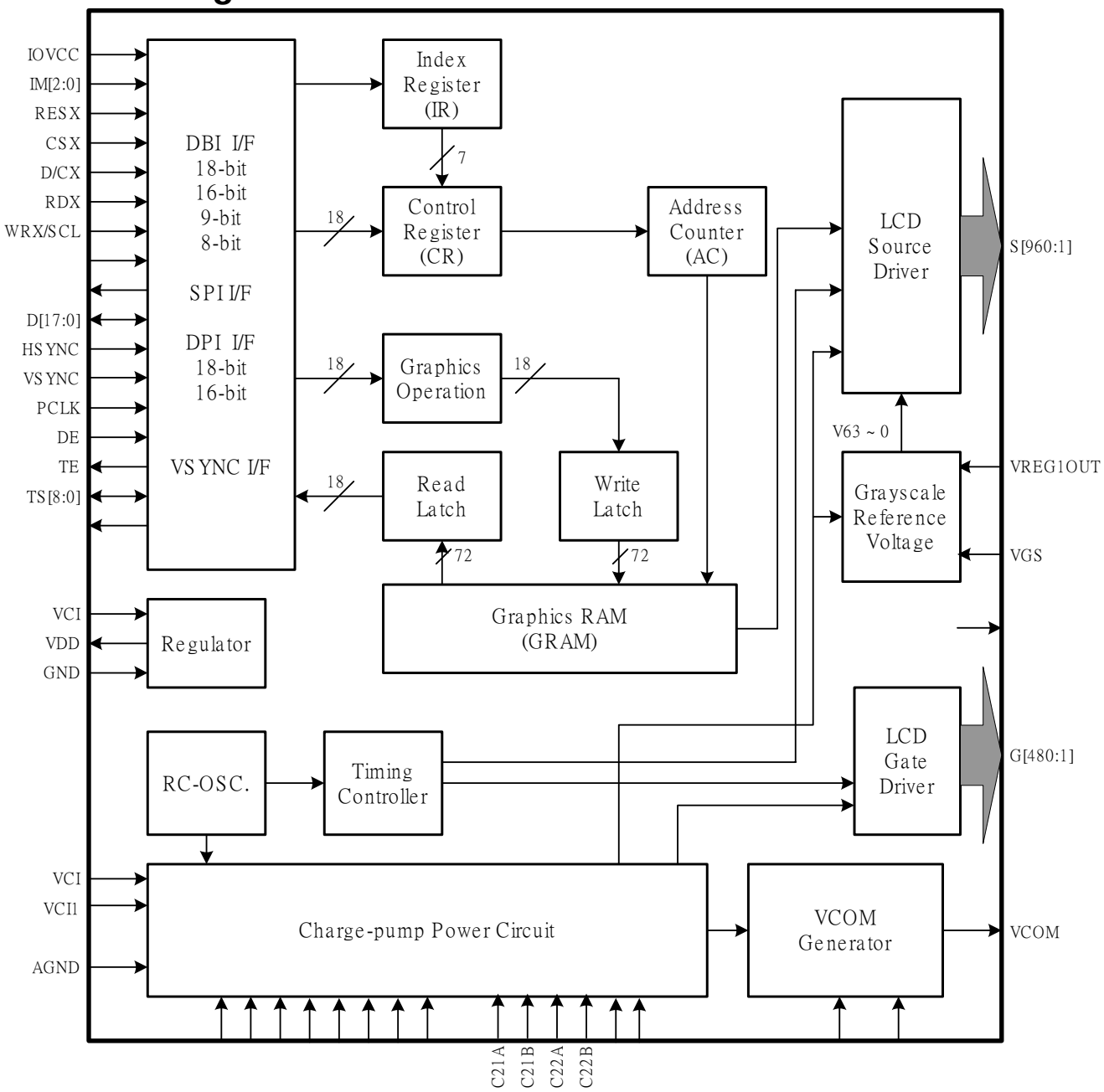
➢ Source/VCOM power supply voltage
- DDVDH - GND = 4.5V ~ 6.0V
- VCL – GND = -1.0V ~ -3.0V
- VCI – VCL ≦ 6.0V

➢ Gate driver output voltage
- VGH - GND = 10V ~ 18V
- VGL – GND = -5V ~ -12.5V
- VGH – VGL ≦ 32V

➢ VCOM driver output voltage
- VCOMH = 3.0V ~ (DDVDH-0.5)V
- VCOML = (VCL+0.5)V ~ 0V
- VCOMH-VCOML ≦ 6.0V

◆ Operate temperature range: -40℃ to 85℃

3. Block Diagram



4. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>IM[2:0]</td><td>I</td><td>Select the MPU system interface mode
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Type B 18-bit</td><td>DB[17:0]</td><td>262K</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Type B 9-bit</td><td>DB[8:0]</td><td>262K</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Type B 16-bit</td><td>DB[15:0]</td><td>65K/262K</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Type B 8-bit</td><td>DB[7:0]</td><td>65K/262K</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DBI Type C 9-bit</td><td>DIN, DOUT</td><td>8/262K</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DBI Type C 8-bit</td><td>DIN, DOUT</td><td>8/262K</td></tr>
</table></td></tr>
<tr><td>RESX</td><td>I</td><td>This signal low will reset the device and must be applied to properly initialize the chip. Signal is low active</td></tr>
<tr><td>CSX</td><td>I</td><td>Chip select input pin (“Low” enable).</td></tr>
<tr><td>D/CX</td><td>I</td><td>Display data / Command selection pin
D/CX=’1’: Display data.
D/CX=’0’: Command data.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>RDX</td><td>I</td><td>Read control pin for the DBI interface.
If not used, please connect this pin to IOVCC.</td></tr>
<tr><td>WRX/SCL</td><td>I</td><td>Write control pin for the DBI interface.
When the DBI type C is selected, this pin is used as serial clock pin.
If not used, please connect this pin to IOVCC.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>These pin are data bus.
If not used, please connect these pins to GND.</td></tr>
<tr><td>DIN/SDA</td><td>I/O</td><td>Serial data input pin and used for the DBI type C mode.
If not used, please connect this pin to ground.</td></tr>
<tr><td>DOUT</td><td>O</td><td>Serial data output pin and used for the DBI type C mode.</td></tr>
<tr><td>TE</td><td>O</td><td>Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, please open this pin.</td></tr>
<tr><td>PCLK</td><td>I</td><td>Pixel clock signal in DPI interface mode.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Vertical sync. signal in DPI interface mode.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>Horizontal sync. signal in DPI interface mode.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>DE</td><td>I</td><td>Data enable signal in DPI interface mode.
If not used, please fix this pin at GND level.</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>SD</td><td>I</td><td>Control pin to shut down display, only used in the DPI interface mode.
<table>
<tr><th>SD</th><th>Shut Down Control</th></tr>
<tr><td>0</td><td>Normal Display</td></tr>
<tr><td>1</td><td>Display shut down</td></tr>
</table></td></tr>
<tr><td>CM</td><td>I</td><td>Control pin for switching between normal color and reduced color mode, only used in the DPI interface mode.
<table>
<tr><th>CM</th><th>Color Mode</th></tr>
<tr><td>0</td><td>Normal Display Color</td></tr>
<tr><td>1</td><td>Reduced Color Mode (8-color)</td></tr>
</table></td></tr>
<tr><td colspan="3">Power Input Pins</td></tr>
<tr><td>IOVCC</td><td>P</td><td>Power supply to interface pins
Connect to external power supply (IOVCC= 1.65~3.3V).</td></tr>
<tr><td>VCI</td><td>P</td><td>Power supply to liquid crystal power supply analog circuit.
Connect to external power supply (VCI=2.5~3.3V).</td></tr>
<tr><td>DGND
AGND</td><td>P</td><td>Power ground pin.
Make sure GND＝0V.</td></tr>
<tr><td>VPG</td><td>P</td><td>Power supply pin for the NV memory programming.
Please provide 7 volt to this pin for NV memory programming.</td></tr>
<tr><td colspan="3">LCD signals Pins</td></tr>
<tr><td>S1 ~ S960</td><td>O</td><td>Source driver output pins.</td></tr>
<tr><td>G1 ~ G480</td><td>O</td><td>Gate driver output pins.</td></tr>
<tr><td>VDD</td><td>O</td><td>Internal logic regulator output.
Used as internal logic power supply. Connect to stabilizing capacitor.</td></tr>
<tr><td>VCI1</td><td>P</td><td>Reference voltage for the step-up circuit 1. Set VCI1 level so that DDVDH, VGH and VGL are within the ratings.</td></tr>
<tr><td>DDVDH</td><td>P</td><td>Power supply for the source driver and VCOM.</td></tr>
<tr><td>VGH</td><td>P</td><td>Power supply to drive liquid crystal.</td></tr>
<tr><td>VGL</td><td>P</td><td>Power supply for LCD drive.</td></tr>
<tr><td>VCL</td><td>P</td><td>Power supply to drive VCOML.</td></tr>
<tr><td>C11A, C11B,
C12A, C12B</td><td>P</td><td>Make sure to connect to capacitor that is used in internal step-up circuit 1.</td></tr>
<tr><td>C13A, C13B,
C21A, C21B,
C22A, C22B,</td><td>P</td><td>Make sure to connect to capacitor that is used in internal step-up circuit 2. Connect to capacitors according to the step-up factors in use.</td></tr>
<tr><td>VREG1OUT</td><td>P</td><td>Outputs voltage level generated from VRH VCILVL. The step-up factor applied to VRH VCILVL is set by VRH bits.
Used as source driver grayscale reference voltage VREG1OUT, reference voltage to VCOMH, and Vcom amplitude reference voltage. Connect to stabilizing capacitor when in use.</td></tr>
</table>

Pin Name	I/O	Descriptions
		VREG1OUT=4.0～(DDVDH-0.500)[V]
VCOM	P	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle. Registers set the alternating cycle and operate or halt VCOM.
VCOMH	P	VCOM high level. Adjust the voltage by internal electronic volume (VCM)
VCOML	P	VCOM low level. Adjust the voltage by VDV bits. VCOML=(VCL+0.5)～0[V]
VGS	I	Reference level for grayscale generating circuit.
TEST pins		
TS[8:0]	I	Test pins These pins are internal pulled low. Please leave these pins as open.
TESTO[16:1]	O	Test pins Please leave these pins as open.
TESTA1-A3	I/O	Test pins Please leave these pins as open.
DUMMY	-	Dummy Pins These pins are floating.
V1T V62T VWT	I	Test pins Please leave these pins as open.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		960 pins (320 x RGB)
2	TFT Gate Driver		480 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1 ~ S960	V0 ~ V63 grayscales
		G1 ~ G480	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	IOVcc	1.65 ~ 3.30V
		Vci	2.50 ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		VGH	10V ~ 18V
		VGL	-5V ~ -12.5V
		VCL	-1.0V ~ -3.0V
		VGH - VGL	Max. 32V
		Vci - VCL	Max. 6.0V
7	Internal Step-up Circuits	DDVDH	Vci1 x2
		VGH	Vci1 x4, x5, x6
		VGL	Vci1 x-3, x-4, x-5
		VCL	Vci1 x-1

Items	Recommended Specification	Pin connection
Capacity 1 μF	6.3V	VREG1OUT, VCI1, VDD, VCL, VCOMH, VCOML, C11+/-, C12+/-, C13+/-,
	10V	DDVDH, C21+/-, C22+/-
	25V	VGH, VGL
Schottky diode	VF<0.4V/20mA at 25°C, VR ≥30V (Recommended diode: HSC226)	(GND – VGL), (DDVDH – VCI)

5. Pad Arrangement and Coordination

Chip Size: 22850um x 1020um

Chip thickness : 280um (typ.)

Pad Location: Pad Center.

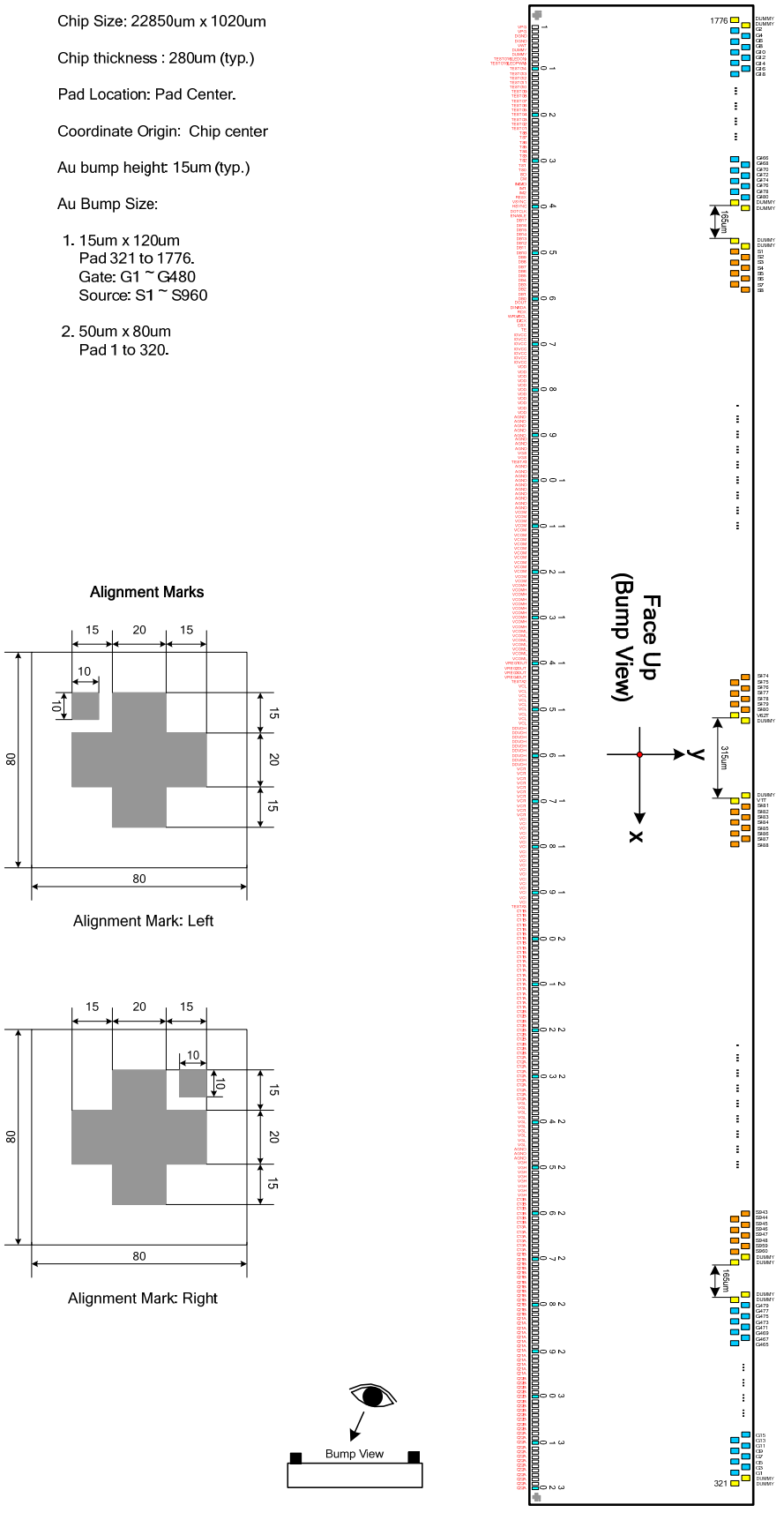
Coordinate Origin: Chip center

Au bump height: 15um (typ.)

Au Bump Size:

1. 15um x 120um
   Pad 321 to 1776.
   Gate: G1 ~ G480
   Source: S1 ~ S960

2. 50um x 80um
   Pad 1 to 320.



Alignment Marks

Alignment Mark: Left

Alignment Mark: Right

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	VPG	-11165	-409	51	DB9	-7665	-409	101	AGND	-4165	-409	151	VCL	-665	-409	201	C11B	2835	-409
2	VPG	-11095	-409	52	DB8	-7595	-409	102	AGND	-4095	-409	152	VCL	-595	-409	202	C11B	2905	-409
3	DGND	-11025	-409	53	DB7	-7525	-409	103	AGND	-4025	-409	153	VCL	-525	-409	203	C11B	2975	-409
4	DGND	-10955	-409	54	DB6	-7455	-409	104	AGND	-3955	-409	154	DDVDH	-455	-409	204	C11B	3045	-409
5	VWT	-10885	-409	55	DB5	-7385	-409	105	AGND	-3885	-409	155	DDVDH	-385	-409	205	C11A	3115	-409
6	DUMMY	-10815	-409	56	DB4	-7315	-409	106	AGND	-3815	-409	156	DDVDH	-315	-409	206	C11A	3185	-409
7	DUMMY	-10745	-409	57	DB3	-7245	-409	107	VCOM	-3745	-409	157	DDVDH	-245	-409	207	C11A	3255	-409
8	TESTO16(LEDON)	-10675	-409	58	DB2	-7175	-409	108	VCOM	-3675	-409	158	DDVDH	-175	-409	208	C11A	3325	-409
9	TESTO15(LEDPWM)	-10605	-409	59	DB1	-7105	-409	109	VCOM	-3605	-409	159	DDVDH	-105	-409	209	C11A	3395	-409
10	TESTO14	-10535	-409	60	DB0	-7035	-409	110	VCOM	-3535	-409	160	DDVDH	-35	-409	210	C11A	3465	-409
11	TESTO13	-10465	-409	61	DOUT	-6965	-409	111	VCOM	-3465	-409	161	DDVDH	35	-409	211	C11A	3535	-409
12	TESTO12	-10395	-409	62	DIN/SDA	-6895	-409	112	VCOM	-3395	-409	162	DDVDH	105	-409	212	C11A	3605	-409
13	TESTO11	-10325	-409	63	RDX	-6825	-409	113	VCOM	-3325	-409	163	VCI1	175	-409	213	C11A	3675	-409
14	TESTO10	-10255	-409	64	WRX/SCL	-6755	-409	114	VCOM	-3255	-409	164	VCI1	245	-409	214	C11A	3745	-409
15	TESTO9	-10185	-409	65	D/CX	-6685	-409	115	VCOM	-3185	-409	165	VCI1	315	-409	215	C11A	3815	-409
16	TESTO8	-10115	-409	66	CSX	-6615	-409	116	VCOM	-3115	-409	166	VCI1	385	-409	216	C12B	3885	-409
17	TESTO7	-10045	-409	67	TE	-6545	-409	117	VCOM	-3045	-409	167	VCI1	455	-409	217	C12B	3955	-409
18	TESTO6	-9975	-409	68	IOVCC	-6475	-409	118	VCOM	-2975	-409	168	VCI1	525	-409	218	C12B	4025	-409
19	TESTO5	-9905	-409	69	IOVCC	-6405	-409	119	VCOM	-2905	-409	169	VCI1	595	-409	219	C12B	4095	-409
20	TESTO4	-9835	-409	70	IOVCC	-6335	-409	120	VCOM	-2835	-409	170	VCI1	665	-409	220	C12B	4165	-409
21	TESTO3	-9765	-409	71	IOVCC	-6265	-409	121	VCOM	-2765	-409	171	VCI1	735	-409	221	C12B	4235	-409
22	TESTO2	-9695	-409	72	IOVCC	-6195	-409	122	VCOM	-2695	-409	172	VCI1	805	-409	222	C12B	4305	-409
23	TESTO1	-9625	-409	73	IOVCC	-6125	-409	123	VCOMH	-2625	-409	173	VCI1	875	-409	223	C12B	4375	-409
24	TS8	-9555	-409	74	IOVCC	-6055	-409	124	VCOMH	-2555	-409	174	VCI	945	-409	224	C12B	4445	-409
25	TS7	-9485	-409	75	VDD	-5985	-409	125	VCOMH	-2485	-409	175	VCI	1015	-409	225	C12B	4515	-409
26	TS6	-9415	-409	76	VDD	-5915	-409	126	VCOMH	-2415	-409	176	VCI	1085	-409	226	C12A	4585	-409
27	TS5	-9345	-409	77	VDD	-5845	-409	127	VCOMH	-2345	-409	177	VCI	1155	-409	227	C12A	4655	-409
28	TS4	-9275	-409	78	VDD	-5775	-409	128	VCOMH	-2275	-409	178	VCI	1225	-409	228	C12A	4725	-409
29	TS3	-9205	-409	79	VDD	-5705	-409	129	VCOMH	-2205	-409	179	VCI	1295	-409	229	C12A	4795	-409
30	TS2	-9135	-409	80	VDD	-5635	-409	130	VCOMH	-2135	-409	180	VCI	1365	-409	230	C12A	4865	-409
31	TS1	-9065	-409	81	VDD	-5565	-409	131	VCOMH	-2065	-409	181	VCI	1435	-409	231	C12A	4935	-409
32	TS0	-8995	-409	82	VDD	-5495	-409	132	VCOMH	-1995	-409	182	VCI	1505	-409	232	C12A	5005	-409
33	SD	-8925	-409	83	VDD	-5425	-409	133	VCOML	-1925	-409	183	VCI	1575	-409	233	C12A	5075	-409
34	CM	-8855	-409	84	VDD	-5355	-409	134	VCOML	-1855	-409	184	VCI	1645	-409	234	C12A	5145	-409
35	IM0/ID	-8785	-409	85	VDD	-5285	-409	135	VCOML	-1785	-409	185	VCI	1715	-409	235	C12A	5215	-409
36	IM1	-8715	-409	86	AGND	-5215	-409	136	VCOML	-1715	-409	186	VCI	1785	-409	236	VGL	5285	-409
37	IM2	-8645	-409	87	AGND	-5145	-409	137	VCOML	-1645	-409	187	VCI	1855	-409	237	VGL	5355	-409
38	RESX	-8575	-409	88	AGND	-5075	-409	138	VCOML	-1575	-409	188	VCI	1925	-409	238	VGL	5425	-409
39	VSYNC	-8505	-409	89	AGND	-5005	-409	139	VCOML	-1505	-409	189	VCI	1995	-409	239	VGL	5495	-409
40	HSYNC	-8435	-409	90	AGND	-4935	-409	140	VREG1OUT	-1435	-409	190	VCI	2065	-409	240	VGL	5565	-409
41	PCLK	-8365	-409	91	AGND	-4865	-409	141	VREG1OUT	-1365	-409	191	VCI	2135	-409	241	VGL	5635	-409
42	DE	-8295	-409	92	AGND	-4795	-409	142	VREG1OUT	-1295	-409	192	VCI	2205	-409	242	VGL	5705	-409
43	DB17	-8225	-409	93	AGND	-4725	-409	143	VREG1OUT	-1225	-409	193	TESTA3	2275	-409	243	VGL	5775	-409
44	DB16	-8155	-409	94	VGS	-4655	-409	144	TESTA2	-1155	-409	194	C11B	2345	-409	244	VGL	5845	-409
45	DB15	-8085	-409	95	VGS	-4585	-409	145	VCL	-1085	-409	195	C11B	2415	-409	245	VGL	5915	-409
46	DB14	-8015	-409	96	TESTA1	-4515	-409	146	VCL	-1015	-409	196	C11B	2485	-409	246	AGND	5985	-409
47	DB13	-7945	-409	97	AGND	-4445	-409	147	VCL	-945	-409	197	C11B	2555	-409	247	AGND	6055	-409
48	DB12	-7875	-409	98	AGND	-4375	-409	148	VCL	-875	-409	198	C11B	2625	-409	248	AGND	6125	-409
49	DB11	-7805	-409	99	AGND	-4305	-409	149	VCL	-805	-409	199	C11B	2695	-409	249	VGH	6195	-409
50	DB10	-7735	-409	100	AGND	-4235	-409	150	VCL	-735	-409	200	C11B	2765	-409	250	VGH	6265	-409

No.	Name	X	Y
251	VGH	6335	-409
252	VGH	6405	-409
253	VGH	6475	-409
254	VGH	6545	-409
255	VGH	6615	-409
256	VGH	6685	-409
257	C13B	6755	-409
258	C13B	6825	-409
259	C13B	6895	-409
260	C13B	6965	-409
261	C13B	7035	-409
262	C13B	7105	-409
263	C13A	7175	-409
264	C13A	7245	-409
265	C13A	7315	-409
266	C13A	7385	-409
267	C13A	7455	-409
268	C13A	7525	-409
269	C21B	7595	-409
270	C21B	7665	-409
271	C21B	7735	-409
272	C21B	7805	-409
273	C21B	7875	-409
274	C21B	7945	-409
275	C21B	8015	-409
276	C21B	8085	-409
277	C21B	8155	-409
278	C21B	8225	-409
279	C21B	8295	-409
280	C21B	8365	-409
281	C21B	8435	-409
282	C21B	8505	-409
283	C21A	8575	-409
284	C21A	8645	-409
285	C21A	8715	-409
286	C21A	8785	-409
287	C21A	8855	-409
288	C21A	8925	-409
289	C21A	8995	-409
290	C21A	9065	-409
291	C21A	9135	-409
292	C21A	9205	-409
293	C21A	9275	-409
294	C21A	9345	-409
295	C21A	9415	-409
296	C22B	9485	-409
297	C22B	9555	-409
298	C22B	9625	-409
299	C22B	9695	-409
300	C22B	9765	-409

No.	Name	X	Y
301	C22B	9835	-409
302	C22B	9905	-409
303	C22B	9975	-409
304	C22B	10045	-409
305	C22B	10115	-409
306	C22B	10185	-409
307	C22B	10255	-409
308	C22A	10325	-409
309	C22A	10395	-409
310	C22A	10465	-409
311	C22A	10535	-409
312	C22A	10605	-409
313	C22A	10675	-409
314	C22A	10745	-409
315	C22A	10815	-409
316	C22A	10885	-409
317	C22A	10955	-409
318	C22A	11025	-409
319	C22A	11095	-409
320	C22A	11165	-409
321	DUMMY	11205	244
322	DUMMY	11190	389
323	G1	11175	244
324	G3	11160	389
325	G5	11145	244
326	G7	11130	389
327	G9	11115	244
328	G11	11100	389
329	G13	11085	244
330	G15	11070	389
331	G17	11055	244
332	G19	11040	389
333	G21	11025	244
334	G23	11010	389
335	G25	10995	244
336	G27	10980	389
337	G29	10965	244
338	G31	10950	389
339	G33	10935	244
340	G35	10920	389
341	G37	10905	244
342	G39	10890	389
343	G41	10875	244
344	G43	10860	389
345	G45	10845	244
346	G47	10830	389
347	G49	10815	244
348	G51	10800	389
349	G53	10785	244
350	G55	10770	389

No.	Name	X	Y
351	G57	10755	244
352	G59	10740	389
353	G61	10725	244
354	G63	10710	389
355	G65	10695	244
356	G67	10680	389
357	G69	10665	244
358	G71	10650	389
359	G73	10635	244
360	G75	10620	389
361	G77	10605	244
362	G79	10590	389
363	G81	10575	244
364	G83	10560	389
365	G85	10545	244
366	G87	10530	389
367	G89	10515	244
368	G91	10500	389
369	G93	10485	244
370	G95	10470	389
371	G97	10455	244
372	G99	10440	389
373	G101	10425	244
374	G103	10410	389
375	G105	10395	244
376	G107	10380	389
377	G109	10365	244
378	G111	10350	389
379	G113	10335	244
380	G115	10320	389
381	G117	10305	244
382	G119	10290	389
383	G121	10275	244
384	G123	10260	389
385	G125	10245	244
386	G127	10230	389
387	G129	10215	244
388	G131	10200	389
389	G133	10185	244
390	G135	10170	389
391	G137	10155	244
392	G139	10140	389
393	G141	10125	244
394	G143	10110	389
395	G145	10095	244
396	G147	10080	389
397	G149	10065	244
398	G151	10050	389
399	G153	10035	244
400	G155	10020	389

No.	Name	X	Y
401	G157	10005	244
402	G159	9990	389
403	G161	9975	244
404	G163	9960	389
405	G165	9945	244
406	G167	9930	389
407	G169	9915	244
408	G171	9900	389
409	G173	9885	244
410	G175	9870	389
411	G177	9855	244
412	G179	9840	389
413	G181	9825	244
414	G183	9810	389
415	G185	9795	244
416	G187	9780	389
417	G189	9765	244
418	G191	9750	389
419	G193	9735	244
420	G195	9720	389
421	G197	9705	244
422	G199	9690	389
423	G201	9675	244
424	G203	9660	389
425	G205	9645	244
426	G207	9630	389
427	G209	9615	244
428	G211	9600	389
429	G213	9585	244
430	G215	9570	389
431	G217	9555	244
432	G219	9540	389
433	G221	9525	244
434	G223	9510	389
435	G225	9495	244
436	G227	9480	389
437	G229	9465	244
438	G231	9450	389
439	G233	9435	244
440	G235	9420	389
441	G237	9405	244
442	G239	9390	389
443	G241	9375	244
444	G243	9360	389
445	G245	9345	244
446	G247	9330	389
447	G249	9315	244
448	G251	9300	389
449	G253	9285	244
450	G255	9270	389

No.	Name	X	Y
451	G257	9255	244
452	G259	9240	389
453	G261	9225	244
454	G263	9210	389
455	G265	9195	244
456	G267	9180	389
457	G269	9165	244
458	G271	9150	389
459	G273	9135	244
460	G275	9120	389
461	G277	9105	244
462	G279	9090	389
463	G281	9075	244
464	G283	9060	389
465	G285	9045	244
466	G287	9030	389
467	G289	9015	244
468	G291	9000	389
469	G293	8985	244
470	G295	8970	389
471	G297	8955	244
472	G299	8940	389
473	G301	8925	244
474	G303	8910	389
475	G305	8895	244
476	G307	8880	389
477	G309	8865	244
478	G311	8850	389
479	G313	8835	244
480	G315	8820	389
481	G317	8805	244
482	G319	8790	389
483	G321	8775	244
484	G323	8760	389
485	G325	8745	244
486	G327	8730	389
487	G329	8715	244
488	G331	8700	389
489	G333	8685	244
490	G335	8670	389
491	G337	8655	244
492	G339	8640	389
493	G341	8625	244
494	G343	8610	389
495	G345	8595	244
496	G347	8580	389
497	G349	8565	244
498	G351	8550	389
499	G353	8535	244
500	G355	8520	389

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
501	G357	8505	244	551	G457	7755	244	601	S926	6855	244	651	S876	6105	244	701	S826	5355	244
502	G359	8490	389	552	G459	7740	389	602	S925	6840	389	652	S875	6090	389	702	S825	5340	389
503	G361	8475	244	553	G461	7725	244	603	S924	6825	244	653	S874	6075	244	703	S824	5325	244
504	G363	8460	389	554	G463	7710	389	604	S923	6810	389	654	S873	6060	389	704	S823	5310	389
505	G365	8445	244	555	G465	7695	244	605	S922	6795	244	655	S872	6045	244	705	S822	5295	244
506	G367	8430	389	556	G467	7680	389	606	S921	6780	389	656	S871	6030	389	706	S821	5280	389
507	G369	8415	244	557	G469	7665	244	607	S920	6765	244	657	S870	6015	244	707	S820	5265	244
508	G371	8400	389	558	G471	7650	389	608	S919	6750	389	658	S869	6000	389	708	S819	5250	389
509	G373	8385	244	559	G473	7635	244	609	S918	6735	244	659	S868	5985	244	709	S818	5235	244
510	G375	8370	389	560	G475	7620	389	610	S917	6720	389	660	S867	5970	389	710	S817	5220	389
511	G377	8355	244	561	G477	7605	244	611	S916	6705	244	661	S866	5955	244	711	S816	5205	244
512	G379	8340	389	562	G479	7590	389	612	S915	6690	389	662	S865	5940	389	712	S815	5190	389
513	G381	8325	244	563	DUMMY	7575	244	613	S914	6675	244	663	S864	5925	244	713	S814	5175	244
514	G383	8310	389	564	DUMMY	7560	389	614	S913	6660	389	664	S863	5910	389	714	S813	5160	389
515	G385	8295	244	565	DUMMY	7395	244	615	S912	6645	244	665	S862	5895	244	715	S812	5145	244
516	G387	8280	389	566	DUMMY	7380	389	616	S911	6630	389	666	S861	5880	389	716	S811	5130	389
517	G389	8265	244	567	S960	7365	244	617	S910	6615	244	667	S860	5865	244	717	S810	5115	244
518	G391	8250	389	568	S959	7350	389	618	S909	6600	389	668	S859	5850	389	718	S809	5100	389
519	G393	8235	244	569	S958	7335	244	619	S908	6585	244	669	S858	5835	244	719	S808	5085	244
520	G395	8220	389	570	S957	7320	389	620	S907	6570	389	670	S857	5820	389	720	S807	5070	389
521	G397	8205	244	571	S956	7305	244	621	S906	6555	244	671	S856	5805	244	721	S806	5055	244
522	G399	8190	389	572	S955	7290	389	622	S905	6540	389	672	S855	5790	389	722	S805	5040	389
523	G401	8175	244	573	S954	7275	244	623	S904	6525	244	673	S854	5775	244	723	S804	5025	244
524	G403	8160	389	574	S953	7260	389	624	S903	6510	389	674	S853	5760	389	724	S803	5010	389
525	G405	8145	244	575	S952	7245	244	625	S902	6495	244	675	S852	5745	244	725	S802	4995	244
526	G407	8130	389	576	S951	7230	389	626	S901	6480	389	676	S851	5730	389	726	S801	4980	389
527	G409	8115	244	577	S950	7215	244	627	S900	6465	244	677	S850	5715	244	727	S800	4965	244
528	G411	8100	389	578	S949	7200	389	628	S899	6450	389	678	S849	5700	389	728	S799	4950	389
529	G413	8085	244	579	S948	7185	244	629	S898	6435	244	679	S848	5685	244	729	S798	4935	244
530	G415	8070	389	580	S947	7170	389	630	S897	6420	389	680	S847	5670	389	730	S797	4920	389
531	G417	8055	244	581	S946	7155	244	631	S896	6405	244	681	S846	5655	244	731	S796	4905	244
532	G419	8040	389	582	S945	7140	389	632	S895	6390	389	682	S845	5640	389	732	S795	4890	389
533	G421	8025	244	583	S944	7125	244	633	S894	6375	244	683	S844	5625	244	733	S794	4875	244
534	G423	8010	389	584	S943	7110	389	634	S893	6360	389	684	S843	5610	389	734	S793	4860	389
535	G425	7995	244	585	S942	7095	244	635	S892	6345	244	685	S842	5595	244	735	S792	4845	244
536	G427	7980	389	586	S941	7080	389	636	S891	6330	389	686	S841	5580	389	736	S791	4830	389
537	G429	7965	244	587	S940	7065	244	637	S890	6315	244	687	S840	5565	244	737	S790	4815	244
538	G431	7950	389	588	S939	7050	389	638	S889	6300	389	688	S839	5550	389	738	S789	4800	389
539	G433	7935	244	589	S938	7035	244	639	S888	6285	244	689	S838	5535	244	739	S788	4785	244
540	G435	7920	389	590	S937	7020	389	640	S887	6270	389	690	S837	5520	389	740	S787	4770	389
541	G437	7905	244	591	S936	7005	244	641	S886	6255	244	691	S836	5505	244	741	S786	4755	244
542	G439	7890	389	592	S935	6990	389	642	S885	6240	389	692	S835	5490	389	742	S785	4740	389
543	G441	7875	244	593	S934	6975	244	643	S884	6225	244	693	S834	5475	244	743	S784	4725	244
544	G443	7860	389	594	S933	6960	389	644	S883	6210	389	694	S833	5460	389	744	S783	4710	389
545	G445	7845	244	595	S932	6945	244	645	S882	6195	244	695	S832	5445	244	745	S782	4695	244
546	G447	7830	389	596	S931	6930	389	646	S881	6180	389	696	S831	5430	389	746	S781	4680	389
547	G449	7815	244	597	S930	6915	244	647	S880	6165	244	697	S830	5415	244	747	S780	4665	244
548	G451	7800	389	598	S929	6900	389	648	S879	6150	389	698	S829	5400	389	748	S779	4650	389
549	G453	7785	244	599	S928	6885	244	649	S878	6135	244	699	S828	5385	244	749	S778	4635	244
550	G455	7770	389	600	S927	6870	389	650	S877	6120	389	700	S827	5370	389	750	S777	4620	389

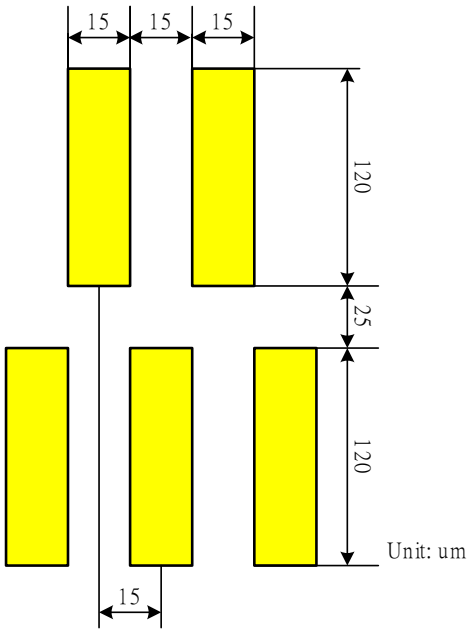
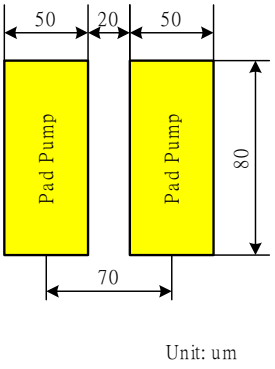
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
751	S776	4605	244	801	S726	3855	244	851	S676	3105	244	901	S626	2355	244	951	S576	1605	244
752	S775	4590	389	802	S725	3840	389	852	S675	3090	389	902	S625	2340	389	952	S575	1590	389
753	S774	4575	244	803	S724	3825	244	853	S674	3075	244	903	S624	2325	244	953	S574	1575	244
754	S773	4560	389	804	S723	3810	389	854	S673	3060	389	904	S623	2310	389	954	S573	1560	389
755	S772	4545	244	805	S722	3795	244	855	S672	3045	244	905	S622	2295	244	955	S572	1545	244
756	S771	4530	389	806	S721	3780	389	856	S671	3030	389	906	S621	2280	389	956	S571	1530	389
757	S770	4515	244	807	S720	3765	244	857	S670	3015	244	907	S620	2265	244	957	S570	1515	244
758	S769	4500	389	808	S719	3750	389	858	S669	3000	389	908	S619	2250	389	958	S569	1500	389
759	S768	4485	244	809	S718	3735	244	859	S668	2985	244	909	S618	2235	244	959	S568	1485	244
760	S767	4470	389	810	S717	3720	389	860	S667	2970	389	910	S617	2220	389	960	S567	1470	389
761	S766	4455	244	811	S716	3705	244	861	S666	2955	244	911	S616	2205	244	961	S566	1455	244
762	S765	4440	389	812	S715	3690	389	862	S665	2940	389	912	S615	2190	389	962	S565	1440	389
763	S764	4425	244	813	S714	3675	244	863	S664	2925	244	913	S614	2175	244	963	S564	1425	244
764	S763	4410	389	814	S713	3660	389	864	S663	2910	389	914	S613	2160	389	964	S563	1410	389
765	S762	4395	244	815	S712	3645	244	865	S662	2895	244	915	S612	2145	244	965	S562	1395	244
766	S761	4380	389	816	S711	3630	389	866	S661	2880	389	916	S611	2130	389	966	S561	1380	389
767	S760	4365	244	817	S710	3615	244	867	S660	2865	244	917	S610	2115	244	967	S560	1365	244
768	S759	4350	389	818	S709	3600	389	868	S659	2850	389	918	S609	2100	389	968	S559	1350	389
769	S758	4335	244	819	S708	3585	244	869	S658	2835	244	919	S608	2085	244	969	S558	1335	244
770	S757	4320	389	820	S707	3570	389	870	S657	2820	389	920	S607	2070	389	970	S557	1320	389
771	S756	4305	244	821	S706	3555	244	871	S656	2805	244	921	S606	2055	244	971	S556	1305	244
772	S755	4290	389	822	S705	3540	389	872	S655	2790	389	922	S605	2040	389	972	S555	1290	389
773	S754	4275	244	823	S704	3525	244	873	S654	2775	244	923	S604	2025	244	973	S554	1275	244
774	S753	4260	389	824	S703	3510	389	874	S653	2760	389	924	S603	2010	389	974	S553	1260	389
775	S752	4245	244	825	S702	3495	244	875	S652	2745	244	925	S602	1995	244	975	S552	1245	244
776	S751	4230	389	826	S701	3480	389	876	S651	2730	389	926	S601	1980	389	976	S551	1230	389
777	S750	4215	244	827	S700	3465	244	877	S650	2715	244	927	S600	1965	244	977	S550	1215	244
778	S749	4200	389	828	S699	3450	389	878	S649	2700	389	928	S599	1950	389	978	S549	1200	389
779	S748	4185	244	829	S698	3435	244	879	S648	2685	244	929	S598	1935	244	979	S548	1185	244
780	S747	4170	389	830	S697	3420	389	880	S647	2670	389	930	S597	1920	389	980	S547	1170	389
781	S746	4155	244	831	S696	3405	244	881	S646	2655	244	931	S596	1905	244	981	S546	1155	244
782	S745	4140	389	832	S695	3390	389	882	S645	2640	389	932	S595	1890	389	982	S545	1140	389
783	S744	4125	244	833	S694	3375	244	883	S644	2625	244	933	S594	1875	244	983	S544	1125	244
784	S743	4110	389	834	S693	3360	389	884	S643	2610	389	934	S593	1860	389	984	S543	1110	389
785	S742	4095	244	835	S692	3345	244	885	S642	2595	244	935	S592	1845	244	985	S542	1095	244
786	S741	4080	389	836	S691	3330	389	886	S641	2580	389	936	S591	1830	389	986	S541	1080	389
787	S740	4065	244	837	S690	3315	244	887	S640	2565	244	937	S590	1815	244	987	S540	1065	244
788	S739	4050	389	838	S689	3300	389	888	S639	2550	389	938	S589	1800	389	988	S539	1050	389
789	S738	4035	244	839	S688	3285	244	889	S638	2535	244	939	S588	1785	244	989	S538	1035	244
790	S737	4020	389	840	S687	3270	389	890	S637	2520	389	940	S587	1770	389	990	S537	1020	389
791	S736	4005	244	841	S686	3255	244	891	S636	2505	244	941	S586	1755	244	991	S536	1005	244
792	S735	3990	389	842	S685	3240	389	892	S635	2490	389	942	S585	1740	389	992	S535	990	389
793	S734	3975	244	843	S684	3225	244	893	S634	2475	244	943	S584	1725	244	993	S534	975	244
794	S733	3960	389	844	S683	3210	389	894	S633	2460	389	944	S583	1710	389	994	S533	960	389
795	S732	3945	244	845	S682	3195	244	895	S632	2445	244	945	S582	1695	244	995	S532	945	244
796	S731	3930	389	846	S681	3180	389	896	S631	2430	389	946	S581	1680	389	996	S531	930	389
797	S730	3915	244	847	S680	3165	244	897	S630	2415	244	947	S580	1665	244	997	S530	915	244
798	S729	3900	389	848	S679	3150	389	898	S629	2400	389	948	S579	1650	389	998	S529	900	389
799	S728	3885	244	849	S678	3135	244	899	S628	2385	244	949	S578	1635	244	999	S528	885	244
800	S727	3870	389	850	S677	3120	389	900	S627	2370	389	950	S577	1620	389	1000	S527	870	389

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1001	S526	855	244	1051	S480	-180	389	1101	S430	-930	389	1151	S380	-1680	389	1201	S330	-2430	389
1002	S525	840	389	1052	S479	-195	244	1102	S429	-945	244	1152	S379	-1695	244	1202	S329	-2445	244
1003	S524	825	244	1053	S478	-210	389	1103	S428	-960	389	1153	S378	-1710	389	1203	S328	-2460	389
1004	S523	810	389	1054	S477	-225	244	1104	S427	-975	244	1154	S377	-1725	244	1204	S327	-2475	244
1005	S522	795	244	1055	S476	-240	389	1105	S426	-990	389	1155	S376	-1740	389	1205	S326	-2490	389
1006	S521	780	389	1056	S475	-255	244	1106	S425	-1005	244	1156	S375	-1755	244	1206	S325	-2505	244
1007	S520	765	244	1057	S474	-270	389	1107	S424	-1020	389	1157	S374	-1770	389	1207	S324	-2520	389
1008	S519	750	389	1058	S473	-285	244	1108	S423	-1035	244	1158	S373	-1785	244	1208	S323	-2535	244
1009	S518	735	244	1059	S472	-300	389	1109	S422	-1050	389	1159	S372	-1800	389	1209	S322	-2550	389
1010	S517	720	389	1060	S471	-315	244	1110	S421	-1065	244	1160	S371	-1815	244	1210	S321	-2565	244
1011	S516	705	244	1061	S470	-330	389	1111	S420	-1080	389	1161	S370	-1830	389	1211	S320	-2580	389
1012	S515	690	389	1062	S469	-345	244	1112	S419	-1095	244	1162	S369	-1845	244	1212	S319	-2595	244
1013	S514	675	244	1063	S468	-360	389	1113	S418	-1110	389	1163	S368	-1860	389	1213	S318	-2610	389
1014	S513	660	389	1064	S467	-375	244	1114	S417	-1125	244	1164	S367	-1875	244	1214	S317	-2625	244
1015	S512	645	244	1065	S466	-390	389	1115	S416	-1140	389	1165	S366	-1890	389	1215	S316	-2640	389
1016	S511	630	389	1066	S465	-405	244	1116	S415	-1155	244	1166	S365	-1905	244	1216	S315	-2655	244
1017	S510	615	244	1067	S464	-420	389	1117	S414	-1170	389	1167	S364	-1920	389	1217	S314	-2670	389
1018	S509	600	389	1068	S463	-435	244	1118	S413	-1185	244	1168	S363	-1935	244	1218	S313	-2685	244
1019	S508	585	244	1069	S462	-450	389	1119	S412	-1200	389	1169	S362	-1950	389	1219	S312	-2700	389
1020	S507	570	389	1070	S461	-465	244	1120	S411	-1215	244	1170	S361	-1965	244	1220	S311	-2715	244
1021	S506	555	244	1071	S460	-480	389	1121	S410	-1230	389	1171	S360	-1980	389	1221	S310	-2730	389
1022	S505	540	389	1072	S459	-495	244	1122	S409	-1245	244	1172	S359	-1995	244	1222	S309	-2745	244
1023	S504	525	244	1073	S458	-510	389	1123	S408	-1260	389	1173	S358	-2010	389	1223	S308	-2760	389
1024	S503	510	389	1074	S457	-525	244	1124	S407	-1275	244	1174	S357	-2025	244	1224	S307	-2775	244
1025	S502	495	244	1075	S456	-540	389	1125	S406	-1290	389	1175	S356	-2040	389	1225	S306	-2790	389
1026	S501	480	389	1076	S455	-555	244	1126	S405	-1305	244	1176	S355	-2055	244	1226	S305	-2805	244
1027	S500	465	244	1077	S454	-570	389	1127	S404	-1320	389	1177	S354	-2070	389	1227	S304	-2820	389
1028	S499	450	389	1078	S453	-585	244	1128	S403	-1335	244	1178	S353	-2085	244	1228	S303	-2835	244
1029	S498	435	244	1079	S452	-600	389	1129	S402	-1350	389	1179	S352	-2100	389	1229	S302	-2850	389
1030	S497	420	389	1080	S451	-615	244	1130	S401	-1365	244	1180	S351	-2115	244	1230	S301	-2865	244
1031	S496	405	244	1081	S450	-630	389	1131	S400	-1380	389	1181	S350	-2130	389	1231	S300	-2880	389
1032	S495	390	389	1082	S449	-645	244	1132	S399	-1395	244	1182	S349	-2145	244	1232	S299	-2895	244
1033	S494	375	244	1083	S448	-660	389	1133	S398	-1410	389	1183	S348	-2160	389	1233	S298	-2910	389
1034	S493	360	389	1084	S447	-675	244	1134	S397	-1425	244	1184	S347	-2175	244	1234	S297	-2925	244
1035	S492	345	244	1085	S446	-690	389	1135	S396	-1440	389	1185	S346	-2190	389	1235	S296	-2940	389
1036	S491	330	389	1086	S445	-705	244	1136	S395	-1455	244	1186	S345	-2205	244	1236	S295	-2955	244
1037	S490	315	244	1087	S444	-720	389	1137	S394	-1470	389	1187	S344	-2220	389	1237	S294	-2970	389
1038	S489	300	389	1088	S443	-735	244	1138	S393	-1485	244	1188	S343	-2235	244	1238	S293	-2985	244
1039	S488	285	244	1089	S442	-750	389	1139	S392	-1500	389	1189	S342	-2250	389	1239	S292	-3000	389
1040	S487	270	389	1090	S441	-765	244	1140	S391	-1515	244	1190	S341	-2265	244	1240	S291	-3015	244
1041	S486	255	244	1091	S440	-780	389	1141	S390	-1530	389	1191	S340	-2280	389	1241	S290	-3030	389
1042	S485	240	389	1092	S439	-795	244	1142	S389	-1545	244	1192	S339	-2295	244	1242	S289	-3045	244
1043	S484	225	244	1093	S438	-810	389	1143	S388	-1560	389	1193	S338	-2310	389	1243	S288	-3060	389
1044	S483	210	389	1094	S437	-825	244	1144	S387	-1575	244	1194	S337	-2325	244	1244	S287	-3075	244
1045	S482	195	244	1095	S436	-840	389	1145	S386	-1590	389	1195	S336	-2340	389	1245	S286	-3090	389
1046	S481	180	389	1096	S435	-855	244	1146	S385	-1605	244	1196	S335	-2355	244	1246	S285	-3105	244
1047	V1T	165	244	1097	S434	-870	389	1147	S384	-1620	389	1197	S334	-2370	389	1247	S284	-3120	389
1048	DUMMY	150	389	1098	S433	-885	244	1148	S383	-1635	244	1198	S333	-2385	244	1248	S283	-3135	244
1049	DUMMY	-150	389	1099	S432	-900	389	1149	S382	-1650	389	1199	S332	-2400	389	1249	S282	-3150	389
1050	V62T	-165	244	1100	S431	-915	244	1150	S381	-1665	244	1200	S331	-2415	244	1250	S281	-3165	244

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1251	S280	-3180	389	1301	S230	-3930	389	1351	S180	-4680	389	1401	S130	-5430	389	1451	S80	-6180	389
1252	S279	-3195	244	1302	S229	-3945	244	1352	S179	-4695	244	1402	S129	-5445	244	1452	S79	-6195	244
1253	S278	-3210	389	1303	S228	-3960	389	1353	S178	-4710	389	1403	S128	-5460	389	1453	S78	-6210	389
1254	S277	-3225	244	1304	S227	-3975	244	1354	S177	-4725	244	1404	S127	-5475	244	1454	S77	-6225	244
1255	S276	-3240	389	1305	S226	-3990	389	1355	S176	-4740	389	1405	S126	-5490	389	1455	S76	-6240	389
1256	S275	-3255	244	1306	S225	-4005	244	1356	S175	-4755	244	1406	S125	-5505	244	1456	S75	-6255	244
1257	S274	-3270	389	1307	S224	-4020	389	1357	S174	-4770	389	1407	S124	-5520	389	1457	S74	-6270	389
1258	S273	-3285	244	1308	S223	-4035	244	1358	S173	-4785	244	1408	S123	-5535	244	1458	S73	-6285	244
1259	S272	-3300	389	1309	S222	-4050	389	1359	S172	-4800	389	1409	S122	-5550	389	1459	S72	-6300	389
1260	S271	-3315	244	1310	S221	-4065	244	1360	S171	-4815	244	1410	S121	-5565	244	1460	S71	-6315	244
1261	S270	-3330	389	1311	S220	-4080	389	1361	S170	-4830	389	1411	S120	-5580	389	1461	S70	-6330	389
1262	S269	-3345	244	1312	S219	-4095	244	1362	S169	-4845	244	1412	S119	-5595	244	1462	S69	-6345	244
1263	S268	-3360	389	1313	S218	-4110	389	1363	S168	-4860	389	1413	S118	-5610	389	1463	S68	-6360	389
1264	S267	-3375	244	1314	S217	-4125	244	1364	S167	-4875	244	1414	S117	-5625	244	1464	S67	-6375	244
1265	S266	-3390	389	1315	S216	-4140	389	1365	S166	-4890	389	1415	S116	-5640	389	1465	S66	-6390	389
1266	S265	-3405	244	1316	S215	-4155	244	1366	S165	-4905	244	1416	S115	-5655	244	1466	S65	-6405	244
1267	S264	-3420	389	1317	S214	-4170	389	1367	S164	-4920	389	1417	S114	-5670	389	1467	S64	-6420	389
1268	S263	-3435	244	1318	S213	-4185	244	1368	S163	-4935	244	1418	S113	-5685	244	1468	S63	-6435	244
1269	S262	-3450	389	1319	S212	-4200	389	1369	S162	-4950	389	1419	S112	-5700	389	1469	S62	-6450	389
1270	S261	-3465	244	1320	S211	-4215	244	1370	S161	-4965	244	1420	S111	-5715	244	1470	S61	-6465	244
1271	S260	-3480	389	1321	S210	-4230	389	1371	S160	-4980	389	1421	S110	-5730	389	1471	S60	-6480	389
1272	S259	-3495	244	1322	S209	-4245	244	1372	S159	-4995	244	1422	S109	-5745	244	1472	S59	-6495	244
1273	S258	-3510	389	1323	S208	-4260	389	1373	S158	-5010	389	1423	S108	-5760	389	1473	S58	-6510	389
1274	S257	-3525	244	1324	S207	-4275	244	1374	S157	-5025	244	1424	S107	-5775	244	1474	S57	-6525	244
1275	S256	-3540	389	1325	S206	-4290	389	1375	S156	-5040	389	1425	S106	-5790	389	1475	S56	-6540	389
1276	S255	-3555	244	1326	S205	-4305	244	1376	S155	-5055	244	1426	S105	-5805	244	1476	S55	-6555	244
1277	S254	-3570	389	1327	S204	-4320	389	1377	S154	-5070	389	1427	S104	-5820	389	1477	S54	-6570	389
1278	S253	-3585	244	1328	S203	-4335	244	1378	S153	-5085	244	1428	S103	-5835	244	1478	S53	-6585	244
1279	S252	-3600	389	1329	S202	-4350	389	1379	S152	-5100	389	1429	S102	-5850	389	1479	S52	-6600	389
1280	S251	-3615	244	1330	S201	-4365	244	1380	S151	-5115	244	1430	S101	-5865	244	1480	S51	-6615	244
1281	S250	-3630	389	1331	S200	-4380	389	1381	S150	-5130	389	1431	S100	-5880	389	1481	S50	-6630	389
1282	S249	-3645	244	1332	S199	-4395	244	1382	S149	-5145	244	1432	S99	-5895	244	1482	S49	-6645	244
1283	S248	-3660	389	1333	S198	-4410	389	1383	S148	-5160	389	1433	S98	-5910	389	1483	S48	-6660	389
1284	S247	-3675	244	1334	S197	-4425	244	1384	S147	-5175	244	1434	S97	-5925	244	1484	S47	-6675	244
1285	S246	-3690	389	1335	S196	-4440	389	1385	S146	-5190	389	1435	S96	-5940	389	1485	S46	-6690	389
1286	S245	-3705	244	1336	S195	-4455	244	1386	S145	-5205	244	1436	S95	-5955	244	1486	S45	-6705	244
1287	S244	-3720	389	1337	S194	-4470	389	1387	S144	-5220	389	1437	S94	-5970	389	1487	S44	-6720	389
1288	S243	-3735	244	1338	S193	-4485	244	1388	S143	-5235	244	1438	S93	-5985	244	1488	S43	-6735	244
1289	S242	-3750	389	1339	S192	-4500	389	1389	S142	-5250	389	1439	S92	-6000	389	1489	S42	-6750	389
1290	S241	-3765	244	1340	S191	-4515	244	1390	S141	-5265	244	1440	S91	-6015	244	1490	S41	-6765	244
1291	S240	-3780	389	1341	S190	-4530	389	1391	S140	-5280	389	1441	S90	-6030	389	1491	S40	-6780	389
1292	S239	-3795	244	1342	S189	-4545	244	1392	S139	-5295	244	1442	S89	-6045	244	1492	S39	-6795	244
1293	S238	-3810	389	1343	S188	-4560	389	1393	S138	-5310	389	1443	S88	-6060	389	1493	S38	-6810	389
1294	S237	-3825	244	1344	S187	-4575	244	1394	S137	-5325	244	1444	S87	-6075	244	1494	S37	-6825	244
1295	S236	-3840	389	1345	S186	-4590	389	1395	S136	-5340	389	1445	S86	-6090	389	1495	S36	-6840	389
1296	S235	-3855	244	1346	S185	-4605	244	1396	S135	-5355	244	1446	S85	-6105	244	1496	S35	-6855	244
1297	S234	-3870	389	1347	S184	-4620	389	1397	S134	-5370	389	1447	S84	-6120	389	1497	S34	-6870	389
1298	S233	-3885	244	1348	S183	-4635	244	1398	S133	-5385	244	1448	S83	-6135	244	1498	S33	-6885	244
1299	S232	-3900	389	1349	S182	-4650	389	1399	S132	-5400	389	1449	S82	-6150	389	1499	S32	-6900	389
1300	S231	-3915	244	1350	S181	-4665	244	1400	S131	-5415	244	1450	S81	-6165	244	1500	S31	-6915	244

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1501	S30	-6930	389	1551	G448	-7830	389	1601	G348	-8580	389	1651	G248	-9330	389	1701	G148	-10080	389
1502	S29	-6945	244	1552	G446	-7845	244	1602	G346	-8595	244	1652	G246	-9345	244	1702	G146	-10095	244
1503	S28	-6960	389	1553	G444	-7860	389	1603	G344	-8610	389	1653	G244	-9360	389	1703	G144	-10110	389
1504	S27	-6975	244	1554	G442	-7875	244	1604	G342	-8625	244	1654	G242	-9375	244	1704	G142	-10125	244
1505	S26	-6990	389	1555	G440	-7890	389	1605	G340	-8640	389	1655	G240	-9390	389	1705	G140	-10140	389
1506	S25	-7005	244	1556	G438	-7905	244	1606	G338	-8655	244	1656	G238	-9405	244	1706	G138	-10155	244
1507	S24	-7020	389	1557	G436	-7920	389	1607	G336	-8670	389	1657	G236	-9420	389	1707	G136	-10170	389
1508	S23	-7035	244	1558	G434	-7935	244	1608	G334	-8685	244	1658	G234	-9435	244	1708	G134	-10185	244
1509	S22	-7050	389	1559	G432	-7950	389	1609	G332	-8700	389	1659	G232	-9450	389	1709	G132	-10200	389
1510	S21	-7065	244	1560	G430	-7965	244	1610	G330	-8715	244	1660	G230	-9465	244	1710	G130	-10215	244
1511	S20	-7080	389	1561	G428	-7980	389	1611	G328	-8730	389	1661	G228	-9480	389	1711	G128	-10230	389
1512	S19	-7095	244	1562	G426	-7995	244	1612	G326	-8745	244	1662	G226	-9495	244	1712	G126	-10245	244
1513	S18	-7110	389	1563	G424	-8010	389	1613	G324	-8760	389	1663	G224	-9510	389	1713	G124	-10260	389
1514	S17	-7125	244	1564	G422	-8025	244	1614	G322	-8775	244	1664	G222	-9525	244	1714	G122	-10275	244
1515	S16	-7140	389	1565	G420	-8040	389	1615	G320	-8790	389	1665	G220	-9540	389	1715	G120	-10290	389
1516	S15	-7155	244	1566	G418	-8055	244	1616	G318	-8805	244	1666	G218	-9555	244	1716	G118	-10305	244
1517	S14	-7170	389	1567	G416	-8070	389	1617	G316	-8820	389	1667	G216	-9570	389	1717	G116	-10320	389
1518	S13	-7185	244	1568	G414	-8085	244	1618	G314	-8835	244	1668	G214	-9585	244	1718	G114	-10335	244
1519	S12	-7200	389	1569	G412	-8100	389	1619	G312	-8850	389	1669	G212	-9600	389	1719	G112	-10350	389
1520	S11	-7215	244	1570	G410	-8115	244	1620	G310	-8865	244	1670	G210	-9615	244	1720	G110	-10365	244
1521	S10	-7230	389	1571	G408	-8130	389	1621	G308	-8880	389	1671	G208	-9630	389	1721	G108	-10380	389
1522	S9	-7245	244	1572	G406	-8145	244	1622	G306	-8895	244	1672	G206	-9645	244	1722	G106	-10395	244
1523	S8	-7260	389	1573	G404	-8160	389	1623	G304	-8910	389	1673	G204	-9660	389	1723	G104	-10410	389
1524	S7	-7275	244	1574	G402	-8175	244	1624	G302	-8925	244	1674	G202	-9675	244	1724	G102	-10425	244
1525	S6	-7290	389	1575	G400	-8190	389	1625	G300	-8940	389	1675	G200	-9690	389	1725	G100	-10440	389
1526	S5	-7305	244	1576	G398	-8205	244	1626	G298	-8955	244	1676	G198	-9705	244	1726	G98	-10455	244
1527	S4	-7320	389	1577	G396	-8220	389	1627	G296	-8970	389	1677	G196	-9720	389	1727	G96	-10470	389
1528	S3	-7335	244	1578	G394	-8235	244	1628	G294	-8985	244	1678	G194	-9735	244	1728	G94	-10485	244
1529	S2	-7350	389	1579	G392	-8250	389	1629	G292	-9000	389	1679	G192	-9750	389	1729	G92	-10500	389
1530	S1	-7365	244	1580	G390	-8265	244	1630	G290	-9015	244	1680	G190	-9765	244	1730	G90	-10515	244
1531	DUMMY	-7380	389	1581	G388	-8280	389	1631	G288	-9030	389	1681	G188	-9780	389	1731	G88	-10530	389
1532	DUMMY	-7395	244	1582	G386	-8295	244	1632	G286	-9045	244	1682	G186	-9795	244	1732	G86	-10545	244
1533	DUMMY	-7560	389	1583	G384	-8310	389	1633	G284	-9060	389	1683	G184	-9810	389	1733	G84	-10560	389
1534	DUMMY	-7575	244	1584	G382	-8325	244	1634	G282	-9075	244	1684	G182	-9825	244	1734	G82	-10575	244
1535	G480	-7590	389	1585	G380	-8340	389	1635	G280	-9090	389	1685	G180	-9840	389	1735	G80	-10590	389
1536	G478	-7605	244	1586	G378	-8355	244	1636	G278	-9105	244	1686	G178	-9855	244	1736	G78	-10605	244
1537	G476	-7620	389	1587	G376	-8370	389	1637	G276	-9120	389	1687	G176	-9870	389	1737	G76	-10620	389
1538	G474	-7635	244	1588	G374	-8385	244	1638	G274	-9135	244	1688	G174	-9885	244	1738	G74	-10635	244
1539	G472	-7650	389	1589	G372	-8400	389	1639	G272	-9150	389	1689	G172	-9900	389	1739	G72	-10650	389
1540	G470	-7665	244	1590	G370	-8415	244	1640	G270	-9165	244	1690	G170	-9915	244	1740	G70	-10665	244
1541	G468	-7680	389	1591	G368	-8430	389	1641	G268	-9180	389	1691	G168	-9930	389	1741	G68	-10680	389
1542	G466	-7695	244	1592	G366	-8445	244	1642	G266	-9195	244	1692	G166	-9945	244	1742	G66	-10695	244
1543	G464	-7710	389	1593	G364	-8460	389	1643	G264	-9210	389	1693	G164	-9960	389	1743	G64	-10710	389
1544	G462	-7725	244	1594	G362	-8475	244	1644	G262	-9225	244	1694	G162	-9975	244	1744	G62	-10725	244
1545	G460	-7740	389	1595	G360	-8490	389	1645	G260	-9240	389	1695	G160	-9990	389	1745	G60	-10740	389
1546	G458	-7755	244	1596	G358	-8505	244	1646	G258	-9255	244	1696	G158	-10005	244	1746	G58	-10755	244
1547	G456	-7770	389	1597	G356	-8520	389	1647	G256	-9270	389	1697	G156	-10020	389	1747	G56	-10770	389
1548	G454	-7785	244	1598	G354	-8535	244	1648	G254	-9285	244	1698	G154	-10035	244	1748	G54	-10785	244
1549	G452	-7800	389	1599	G352	-8550	389	1649	G252	-9300	389	1699	G152	-10050	389	1749	G52	-10800	389
1550	G450	-7815	244	1600	G350	-8565	244	1650	G250	-9315	244	1700	G150	-10065	244	1750	G50	-10815	244

No.	Name	X	Y
1751	G48	-10830	389
1752	G46	-10845	244
1753	G44	-10860	389
1754	G42	-10875	244
1755	G40	-10890	389
1756	G38	-10905	244
1757	G36	-10920	389
1758	G34	-10935	244
1759	G32	-10950	389
1760	G30	-10965	244
1761	G28	-10980	389
1762	G26	-10995	244
1763	G24	-11010	389
1764	G22	-11025	244
1765	G20	-11040	389
1766	G18	-11055	244
1767	G16	-11070	389
1768	G14	-11085	244
1769	G12	-11100	389
1770	G10	-11115	244
1771	G8	-11130	389
1772	G6	-11145	244
1773	G4	-11160	389
1774	G2	-11175	244
1775	DUMMY	-11190	389
1776	DUMMY	-11205	244
Alignment mark -Left		-11300	-400
Alignment mark -Right		11300	-400

S1 ~ S960 G1 ~ G480 (No. 321 ~ 1776)	
I/O Pads (No. 1 ~ 320)	

6. Block Function Description

Interface

The ILI9481 incorporates command method 18-/16-/9-/8-bits bus display command interface, which consists of 8 bits command registers and 8 bits parameter registers. Parameter registers consist of 8 bits write data register (WDR) and 8bit read data register (RDR).

WDR stores data to be written into GRAM or parameters temporarily while RDR stores data read out from GRAM temporarily. When data is written from microcomputer to GRAM, the ILI9481 writes firstly to WDR, and then the data is written to GRAM automatically by internal operation. Because read out operation from GRAM is conducted through RDR, first read out data is invalid. Normal data is read out from 2nd read out data.

Register selection

DCX	RDX	WRX	Operation
0	1	↑	Command
1	↑	1	Read parameter
1	1	↑	Write parameter

Address Counter (AC)

Address counter (AC) gives address to GRAM. When command setting address is written to CDR, the data is transferred from CDR to AC.

When data is written to GRAM, address counter (AC) increments by +1 or –1 automatically. AC after data is read out increments by +1 or –1 likewise. The ILI9481 writes data to only rectangular area that was specified by GRAM.

Graphic RAM (GRAM)

The graphic RAM (GRAM) stores 345,600 byte bit pattern data using 18 bits for one pixel, enabling a maximum 320RGB x 480 dot graphic display at the maximum.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the γ correction register. The ILI9481 displays 262,144 colors at the maximum.

Power Supply Circuit

The power supply circuit generates supply voltages to a-TFT panel, VREG1OUT, VGH, VGL, VCOMH and VCOML.

Timing Generating

The timing generator generates timing signals for internal circuits such as the internal GRAM. The timing for display operation such as RAM read operation and the timing for internal operation such as RAM access by MPU is outputted separately so that they do not interfere with each other.

Oscillator

The ILI9481 incorporates RC oscillator circuit. The frame frequency is changeable by command settings.

Panel Driver Circuit

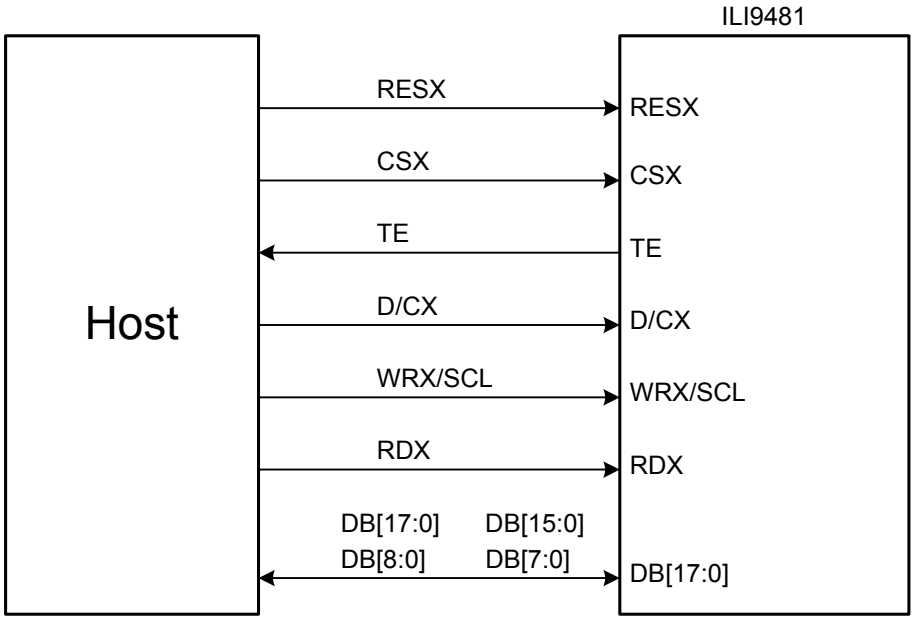
The liquid crystal display driver circuit consists of 960 source drivers (S1~S960). Display pattern data is latched when 960 byte data is input. This latched data controls source drivers and outputs drive waveform. The shift direction of 960-bit output from the source driver can be changed by setting commands.

The gate driver consists of 480 gate drivers (G1~G480) and outputs either VGH or VGL level. The shift direction of gate driver is set by GS bit. Scan direction of gate driver is set by SM bit enabling users to set the ILI9481 so that it suits mounting method

7. Function Description

7.1. Display Bus Interface (DBI)

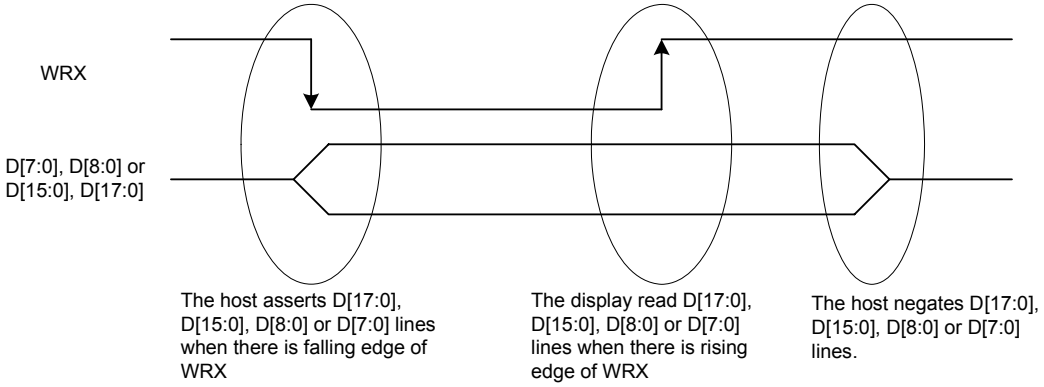
The ILI9481 uses a 22-wires 18-bit parallel interface. The chip-select CSX (active low) enables and disables the DBI interface. RESX (active low) is an external reset signal. WRX is the data write, RDX is the data read and D[17:0] is parallel DBI data. There are four 18/16/9/8-bit types interface supported for the display data transfer. The Graphics Controller Chip reads the data at the rising edge of RDX signal. The D/CX is data/command flag. When D/CX = "1", D17 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

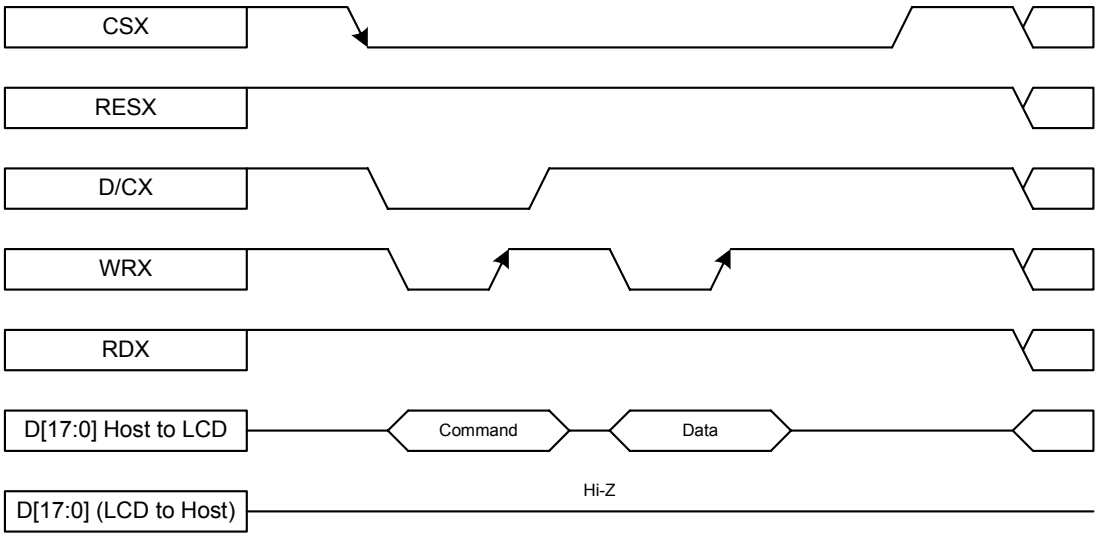


7.1.1. Write Cycle

During a write cycle the host processor sends data to the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. WRX is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of WRX. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The following figure shows a write cycle for the type B interface.

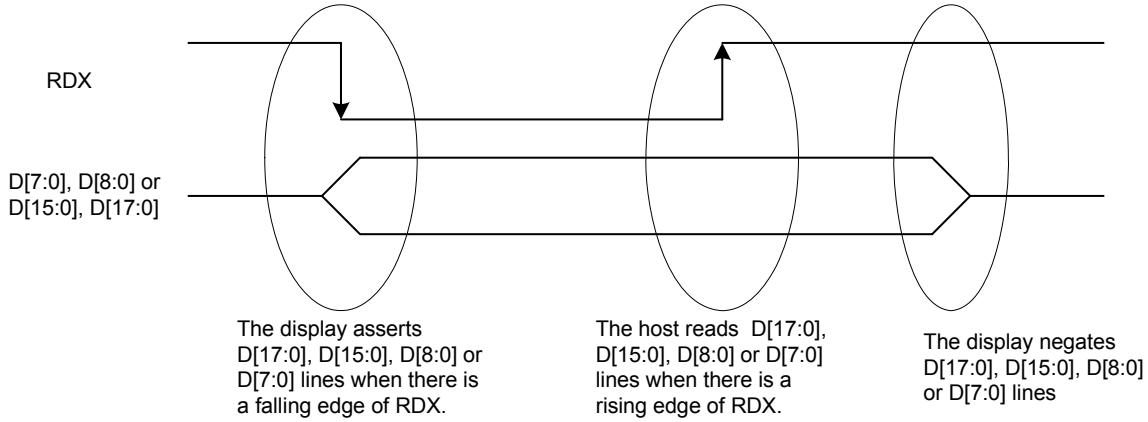




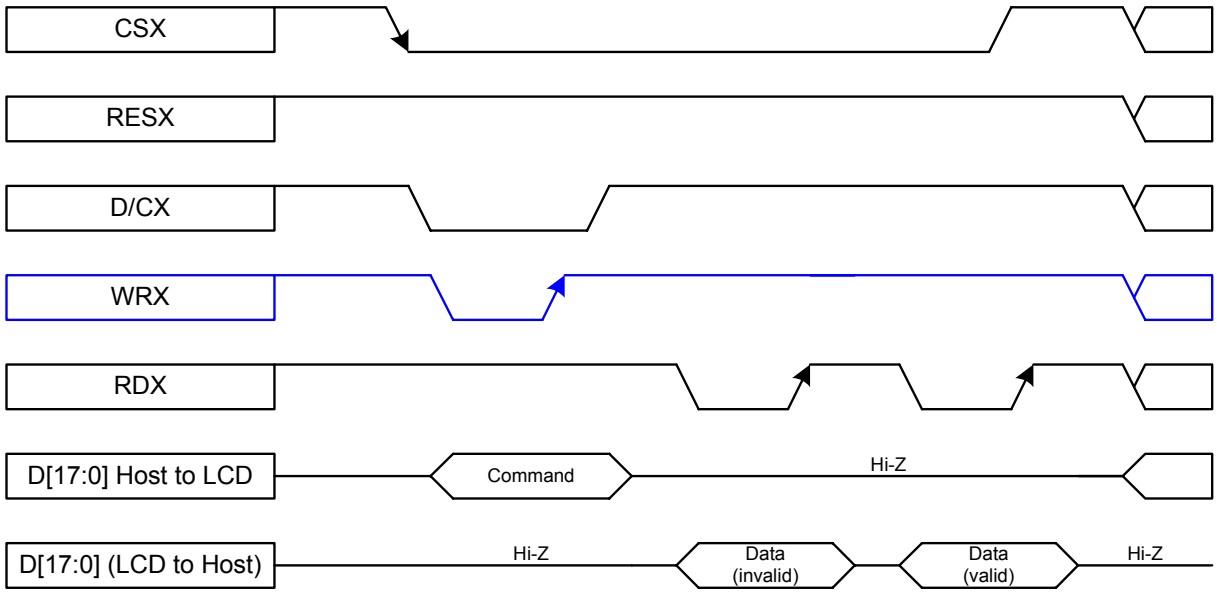
7.1.2. Read Cycle

During a read cycle the host processor reads data from the display module via the interface. The Type B interface utilizes D/CX, RDX and WRX signals as well as all eight (D[7:0]), nine (D[8:0]), sixteen (D[15:0]) or eighteen (D[17:0]) information signals. RDX is driven from high to low then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX. D/CX is driven high during the read cycle.

The following figure shows the read cycle for the type B interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read Data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

DBI Type B Interface

18-bit data bus DB[17:0] interface, IM[2:0] = 000

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*											D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

16-bit data bus DB[15:0] interface, IM[2:0] = 010

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*									D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

	Set_pixel_format	DFM	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

			First Transfer				Second Transfer				Third Transfer			
	Set_pixel_format	DFM	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
18bpp Frame Memory Write	3'h6	0	R1[5:0]		G1[5:0]		B1[5:0]		R2[5:0]		G2[5:0]		B2[5:0]	
		1			R1[5:0]		G1[5:0]		B1[5:0]				R2[5:0]	

			First Transfer				Second Transfer				Third Transfer			
	Set_pixel_format	DFM	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]	DB[15:10]	DB[9:8]	DB[7:2]	DB[1:0]
Frame Memory Read	*	0	r1[5:0]		g1[5:0]		b1[5:0]		r2[5:0]		g2[5:0]		b2[5:0]	
		1			r1[5:0]		g1[5:0]		b1[5:0]				r2[5:0]	

9-bit data bus DB[8:0] interface, IM[2:0] = 001

	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

			First Transfer									Second Transfer								
	Set_pixel_format	DFM	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[5]	r4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[5]	b[4]	b[3]	b[2]	b[1]	b[0]

8-bit data bus DB[7:0] interface, IM[2:0] = 011

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Command/Parameter Write	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Command/Parameter Read	*	*	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

			First Transfer								Second Transfer							
	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
16bpp Frame Memory Write	3'h5	*	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]
Frame Memory Read	*	*	r[4]	r[3]	r[2]	r[1]	r[0]	g[5]	g[4]	g[3]	g[2]	g[1]	g[0]	b[4]	b[3]	b[2]	b[1]	b[0]

			First Transfer								Second Transfer								Third Transfer							
	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	r[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

16-bit data extend to 18-bit

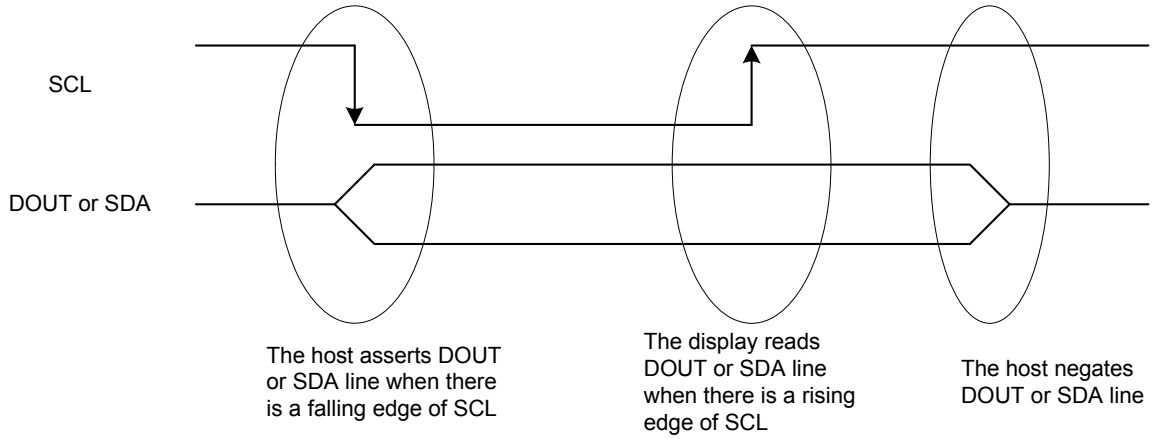
		Frame Memory Data (18bpp)																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
	2'h1	R4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R4]	R[3]	R[2]	R[1]	R[0]	R4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

7.2. Serial Interface (Type C)

7.2.1. Write Cycle and Sequence

During a write cycle the host processor sends a single bit of data to the display module via the interface. The Type C interface utilizes CSX, SCL and SDA or DOUT signals. SCL is driven from high to low then pulled back to high during the write cycle. The host processor provides information during the write cycle while the display module reads the host processor information on the rising edge of SCL.

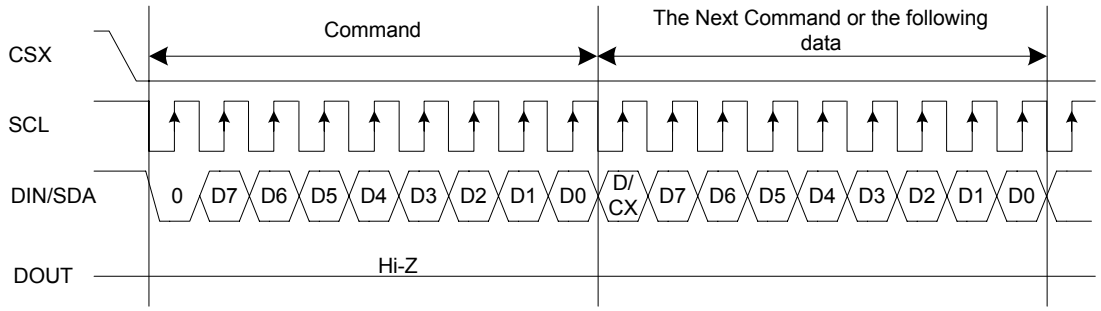
The following figure shows the write cycle for the type C interface.



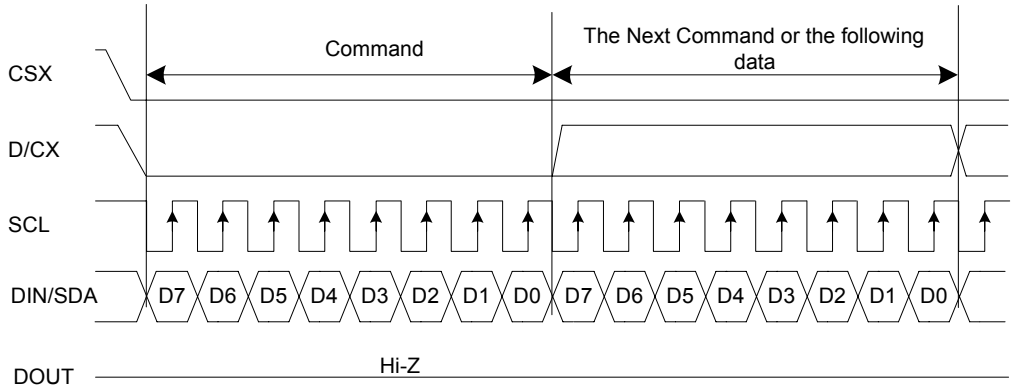
Note: SCL is an unsynchronized signal; it can be stopped.

During the write sequence the host processor writes one or more bytes of information to the display module via the interface. The write sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight write cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface write sequences are described in the following Figure



DBI Type C Interface Write Sequence – Option 1



DBI Type C Interface Write Sequence – Option 3

Note:

1. D7 is MSB and D0 is LSB of byte.
2. When the Interface control register (C6h) SDA_EN is set as '1', the DIN/SDA pin is bi-direction and DOUT pin is not used.
3. When the Interface control register (C6h) SDA_EN is set as '0', the DIN/SDA pin is uni-direction and DIN and DOUT pins are used for data write and read.

DBI Type C Interface IM[2:0]=101/111

	Set_pixel_format	DFM	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3bpp Frame Memory Write	3'h1	0			R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]			R3[0]	G3[0]	B3[0]	R4[0]	G4[0]	B4[0]			R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]
	3'h1	1		R1[0]	G1[0]	B1[0]		R2[0]	G2[0]	B2[0]		R3[0]	G3[0]	B3[0]		R4[0]	G4[0]	B4[0]		R5[0]	G5[0]	B5[0]		R6[0]	G6[0]	B6[0]
18bpp Frame Memory Write	3'h6	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]			G[5]	G[4]	G[3]	G[2]	G[1]	G[0]			B[5]	B[4]	B[3]	B[2]	B[1]	B[0]		
Frame Memory Read	*	*	r[5]	r[4]	R[3]	r[2]	r[1]	r[0]			g[5]	g[4]	g[3]	g[2]	g[1]	g[0]			b[5]	b[4]	b[3]	b[2]	b[1]	b[0]		

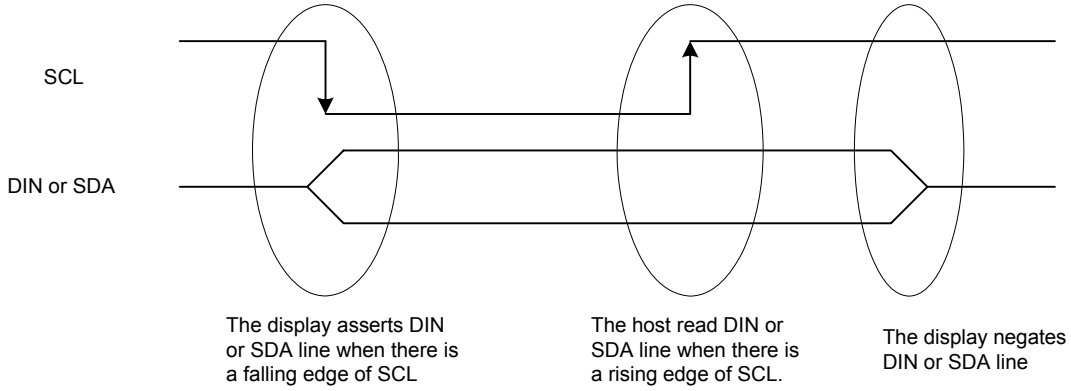
3/16-bit data extend to 18-bit

		Frame Memory Data (18bpp)																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
3bpp	*	R[0]	R[0]	R[0]	R[0]	R[0]	R[0]	G[0]	G[0]	G[0]	G[0]	G[0]	G[0]	B[0]	B[0]	B[0]	B[0]	B[0]	B[0]

7.2.2. Read Cycle and Sequence

During a read cycle the host processor reads a single bit of data from the display module via the interface. The Type C interface utilizes CSX, SCL and DIN signals. SCL is driven from high to low then pulled back to high during the read cycle. The display module provides information during the read cycle while the host processor reads the display module information on the rising edge of SCL. D/CX is driven during the read cycle if it is used in option 3.

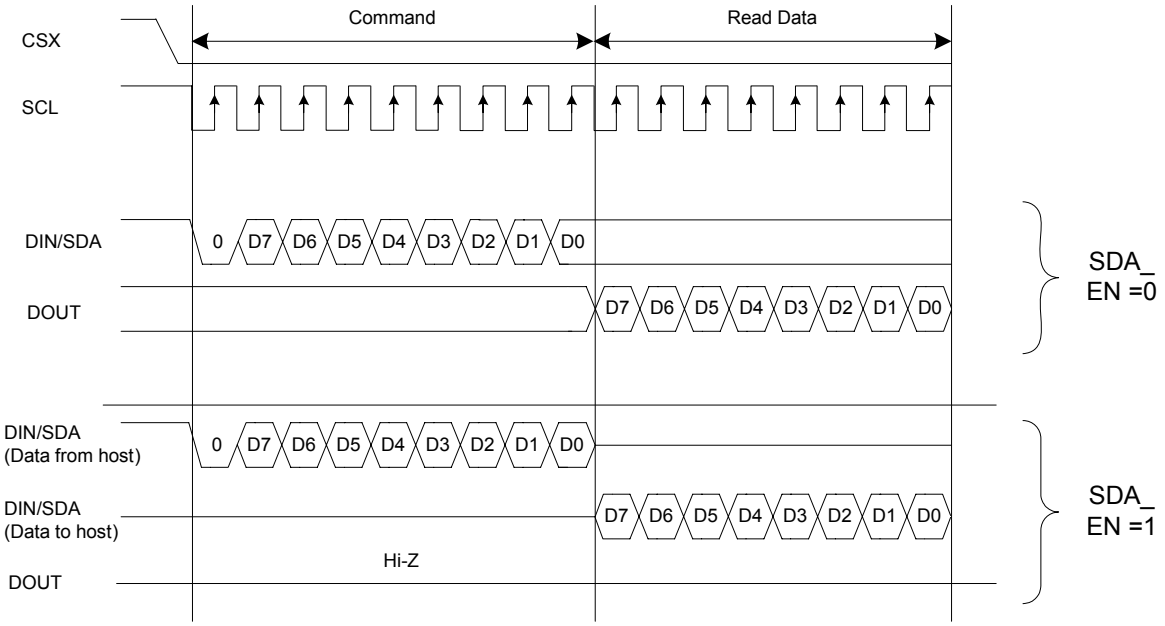
The following figure shows the read cycle for the type C interface.



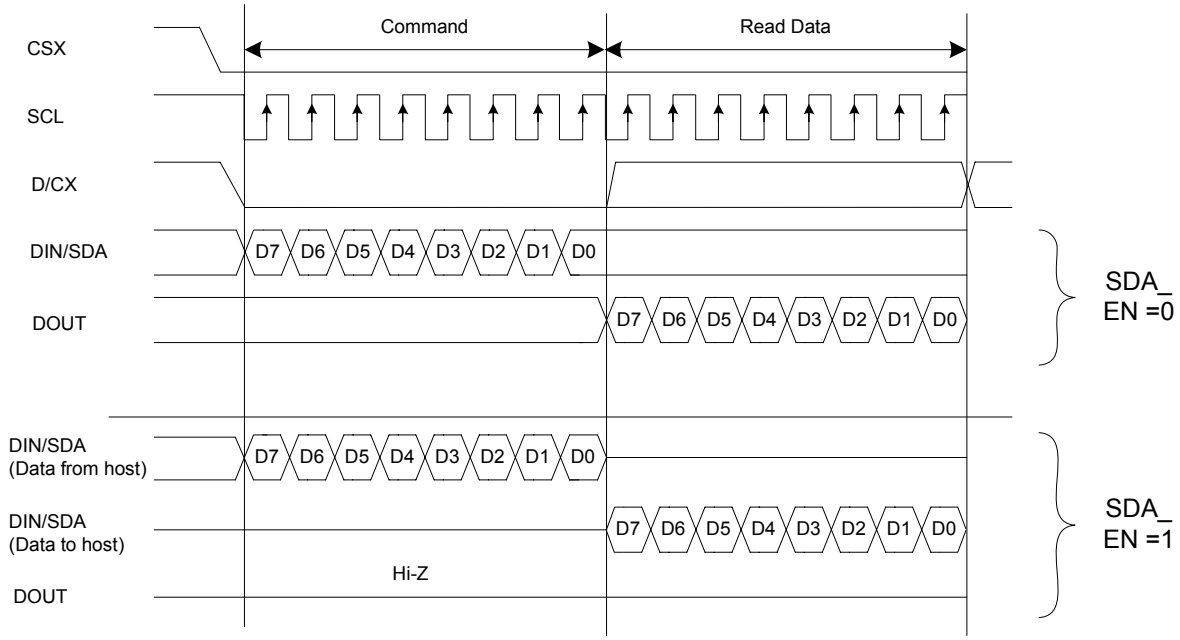
Note: SCL is an unsynchronized signal; it can be stopped.

During the read sequence the host processor reads one or more bytes of information from the display module via the interface. The read sequence is initiated when CSX is driven from high to low and ends when CSX is pulled high. Each byte is either nine or sixteen write cycles in length. If the optional D/CX signal is used a byte is eight read cycles long. D/CX is driven low while command information is on the interface and is pulled high when data is present.

The type C interface read sequences are shown in the following figures



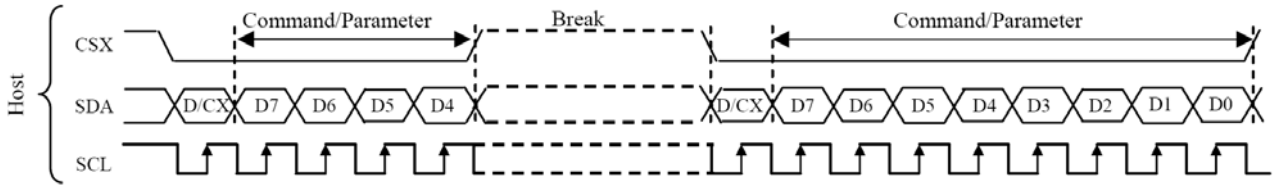
Note: D7 is MSB and D0 is LSB of byte.



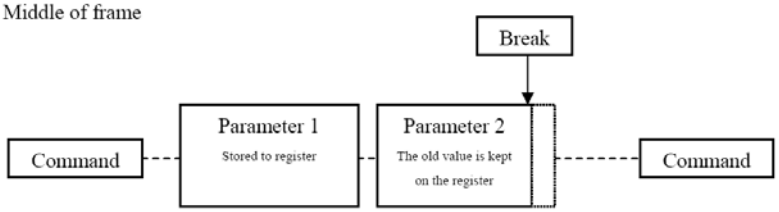
7.2.3. Break and Pause Sequences

The host processor can break a read or write sequence by pulling the CSX signal high during a command or data byte. The display module shall reset its interface so it will be ready to receive the same byte when CSX is again driven low.

The host processor can pause a read or write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the read or write sequence at the point where the sequence was paused.

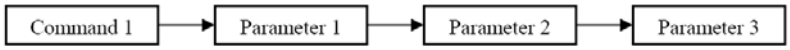


1. Middle of frame

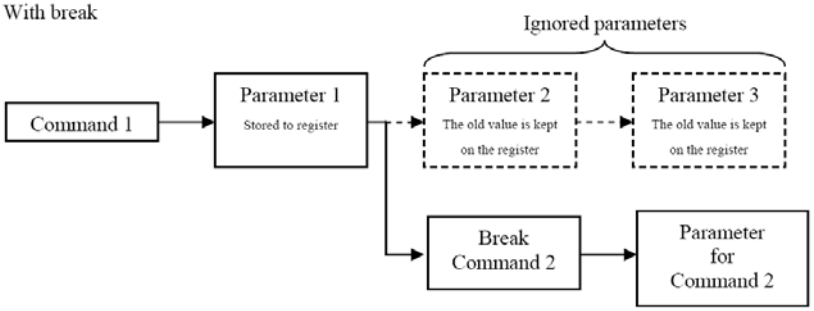


2. Between frames

Without break



With break



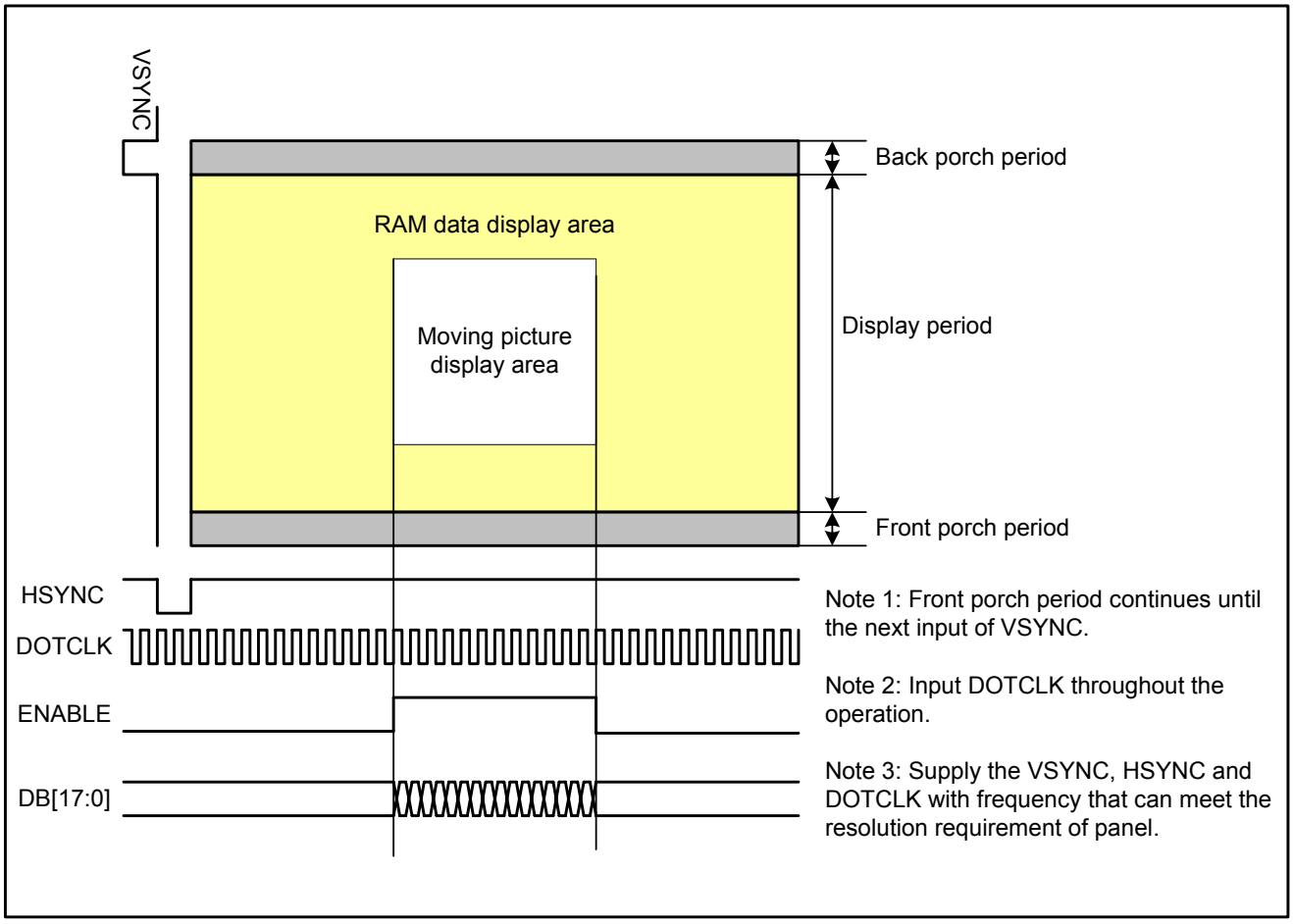
Break can be e.g. another command or noise pulse.

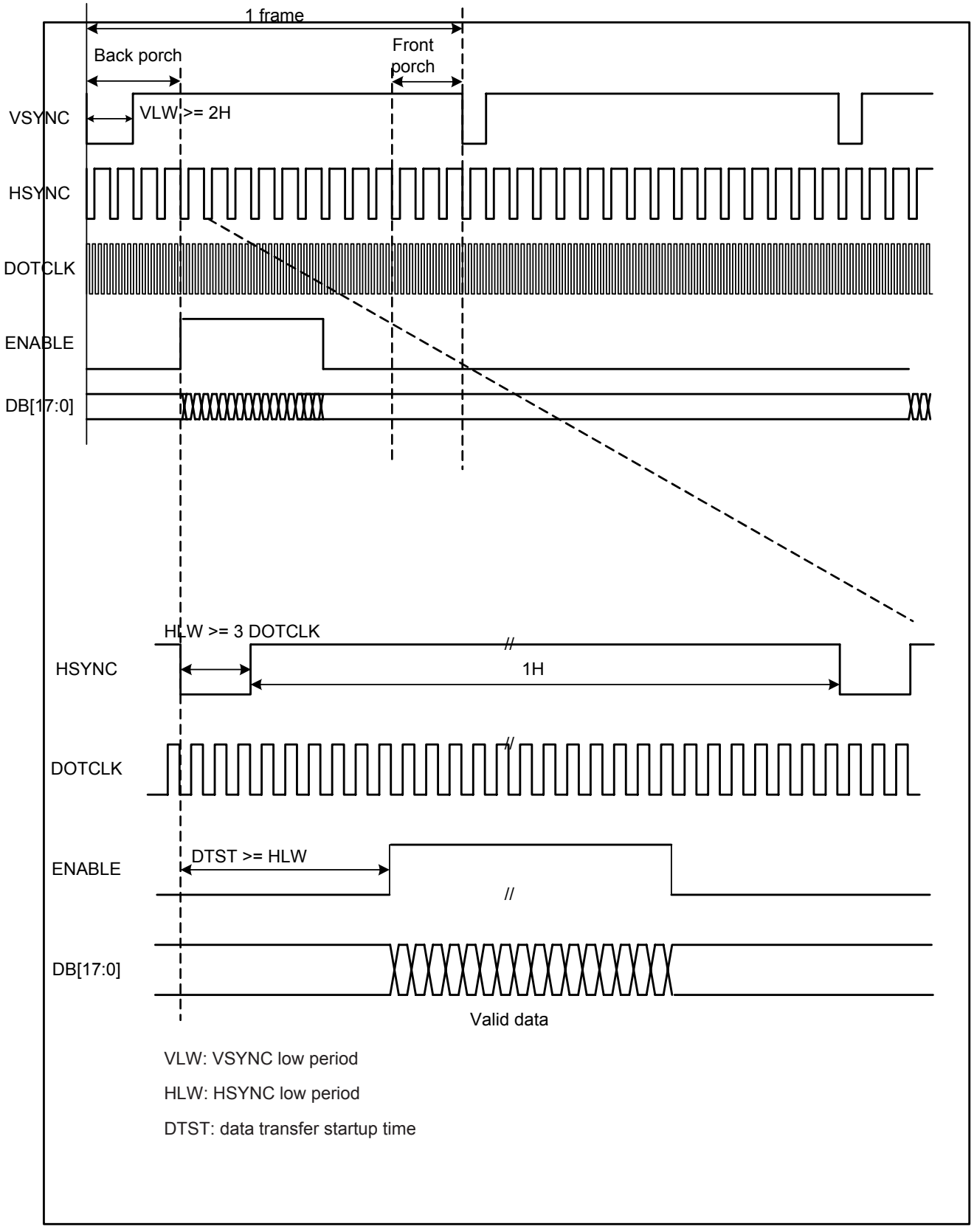
7.3. Display Pixel Interface (DPI)

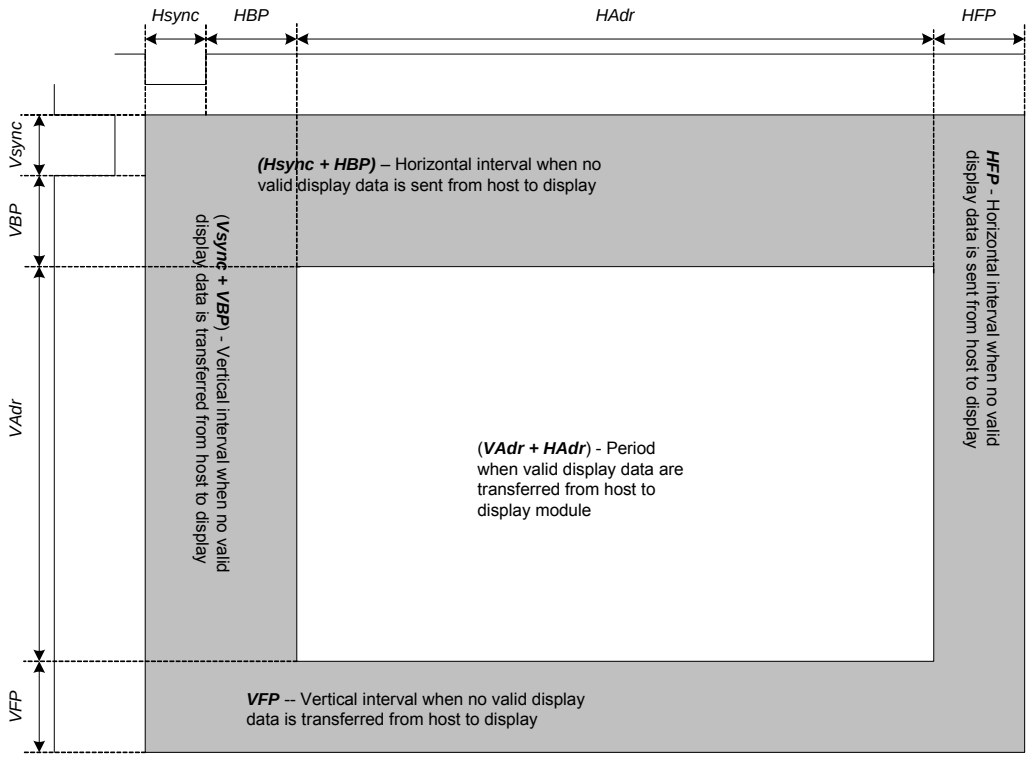
In normal operation, systems based on DPI architecture rely on the host processor to continuously provide complete frames of image data at a sufficient frame rate to avoid flicker or other visible artifacts. The displayed image, or frame, is comprised of a rectangular array of pixels. The frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync indicates the beginning of each frame of the displayed image.
Hsync signals the beginning of each horizontal line of pixels.

Each pixel value (16 or 18-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.





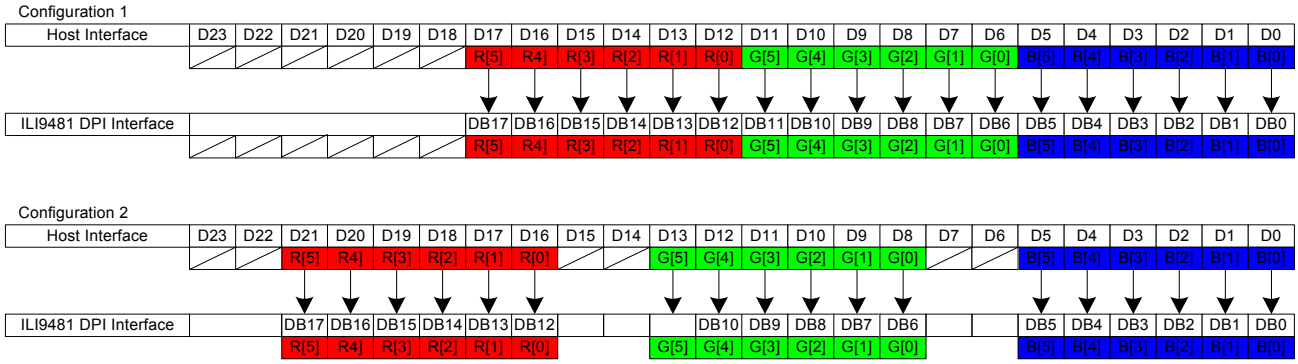


Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
PCLK Cycle	$PCLK_{CYC}$		-	125	104	ns
Horizontal Synchronization	Hsync		2	2	4	PCLK
Horizontal Back Porch	HBP		3	3	20	PCLK
Horizontal Address	HAdr		-	320	-	PCLK
Horizontal Front Porch	HFP		3	3	40	PCLK
Vertical Synchronization	Vsync		2	2	-	Line
Vertical Back Porch	VBP		2	2	30	Line
Vertical Address	VAdr		-	480	-	Line
Vertical Front Porch	VFP		2	4	30	Line
Vsync setup time	VSST					Hz
Vsync hold time	VSHT					Hz
Hsync setup time	HSST					Hz
Hsync hold time	HSHT					Hz
Data setup time	DST					Hz
Data hold time	DHT					Hz
Vertical Frequency(*)				50	60	Hz
Horizontal Frequency(*)			-	-	-	KHz
PCLK Frequency(*)			-	8	9.6	MHz

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

18bit DPI Interface Connection: set_pixel_format D[6:4]=3'h6：18bpp



16bit DPI Interface Connection: set_pixel_format D[6:4]=3'h5：16bpp

16-bit data extend to 18-bit

		Frame Memory Data (18bpp)																	
Set_pixel_format	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18bpp	*	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
16bpp	2'h0	R4]	R[3]	R[2]	R[1]	R[0]	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	0
	2'h1	R4]	R[3]	R[2]	R[1]	R[0]	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	1
	2'h2	R4]	R[3]	R[2]	R[1]	R[0]	R4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]

8. Command

8.1. Command List

Operational Code (Hex)	Command	Command(C) /Read(R) /Write(W)	Number Of Parameter	MIPI DCS Type1 Requirement	ILI9481 Implementation
00h	nop	C	0	Yes	Yes
01h	soft_reset	C	0	Yes	Yes
06h	get_red_channel	R	1	No	No
07h	get_green_channel	R	1	No	No
08h	get_blue_channel	R	1	No	No
0Ah	get_power_mode	R	1	Yes	Yes
0Bh	get_address_mode	R	1	Yes (Bit[7:0])	Yes (Bit[7:3]) , Only)
0Ch	get_pixel_format	R	1	Yes	Yes
0Dh	get_display_mode	R	1	Yes	Yes
0Eh	get_signal_mode	R	1	Yes	Yes
0Fh	get_diagnostic _result	R	1	Bit7/6：Yes Bit5/4：Optional	Yes (Bit7/6 Only)
10h	enter_sleep_mode	C	0	Yes	Yes
11h	exit_sleep_mode	C	0	Yes	Yes
12h	enter_partial_mode	C	0	Yes	Yes
13h	enter_normal_mode	C	0	Yes	Yes
20h	exit_invert_mode	C	0	Yes	Yes
21h	enter_invert_mode	C	0	Yes	Yes
26h	set_gamma_curve	W	1	Yes	No
28h	set_display_off	C	0	Yes	Yes
29h	set_display_on	C	0	Yes	Yes
2Ah	set_column_address	W	4	Yes	Yes
2Bh	set_page_address	W	4	Yes	Yes
2Ch	write_memory_start	W	Variable	Yes	Yes
2Dh	wite_LUT	W	Variable	Optional	No
2Eh	read_memory_start	R	Variable	Yes	Yes
30h	set_partial_area	W	4	Yes	Yes
33h	set_scroll_area	W	6	Yes	Yes
34h	set_tear_off	C	0	Yes	Yes
35h	set_tear_on	W	1	Yes	Yes
36h	set_address_mode	W	1	Yes (Bit7-0)	Yes (Bit[7:3], Bit[1:0] Only)
37h	set_scroll_start	W	2	Yes	Yes
38h	exit_idle_mode	C	0	Yes	Yes
39h	enter_idle_mode	C	0	Yes	Yes
3Ah	set_pixel_format	W	1	Yes	Yes
3Ch	write_memory _continue	W	Variable	Yes	Yes
3Eh	read_memory _continue	R	Variable	Yes	Yes
44h	set_tear_scanline	W	2	Yes	Yes
45h	get_scanline	R	3	Yes	Yes
A1h	read_DDB_start	R	6	Yes	Yes

Operational Code (Hex)	Function	Command(C) Read(R)/Write(W)	Number Of Parameter
B0h	Command Access Protect	W/R	1
B3h	Frame Memory Access and Interface setting	W/R	4
B4h	Display Mode and Frame Memory Write Mode setting	W/R	1
BFh	Device code Read	R	6
C0h	Panel Driving Setting	W/R	5
C1h	Display Timing Setting for Normal Mode	W/R	3
C2h	Display Timing Setting for Partial Mode	W/R	3
C3h	Display Timing Setting for Idle Mode	W/R	3
C5h	Frame rate and Inversion Control	W/R	1
C6h	Interface Control	W/R	1
C8h	Gamma Setting	W/R	12
D0h	Power Setting	W/R	3
D1h	VCOM Control	W/R	3
D2h	Power Setting for Normal Mode	W/R	2
D3h	Power Setting for Partial Mode	W/R	2
D4h	Power Setting for Idle Mode	W/R	2
E0h	NV Memory Write	W/R	1
E1h	NV Memory Control	W/R	1
E2h	NV Memory Status	R	3
E3h	NV Memory Protection	W/R	2
B0～FF Except above command	LSI TEST Registers	W/R	Variable

8.2. Command Description

8.2.1. NOP (00h)

00H	NOP (No Operation)												
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart: None

8.2.2. Soft_reset (01h)

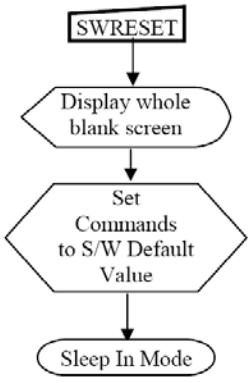
01H	Soft_reset												
	D/CX	RDX	WRX	D17-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are affected by this command. X = Don't care												
Restriction	Software Reset Command cannot be sent during Sleep Out sequence. Any new command is cannot be sent for 10-frame period until the ILI9481 enters Sleep-In mode. Do not send any command.												
Register Availability													

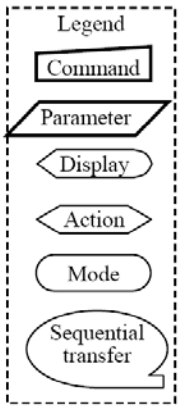
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

Flow Chart





8.2.3. Get_power_mode (0Ah)

0AH	Get_power_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	0	0A
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Not Defined	Set to '0'
D6	Idle Mode On/Off	
D5	Partial Mode On/Off	
D4	Sleep In/Out	
D3	Display Normal Mode On/Off	
D2	Display On/Off	
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D7 – Booster Voltage Status

'0' = Booster Off or has a fault.

'1' = Booster On and working OK (Meets Nokia's optical requirements).

Bit D6 - Idle Mode On/Off

'0' = Idle Mode Off.

'1' = Idle Mode On.

Bit D5 – Partial Mode On/Off

'0' = Partial Mode Off.

'1' = Partial Mode On.

Bit D4 – Sleep In/Out

'0' = Sleep In Mode.

'1' = Sleep Out Mode.

Bit D3 – Display Normal Mode On/Off

'0' = Display Normal Mode Off.

'1' = Display Normal Mode On.

Bit D2 – Display On/Off

'0' = Display is Off.

'1' = Display is On.

Bit D1 – Not Defined

'This bit is not applicable for this project, so it is set to '0'

Bit D0 – Not Defined

'This bit is not applicable for this project, so it is set to '0'

X = Don't care

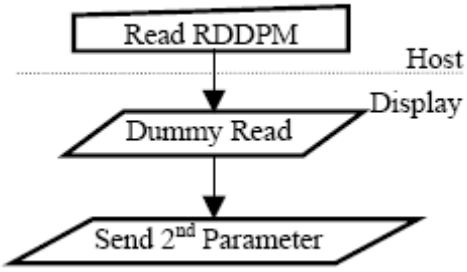
Register Availability

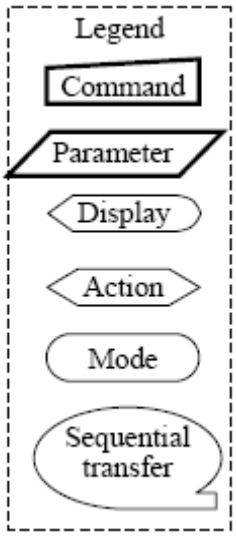
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08_{HEX}
SW Reset	08_{HEX}
HW Reset	08_{HEX}

Flow Chart





8.2.4. Get_address_mode (0Bh)

0BH	Get_address_mode												
	D/CX	RDX	WRX	D17-0	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	0	1	1	0B
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	D7	D6	D5	D4	D3	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	
D6	Column Address Order	
D5	Page/Column Order	
D4	Line Address Order	
D3	RGB/BGR Order	
D2	Reserved	Set to '0'
D1	Reserved	Set to '0'
D0	Reserved	Set to '0'

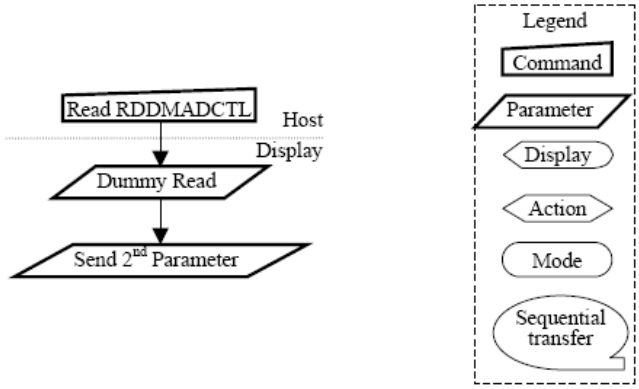
- Bit D7 – Page Address Order
  '0' = Top to Bottom
  '1' = Bottom to Top
- Bit D6 – Column Address Order
  '0' = Left to Right
  '1' = Right to Left
- Bit D5 - Page/Column Order
  '0' = Normal Mode
  '1' = Reverse Mode
  Note: For Bits D7 to D5, also refer to Section 8.2.3 MCU to memory write/read direction.
- Bit D4 – Line Address Order
  '0' = LCD Refresh Top to Bottom
  '1' = LCD Refresh Bottom to Top
- Bit D3 – RGB/BGR Order
  '0' = RGB
  '1' = BGR

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00_{HEX}
SW Reset	**No Change**
HW Reset	00_{HEX}

Flow Chart	

8.2.5. Get_pixel_format (0Ch)

0CH	Get_pixel_format												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	0	0C
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	0	D6	D5	D4	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

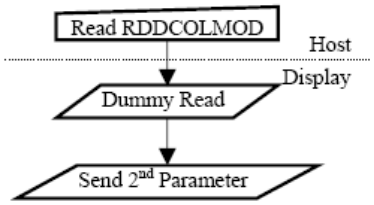
Bit	Description
D7	DPI Pixel Format (RGB Interface Color Format)
D6	
D5	
D4	
D3	DBI Pixel Format (Control Interface Color Format)
D2	
D1	
D0	

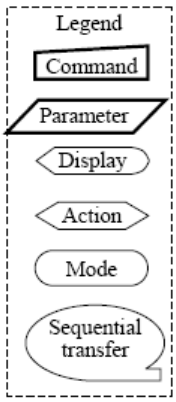
Pixel Format	D6/D2	D5/D1	D4/D0
Reserved	0	0	0
3 bits / pixel	0	0	1
Reserved	0	1	0
Reserved	0	1	1
Reserved	1	0	0
16 bits / pixel	1	0	1
18 bits / pixel	1	1	0
Reserved	1	1	1

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart





8.2.6. Get_display_mode (0Dh)

0DH	Get_display_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	0	1	0D
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	0	0	0	0	0	0	0	0	xx

Description

The display module returns the Display Image Mode status.

Bit	Description	Symbol
D7	Vertical Scrolling Status	VSSON
D6	Reserved	
D5	Inversion On/Off	DSPINVON
D4	Reserved	
D3	Reserved	
D2	Gamma Curve Selection	
D1	Gamma Curve Selection	
D0	Gamma Curve Selection	

This command indicates the current status of the display as described in the table below:

- Bit D7 – Vertical Scrolling On/Off

  '0' = Vertical Scrolling is Off.

  '1' = Vertical Scrolling is On.

- Bit D6 – Reserved
- Bit D5 – Inversion On/Off

  '0' = Inversion is Off.

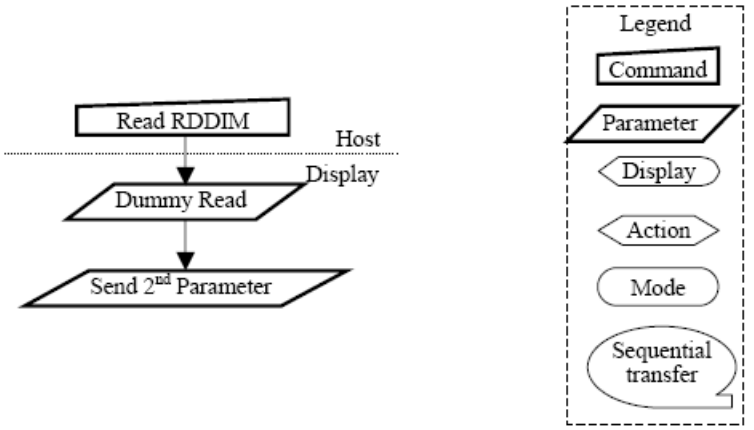
  '1' = Inversion is On.

- Bit D4 – Reserved
- Bit D3 – Reserved
- Bits D2, D1, D0 – Gamma Curve Selection

  These bits are not applicable for this project, so they are set to '000'

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart	

8.2.7. Get_signal_mode (0Eh)

0EH	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	0	0E
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	xx

Description

The display module returns the Display Signal Mode.

Bit	Description	Symbol
D7	Tearing Effect Line On/Off	TEON
D6	Tearing Effect Line Output Mode	TELOM
D5	Reserved	
D4	Reserved	
D3	Reserved	
D2	Reserved	
D1	Reserved	
D0	Reserved	

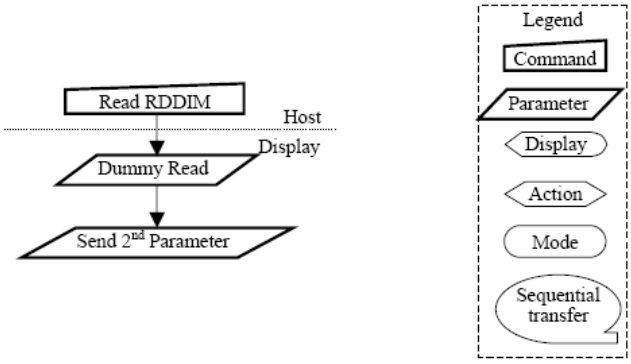
This command indicates the current status of the display as described in the table below:

- Bit D7 – Tearing Effect Line On/Off
  - '0' = Tearing Effect Line Off.
  - '1' = Tearing Effect On.
- Bit D6 – Tearing Effect Line Output Mode, see section 8.3 for mode definitions.
  - '0' = Mode 1.
  - '1' = Mode 2.
- Bit D[5:0] – Reserved

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart



8.2.8. Get_diagnostic_result (0Fh)

0FH	Get_diagnostic_result												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	0	1	1	1	1	0F
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	D7	D6	0	0	0	0	0	0	xx

Description

The display module returns the self-diagnostic results following a Sleep Out command.

Bit	Description	Symbol
D7	Register Loading Detection	SDR
D6	Functionality Detection	FUNCD
D5	Chip attachment Detection	Set '0'
D4	Display Glass Break Detection	Set '0'
D3	Reserved	Set '0'
D2	Reserved	Set '0'
D1	Reserved	Set '0'
D0	Reserved	Set '0'

Bit D7 – Register Loading Detection

Bit D6 – Functionality Detection

Bit D5 – Chip Attachment Detection

Set to '0' if feature unimplemented.

Bit D4 – Display Glass Break Detection

Set to '0' if feature unimplemented.

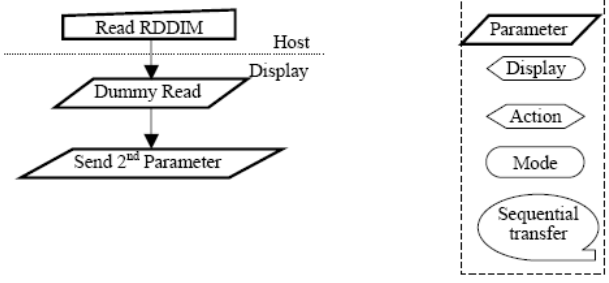
Bits D[3:0] – Reserved

Set to '0'.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

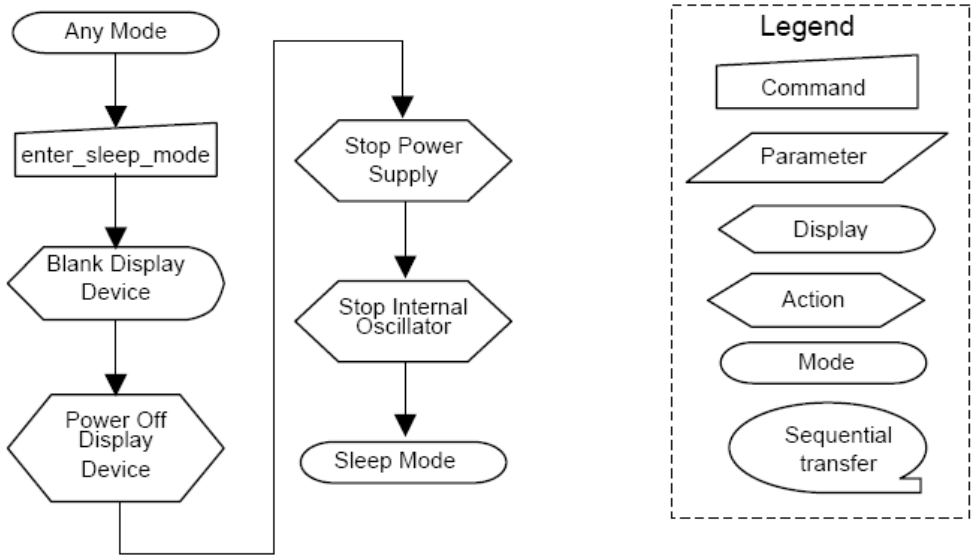
Flow Chart



8.2.9. Enter_sleep_mode (10h)

<table>
<tr><th>10H</th><th colspan="13">Enter_sleep_mode</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>x</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the display module to enter the Sleep mode.
This command causes the LCD module to enter the Sleep mode. In this mode, the DC/DC converter, internal oscillator and panel scanning stop.

DBI or DSI Command Mode remains operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information to Type 2 and Type 3 display modules for two frames after this command is sent when the display module is in Normal mode.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when the display module is already in Sleep mode.
The host processor must wait five milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.
The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>SW Reset</td><td>Sleep In Mode</td></tr><tr><td>HW Reset</td><td>Sleep In Mode</td></tr></table></td></tr>
</table>

Flow Chart	

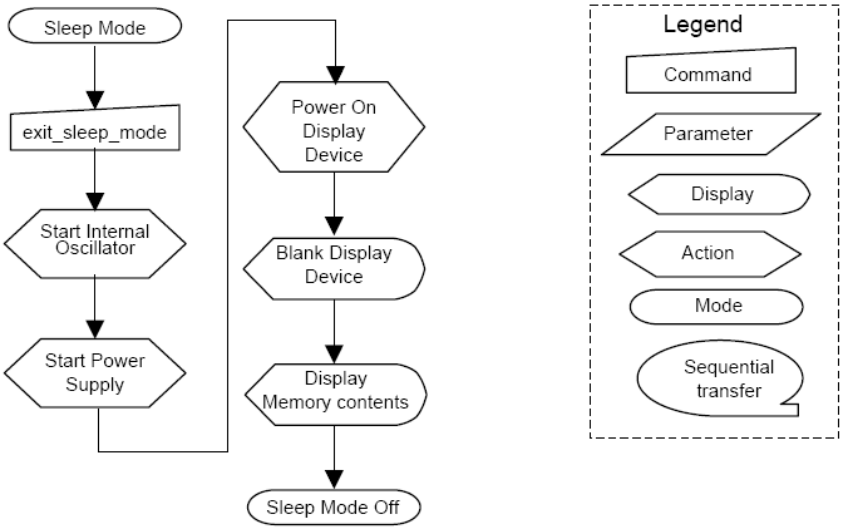
8.2.10. Exit_sleep_mode (11h)

11H	Exit_sleep_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	0	1	11
Parameter	No Parameter												
Description	This command causes the display module to exit Sleep mode. All blocks inside the display module are enabled. The host processor sends PCLK, HS and VS information to Type 2 and Type 3 display modules two frames before this command is sent when the display module is in Normal Mode.												
Restriction	This command shall not cause any visible effect on the display device when the display module is not in Sleep mode. The host processor must wait five milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize. The host processor must wait 120 milliseconds after sending an exit_sleep_mode command before sending an enter_sleep_mode command. The display module loads the display module's default values to the registers when exiting the Sleep mode. There shall not be any abnormal visual effect on the display device when loading the registers if the factory default and register values are the same or when the display module is not in Sleep mode. The display module runs the self-diagnostic functions after this command is received. See section 5.3 for a description of the self-diagnostic functions.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
SW Reset	Sleep In Mode
HW Reset	Sleep In Mode

Flow Chart	

8.2.11. Enter_Partial_mode (12h)

12H	Enter_Partial_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	1	0	12
Parameter	No Parameter												
Description	This command causes the display module to enter the Partial Display Mode. The Partial Display Mode window is described by the set_partial_area (30h) command. To leave Partial Display Mode, the enter_normal_mode (13h) command should be written. The host processor continues to send PCLK, HS and VS information to Type 2 display modules for two frames after this command is sent when the display module is in Normal Display Mode.												
Restriction	This command has no effect when Partial Display Mode is already active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

Flow Chart	Refer to Partial Area (30h)

8.2.12. Enter_normal_mode (13h)

13H	Enter_normal_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	0	1	0	0	1	1	13
Parameter	No Parameter												
Description	This command causes the display module to enter the Normal mode. Normal Mode is defined as Partial Display mode and Scroll mode are off. The host processor sends PCLK, HS and VS information to Type 2 display modules two frames before this command is sent when the display module is in Partial Display Mode.												
Restriction	This command has no effect when Normal Display mode is already active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

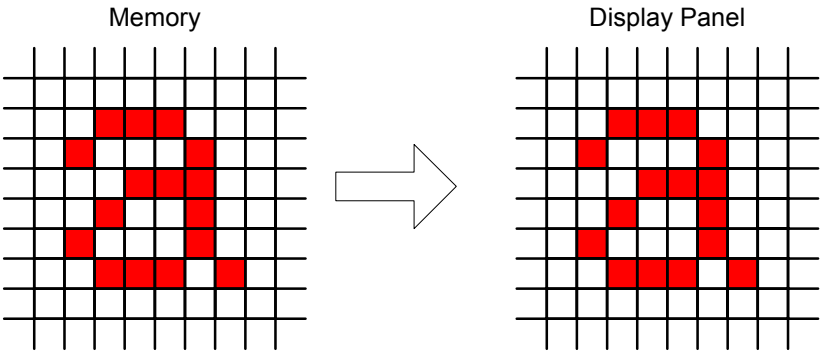
Flow Chart	Refer to the description of set_partial_area(30h) and set_scroll_area(33h)

8.2.13. Exit_invert_mode (20h)

20H	Exit_invert_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	0	20
Parameter	No Parameter												

Description

This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.



Restriction

This command has no effect when the display module is not inverting the display image.

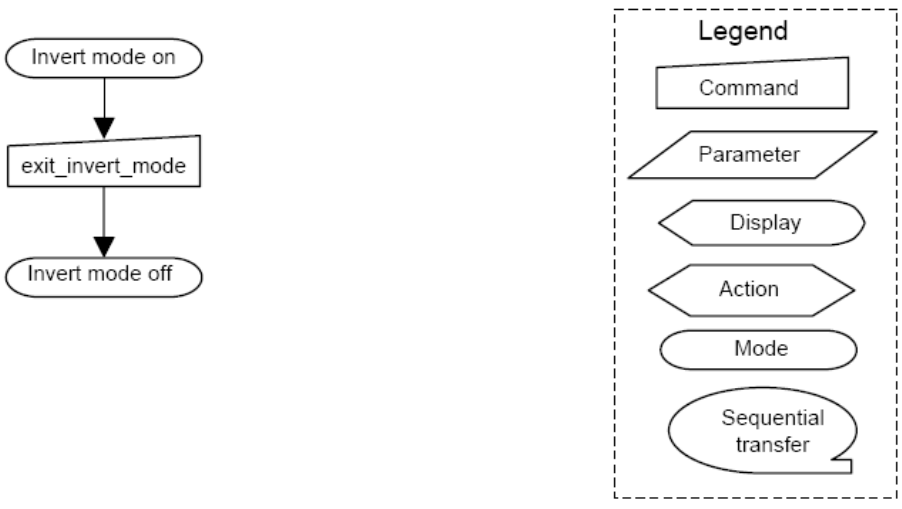
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Exit_invert_mode
SW Reset	Exit_invert_mode
HW Reset	Exit_invert_mode

Flow Chart

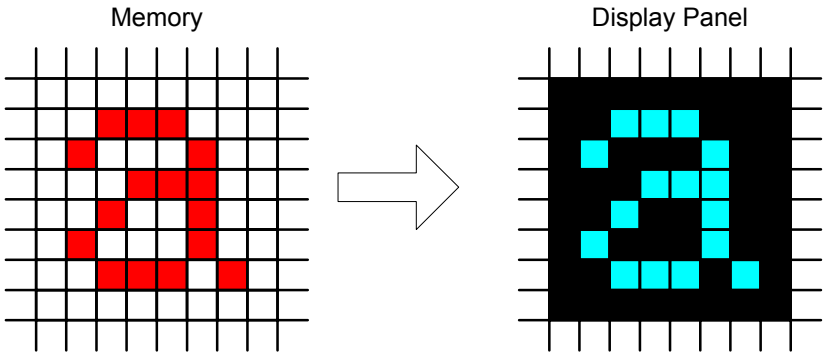


8.2.14. Enter_invert_mode (21h)

21H	Enter_invert_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	0	0	0	1	21
Parameter	No Parameter												

Description

This command causes the display module to invert the image data only on the display device. The frame memory contents remain unchanged. No status bits are changed.



Restriction

This command has no effect when module is already in inversion on mode.

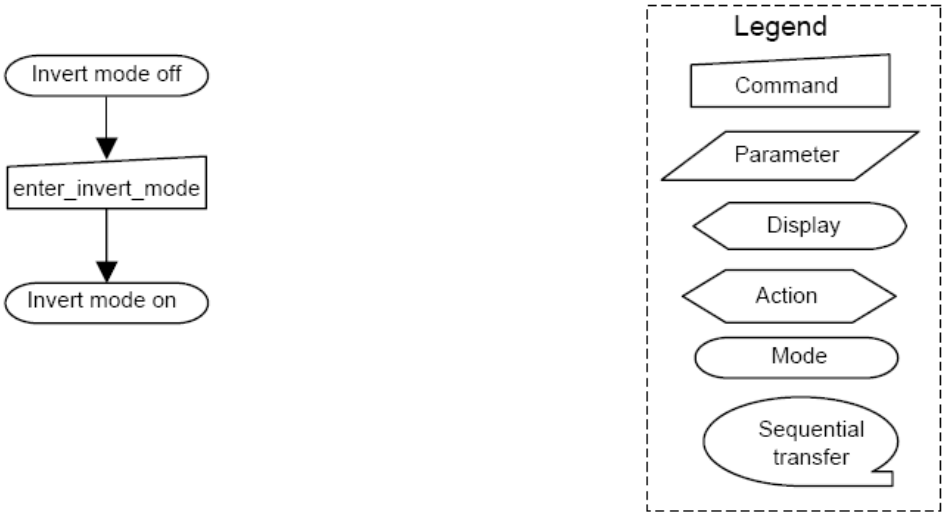
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Exit_invert_mode
SW Reset	Exit_invert_mode
HW Reset	Exit_invert_mode

Flow Chart

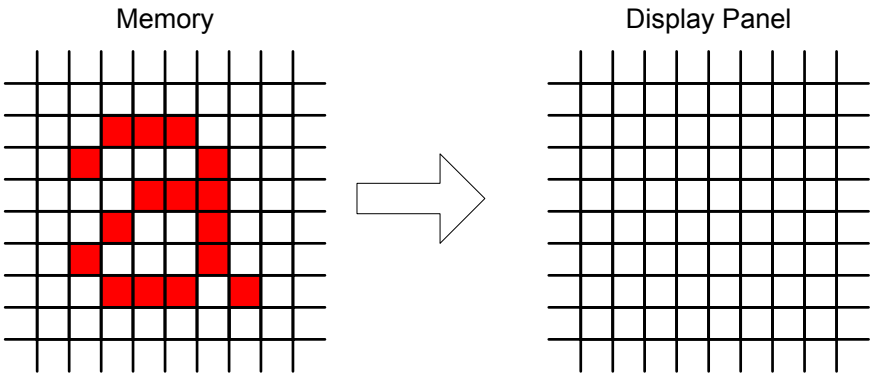


8.2.15. Set_display_off (28h)

28H	Set_display_off												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	0	28
Parameter	No Parameter												

Description

This command causes the display module to stop displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.



Restriction

This command has no effect when module is already in display off mode.

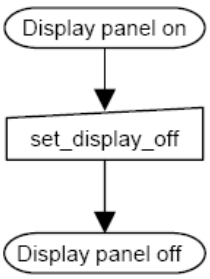
Register Availability

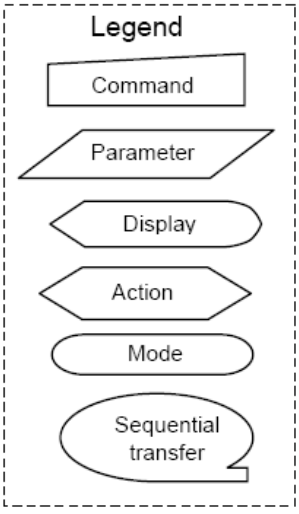
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

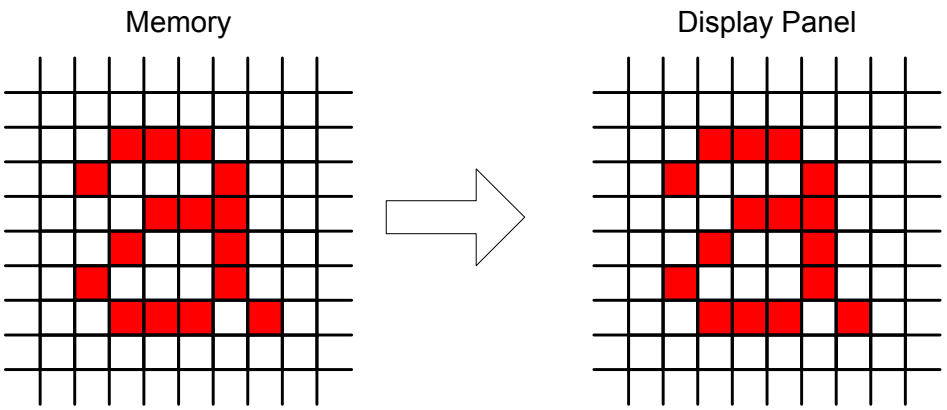
Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart





8.2.16. Set_display_on (29h)

29H	Set_display_on												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	0	1	29
Parameter	No Parameter												
Description	This command causes the display module to start displaying the image data on the display device. The frame memory contents remain unchanged. No status bits are changed. 												
Restriction	This command has no effect when module is already in display on mode.												

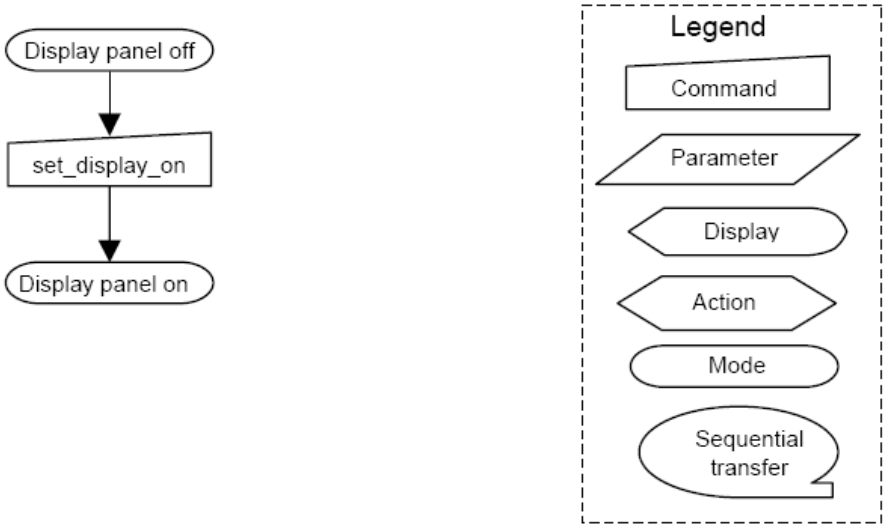
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
SW Reset	Display Off
HW Reset	Display Off

Flow Chart

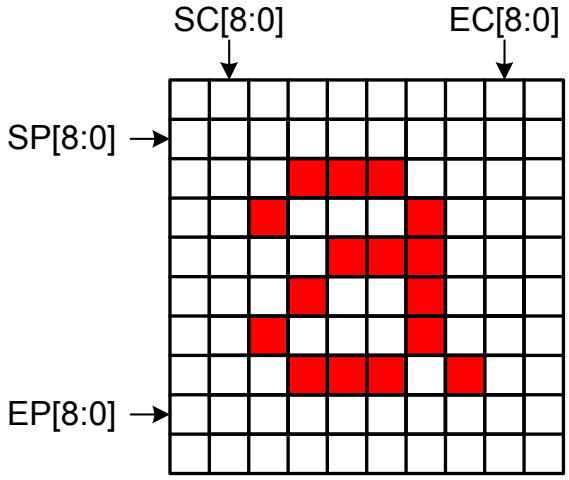


8.2.17. Set_column_address (2Ah)

2AH	Set_column_address												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	0	2A
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SC8	Note
2nd Parameter	1	1	↑	x	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	1
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EC8	Note
4th Parameter	1	1	↑	x	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	2

Description

This command defines the column extent of the frame memory accessed by the host processor with the read_memory_continue and write_memory_continue commands. No status bits are changed.



Restriction

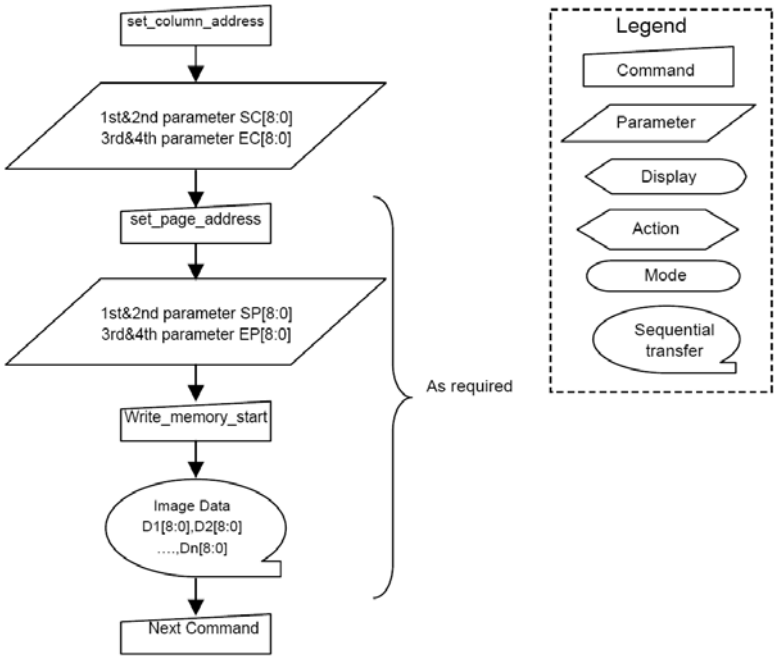
SC [8:0] always must be equal to or less than EC[8:0]. If SC[8:0] or EC[8:0] is greater than the available frame memory then the parameter is not updated.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC[8:0]=0000_{HEX}	SC[8:0]=000_{HEX} SE[8:0]=$013F_{HEX}$
SW Reset	SC[8:0]=0000_{HEX}	If Set_address_mode(36h) B5=0 : EC[8:0]=$013F_{HEX}$ If Set_address_mode(36h) B5=1 : EC[8:0]=$01DF_{HEX}$
HW Reset	SC[8:0]=0000_{HEX}	SC[8:0]=000_{HEX} SE[8:0]=$013F_{HEX}$

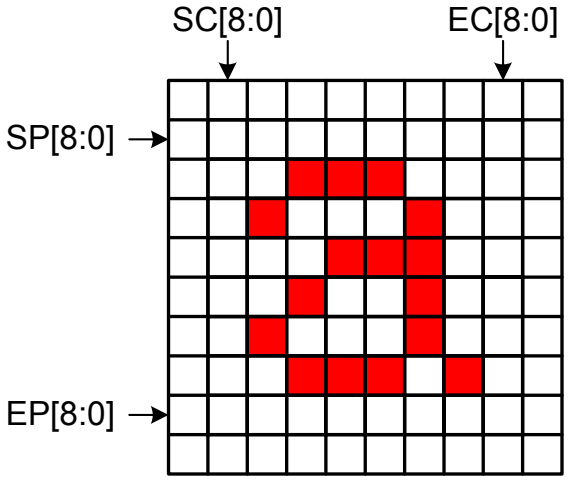
Flow Chart	

8.2.18. Set_page_address (2Bh)

2BH	Set_page_address												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	0	1	1	2B
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SP8	xxx
2nd Parameter	1	1	↑	x	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	EP8	xxx
4th Parameter	1	1	↑	x	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command defines the page extent of the frame memory accessed by the host processor with the write_memory_continue and read_memory_continue command. No status bits are changed.



Restriction

SP [8:0] always must be equal to or less than EP [8:0].

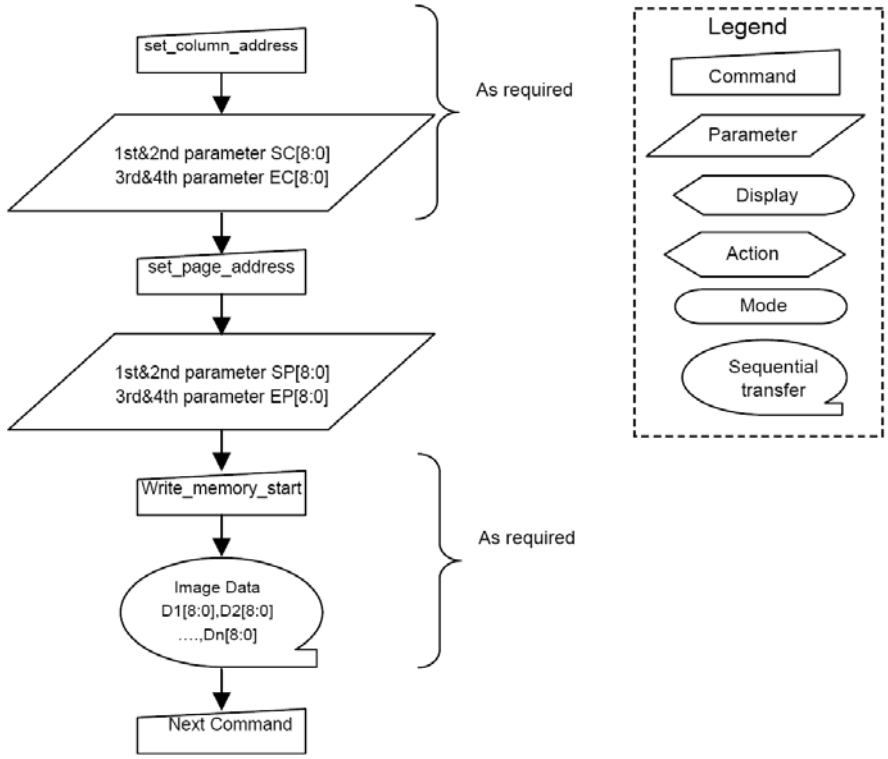
If SP[8:0] or EP[8:0] is greater than the available frame memory then the parameter is not updated.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP[8:0]=0000_{HEX}	EP[8:0]=$01DF_{HEX}$
SW Reset	SP[8:0]=0000_{HEX}	If Set_address_mode(36h) B5=0 : EP[8:0]=$01DF_{HEX}$ If Set_address_mode(36h) B5=1 : EP[8:0]=$013F_{HEX}$
HW Reset	SP8:0]=0000_{HEX}	EP[8:0]=$01DF_{HEX}$

Flow Chart	

8.2.19. Write_memory_start (2Ch)

2CH	Write_memory_start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	0	0	1	0	1	1	0	0	2C
1st pixel data	1	1	↑	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00000..3FFF
:	1	1	↑	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00000..3FFF
NTH pixel data	1	1	↑	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00000..3FFF

Description

This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address (2Ah) and set_page_address (2Bh) commands.

If set_address_mode (36h) B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode (36h) B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Restriction

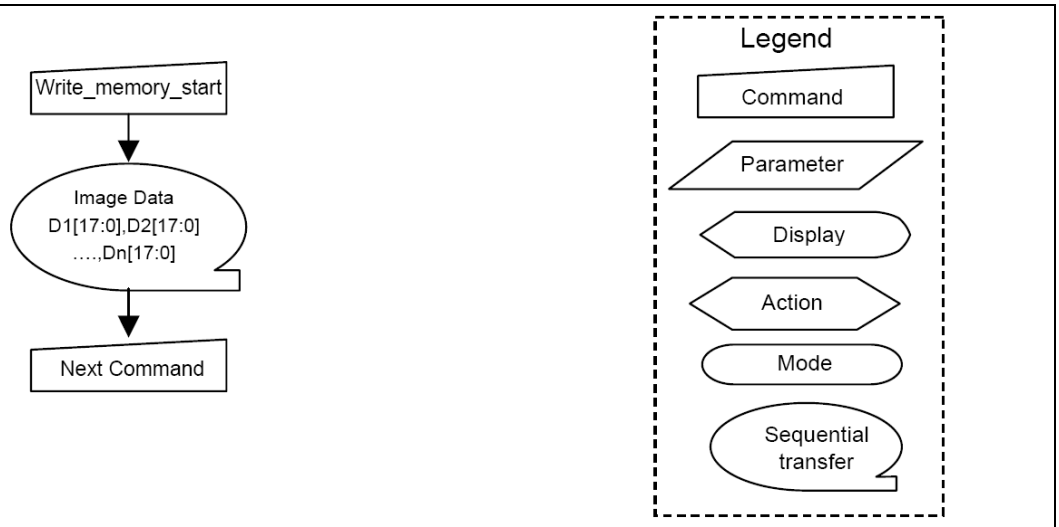
A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write location. Otherwise, data written with write_memory_start and any following write_memory_continue commands is written to undefined locations..

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	

8.2.20. Read_memory_start (2Eh)

2EH	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	0	1	1	1	0	2E
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	D1 [17..8]	D1 7	D1 6	D1 5	D1 4	D1 3	D1 2	D1 1	D1 0	00000..3FF
:	1	↑	1	Dx [17..8]	Dx 7	Dx 6	Dx 5	Dx 4	Dx 3	Dx 2	Dx 1	Dx 0	00000..3FF
(N+1)TH Parameter	1	↑	1	Dn [17..8]	Dn 7	Dn 6	Dn 5	Dn 4	Dn 3	Dn 2	Dn 1	Dn 0	00000..3FF

Description

This command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If set_address_mode B5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If set_address_mode B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

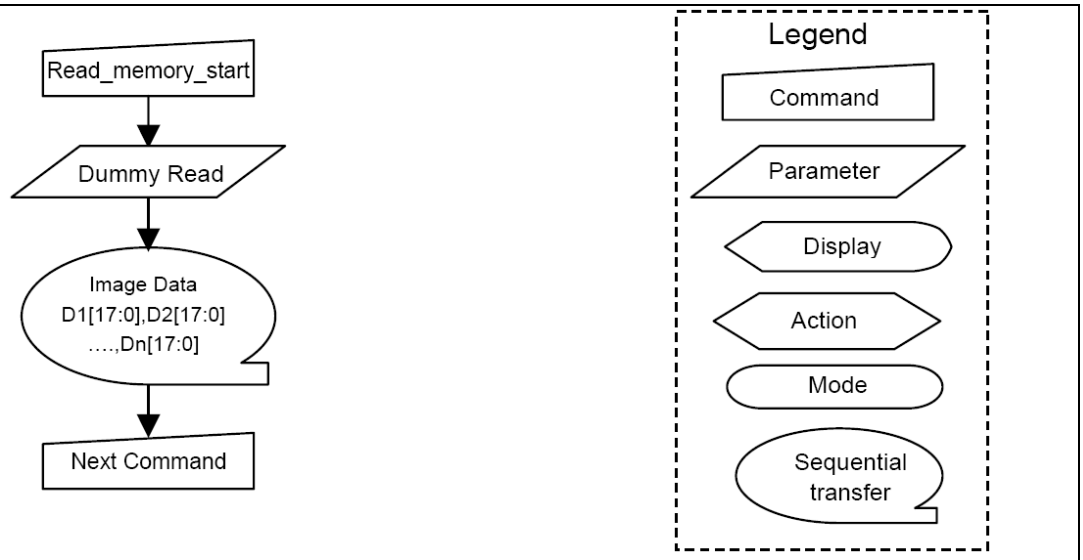
A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	

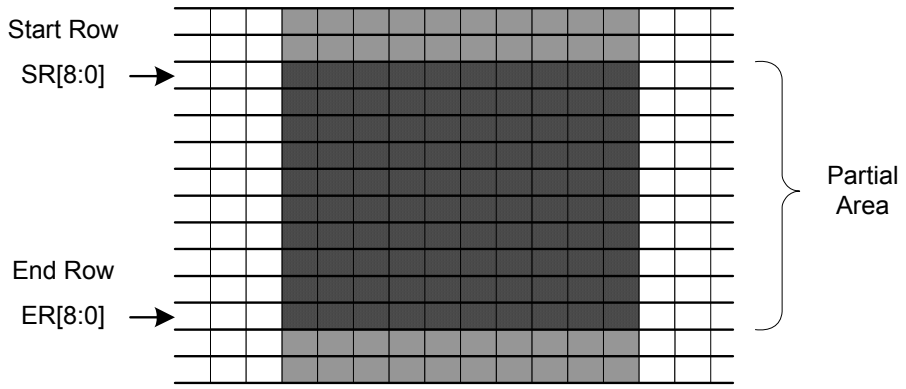
8.2.21. Set_partial_area (30h)

30H	Set_partial_area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	0	0	30
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	SR8	000..1DFh
2nd Parameter	1	1	↑	x	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	ER8	000..1DFh
4th Parameter	1	1	↑	x	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	

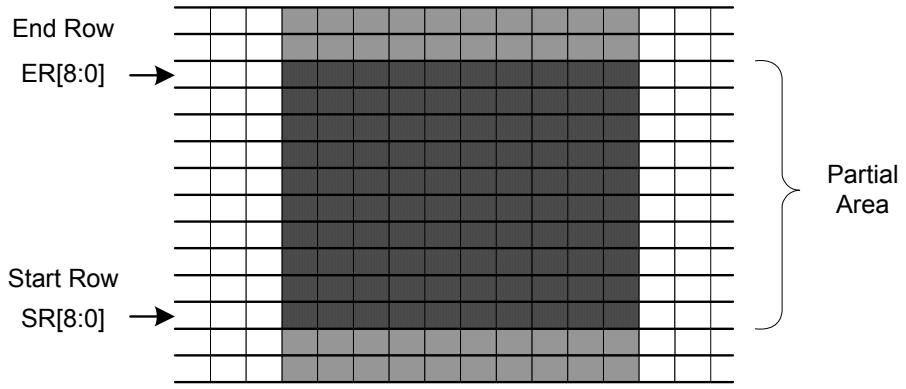
Description

This command defines the Partial Display mode's display area. There are two parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the following figure. SR and ER refer to the Frame Memory

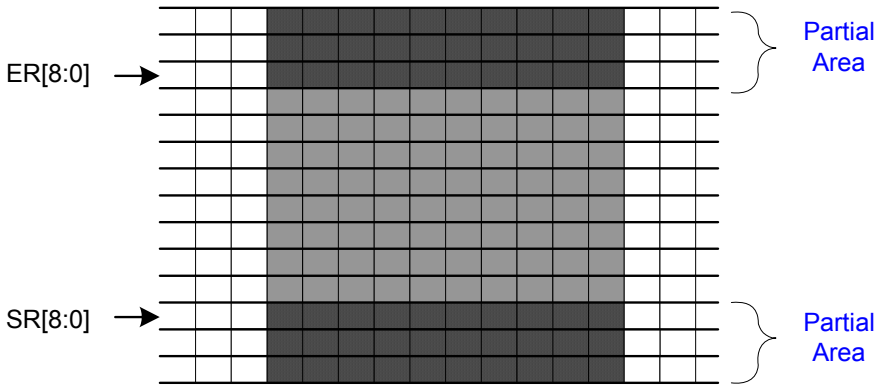
If End Row > Start Row and set_address_mode B4 = 0:



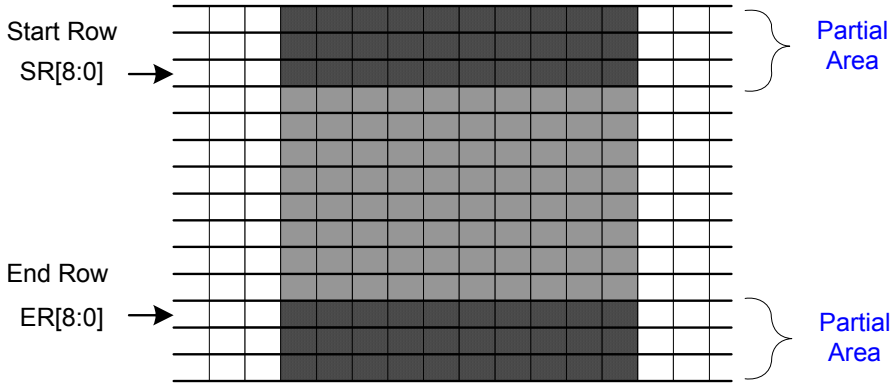
If End Row > Start Row and set_address_mode B4 = 1:



End Row < Start Row (set_address_mode(36h) B4=0)



End Row < Start Row (set_address_mode(36h) B4=1)



If End Row = Start Row then the Partial Area will be one row deep.

Restriction	SR[15:0] and ER[15:0] cannot be 0000h nor exceed the last vertical line number (01DFh).

Register Availability

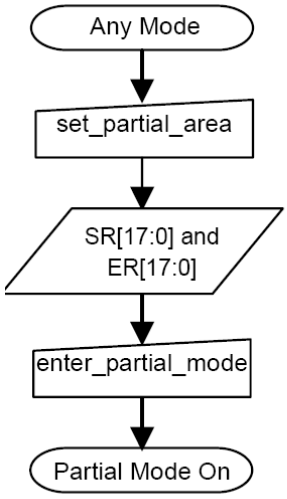
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

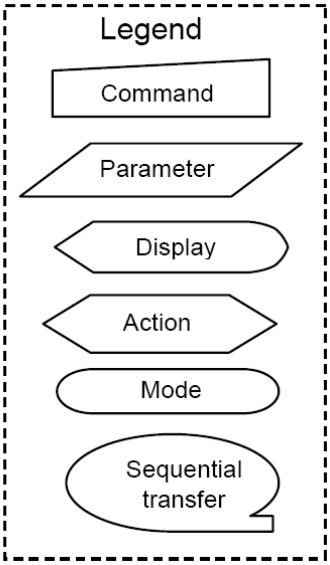
Default

Status	Default Value	
Power On Sequence	SR[8:0]=0000_{HEX}	ER[8:0]=$01DF_{HEX}$
SW Reset	SR[8:0]=0000_{HEX}	ER[8:0]=$01DF_{HEX}$
HW Reset	SR[8:0]=0000_{HEX}	ER[8:0]=$01DF_{HEX}$

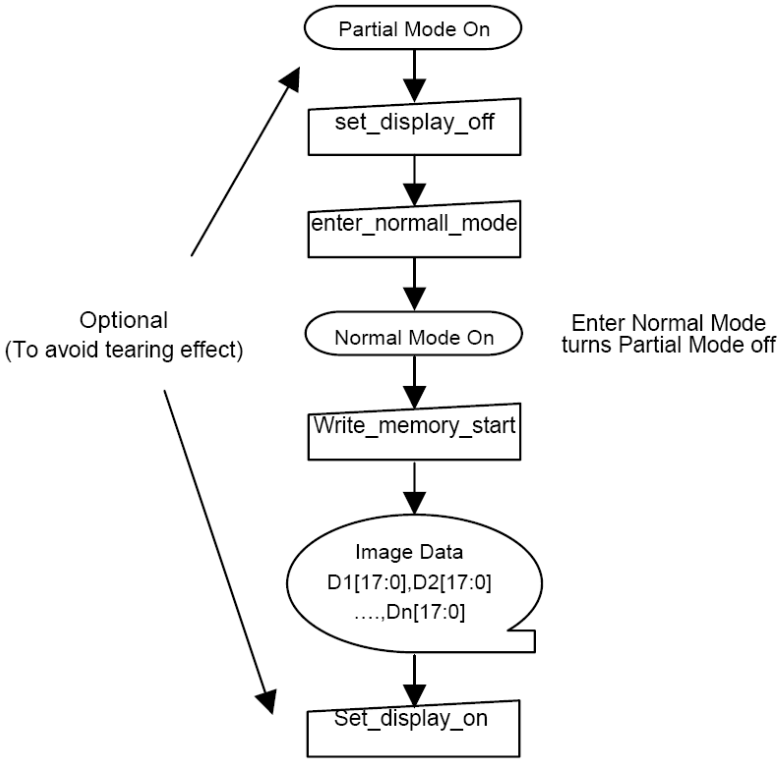
Flow Chart

1. To Enter Partial Mode





2. To Leave Partial Mode



8.2.22. Set_scroll_area (33h)

33H	Set_scroll_area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	0	1	1	33
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	TFA [8]	0000 … 01E0
2nd Parameter	1	1	↑	x	TFA [7]	TFA [6]	TFA [5]	TFA [4]	TFA 3]	TFA [2]	TFA [1]	TFA [0]	
3rd Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSA [8]	0000 … 01E0
4th Parameter	1	1	↑	x	VSA [7]	VSA [6]	VSA [5]	VSA [4]	VSA [3]	VSA [2]	VSA [1]	VSA [0]	
5th Parameter	1	1	↑	x	0	0	0	0	0	0	0	BFA [8]	0000 … 01E0
6th Parameter	1	1	↑	x	BFA [7]	BFA [6]	BFA 5]	BFA [4]	BFA [3]	BFA [2]	BFA [1]	BFA [0]	

Description

This command defines the display vertical scrolling area.

set_address_mode (36h) B4 = 0:

The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned. The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the bottom most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the top most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.

set_scroll_area set_address_mode B4 = 0 Example

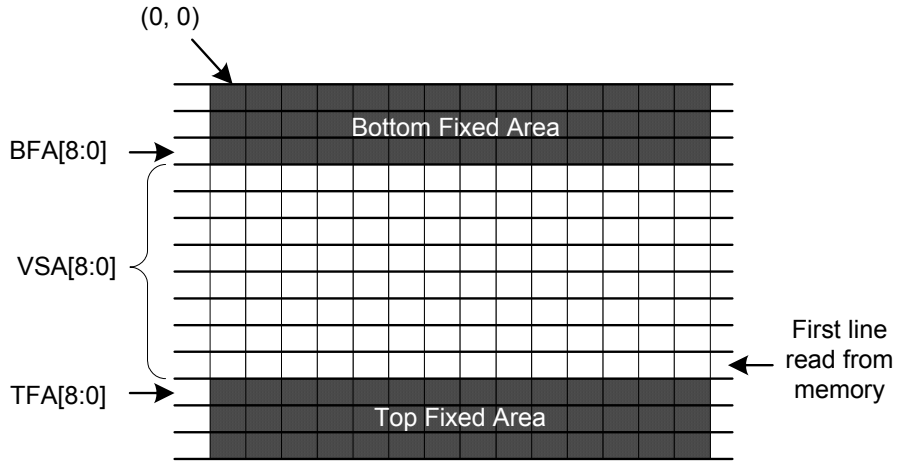
set_address_mode (36h) B4 = 1:

The 1st & 2nd parameter, TFA[8:0], describes the Top Fixed Area in number of lines from the bottom of the frame memory. The bottom of the frame memory and bottom of the display device are aligned.

The 3rd & 4th parameter, VSA[8:0], describes the height of the Vertical Scrolling Area in number of lines of frame memory from the Vertical Scrolling Start Address. The first line of the Vertical Scrolling Area starts immediately after the top most line of the Top Fixed Area. The last line of the Vertical Scrolling Area ends immediately before the bottom most line of the Bottom Fixed Area.

The 5th & 6th parameter, BFA[8:0], describes the Bottom Fixed Area in number of lines from the top of the frame memory. The top of the frame memory and top of the display device are aligned.

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



set_scroll_area set_address_mode B4 = 1 Example

Restriction

The sum of TFA, VSA and BFA must equal the number of the display device's horizontal lines (pages), otherwise Scrolling mode is undefined. In Vertical Scroll Mode, set_address_mode B5 should be set to '0' – this only affects the Frame Memory Write.

Register Availability

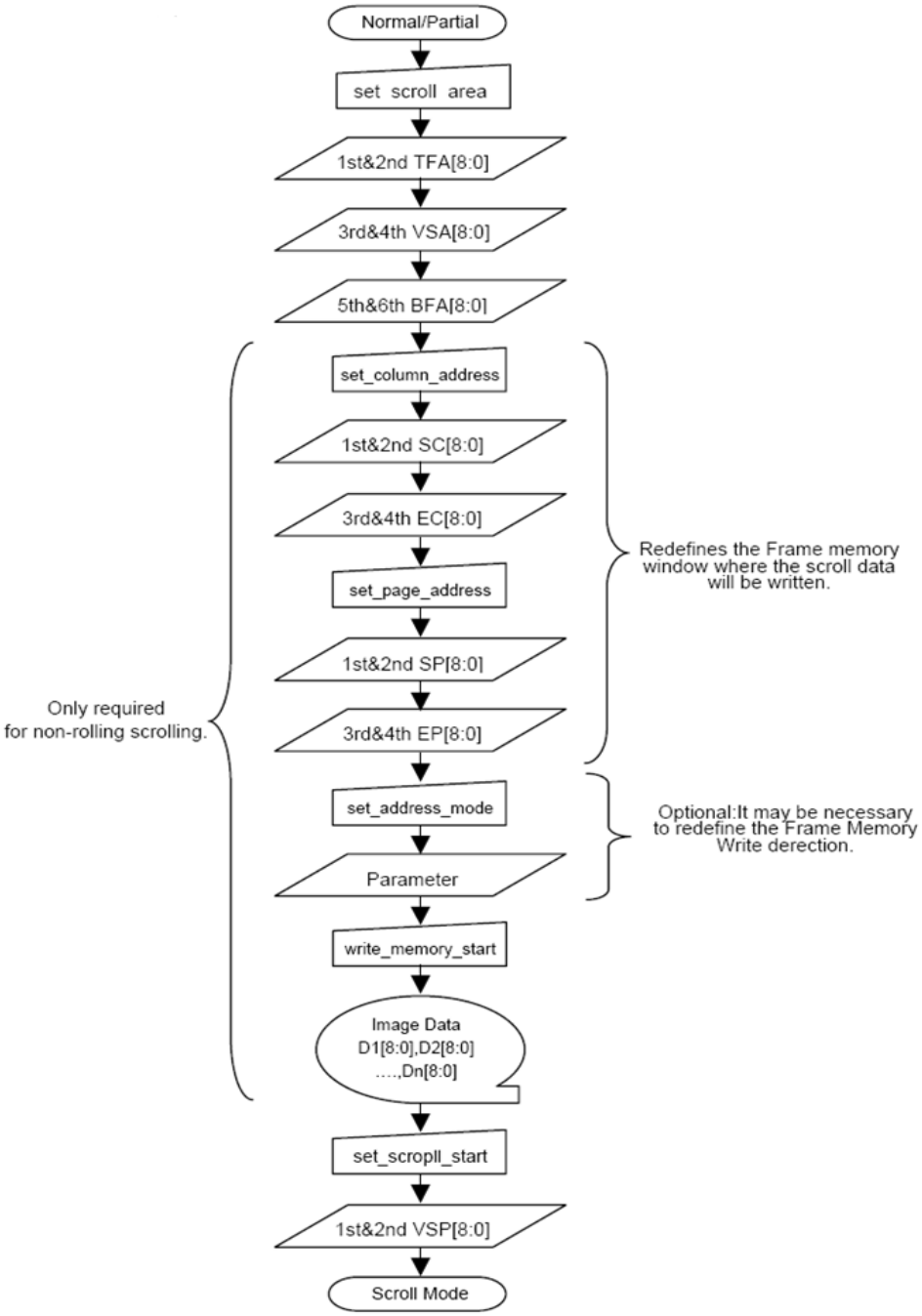
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
Power On Sequence	TFA[8:0]=0000_{HEX}	VSA[8:0]=$01E0_{HEX}$	BFA[8:0]=0000_{HEX}
SW Reset	TFA [8:0]=0000_{HEX}	VSA[8:0]=$01E0_{HEX}$	BFA[8:0]=0000_{HEX}
HW Reset	TFA [8:0]=0000_{HEX}	VSA[8:0]=$01E0_{HEX}$	BFA[8:0]=0000_{HEX}

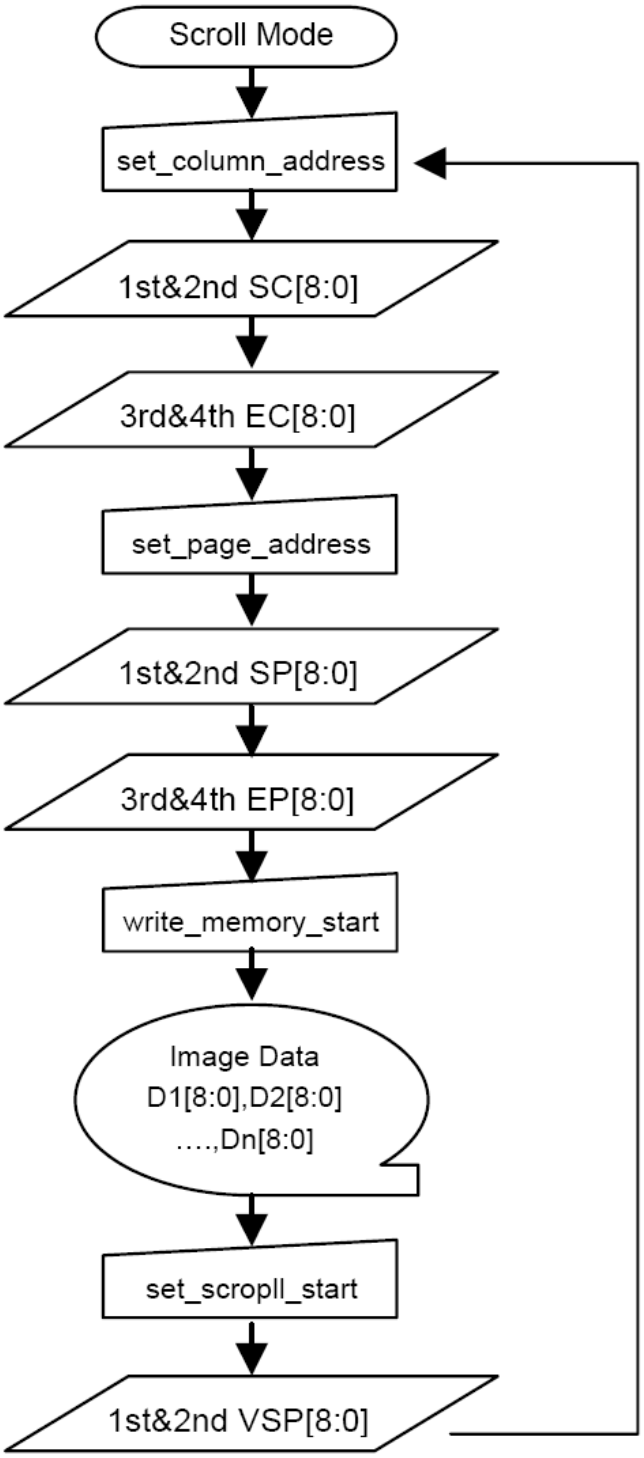
Flow Chart

1. To enter Vertical Scroll Mode:

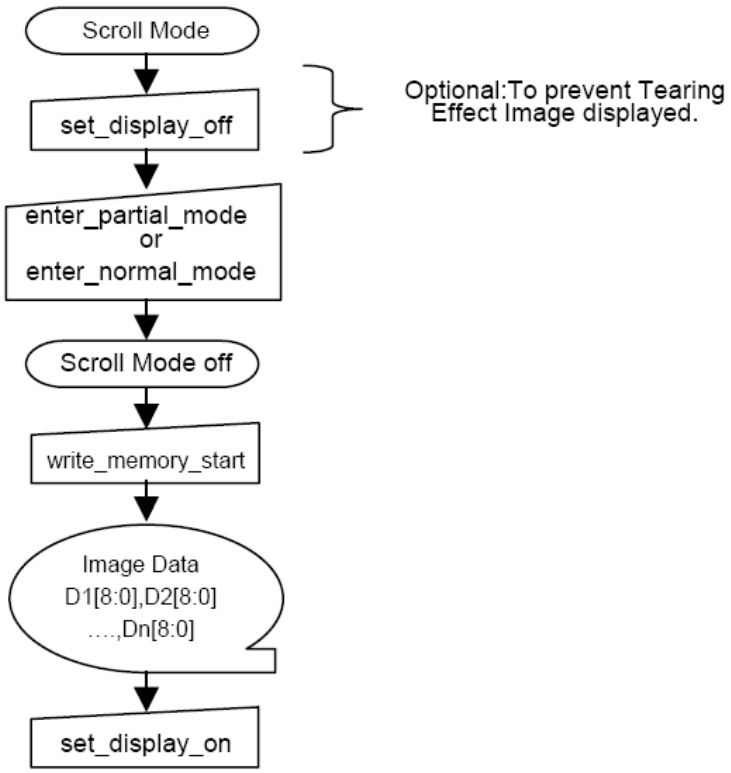


Since the value of the Vertical Scrolling Start Address is absolute with reference to the Frame Memory, it must not enter the fixed area; otherwise an undesirable image may be shown on the Display Panel.

2. Continuous Scroll:



3. To Leave Vertical Scroll Mode:



8.2.23. Set_tear_off (34h)

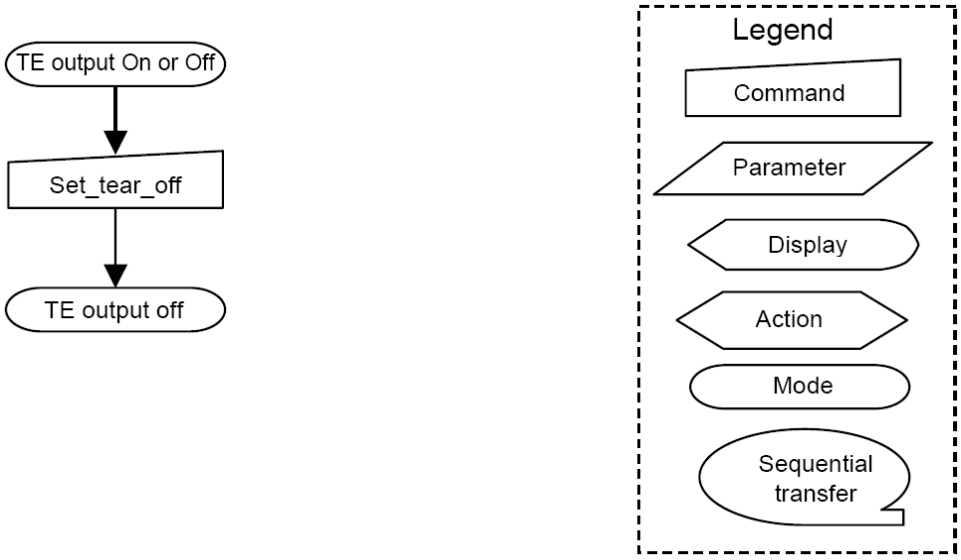
34H	Set_tear_off												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER												
Description	This command turns off the display module's Tearing Effect output signal on the TE signal line.												
Restriction	This command has no effect when the Tearing Effect output is already off.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



8.2.24. Set_tear_on (35h)

35H	Set_tear_on												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	0	1	35
1st Parameter	1	1	↑	x	x	x	x	x	x	x	x	TELOM	xx

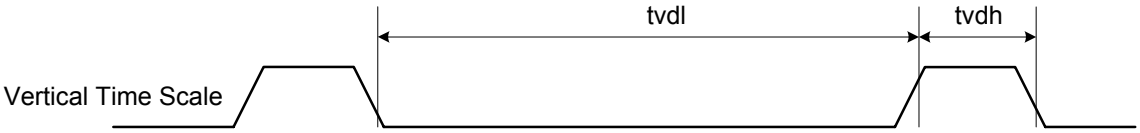
Description

This command turns on the tearing Effect output signal on the TE signal line. The TE signal is not affected by changing set_address_mode (36h) bit B4 (Line Address Order).

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.

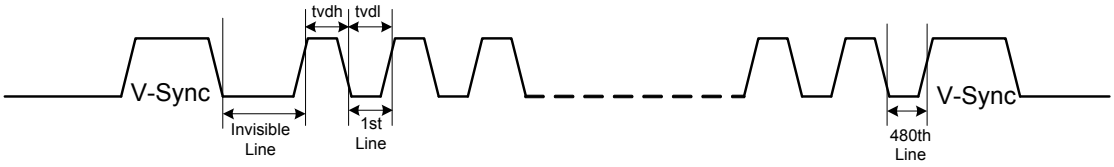
If TELOM = 0:

The Tearing Effect Output line consists of V-Blanking information only.



If TELOM = 1:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

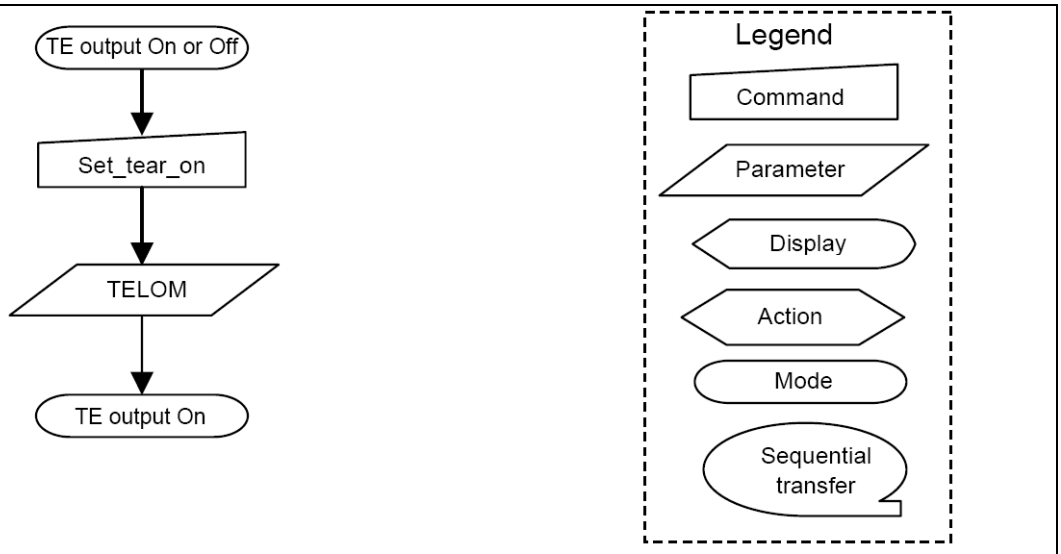
This command has no effect when Tearing Effect output is already ON.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

8.2.25. Set_address_mode (36h)

36H	Set_address_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	0	36
1st Parameter	1	1	↑	x	B7	B6	B5	B4	B3	0	B1	B0	xx

Description

This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

Bit	Description	Comment
B7	Page Address Order	
B6	Column Address Order	
B5	Page/Column Selection	
B4	Vertical Order	
B3	RGB/BGR Order	
B2	Display data latch data order	Set to '0'
B1	Horizontal Flip	
B0	Vertical Flip	

・Bit B7 – Page Address Order

'0' = Top to Bottom

'1' = Bottom to Top

・Bit B6 – Column Address Order

'0' = Left to Right

'1' = Right to Left

・Bit B5 – Page/Column Order

'0' = Normal Mode

'1' = Reverse Mode

・Bit B4 –Line Address Order

'0' = LCD Refresh Top to Bottom

'1' = LCD Refresh Bottom to Top

・Bit B3 – RGB/BGR Order

'0' = Pixels sent in RGB order

'1' = Pixels sent in BGR order

・Bit B2 –Display Data Latch Data Order

This bit is not applicable for this project, so it is set to '0'. (Not supported)

・Bit B1 – Horizontal Flip

'0' = Normal display

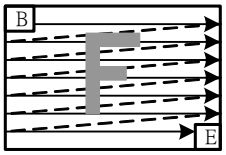
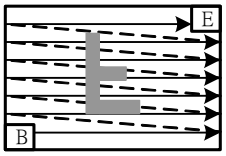
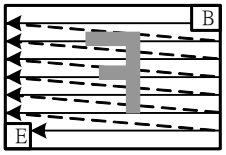
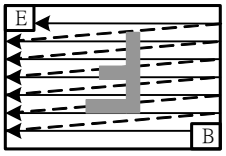
'1' = Flipped display

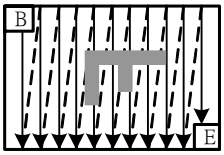
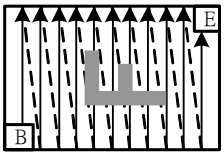
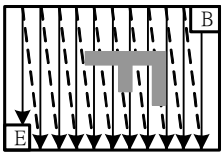
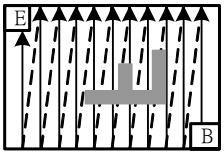
・Bit B0 – Vertical Flip

'0' = Normal display

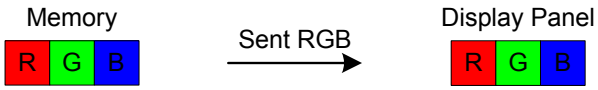
'1' = Flipped display

X = Don't care

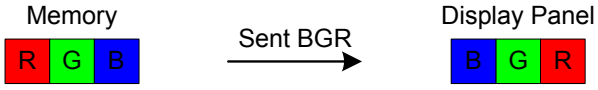
B5	B6	B7	Image in Frame Memory
0	0	0	
0	0	1	
0	1	0	
0	1	1	

B5	B6	B7	Image in Frame Memory
1	0	0	
1	0	1	
1	1	0	
1	1	1	

B3 = 0



B3 = 1



Restriction	

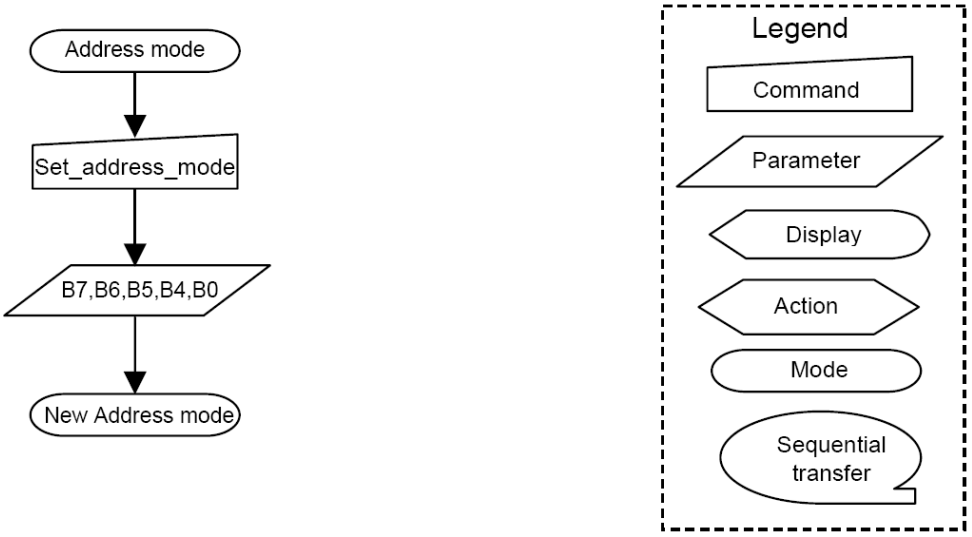
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000 0000_{HEX}
SW Reset	No Change
HW Reset	0000 0000_{HEX}

Flow Chart



8.2.26. Set_scroll_start (37h)

37H	Set_scroll_start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	0	1	1	1	37
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	VSP 8	xx
2nd Parameter	1	1	↑	x	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	xx

Description

This command sets the start of the vertical scrolling area in the frame memory. The vertical scrolling area is fully defined when this command is used with the set_scroll_area command

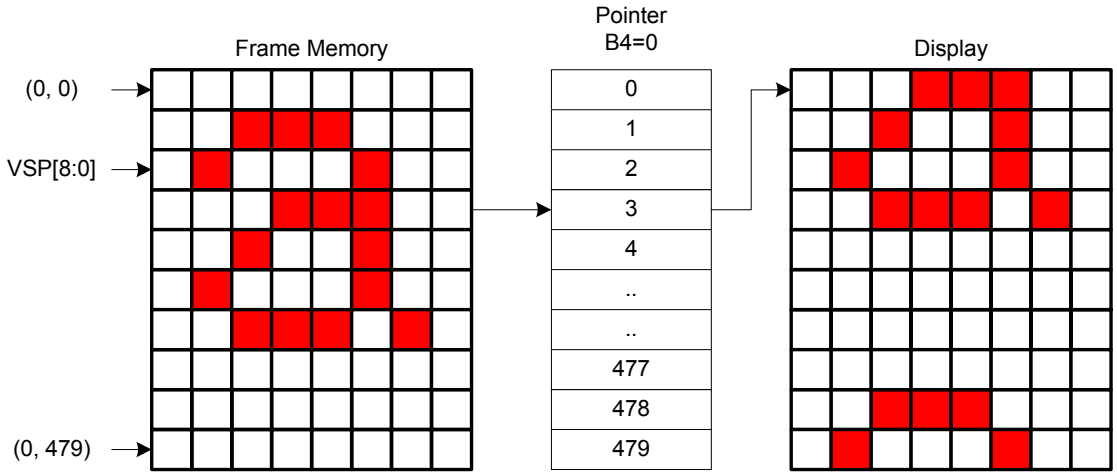
The set_scroll_start command has one parameter, the Vertical Scroll Pointer. The VSP defines the line in the frame memory that is written to the display device as the first line of the vertical scroll area.

The displayed image also depends on the setting of the Line Address Order bit, B4, in the set_address_mode register. See the examples below.

If set_address_mode (R36h) B4 = 0:

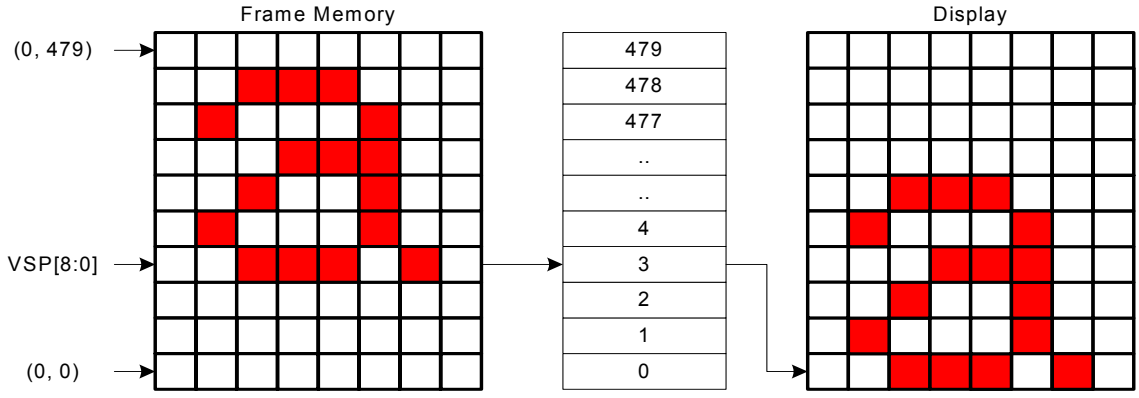
Example:

When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 480 and VSP = 3.



If set_address_mode (R36h) B4 = 1:

Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 480 and VSP='3'.



Note: When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is ***absolute*** (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be

<table>
<tr><td></td><td>displayed on the Panel.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0000_{HEX}</td></tr>
<tr><td>SW Reset</td><td>0000_{HEX}</td></tr>
<tr><td>HW Reset</td><td>0000_{HEX}</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>Refer to the description set_scroll_area (33h)</td></tr>
</table>

8.2.27. Exit_idle_mode (38h)

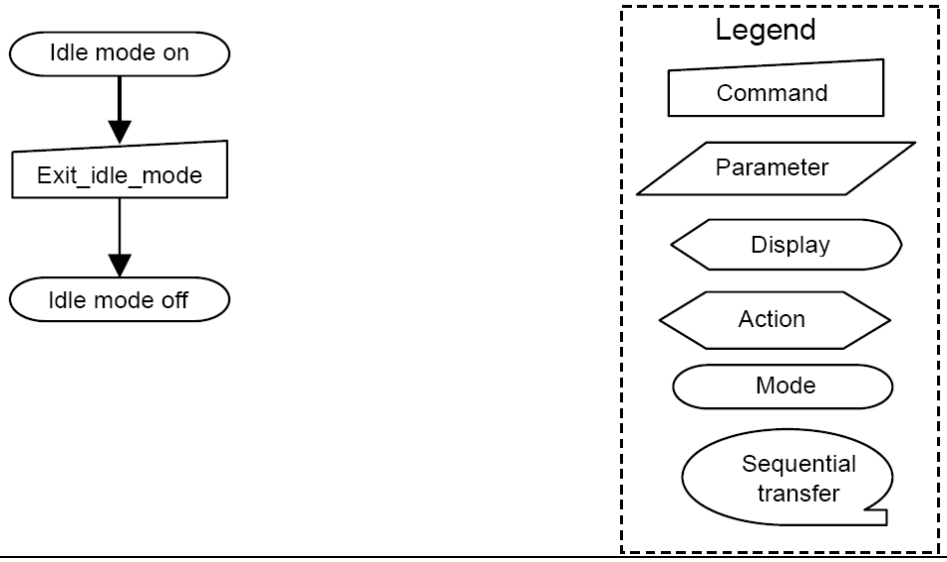
38H	Exit_idle_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command causes the display module to exit Idle mode.												
Restriction	This command has no effect when the display module is not in Idle mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



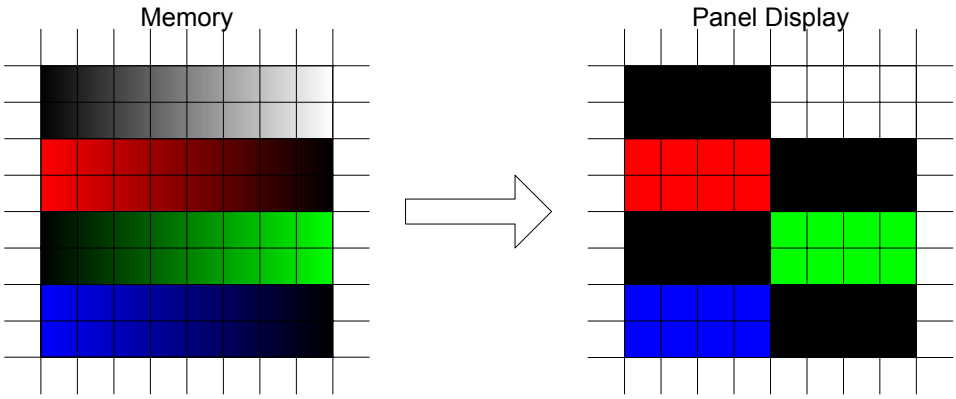
8.2.28. Enter_idle_mode (39h)

39H	Enter_idle_mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command causes the display module to enter Idle Mode.

In Idle Mode, color expression is reduced. Colors are shown on the display device using the MSB of each of the R, G and B color components in the frame memory.



	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

This command has no effect when module is already in idle on mode.

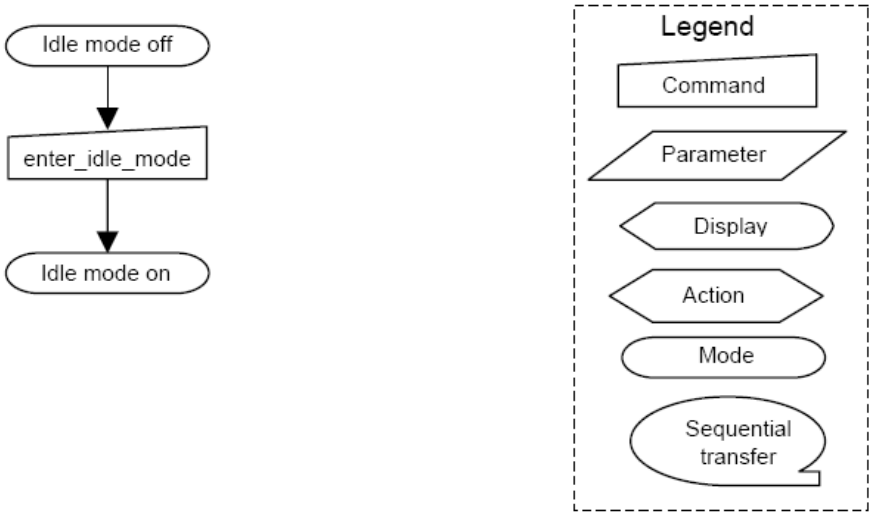
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
SW Reset	Idle Mode Off
HW Reset	Idle Mode Off

Flow Chart



8.2.29. Set_pixel_format (3Ah)

3AH	Set_pixel_format												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	0	1	0	3A
1st Parameter	1	1	↑	x	x	D6	D5	D4	x	D2	D1	D0	xx

Description

This command sets the pixel format for the RGB image data used by the interface.

Bits D[6:4] – DPI Pixel Format Definition

Bits D[2:0] – DBI Pixel Format Definition

Bits D7 and D3 are not used.

If a particular interface, either DBI or DPI, is not used then the corresponding bits in the parameter are ignored.

Control Interface Color Format	D6/D2	D5/D1	D4/D0
Not defined	0	0	0
3bit/pixel (8 color)	0	0	1
Not defined	0	1	0
Not defined	0	1	1
Not defined	1	0	0
16bit/pixel (65,536 colors)	1	0	1
18bit/pixel (262,144 colors)	1	1	0
Not defined	1	1	1

Restriction

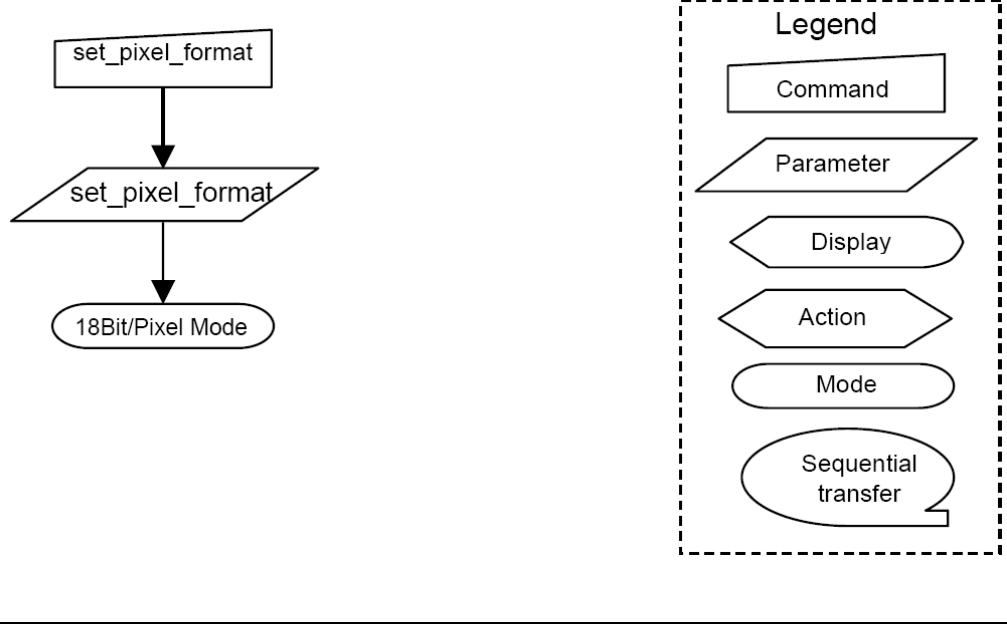
There is no visible effect until the Frame Memory is written to.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18bit/pixel
SW Reset	No change
HW Reset	18bit/pixel

Flow Chart	

8.2.30. Write_Memory_Continue (3Ch)

3CH	Write_Memory_Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	0	0	3C
1st Parameter	1	1	↑	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
xst Parameter	1	1	↑	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
Nst Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF

Description

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If set_address_mode B5 = 0:

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode B5 = 1:

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=1

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

Restriction

A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.

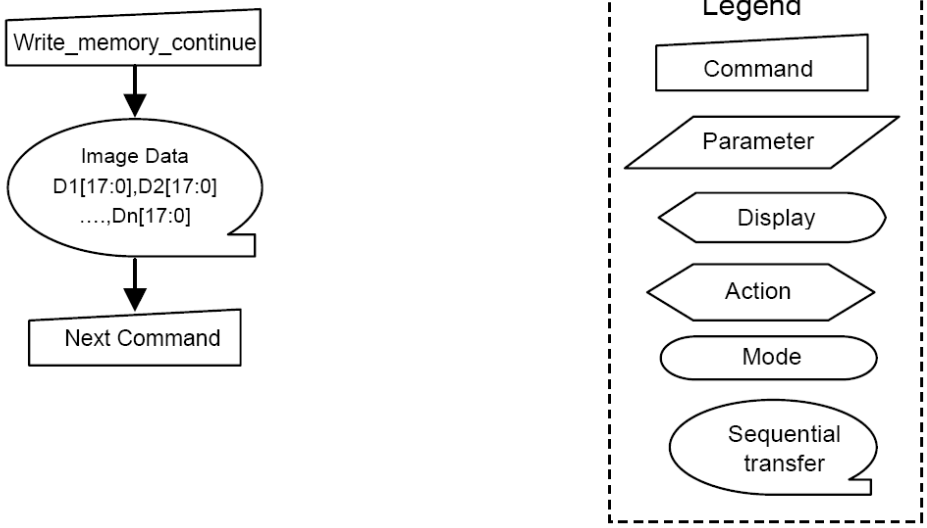
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All zero
SW Reset	No change
HW Reset	All zero

Flow Chart



8.2.31. Read_Memory_Continue (3Eh)

3EH	Read_Memory_Continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	0	1	1	1	1	1	0	3E
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
xst Parameter	1	↑	1	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
Nst Parameter	1	↑	1	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF

Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command.

If set_address_mode B5 = 0:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If set_address_mode B5 = 1:

Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

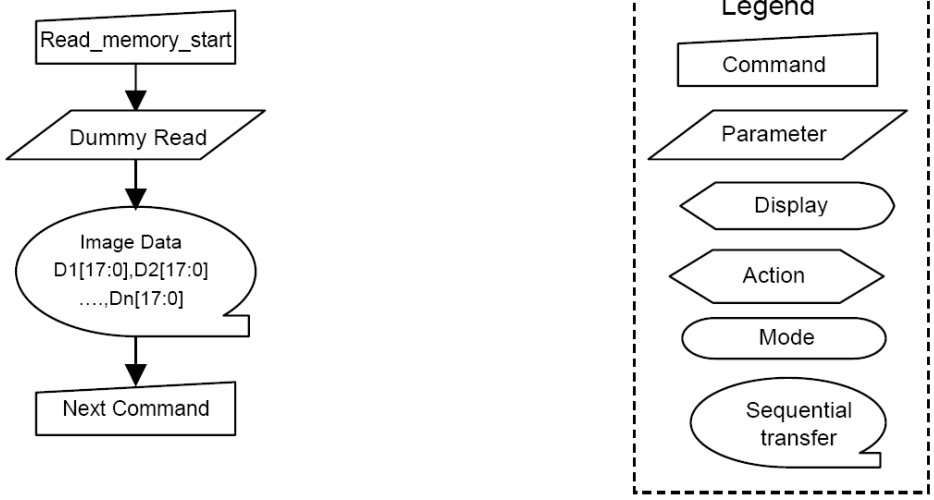
A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random data
SW Reset	No change
HW Reset	Random data

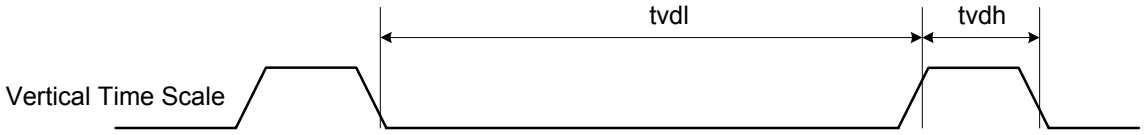
Flow Chart	

8.2.32. Set_Tear_Scanline (44h)

44H	Set_Tear_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	0	44
1st Parameter	1	1	↑	xx	0	0	0	0	0	0	0	STS [8]	0x
2nd Parameter	1	1	↑	xx	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	xx

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line N. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

-

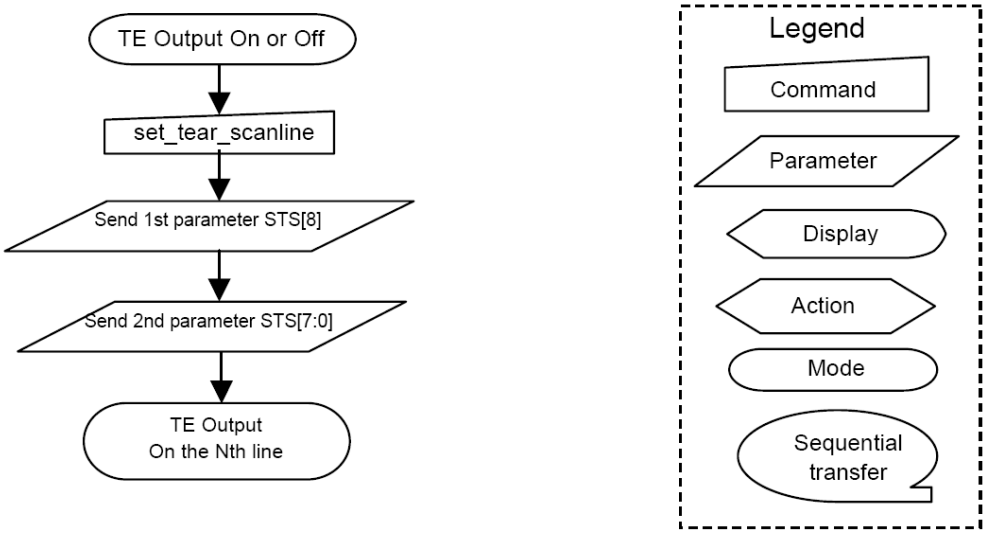
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS[8:0]=8'h0000
SW Reset	No change
HW Reset	STS[8:0]=8'h0000

Flow Chart

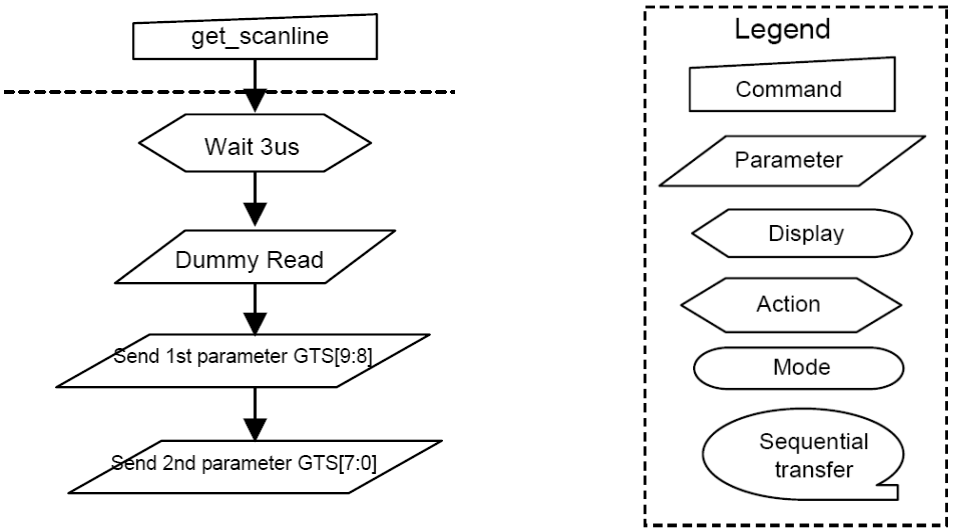


8.2.33. Get_Scanline (45h)

45H	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	0	1	0	0	0	1	0	1	45
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	xx	0	0	0	0	0	0	0	GTS [8]	0x
3rd Parameter	1	↑	1	xx	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	xx
Description	The display returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart



8.2.34. Read_DDB_Start (A1h)

A1H	Read_DDB_Start												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	0	1	0	0	0	0	1	A1
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	xx	ID2 [15]	ID2 [14]	ID2 [13]	ID2 [12]	ID2 [11]	ID2 [10]	ID2 [9]	ID2 [8]	xx
3rd Parameter	1	↑	1	xx	ID2 [7]	ID2 [6]	ID2 [5]	ID2 [4]	ID2 [3]	ID2 [2]	ID2 [1]	ID2 [0]	xx
4th Parameter	1	↑	1	xx	ID1 [15]	ID1 [14]	ID1 [13]	ID1 [12]	ID1 [11]	ID1 [10]	ID1 [9]	ID1 [8]	xx
5th Parameter	1	↑	1	xx	ID1 [7]	ID1 [6]	ID1 [5]	ID1 [4]	ID1 [3]	ID1 [2]	ID1 [1]	ID1 [0]	xx
6th Parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	FF

Description

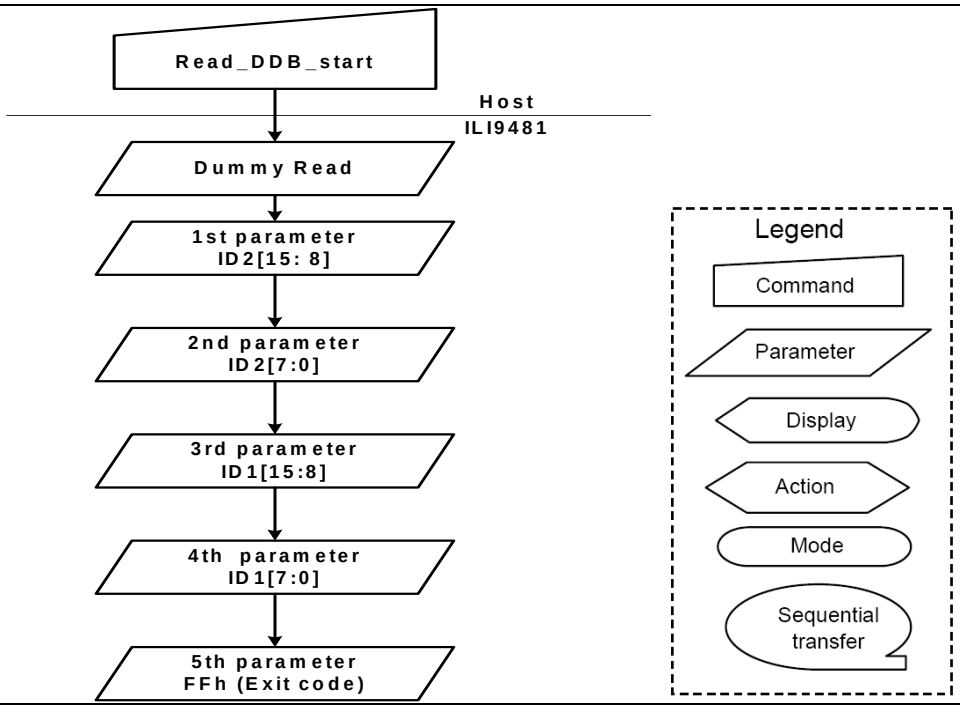
1st parameter: Dummy read
2nd parameter: Supplier Elective Data ID code ID2[15:8]
3rd parameter: Supplier Elective Data ID code ID2[7:0]
4th parameter: Supplier ID1[15:8]
5th parameter: Supplier ID1[7:0]
6th Exit code (FFh).

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Flow Chart



8.2.35. Command Access Protect (B0h)

B0H	Command Access Protect												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	0	0	0	B0
1st parameter	1	1	↑	xx	0	0	0	0	0	0	MCAP[1]	MCAP[0]	xx

Description

MCAP[1:0]	User Command	Protect command	Manufacturer Command		
	00h ~ AFh	B0h	B1h ~ DFh	E0h~EFh	F0h~FFh
2'h0	Yes	Yes	Yes	Yes	Yes
2'h1	Yes	Yes	Yes	Yes	No
2'h2	Yes	Yes	Yes	No	No
2'h3	Yes	Yes	No	No	No

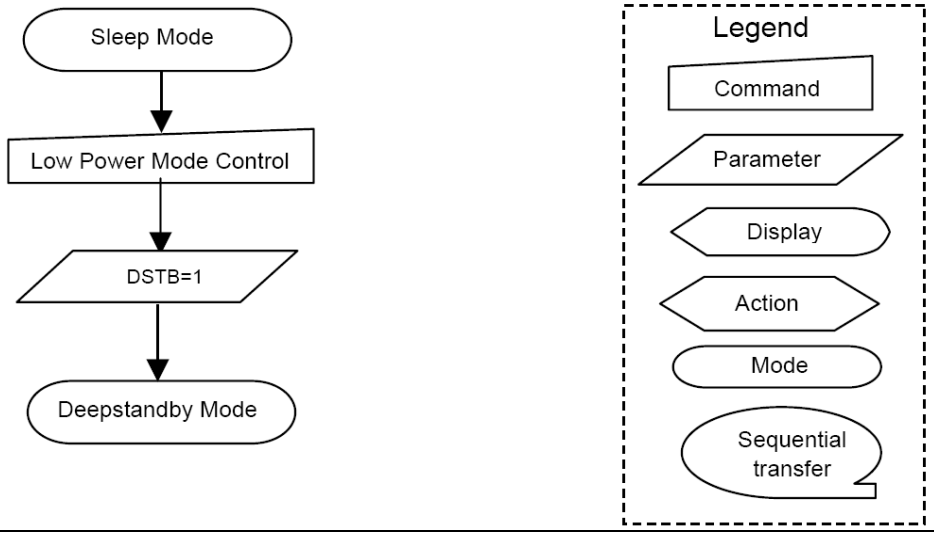
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	MCAP[1:0]=2'h0
SW Reset	No change
HW Reset	MCAP[1:0]=2'h0

Flow Chart



8.2.36. Frame Memory Access and Interface Setting (B3h)

B3H	Frame Memory Access and Interface Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	0	1	1	B3
1st parameter	1	1	↑	xx	0	0	0	0	0	0	WEMODE	0	xx
2nd parameter	1	1	↑	xx	0	0	0	0	0	TEI[2]	TEI[10]	TEI[0]	xx
3rd parameter	1	1	↑	xx	0	0	0	0	0	DENC[2]	DENC[1]	DENC[0]	xx
4th parameter	1	1	↑	xx	0	0	EPF[1]	EPF[0]	0	0	0	DFM	xx

Description

WEMODE: Memory write control

WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

TEI[2:0]: ILI9481 starts to output TE signal in the output interval set by TEI[2:0] bits.

TEI[2:0]	Output Interval
000	1 frame
001	2 frame
011	4 frame
101	6 frame
Others	Setting Prohibited

DENC[2:0]: Set the GRAM write cycle through the RGB interface

DENC[2:0]	GRAM Write Cycle (Frame periods)
000	1 Frame
001	2 Frames
010	3 Frames
011	4 Frames
100	5 Frames
101	6 Frames
110	7 Frames
111	8 Frames

DFM: The bit is used to define image data write/read format to the Frame Memory in DBI Type B (16bit bus interface) and DBI Type C serial interface operation.

EPF[1:0] Set the data format when 16bbp (R,G,B) to 18 bbp (r, g, b) is stored in the internal GRAM.

EPF[1:0]	Expand 16bbp (R,G,B) to 18 bbp (R, G, B)
00	"0" is inputted to LSB r[5:0] = {R[4:0], 0} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 0} Exception: R[4:0], B[4:0]=5'h1F → r[5:0], b[5:0] = 6'h3F
01	"1" is inputted to LSB r[5:0] = {R[4:0], 1} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], 1} Exception:

			R[4:0], B[4:0]=5'h00 → r[5:0], b[5:0] = 6'h00
		10	MSB is inputted to LSB r[5:0] = {R[4:0], R[4]} g[5:0] = {G[5:0]} b[5:0] = {B[4:0], B[4]}
		11	Setting disabled

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0
SW Reset	No change
HW Reset	WEMODE=1, TEI[2:0]=3'h0, DENC[2:0]=3'h0, DFM=1'h0, EPF[1:0]=2'h0

8.2.37. Display Mode and Frame Memory Write Mode Setting (B4h)

B4H	Display Mode and Frame Memory Write Mode Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	0	1	0	0	B4
1st parameter	1	1	↑	xx	0	0	0	RM	0	0	0	DM	xx

Description

DM Select the display operation mode.

DM0	Display Interface
0	Internal system clock
1	DPI (RGB) interface

The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

RM Select the interface to access the GRAM.

Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	DBI Interface (CPU)
1	DPI Interface (RGB)

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM[1:0]
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 0)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 1)
Rewrite still picture area while RGB interface Displaying moving pictures.		System interface (RM = 0)	RGB interface (DM = 1)

Note 1: Registers are set only via the system interface or SPI interface.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DM=0, RM=0
SW Reset	No change
HW Reset	DM=0, RM=0

8.2.38. Device Code Read (BFh)

BFH	Device Code Read												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	xx	1	0	1	1	1	1	1	1	BF
1st parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd parameter	1	↑	1	xx	0	0	0	0	0	0	1	0	02
3rd parameter	1	↑	1	xx	0	0	0	0	0	1	0	0	04
4th parameter	1	↑	1	xx	1	0	0	1	0	1	0	0	94
5th parameter	1	↑	1	xx	1	0	0	0	0	0	0	1	81
6th parameter	1	↑	1	xx	1	1	1	1	1	1	1	1	FF
Description	1st parameter : dummy read 2nd parameter : MIPI Alliance code 3rd parameter : MIPI Alliance code 4th parameter : Device ID code of ILI9481 5th parameter : Device ID code of ILI9481 6th parameter : Exit code (FFh)												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

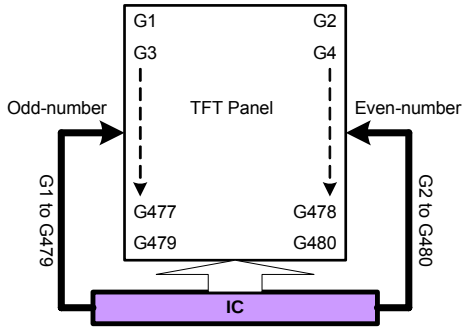
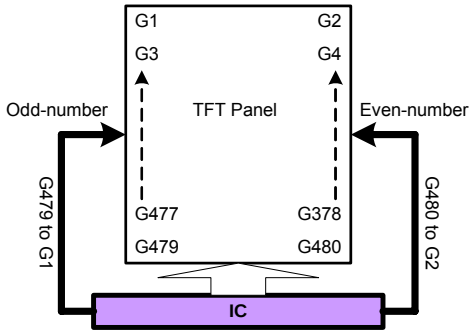
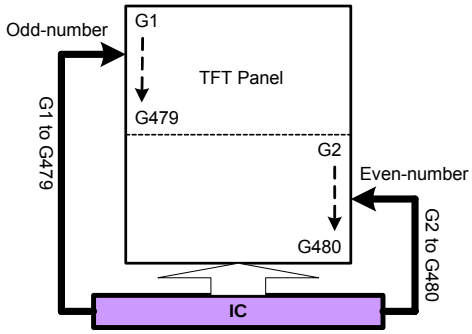
Status	Default Value
Power On Sequence	02,04,94,81,FF
SW Reset	No change
HW Reset	02,04,94,81,FF

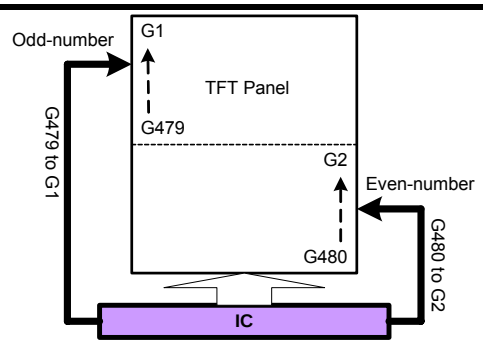
8.2.39. Panel Driving Setting (C0h)

C0H	Panel Driving Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	0	C0
1st Parameter	1	1	↑	0	0	0	0	REV	SM	GS	0	0	x
2nd Parameter	1	1	↑	0	0	0	NL [5]	NL [4]	NL [3]	NL [2]	NL [1]	NL [0]	xx
3rd Parameter	1	1	↑	0	0	SCN [6]	SCN [5]	SCN [4]	SCN [3]	SCN [2]	SCN [1]	SCN [0]	xxx
4th Parameter	1	1	↑	0	0	0	0	NDL	0	PTS [2]	PTS [1]	PTS [0]	xxx
5th Parameter	1	1	↑	0	0	0	0	PTG	ISC [3]	ISC [2]	ISC [1]	ISC [0]	xxx

Description

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4, …,G476 G477, G478, G479, G480
0	1		G480, G479, G478, …, G9 G7, G5, G4, G3, G2, G1
1	0		G1, G3, G5, G7, …,G471 G473, G475, G477, G479 G2, G4, G6, G8, …,G472 G474, G476, G478, G480

1	1		G480, G478, G476, …,G14 G12, G10, G8, G6, G4, G2 G479, G477, G475,…,G13 G11, G9, G7, G5, G3, G1

REV: Enables the grayscale inversion of the image by setting REV=1.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	:	:	:
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	:	:	:
	18'h3FFFF	V63	V0

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	LCD Drive Line
6'h00 ~ 6'h3B	8 * (NL5:0]+1) lines
Others	Setting inhibited

SCN[6:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h ~ 3Bh	G[1+SCN[6:0]*4]	G[480 - SCN[6:0]*4]	G[1+SCN[6:0]*8]	G[480 - SCN[6:0]*8]
3Ch ~ 77h	G[1+SCN[6:0]*4]	G[480 - SCN[6:0]*4]	G[2+(SCN[6:0]-3Ch)*8]	G[479 – (SCN[6:0]-3Ch)*8]
Others	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NDL: Sets the source output level in non-display area. Settings are different to normally black panels and normally white panels.

NDL	Non-display Area	
	Positive	Negative
0	V63	V0
1	V0	V63

PTG: Sets the scan mode in non-display area. Select frame-inversion AC drive when interval-scan is selected.

PTG	Scan Mode in non-display area
0	Normal Scan
1	Interval Scan

ISC[3:0]: Set the scan cycle when PTG selects interval scan in non-display area drive period. The scan cycle is defined by n frame periods, where n is an odd number from 3 to 31. The polarity of liquid crystal drive voltage from the gate driver is

inverted in the same timing as the interval scan cycle.

ISC[3:0]	Scan cycle	(f_{FRAME})=60Hz
4'h0	Setting inhibited	—
4'h1	3 frames	50ms
4'h2	5 frames	84ms
4'h3	7 frames	117ms
4'h4	9 frames	150ms
4'h5	11 frames	184ms
4'h6	13 frames	217ms
4'h7	15 frames	251ms
4'h8	17 frames	284ms
4'h9	19 frames	317ms
4'hA	21 frames	351ms
4'hB	23 frames	384ms
4'hC	25 frames	418ms
4'hD	27 frames	451ms
4'hE	29 frames	484ms
4'hF	31 frames	518ms

PTS[2:0]:

Set the source output level in non-display area drive period (front/back porch period and blank area between partial displays).

When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in non-display drive period in order to reduce power consumption.

PTS[2:0]	Source output level		Grayscale amplifier in operation	Step-up clock frequency
	Positive polarity	Negative polarity		
000	V63	V0	V63 and V0	Register Setting(DC1, DC0)
001	V0	V63	-	-
010	GND	GND	V63 and V0	Register Setting(DC1, DC0)
011	Hi-Z	Hi-Z	V63 and V0	Register Setting(DC1, DC0)
100	Setting Prohibited	Setting Prohibited		
101	Setting Prohibited	Setting Prohibited		
110	Setting Prohibited	Setting Prohibited		
111	Setting Prohibited	Setting Prohibited		

Restriction: -

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	SM=0, GS=0, REV=1, NL[6:0]=7'h3B, SCN[6:0]=0, NDL=0, PTG=1, ISC[3:0]=4'h1, PTS[2:0]=3'h2
SW Reset	No change
HW Reset	SM=0, GS=0, REV=1, NL[6:0]=7'h3B, SCN[6:0]=0, PTG=1, NDL=0,ISC[3:0]=4'h1, PTS[2:0]=3'h2

8.2.40. Display_Timing_Setting for Normal Mode (C1h)

C1H	Display_Timing_Setting for Normal Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	0	1	C1
1st Parameter	1	1	↑	0	0	0	0	BC0	0	0	DIV0[1]	DIV0[0]	x
2nd Parameter	1	1	↑	0	0	0	0	RTN0[4]	RTN0[3]	RTN0[2]	RTN0[1]	RTN0[0]	xx
3rd Parameter	1	1	↑	0	FP0[3]	FP0[2]	FP0[1]	FP0[0]	BP0[3]	BP0[2]	BP0[1]	BP0[0]	xxx

Description

BC0: BC0 is used to select VCOM liquid crystal drive waveform.

BC0 = 0: Frame inversion waveform is selected.

BC0 = 1: Line inversion waveform is selected.

DIV0[1:0]: DIV0[1:0] is used to set division ratio of internal clock frequency.

The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed.

The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.

DIV0[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]

fosc. : internal oscillator frequency

clocks per line : RTNn setting

division ratio: DIVn setting

Line: total driving line number

BP: back porch line number

FP: front porch line number

RTN0[4:0]: RTN0[4:0] is used to set 1H (line) period.

RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line	RTN[4:0]	Clocks per line
5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

FP0[3:0], BP0[3:0]

FP0[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP0[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of

display).

FP[3:0] BP[3:0]	Front and back porch period (line period)	FP[3:0] BP[3:0]	Front and back porch period (line period)
4'h0	Setting prohibited	4'h8	8 lines
4'h1	Setting prohibited	4'h9	9 lines
4'h2	2 lines	4'hA	10 lines
4'h3	3 lines	4'hB	11 lines
4'h4	4 lines	4'hC	12 lines
4'h5	5 lines	4'hD	13 lines
4'h6	6 lines	4'hE	14 lines
4'h7	7 lines	4'hF	15 lines

Note to Setting BP and FP

The condition in setting BP and FP bits are: BP≧2 lines FP≧2 lines FP+BP ≤ 16 lines

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP=4'h8
SW Reset	No change
HW Reset	BC0=1'h1, DIV0=2'h0, RTN0=5'h10, FP0=4'h8, BP0=4'h8

8.2.41. Display_Timing_Setting for Partial Mode (C2h)

C2H	Display_Timing_Setting for Partial Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	0	C2
1st Parameter	1	1	↑	0	0	0	0	BC1	0	0	DIV1[1]	DIV1[0]	x
2nd Parameter	1	1	↑	0	0	0	0	RTN1[4]	RTN1[3]	RTN1[2]	RTN1[1]	RTN1[0]	xx
3rd Parameter	1	1	↑	0	FP1[3]	FP1[2]	FP1[1]	FP1[0]	BP1[3]	BP1[2]	BP1[1]	BP1[0]	xxx

Description

BC1: BC1 is used to select VCOM liquid crystal drive waveform.

BC1 = 0: Frame inversion waveform is selected.

BC1 = 1: Line inversion waveform is selected.

DIV1[1:0]: DIV1[1:0] is used to set division ratio of internal clock frequency.

The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed.

The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.

DIV1[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]

fosc. : internal oscillator frequency

clocks per line : RTNn setting

division ratio: DIVn setting

Line: total driving line number

BP: back porch line number

FP: front porch line number

RTN1[4:0]: RTN0[4:0] is used to set 1H (line) period.

RTN1[4:0]	Clocks per line	RTN1[4:0]	Clocks per line	RTN1[4:0]	Clocks per line
5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

FP1[3:0], BP1[3:0]

FP1[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP1[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of

display).

FP1[3:0] BP1[3:0]	Front and back porch period (line period)	FP1[3:0] BP1[3:0]	Front and back porch period (line period)
4'h0	Setting prohibited	4'h8	8 lines
4'h1	Setting prohibited	4'h9	9 lines
4'h2	2 lines	4'hA	10 lines
4'h3	3 lines	4'hB	11 lines
4'h4	4 lines	4'hC	12 lines
4'h5	5 lines	4'hD	13 lines
4'h6	6 lines	4'hE	14 lines
4'h7	7 lines	4'hF	15 lines

Note to Setting BP and FP

The condition in setting BP and FP bits are: BP≧2 lines FP≧2 lines FP+BP ≤ 16 lines

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BC1=1'h1, DIV1=2'h0, RTN1=5'h10, FP1=4'h8, BP1=4'h8
SW Reset	No change
HW Reset	BC1=1'h1, DIV1=2'h0, RTN1=5'h10, FP1=4'h8, BP1=4'h8

8.2.42. Display_Timing_Setting for Idle Mode (C3h)

C3H	Display_Timing_Setting for Idle Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	0	1	1	C3
1st Parameter	1	1	↑	0	0	0	0	BC2	0	0	DIV2[1]	DIV2[0]	x
2nd Parameter	1	1	↑	0	0	0	0	RTN2[4]	RTN2[3]	RTN2[2]	RTN2[1]	RTN2[0]	xx
3rd Parameter	1	1	↑	0	FP2[3]	FP2[2]	FP2[1]	FP2[0]	BP2[3]	BP2[2]	BP2[1]	BP2[0]	xxx

Description

BC2: BC1 is used to select VCOM liquid crystal drive waveform.

BC1 = 0: Frame inversion waveform is selected.

BC1 = 1: Line inversion waveform is selected.

DIV2[1:0]: DIV1[1:0] is used to set division ratio of internal clock frequency.

The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width of the reference clock for liquid crystal control signals is changed.

The frame frequency can be adjusted by register setting (RTN and DIV bits). When number of lines to drive is changed, adjust the frame frequency too.

DIV2[1:0]	Division Ratio
2'h0	1/1
2'h1	1/2
2'h2	1/4
2'h3	1/8

Frame Frequency = fosc. / [Clocks per line x division ratio x (Line +BP+FP)]

fosc. : internal oscillator frequency

clocks per line : RTNn setting

division ratio: DIVn setting

Line: total driving line number

BP: back porch line number

FP: front porch line number

RTN2[4:0]: RTN0[4:0] is used to set 1H (line) period.

RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line	RTN2[4:0]	Clocks per line
5'h00~0F	Setting prohibited	5'h15	21 clocks	5'h1B	27 clocks
5'h10	16 clocks	5'h16	22 clocks	5'h1C	28 clocks
5'h11	17 clocks	5'h17	23 clocks	5'h1D	29 clocks
5'h12	18 clocks	5'h18	24 clocks	5'h1E	30 clocks
5'h13	19 clocks	5'h19	25 clocks	5'h1F	31 clocks
5'h14	20 clocks	5'h1A	26 clocks		

FP2[3:0], BP2[3:0]

FP2[3:0] is used to set the number of lines for a front porch period (a blank period following the end of display).

BP2[3:0] is used to set the number of lines for a back porch period (a blank period made before the beginning of

display).

FP2[3:0] BP2[3:0]	Front and back porch period (line period)	FP2[3:0] BP2[3:0]	Front and back porch period (line period)
4'h0	Setting prohibited	4'h8	8 lines
4'h1	Setting prohibited	4'h9	9 lines
4'h2	2 lines	4'hA	10 lines
4'h3	3 lines	4'hB	11 lines
4'h4	4 lines	4'hC	12 lines
4'h5	5 lines	4'hD	13 lines
4'h6	6 lines	4'hE	14 lines
4'h7	7 lines	4'hF	15 lines

Note to Setting BP and FP

The condition in setting BP and FP bits are: BP≧2 lines FP≧2 lines FP+BP ≤ 16 lines

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h8, BP2=4'h8
SW Reset	No change
HW Reset	BC2=1'h1, DIV2=2'h0, RTN2=5'h10, FP2=4'h8, BP2=4'h8

8.2.43. Frame Rate and Inversion Control (C5h)

C5H	Frame Rate Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	0	0	1	0	1	C5
1st Parameter	1	1	↑	0	0	0	0	0	0	FRA[2]	FRA[1]	FRA[0]	-

Description

Set the frame frequency of the full colors normal mode.

The frame frequency needs to meet 80Hz±5% in this mode.

FRA[2:0]	Frame Rate (Hz)
000	125
001	100
010	85
011	**72 (default)**
100	56
101	50
110	45
111	42

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	FRA[3:0]
Power On Sequence	4'b0011
SW Reset	4'b0011
HW Reset	4'b0011

8.2.44. Interface Control (C6h)

C6H	Interface Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	0	1	1	0	C6
1st Parameter	1	1	↑	x	SDA_EN	0	0	VSPL	HSPL	0	EPL	DPL	xx

Description

DPL: Sets the signal polarity of the PCLK pin.

DPL = "0" The data is input on the rising edge of PCLK.

DPL = "1" The data is input on the falling edge of PCLK.

EPL: Sets the signal polarity of the ENABLE pin.

EPL = "0" The data DB[17:0] is written when ENABLE = "0".

EPL = "1" The data DB[17:0] is written when ENABLE = "1".

HSPL: Sets the signal polarity of the HSYNC pin.

HSPL = "0" Low active

HSPL = "1" High active

VSPL: Sets the signal polarity of the VSYNC pin.

VSPL = "0" Low active

VSPL = "1" High active

SDA_EN: DBI type C interface selection

SDA_EN = "0", DIN and DOUT pins are used for DBI type C interface mode.

SDA_EN = "1", DIN/SDA pin is used for DBI type C interface mode and DOUT pin is not used.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0
SW Reset	No change
HW Reset	DPL=1'h0, EPL=1'h1, VSPL=1'h0, HSPL=:1'h0,SDA_EN=1'h0

8.2.45. Gamma Setting (C8h)

C8H	Gamma Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	0	1	0	0	0	C8
1st Parameter	1	1	↑	x	0	KP1[2]	KP1[1]	KP1[0]	0	KP0[2]	KP0[1]	KP0[0]	xx
2nd Parameter	1	1	↑	x	0	KP3[2]	KP3[1]	KP3[0]	0	KP2[2]	KP2[1]	KP2[0]	xx
3rd Parameter	1	1	↑	x	0	KP5[2]	KP5[1]	KP5[0]	0	KP4[2]	KP4[1]	KP4[0]	xx
4th Parameter	1	1	↑	x	0	RP1[2]	RP1[1]	RP1[0]	0	RP0[2]	RP0[1]	RP0[0]	xx
5th Parameter	1	1	↑	x	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]	xx
6th Parameter	1	1	↑	x	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	xx
7th Parameter	1	1	↑	x	0	KN1[2]	KN1[1]	KN1[0]	0	KN0[2]	KN0[1]	KN0[0]	xx
8th Parameter	1	1	↑	x	0	KN3[2]	KN3[1]	KN3[0]	0	KN2[2]	KN2[1]	KN2[0]	xx
9th Parameter	1	1	↑	x	0	KN5[2]	KN5[1]	KN5[0]	0	KN4[2]	KN4[1]	KN4[0]	xx
10th Parameter	1	1	↑	x	0	RN1[2]	RN1[1]	RN1[0]	0	RN0[2]	RN0[1]	RN0[0]	xx
11th Parameter	1	1	↑	x	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]	xx
12th Parameter	1	1	↑	x	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	xx

Description

KP5-0[2:0] : γ fine adjustment register for positive polarity

RP1-0[2:0] : γ gradient adjustment register for positive polarity

VRP1-0[4:0] : γ amplitude adjustment register for positive polarity

KN5-0[2:0] : γ fine adjustment register for negative polarity

RN1-0[2:0] : γ gradient adjustment register for negative polarity

VRN1-0[4:0] : γ amplitude adjustment register for negative polarity

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All the parameters are 00h
SW Reset	No change
HW Reset	All the parameters are 00h

8.2.46. Power_Setting (D0h)

D0H	Power_Setting												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	0	D0
1st Parameter	1	1	↑	x	0	0	0	0	0	VC[2]	VC[1]	VC[0]	xx
2nd Parameter	1	1	↑	x	0	PON	0	0	0	BT[2]	BT[1]	BT[0]	xx
3rd Parameter	1	1	↑	x	0	0	0	VCIRE	VRH[3]	VRH[2]	VRH[1]	VRH[0]	xx

Description

VC[2:0] Sets the ratio factor of Vci to generate the reference voltages Vci1.

VC[2:0]	Vci1 voltage
3'h0	0.95 x Vci
3'h1	090 x Vci
3'h2	0.85 x Vci
3'h3	0.80 x Vci
3'h4	0.75 x Vci
3'h5	0.70 x Vci
3'h6	Disable
3'h7	1.0 x Vci

BT[2:0] Sets the Step up factor and output voltage level from the reference voltages Vci1.

BT[2:0]	DDVDH	VCL	VGH	VGL
3'h0	Vci1 x 2	- Vci1	Vci1 x 6	- Vci1 x 5
3'h1	Vci1 x 2	- Vci1		- Vci1 x 4
3'h2				- Vci1 x 3
3'h3	Vci1 x 2	- Vci1	Vci1 x 5	- Vci1 x 5
3'h4				- Vci1 x 4
3'h5				- Vci1 x 3
3'h6	Vci1 x 2	- Vci1	Vci1 x 4	- Vci1 x4
3'h7				- Vci1 x3

Note 1: Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.
Note 2: Set following voltages within the respective ranges:
DDVDH = 6.0V (max)
VGH = 18.0V (max)
VGL= -12.5V (max)
VCL= -3.0V (max).

PON is used to control the operation to generate VGL.

PON=0: Halts the step-up operation to generate VGL.

PON=1: Starts the step-up operation to generate VGL.

VRH[3:0]: Sets the factor to generate VREG1OUT from VCI

VCIRE: Select the external reference voltage Vci or internal reference voltage VCIR.

VCIRE=0	External reference voltage Vci (**default**)
VCIRE =1	Internal reference voltage 2.5V

VCIRE =0					VCIR1 =1				
VRH3	VRH2	VRH1	VRH0	VREG1OUT	VRH3	VRH2	VRH1	VRH0	VREG1OUT
0	0	0	0	Halt	0	0	0	0	Halt
0	0	0	1	Vci x 2.00	0	0	0	1	2.5V x 2.00 = 5.000V
0	0	1	0	Vci x 2.05	0	0	1	0	2.5V x 2.05 = 5.125V
0	0	1	1	Vci x 2.10	0	0	1	1	2.5V x 2.10 = 5.250V
0	1	0	0	Vci x 2.20	0	1	0	0	2.5V x 2.20 = 5.500V
0	1	0	1	Vci x 2.30	0	1	0	1	2.5V x 2.30 = 5.750V
0	1	1	0	Vci x 2.45	0	1	1	0	2.5V x 2.40 = 6.000V
0	1	1	1	Vci x 2.40	0	1	1	1	2.5V x 2.40 = 6.000V
1	0	0	0	Vci x 1.60	1	0	0	0	2.5V x 1.60 = 4.000V
1	0	0	1	Vci x 1.65	1	0	0	1	2.5V x 1.65 = 4.125V
1	0	1	0	Vci x 1.70	1	0	1	0	2.5V x 1.70 = 4.250V
1	0	1	1	Vci x 1.75	1	0	1	1	2.5V x 1.75 = 4.375V
1	1	0	0	Vci x 1.80	1	1	0	0	2.5V x 1.80 = 4.500V
1	1	0	1	Vci x 1.85	1	1	0	1	2.5V x 1.85 = 4.625V
1	1	1	0	Vci x 1.90	1	1	1	0	2.5V x 1.90 = 4.750V
1	1	1	1	Vci x 1.95	1	1	1	1	2.5V x 1.95 = 4.875V

When VCI<2.5V, Internal reference voltage will be same as VCI.

Make sure that VC[2:0] and VRH[3:0] setting restriction: VREG1OUT ≦ (DDVDH - 0.25)V.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VC[2:0]=3'h0, BT[2:0]=3'h3, PON=1'h1; VRH[3:0]=4'h8, VCIRE=1'h1
SW Reset	No change
HW Reset	VC[2:0]=3'h0, BT[2:0]=3'h3, PON=1'h1; VRH[3:0]=4'h8, VCIRE=1'h1

8.2.47. VCOM Control (D1h)

D1H	VCOM Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	0	1	D1
1st Parameter	1	1	↑	x	0	0	0	0	0	0	0	**SEL VCM**	xx
2nd Parameter	1	1	↑	x	0	0	VCM[5]	VCM[4]	VCM[3]	VCM[2]	VCM[1]	VCM[0]	xx
3rd Parameter	1	1	↑	x	0	0	0	VDV[4]	VDV[3]	VDV[2]	VDV[1]	VDV[0]	xx

Description

VCM [6:0] is used to set factor to generate VCOMH voltage from the reference voltage VREG1OUT.

VCM[5:0]	VCOMH Voltage
6'h00	VREG1OUT x 0.685
6'h01	VREG1OUT x 0.690
6'h02	VREG1OUT x 0.695
6'h03	VREG1OUT x 0.700
6'h04	VREG1OUT x 0.705
6'h05	VREG1OUT x 0.710
6'h06	VREG1OUT x 0.715
6'h07	VREG1OUT x 0.720
6'h08	VREG1OUT x 0.725
6'h09	VREG1OUT x 0.730
6'h0A	VREG1OUT x 0.735
6'h0B	VREG1OUT x 0.740
6'h0C	VREG1OUT x 0.745
6'h0D	VREG1OUT x 0.750
6'h0E	VREG1OUT x 0.755
6'h0F	VREG1OUT x 0.760
6'h10	VREG1OUT x 0.765
6'h11	VREG1OUT x 0.770
6'h12	VREG1OUT x 0.775
6'h13	VREG1OUT x 0.780
6'h14	VREG1OUT x 0.785
6'h15	VREG1OUT x 0.790
6'h16	VREG1OUT x 0.795
6'h17	VREG1OUT x 0.800
6'h18	VREG1OUT x 0.805
6'h19	VREG1OUT x 0.810
6'h1A	VREG1OUT x 0.815
6'h1B	VREG1OUT x 0.820
6'h1C	VREG1OUT x 0.825
6'h1D	VREG1OUT x 0.830
6'h1E	VREG1OUT x 0.835
6'h1F	VREG1OUT x 0.840

VCM[5:0]	VCOMH Voltage
6'h20	VREG1OUT x 0.845
6'h21	VREG1OUT x 0.850
6'h22	VREG1OUT x 0.855
6'h23	VREG1OUT x 0.860
6'h24	VREG1OUT x 0.865
6'h25	VREG1OUT x 0.870
6'h26	VREG1OUT x 0.875
6'h27	VREG1OUT x 0.880
6'h28	VREG1OUT x 0.885
6'h29	VREG1OUT x 0.890
6'h2A	VREG1OUT x 0.895
6'h2B	VREG1OUT x 0.900
6'h2C	VREG1OUT x 0.905
6'h2D	VREG1OUT x 0.910
6'h2E	VREG1OUT x 0.915
6'h2F	VREG1OUT x 0.920
6'h30	VREG1OUT x 0.925
6'h31	VREG1OUT x 0.930
6'h32	VREG1OUT x 0.935
6'h33	VREG1OUT x 0.940
6'h34	VREG1OUT x 0.945
6'h35	VREG1OUT x 0.950
6'h36	VREG1OUT x 0.955
6'h37	VREG1OUT x 0.960
6'h38	VREG1OUT x 0.965
6'h39	VREG1OUT x 0.970
6'h3A	VREG1OUT x 0.975
6'h3B	VREG1OUT x 0.980
6'h3C	VREG1OUT x 0.985
6'h3D	VREG1OUT x 0.990
6'h3E	VREG1OUT x 0.995
6'h3F	VREG1OUT x 1.000

VDV[4:0] is used to set the VCOM alternating amplitude in the range of VREG1OUT x 0.70 to VREG1OUT x 1.32.

VDV[4:0]	VCOM amplitude	VDV[4:0]	VCOM amplitude
5'h00	VREG1OUT x 0.70	5'h10	VREG1OUT x 1.02
5'h01	VREG1OUT x 0.72	5'h11	VREG1OUT x 1.04
5'h02	VREG1OUT x 0.74	5'h12	VREG1OUT x 1.06
5'h03	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.08
5'h04	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.10
5'h05	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.12
5'h06	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.14
5'h07	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.16
5'h08	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.18
5'h09	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.20
5'h0A	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.22
5'h0B	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.24
5'h0C	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.26
5'h0D	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.28
5'h0E	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.30
5'h0F	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.32

Set VDV[4:0] to let VCOM amplitude less than 6V.

SELVCM: Selection the VCM setting.

SELVCM =0	Register D1h for VCM setting
SELVCM =1	NV Memory selected for VCM setting

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VCM[5:0]=6'h00, VDV[4:0]=5'h00, SELVCM=1'h0
SW Reset	No change
HW Reset	VCM[5:0]=6'h00, VDV[4:0]=5'h00, SELVCM=1'h0

8.2.48. Power_Setting for Normal Mode (D2h)

D2H	Power_Setting for Normal Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	1	0	D2
1st Parameter	1	1	↑	x	0	0	0	0	0	AP0[2]	AP0[1]	AP0[0]	xx
2nd Parameter	1	1	↑	x	0	DC10[2]	DC10[1]	DC10[0]	0	DC00[2]	DC00[1]	DC00[0]	xx

Description

AP0[2:0]

AP0 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP0[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
3'h0	Halt operation	Halt operation
3'h1	1.00	1.00
3'h2	1.00	0.75
3'h3	1.00	0.50
3'h4	0.75	1.00
3'h5	0.75	0.75
3'h6	0.75	0.50
3'h7	0.50	0.50

DC00[2:0], DC10[2:0]

DC00/DC10 are used to select the charge-pump frequency of circuit and circuit2.

DC00[1:0]	Step-up circuit 1 clock frequency (fDCDC1)
2'h0	Fosc
2'h1	Fosc / 2
2'h2	Fosc / 4
2'h3	Fosc / 8
2'h4	Fosc / 16
2'h5	Fosc / 32
2'h6	Fosc / 64
2'h7	Halt step-up circuit 1

DC10[1:0]	Step-up circuit 2 clock frequency (fDCDC2)
2'h0	Fosc / 16
2'h1	Fosc / 32
2'h2	Fosc / 64
2'h3	Fosc / 128
2'h4	Fosc / 256
2'h5	Fosc / 512
2'h6	Setting inhibited
2'h7	Halt step-up circuit 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2
SW Reset	No change
HW Reset	AP0[2:0]=3'h1, DC10[2:0]=3'h2, DC00[2:0]=3'h2

8.2.49. Power_Setting for Partial Mode (D3h)

D3H	Power_Setting for Partial Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	0	1	1	D3
1st Parameter	1	1	↑	x	0	0	0	0	0	AP1[2]	AP1[1]	AP1[0]	xx
2nd Parameter	1	1	↑	x	0	DC11[2]	DC11[1]	DC11[0]	0	DC01[2]	DC01[1]	DC01[0]	xx

Description

AP1[2:0]

AP1 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP1=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP1[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
3'h0	Halt operation	Halt operation
3'h1	1.00	1.00
3'h2	1.00	0.75
3'h3	1.00	0.50
3'h4	0.75	1.00
3'h5	0.75	0.75
3'h6	0.75	0.50
3'h7	0.50	0.50

DC01[2:0], DC11[2:0]

DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.

DC01[1:0]	Step-up circuit 1 clock frequency (fDCDC1)
2'h0	Fosc
2'h1	Fosc / 2
2'h2	Fosc / 4
2'h3	Fosc / 8
2'h4	Fosc / 16
2'h5	Fosc / 32
2'h6	Fosc / 64
2'h7	Halt step-up circuit 1

DC11[1:0]	Step-up circuit 2 clock frequency (fDCDC2)
2'h0	Fosc / 16
2'h1	Fosc / 32
2'h2	Fosc / 64
2'h3	Fosc / 128
2'h4	Fosc / 256
2'h5	Fosc / 512
2'h6	Setting inhibited
2'h7	Halt step-up circuit 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2
SW Reset	No change
HW Reset	AP1[2:0]=3'h1, DC11[2:0]=3'h2, DC01[2:0]=3'h2

8.2.50. Power_Setting for Idle Mode (D4h)

D4H	Power_Setting for Idle Mode												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	0	1	0	1	0	0	D4
1st Parameter	1	1	↑	x	0	0	0	0	0	AP2[2]	AP2[1]	AP2[0]	xx
2nd Parameter	1	1	↑	x	0	DC12[2]	DC12[1]	DC12[0]	0	DC02[2]	DC02[1]	DC02[0]	xx

Description

AP2[2:0]

AP2 bit is used to adjust the constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off between the display quality and the current consumption into account. In no-display period, set AP2=3'h0 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

AP2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
3'h0	Halt operation	Halt operation
3'h1	1.00	1.00
3'h2	1.00	0.75
3'h3	1.00	0.50
3'h4	0.75	1.00
3'h5	0.75	0.75
3'h6	0.75	0.50
3'h7	0.50	0.50

DC02[2:0], DC12[2:0]

DC01/DC11 are used to select the charge-pump frequency of circuit and circuit2.

DC02[1:0]	Step-up circuit 1 clock frequency (fDCDC1)
2'h0	Fosc
2'h1	Fosc / 2
2'h2	Fosc / 4
2'h3	Fosc / 8
2'h4	Fosc / 16
2'h5	Fosc / 32
2'h6	Fosc / 64
2'h7	Halt step-up circuit 1

DC12[1:0]	Step-up circuit 2 clock frequency (fDCDC2)
2'h0	Fosc / 16
2'h1	Fosc / 32
2'h2	Fosc / 64
2'h3	Fosc / 128
2'h4	Fosc / 256
2'h5	Fosc / 512
2'h6	Setting inhibited
2'h7	Halt step-up circuit 2

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	AP2[2:0]=3'h1, DC12[2:0]=3'h2, DC02[2:0]=3'h2
SW Reset	No change
HW Reset	AP2[2:0]=3'h1, DC11[2:0]=3'h2, DC02[2:0]=3'h2

8.2.51. NV Memory Write (E0h)

E0H	NV Memory Write												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	0	0	E0
1st Parameter	1	1	↑	x	VM_D [7]	VM_D [6]	VM_D [5]	VM_D [4]	VM_D [3]	VM_D [2]	VM_D [1]	VM_D [0]	xx
Description	This command is used to program the NV memory data. **VM_D[7:0]:** Use to write the data (including VCM and ID code) into the NV memory data. When program VCM: 1. VM_D[7]: Must be set to"1". 2. VM_D[6]: Set to "0" when SELVCM=1. 3. VM_D[5:0]: Program VCM data.												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	VM_D[7:0]=8'h00
SW Reset	No change
HW Reset	VM_D[7:0]=8'h00

8.2.52. NV Memory Control (E1h)

E1H	NV Memory Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	0	1	E1
1st Parameter	1	1	↑	x	0	0	ID_ PGM_EN	VCM_ PGM_EN	0	0	ID_SEL[1]	ID_SEL[0]	xx

Description

This command is used to control the NV memory programming.

ID_SEL[1:0]: ID NV memory selection

ID_SEL[1:0]	ID OTP Selection
00	ID code 1 [15:8]
01	ID code 1 [7:0]
10	ID code 2 [15:8]
11	ID code 2 [7:0]

VCM_PGM_EN: VCM OTP programming enable. When writing the VCOMH NV memory, the bit must be set as '1'.

ID_PGM_EN: ID OTP programming enable. When writing the ID code NV memory, the bit must be set as '1'.

ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection
0	0	NV Memory programming disabled
0	1	VCM (VCOMH) NV Memory programming enable
1	0	ID code NV Memory programming enable
1	1	Setting Prohibited

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_SEL[1:0]=2'h0
SW Reset	No change
HW Reset	ID_PGM_EN=1'h0; VCM_PGM_EN=1'h0; ID_SEL[1:0]=2'h0

8.2.53. NV Memory Status Read (E2h)

E2H	NV Memory Status Read												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	x	1	1	1	0	0	0	1	0	E2
1st Parameter	1	↑	1	x	x	x	x	x	x	x	x	x	x
2nd Parameter	1	↑	1	x	0	0	0	0	0	0	PGM_ CNT1	PGM_ CNT0	xx
3rd Parameter	1	↑	1	x	0	0	NV_ VCM[5]	NV_ VCM[4]	NV_ VCM[3]	NV_ VCM[2]	NV_ VCM[1]	NV_ VCM[0]	xx

Description

PGM_CNT[1:0]: NV memory programmed record. The bit will increase "+1" automatically when writing the NV_VCM [5:0].

PGM_CNT[1:0]	Description
00	NV Memory clean
01	NV Memory programmed 1 time
10	NV Memory programmed 2 times

These bits are read only.

NV_VCM [5:0]: NV memory VCM data read value. These bits are read only.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

8.2.54. NV Memory Protection (E3h)

E3H	NV Memory Protection												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	--	1	1	1	0	0	0	1	1	E3
1st Parameter	1	1	↑	--	KEY [15]	KEY [14]	KEY [13]	KEY [12]	KEY [11]	KEY [10]	KEY [9]	KEY [8]	xx
2nd Parameter	1	1	↑	--	KEY [7]	KEY [6]	KEY [5]	KEY [4]	KEY [3]	KEY [2]	KEY [1]	KEY [0]	xx
Description	**KEY[15:0]:** NV memory programming protection key. When writing OTP data C8h, this register must be set as 0xAA55 to enable OTP programming. If C8h register is not written with 0xAA55, NV Memory programming will fail.												
Restriction													
Register Availability													
Default													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

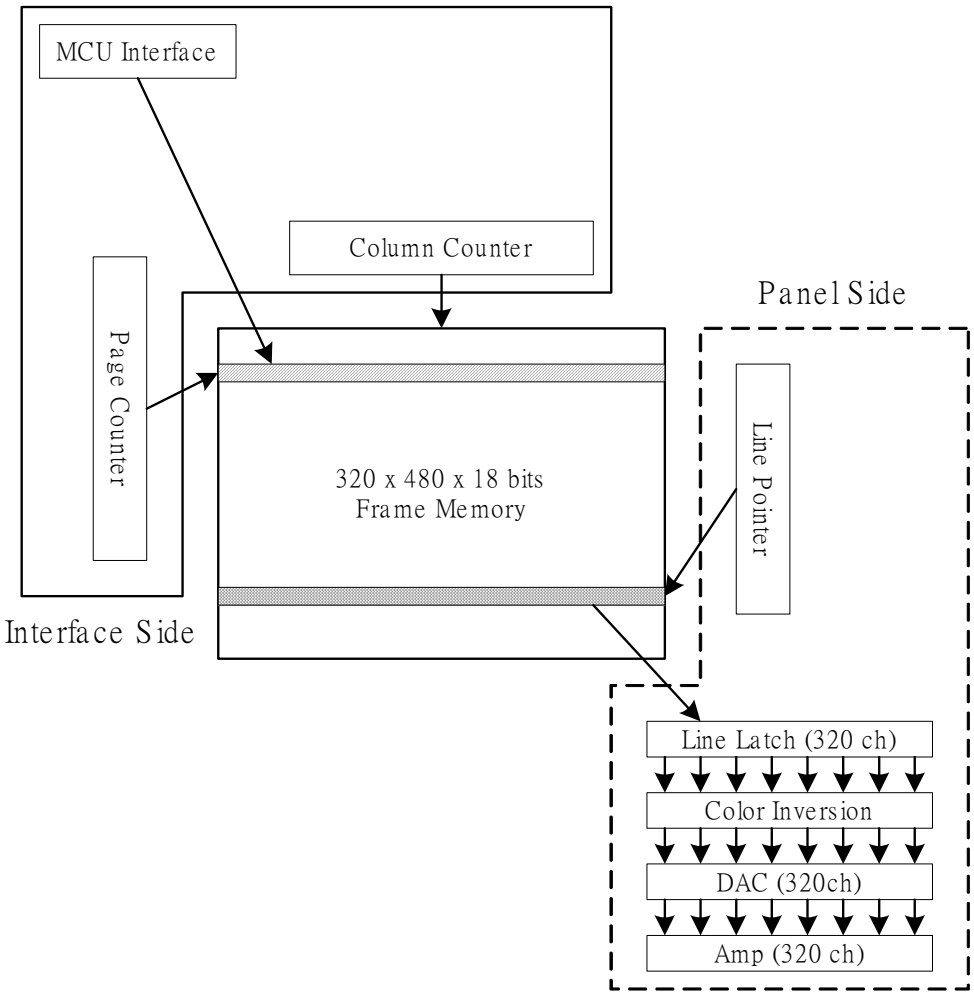
Status	Default Value
Power On Sequence	KEY[15:0]=16'h0000
SW Reset	No change
HW Reset	KEY[15:0]=16'h0000

9. Display Data RAM

9.1. Configuration

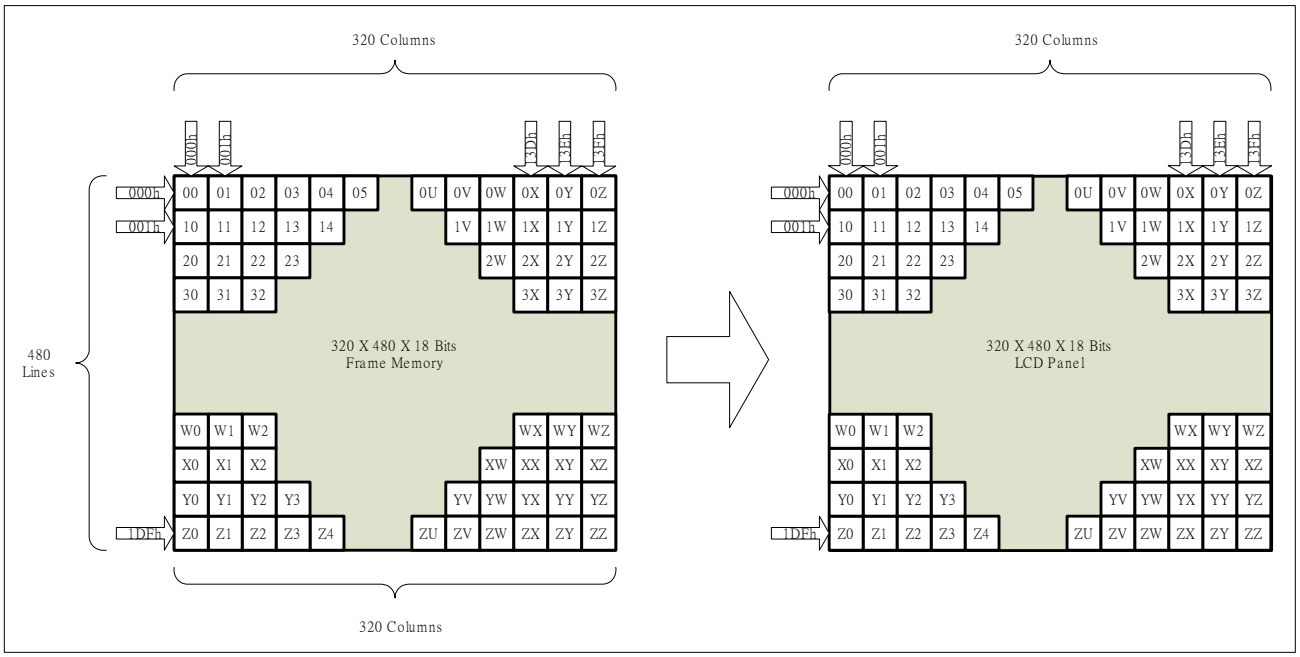
The display data RAM stores display dots and consists of 2,764,800bits (320 x 18 x 480 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC.

There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the frame memory.



9.2. Memory to Display Address Mapping

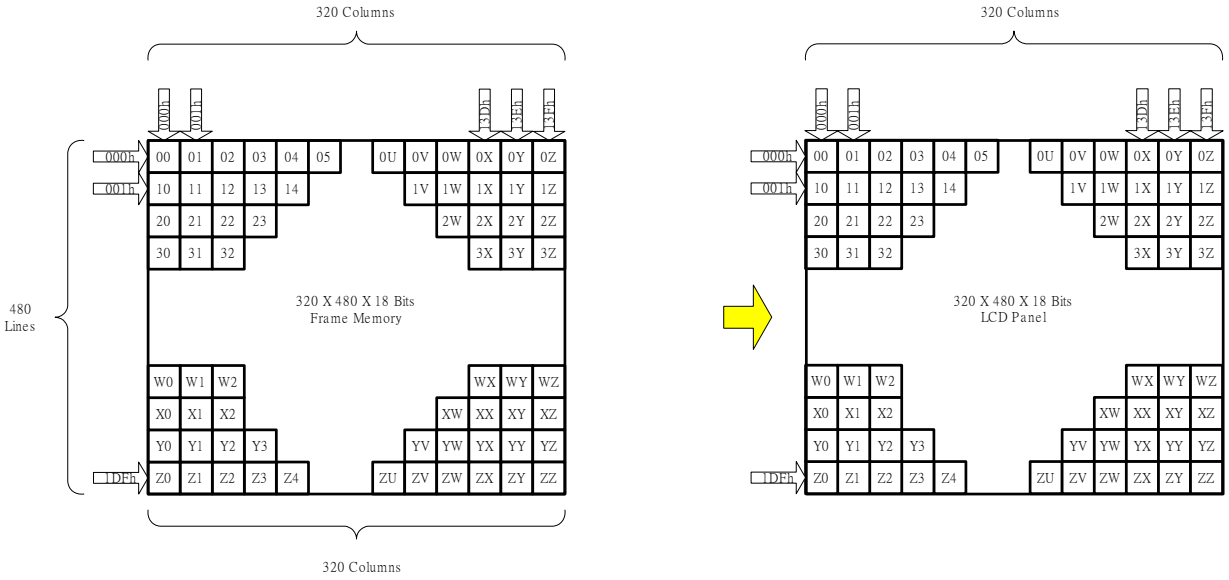
In this mode, content of the frame memory within an area where column pointer is 0000h to 013Fh and page pointer 0000h to 01DFh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0).



9.3. Vertical Scroll Mode

There is a vertical scrolling mode, which is described by the commands “set_scroll_area”(33h) and “set_scroll_start”(37h).

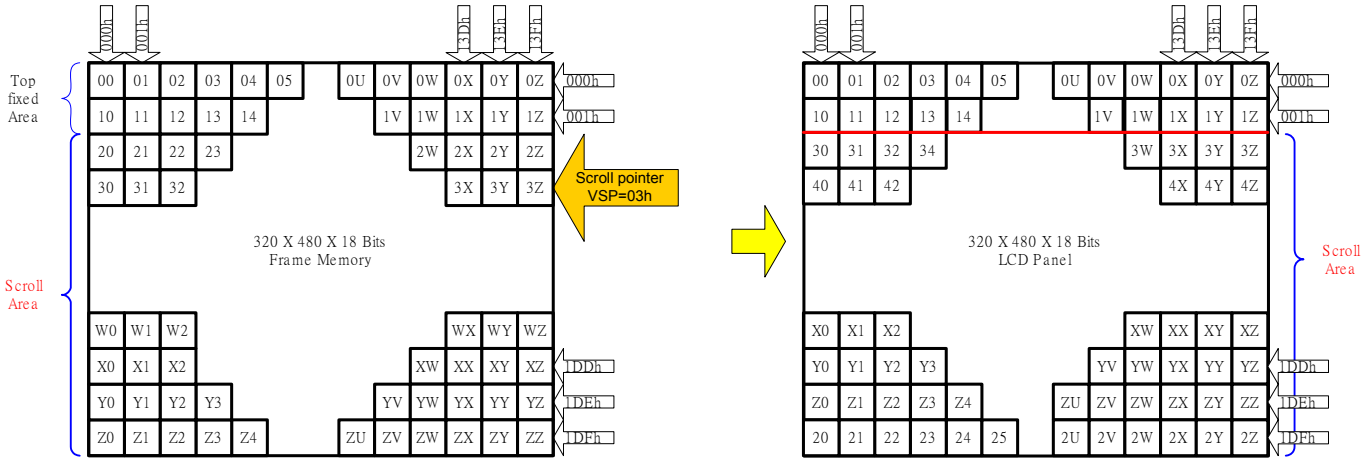
(1)Normal Display On or Partial Mode On, Vertical Scroll Off



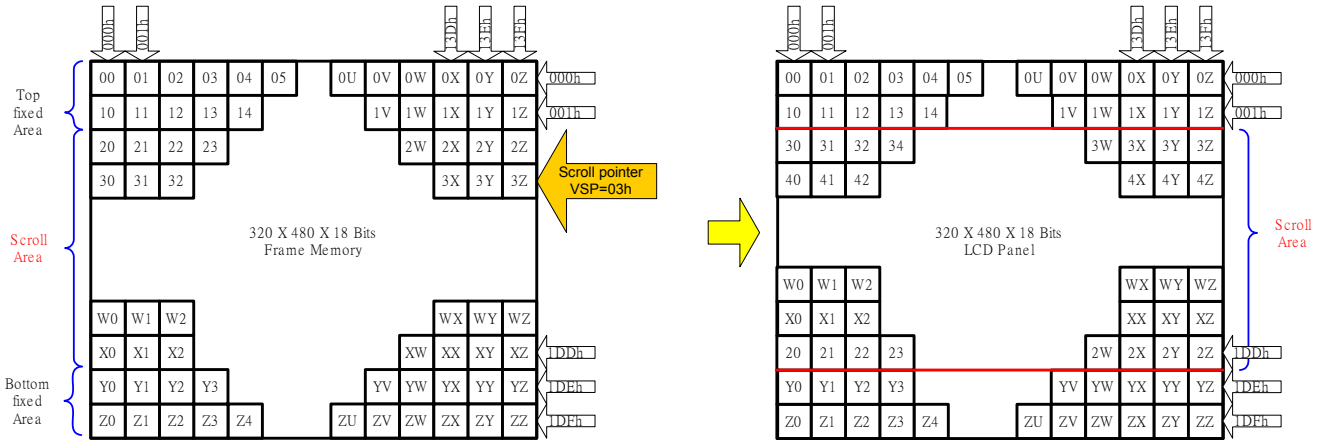
(2) Vertical Scroll Mode

“set_scroll_area(33h)”and ”set_scroll_start(37h)” setting define the scroll area.

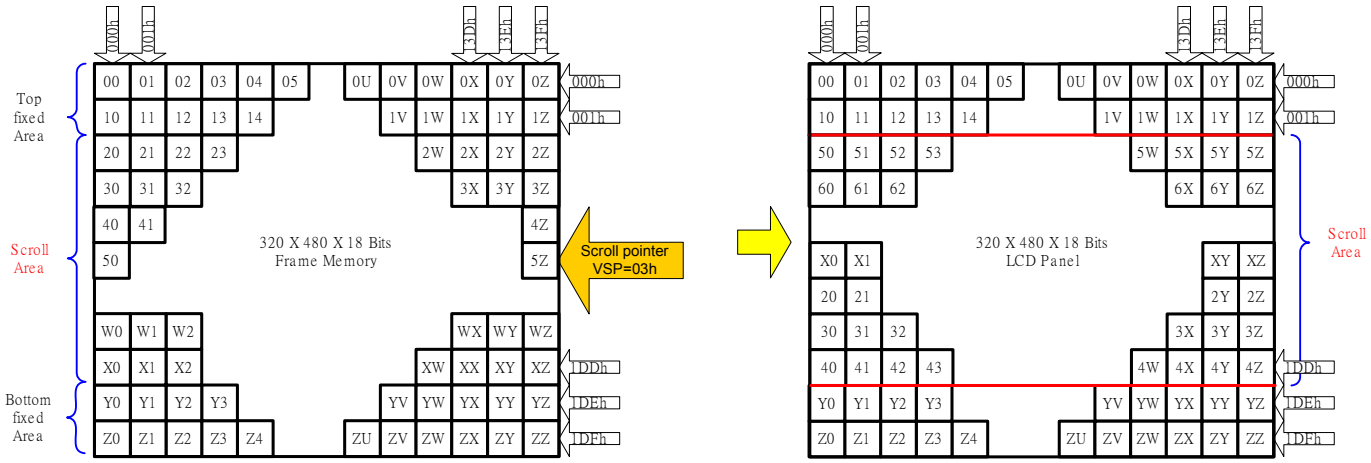
Example1: TFA=2, VSA=478, BFA=0 (set_address_mode(36h) B4=0), VSP=3



Example2: TFA=2,VSA=476,BFA=2 (set_address_mode(36h) B4=0), VSP=3



Example3: TFA=2,VSA=476,BFA=2 (set_address_mode(36h) B4=0), VSP=5

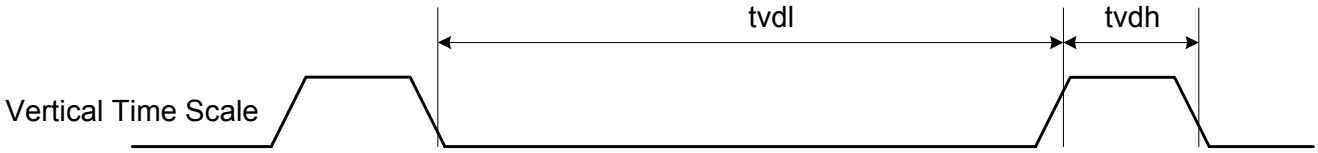


10. Tearing Effect Output

The tearing effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the set_tear_off (34h) and set_tear_on (35h) commands. The mode of the tearing effect signal is defined by the parameter of the set_tear_on (35h) and set_tear_scanline(44h) commands.
The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

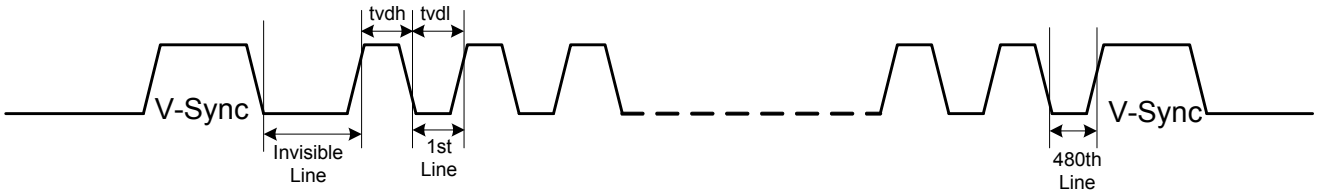
10.1. Tearing Effect Line Modes

Mode 1 (set_tear_on, TELOM=0) , the Tearing Effect Output signal consists of V-Sync information only:

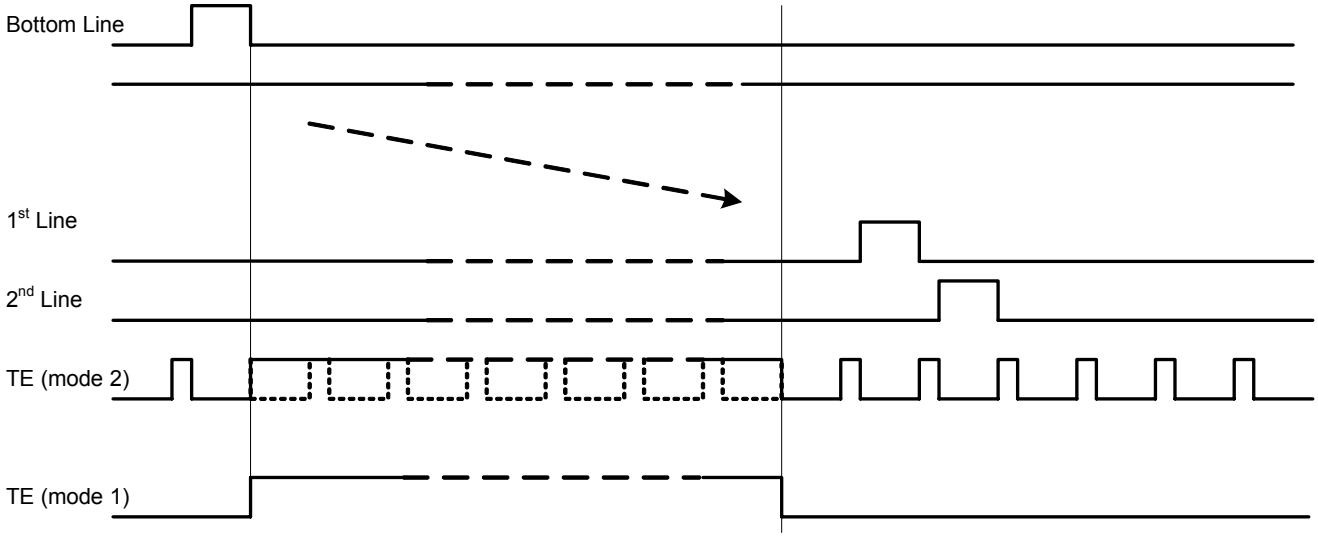


tvdh = The LCD display is not updated from the Frame Memory.
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2 (set_tear_on, TELOM=1), the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 480 H-sync pulses per field:



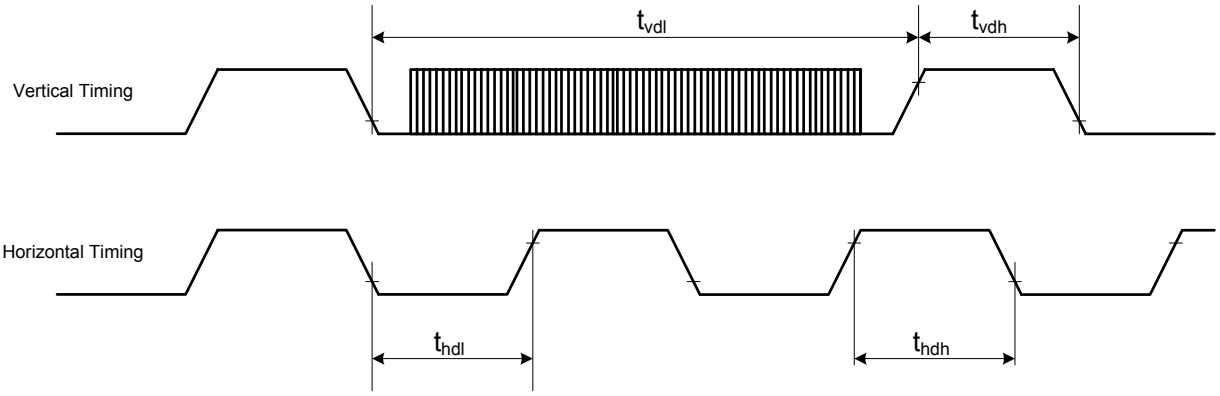
thdh = The LCD display is not updated from the Frame Memory.
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

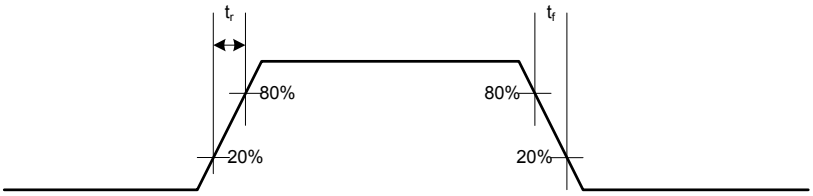


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	16.5		ms	
t_{vdh}	Vertical timing high duration	302		us	
t_{hdl}	Horizontal timing low duration	11.2		us	
t_{hdh}	Horizontal timing high duration	22.4		us	

Notes:

1. The timings in Table 8.3.1 apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

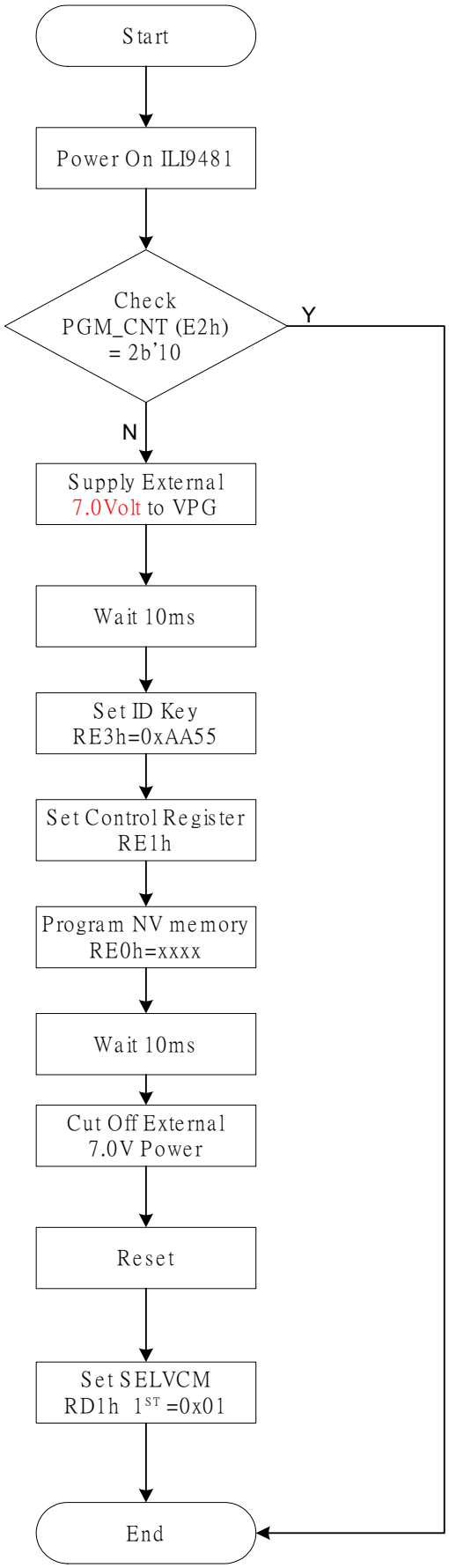


The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the set_tear_off(34h), set_tear_on(35h) commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

TEON (35h)	TELOM (35h, 1st bit)	TE signal Output
0	*	GND
1	0	TE (Mode 1)
1	1	TE (Mode 2)

11. NV Memory Programming Flow



12. Gamma Correction

ILI9481 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9481 available with liquid crystal panels of various characteristics.

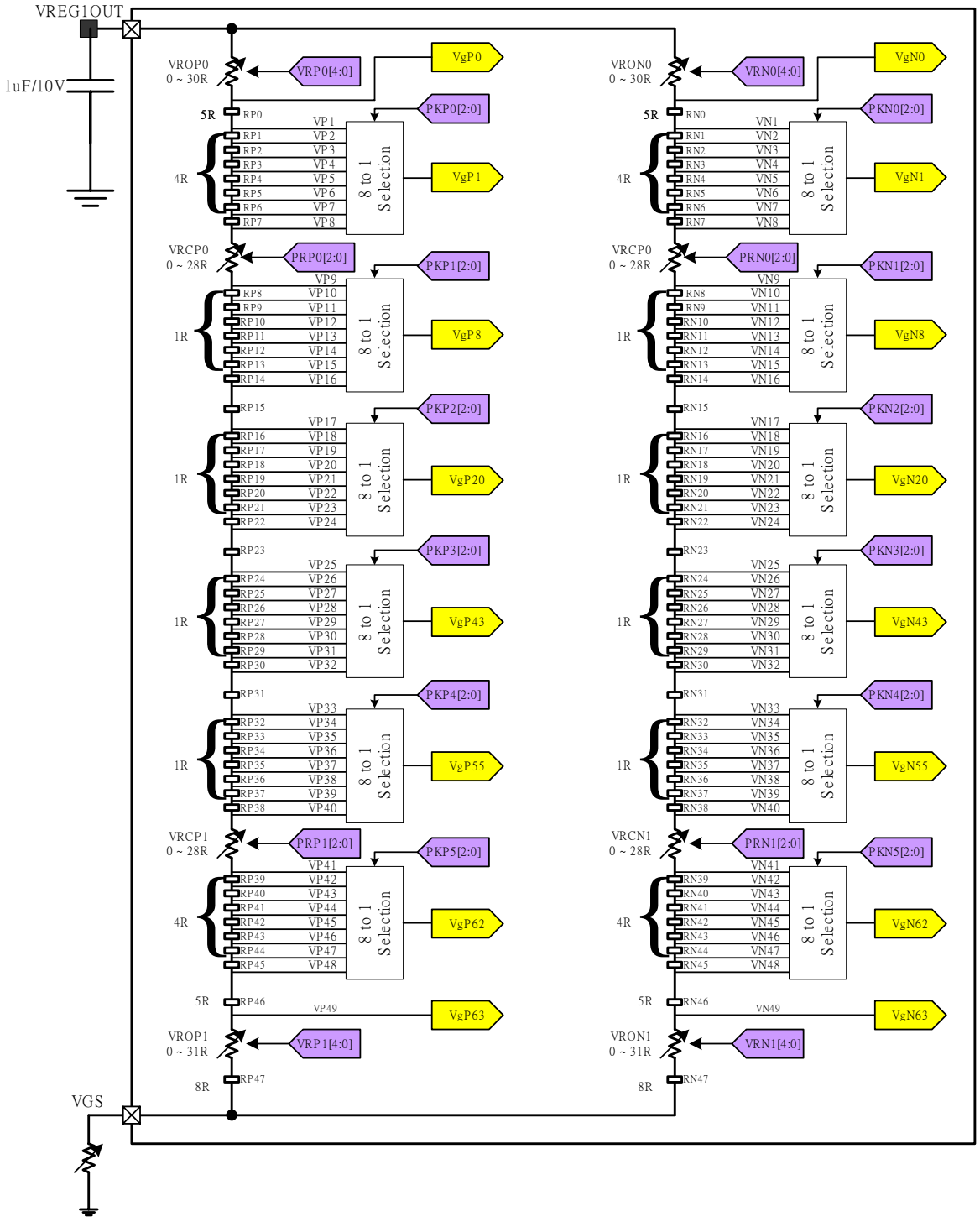
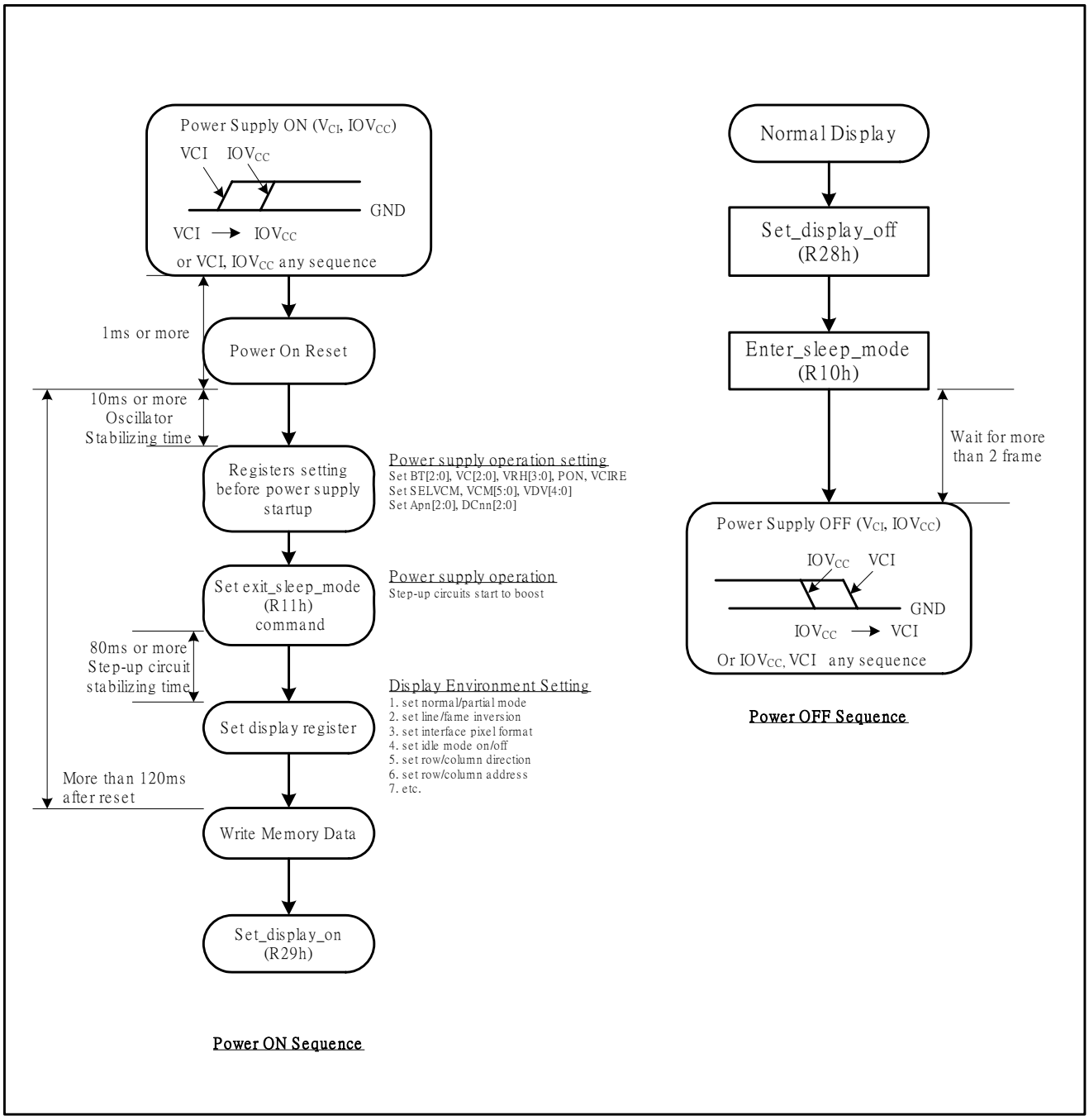


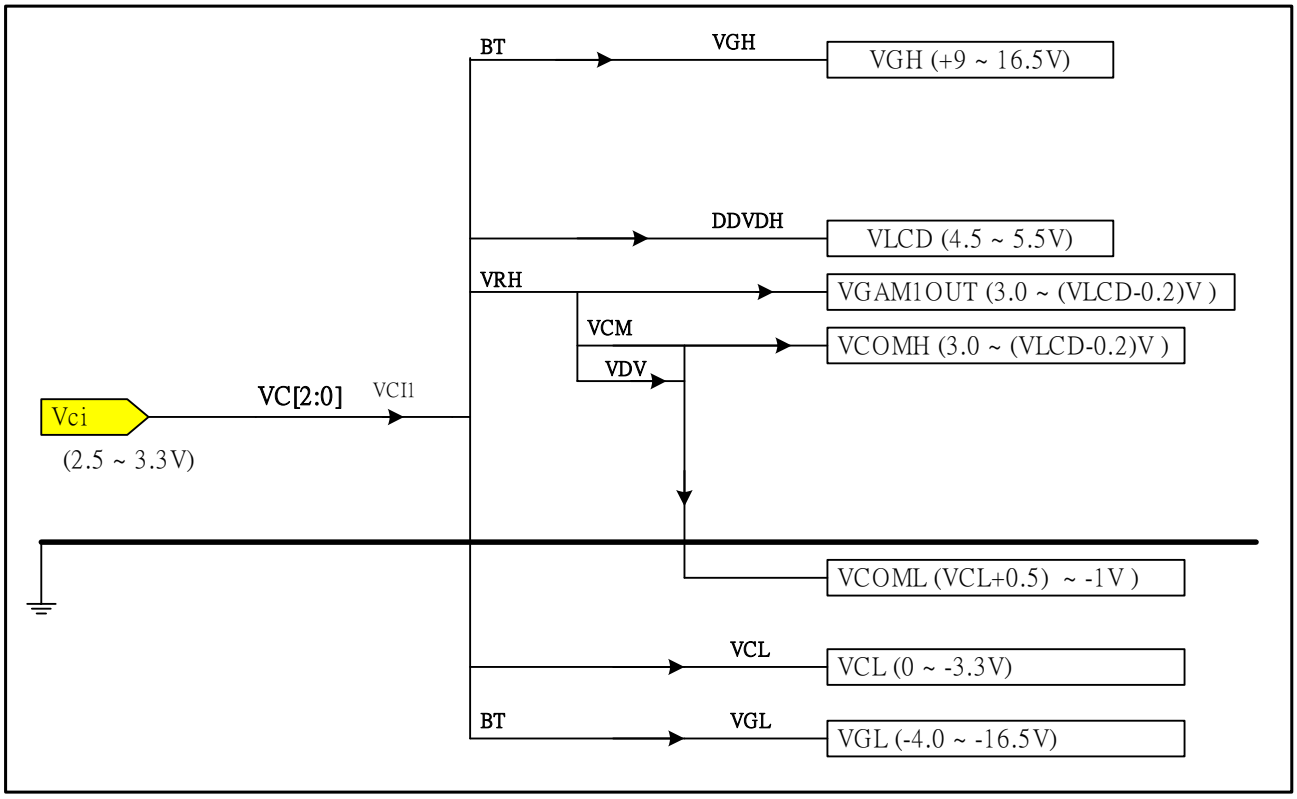
Figure 1 Grayscale Voltage Adjustment

13. Application

13.1. Power Supply Configuration



13.2. Voltage Generation



14. Electrical Characteristics

14.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9481 is used out of the absolute maximum ratings, the ILI9481 may be permanently damaged. To use the ILI9481 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9481 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage	IOVCC	V	-0.3 ~ + 4.6	1,
Power supply voltage	VCI - GND	V	-0.3 ~ + 4.6	2
Power supply voltage	DDVDH - GND	V	-0.3 ~ + 6.5	3
Power supply voltage	GND -VCL	V	-0.3 ~ + 4.6	4
Power supply voltage	DDVDH - VCL	V	-0.3 ~ + 9.0	
Power supply voltage	VGH - GND	V	-0.3 ~ + 18.5	
Power supply voltage	GND - VGL	V	-0.3 ~ + 18.5	
Power supply voltage	VGH - VGL	V	-0.3 ~ + 32	
Input voltage	Vt	V	-0.3 ~ IOVCC+ 0.3	
Operating temperature	Topr	°C	-40 ~ + 85	
Storage temperature	Tstg	°C	-55 ~ + 110	

Notes:

1. Make sure IOVCC ≥ GND
2. Make sure VCI ≥ AGND.
3. Make sure DDVDH ≥ VCL and DDVDH ≥ VCI
4. Make sure AGND ≥ VGL.

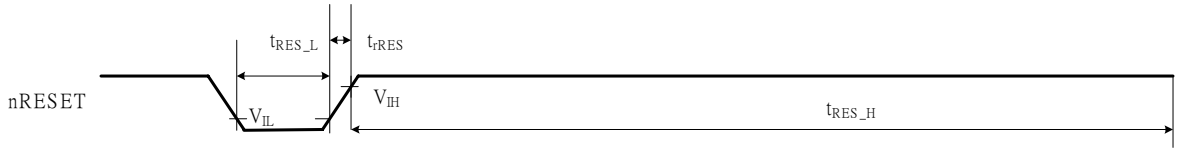
14.2. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog Power Supply Voltage	VCI	Analog Operation Voltage	2.5	2.8	3.3	V
I/O pin Power Supply Voltage	IOVCC	I/O pin Operation Voltage	1.65	2.8	3.3	V
Logic High level input voltage	V_{IH}	IOVCC = 1.65V ~ 3.3V	0.7*IOVCC	-	IOVCC	V
Logic Low level input voltage	V_{IL}	IOVCC = 1.65V ~ 3.3V	0.0	-	0.3*IOVCC	V
Logic High level Output voltage	V_{IH}	Iout = -1 mA	0.8*IOVCC	-	IOVCC	V
Logic Low level Output voltage	V_{IL}	Iout = +1 mA	0.0	-	0.2*IOVCC	V
Logic High level input current	I_{IHD}	D[17:0]			10	uA
Logic Low level input current	I_{ILD}	D[17:0]	-10			uA

14.3. Reset Timing Characteristics

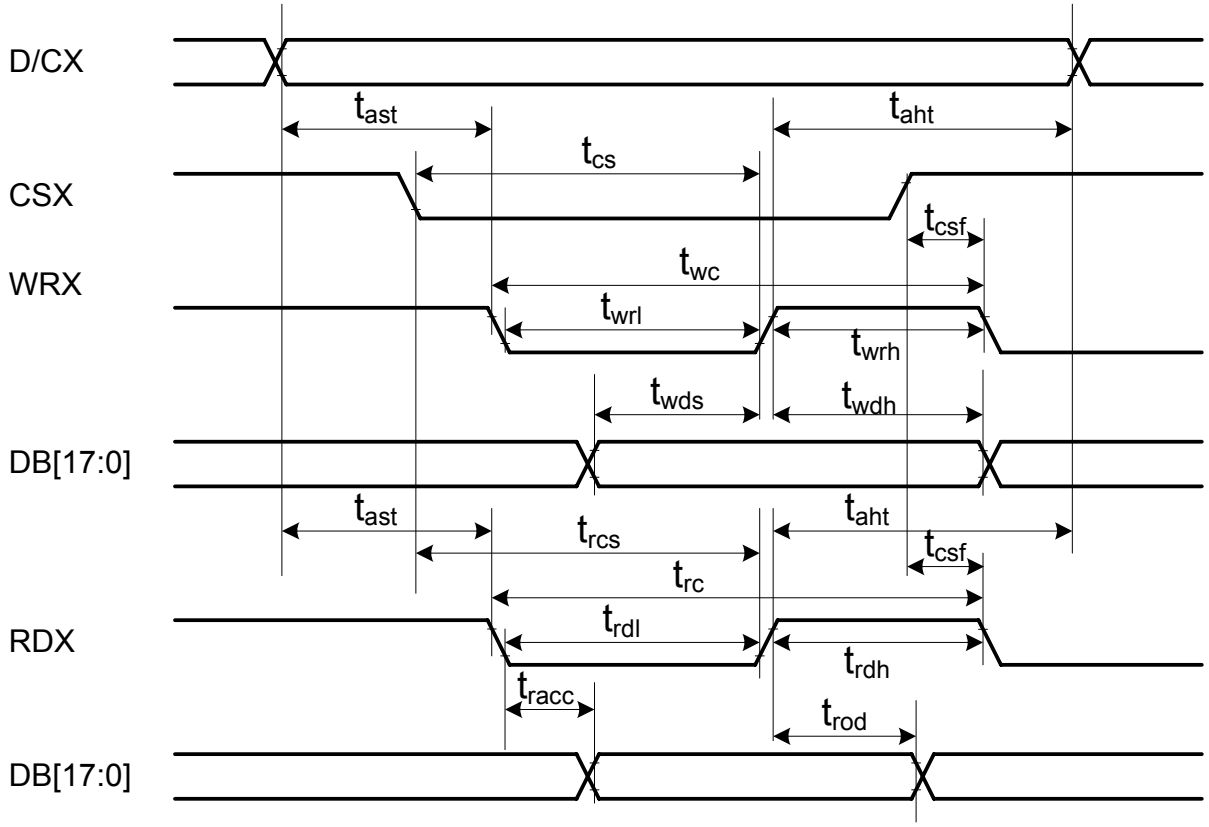
Reset Timing Characteristics (IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	t_{RES_L}	ms	1	-	-
Reset rise time	t_{rRES}	µs	-	-	10
Reset high-level width	t_{RES_H}	ms	50	-	-



14.4. AC Characteristics

14.4.1. DBI Type B (18/16/9/8 bit) Interface Timing Characteristics

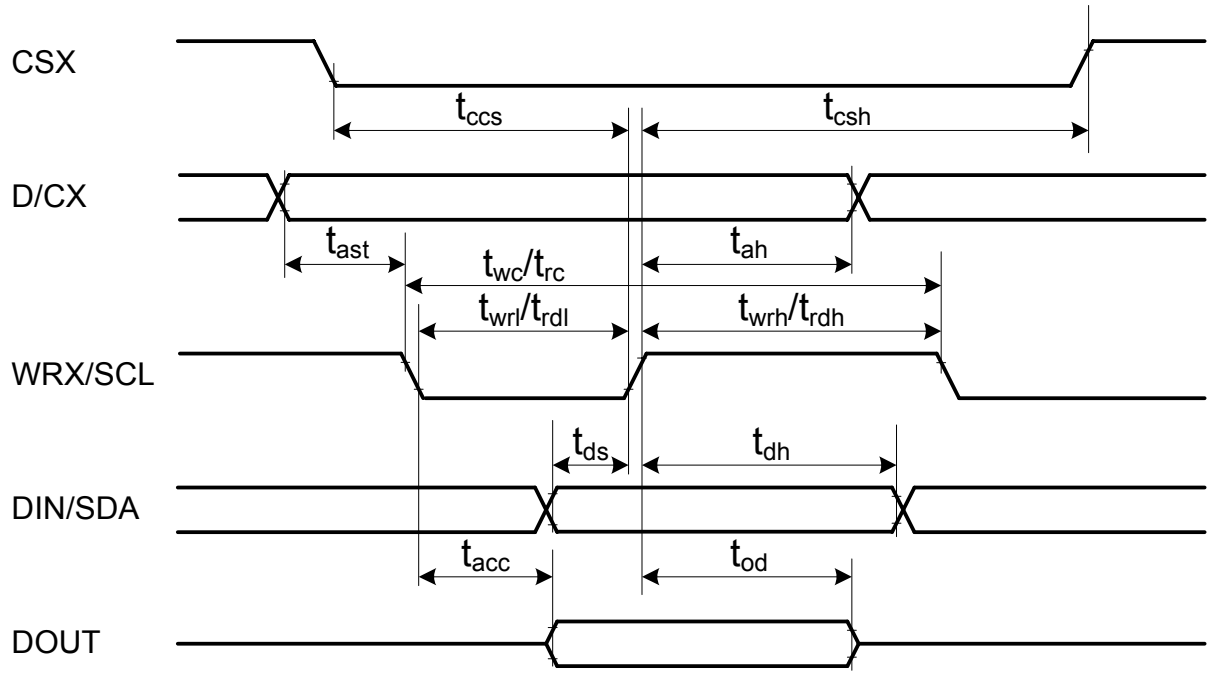


Signal	Symbo l	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	10	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tcs	Chip Select setup time (Write)	20	-	ns	
	trcs	Chip Select setup time (Read)	20	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	20	-	ns	
WRX	twc	Write cycle	100	-	ns	
	twrh	Write Control pulse H duration	30	-	ns	
	twrl	Write Control pulse L duration	25	-	ns	
RDX	trc	Read cycle	450	-	ns	
	trdh	Read Control pulse H duration	250	-	ns	
	trdl	Read Control pulse L duration	170	-	ns	
DB[17:0], DB[15:0], DB[8:0], DB[7:0]	twds	Write data setup time	15	-	ns	For maximum CL=30pF For minimum CL=8pF
	twdh	Write data hold time	25	-	ns	
	tracc	Read access time	10	340	ns	
	trod	Read output disable time	10	-	ns	

Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

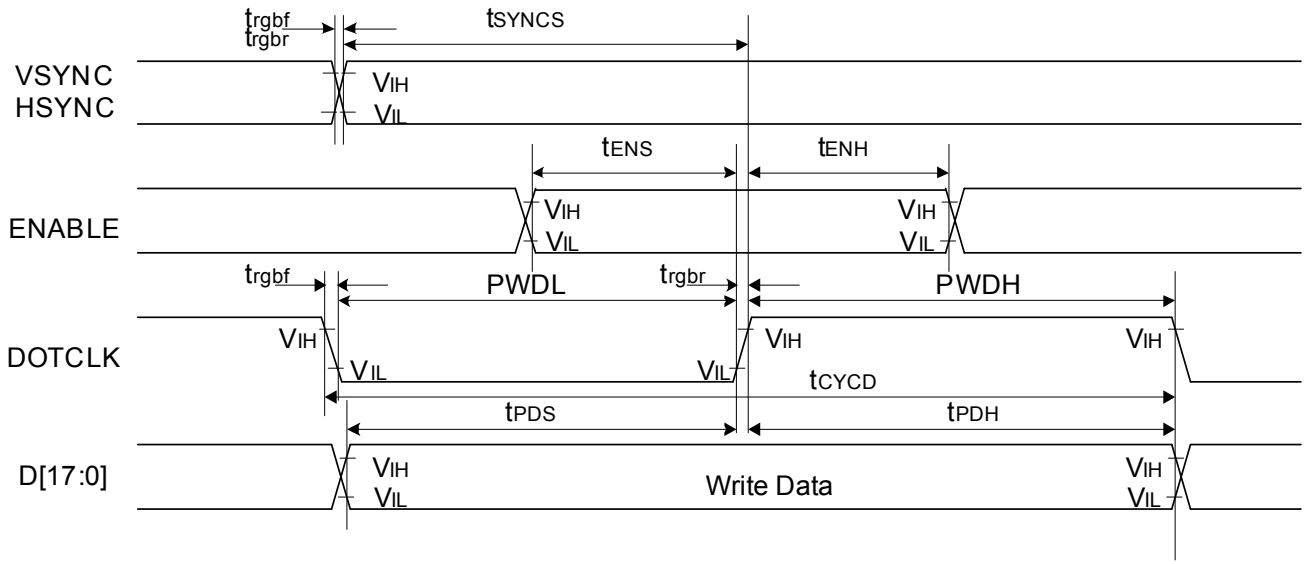
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, GND=0V

14.4.2. DBI Type C Interface Timing Characteristics



Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{css}	Chip select setup time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Write)	40	-	ns	
D/CX	t_{as}	Address setup time	10		ns	
	t_{ah}	Address hold time (Write/Read)	10		ns	
WRX/SCL (Write)	t_{wc}	Write cycle	100		ns	
	t_{wrh}	SCL High duration (write)	40		ns	
	t_{wrl}	SCL Low duration (write)	40		ns	
WRX/SCL (Read)	t_{rc}	Read cycle	300		ns	
	t_{rdh}	SCL High duration (read)	120		ns	
	t_{rdl}	SCL Low duration (read)	120		ns	
DIN/SDA (Driver IC)	t_{ds}	Data setup time	30		ns	
	t_{dh}	Data hold time	30		ns	
DOUT (Driver IC)	t_{acc}	Access time	-	110	ns	
	t_{od}	Output disable time	10		ns	

14.4.3. DPI Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns
ENABLE	t_{ENS}	ENABLE setup time	15	-	ns
	t_{ENH}	ENABLE hold time	15	-	ns
D[17:0]	t_{POS}	Data setup time	15	-	ns
	t_{PDH}	Data hold time	15	-	ns
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns
	PWDL	DOTCLK low-level period	15	-	ns
	t_{CYCD}	DOTCLK cycle time	104	-	ns
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns

15. Revision History

Version No.	Date	Page	Description
0.00	2007/1/8		New Formal Create
0.25	2008/2/22	13	Modify Pin141~143 : VGREG1OUT
		138	Modify tast = 10, trcs = 20, twc = 100, twrh=30, twrl = 20
0.26	2008/3/11	115	Modify VC Table
		116	Modify VCIRE Table
0.27	2008/4/28	98	Modify the default value of WEMODE
			Change NV memory programming voltage (6V → 7V)
0.28	2008/6/28	98	Remove DSTB function.
0.29	20008/11/26	98	Delete Note2
		11	Add external component specification
0.3	2009/06/12	12	Modify Type error in Pad arrangement and Coordination
		34	Modify DPI PCLK timing
		138	Modify DPI timing Characteristics
0.31	2009/06/29	135	Add power on sequence
0.32	2009/07/27	135	PCLK frequence
0.33	2009/08/05		Register default value
		34	Modify DPI PCLK timing
		137	Add Voltage Generation
		138	Add Reset timing
0.34	2009/10/22	35	Add timing limitation
		91	Modify the register parameter setting
0.35	2009/11/24	35	Modify RGB PCLK limitation
		141	