Features

- Fast 8-bit MPU interface compatible with 80-and 68-family microcomputers
- Many command set
- Total 80 (segment + common) drive sets
- Low power 30 μW at 2 kHz external clock
- Wide range of supply voltages
- V_{DD}-Vss: +2.7~+5.5V
  V_{DD}-V_5: +3.5~+13.0V
- Low-power CMOS

Descriptions

The NT7450B family of dot matrix LCD drivers is designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM. The drivers are available in two configurations. The NT7450B family drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.

These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

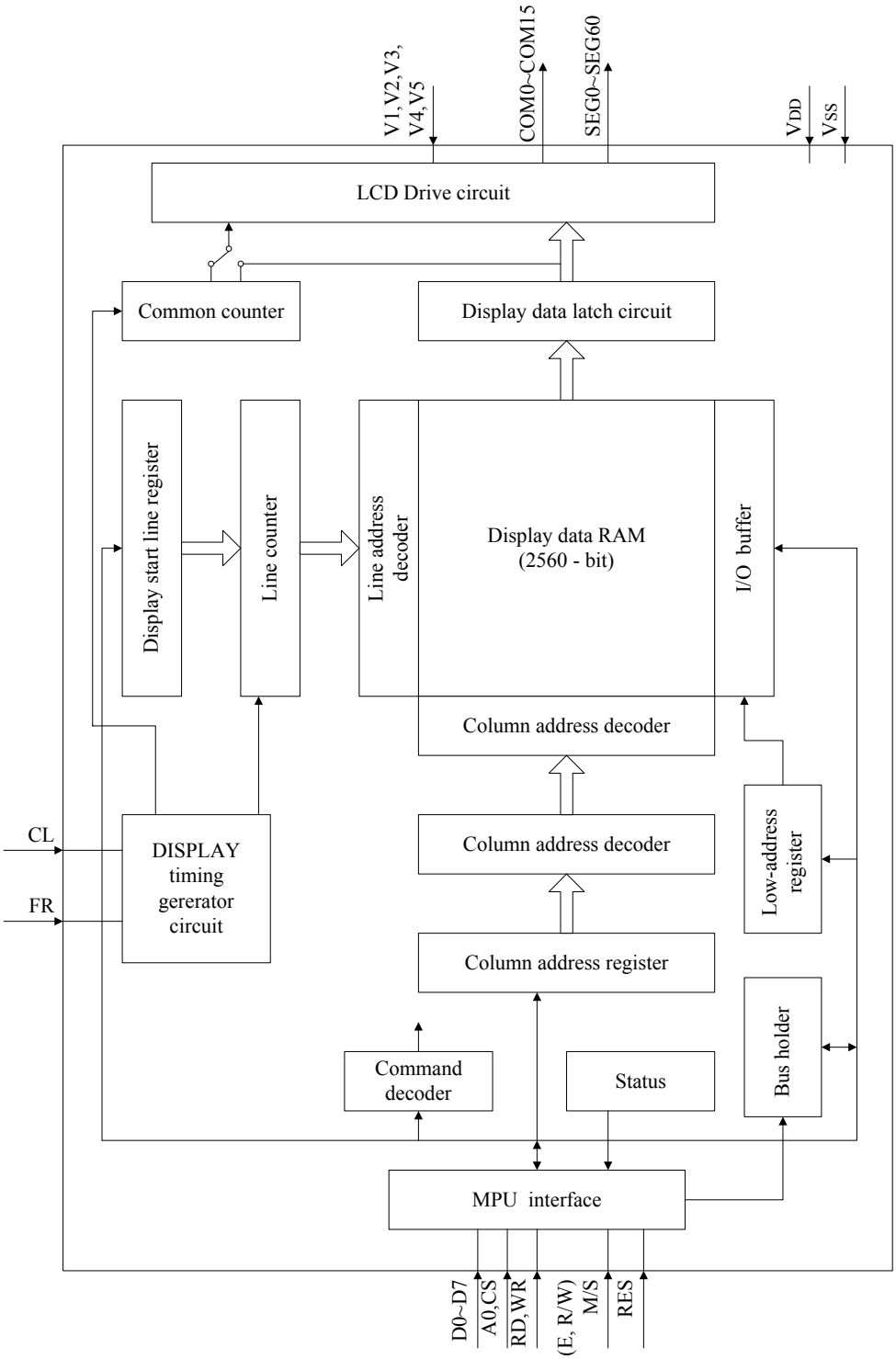
The NT7450B which is able to drive two lines of twelve characters each.

Order Information

NT7450B-OAZ0

- Package Type
  Z0：Bare Chip
- Clock Frequency
  OA：18KHz(On chip & Internal)

BOLCK DIAGRAM



PIN DESCRIPTION

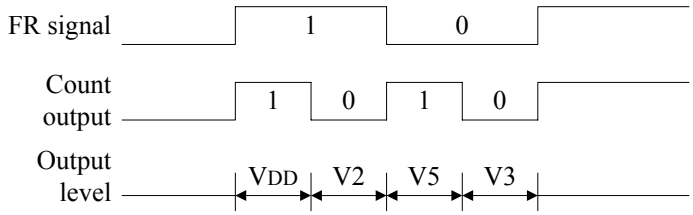
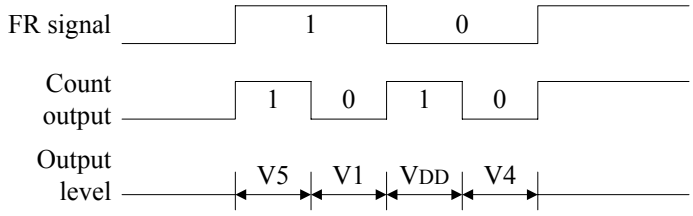
Power Pins

Name	Description
VDD	Connected to the +5V dc power. Common to the Vcc MPU power pin.
VSS	0Vdc pin connected to the system ground.
V1,V2,V3,V4,V5	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp and supplied. These voltages must satisfy the following: VDD≧V1≧V2≧V3≧V4≧V5

System Bus Connection Pins

Name	Description
D7 to D0	Three-state I/O. The 8-bit bi-directional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ⊓ the 68-series MPU is initialized, and when it goes ⊔, the 80-series MPU is initialized. The system is reset during edge sense of the RES signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level : 80-series MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only. An address bus signal is usually decoded by use of chip select signal, and it is entered. If the system has a built-in oscillator, this is used as an input pin to the oscillator amp and a Rf oscillator resistor is connected to it. In such case, the $\overline{RD}$, $\overline{WR}$ and E signals must be ORed with the $\overline{CS}$ signals and entered.
E($\overline{RD}$)	If the 68-series MPU is connected: Input. Active high. Used as an enable clock input of the 68-series MPU. If the 80-series MPU is connected: Input. Active low. The $\overline{RD}$ signal of the 80series MPU is entered in this pin. When this signal is kept low, the NT7450B data bus is in the output status.
R/$\overline{W}$($\overline{WR}$)	If the 68-series MPU is connected: Input. Used as input pins of read control signals (if R/$\overline{W}$ is high) or writes control signals (if low). If the 80-series MPU is connected: Input. Active low. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

LCD Drive Circuit Signals

<table>
<tr><th>Name</th><th>Description</th></tr>
<tr><td>CL</td><td>Input.
Effective for an external clock operation model only.
This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges. If the system has a built-in oscillator. This is used as an output pin for the oscillator amp and a Rf oscillator resistor is connected to it.</td></tr>
<tr><td>FR</td><td>Input/output.
This is an I/O pin of LCD AC signals, and connected to the M terminal of common driver.
I/O selection
Common oscillator built-in model: Output if M/S is 1;
Input if M/S is 0
Dedicate segment model: Input</td></tr>
<tr><td>SEGn</td><td>Output.
The output pin for LCD column (segment) driving. A single level of VDD, V2, V3 and V5 is selected by the combination of display RAM contents and FR signal.
 
</td></tr>
<tr><td>COMn</td><td>Output.
The Output pin for LCD common (Low) driving. A single level of VDD, V1, V4 and V5 is selected by the combination of common counter output and FR signal. The slave LSI has the reverse common output scan sequence than the master LSI.
 
</td></tr>
<tr><td>M/S</td><td>Input.
The master LSI or slave LSI operation select pin for the NT7450B.
Connected to VDD (to select the master LSI operation mode) or Vss (to select the slave LSI operation mode).
When this M/S pin is set, the functions of FR, COM0 to COM15, OSC1 (CS), and OSC2 (CL) pins are changed.
<table>
<tr><td rowspan="4">NT7450BOA</td><td>M/S</td><td>FR</td><td>COM output</td><td>OSC1</td><td>OSC2</td></tr>
<tr><td>VDD</td><td>Output</td><td>COM0 to COM15</td><td>Input</td><td>Output</td></tr>
<tr><td>Vss</td><td>Input</td><td>COM31 to COM16</td><td>NC</td><td>Input</td></tr>
</table>
*The slave driver has the reverse common output scan sequence than the master driver.</td></tr>
</table>

BLOCK DESCRIPTION

System Bus

MPU interface

Selecting an interface type

The NT7450B series transfers data via 8-bit bi-directional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of high or low RES signal level after reset (see Table 1).

When the $\overline{CS}$ signal is high, the NT7450B series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table 1

$\overline{RES}$ signal input level	MPU type	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7
Active low	68-series	↑	↑	↑	↑	↑
Active High	80-series	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

Data transfer

The NT7450B and NT7451B divers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used are given in the table blow.

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.

No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

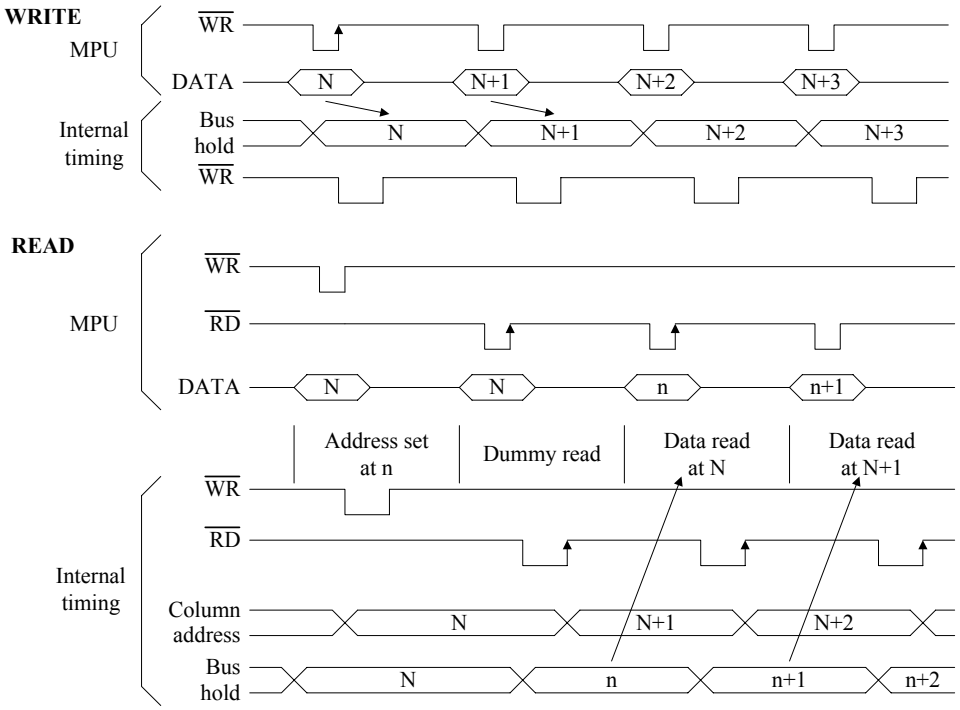


Figure 1 Bus Buffer Delay

Busy flag

When the Busy flag is logical 1, the NT7450B series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and therefore, the MPU processing capacity can greatly be enhanced.

Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command.

The contents of the display start line register are copied into the line count register at the start of every frame that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

Column Address Counter

The column address counter is a 7-bit preset table counter that supplies the column address for MPU access to the display data RAM. See figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

Page Register

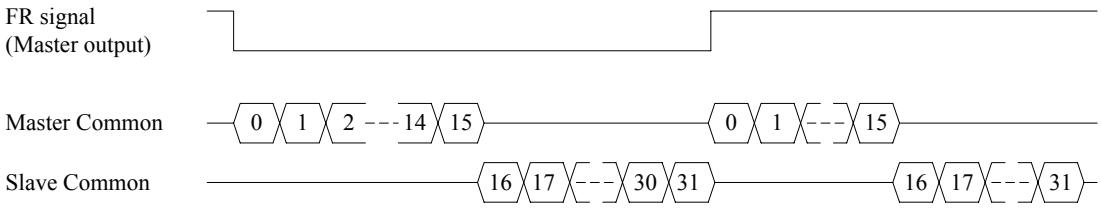
The page resister is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/16 or 1/32 duty (forNT7450B) can be selected by the Duty Select command. If the 1/32 duty is selected for the NT7450B, the 1/32 duty is provided by two chips, COM1~16 by the master and COM17~32 by the slave chips in the common



multi-chip mode.

Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands.

LCD Driver Circuit

The LCD driver circuitry generates the 80-4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

Display Timing Generator

This circuit generates the internal display- timing signal using the basic clock, CL, and the frame signals, FR.

FR is used to generate the dual frame AC-drive wave-from (type B drive) and to lock the line counter and common timing generator to the system frame rate.

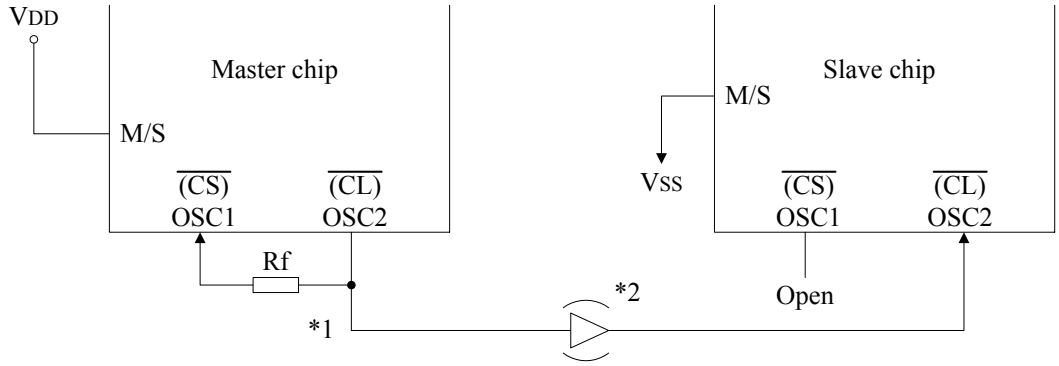
CL is used to lock the line counter to the system line scan rate. If a system uses both NT7450Bs and NT7451s they must have the same CL frequency rating.

Oscillator Circuit (NT7450B$_{OA}$)

A low power-consumption CR oscillator for adjusting the oscillation frequency is using Rf oscillation resistor only. This circuit generates a display timing signal. Some of NT7450B series models have a built-in oscillator and others use an external clock. This difference must be checked before use.

Connect the Rf oscillation resistor as follows. To suppress the built-in oscillator circuit and drive the MPU using an external clock, the clock having the same phase as the OSC2 of mater chip into OSC2 of the slave chip.

MPU having a built-in oscillator



*1 If the parasitic capacitance of this section increases, the oscillation frequency may shift to the lower frequency. Therefore, the Rf oscillation frequency must be reduced below the specified level.

*2 A CMOS buffer is required if the oscillation circuit is connected to two or more slave chips.

Reset Circuit

Detects a rising or falling edge of a $\overline{RES}$ input and initializes the MPU during power-on.

- Initialization status

  Display is off.

  Display start line register is set to line 1.

  Static drive is turned off.

  Column address counter is set to address 0.

  Page address register is set to page 3.

  1/32 duty NT7450B is selected.

  Forward ADC is selected (ADC command D0 is 0 and ADC status flag is 1).

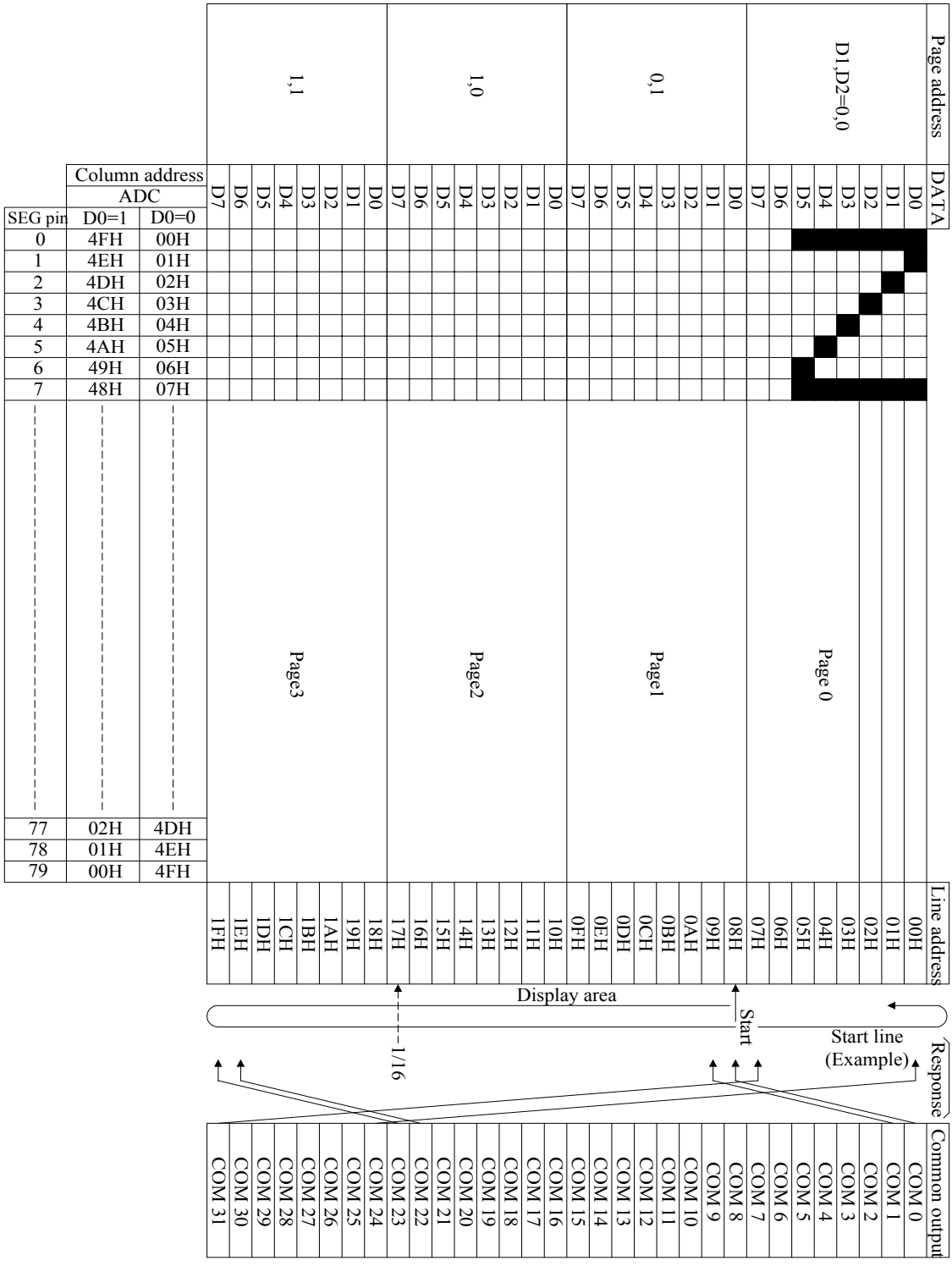
  Read-modify-write is turned off.

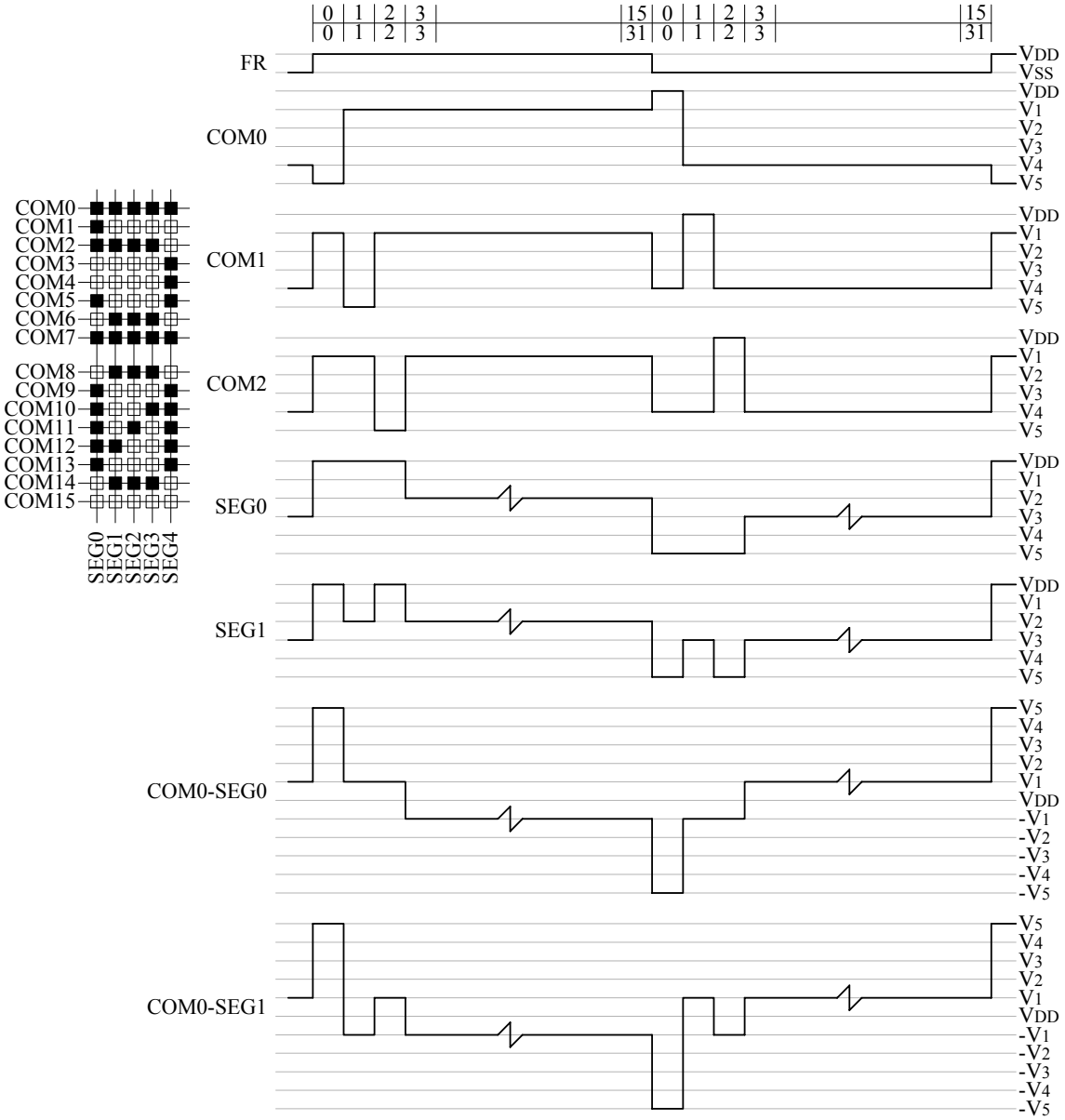
The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.

As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.

If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur. When the Reset command id issued, initialization.

Figure 2 Display Data RAM Addressung





COMMANDS

Summary

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display On/Off	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
Display start line	0	1	0	1	1	0	Display start address (0 to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
Set column (Segment) address	0	1	0	0	Column address (0 to 79)							Sets Display RAM column address in column address register.
Read status	0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output NO/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0:CW output, 1:CCW output
Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1:Static drive, 0:Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD duty cycle 1:1/32, 0:1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The NT7450B series identifies a data bus using a combination of A0 and R/$\overline{W}$ ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

Display ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 2 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H, DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		.			.
		.			.
		.			.
		.			.
1	1	1	1	1	31

See Figure 2.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H, BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80 and the page address is not changed continuously.

A0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			.				.
			.				.
			.				.
			.				.
1	1	1	1	1	1	1	79

Read Status

A0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Busy	ADC	On/ Off	Reset	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

• The busy bit indicates whether the driver will accept a command or not.

Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.

Busy=0: The driver will accept a new command.

• The ADC bit indicates the way column addresses are assigned to segment drivers.

ADC=1: Normal. Column address n → segment driver n.

ADC=0: Inverted. Column address 79-u → segment driver u.

• The ON/OFF bit indicates the current status of the display.

It is the inverse of the polarity of the display ON/OFF command.

ON/OFF=1: Display OFF

ON/OFF=0: Display ON

• The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operation mode.

RESET=1: Currently executing reset command.

RESET=0: Normal operation

Write Display Data

A0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Write 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page, address registers and then increments the column address register by one.

Read Display Data

A0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bit of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.

After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.

D=1: SEG0 ← column address 4FH, ...(Inverted)

D=0: SEG0 ← column address 00H, …(Normal)

This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.

D=1: Static drive on

D=0: Static drive off

Select Duty

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the NT7450B. It is invalid for the NT7451 whose performs passive operation. The duty cycle of the NT7451 is determined by the externally generated FR signal.

D=1: 1/32 duty cycle

D=0: 1/16 duty cycle

When using the NT7450BOA, (having a built-in oscillator) and the NT7451OA continuously, set the duty as follows:

NT7450BOA	NT7451OA
1/32	1/32
1/16	1/16

Read-Modify-Write

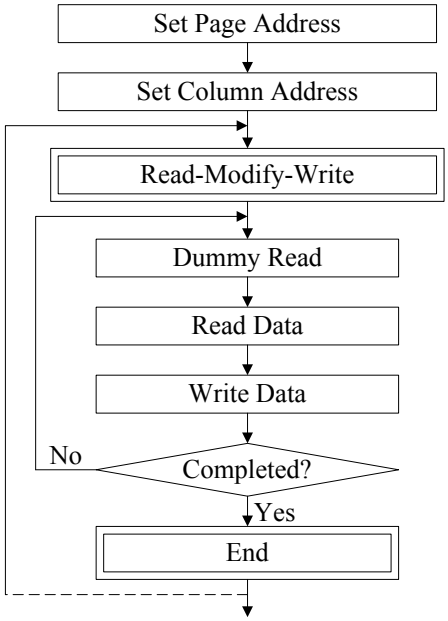
A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an End command is received.

Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This Function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

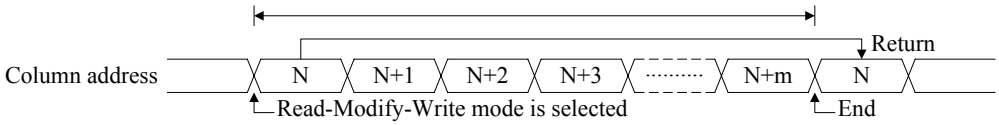
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to



their value prior to the receipt of the Read-Modify-Write command.

Reset

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears

- the display start line register.
- and set page address register to 3 page.

It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the RES pin. The Reset command cannot be used instead of this Reset signal.

Power Save (Combination command)

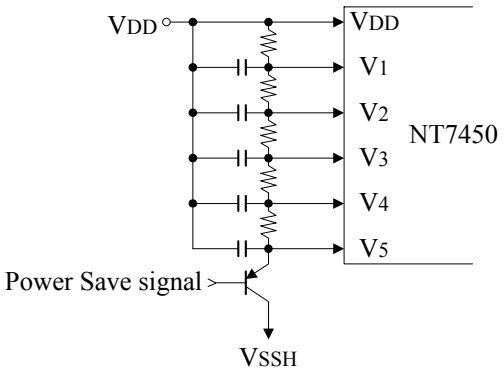
The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:

(a) The LCD drive is stopped, and the segment and common driver outputs are set to the VDD level.

(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.

(c) The display and operation modes are kept.

The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



If the LCD drive-power generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affected and reduce the power consumption using the divider resistor.

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage(1)	Vss	-8.0 to +0.3	V
Supply voltage(2)	V5	-16.5 to +0.3	V
Supply voltage(3)	V1,V4,V2,V3	V5 to +0.3	V
Input voltage	VIN	Vss-0.3 to +0.3	V
Output voltage	VO	Vss-0.3 to +0.3	V
Power dissipation	PD	250	mW
Operating temperature	Topr	-40 to +85	℃
Storage temperature	Tstg	-65 to +150	℃
Soldering temperature time at lead	Tsol	260, 10	℃, sec

Notes:
All voltages are specified relative to VDD=0V.
The following relation must be always hold
VDD≧V1≧V2≧V3≧V4≧V5
Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
The soldering process can reduce moisture resistance of flat packages, so care should be taken to avoid thermally stressing the package during board assembly.

Electrical Specifications

DC Characteristics

Ta=-20 to 75℃, VDD=0V unless stated otherwise

Parameter		Symbol	Condition		Rating			Unit	Applicable Pin
					Min.	Typ.	Max.		
Operating voltage (1) See note1. Recommended		VSS			-5.5	-	-2.7	V	VSS
Operating voltage (2)	Recommended	V5			-13.0	-	-3.5	V	V5 See note 10
	Allowable				-13.0	-	-		
	Allowable	V1, V2			0.6xV5	-	VDD	V	V1, V2
	Allowable	V3, V4			V5	-	0.4xV5		V3, V4
High-level input voltage		VIHT			VSS+2.0	-	VDD	V	See note 2 & 3
		VIHC			0.2x VSS	-	VDD		
		VIHT	VSS=-3V		0.2x VSS	-	VDD		See note 2 & 3
		VIHC	VSS=-3V		0.2x VSS	-	VDD		
Low-level input voltage		VILT			VSS		VSS+0.8		See note 2 & 3
		VILC			VSS		0.8xVSS		
		VILT	VSS=-3V		VSS		0.85xVSS		See note 2 & 3
		VILC	VSS=-3V		VSS		0.8xVSS		
High-level output voltage		VOHT	IOH=-3mA		VSS+2.4	-	-	V	OSC2 See note 4 & 5
		VOHC1	IOH=-2mA		VSS+2.4	-	-		
		VOHC2	IOH=-120 μA		0.2x VSS	-	-		
		VOHT	VSS=-3V	IOH=-2mA	0.2x VSS			V	OSC2 See note 4 & 5
		VOHC1	VSS=-3V	IOH=-2mA	0.2x VSS				
		VOHC2	VSS=-3V	IOH=-2mA	0.2x VSS				

DC Characteristics (Cont'd)

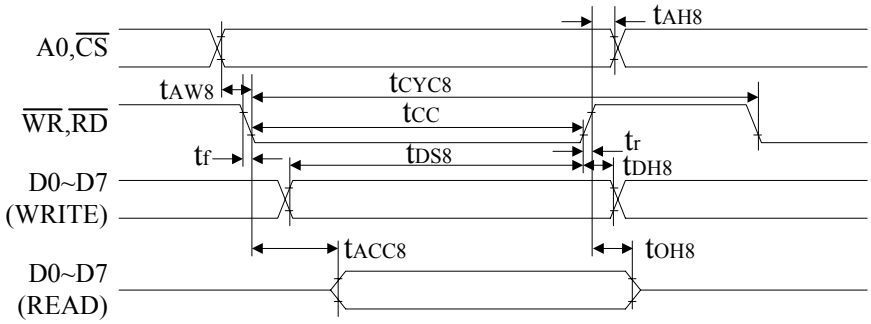
Ta=-20 to 75℃, VDD=0V unless stated otherwise

Parameter	Symbol	Condition		Rating			Unit	Applicable Pin
				Min.	Typ.	Max.		
Low-level output voltage	VOLT	IOL=3.0mA				VSS+0.4	V	OSC2 See note 4 & 5
	VOLC1	IOL=2.0mA				VSS+0.4		
	VOLC2	IOL=120μA				0.8xVSS		
	VOLT	VSS=-3V	IOH=-2mA			0.8xVSS	V	OSC2 See note 4 & 5
	VOLC1	VSS=-3V	IOH=-2mA			0.8xVSS		
	VOLC2	VSS=-3V	IOH=-2μA			0.8xVSS		
Input leakage current	ILI			-1.0		1.0	μA	See note 6
Output leakage current	ILO			-3.0		3.0	μA	See note 7
LCD drive ON resister	RON	Ta=25℃	V5=-5.0		5.0	7.5	KΩ	SEG0~79 COM0~15, See note 11
			V5=-3.5		10.0	50.0		
Static current dissipation	IDDQ	CS=$\overline{CL}$=VDD			0.05	1.0	μA	VDD
Dynamic current dissipation	IDD(1)	During display V5=-5.0V	fCL= 2KHz		2.0	5.0	μA	VDD See note 12 & 13 & 14
			Rf=1MΩ		9.5	15.0		
		During display V5=-5.0V VSS=-3V	fCL= 2KHz		1.5	4.5	μA	VDD See note 12 & 13
			Rf=1MΩ		6.0	12.0		
	IDD(2)	During access tcyc=200KHz			300	500	μA	See note 8
		VSS=-3V During access tcyc=200KHz			150	300		
Input pin capacitance	CIN	Ta=25℃, f=1MHz			5.0	8.0	pF	All input pins
Oscillation frequency	fOSC	Rf=1MΩ±2%, VSS=-5.0V		15	18	21	KHz	See note 9
		Rf=1MΩ±2%, VSS=-3.0V		11	16	21		
Reset time	tR			1.0			μs	$\overline{RES}$ See note 15

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E(or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/S and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL, M/S and $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V1,..., V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
12. NT7450B and NT7451 only. Does not include transient currents due to stray and panel capacitances.

13. NT7450B only. Does not include transient currents due to stray and panel capacitances.
14. NT7451 only. Does not include transient currents due to stray and panel capacitances.
15.tR (Rest time) represents the time from the $\overline{RES}$ signal edge to the completion of rest of the internal circuit. Therefore, the NT7450B series enters the normal operation status after this tR.

AC Characteristics



MPU Bus Read/Write I (80-Family MPU)

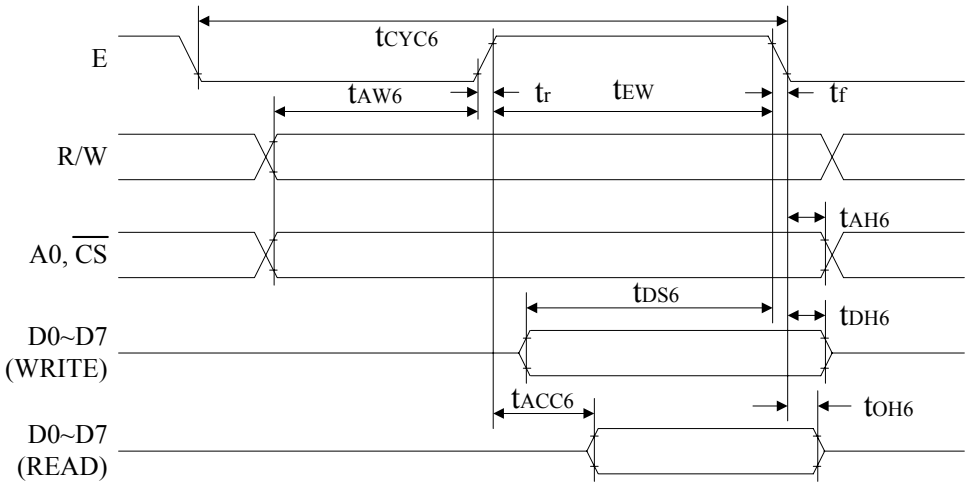
Ta=-20 to 75℃, Vss=-5.0V± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8		10	-	ns	A0, $\overline{CS}$
Address setup time	tAW8		20	-		
System cycle time	tCYC8		1000	-		$\overline{RD}$, $\overline{WR}$
Control pulse width	tcc		200	-		
Data setup time	tDS8		80	-		D0 to D7
Date hold time	tDH8		10	-		
RD access time	tACC8		-	90		
Output disable time	tOH8	CL=100pF	10	60		
Rise and fall time	tr, tf	-	-	15		-

Vss=-2.7 to -4.5V, Ta=-20 to +75℃

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8		20	-	ns	A0, $\overline{CS}$
Address setup time	tAW8		40	-		
System cycle time	tCYC8		2000	-		$\overline{RD}$, $\overline{WR}$
Control pulse width	tcc		400	-		
Data setup time	tDS8		160	-		D0 to D7
Date hold time	tDH8		20	-		
RD access time	tACC8		-	180		
Output disable time	tOH8	CL=100pF	20	120		
Rise and fall time	tr, tf	-	-	15		-

MPU Bus Read/Write II (68-Family MPU)



Ta=-20 to 75℃, Vss=-5.0V± 10% unless stated otherwise

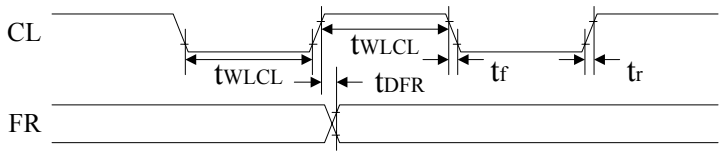
Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		tCYC6		1000	-	ns	A0,$\overline{CS}$,R/$\overline{W}$
Address setup time		tAW6		20	-		
Address hold time		tAH6		10	-		
Data setup time		tDS6		80	-		D0 to D7
Data hold time		tDH6		10	-		
Output disable time		tOH6	CL=100pF	10	60		
Access time		tACC6		-	90		
Enable Pulse Width	Read	tEW		100	-		E
	Write			80	-		
Rise and fall time		tr, tf	-	-	15		-

Vss=-2.7 to -4.5V, Ta=-20 to +75℃

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		tCYC6		2000	-	ns	A0,$\overline{CS}$,R/$\overline{W}$
Address setup time		tAW6		40	-		
Address hold time		tAH6		20	-		
Data setup time		tDS6		160	-		D0 to D7
Data hold time		tDH6		20	-		
Output disable time		tOH6	CL=100pF	20	120		
Access time		tACC6		-	180		
Enable Pulse Width	Read	tEW		200	-		E
	Write			160	-		
Rise and fall time		tr, tf	-	-	15		-

Notes: 1.tcyc6 is the cycle time of $\overline{CS}$. E=H, not the cycle time of E.

Display Control Signal Timing



Input

Ta=-20 to 75℃, Vss=-5.0V± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulse width	tWLCL		35	-	-	μs	CL
High-level pulse width	tWHCL		35	-	-	μs	
Rise time	tr		-	30	150	ns	
Fall time	tf		-	30	150	ns	
FR delay time	tDFR		-2.0	0.2	2.0	μs	FR

Vss=-2.7 to -4.5V, Ta=-20 to +75℃

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulse width	tWLCL		70	-	-	μs	CL
High-level pulse width	tWHCL		70	-	-	μs	
Rise time	tr		-	60	300	ns	
Fall time	tf		-	60	300	ns	
FR delay time	tDFR		-4.0	0.4	4.0	μs	FR

Note: The listed input tDFR applies to the NT7450B and NT7451 in slave mode.

Output

Ta=-20 to 75℃, Vss=-5.0V± 10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	tDFR	CL=100pF	-	0.2	0.4	μs	FR

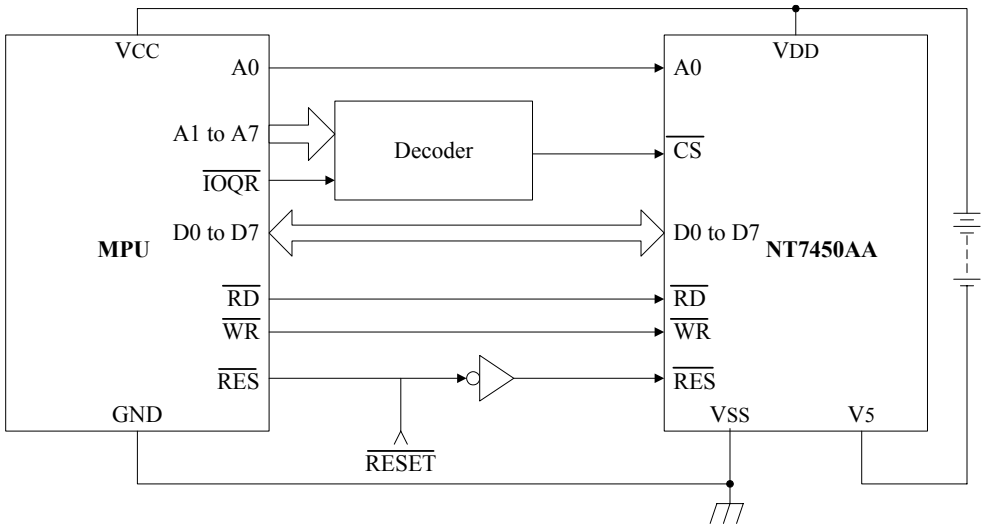
Vss=-2.7 to -4.5V, Ta=-20 to +75℃

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	tDFR	CL=100pF	-	0.4	0.8	μs	FR

APPLICATION NOTES

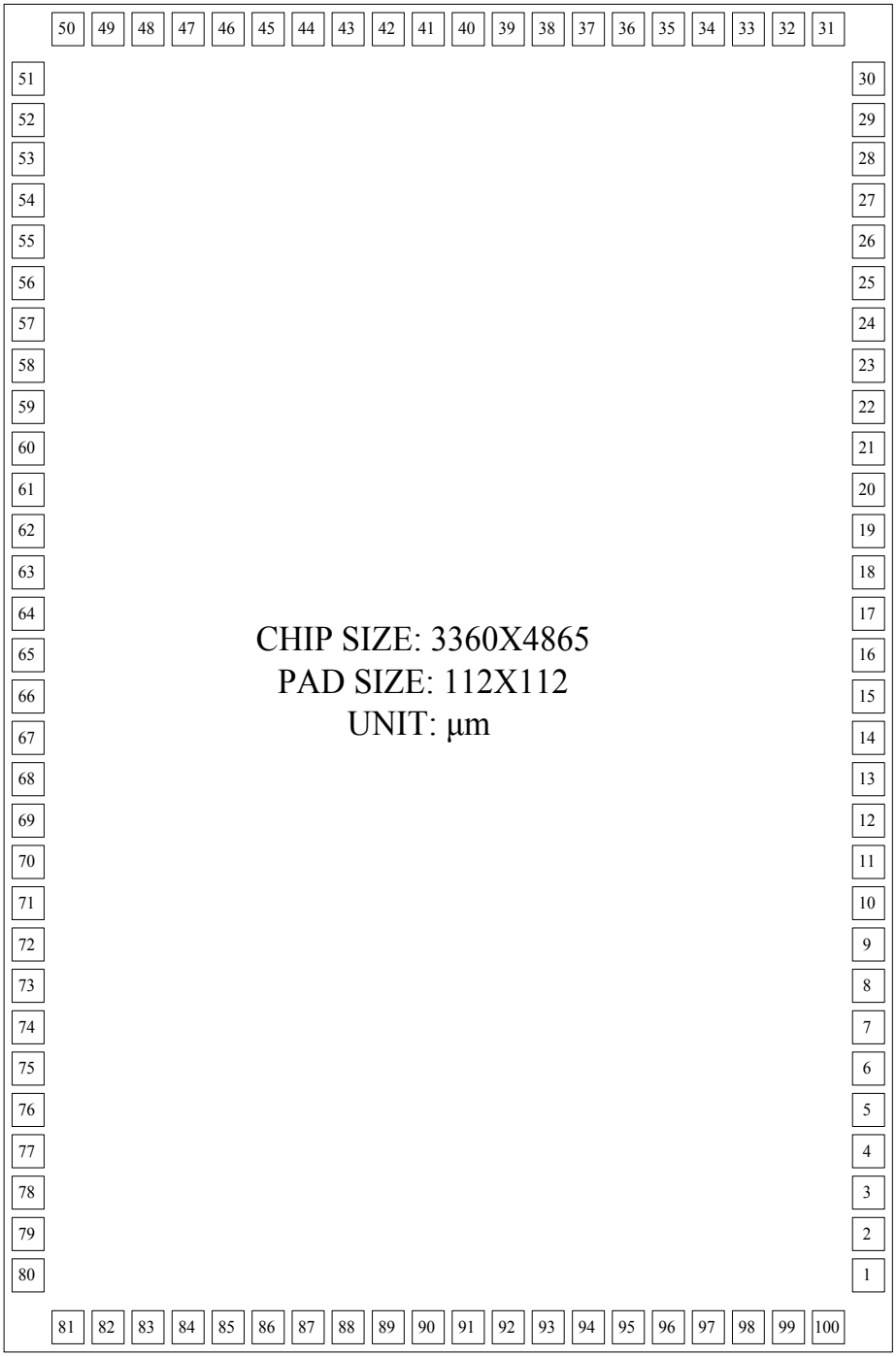
MPU Interface Configuration

80 Family MPU



PAD DIAGRAM

Note: Please connects the substrate to VDD or floating



PAD DIAGRAM (NT7450B)

Pad No.	Pad name	X	Y	Pad No.	Pad name	X	Y
1	COM5	3334	142	51	SEG21	540	3695
2	COM6	▲	258	52	SEG20	105	3649
3	COM7	|	383	53	SEG19	▲	3524
4	COM8	|	508	54	SEG18	|	3399
5	COM9	|	633	55	SEG17	|	3274
6	COM10	|	758	56	SEG16	|	3149
7	COM11	|	883	57	SEG15	|	3024
8	COM12	|	1008	58	SEG14	|	2899
9	COM13	|	1133	59	SEG13	|	2774
10	COM14	|	1258	60	SEG12	|	2649
11	COM15	|	1383	61	SEG11	|	2524
12	SEG60	|	1508	62	SEG10	|	2399
13	SEG59	|	1633	63	SEG9	|	2274
14	SEG58	|	1758	64	SEG8	|	2149
15	SEG57	|	1883	65	SEG7	|	2024
16	SEG56	|	2008	66	SEG6	|	1899
17	SEG55	|	2133	67	SEG5	|	1774
18	SEG54	|	2258	68	SEG4	|	1649
19	SEG53	|	2383	69	SEG3	|	1524
20	SEG52	|	2508	70	SEG2	|	1399
21	SEG51	|	2633	71	SEG1	|	1274
22	SEG50	|	2758	72	SEG0	|	1149
23	SEG49	|	2883	73	A0	|	1024
24	SEG48	|	3008	74	$\overline{CS}$	|	899
25	SEG47	|	3133	75	CL	|	774
26	SEG46	|	3258	76	E /RD	|	649
27	SEG45	|	3383	77	R/W/ (WR)	|	524
28	SEG44	|	3508	78	GND	|	399
29	SEG43	▼	3633	79	DB0	▼	274
30	SEG42	3165	3695	80	DB1		149
31	SEG41	3040	▲	81	DB2	308	105
32	SEG40	2915	|	82	DB3	440	▲
33	SEG39	2790	|	83	DB4	572	|
34	SEG38	2665	|	84	DB5	704	|
35	SEG37	2540	|	85	DB6	836	|
36	SEG36	2415	|	86	DB7	968	|
37	SEG35	2290	|	87	V_{CC}	1100	|
38	SEG34	2165	|	88	$\overline{RES}$	1232	|
39	SEG33	2040	|	89	FR	1364	|
40	SEG32	1915	|	90	V5	1496	|
41	SEG31	1790	|	91	V3	1628	|
42	SEG30	1665	|	92	V2	1760	|
43	SEG29	1540	|	93	M/S	1892	|
44	SEG28	1415	|	94	V4	2024	|
45	SEG27	1290	|	95	V1	2156	|
46	SEG26	1165	|	96	COM0	2288	|
47	SEG25	1040	|	97	COM1	2420	|
48	SEG24	915	|	98	COM2	2552	|
49	SEG23	790	|	99	COM3	2684	|
50	SEG22	665	▼	100	COM4	2816	▼