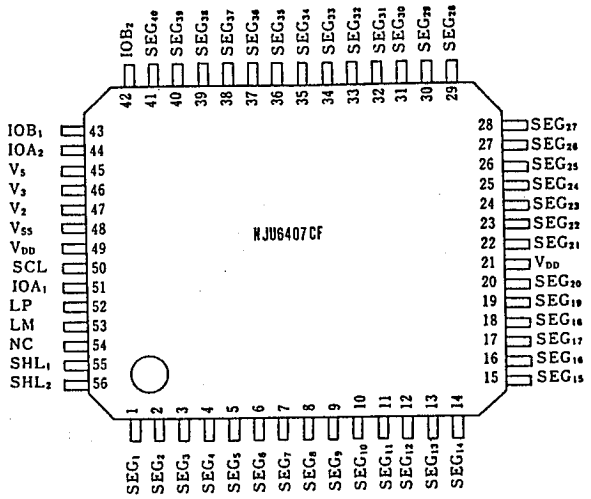
■ PIN CONFIGURATION



■ TERMINAL DESCRIPTION

No.	SYMBOL	F U N C T I O N
1～20 22～41	SEG_1～ SEG_{40}	LCD segment driving terminal. Each terminal corresponds to each bit of shift register
21, 49 48	V_{DD} V_{SS}	Power supply terminal (connect to the controller's V_{DD} terminal) Power supply terminal (connect to the controller's V_{SS} terminal)
42 43	IOB_2 IOB_1	Data input/output terminals for 21st to 40th bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL_2 terminal.
44 51	IOA_2 IOA_1	Data input/output terminals for 1st to 20th bits shift register. Display data is input (output) synchronized with clock pulse. Input or output is selected by SHL_1 terminal.
45, 46 47	V_5, V_3 V_2	LCD driving power source terminals. $V_{DD} \geqq V_2 \geqq V_3 \geqq V_5$
50	SCL	Shift register clock pulse input terminal. The data is shifted in the shift register by the falling edge of the clock pulse. A data setup time and hold time are required between data input and SCL. Clock pulse rising time (T_{RS}) and falling time (T_{FS}) should be set less than 50ns respectively.
52	LP	Latch pulse input terminal. The data in the shift register is latched to the Latch by this signal. "H" : Data writing, "L" : Data latch
53	LM	Alternate signal input for LCD driving.
55	SHL_1	Shift direction and input/output control terminal(Pull-up R). "H" or Open : Shift direction is from 1st bit to 20th bit. "L" : Shift direction is from 20th bit to 1st bit.
56	SHL_2	Shift direction and input/output control terminal(Pull-up R). "H" or Open : Shift direction is from 21st bit to 40th bit. "L" : Shift direction is from 40th bit to 21st bit.
54	NC	Non connection.

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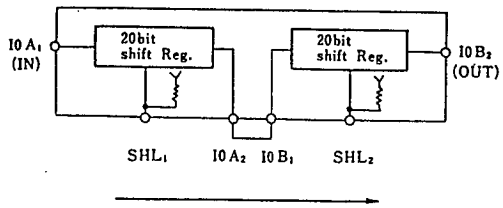
■ FUNCTIONAL DESCRIPTION

(1) Shift register control

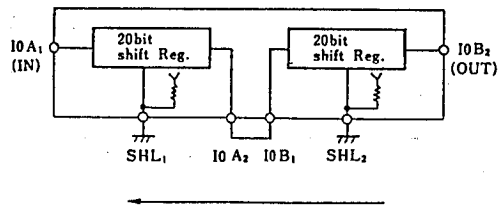
The 40-bit shift register is divided into two of 20-bit shift register.
The shift direction of each 20-bit shift register can be set independently to each other shown in below.

Control Terminal	Input	Shift Direction
SHL_1	"H" or Open	$IOA_1 \rightarrow IOA_2$
	"L"	$IOA_1 \leftarrow IOA_2$
SHL_2	"H" or Open	$IOB_1 \rightarrow IOB_2$
	"L"	$IOB_1 \leftarrow IOB_2$

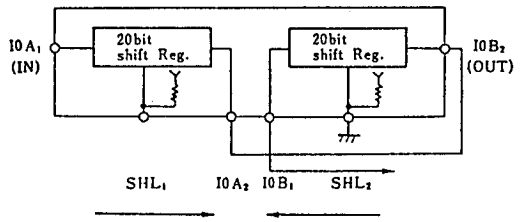
(1−1) When the terminals SHL_1 and SHL_2 are "H" or open, the data shift from SEG_1 to SEG_{40}.



(1−2) When the terminals SHL_1 and SHL_2 are "L", the data shift from SEG_{40} to SEG_1.



(1−3) Reversed sift direction to each other is also available.
$SEG_1 \rightarrow SEG_{20} \rightarrow SEG_{40} \rightarrow SEG_{21}$ example is shown in below:



(2) LCD driver output truth table.

Input Data	Selection/Non-selection	LM	Driver Output (SEG_1 to SEG_{40})
"H"	Selection	H	V_5
		L	V_{DD}
"L"	Non-selection	H	V_3
		L	V_2

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0	V
Supply Voltage (2) Note 1)	V_{DD} ~ V_5	V_{DD}-13.5 ~ V_{DD}+0.3	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD}+0.3	V
Operating Temperature	Topr	- 30 ~ + 80	℃
Storage Temperature	Tstg	- 55 ~ + 150	℃

Note 1) The relation : $V_{DD} \geqq V_2 \geqq V_3 \geqq V_5$ must be maintained.

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■ ELECTRICAL CHARACTERISTICS

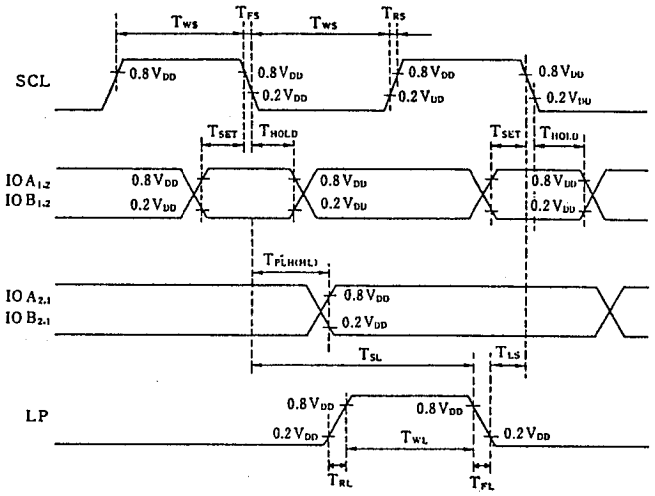
• DC Characteristics

(V_{DD}=5V±10% , Ta=-20 ~ +75℃)

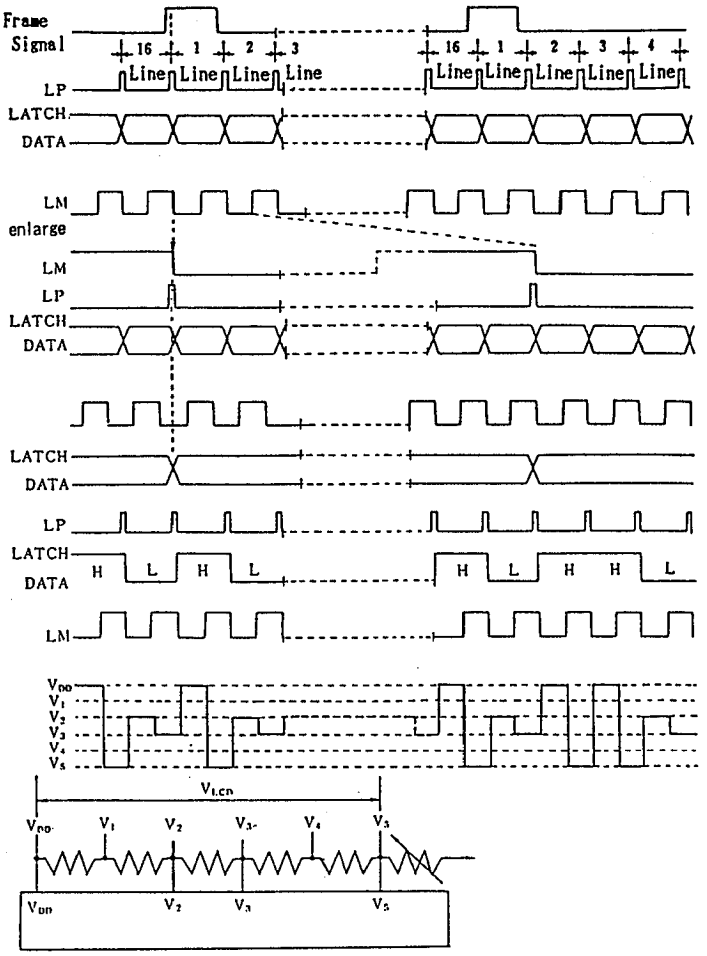
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage	V_{IH}	LM, LP, SHL_1, SHL_2 Terminals		0.8V_{DD}		V_{DD}	V
	V_{IL}					0.2V_{DD}	
Input Current	I_{IH1}	V_{IH}=V_{DD}	LM, LP Terminals			1	uA
	I_{IL1}	V_{IL}=0V				- 1	
	I_{IH2}	V_{IH}=V_{DD}	SHL_1, SHL_2 Terminals			1	
	I_{IL2}	V_{IL}=0V		- 10	- 15	- 25	
Output Voltage	V_{OH}	I_O=- 40uA	IOA_1, IOA_2, IOB_1, IOB_2 Terminals	4.2			V
	V_{OL}	I_O= 400uA				0.4	
Driver On-resistance	R_{ON}	Id=0.05mA	SEG_1 ~ SEG_{40} Terminals			30	kΩ
Operating Current	I_{DD}	SCL=1.5MHz, LM,LP=130us cycle No Load			0.6	1.0	mA
LCD Driving Voltage	V_{LCD}	V_{DD} - V_5		V_{DD}-3.0		V_{DD}-13.5	V

• AC Characteristics

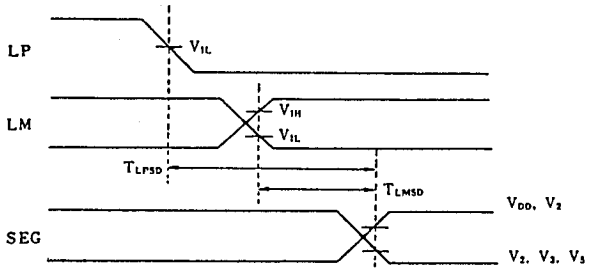
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	$T_{PLH(HL)}$				250	ns
Maximum Operating Frequency	f_{SCL}	Duty = 50 %	3.3			MHz
SCL Pulse Width	T_{WS}		125			ns
LP Pulse Width	T_{WL}		125			ns
Set up Time	T_{SET}		50			ns
SCL → LP Time	T_{SL}		250			ns
LP → SCL Time	T_{LS}		0			ns
Data Hold Time	T_{HOLD}		50			ns
SCL Rise, Fall Time	T_{RS}, T_{FS}				50	ns
LP Rise, Fall Time	T_{RL}, T_{FL}				1	us



■ TIMING CHART 1/5 Bias, 1/16 Duty Ratio



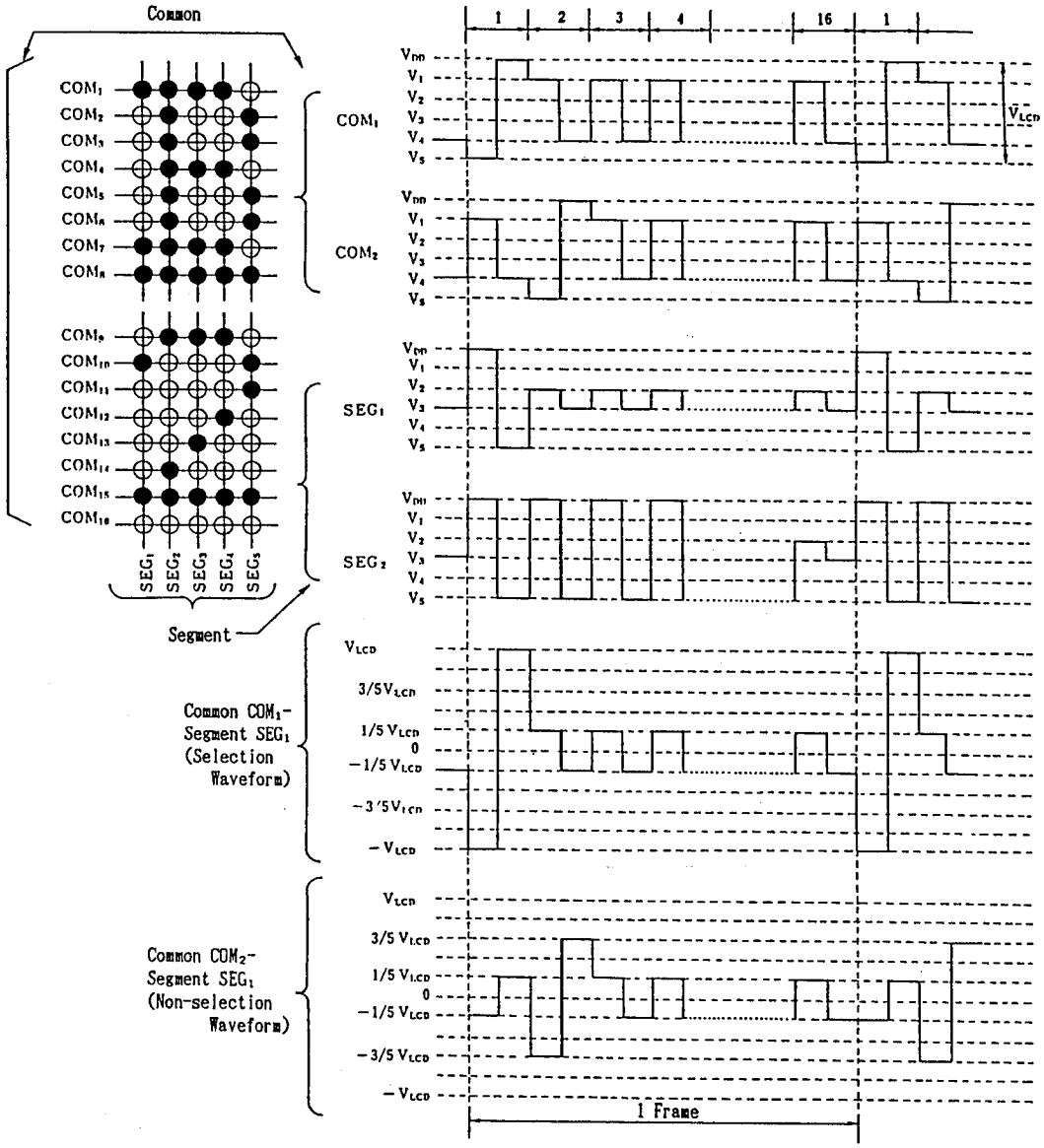
■ SEGMENT SIGNAL OUTPUT TIMING



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LP - SEG Output Delay Time	T_{LPSD}	C_L = 100pF			4.5	us
LM - SEG Output Delay Time	T_{LMSD}	C_L = 100pF			4.5	

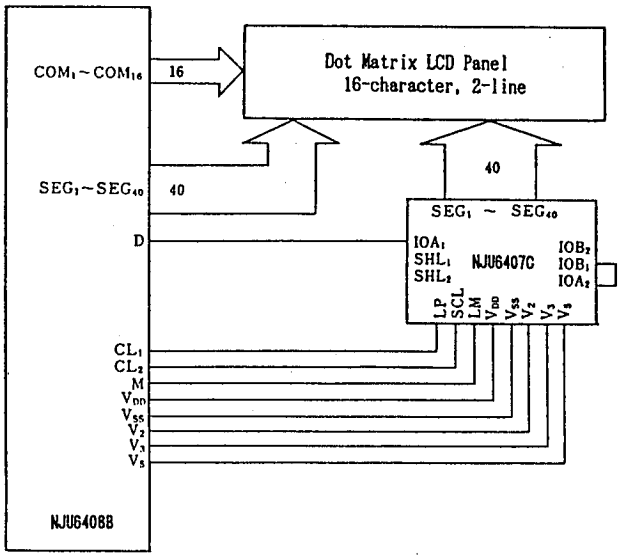
■ LCD DRIVING WAVEFORM EXAMPLE

1/5 Bias, 1/16 Duty Ratio

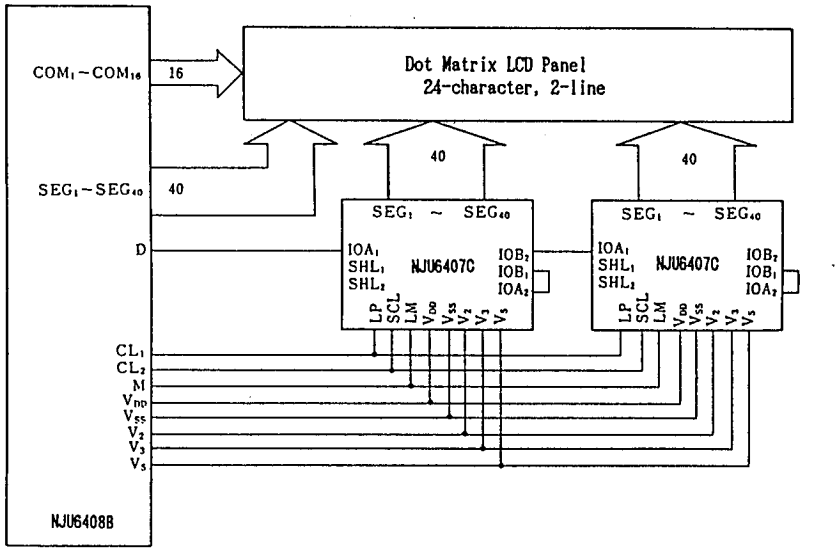


■ APPLICATION CIRCUITS

(1) 16-character 2-line Display Example (Combine with NJU6408B)



(2) 24-character 2-line Display Example (NJU6408B + NJU6407C x 2)



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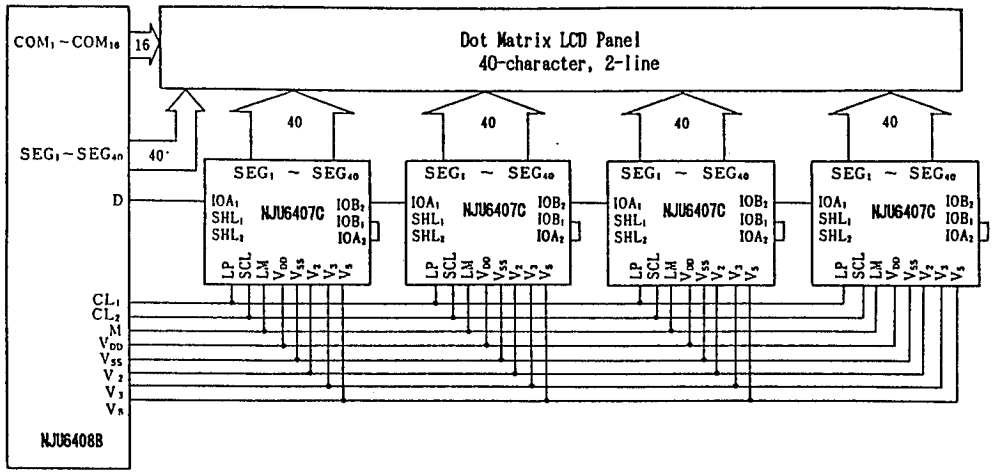
(3) 40-character 2-line Display Example (NJU6408B + NJU6407C x 4)



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MEMO