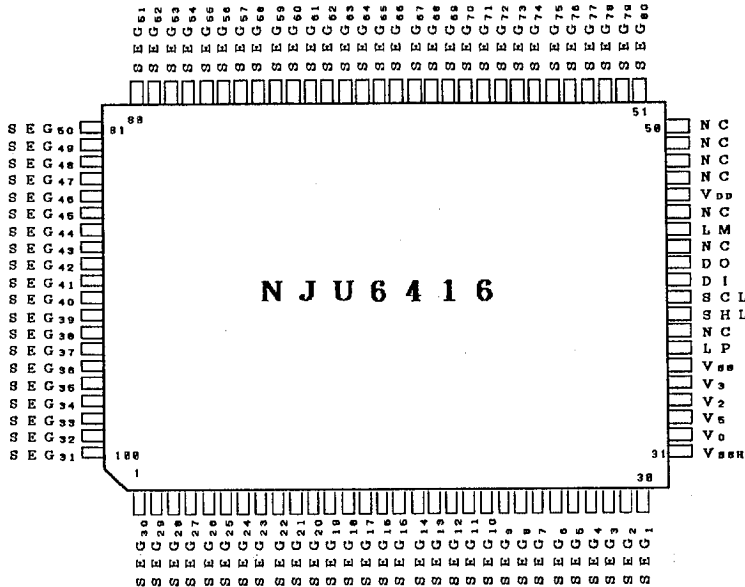




**■ PIN CONFIGURATION**

**■ TERMINAL DESCRIPTION**

NO.	SYMBOL	F U N C T I O N
1~30 51~100	SEG <sub>1</sub> ~ SEG <sub>80</sub>	LCD segment driving terminal. Each terminal corresponds to each bit of shift register
41	DI	Data input terminal. The DI terminal is fixed the input terminal regardless the shift direction. Display data is input synchronized with the clock signal.
42	DO	Data output terminal. The DO terminal is fixed the output terminal regardless the shift direction. The data is output synchronized with the clock signal.
40	SCL	Shift register clock pulse input terminal. The data is shifted in the shift register by the falling edge of the clock pulse. A data setup time and hold time are required between data input and SCL. Clock pulse rising time and falling time should be set less than 50ns(MAX) respectively.
39	SHL	Shift direction select terminal. "H": Shift direction is from 80th bit to 1st bit. "L": Shift direction is from 1st bit to 80th bit. The DI and DO terminals are fixed input and output terminal respectively regardless this terminal input level.
37	LP	Latch pulse input terminal. The data in the shift register is latched to the Latch by this signal. "H": Data writing, "L": Data latch
44	LM	Alternate signal input for LCD driving.
46 36	V <sub>DD</sub> V <sub>SS</sub>	Power supply terminal (connect to the controller's V <sub>DD</sub> terminal) Power supply terminal (connect to the controller's V <sub>SS</sub> terminal)
32,34,35,33 31	V <sub>0</sub> ,V <sub>2</sub> ,V <sub>3</sub> ,V <sub>5</sub> V <sub>SSH</sub>	LCD driving power source terminals. V <sub>DD</sub> ≥ V <sub>0</sub> ≥ V <sub>2</sub> ≥ V <sub>3</sub> ≥ V <sub>5</sub> ≥ V <sub>SSH</sub>
38,43,45 47~50	NC	Non connection. (Normally open)

**FUNCTIONAL DESCRIPTION**

## (1) Shift register control

The 80-bit shift register is a bidirectional register.  
The shift direction of 80-bit bidirectional shift register is shown below:

Control Terminal	Input	Shift Direction
SHL	"H"	80 → 1
	"L"	1 ← 80

(Note) DI and DO terminals are fixed input and output terminal respectively regardless the SHL input level.

## (2) LCD driver output truth table

Input Data	Selection/Non-selection	LM	Driver Output (SEG <sub>1</sub> to SEG <sub>80</sub> )
"H"	Selection	H	V <sub>5</sub>
		L	V <sub>0</sub>
"L"	Non-selection	H	V <sub>3</sub>
		L	V <sub>2</sub>

**ABSOLUTE MAXIMUM RATINGS**

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V <sub>DD</sub>	- 0.3 ~ + 7.0	V
Supply Voltage (2) Note 1)	V <sub>DD</sub> ~ V <sub>S</sub>	V <sub>DD</sub> -13.5 ~ V <sub>DD</sub> +0.3	V
Input Voltage	V <sub>IN</sub>	- 0.3 ~ V <sub>DD</sub> +0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 150	°C

Note 1) The relation : V<sub>DD</sub> ≥ V<sub>0</sub> ≥ V<sub>2</sub> ≥ V<sub>3</sub> ≥ V<sub>5</sub> ≥ V<sub>SSH</sub> must be maintained.

**■ ELECTRICAL CHARACTERISTICS**

·DC Characteristics

 (  $V_{DD}=5V \pm 10\%$  ,  $T_a=-20 \sim +75^\circ C$  )

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Note1)	$V_{IH}$		$0.8V_{DD}$		$V_{DD}$	V
	$V_{IL}$				$0.2V_{DD}$	
Input Current Note1)	$I_{IH}$	$V_{IH} = V_{DD}$			1	$\mu A$
	$I_{IL}$	$V_{IL} = 0V$	-1			
Output Voltage Note2)	$V_{OH}$	$I_o = -40\mu A$	4.2			V
	$V_{OL}$	$I_o = 0.4mA$			0.4	
Driver On-resistance Note3)	$R_{ON}$	$I_d = 0.05mA$			5	$k\Omega$
Operating Current ( Logic Part )	$I_{SSO}$	LM,LP=130 $\mu s$ cycle, SCL=1.5MHz. Every one bit Inverted Data. No Load.		1.1	1.5	mA
Operating Current ( LCD Driver Part )	$I_{SSHO}$	LM,LP=130 $\mu s$ cycle, SCL=1.5MHz. Every one bit Inverted Data. No Load.		70	100	$\mu A$
LCD Driving Voltage	$V_{LCD}$	$V_{SSH}$ Terminal, $V_{DD}=5V$	$V_{DD}-3.0$		$V_{DD}-13.5$	V

Note 1) Apply to LM, LP, SCL, SHL and DI terminals.

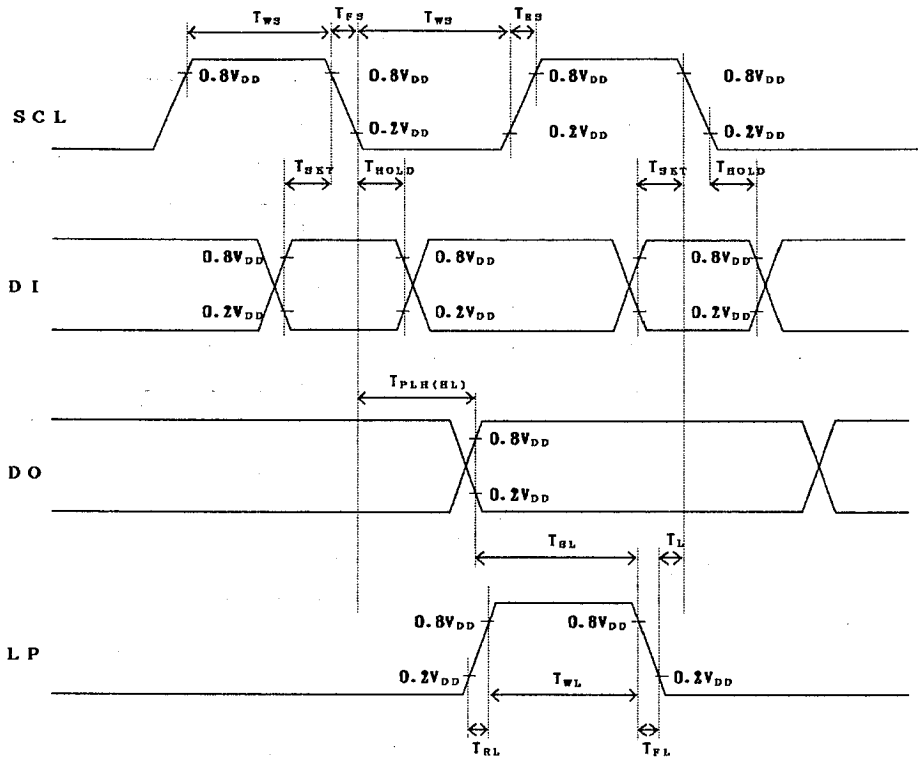
Note 2) Apply to DO terminal.

 Note 3) Apply to  $SEG_1 \sim SEG_{80}$  terminals.

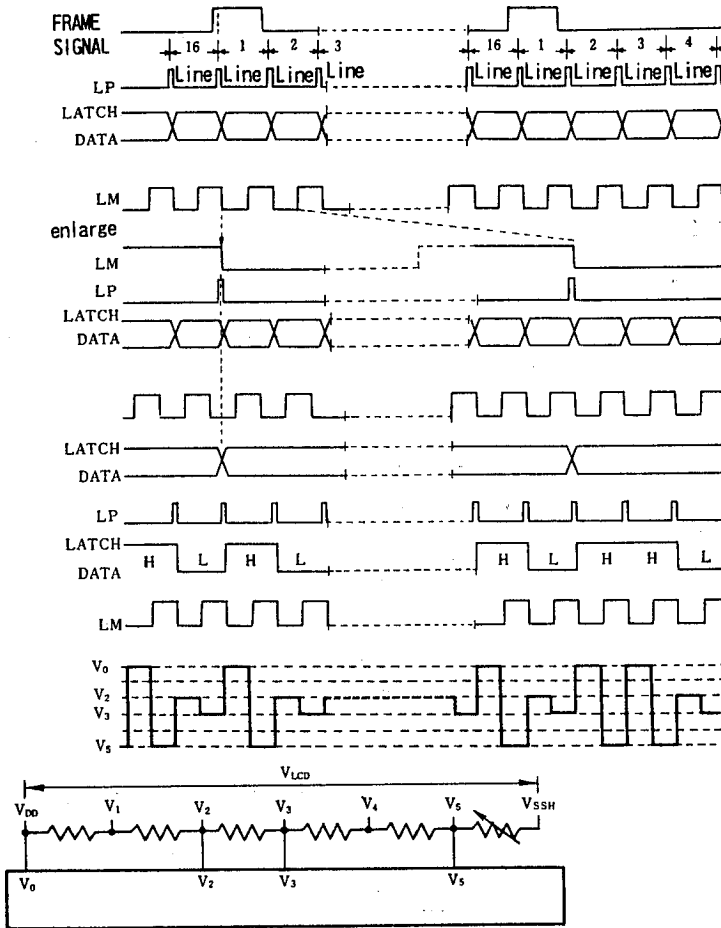
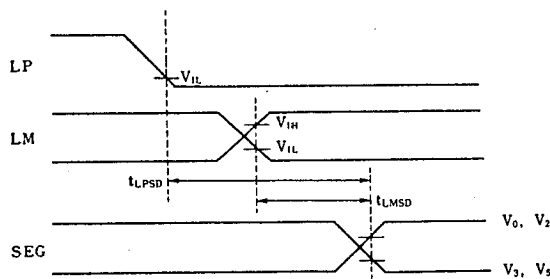
·AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	$T_{PLH(HL)}$				250	ns
Maximum Operating Frequency	$f_{SCL}$	Duty = 50 %	3.3			MHz
SCL Pulse Width	$T_{WS}$		125			ns
LP Pulse Width	$T_{WL}$		125			ns
Set up Time	$T_{SET}$		50			ns
SCL → LP Time	$T_{SL}$		250			ns
LP → SCL Time	$T_{LS}$		0			ns
Data Hold Time	$T_{HOLD}$		50			ns
SCL Rise, Fall Time	$T_{FS}, T_{RS}$				50	ns
LP Rise, Fall Time	$T_{FL}, T_{RL}$				1	$\mu s$

■ AC CHARACTERISTICS TIMING CHART



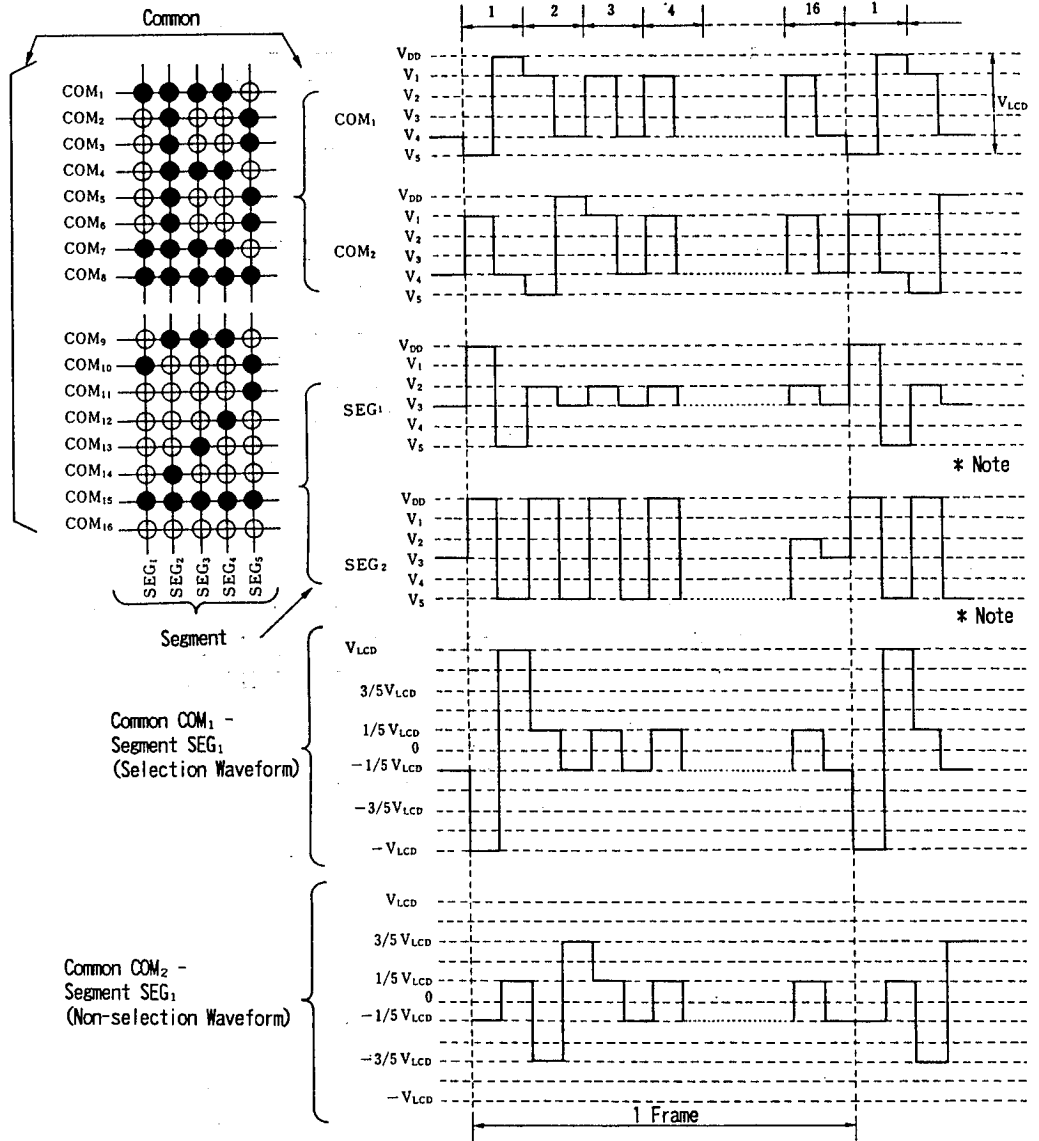
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**■ TIMING CHART**      1/5 Bias, 1/16 Duty Ratio

**■ SEGMENT SIGNAL OUTPUT TIMING**


PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LP - SEG Output Delay Time	T <sub>LP<sub>SD</sub></sub>	C <sub>L</sub> = 100pF			4.5	μS
LM - SEG Output Delay Time	T <sub>LM<sub>SD</sub></sub>	C <sub>L</sub> = 100pF			4.5	

■ LCD DRIVING WAVEFORM EXAMPLE

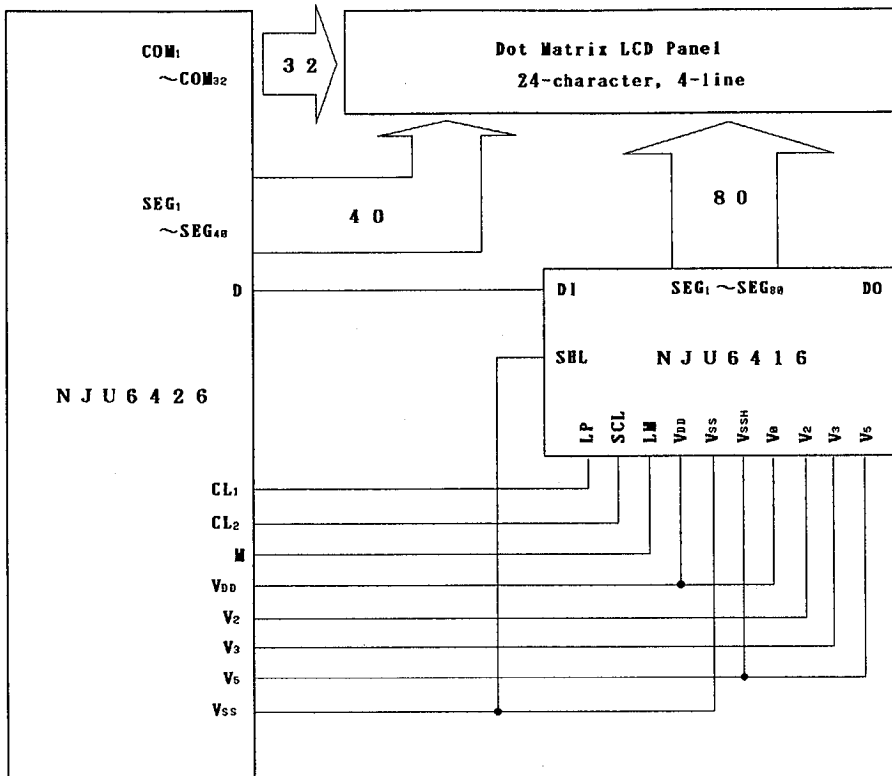
1/5 Bias, 1/16 Duty Ratio



\* Note : In case of V<sub>0</sub> terminal connected to the V<sub>DD</sub>.

■ APPLICATION CIRCUIT

24-character 4-line Display Example (NJU6426 + NJU6416)





## MEMO

[CAUTION]

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