PRELIMINARY

10COM x 65SEG 1/8, 1/9, 1/10 Duty BITMAP LCD DRIVER with KEY SCAN

■ GENERAL DESCRIPTION

The NJU6539 is a 10-common x 65-segment bitmap LCD driver to display graphics or characters.

The NJU6539 consists of a 650 bits display data RAM (DDRAM), the serial interface, the common and segment drivers, the key scan circuit, and several general output ports.

The display data via the serial interface is stored at the DDRAM first, and then is displayed on the LCD panel by the common and segment drivers.

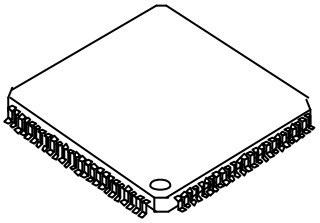
The NJU6539 can display a 10 x 65 dots graphic or 1-line by 11-character (5 x 7 dots per character)+ 3 x 65 icons.

The key scan circuit can transmit max.25 key data to MPU.

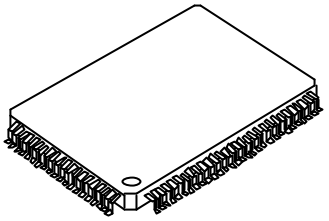
It also can provide as many as four general-purpose output ports for PWM signals to control LED or other devices.

Furthermore, the selectable LCD driving voltage out of 16 steps makes it easy to adjust the display contrast.

■ PACKAGE OUTLINE



NJU6539FG1



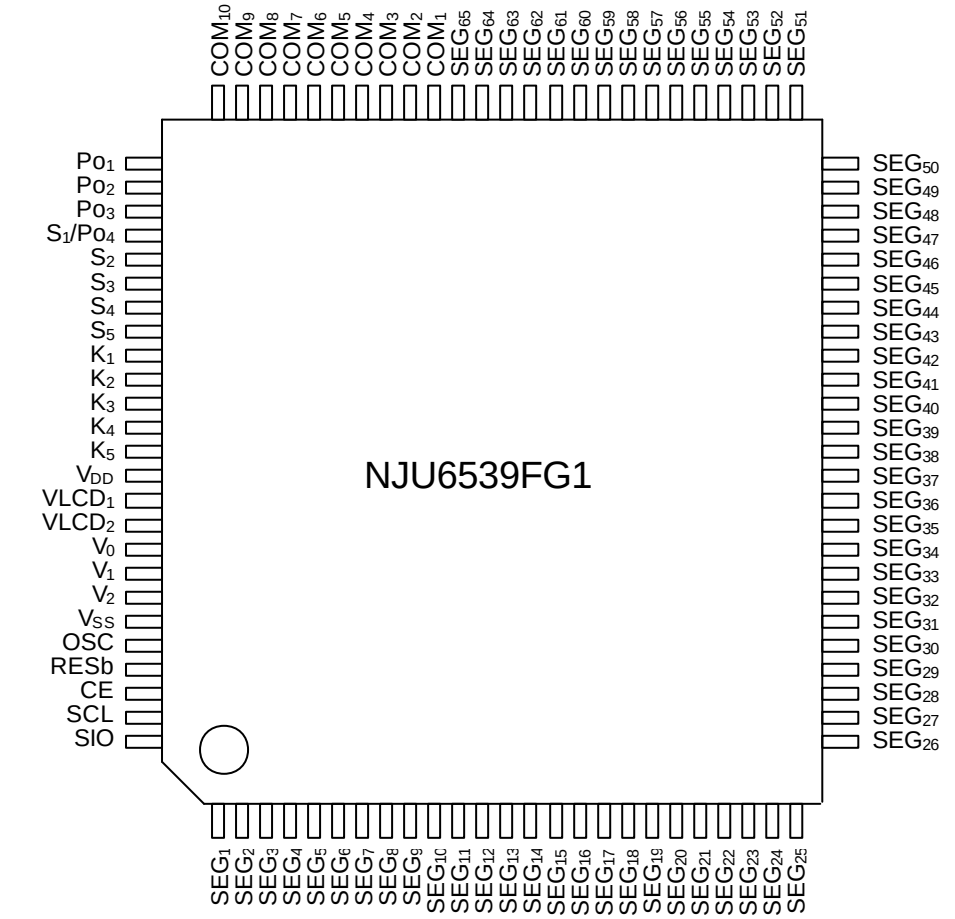
NJU6539FC2

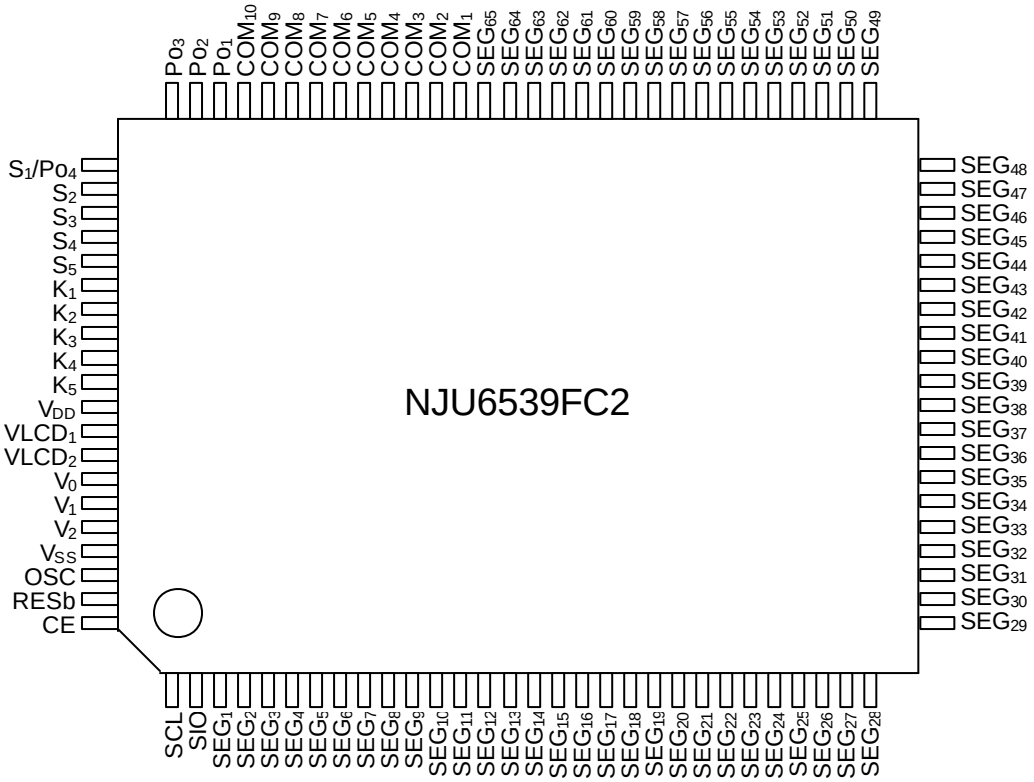
■ FEATURES

- Directly corresponding relationship between DDRAM data and LCD pixels
- DDRAM 650 bits
- LCD Drivers 65-seg, 10-com
- Serial interface SIO, SCL, CS
- Programmable Duty Ratio 1/8, 1/9, 1/10
- Bias Ratio 1/4
- 25 Key Scan 5 x 5 matrix (No need of anti-reverse current diodes)
- General Output Ports Max. 4 ports (The duty cycle variation of PWM is divided into128 steps)
- Program Function
- Brightness Correction
- Various Instructions
  Display ON/OFF, Page Address, Column Address, ADC Select, Display Inverse, All Pixel ON, Reset, EVR Register, Duty Selection, Power Save Mode, PWM Frequency/Po4 (S1), PWM Output Port, PWM Program/Port Mode, Slope/Stepping Time, PWM Program ON, Display Data Write.
- Built-in LCD driving bias voltage generation circuit
- Software for Contrast Control (16 steps)
- Operating Voltage
  - Logic Operating Voltage 2.7 to 5.5V
  - LCD Driving Voltage 5.0 to 10.0V
- Package QFP100-G1
  QFP100-C2
- C-MOS Technology Substrate: P

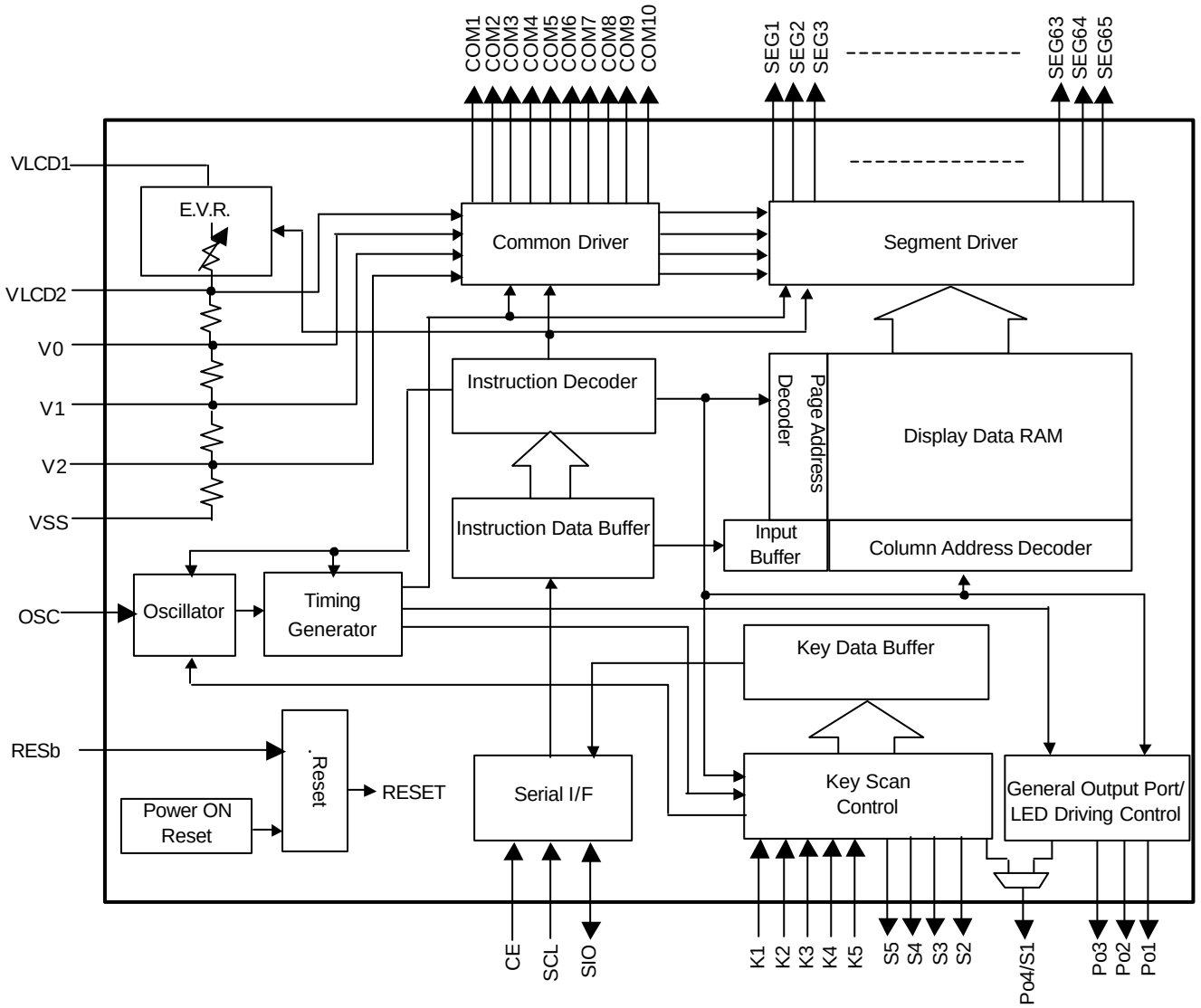
Contents

■ PIN CONFIGRATION





■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.		Symbol	I/O	Description
FG1	FC2			
1 to 65	3 to 67	SEG_1 to SEG_{65}	O	Segment output terminals.
66 to 72	68 to 74	COM_1 to COM_7	O	Common output terminals.
73 to 75	75 to 77	COM_8 to COM_{10}	O	Icon common output terminals.
76 to 78	78 to 80	Po1 to Po3	O	General output ports Output PWM signal. The duty cycle variation of PWM from 0% to 100% is divided into 128 steps
79	81	Po4/S_1	O	General output port / key scan output terminal Must be selected either as general output port or as key scan output port by the instruction Selected as general output port Key scan output terminals (No need for anti-reverse current diode in key scan circuit)
80 to 83	82 to 85	S_2 to S_5	O	Key scan output terminals. (No need for anti-reverse current diode in key scan)
84 to 88	86 to 90	K_1 to K_5	I	Key scan input terminals. (built-in pull-down resistor)
89	91	V_{DD}	-	Power supply terminal for logic circuit (2.7V to 5.5V)
90	92	VLCD1	I	Power supply terminal for LCD driving voltage.
91 92 93 94	93 94 94 96	VLCD2 V_0 V_1 V_2	I	LCD driving bias voltage terminals. Connect a capacitor between each terminal and Vss
95	97	V_{SS}	-	Ground terminal.
96	98	OSC	I/O	Oscillator terminal. Oscillation circuit is configured with an external resistor
97	99	RESb	I	Reset terminal. (The built-in internal pull-up resistor) If using Power-on Reset function, keep this pin open.
98	100	CE	I	Chip enable terminal
99	1	SCL	I	Serial clock input terminal
100	2	SIO	I/O	Serial Data input or output terminal

■ FUNCTIONAL DESCRIPTION

(1) Description of Each Block

(1-1) Serial Interface
Interface for serial data input/output. .

(1-2) Instruction Data Buffer
The instruction data is stored temporarily at this buffer.

(1-3) Instruction Decoder
The instruction data is decoded.

(1-4) Display Data RAM (DDRAM)
The DDRAM is used to store display data.

Table.1 Display data RAM (DDRAM) Map

Page address	Data	Display Pattern
D0="0"	D0	PAGE 0
	D1	
	D2	
	D3	
	D4	
	D5	
	D6	
D0="1"	D0	PAGE 1
	D1	
	D2	

Column Address	ADC											
		D0="0"	00	01	02	03	04	05	06	→	3F	40
		D0="1"	40	3F	3E	3D	3C	3B	3A	←	01	00
	Segment Drivers		1	2	3	4	5	6	7	- - - - - - - - - - - - - - - -	64	65

Common Drivers
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10

(1-5) Segment Driver
The Segment driver generates driving waveform to segment terminal in accordance with display data.

(1-6) Common Driver
The Common driver generates driving waveform to common terminal.

(1-7) Electrical Variable Resistor (E.V.R.)
The Electrical Variable Resistance is used to adjust LCD driving bias voltage V0~V2.

(1-8) Key Scan Controller
The key scan controller is used to control the input of the key scan data.

(1-9) Key Data Buffer
The buffer stores key scan data before reading out by CPU

(1-10) Oscillator
With the external resistor, the Oscillator generates the master clock.

(1-11) Reset Circuit
The Reset circuit uses voltage detecting function to reset the internal circuit whenever the power turns on or drops below a certain level voltage.

(1-12) General Output Port

PWM signals are outputted through these ports. The duty cycle variation of PWM signal from 0% to 100% is divided into 128 steps, but for LED driving control, the duty cycle variation is divided into 16 steps.

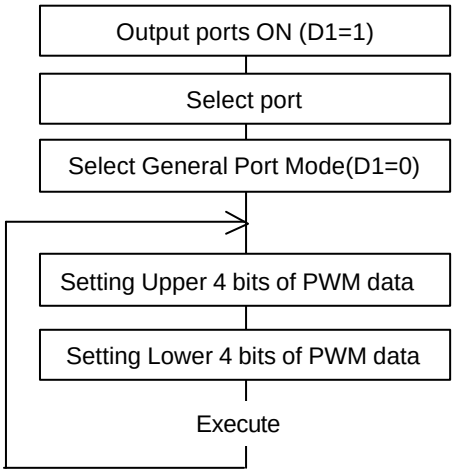
The different PWM value can be set to each port separately.

Either 128 steps or 16 steps PWM signal can be selected for output through setting (n) PWM Program/Port Mode.

General Port Mode

The duty cycle of PWM signal is selected from one of 128 steps.

PWM data for Po1~Po4 ports is set as below. First select output port through setting (m) PWM Output Port instruction, and then enable the General Port mode through setting (n) PWM Program/Port Mode, then set up the PWM data for the selected output port.

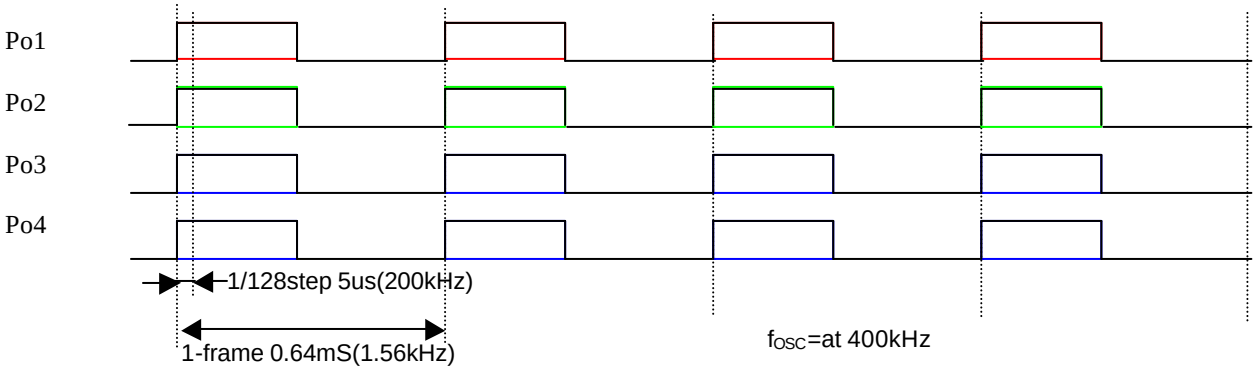


(a) Display ON/OFF Output Ports ON/OFF

(m) PWM Output Port

(n) PWM Program/Port Mode

The waveforms are like below (64/128 duty for all ports)



*If only output "H" or "L" signal, the following data can be input.

"L" PWM $_7$~PWM $_0$ "00000000" (0/128Duty)

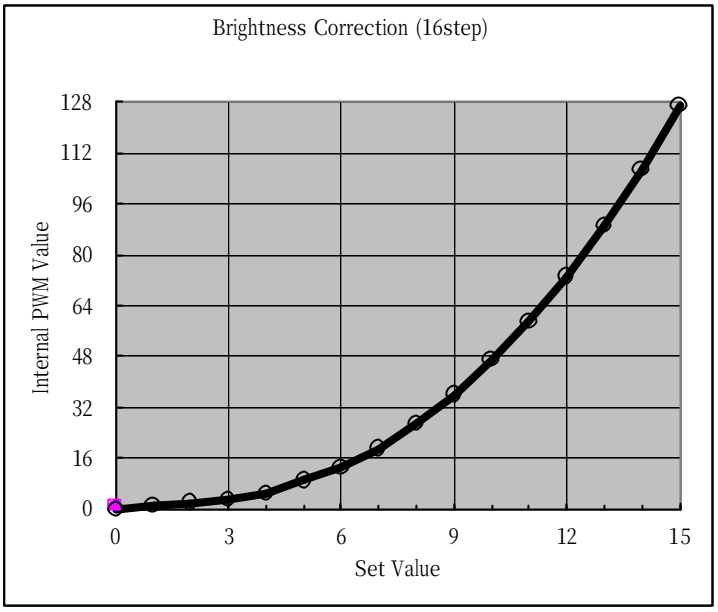
"H" PWM $_7$~PWM $_0$ "1*******" (128/128Duty) (*: Don't Care)

LED Port Mode

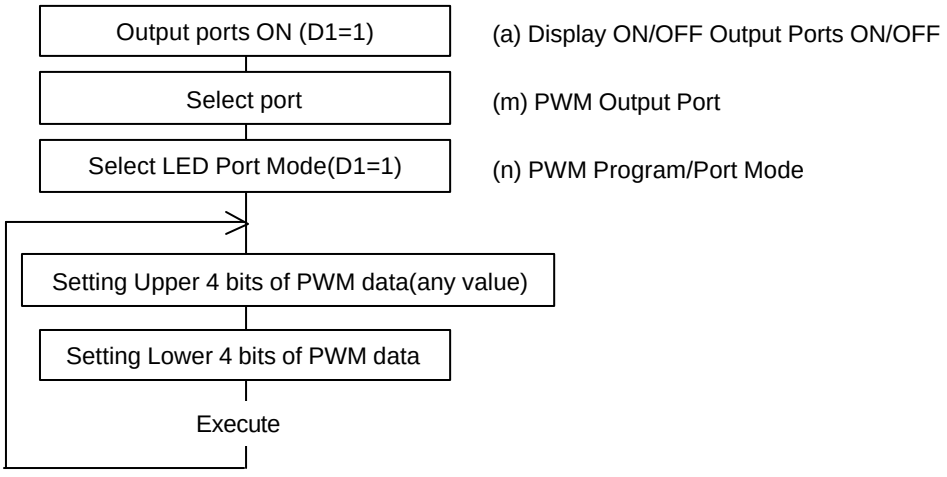
This mode is used for LED driving control. The sweep function and the brightness correction function (Gamma curve adjustment) are available. The duty cycle of PWM signal is selected from one of 16 steps.

Even if the change of the brightness of LED is linear, human eyes perceive a curve change. The built-in brightness correction function can rectify the difference between actual LED luminance and its appearance.

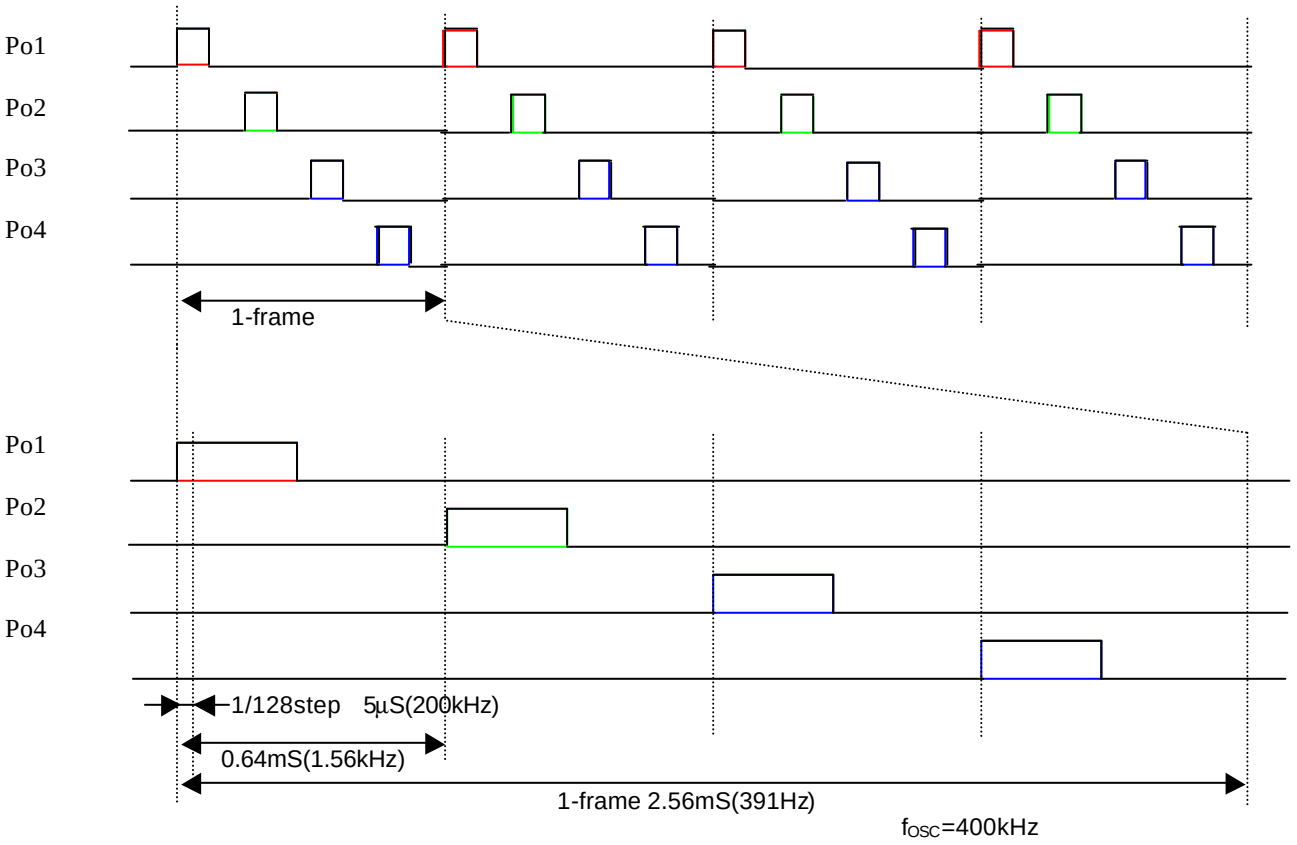
According to the following compensation curve, 16 steps are selected from 128 steps PWM. And the nonlinear luminance characteristic of LED is rectified so that it looks like linear on appearance.



PWM data for Po1~Po4 ports is set as below. First select output port through setting (m) PWM Output Port, and then enable the LED Port mode through setting (n) PWM Program/Port Mode, then setup the PWM data for the selected output port.



By staggering the output waveforms' phases, allowable dissipation of LED package can be reduced.
The LED brightness can be selected from 16 levels (0 to 15) for brightness correction.



Sweep Function

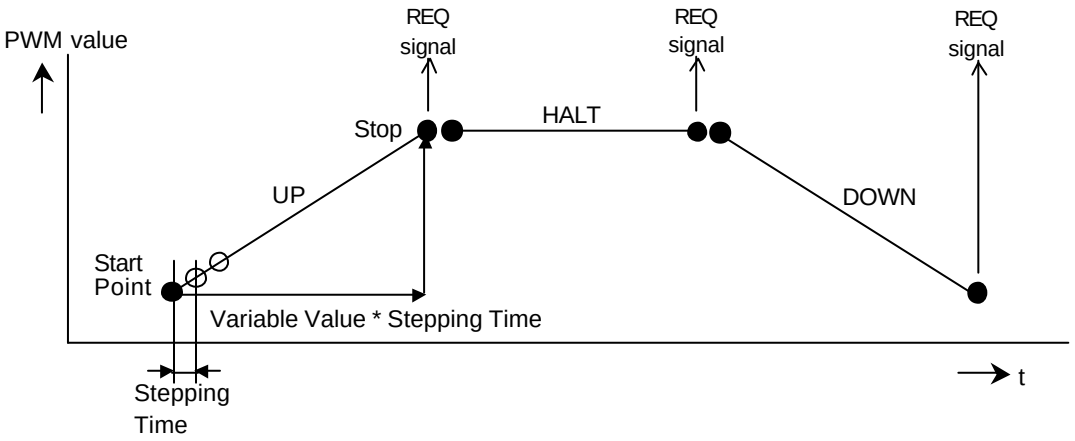
The Sweep Function allows a smooth color-change of a RGB LED.

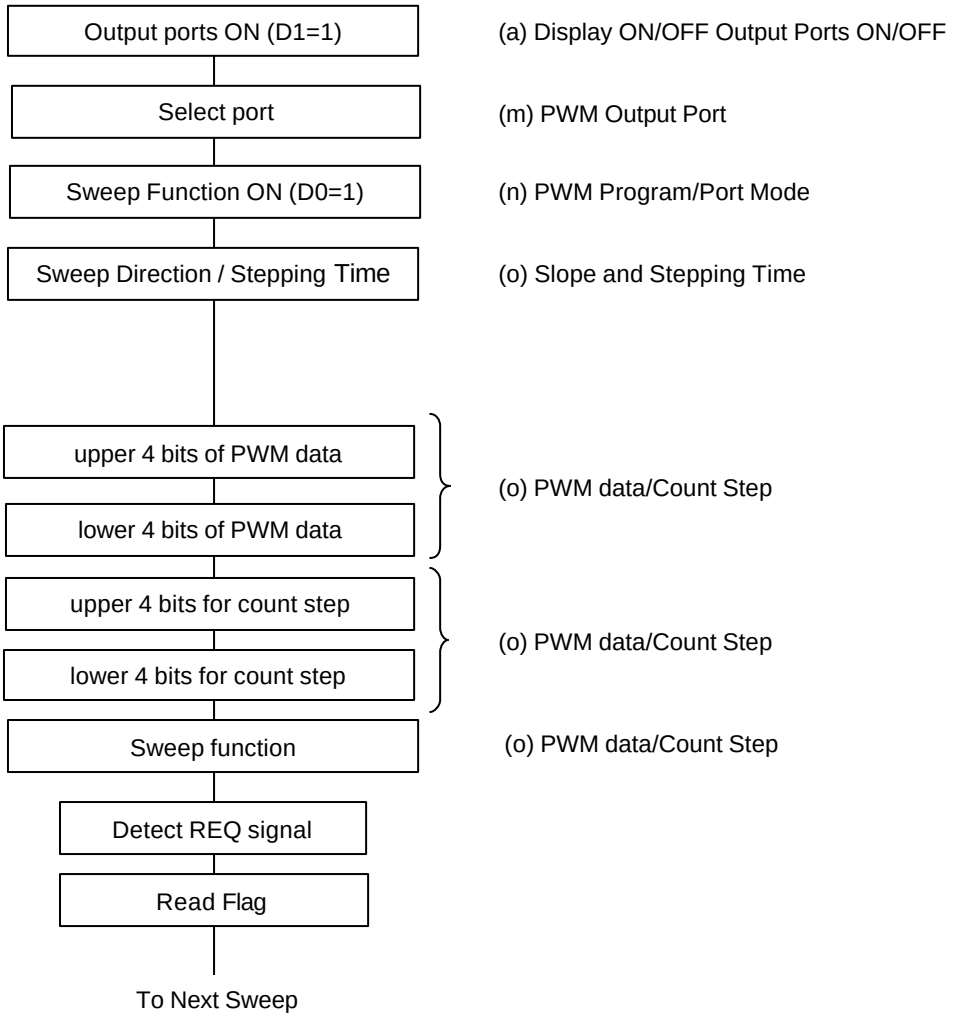
By setting up the initial value, count step, sweep direction and stepping time, adjusted PWM data can realize a smoothly color-changing.

Sweep function can be used for either the General Port Mode (max. 128 count) or the LED Mode (max.16 count).

At the end of the program, the NJU6539 will send request signal to CPU and the SIO pin is pulled to "L", the PWM value at the last count will be maintained and outputted.

Request signal is used as key scan request signal too.





(2) Instruction

The interface is a 3-wire serial interface. The serial data is transferred synchronously with SCL clock. And D_7-D_0 data is interrupted as instruction data or display data by A0. (For the details, refer to [data input timing]), The instruction table is shown as below, and D7 is the MSB.

Table 1. Instruction Code (*: Don't Care)

Instruction		Code									Description
		A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
(a)	Display ON/OFF Output ports ON/OFF	0	1	0	1	0	1	1	0/1	0/1	D_0=0: display OFF, D_0=1: display ON D_1=0: ports OFF, D_1=1: ports ON
(b)	Page address	0	1	0	1	1	0	0	0	0/1	D_0=0: PAGE 0, D_0=1: PAGE 1
(c)	Column address (Upper 3 bits)	0	0	0	0	1	*	Address			Set 3 bits data to the register.
	Column address (Lower 4 bits)	0	0	0	0	0	Address				Set 4 bits data to the register.
(d)	Display data write	1	*	Write data							Write the data to the DDRAM
(e)	ADC select	0	1	0	1	0	0	0	0	0/1	Reverse the column address D_0=0: Normal, D_0=1: Inverse
(f)	Display inverse	0	1	0	1	0	0	1	1	0/1	D_0=0: Normal, D_0=1: Inverse
(g)	All pixels ON	0	1	0	1	0	1	0	0	0/1	D_0=0: Normal, D_0=1: All pixel ON
(h)	Reset	0	1	1	1	0	0	0	1	0	Initialization
(i)	E.V.R. register	0	0	0	1	0	E.V.R. data				Set the Contrast control data (16 steps)
(j)	Duty select	0	0	0	1	1	0	Duty			Duty set (1/8,1/9,1/10) (D_2, D_1, D_0)=(0, 0, 0): 1/8Duty (D_2, D_1, D_0)=(0, 0, 1): 1/9 Duty (D_2, D_1, D_0)=(0, 1, 0): 1/10 Duty
(k)	Power save mode	0	0	1	0	0	0	0	Power save		Set the Power save mode (D_1, D_0)=(0,0): Normal (D_1, D_0)=(0,1): Power save 1 (D_1, D_0)=(1,0): Power save 2 (D_1, D_0)=(1,1): Power save 3
(l)	PWM frequency/Po4 (S1)	0	0	1	0	1	0	0	0/1	0/1	Set PWM frequency, and select pin 79 (NJU6539FC2: pin 81) as Po4 or S_1 D_0=0 fsys/128, D_0=1 fsys/256 D_1=0 Po4, D_1=1 S_1
(m)	PWM output port	0	0	1	1	0	0	0	Port		Select the output port (D_1, D_0)=(0,0): P_{O1}, (D_1, D_0)=(0,1): P_{O2}, (D_1, D_0)=(1,0): P_{O3}, (D_1, D_0)=(1,1): P_{O4}
(n)	PWM program/port mode	0	0	1	1	0	0	1	0/1	0/1	D_0=0 Sweep Function disable, D_0=1 Sweep Function Enable D_1=0 General Port mode D_1=1 LED Port mode
(o)	PWM data / count step	0	1	0	0	0	Upper 4 bits				Set the upper 4 bits to the register.
	PWM data / count step	0	0	1	1	1	Lower 4 bits				Set the Lower 4 bits to the register.
(p)	Slope and Stepping time	0	1	0	0	1	Slope		Stepping time		Set PWM data changing direction and changing speed when PWM program function is used.
(q)	PWM Program ON	0	1	1	0	0	0/1	0/1	0/1	0/1	D_0=1: P_{O1} Exec., D_1=1: P_{O2} Exec., D_2=1: P_{O3} Exec., D_3=1: P_{O4} Exec.
(r)	Testing	0	1	1	1	1	Test data				Do not use this instruction.

Instruction Description

(a) Display ON /OFF Output Port ON/OFF

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	1	1	D	D

D_0=0: All pixels off, the waveform from COM driver is not changed, but all SEG drivers output V_1
D_0=1: Display on
D_1=0: All ports output "L" regardless of PWM data.
D_1=1: General output ports can output PWM signal.

(b) Page Address

The page address is set up before writing display data to the DDRAM
Page 0: RAM area for display data, D_0-D_6 valid.
Page 1: RAM area for icon data, D_0 -D_2 valid.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	1	0	0	0	A_0

A_0	Page
0	0
1	1

(c) Column Address

The column address is set up before data writing. The address will be valid after both upper 3-bit and lower 4-bit data are set into the column address register.

Once the column address is setup, it will automatically increase (+1) whenever the DDRAM is accessed, so the DDRAM can be continuously accessed without "column address" instruction.

The column address will stop increment and the page address will not change when the last address $(41)_H$ is accessed.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	0	1	*	A_6	A_5	A_4	Upper 4-bit
0	0	0	0	0	A_3	A_2	A_1	A_0	Lower 4-bit

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column address (HEX)
0	0	0	0	0	0	0	00
0	0	0	0	0	0	1	01
:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	40

(d) Display Data Write

This instruction let display data writing into the selected column address on the DDRAM.

The column address automatically increases (+1) whenever the display data is written, so the display data can be continuously written without "column address" instruction.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	*	Write data						

*: Do not care

(e) ADC Select

This instruction reverses the column address. The correspondence relationship between the column address and segment driver is shown in Table 1.

The segment driver output order is inversed. This instruction can reduce the placement limits of IC assembly.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	0	0	D

D 0: Clockwise output (Normal) $S_1 \rightarrow S_{65}$

1: Counterclockwise output (Inverse) $S_{65} \rightarrow S_1$

(f) Display Inverse

If D=0, without changing the data on DDRAM, the status of all the pixels will be inversed.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"

1: Inverse RAM data "0" correspond to "On"

(g) All Pixels ON

This instruction turns on the entire LCD pixels regardless of the contents of the DDRAM. It doesn't change the contents of DDRAM. This instruction has priority over the "Display Inverse" Instruction.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	0	0	1	0	D

D 0: Normal Display

1: All pixels ON

(h) Reset

This instruction resets the LSI to the following status, however it doesn't change the contents of the DDRAM. Because it is different from hardware reset, please execute Power On Reset or Hardware Reset when switch on.

After reset:

1. Page address: (0) page
2. Column address: $(00)_H$
3. EVR register: D_3, D_2, D_1, D_0 = "1, 1, 1, 1"
4. Duty select: 1/10 Duty
5. P_{O4}/S_1 terminal. P_{O4}
6. PWM frequency: fsys/128
7. PWM output port: P_{o1}
8. Sweep Function disable, General Port mode
9. Set upper 4 bit of (o) instruction D_3, D_2, D_1, D_0 = "0,0,0,0"
10. Set lower 4 bits of (o) instruction D_3, D_2, D_1, D_0 = "0,0,0,0"
11. Set (p) instruction D_3, D_2, D_1, D_0 = "0, 0, 0, 0"
12. Set (q) instruction D_3, D_2, D_1, D_0 = "0, 0, 0, 0"

The data on DDRAM is not affected by the initialization.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	0	0	0	1	0

(i) EVR Register

Through E.V.R. register, the LCD driving voltage V_{LCD} can be selected out of 16 levels. Set the binary code "0000" when contrast adjustment is unused.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	0	E.V.R. data			

D_3	D_2	D_1	D_0	V_{LCD2} terminal level (Typical)
0	0	0	0	V_{LCD1}
0	0	0	1	$0.968V_{LCD1}$
0	0	1	0	$0.937V_{LCD1}$
0	0	1	1	$0.909V_{LCD1}$
0	1	0	0	$0.882V_{LCD1}$
0	1	0	1	$0.857V_{LCD1}$
0	1	1	0	$0.833V_{LCD1}$
0	1	1	1	$0.811V_{LCD1}$
1	0	0	0	$0.789V_{LCD1}$
1	0	0	1	$0.769V_{LCD1}$
1	0	1	0	$0.750V_{LCD1}$
1	0	1	1	$0.731V_{LCD1}$
1	1	0	0	$0.714V_{LCD1}$
1	1	0	1	$0.698V_{LCD1}$
1	1	1	0	$0.682V_{LCD1}$
1	1	1	1	$0.667V_{LCD1}$

(j) Duty Select

Three duty ratios 1/8, 1/9 and 1/10 are available.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	1	0	Duty		

D_2	D_1	D_0	Duty ratio	Scan Common
0	0	0	1/8 Duty	COM1 to COM8 (5x7 character + 1-icon)
0	0	1	1/9 Duty	COM1 to COM9 (5x7 character + 2-icon)
0	1	0	1/10 Duty	COM1 to COM10 (5x7 character + 3-icon)

(k) Power Save Mode

When Power Save mode is on, the SEG and COM drivers output "L", the built-in oscillator stops working (if one of the keys is pressed, the oscillator start working), so the operating current can be reduced. Under Power Save mode, the status of the key scan output terminals (S_1~S_5) can be selected. If pin status = "L", there is no output of key scan signal from the pin.

Under Power Save mode, outputs from Po1~Po4 ports are just kept as before

Power Save mode will be canceled when operate normally.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	0	0	0	Power save	

D_1	D_0	Function	Internal OSC.	LCD	Key scan output terminals *1				
					S_1 *2	S_2	S_3	S_4	S_5
0	0	Normal	ON	ON	H	H	H	H	H
0	1	Power save 1	Stop	Display Off	L	L	L	L	H
1	0	Power save 2	Stop	Display Off	L	L	L	H	H
1	1	Power save 3	Stop	Display Off	H	H	H	H	H

*1 The status during no key scan signal.

*2 Pin 79 (NJU6539FC2: pin 81) can be used as S_1 or Po4. Refer to (i) instruction for setting.

(i) PWM Frequency / Po4 (S1)

This instruction is used to set PWM frequency, and choose pin 79 (for NJU6539FC2: pin 81) as a PWM signal output port (Po4) or a key scan port (S1).

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	1	0	0	Port	PWM frequency

D_0 0: fsys / 128 frequency. (Default)
1: fsys / 256 frequency
D_1 0: PWM port (Po4)
1: Key scan port (S_1)

(m) PWM Output Port

This instruction is used to select port for PWM output. The PWM data, which is determined by (n) PWM Program/Port Mode and (o) PWM Data / Count Step, will be output via the selected port.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	0	0	0	PWM port	

D_1	D_0	PWM output port
0	0	Po1
0	1	Po2
1	0	Po3
1	1	Po4

(n) PWM Program / Port Mode

This instruction is used to enable/disable the Sweep function and selects port mode.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	0	0	1	Port mode	Sweep function

D_0 0: Sweep function disable
1: Sweep function enable
D_1 0: General port mode
1: LED port mode

(o) PWM Data / Count Step

This instruction is used to set PWM data and count step for the selected port (Po1~Po4). For the General Port mode, the duty cycle variation of the PWM signal from 0% to 100% can be divided into 128 steps. For LED Port mode, 16 steps are available.

If not using Sweep function, after PWM data is setup, the new PWM data will be outputted from the next frame. If using sweep function, initial value of PWM data and count step need to be input, and then execute (q) PWM Program ON, finally the new PWM data will be outputted from the next frame.

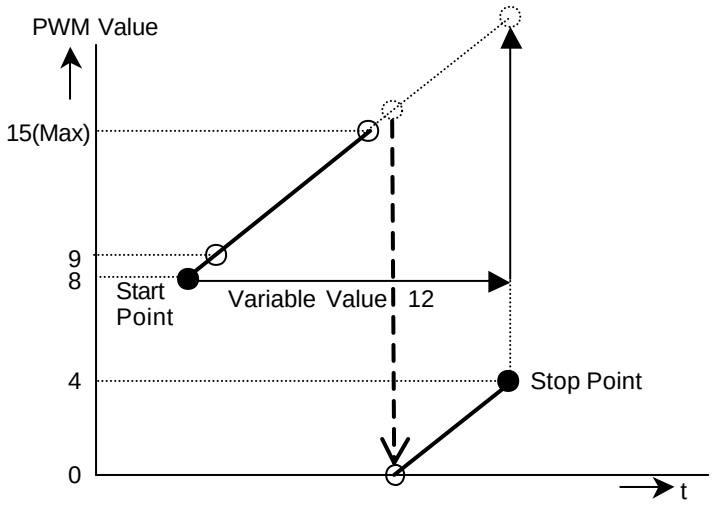
The upper bits of PWM data shall be input first and then the lower bits, after the lower bits setup over, the new PWM data will be outputted from the next frame. Only setting up upper bits will not change the PWM data.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	0	0	PWM_7	PWM_6	PWM_5	PWM_4	Upper bits
0	0	1	1	1	PWM_3	PWM_2	PWM_1	PWM_0	Lower bits

PWM7~PWM0: PWM data for General Output ports Po1~Po4.

If the PWM data reached the maximum (minimum) value before count-up is over, the PWM data will return to 0 (128/128), and count up (down) from 0 (128/128) continually until all the count step is counted.

Ex.) LED Port Mode
Start point PWM value 8 (27/128 duty)
Counter Step 12
Sweep Direction UP



8(Start)↦ 9 → (Count up) → 15 (Max) → 0 (Min) → 4 (Stop)

PWM Port mode PWM Value (*: Don't Care)

PWM_7	PWM_6	PWM_5	PWM_4	PWM_3	PWM_2	PWM_1	PWM_0	PWM DUTY	Counter Number	PWM_7	PWM_6	PWM_5	PWM_4	PWM_3	PWM_2	PWM_1	PWM_0	PWM DUTY	Counter Number
0	0	0	0	0	0	0	0	0/128	0	0	1	0	0	0	0	0	1	65/128	65
	0	0	0	0	0	0	1	1/128	1		1	0	0	0	0	1	0	66/128	66
	0	0	0	0	0	1	0	2/128	2		1	0	0	0	0	1	1	67/128	67
	0	0	0	0	0	1	1	3/128	3		1	0	0	0	1	0	0	68/128	68
	0	0	0	0	1	0	0	4/128	4		1	0	0	0	1	0	1	69/128	69
	0	0	0	0	1	0	1	5/128	5		1	0	0	0	1	1	0	70/128	70
	0	0	0	0	1	1	0	6/128	6		1	0	0	0	1	1	1	71/128	71
	0	0	0	0	1	1	1	7/128	7		1	0	0	1	0	0	0	72/128	72
	0	0	0	1	0	0	0	8/128	8		1	0	0	1	0	0	1	73/128	73
	0	0	0	1	0	0	1	9/128	9		1	0	0	1	0	1	0	74/128	74
	0	0	0	1	0	1	0	10/128	10		1	0	0	1	0	1	1	75/128	75
	0	0	0	1	0	1	1	11/128	11		1	0	0	1	1	0	0	76/128	76
	0	0	0	1	1	0	0	12/128	12		1	0	0	1	1	0	1	77/128	77
	0	0	0	1	1	0	1	13/128	13		1	0	0	1	1	1	0	78/128	78
	0	0	0	1	1	1	0	14/128	14		1	0	0	1	1	1	1	79/128	79
	0	0	0	1	1	1	1	15/128	15		1	0	1	0	0	0	0	80/128	80
	0	0	1	0	0	0	0	16/128	16		1	0	1	0	0	0	1	81/128	81
	0	0	1	0	0	0	1	17/128	17		1	0	1	0	0	1	0	82/128	82
	0	0	1	0	0	1	0	18/128	18		1	0	1	0	0	1	1	83/128	83
	0	0	1	0	0	1	1	19/128	19		1	0	1	0	1	0	0	84/128	94
	0	0	1	0	1	0	0	20/128	20		1	0	1	0	1	0	1	85/128	85
	0	0	1	0	1	0	1	21/128	21		1	0	1	0	1	1	0	86/128	86
	0	0	1	0	1	1	0	22/128	22		1	0	1	0	1	1	1	87/128	87
	0	0	1	0	1	1	1	23/128	23		1	0	1	1	0	0	0	88/128	88
	0	0	1	1	0	0	0	24/128	24		1	0	1	1	0	0	1	89/128	89
	0	0	1	1	0	0	1	25/128	25		1	0	1	1	0	1	0	90/128	90
	0	0	1	1	0	1	0	26/128	26		1	0	1	1	0	1	1	91/128	91
	0	0	1	1	0	1	1	27/128	27		1	0	1	1	1	0	0	92/128	92
	0	0	1	1	1	0	0	28/128	28		1	0	1	1	1	0	1	93/128	93
	0	0	1	1	1	0	1	29/128	29		1	0	1	1	1	1	0	94/128	94
	0	0	1	1	1	1	0	30/128	30		1	0	1	1	1	1	1	95/128	95
	0	0	1	1	1	1	1	31/128	31	0	1	1	0	0	0	0	0	96/128	96
0	0	1	0	0	0	0	0	32/128	32		1	1	0	0	0	0	1	97/128	97
	0	1	0	0	0	0	1	33/128	33		1	1	0	0	0	1	0	98/128	98
	0	1	0	0	0	1	0	34/128	34		1	1	0	0	0	1	1	99/128	99
	0	1	0	0	0	1	1	35/128	35		1	1	0	0	1	0	0	100/128	100
	0	1	0	0	1	0	0	36/128	36		1	1	0	0	1	0	1	101/128	101
	0	1	0	0	1	0	1	37/128	37		1	1	0	0	1	1	0	102/128	102
	0	1	0	0	1	1	0	38/128	38		1	1	0	0	1	1	1	103/128	103
	0	1	0	0	1	1	1	39/128	39		1	1	0	1	0	0	0	104/128	104
	0	1	0	1	0	0	0	40/128	40		1	1	0	1	0	0	1	105/128	105
	0	1	0	1	0	0	1	41/128	41		1	1	0	1	0	1	0	106/128	106
	0	1	0	1	0	1	0	42/128	42		1	1	0	1	0	1	1	107/128	107
	0	1	0	1	0	1	1	43/128	43		1	1	0	1	1	0	0	108/128	108
	0	1	0	1	1	0	0	44/128	44		1	1	0	1	1	0	1	109/128	109
	0	1	0	1	1	0	1	45/128	45		1	1	0	1	1	1	0	110/128	110
	0	1	0	1	1	1	0	46/128	46		1	1	0	1	1	1	1	111/128	111
	0	1	0	1	1	1	1	47/128	47		1	1	1	0	0	0	0	112/128	112
	0	1	1	0	0	0	0	48/128	48		1	1	1	0	0	0	1	113/128	113
	0	1	1	0	0	0	1	49/128	49		1	1	1	0	0	1	0	114/128	114
	0	1	1	0	0	1	0	50/128	50		1	1	1	0	0	1	1	115/128	115
	0	1	1	0	0	1	1	51/128	51		1	1	1	0	1	0	0	116/128	116
	0	1	1	0	1	0	0	52/128	52		1	1	1	0	1	0	1	117/128	117
	0	1	1	0	1	0	1	53/128	53		1	1	1	0	1	1	0	118/128	118
	0	1	1	0	1	1	0	54/128	54		1	1	1	0	1	1	1	119/128	119
	0	1	1	0	1	1	1	55/128	55		1	1	1	1	0	0	0	120/128	120
	0	1	1	1	0	0	0	56/128	56		1	1	1	1	0	0	1	121/128	121
	0	1	1	1	0	0	1	57/128	57		1	1	1	1	0	1	0	122/128	122
	0	1	1	1	0	1	0	58/128	58		1	1	1	1	0	1	1	123/128	123
	0	1	1	1	0	1	1	59/128	59		1	1	1	1	1	0	0	124/128	124
	0	1	1	1	1	0	0	60/128	60		1	1	1	1	1	0	1	125/128	125
	0	1	1	1	1	0	1	61/128	61		1	1	1	1	1	1	0	126/128	126
	0	1	1	1	1	1	0	62/128	62		1	1	1	1	1	1	1	127/128	127
	0	1	1	1	1	1	1	63/128	63	1	*	*	*	*	*	*	*	128/128	128
	1	0	0	0	0	0	0	64/128	64										

LED Mode PWM Value (*: Don't Care)

PWM_7	PWM_6	PWM_5	PWM_4	PWM_3	PWM_2	PWM_1	PWM_0	PWM DUTY	Counter Number
*	*	*	*	0	0	0	0	0/128	0
*	*	*	*	0	0	0	1	1/128	1
*	*	*	*	0	0	1	0	2/128	2
*	*	*	*	0	0	1	1	3/128	3
*	*	*	*	0	1	0	0	5/128	4
*	*	*	*	0	1	0	1	8/128	5
*	*	*	*	0	1	1	0	13/128	6
*	*	*	*	0	1	1	1	19/128	7
*	*	*	*	1	0	0	0	27/128	8
*	*	*	*	1	0	0	1	36/128	9
*	*	*	*	1	0	1	0	46/128	10
*	*	*	*	1	0	1	1	59/128	11
*	*	*	*	1	1	0	0	73/128	12
*	*	*	*	1	1	0	1	90/128	13
*	*	*	*	1	1	1	0	108/128	14
*	*	*	*	1	1	1	1	128/128	15

(p) Slope / Stepping Time

The changing speed of the PWM signal and the count direction can be programmed by this instruction. The Stepping Time is defined as the time that one count step takes.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	1	Direction		Stepping Time	

D_1	D_0	Stepping Time	
		PWM Port mode	LED Mode
0	0	4-frame	8-frame
0	1	8-frame	16-frame
1	0	12-frame	24-frame
1	1	16-frame	32-frame

D_3	D_2	Direction
0	0	HALT
0	1	UP
1	0	DOWN
1	1	Don't care

(q) PWM Program ON

At the end of the program, as a request signal to CPU, the SIO pin become low, the PWM value will be maintained as in the last count.

Because the request signal is also used as key scan request signal, it is necessary to read out the data and determine which one it is.

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	0	PWM Program Execution			

D_3 1: P_{O4} PWM Program Execution
D_2 1: P_{O3} PWM Program Execution
D_1 1: P_{O2} PWM Program Execution
D_0 1: P_{O1} PWM Program Execution

(r) Maker Test

This instruction is used only for device testing by the manufacturer.

If use this instruction by mistake, reset data again for an ordinary operation, Using reset instruction or inputting "L" into RSTb pin can make the testing mode ineffective

A0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	1	TB_3	TB_2	TB_1	TB_0

TB_3	TB_2	TB_1	TB_0	Test Data
0	0	0	0	Normal mode

(3) The Example of Using Sweep Function

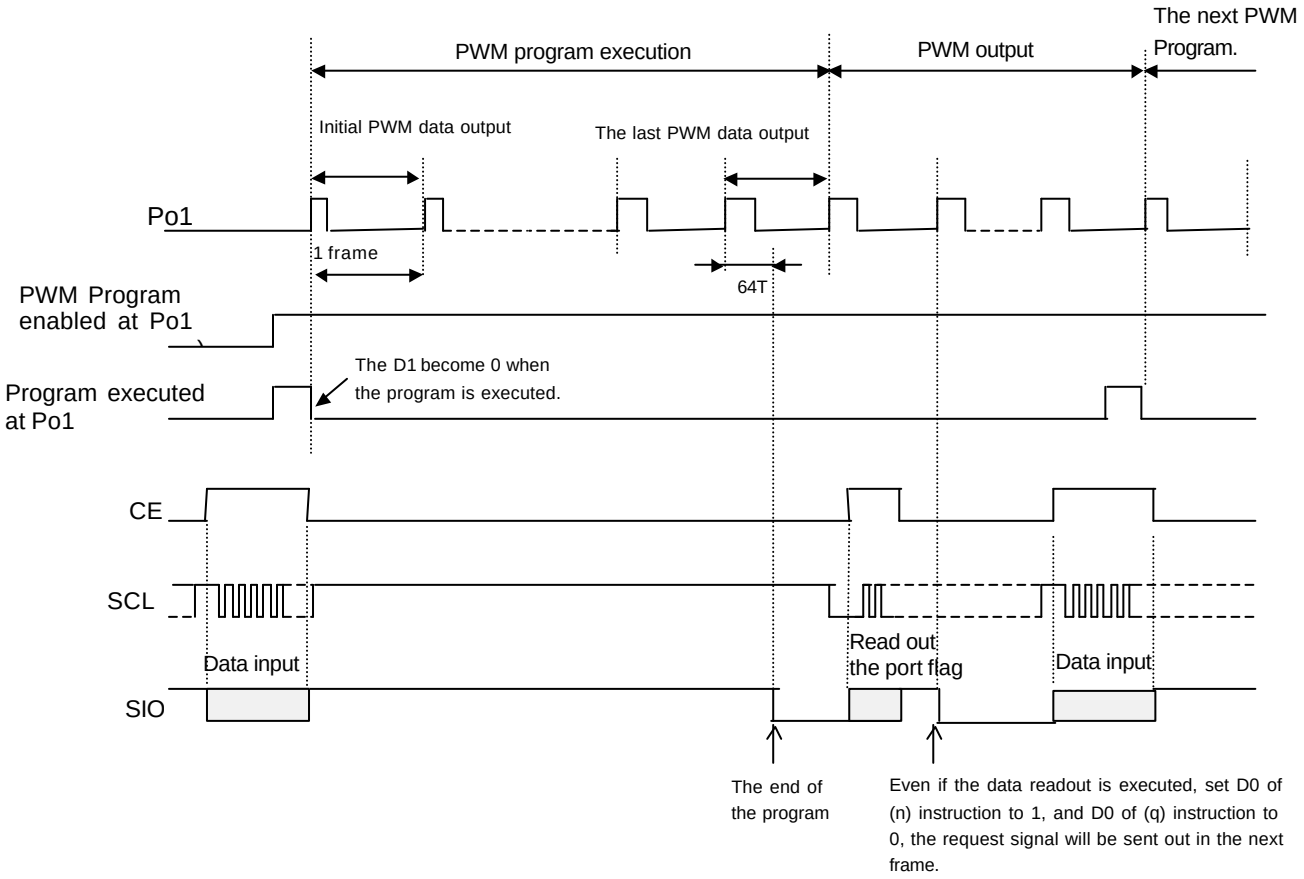
Set D_0 of (n) PWM Program/Port Mode to "1", the Sweep Function (PWM program) is enabled, and set D_0 (or D_1, D_2, D_3) of (q) PWM Program On to "1", the Sweep function starts to work, and D_0 (or D_1, D_2, D_3) changes from "1" to "0" automatically.

After the execution of the PWM program, SIO pin output "L" as a request signal at the last frame of PWM signal. CPU will detect the signal from which LED port, and ready for setting the next PWM program.

The request signal will be outputted even after data readout operation, but from the next data input, the output of the request signal will be stopped.

If set D_0 of (n) PWM Program/Port Mode to "0", the executed program will be stopped, and no request signal output too.

Example) PWM program for Po1



(4) Key Scan Circuit

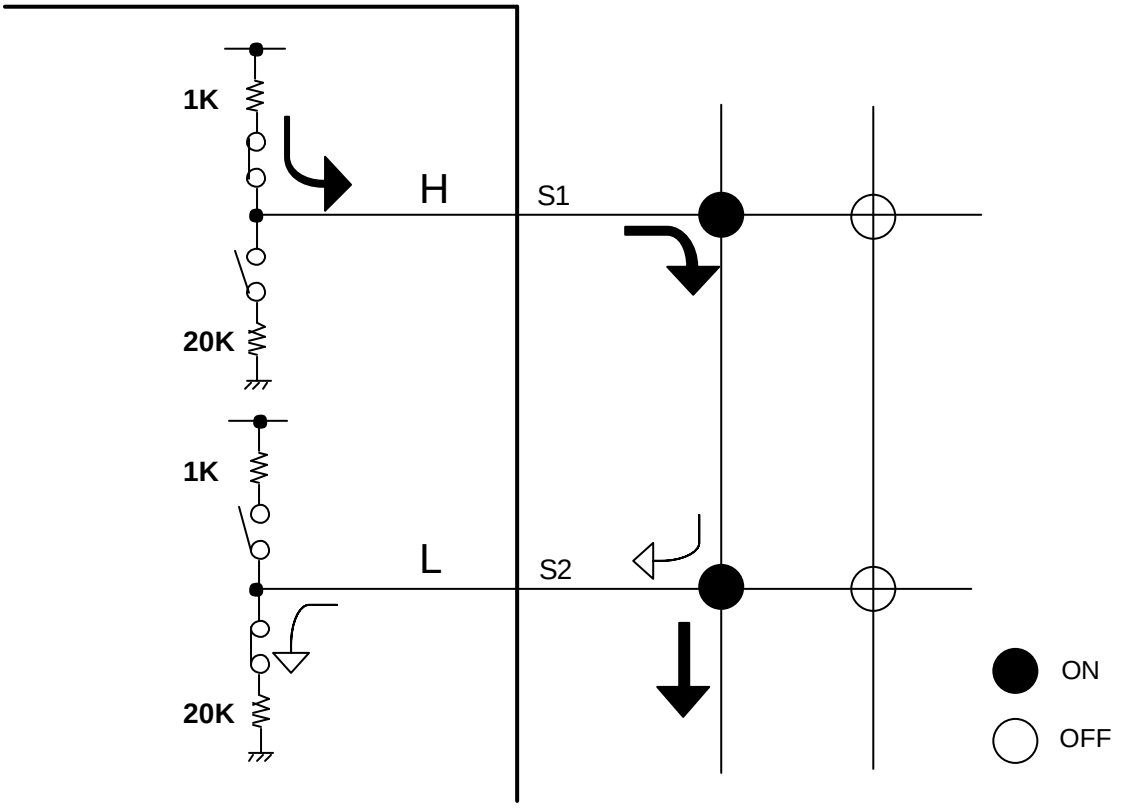
The key scan circuit can configure a max. 5 x 5 key matrix and read as many as 25-key inputs. The total key number varies with the different setting of (l) PWM Frequency/Po4 (S1).

The key scan data is taken in by two steps, first confirms whether the key is pressed or not by comparing the scan data of the two straight scan cycle, if the scan data are the same, then send the scan data to MPU.

If a key is pressed, after 322T seconds (T=1/fsys=16/fosc, fsys: internal system clock frequency), SIO terminal becomes "L" as a request signal. Because SIO ="L" is also used as the request signal for Sweep function. It is necessary to know the request signal for which one.

The key scan circuit does not require external diode to prevent it from circuit short.

Shown as below, ON resistance (1k ohm) when the transistor = "H" is different from ON resistance (20k ohm) when the transistor = "L", so even if two keys were pushed simultaneously, there is little current flowing into the "L" side. Therefore the "H" level output at S1 can be maintained, and the short among output pins can be avoided.



Internal equivalent circuit (VDD=5V)

(4-1) The Relation Between Key Scan Data and Key Matrix

The relation between key data (KD) and key matrix shows as below, when the n^{th} key is pushed, KDn (n=1~25) is set to "1".

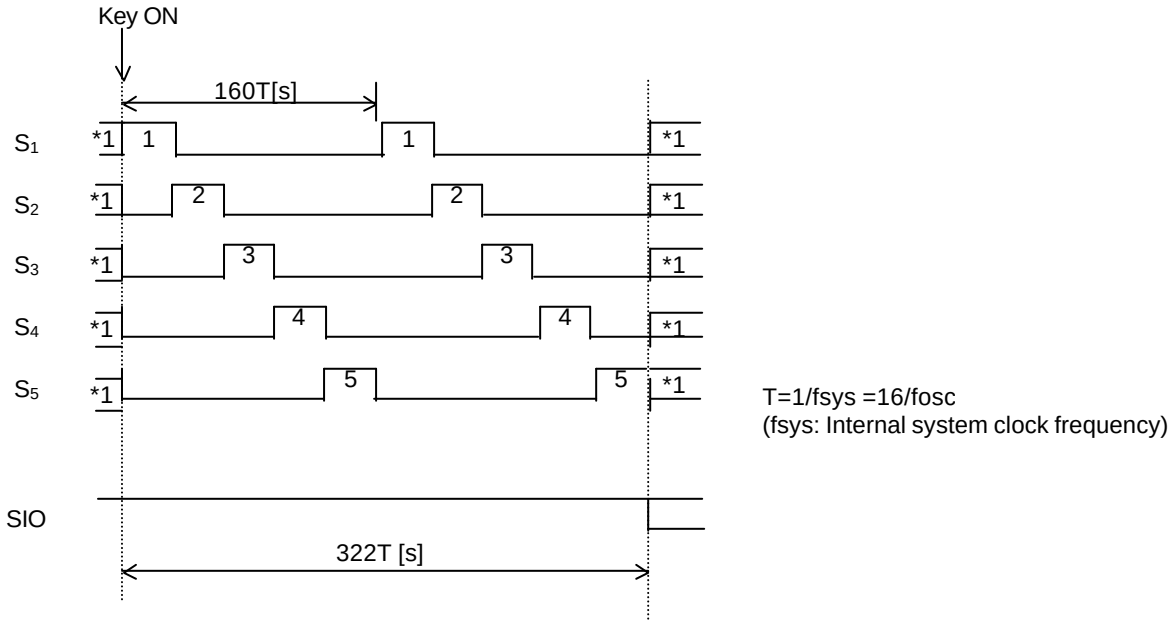
In case of 20 keys application, KD1 to KD5 are "0".

Under Power Save mode1, KD1 to KD20 = "0". Under Power Save mode2, KD1 to KD15 = "0". The terminals, which are not connected to any keys, should be open.

	K_1	K_2	K_3	K_4	K_5
S_1	KD1	KD2	KD3	KD4	KD5
S_2	KD6	KD7	KD8	KD9	KD10
S_3	KD11	KD12	KD13	KD14	KD15
S_4	KD16	KD17	KD18	KD19	KD20
S_5	KD21	KD22	KD23	KD24	KD25

(4-2) Timing of Key Scan

The key scan cycle is 160T seconds (T=1/fsys=16/fosc, fsys: Internal system clock frequency). To identify whether a key is pressed or not, key scan will be conducted twice before a possible key data output. If both key data are "1" during the two scan cycles, the key-press action is recognized. After 322T seconds since the key scan starting, SIO pin output "L" to CPU as a request signal for key data readout. When SIO pin ="L", the next key scan operation will stop until the key data is read out. If the key data is different in two scan operations, key scan will be done again, therefore, if a key-press action is shorter than 322T seconds, it is possible that there is no key data output



*1 The state of S1~S5 is decided by (1) PWM Frequency/Po4 (S1) and (n) Power Save Mode. The scan cycle and the timing of key data readout request are the same no matter which Power Save mode is used.

(4-3) Normal Mode

The key scan operation under normal mode is as follows.

1 The S1–S5 pins = "H" and the K1– K5 l= "L" if no key is pressed. When a key is pressed, the corresponding Kn (n=1~5) pins will become "H".

2, As soon as one of the keys is pushed, the scan operation starts, and this operation will be done twice continuously. If both of the key scan data are "1" in the two scan cycle, the scan operation will stop. If the two scan data are different, or key(s) still being pressed, the scan operation will continue until the key-press action confirmed or no pressed key anymore. The key scan operation will start again after key data read out by CPU.

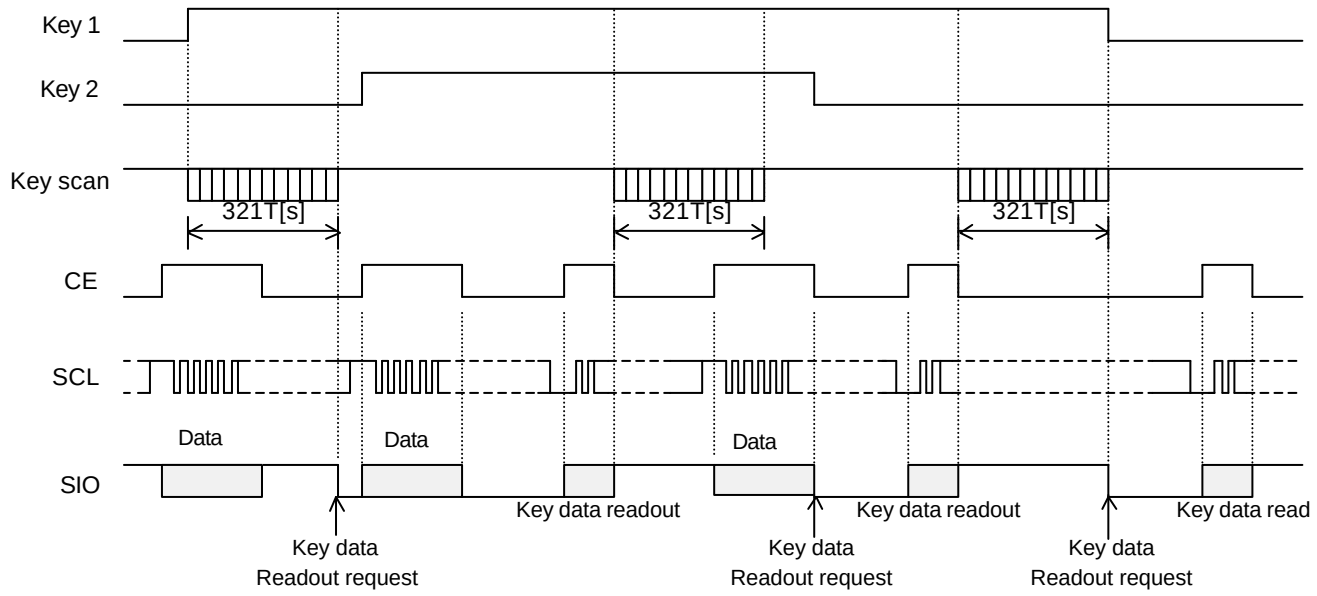
3 When the scan data is fixed (two scan data are the same), the SIO pin will output "L" as a request signal to CPU for data read. When CPU detects this request signal, data read will be conducted.

4 After the data read, the SIO pin becomes"H", and the CPU waits for the next scan data.

Because the SIO terminal is an open-drain type output circuit, the pull-up impedance to CPU power supply is required, if more than one key are pushed, the CPU will determine whether it is a multi key scan operation or not.

Key scan example (Normal mode)

T=1/fsys =16/fosc



(4-4) Power Save mode

Under Power Save mode, the key scan operation is like below.

1 The S1–S5 pins are set to "H" or "L" according to (k) Power Save Mode. The K1– K5 l="L" if no key is pressed. When a key is pressed, the corresponding Kn (n=1~5) pins will become "H".

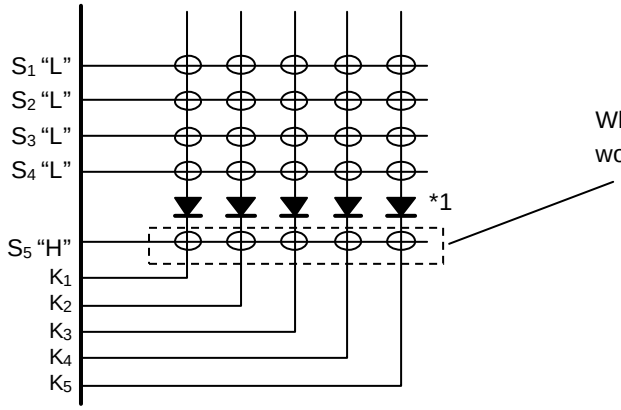
2. Under Power Save mode 3, all the pins of S1–S5 are set to "H". If a key is pushed, the oscillation circuit starts to work, and scan operation will be executed twice. If the same data can be obtained in this two scans, the scan operation and oscillation circuit will stop working. If the data is different in this two scans or the key is still being pushed, another two scan operations will be exe cuted.

3. When the scan data is fixed, the SIO pin will output "L" as a request signal to CPU for data read. When CPU detects this request signal, data read will be conducted.

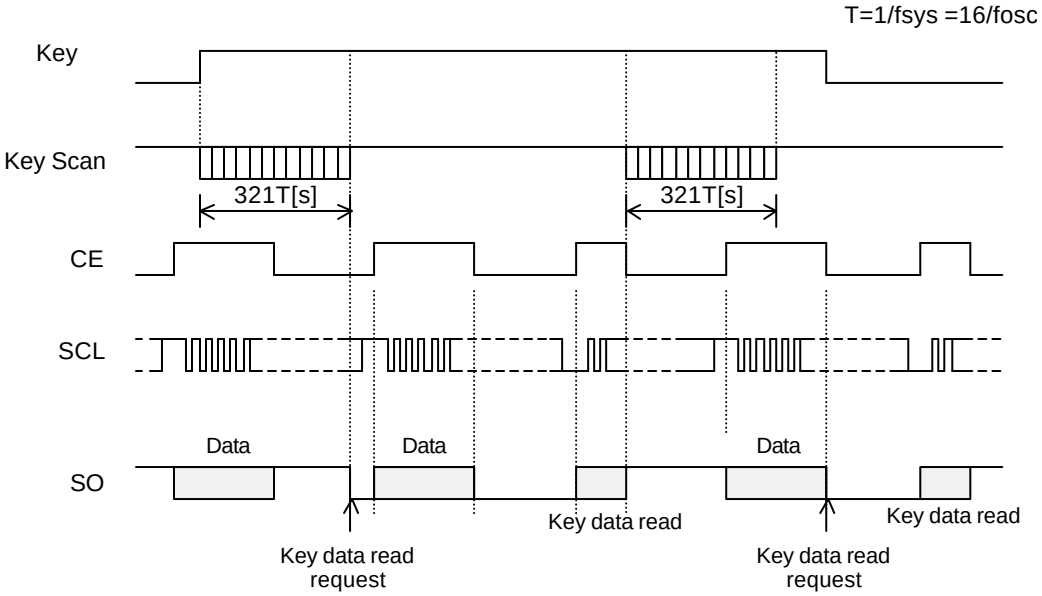
4. After the data read, the SIO pin becomes "H", and the CPU waits for the n ext scan data, and the Power Save mode is still effective.

Because the SIO terminal is an open-drain type circuit, the pull-up impedance to CPU power supply is required. If more than one key is pushed, the CPU will determine whether it is a multi-key scan operation or not.

Key scan example (Power Save mode 1)
Ex.) D0="0", D1="1" (S5="H" Power Save)



*1 Under the above Power Save mode, these diodes are used to prevent malfunction during the multi-key scan operation.



(4-5) Multi-key Scan Operation

As described in (4) Key Scan Circuit, even several keys are pushed simultaneously, S1~S5 pins can be maintained at "H" level (normal mode), so without the diode, the scan data can be detected and read out. But, if more than 2 keys are pressed like in Figure 1, the key 4 will be recognized as pressed. To prevent this kind of malfunction, diodes can be used like in Figure 3, or use software to reject possible misread multi-key input. (For example, make it invalid if 4 keys are pushed simultaneously)

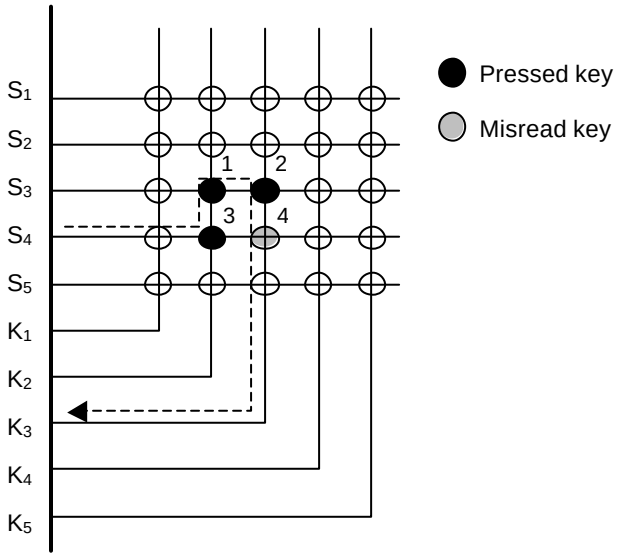


Fig. 1 Miss-recognized key of multi-key scan operation

Under Power Save mode 1 (only the keys on S5 line are valid) and Power Save mode 2 (only the keys on S4 and S5 lines are valid), if the inactive keys and the active keys are pushed together like in Figure 2, the key 4 will be recognized as pushed, in this case, the software can not reject the misread of key 4. The diodes need to be used as in Figure 3.

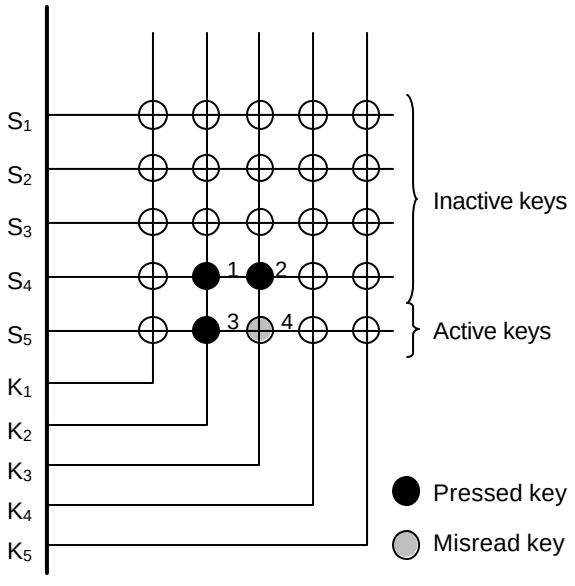


Fig. 2 Miss-recognition under Power Save mode 1

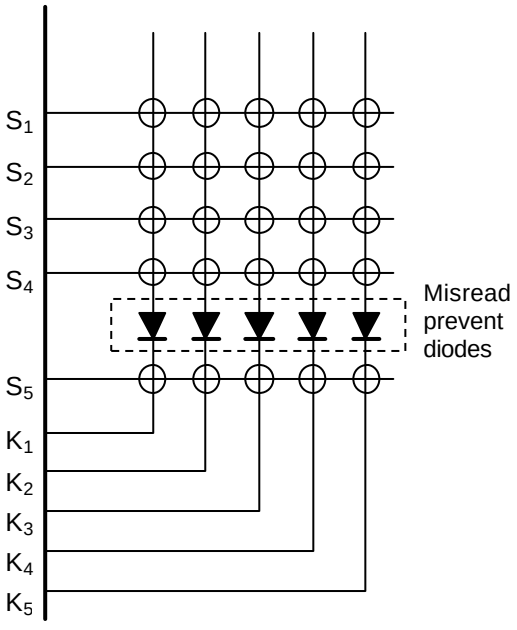


Fig. 3 Connect miss-recognition prevent diodes

(4-6) Key Scan Data Readout

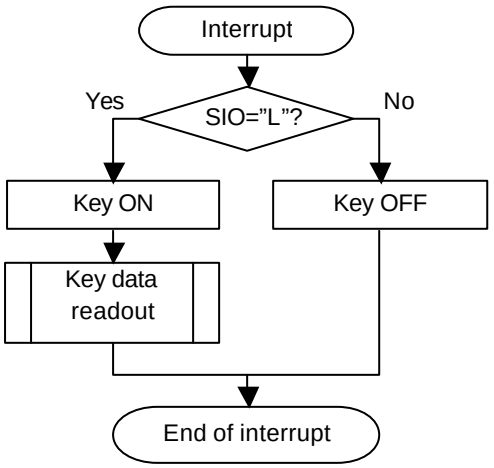
Key Data Readout

The minimum period between pressing a key and SIO becoming "L" is t1=332T seconds (T=1/fsys=16/fosc), but if the key-press is unstable or noise is strong, two key scan cycle will be conducted again, so the time frame becomes t1=676T seconds. After SIO becoming "L", there is no scan operation until the key scan data is read out. Once the scan data fixed, even there is a change of key status, the scan data will be maintained until it is read out. If data readout is during SIO= "H", key scan data or Power Save flag (PSF) data cannot be output correctly.

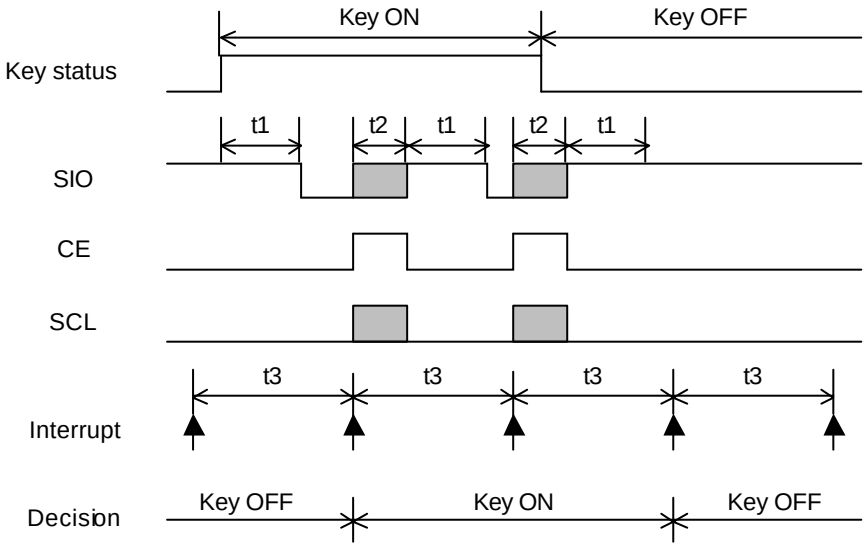
Exp. Key Data Readout

The interrupt processing of key data is as below. When there is an interruption request, SIO pin will be checked, if SIO = "L", the key(s) is recognized as being pushed (key ON), if SIO= "H", the key(s) is recognized as not being pushed (key OFF). To verify the key ON or OFF correctly, the time frame of interrupt processing shall be longer than the t1+t2 (t1: key scan time, considering unstable key scan data, t1 shall be 676T, t2: key data readout time).

- Sequence of key data reading out operation



- Timing chart of key data readout operation



t1: Key scan time
t2: Key data readout time
t3: Interrupt cycle

*: t3 > t1 + t2

(5) Reset

When the power supply voltage is lower than VDET (power down detect voltage, typically 1.6V), the device will be initialized by internally generated reset signal. This function allows the NJU6539 to be initialized whenever the power is ON or OFF.

(5-1) Initialization

1 The oscillation circuit stops working
2 Display off
3 No key scan operation
4 All the key data at buffer set to "0"

(5-2) The Status of Output Pin

Output terminals	Reset status
SEG_1 to SEG_{65}	L
COM_1 to COM_{10}	L
Po0 to Po2	L
Po3/S_0	L *1
S_1 to S_4	H
SIO	H *2

*1 This terminal outputs "L" as a general output port.
*2 Because the SIO terminal is an open-drain type output circuit, the pull-up impedance to CPU power supply is required. If key data readout is executed during power on reset, the read data is fixed to "H".

The reset instruction cannot substitute the hardware reset. The instruction only can initialize from 7 to 13 items as follows.

Initialization (Default)

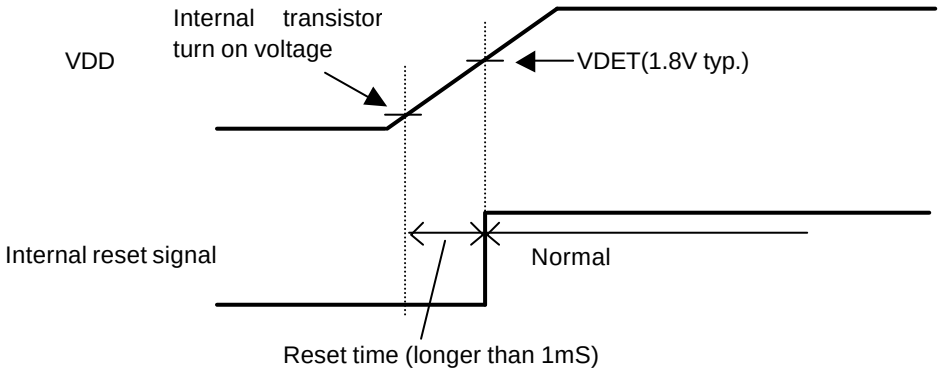
1. Clear serial interface register
2. Display off
3. ADC select — D_0="0" (Normal mode)
4. Normal Display — Non-inverse display
5. Whole display off — D_0="0" (Normal mode)
6. Power Save mode — D_1, D_0="0, 0" (Normal mode)
7. Page Address — 0 page
8. Column address — 00_H
9. EVR Register — D_3, D_2, D_1, D_0= "1, 1, 1, 1"
10. Duty Select — 1/10 Duty
11. Output Port (Po1~Po4) — f_{PWM} = (fosc/2)/128
12. Po4/S1 pin — Po4
13. Port Select — Po1
14. Not using PWM program, Po1~Po4 set as output port
15. PWM data/count step Register — D3, D2, D1, D0 = "0, 0, 0, 0" (upper 4 bits)
16. PWM data/count step Register — D3, D2, D1, D0= "0,0,0,0"(lower 4 bits)
17. Slope and Stepping Time — D1, D0= "0,0", slope =HALT
18. PWM Program On — No PWM program executed at Po1~Po4

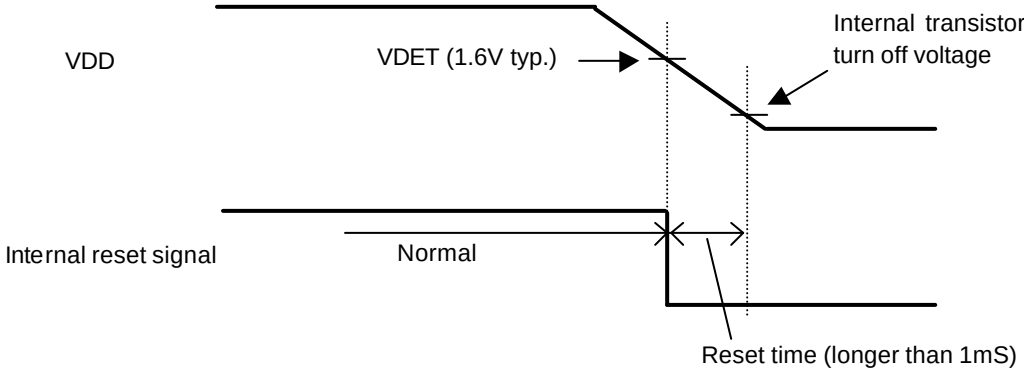
(5-3) Initialization by Hardware

After power ON, the hardware reset of NJU6539 can be realized by inputting a longer-than-10μs reset signal into RESb pin. The LSI will return to the normal operation about 1.0μs(max.) later from the rising edge of the reset signal.

(5-4) Power ON Reset Operation

With the built-in power-on-reset circuit (voltage detect), the device will be initialized during power ON or when the VDD going down below VDET. The reset operation will be conducted during VDD changing from 0 to VDET period. If this period is less than 1 ms, the correct initialization can not be guaranteed. Please use a capacitor to make sure the reset period is longer than 1 ms, on the other hand, the hardware reset can be used when the power supply cannot meet the time demand.

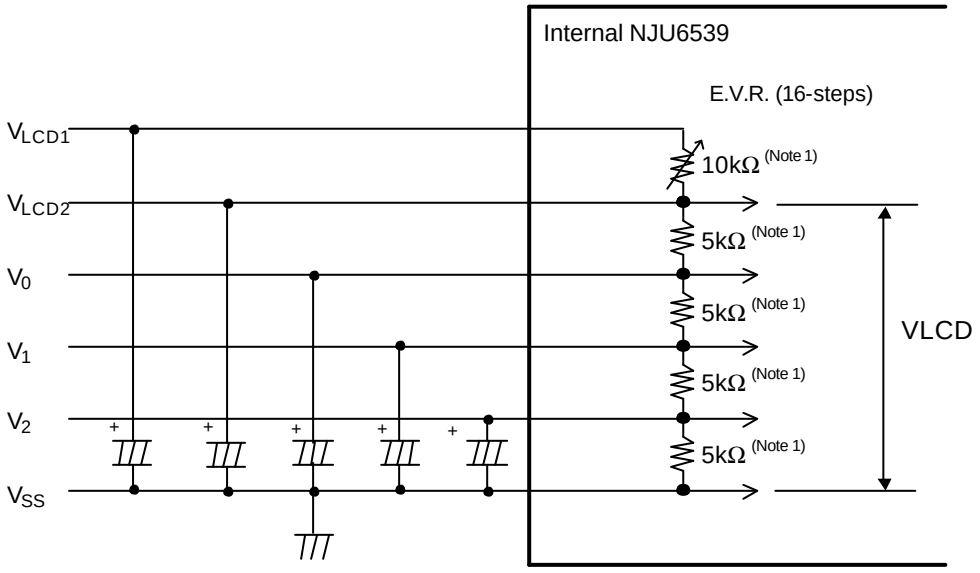




(6) LCD Driving Voltage Generation Circuit

The LCD driving bias voltages (V_{LCD2}, V_0, V_1 and V_2) are from by dividing input voltage V_{LCD1}. The built-in 16-step electronic volume is used for fine adjustment of the bias voltage. To stabilize the bias voltage, the external capacitors need to be used. The parameter of the capacitors shall be determined according to the LCD characteristics.

Power Supply	Duty ratio	1/8,1/9,1/10
	Bias	1/4
	V_{LCD}	V_{LCD2}-V_{SS}



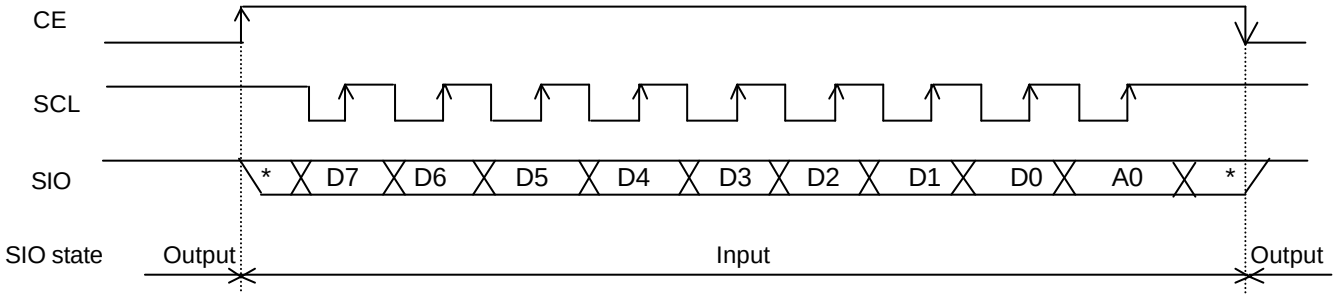
Note 1: Typical values of the resistors.

(7) Data Input Timing

Data format is shown below.

When the CE terminal = "L", SIO is ready for data output.

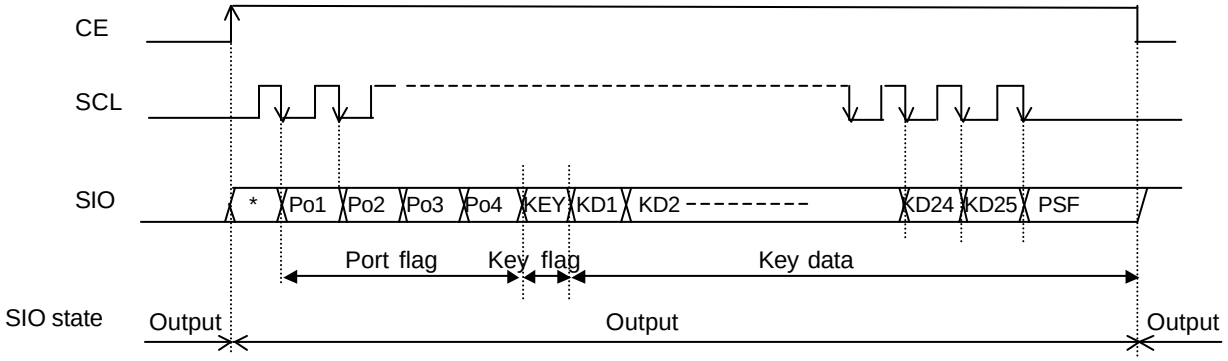
When the CE terminal at the rising edge, and SCL terminal ="H", SIO is ready for data input.



Note1) Data is fetched at the SCL rising edge.
Note2) At the rising edge of 9th SCL signal, input data will be interrupted as display data or instruction code according to A0.
Note3) If input data is less than 9 bits, no data will be fetched.
Note4) If input data is longer than 9 bits, the last 9 bits are fetched as valid data.

(8) Data Output Timing

The data output format shows bellow. The data output mode is set by "L" status of SCL terminal at the rising signal of CE terminal.



(8-1) Port Flag (Po1~Po4)

When the Sweep Function is over, this flag is set to "1".

(8-2) Key Flag

When key scan is over and there is key scan data, this flag is "1", if there is no key scan data, this flag is set to "0". When flag = "0", if make a readout of key data, the data is indefinite.

(8-3) Power Save Flag (PSF)

When key flag = "1", after KD25 is read out, PSF will be outputted. If PSF = "1", Power Save mode is ON, if PSF= "0", normal mode is ON.

■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply voltage	VDD max	V_{DD} terminal	-0.3 to +7.0	V
	VLCD max	V_{LCD1} terminal	-0.3 to +11.0	
Input terminal voltage	V_{IN1}	OSC, K_1 to K_5, CE, SCL, SIO terminal	-0.3 to VDD+0.3	V
	V_{IN2}	V_{LCD2}, V_0 to V_2 terminal	-0.3 to VLCD+0.3	
Output terminal voltage	V_{OUT1}	SIO terminal	-0.3 to +6.0	V
	V_{OUT2}	OSC, SEG_1 to SEG_{65}, COM_1 to COM_{10}, S_2 to S_5, Po1 to Po3, Po4 /S_1 terminal	-0.3 to VDD+0.3	
Power dissipation	Pdmax	Ta=25°C QFP100-C2	1000	mW
		Ta=25°C QFP100-G1	700	
Storage temperature	Tstg	-	-55 to +125	°C
Operating temperature	Topr	-	-40 to +85	°C

Note 1) All the pins potential values are specified as V_{SS}=0V.

Note 2) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used in the range specified in the DC electrical characteristics, or the electrical stress may cause mulfunctions and impact on the reliability

Note 3) Decoupling capacitor should be connected between VDD and VSS for stabilized operation.

■ DC ELECTRICAL CHARACTERISTICS

VDD=2.7 to 5.5V, Ta= - 40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max.	Unit	Note
Power supply (1)	VDD	VDD	2.7		5.5	V	
Power supply (2)	VLCD1	VLCD1	5.0		10.0		
Output voltage	VLCD2	VLCD2	2/3VLCD1		VLCD1	V	
Input voltage	V0	V0	VSS	3/4VLCD2	VLCD2	V	1
	V1	V1	VSS	2/4VLCD2	VLCD2		
	V2	V2	VSS	1/4VLCD2	VLCD2		
"H" level input voltage (1)	VIH(1)	K_1 to K_5	0.6VDD		VDD	V	
"H" level input voltage (2)	VIH(2)	SCL, SIO, CE	0.8VDD		VDD	V	
"L" level input voltage (1)	VIL(1)	K_1 to K_5, SCL, SIO, CE	0		0.2VDD	V	
Hysteresis voltage	VH	SCL, SIO, CE		0.25VDD		V	
"H" level input current	I_{IH}	SCL, SIO, CE, V_{IN} = VDD			5.0	μA	
"L" level input current	I_{IL}	SCL, SIO, K_1 to K_5, CE, V_{IN} = 0V	-5.0			μA	
Pull-up resistance	R_{PU}	RESb VDD=5.0V, V_{IN} = 0V	50	150	250	kΩ	
Pull-down resistance	R_{PD}	K_1 to K_5, VDD=5.0V, V_{IN} = VDD	50	150	250	kΩ	
Output off-leak current	IOFFH	SIO, VO=5.5V			6.0	μA	
"H" level output voltage (1)	VOH(1)	S_1 to S_5 VDD=5.0V, Io = -500uA	VDD-1.2		VDD-0.2	V	
		S_1 to S_5 VDD=3.0V, Io = -250uA	VDD-1.1		VDD-0.1		
"H" level output voltage (2)	VOH(2)	Po_1 to Po_4 VDD=5.0V, Io = -10mA	VDD-1.0			V	
		Po_1 to Po_4 VDD=3.0V, Io = -5mA	VDD-0.6				
"L" level output voltage (1)	VOL(1)	S_1 to S_5 VDD=5.0V, Io = 25μA	0.2		1.5	V	
		S_1 to S_5 VDD=3.0V, Io = 5μA	0.05		0.6		
"L" level output voltage (2)	VOL(2)	Po_1 to Po_4 VDD=5.0V, Io = 10mA			1.0	V	
		Po_1 to Po_4 VDD=3.0V, Io = 5mA			0.6		
"L" level output voltage (3)	VOL(3)	SIO Io = 1mA			0.5	V	
Driver ON-resistance (COM)	R_{COM}	Ta=25°C, VO=V_{LCD2}, VSS, V0, V2 ±Id=1μA (COM terminal)			10	kΩ	2
Driver ON-resistance (SEG)	R_{SEG}	Ta=25°C, VO=V_{LCD2}, VSS, V1 ±Id=1μA (SEG terminal)			10	kΩ	2
Oscillation Frequency	f_{OSC}	Ta=25°C, VDD=5.0V R_{OSC}=180kΩ	320	400	480	kHz	
LCD Driving voltage	V0	E.V.R. value "0,0,0,0" V_{LCD1}=8.0V	5.8	6.0	6.2	V	
	V1		3.8	4.0	4.2		
	V2		1.8	2.0	2.2		
Bleeder resistance	R_B	VLCD2-VSS, Ta=25°C		20		kΩ	
E.V.R. resistance	R_{EVR}	VLCD1-VLCD2, Ta=25°C		10		kΩ	
Power down detect voltage	VDET		1.0	1.6	2.2	V	
Reset time	Tr	RESb	1.0			μs	
Reset "L" pulse width	Trw	RESb	10.0			μs	
Operating current	IDD1	Power save mode			20	μA	
	IDD2	VDD=5.5V, Output open f_{OSC}=400kHz,			200	μA	
	ILCD1	Power save mode			**5**	μA	
	ILCD2	VLCD1=10.0V Output open f_{OSC}=400kHz,			**1000**	μA	

Note 1) The order VLCD1≥VLCD2≥V0≥V1≥V2≥VSS must be maintained.

Note 2) R_{COM} and R_{SEG} are the resistance between power supply terminals (VSS, VLCD2, or V0, V1, V2) and each common terminal, and supply voltage (VSS, VLCD2, or V0, V1, V2) and each segment terminal respectively, and measured when the current Id is flown into every common and segment terminals at a same time.

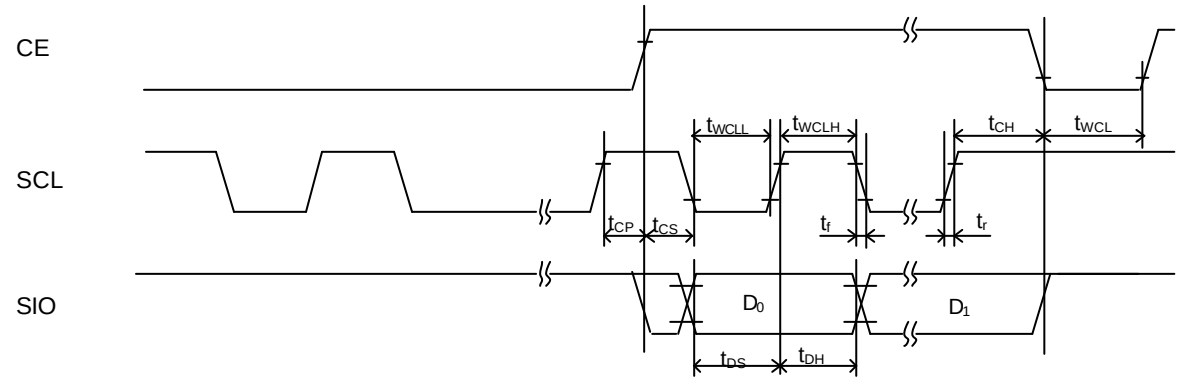
■ AC CHARACTERISTICS

VDD=2.7 to 5.5V, Ta= - 40 to 85°C

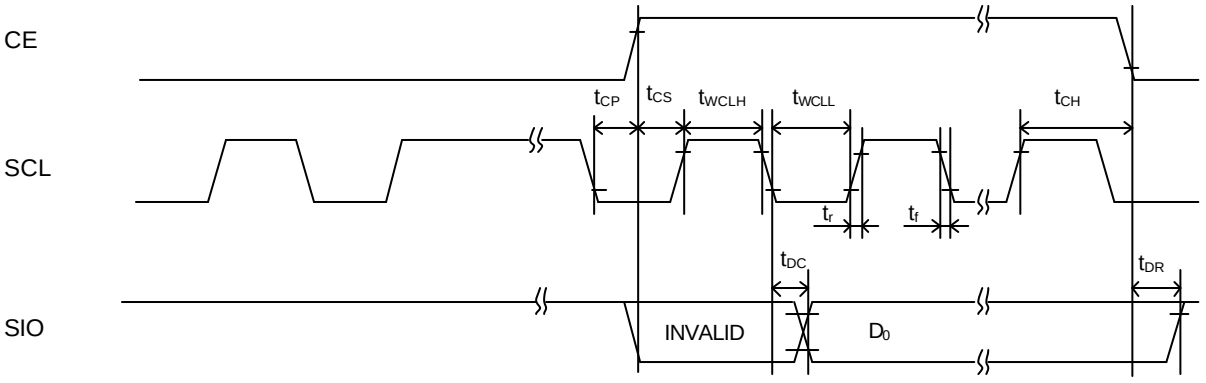
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
"L" level clock pulse width	t_{WCLL}	SCL	160			ns	
"H" level clock pulse width	t_{WCLH}	SCL	160			ns	
Data setup time	t_{DS}	SCL, SIO	160			ns	
Data hold time	t_{DH}	SCL, SIO	160			ns	
CE wait time	t_{CP}	CE, SCL	160			ns	
CE setup time	t_{CS}	CE, SCL	160			ns	
CE hold time	t_{CH}	CE, SCL	160			ns	
CE "L" level width	t_{WCL}	CE	160			ns	
SIO output delay time	t_{DC}	SIO, Rpu=4.7kΩ, CL=10pF			1.5	µs	1
SIO rise time	t_{DR}	SIO, Rpu=4.7kΩ, CL=10pF			1.5	µs	
SCL rise tine	t_r				15	ns	
SCL fall time	t_f				15	ns	

Note 1) Because SIO terminal is Open-Drain type output, the delay and rise time varies with the Rpu and CL.

(1) Write operation

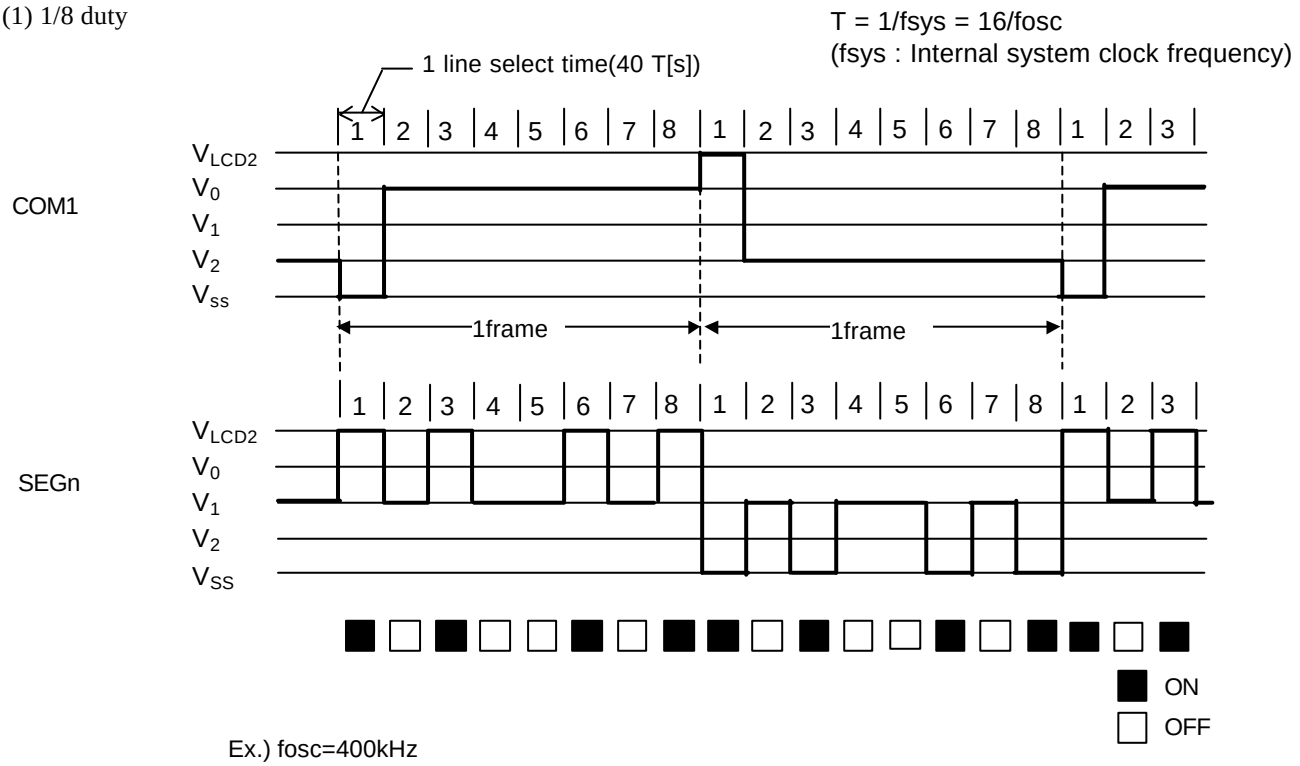


(2) Key data read operation



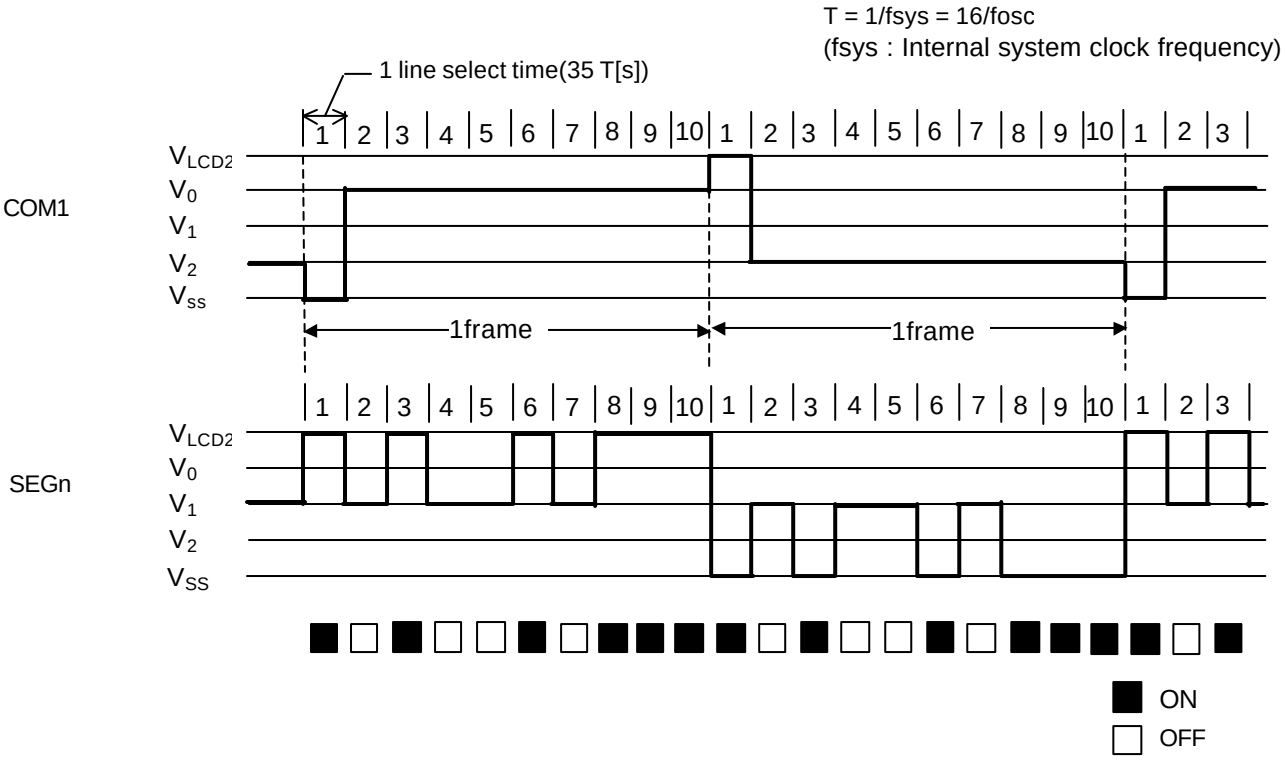
Relation between oscillation frequency and LCD frame frequency

(1) 1/8 duty



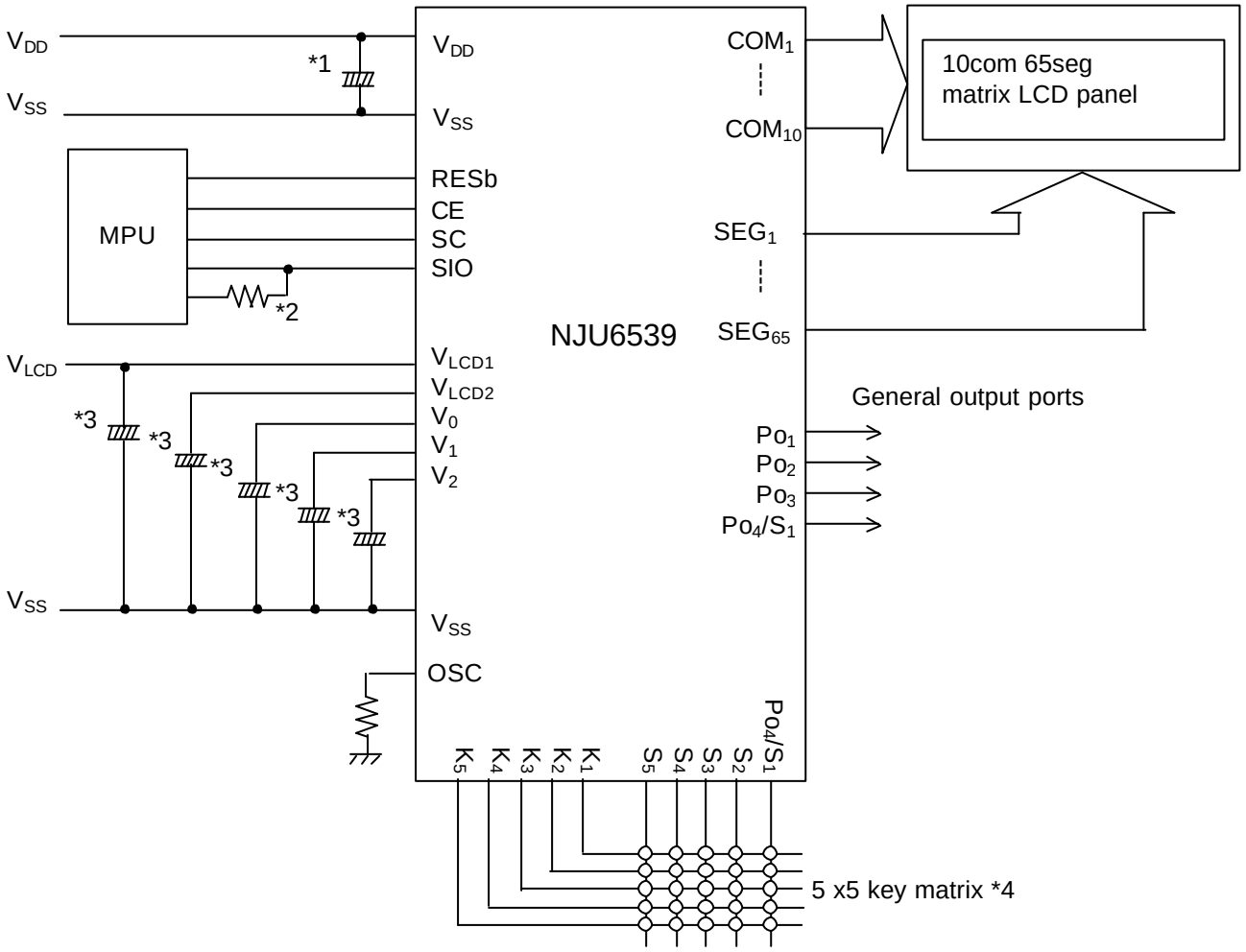
Ex.) fosc=400kHz
Frame frequency =1/(40T x duty)=1/(40 x (16/400kHz) x 8)=78.1(Hz)

(2) 1/10 duty



fosc=400kHz
Frame frequency =1/(35T x duty)=1/(35 x (16/400kHz) x 10)=71.4(Hz)

■ APPLICATION CIRCUIT



*1 To use the Voltage-Detect reset circuit, the rising time during Power on and the falling time during Power off must be kept longer than 1ms.
*2 The SIO terminal requires external pull-up resistor connected to the MPU power.
*3 This capacitor for bias voltage stabilization should be selected according to the characteristics of LCD.
*4 P_{O4} /S_1 terminal is either a general output ports or a key scan signal output terminals.