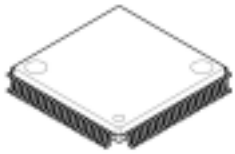
**Preliminary**

# 12CHARACTER 1-LINE DOT MATRIX LCD CONTROLLER DRIVER with SMOOTH SCROLL FUNCTION

## ■ GENERAL DESCRIPTION

The **NJU6625** is a Dot Matrix LCD controller driver for 12-character 1-line with icon display in single chip.
It contains bleeder resistance, general output port, keyscan circuit, CR oscillator, microprocessor interface circuit, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers, and others.
The character generator ROM consisting of 7,840bits stores 224 kinds of character font, Each 1,120 bits CG RAM and Icon display RAM can store 32 kind of special character displayed on the dot matrix display area or 60 kinds of Icon display area.
The 8-common(7 for character, 1 for Icon) and 71-segment drivers operate 12-character 1-line with 60 Icon LCD display and LED driver drives 4 LED which can use like as indicator.
The 16$^{th}$ display contrast control function is incorporated. Therefore, only simple power supply circuit on chip operates the contrast adjustment easily.
The complete CR oscillator requires no external components.
The serial interface which operates by 1MHz, communicates with external MCU.
As an outstanding feature, NJU6625 realizes the horizontal smooth scroll of characters by combination of instruction.

## ■ PACKAGE OUTLINE

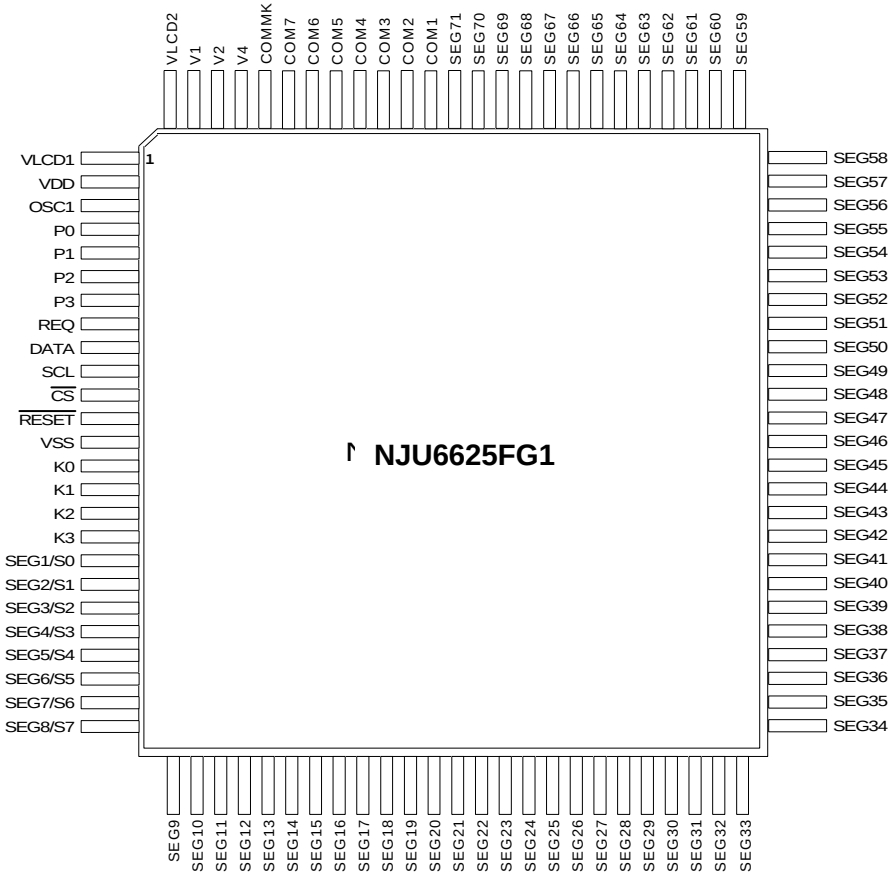


**NJU6625FG1**

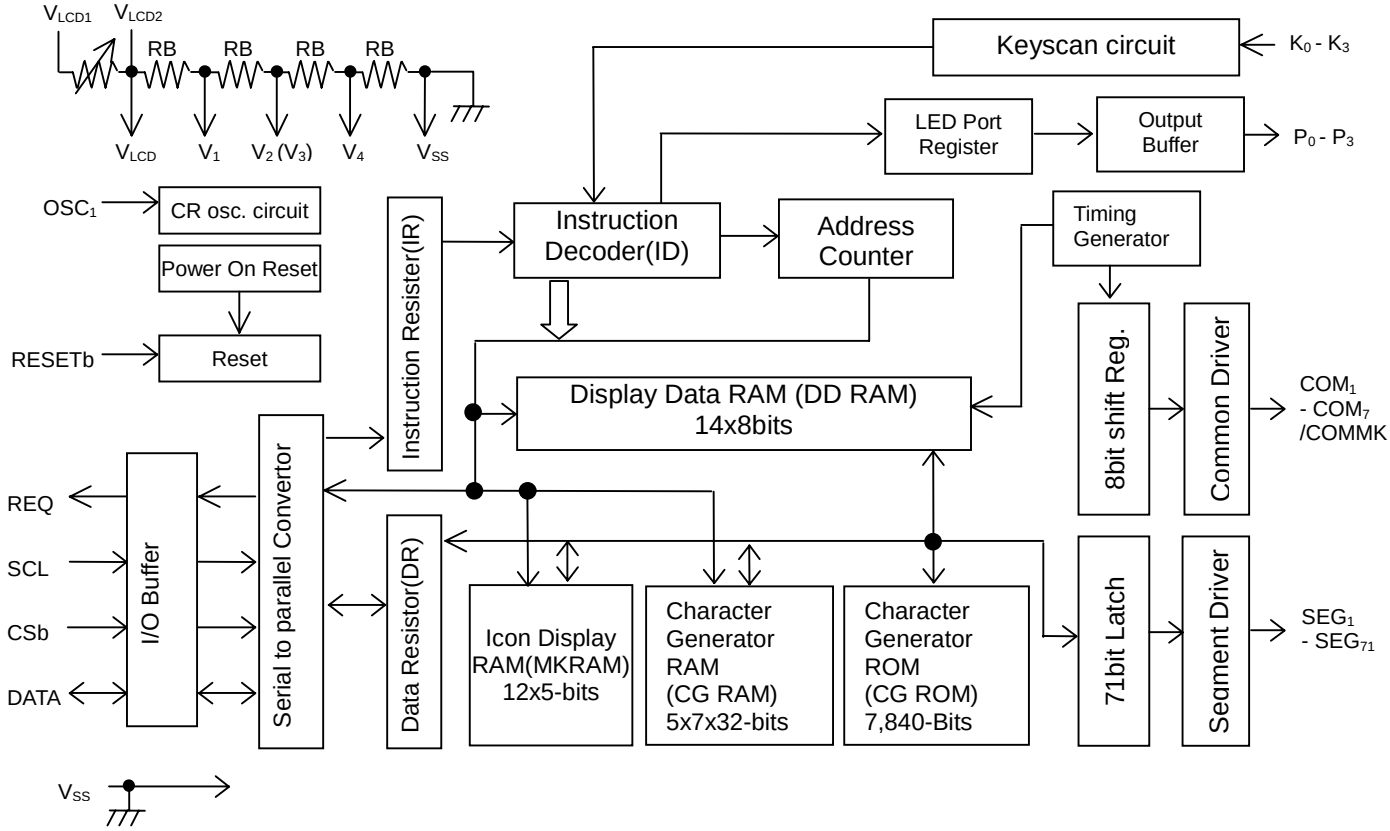
## ■ FEATURES

- 12-character 1-line Dot Matrix LCD Controller Driver
- Maximum 60 Icon Display
- Serial Direct Interface with Microprocessor
- Display Data RAM 14 x 8 bits :Maximum 12-character 1-line Display
- Character Generator ROM 7,840bits :224 Characters for 5 x 7 Dots
- Character Generator RAM 1,120bits :32 Patterns (5 x 7 Dots)
- Icon Display RAM Maximum 60-Icons
- High voltage LCD Driver 8-common / 71-segment
- Duty and Bias Ratio 1/8 duty, 1/4 bias
- Useful Instruction set Clear Display, Address Home, Display ON/OFF, Display blink, Address shift, Character Shift, Dot Shift, Keyscan ON/OFF cont. e.t.c.
- 32-Key input(4x8 keyscan)
- General output ports (4-ports)
- Power on Initialization / Hardware Reset
- Bleeder resistance on chip
- Software contrast control(16-step)
- Oscillation Circuit on-chip
- Low Power Consumption
- Operating Voltage 2.4 to 5.5V
- Package Outline QFP100-G1
- C-MOS Technology

## ■ PIN CONFIGURATION




## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

| No. | SYMBOL | I/O | F U N C T I O N |
|---|---|---|---|
| 2<br>13 | $V_{DD}$<br>$V_{SS}$ | - | Power Source :$V_{DD}$=+5V, GND :$V_{SS}$=0V |
| 1 | $V_{LCD1}$ | I | LCD driving voltage input terminal |
| 100<br>99<br>98<br>97 | $V_{LCD2}$<br>$V_1$<br>$V_2$<br>$V_4$ | I | LCD driving voltage stabilization capacitor terminals.<br>Connect the capacitor between VLCD2 and VSS, V1 and VSS, V2 and VSS, V4 and VSS.<br>typ. : 0.1uF |
| 3 | $OSC_1$ | I | Resistor connection terminal for oscillation<br>/ External clock input terminal |
| 11 | CSb | I | Chip select signal input of serial I/F. |
| 10 | SCL | I | Shift clock input of serial I/F. |
| 9 | DATA | I/O | Serial data input of serial I/F. |
| 12 | RESETb | I | Reset terminal<br>When the "L" level is input over than 1.2ms to this terminal, the system will be reset ( at $f_{OSC}$ 145KHz ). |
| 4-7 | $P_0$-$P_3$ | O | General output port<br>LED driver drives LED as indicator on ethers. |
| 8 | REQ | O | Key request signal output terminal. |
| 14-17 | $K_0$-$K_3$ | I | Key scanning input terminals. |
| 18-25 | $SEG_1/S_0$-<br>$SEG_8/S_7$ | O | LCD segment driving signal output / Key scanning output terminals. |
| 26-88 | $SEG_9$-$SEG_{71}$ | O | LCD segment driving signal output terminals. |
| 89-95 | $COM_1$-$COM_7$ | O | LCD common driving signal output terminals. |
| 96 | COMMK | O | LCD Icon common driving signal output terminals. |

## ■ FUNCTIOAL DESCRIPTION

(1-1) Register

The **NJU6625** incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register (DR). The Register (IR) stores instruction codes such as “Clear Display” and “Cursor Shift” or address data for Display Data RAM (DDRAM), Character Generator ROM (CGRAM) and Icon Display RAM (MKRAM).
The Register (DR) is a temporary register, the data in the Register (DR) is written into the DDRAM, CGRAM or MK RAM.
The data in the Register (DR) written by the MPU is transferred automatically to the DDRAM, CGRAM or MKRAM by internal operation.
These two registers are selected by the selection signal RS as shown below.

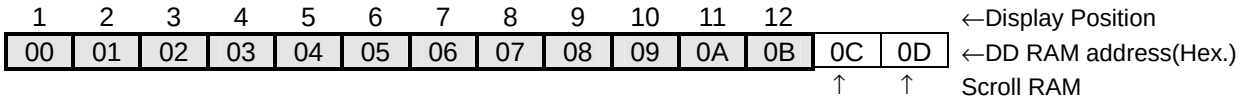
(1-2) Address Counter (AC)

The address counter (AC) addresses the DDRAM, CGRAM or MKRAM.
When the address setting instruction is written into the Register (IR), the address information is transferred from Register (IR) to the Counter (AC). The selection of either the DDRAM, CGRAM or MKRAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DDRAM, CGRAM or MKRAM, the Counter (AC) increments (or decrements) automatically.

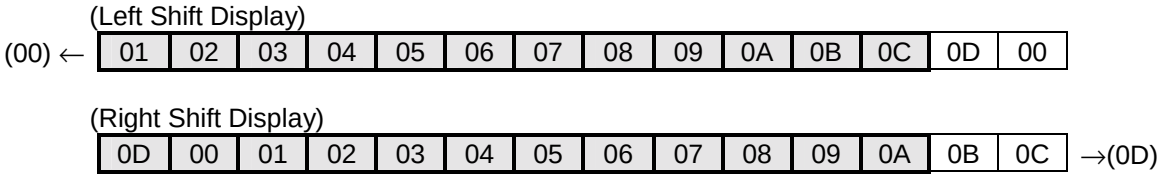
(1-3) Display Data RAM(DD RAM)

The Display Data RAM (DD RAM)consist of 14 x 8 bits stores up to 14-character display data represented in 8-bit code. (2 out of the 14-characters are used for scroll RAM.)
The DDRAM address data set in the address counter (AC) is represented in Hexadecimal.


The relation between DDRAM address and display position on the LCD is shown below.




When the display shift is performed, the DDRAM address changes as follows:



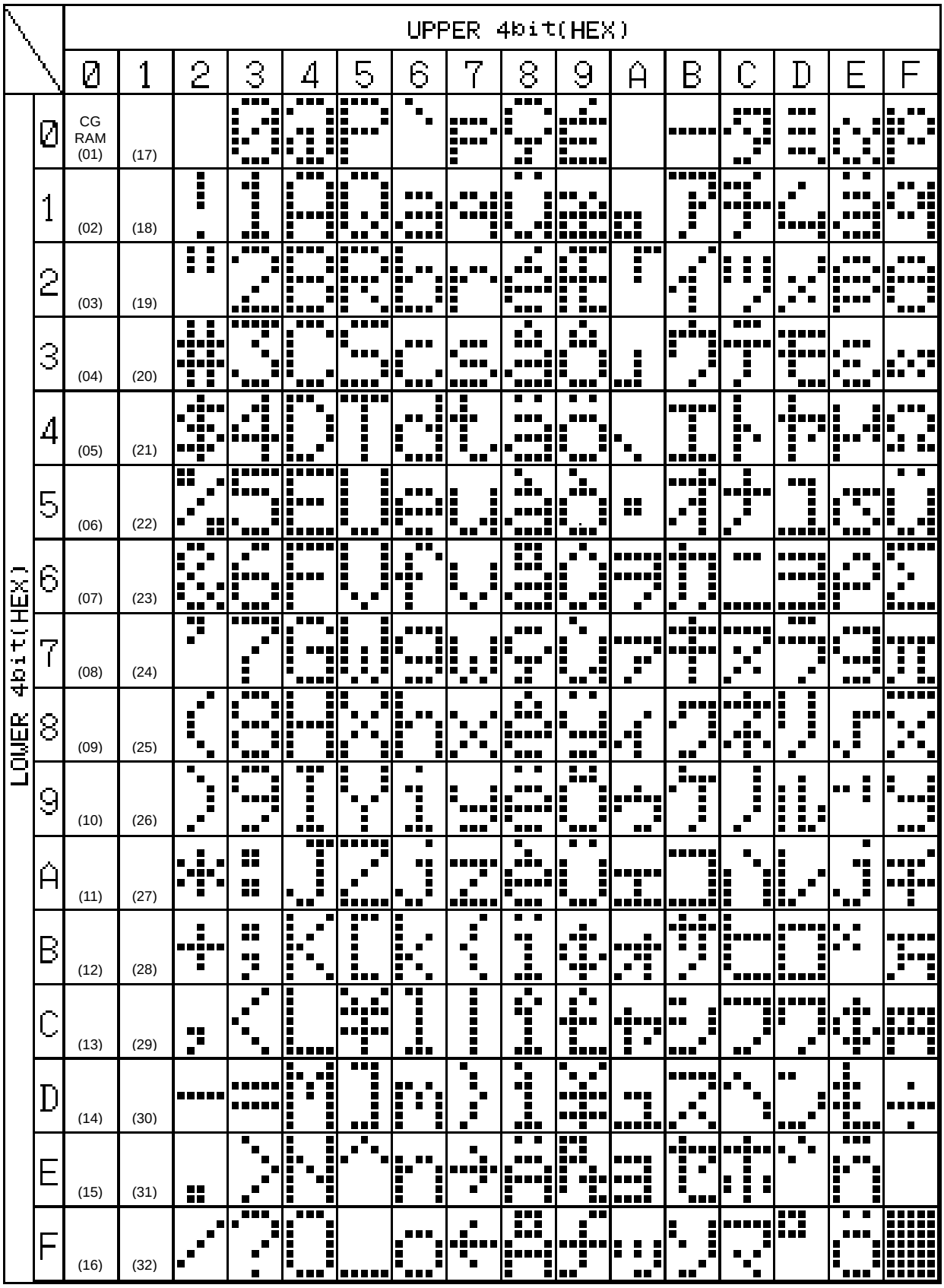

(1-4) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character code.

The storage capacity is up to 224 kinds of 5 x 7 dots character pattern (available address is $(20)_H$ through $(FF)_H$).

The correspondence between character code and standard character pattern of **NJU6625** is shown in Table 1. User-defined character patterns (Custom Font) are also available by mask option.

Table 1. CG ROM Character Pattern ( ROM version -02 )



(1-5) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 32 kind of character in 5 x 7 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$-$(1F)_H$ should be written to the DD RAM as shown in Table 1.

Table 2. shows the correspondence among the character pattern, CG RAM address and Data

Table 2. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern( 5 x 7 dots )

| Character Code (DD RAM Data) | CG RAM Address | | | Character Pattern (CG RAM Data) | |
|---|---|---|---|---|---|
| 7 6 5 4 3 2 1 0<br>← →<br>Upper bit Lower bit | 7 6 5 4 3 2 1 0<br>← →<br>Upper bit Lower bit | | | 4 3 2 1 0<br>← →<br>Upper bit Lower bit | |
| 0 0 0 0 0 0 0 0 | 0 0 0 0 0 | 0 0 0<br>0 0 1<br>0 1 0<br>0 1 1<br>1 0 0<br>1 0 1<br>1 1 0<br>1 1 1 | | 1 1 1 1 0<br>1 0 0 0 1<br>1 0 0 0 1<br>1 1 1 1 0<br>1 0 1 0 0<br>1 0 0 1 0<br>1 0 0 0 1<br>* * * * * | Character Pattern Example (1) |
| 0 0 0 0 0 0 0 1 | 0 0 0 0 1 | 0 0 0<br>0 0 1<br>0 1 0<br>0 1 1<br>1 0 0<br>1 0 1<br>1 1 0<br>1 1 1 | | 1 0 0 0 1<br>0 1 0 1 0<br>1 1 1 1 1<br>0 0 1 0 0<br>1 1 1 1 1<br>0 0 1 0 0<br>0 0 1 0 0<br>* * * * * | Character Pattern Example (2) |
| | | 0 0 0<br>0 0 1 | | | |
| • | • | • | | • | |
| • | • | • | | • | |
| • | • | • | | • | |
| • | • | • | | • | |
| • | • | • | | • | |
| 0 0 0 1 1 1 1 1 | 1 1 1 1 1 | 1 0 0<br>1 0 1<br>1 1 0<br>1 1 1 | | | Character Pattern Example (32) |

* Don't Care

Note) 1. Character code bit 0 to 4 correspond to the CG RAM address bit 3 to 7 (5bits:32 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is Don't care line. In case of input CG RAM data continuously, invalid address are Cursor position automatically.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code of DD RAM bits 5 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1-6) Icon Display RAM (MK RAM)

The **NJU6625** can display maximum 60 Icons.
The Icon Display can be controlled by writing the Data in MK RAM corresponds to the Icon.
The relation between MK RAM address and Icon Display position is shown below:

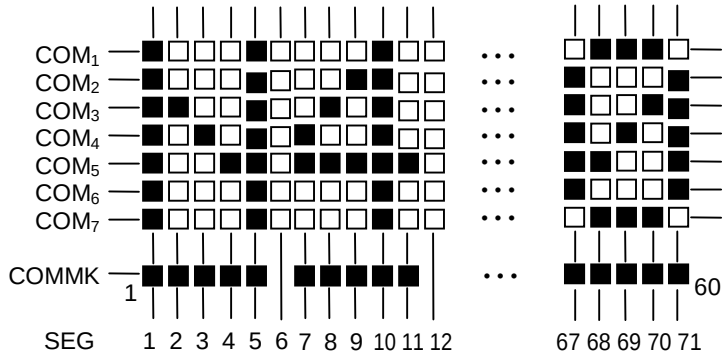



Table 3. Correspondence among Icon Position, MK RAM Address and Data

| MK RAM Address ($10_H$ to $1B_H$) | | Bits for Icon Display Position | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| 1 0000 | $10_H$ | 0 | 0 | 0 | “1” | “2” | “3” | “4” | “5” |
| 1 0001 | $11_H$ | 0 | 0 | 0 | “6” | “7” | “8” | “9” | “10” |
| 1 0010 | $12_H$ | 0 | 0 | 0 | “11” | “12” | “13” | “14” | “15” |
| 1 0011 | $13_H$ | 0 | 0 | 0 | “16” | “17” | “18” | “19” | “20” |
| : | : | : | | | | | | | |
| 1 1011 | $1B_H$ | 0 | 0 | 0 | “56” | “57” | “58” | “59” | “60” |

Note) There is no icon, on the segment terminals which are six times number of lines. (6th, 12th, 18th, 24th.... )

After power on or hardware reset, the data of MK RAM can not be initialized. To display Icons, the data of MKRAM need to be written in before display on. The displayed icons can not be shifted by Display Shift instruction. The MK RAM data at (1C)H and (1D)H address can not be used, became the address will be automatically increased, even the data was written into (1C)H and (1D)H, there is change of display.

(1-7) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

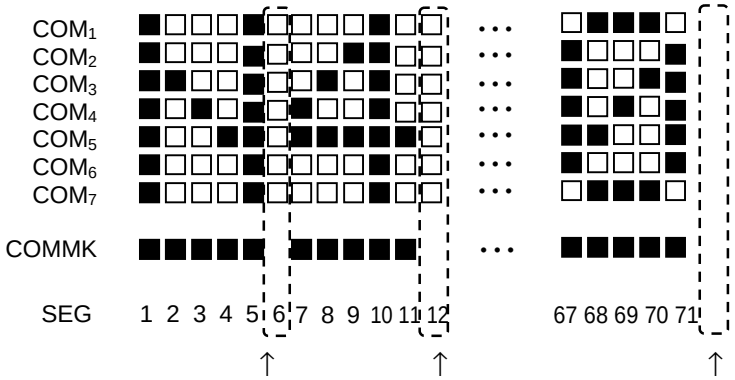
(1-8) LCD Driver

LCD Driver consists of 8-common driver and 71-segment driver.

The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

Note) Display

The **NJU6625** generate “SPACE” automatically on the segment terminals. Which are six times number of lines, regardless the smooth scroll function. In busy of the smooth scroll operation, this “SPACE” scrolls also with characters, there is no icon on the segment terminals which are six times number of lines.




“SPACE” is generated when data read out from CGROM or CGRAM

The loot number of segment is 71, so that “SPACE” is not here.

(1-9) Keyscan circuit

The Keyscan circuit consists of a detector block of key pressing and a fetching block of key status. It scans 4x8 key matrix and fetches conditions of 32 keys. Furthermore, it operates correctly against the key roll over input.

• Request signal output

When the **NJU6625** detect the key-in by the key scan circuit, it outputs "H" signal as the request signal from the "REQ" terminal to notice the key pressing information to an application system.
The request signal resets to "L" level before 2 clock of next scanning.

• Contents of key register renewal

Contents of key register are "0000 0000" in case of no key operation. Contents of key register are not changed in busy of key data reading operation. Key data is fetched into the key register after 2 clock of the end of a keyscan cycle and kept by the start of next cycle.

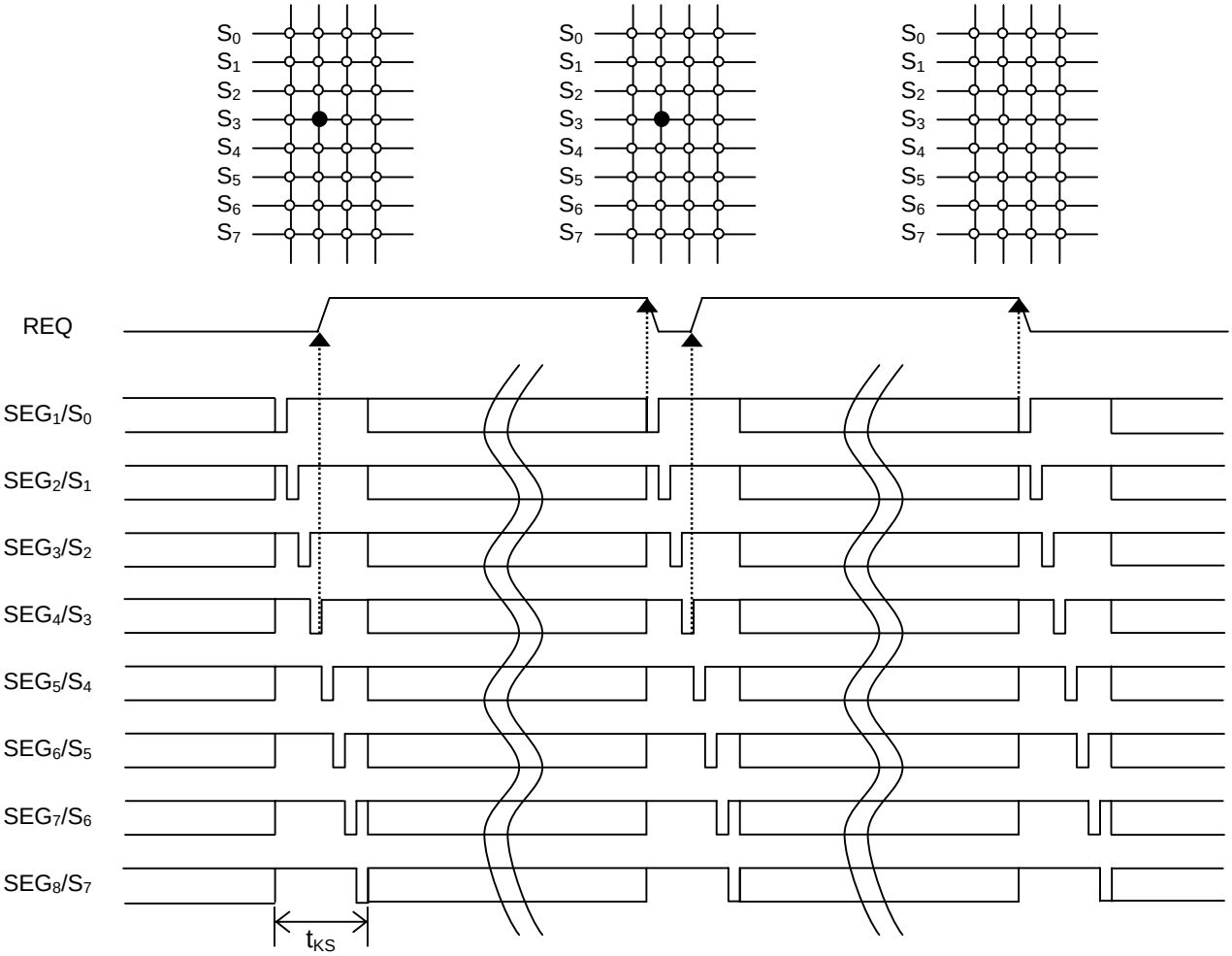
• Key data input terminal and segment terminal

Keyscan signal output terminals operate as segment terminals ($SEG_1$ to $SEG_8$) also and keyscan signals are output in interval period of segment signals. Key data input terminals ($K_0$ to $K_3$) are pulled up to $V_{DD}$ in busy of keyscan operation ($t_{KS}$). In this period, terminals of $SEG_9$ to $SEG_{71}$ output the voltage of $V_2$ or $V_{LCD2}$.

• Keyscan OFF mode

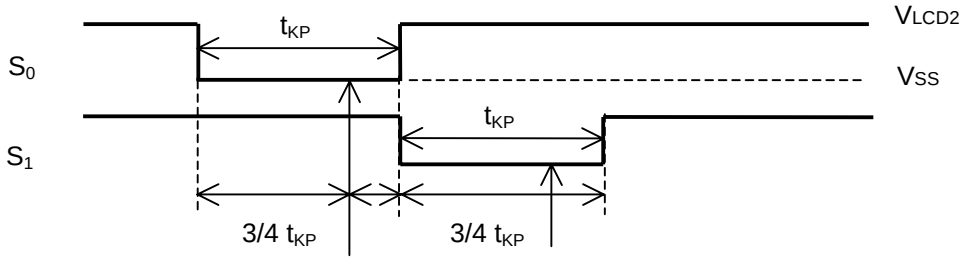
Keyscan operation is turned ON or OFF by the instruction. In case of keyscan OFF, the detector of key pressing is not operating and key data input terminals ($K_0$ to $K_3$) are not pulled up during the period of keyscan ($t_{KS}$). In the period of keyscan ($t_{KS}$), all of segment terminals ($SEG_1$ to $SEG_{71}$) output the voltage of $V_2$ or $V_{LCD2}$.

• Example Keyscan



• Key status fetching timing

Key status is fetched at third quarter of "L" period ($t_{KP}$) of scan signals ($S_0$ to $S_7$) as shown below:




Fetching timing

•Keyscan data format

Scaned 8-bit data of key are read out through the srial I/F.

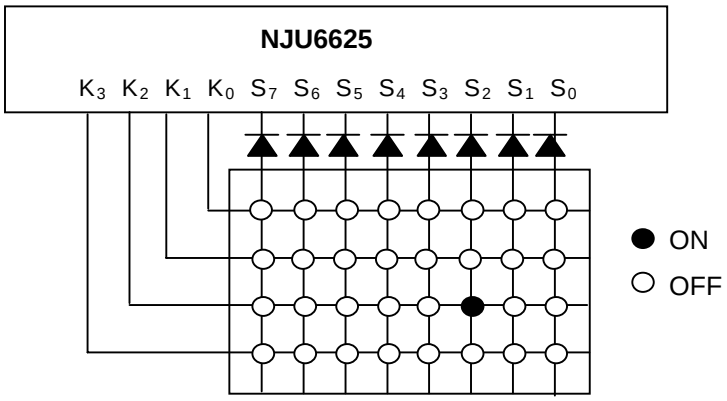
| $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | KL3 | KL2 | KL1 | KL0 | 0 | KH2 | KH1 | KH0 |
| | | | | | | | | ← | $K_3$ - $K_0$ | | → | | ← | $S_7$ - $S_0$ | → |

| Keyscan output data | KH2 | KH1 | KH0 |
|---|---|---|---|
| $S_7$ | 1 | 1 | 1 |
| $S_6$ | 1 | 1 | 0 |
| $S_5$ | 1 | 0 | 1 |
| $S_4$ | 1 | 0 | 0 |
| $S_3$ | 0 | 1 | 1 |
| $S_2$ | 0 | 1 | 0 |
| $S_1$ | 0 | 0 | 1 |
| $S_0$ | 0 | 0 | 0 |

When a key on the key matrix is pressed, the bit corresponding to terminals ($K_3$ to $K_0$, $S_7$ to $S_0$) connected the switch goes to "1" and another bits go to "0".

In case of Example 1, when the switch connecting to $K_2$ and $S_2$ is pressed, bit ($D_6$) corresponding to $K_2$ and bit ($D_1$) corresponding to $S_2$ go to "1" but another bits go to "0".

Example 1. One key is pressed



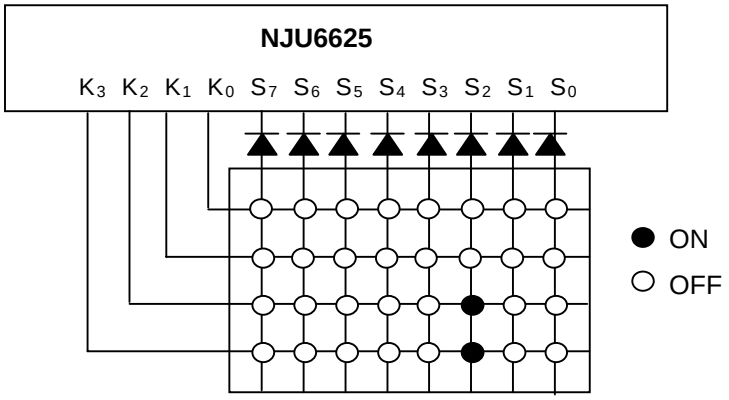

Read out data

| $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | ← | $K_3$ - $K_0$ | | → | | ← | $S_7$ - $S_0$ | → |

The key roll over input is the vertical line as shown below (Example 2) can be accepted with the keyscan circuit. But in case of Example 3, the key roll over input in the horizontal line can not be accepted.

The key roll over input must be taken care for key data judgement.

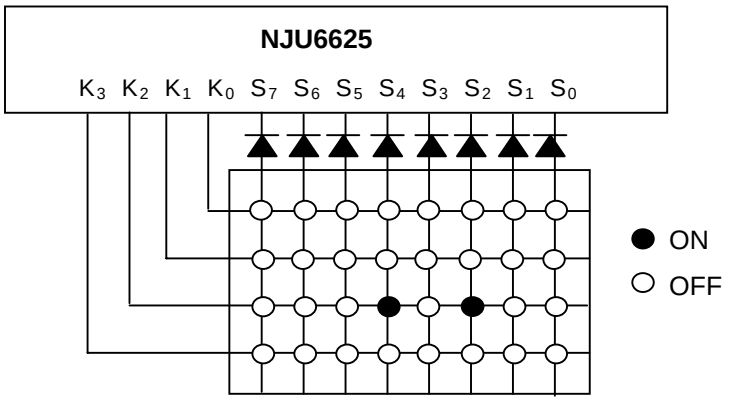
Example 2. The key roll over input (1)




Read out data

| $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| | | | | | | | | ← | $K_3$ - $K_0$ | → | | ← | $S_7$ - $S_0$ | → | |

Example 3. The key roll over input (2)

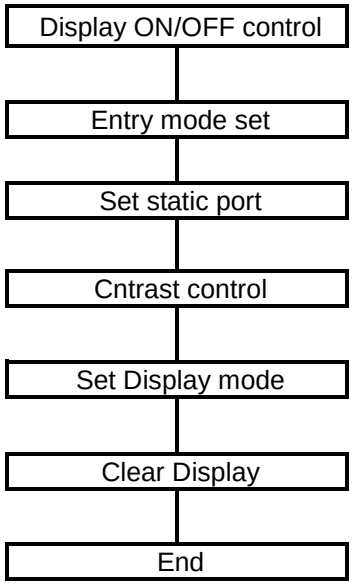



Note) In case of can not read out correct.

(2) Power on Initialization by internal circuits

(2-1) Initialization By Internal Reset Circuits

The **NJU6625** is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 1.5ms (fosc=145kHz) after $V_{DD}$ rises to 2.4V. Initialization flow is shown below:




D=0 Display OFF
M=0 Icon OFF
B=0 Cursor Blink OFF

I/D=1 Increment by 1
S=0 No Shift

P3-P0=0000 All static port output signal is “L”

E.V.R Value=0000 $V_{LCD}$ Low

K=1 Keyscan ON
DF=0 Release the power down mode

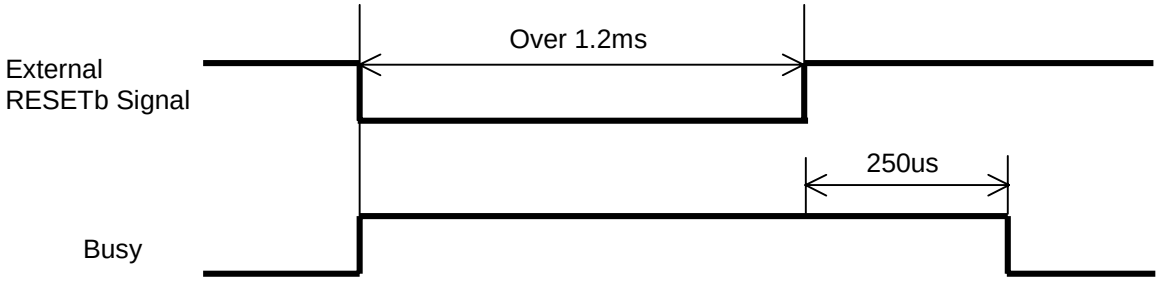
AC=$00_H$ Initialize the address counter to 00H
$20_H$ is written on DD RAM

Note) If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed. In this case the initialization by MPU software is required.

(2-2) Initialization By Hardware

The **NJU6625** incorporates RESETb terminal to initialize the all system. When the "L" level input over 1.2ms to the RESETb terminal, reset sequence is executed. In this time, busy signal output during 250us (fosc=145kHz) after RESETb terminal goes to "H". During this 250us period, any other instruction must not be input to the **NJU6625**.

- Timing Chart



(3) Instructions

The **NJU6625** incorporates two registers, an Instruction Register (IR) and a Data Register (DR).

These two registers store control information temporarily to allow interface between **NJU6625** and MPU or peripheral ICs operating different cycles.

Table 4. Table of Instructions

| Instruction | | Code | | | | | | | | | | | | | | | | Execute Time *1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
| (a) | Maker Testing | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | Test Data | | | | | | | | - |
| (b) | Clear Display | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | * | * | * | * | * | * | * | * | 234.48us |
| (c) | Return Home | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | * | * | * | * | * | * | * | * | 0us |
| (d) | Entry Mode Set | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | * | * | * | * | * | * | I/D | S | 0us |
| (e) | Display ON/OFF Control | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | * | * | * | * | * | D | M | B | 0us |
| (f) | Address Shift | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | * | * | * | * | * | * | * | ARL | 0us |
| (g) | Display Shift | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | * | * | * | * | * | * | * | DRL | 0us |
| (h) | Set Static Port | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | * | * | * | * | P3 | P2 | P1 | P0 | 0us |
| (i) | Contrast Control | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | * | * | * | * | E.V.R Value | | | | 0us |
| (j) | Dot Shift | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | * | * | * | * | * | Number of Dot Shift | | | 0us |
| (k) | Set Display Mode | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | * | * | * | * | * | * | K | PD | 0us |
| (l) | Set DD/MK RAM Address | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | * | * | * | DD RAM $(00 \text{ to } 0D)_H$<br>MK RAM $(10 \text{ to } 1D)_H$ | | | | | 0us |
| (m) | Set CG RAM Address | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | CG RAM $(00 \text{ to } FE)_H$ | | | | | | | | 0us |
| (n) | Write DD RAM Data | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | Write Data (DD RAM) | | | | | | | | 41.38us |
| | Write MK RAM Data | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | * | * | Write Data (MK RAM) | | | | | 41.38us |
| | Write CG RAM Data | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | * | * | Write Data (CG RAM) | | | | | 41.38us |
| (o) | Read Keyscan Data | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | Key Data | | | | | | | | 0us |

*1 $f_{OSC}$=145KHz. If the oscillation frequency is changed, the execution time is also changed.

(3-1) Description of each instructions

(a) Maker Test

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | * | * | * | * |

*: Don't care

This code is using for device testing mode (only for maker).
Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".
(Especially please check the output condition of Enable signal when the power turns on.)

(b) Clear Display

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | * | * | * | * | * | * | * | * |

When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set to increment. The S of entry mode does not change.

Note) The character pattern for character code $(20)_H$ must be blank code in the user-defined character
pattern (Custom font).

(c) Return Home

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | * | * | * | * | * | * | * | * |

Return home instruction is executed, the DD RAM address $(00)_H$ is set into the address counter. Display is returned its original position if shifted. The DD RAM contents do not change.

(d) Entry Mode Set

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | * | * | * | * | * | * | I/D | S |

Entry mode set instruction which sets the address moving direction and display shift On/Off, is executed when the codes of (I/D) and (S) are written into $DB_1$(I/D) and $DB_0$(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the whole display shift in the DD RAM writing.

| I/D | Function |
|---|---|
| 1 | Address increment : The address of the DD RAM or MK RAM or CG RAM increment(+1) when the write. |
| 0 | Address decrement : The address of the DD RAM or MK RAM or CG RAM decrement(-1) when the write. |

| S | Function |
|---|---|
| 1 | Whole display shift.<br>The shift direction is determined by I/D. : Shift to the left at I/D=1 and shift to the right at the I/D=0.<br>The display does not shift when writing into CG RAM, MK RAM |
| 0 | The display does not shift. |

(e) Display ON/OFF Control

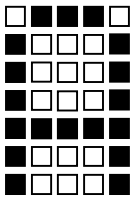
| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | * | * | * | * | * | D | M | B |

Display On/Off control instruction which controls the whole display On/Off and the addressed position character blink, is executed when the codes of (D) and (B) are written into $DB_2$(D) and $DB_0$(B), as shown below.

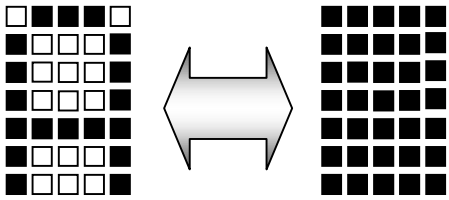
| D | Function |
|---|---|
| 1 | Display On. |
| 0 | Display Off. In the mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1. |

| M | Function |
|---|---|
| 1 | Icon display ON. |
| 0 | Icon display OFF. |

| B | Function |
|---|---|
| 1 | The addressed position character is blinking. Blinking rate is 500ms at $f_{OSC}$=145kHz.<br>The cursor and the blink can be displayed simultaneously. |
| 0 | The character does not blink. |



Character Font 5 x 7 dots
(1) Cursor display example



Alternating display
(2) Blink display example

When the number of dot-shift is not set “0” in (j) Dot shift instruction, the blink operation will be appeared at the irregular position.

(f) Address Shift

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | * | * | * | * | * | * | * | ARL |

The Address shift instruction shifts the Address to the right or left without writing or reading display data.

| ARL | Function |
|---|---|
| 0 | Shift the address position to the left ((AC) is decremented by 1) |
| 1 | Shift the address position to the right ((AC) is incremented by 1) |

(g) Display Shift

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | * | * | * | * | * | * | * | DRL |

The Display shift instruction shifts the Display to the right or left without writing or reading display data. The contents of address counter (AC) does not change by operation of the display shift only.

| DRL | Function |
|---|---|
| 0 | Shifts the whole display to the left and the cursor follows it. |
| 1 | Shifts the whole display to the right and the cursor follows it. |

(h) Static Port Set

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | * | * | * | * | P3 | P2 | P1 | P0 |

It sets Static Output Port signal which can drive LED directly like as indicator. Initial status is “L”.

(i) Contrast Contol

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | * | * | * | * | C3 | C2 | C1 | C0 |

Contrast Control instruction which adjusts the contrast of the LCD is executed when the code "1" is written into $D_6$ and the codes of C3 to C0 are written into $D_3$ to $D_0$ as shown below.
The contrast of LCD can be adjusted one of 16 voltage-stages by setting this 4-bit register.
See (4-1) "how to adjust the Contrast of LCD".
Set the binary code "0,0,0,0" when contrast adjustment is unused.

| C3 | C2 | | C1 | C0 | $V_{LCD}$ |
|---|---|---|---|---|---|
| 0 | 0 | | 0 | 0 | Low |
| | | : | | | |
| | | : | | | |
| 1 | 1 | | 1 | 1 | High |

$V_{LCD}=V_{LCD2}-V_{SS}$

(j) Dot Shift

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | * | * | * | * | * | SC2 | SC1 | SC0 |

The dot shift instruction sets shift line and the number of dot-shift.

Conbination of this instruction and the Display shift instruction realize the horizontal smooth scroll. Refer to the following table.

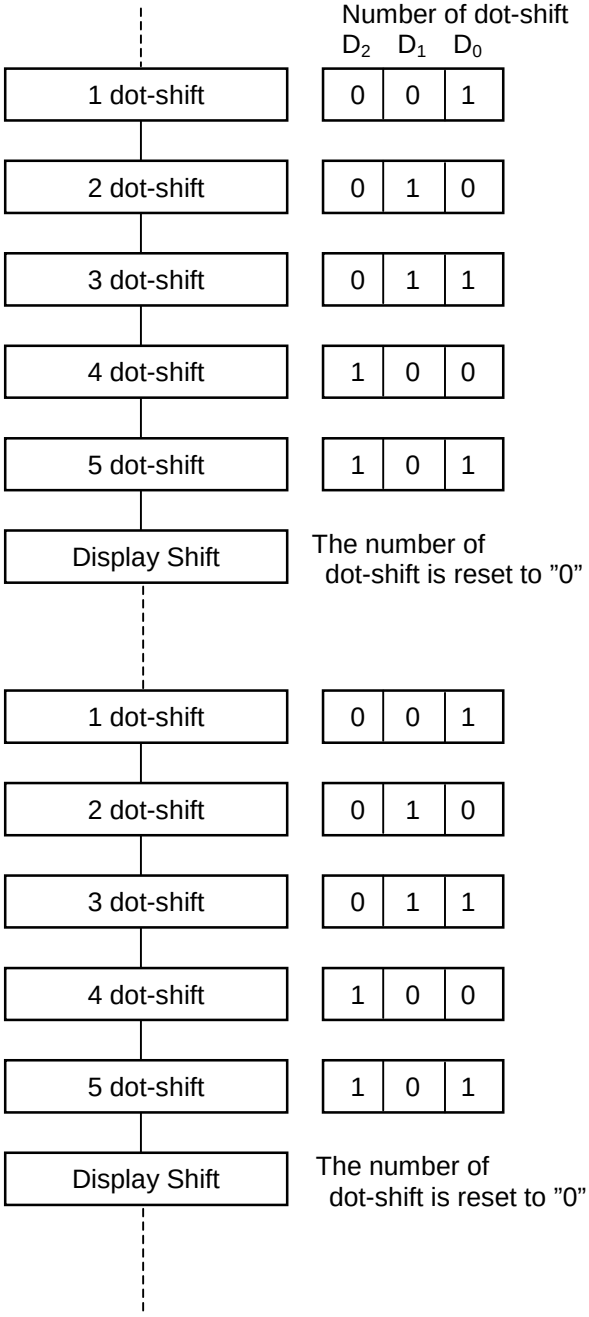
| SC2 | SC1 | SC0 | Function |
|---|---|---|---|
| 0 | 0 | 0 | No shift. |
| 0 | 0 | 1 | 1 dot-shift to the left. |
| 0 | 1 | 0 | 2 dot-shift to the left. |
| 0 | 1 | 1 | 3 dot-shift to the left. |
| 1 | 0 | 0 | 4 dot-shift to the left. |
| 1 | 0 | 1 | 5 dot-shift to the left. |
| 1 | 1 | 0 | Don't Care. |
| 1 | 1 | 1 | |

Note 1) Set 1/D=1, S=0, in the entry mode set, for the line using the smooth scroll function.
Note 2) The number of dot-shift is reset to "0" by the execution of the Display Shift instruction.
Note 3) Only character is shifted by Dot shift instruction.

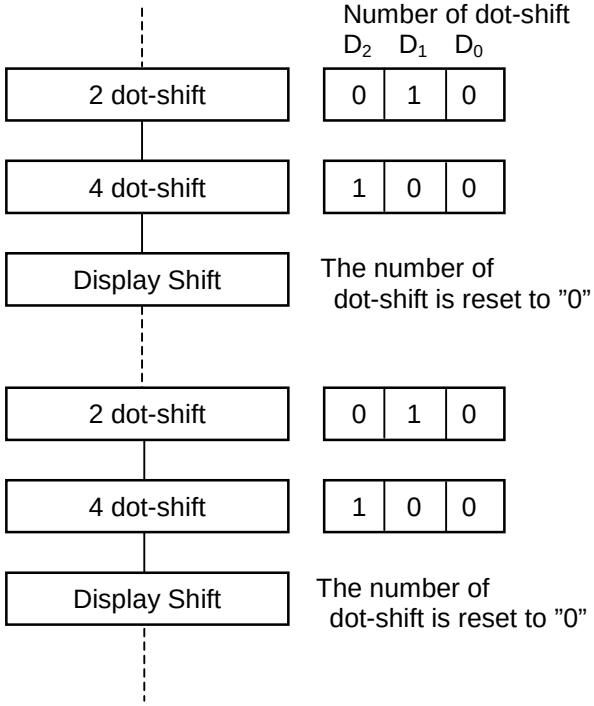
•Smooth scroll sequence

One out of the following three types of smooth scroll can be selectd by the instructions.

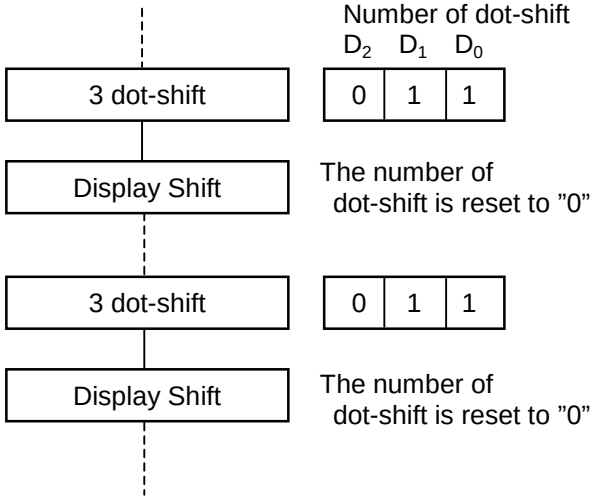
**1 dot smooth scroll**




**2 dot smooth scroll**

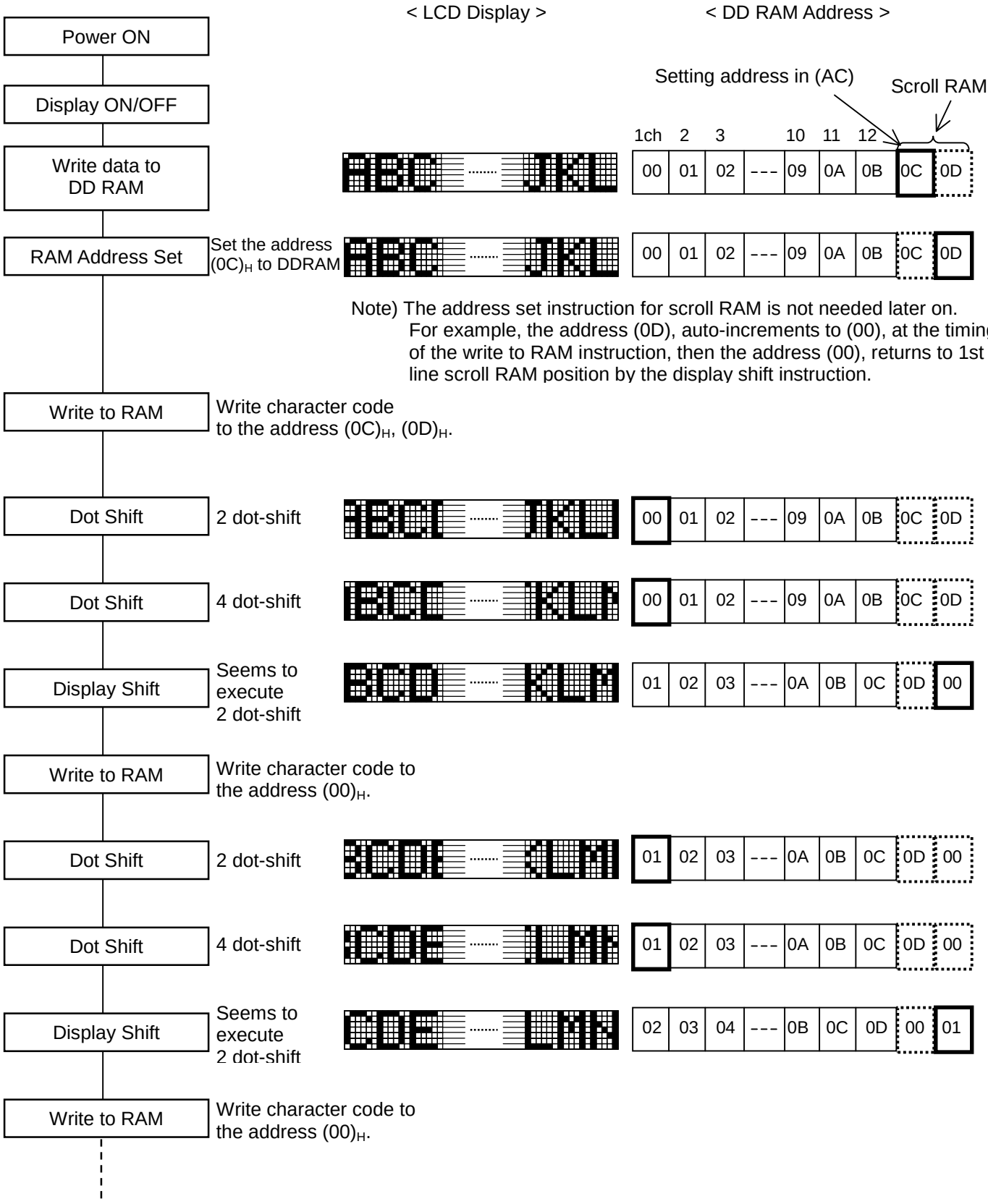



**3 dot smooth scroll**



• Example of 2 dot smooth scroll

The smooth scroll sequence, which is executed by the 2 dot-shift and 4 dot-shift instruction, LCD display and DD RAM address movement are shown as follows.



(k) Set Display Mode

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | * | * | * | * | * | * | K | PD |

The Set Display Mode instruction control the function of keyscan and power down mode.

| K | Function |
|---|---|
| 1 | Keyscan ON |
| 0 | Keyscan OFF<br>In busy of keyscan ($t_{KS}$), all of segment terminal ($S_0$ to $S_7$) output the voltage of $V_2$ of $V_{LCD2}$. |

| PD | Function |
|---|---|
| 1 | Power down mode.<br>All common and segment terminal set the voltage level of $V_{LCD2}$. |
| 0 | Release the power down mode. |

In busy of Power down mode, do not input any instructions except for release the power down mode.
The power down mode should be set before power off because any irregular display appearance at power off is prevented.

• The key scan operation when switching to the power down mode during key scan
When switching to the power down mode during key scan operation, it stops key scan operation in the period and after power down mode cancellation too.
After power down mode cancellation, the REQ signal maintains "H" when detects key-in signal before switches to power down mode and REQ signal rises to "H".
However, the key scan operation becomes invalid data even if it reads key-in data because it stopped. The key data becomes to valid with the key scan by the next key scan of frame.

(l) Set DD/MK RAM Address

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | * | * | * | AD4 | AD3 | AD2 | AD1 | AD0 |

The address data ($D_4$ to $D_0$) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing is performed into the addressed DD/MK RAM.
The RAM includes DD RAM and MK RAM, and these RAMs are shared by address as shown below.

| | RAM Address |
|---|---|
| DD RAM : | $(00)_H$ to $(0D)_H$ |
| MK RAM : | $(10)_H$ to $(1D)_H$ |

(m) Set CG RAM Address

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | AC7 | AC6 | AC5 | AD4 | AD3 | AD2 | AD1 | AD0 |

The CG RAM address set instruction is executed when the "H" level input to the AC terminal and the address is written into $D_7$ to $D_0$ as shown above.
The address data ($D_7$ to $D_0$) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing is performed into the addressed RAM.
The RAM includes CG RAM address as shown below.

| | RAM Address |
|---|---|
| CG RAM : | $(00)_H$ to $(FE)_H$ |

(n) Write Data to CG, DD or MK RAM

- Write Data to DD RAM

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | DD7 | DD6 | DD5 | DD4 | DD3 | DD2 | DD1 | DD0 |

- Write Data to MK RAM

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | * | * | DM4 | DM3 | DM2 | DM1 | DM0 |

- Write Data to CG RAM

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | * | * | DC4 | DC3 | DC2 | DC1 | DC0 |

By the execution of this instruction, the binary 8-bit data ($A_7$ to $A_0$) are written into the DD RAM, and the binary 5-bit data ($A_4$ to $A_0$) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment (+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

However, the data in MK RAM $(1C)_H$ and $(1D)_H$ are not displayed, bat the automatic address increment is performed. And the display is not changed by the data written into MK RAM $(1C)_H$ and $(1D)_H$

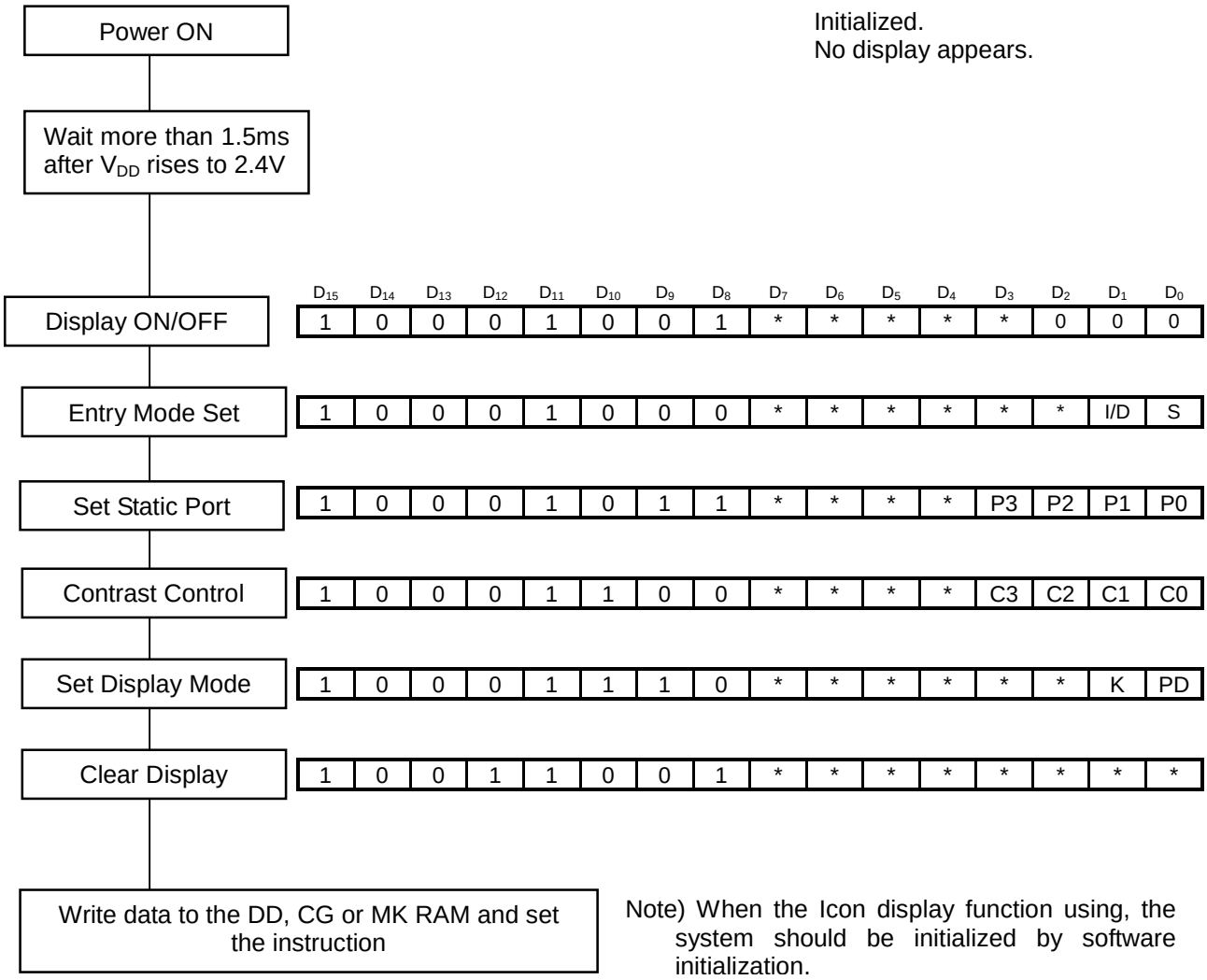
(o) Read Data Key

| | $D_{15}$ | $D_{14}$ | $D_{13}$ | $D_{12}$ | $D_{11}$ | $D_{10}$ | $D_9$ | $D_8$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | KL3 | KL2 | KL1 | KL0 | 0 | KH2 | KH1 | KH0 |
| | ← Input → | | | | | | | | ← Output → | | | | | | | |

Read data key is a instruction for data reading out of keyscan. However, the bit 8 to 15 are input data. After this 8-bit data were input, the operation change to output from input at the falling edge of 8th SCK clock.

(3-2) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not satisfied, the **NJU6625** must be initialized by the instruction.




Note) When the Icon display function using, the system should be initialized by software initialization.

(4) LCD display

(4-1) Bleeder Resistance

Each LCD driving voltage ( $V_1$, $V_2$, $V_3$, $V_4$ ) is LCD driving high voltage input to the $V_{LCD1}$ terminal, generated by the E.V.R. and high impedance bleeder resistance.

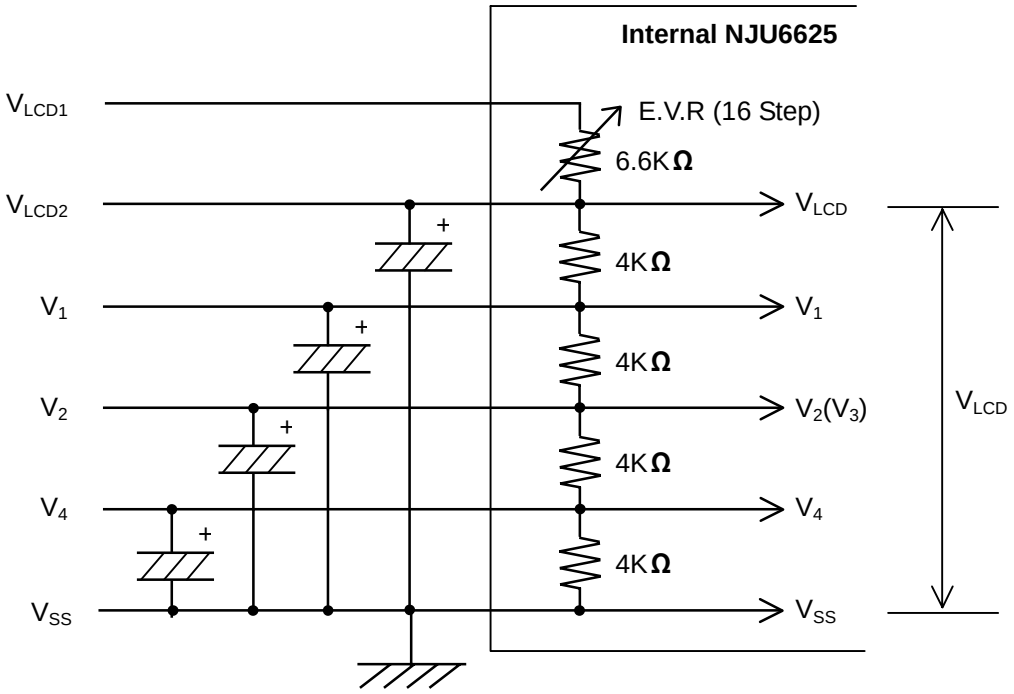
The bleeder resistance is set 1/4 bias suitable for 1/8 duty ratio.

The capacitor connected between $V_{LCD2}$ / $V_1$/ $V_2$/ $V_4$ and $V_{SS}$ is needed for stabilizing $V_{LCD}$. The determination of the each capacitance requires to operate with the LCD panel actually.

LCD Driving Voltage vs Duty Ratio

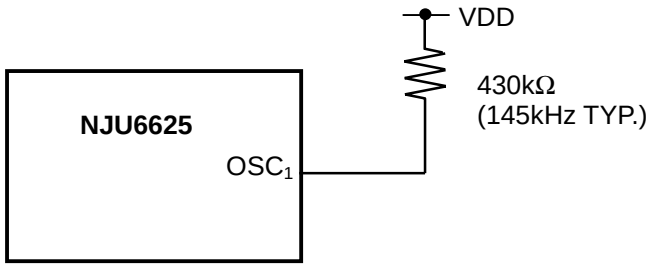
| Power supply | Duty Ratio | 1/8 |
|---|---|---|
| | Bias | 1/4 |
| $V_{LCD}$ | | $V_{LCD2}$ - $V_{SS}$ |

$V_{LCD}$ is the maximum amplitude for LCD driving voltage.




(4-2) Oscillation Circuit

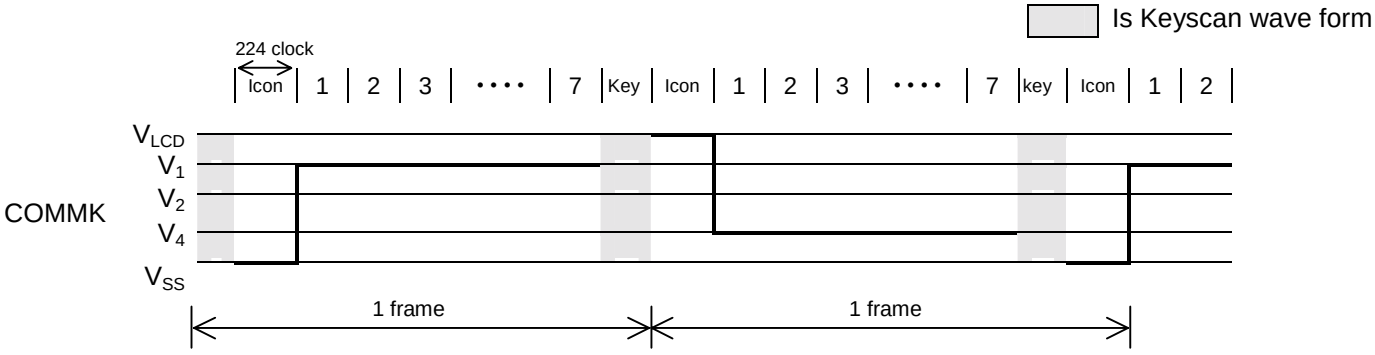
A resistor is connected to $OSC_1$ pin to configure the oscillation circuit. External clock can also be inputted through the $OSC_1$ pin.



(4-3) Relation between oscillation frequency and LCD frame frequency

As the **NJU6625** incorporate oscillation capacitor and resistor for CR oscillation, 145kHz oscillation is available without any external components.

The LCD frame frequency example mentioned below is based on 145kHz oscillation.(1clock =6.90us)

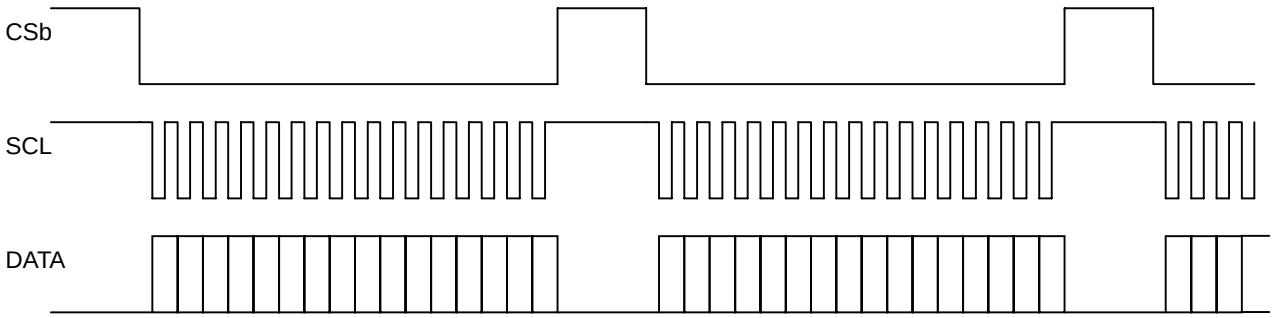



1 frame = 6.90(us) x 224 x 8 = 12.36(ms)
Frame frequency = 1 / 12.36(ms) = 79.50(Hz)
Keyscan time = 220.70(us)

(5) Interface with MPU

The instructions and data are communicated with the serial port which is a clock synchronization type based on 16-bit per word.

The **NJU6625** can be controlled by the serial data as shown below.




The serial interface circuit operates in CSb=L.

A communication unit consists of 16-bit data. The communication period is from the falling edge of CSb terminal to the rising edge. The inputs data and latched at rising edge of shift clock (SCL) and the first 16-bit data are fetched into the **NJU6625** at the rising edge of chip select (CSb). The data over than 16 bits are ignored. If the input data are less than 16 bits, they are ignored at the rising edge of "CSb". Therefore, just 16 bits data should be input for the correct communication. In case of RAM data input, the RAM address is changed automatically as increment or decrement.

The data to input is MSB first. Although the output data is just only key scan, data bits $D_8$ to $D_{15}$ in the key data read out instruction are input. After these 8-bit instruction is input, this serial data input terminal is changed to the output terminal at the 8th falling edge of SCL clock.

The electrical short between the **NJU6625** and external circuit must be prevented in the application.

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

| PARAMETER | SYMBOL | RATINGS | UNIT | NOTE |
|---|---|---|---|---|
| Supply Voltage (1) | $V_{DD}$ | -0.3 to +7.0 | V | |
| Supply Voltage (2) | $V_{LCD1}$ | $V_{DD}$+10.5 to $V_{SS}$+0.3 | V | $V_{LCD1}$ Terminal |
| Input Voltage | $V_t$ | -0.3 to $V_{DD}$+0.3 | V | |
| Operating Temperature | $T_{opr}$ | -40 to +85 | °C | |
| Storage Temperature | $T_{stg}$ | -55 to +125 | °C | |
| Power Dissipation | PD | 500 | mW | |

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause mal function and poor reliability.

Note 2) Decoupling capacitor should be connected between $V_{DD}$ and $V_{SS}$, $V_{LCD1}$-$V_{SS}$due to the stabilized operation for the Voltage converter.

Note 3) All voltage values are specified as $V_{SS}$ = 0V
The relation : $V_{LCD1} \geq V_{LCD2} > V_{DD} > V_{SS}$, $V_{SS}$=0V must be maintained.

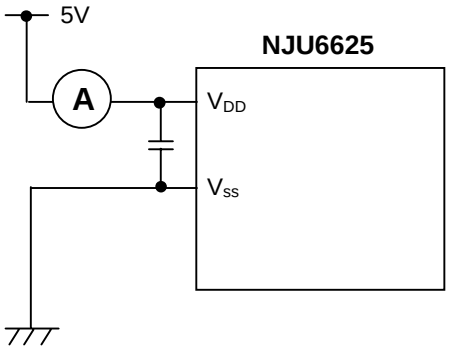
## ■ ELECTRICAL CHARACTERISTICS

($V_{DD}$=4.5V to 5.5V、Ta= -40 to +85°C)

| PARAMETER | | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|
| Input Voltage (1) | | $V_{IH1}$ | | 0.8$V_{DD}$ | - | $V_{DD}$ | V | 4 |
| | | $V_{IL1}$ | | $V_{SS}$ | - | 0.2$V_{DD}$ | | |
| Input Voltage (2) | | $V_{IH2}$ | | 0.8$V_{DD}$ | - | $V_{LCD1}$ | V | 5 |
| | | $V_{IL2}$ | | $V_{SS}$ | - | 0.2$V_{DD}$ | | |
| Output Voltage | | $V_{OH}$ | -$I_{OH}$=2mA,$V_{DD}$=5.0V | 4.0 | - | - | V | 6 |
| | | $V_{OL}$ | $I_{OL}$=2mA,$V_{DD}$=5.0V | - | - | 0.5 | | |
| Driver On-resist. (COM) | | $R_{COM}$ | ±Id=1uA(COM Terminal) $V_O$=$V_{LCD}$, $V_{SS}$, $V_1$, $V_4$ | - | - | 40 | kΩ | 8 |
| Driver On-resist. (SEG) | | $R_{SEG}$ | ±Id=1uA(SEG Terminal) $V_O$=$V_{LCD}$, $V_{SS}$, $V_2$ | - | - | 40 | kΩ | 8 |
| Pull-up MOS Current 1 | | -$I_{p1}$ | $V_{DD}$=5V | 5 | 25 | 50 | uA | 5 |
| Pull-up MOS Current 2 | | -$I_{p2}$ | $V_{DD}$=5V | 10 | 25 | 50 | uA | 5 |
| Input Leakage Current | | $I_{LI}$ | $V_{IN}$=0 to $V_{DD}$ | -1.0 | - | 1.0 | uA | 10 |
| Operating Current | | $I_{DD1}$ | $V_{DD}$=5V, $f_{OSC}$=145kHz Display, Keyscan ON, Ta=25°C | - | - | 500 | uA | 7 |
| | | $I_{DD2}$ | $V_{DD}$=5V, Stand-by mode, Ta=25°C | - | 7 | 10 | uA | 7 |
| Bleeder resistance circuit | LCD Driving Voltage | $V_1$ | E.V.R Value : "1111" $V_{LCD1}$ - $V_{SS}$=8.0V | 5.8 | 6.0 | 6.2 | V | |
| | | $V_2$ | | 3.8 | 4.0 | 4.2 | | |
| | | $V_4$ | | 1.8 | 2.0 | 2.2 | | |
| | Bleeder resistance $RB=(V_{LCD}-V_{SS})/IB$ | RB | E.V.R Value : "1111" $V_{LCD1}$ - $V_{SS}$=8.0V, Ta=25°C | 11.2 | 16.0 | 20.8 | kΩ | |
| Internal Oscillation Frequency | | $f_{OSC}$ | $V_{DD}$=5V, Ta=25°C Rosc=430kΩ | 72 | 145 | 218 | kHz | |
| External Clock Frequency | | $f_{CP}$ | Input from $OSC_1$ | 144 | 290 | 436 | kHz | 11 |
| External Clock Duty | | Duty | Input from $OSC_1$ | 45 | 50 | 55 | % | |
| LCD Display Voltage | | $V_{LCD1}$ | $V_{LCD1}$ Terminal, $V_{SS}$=0V | $V_{DD}$ | - | 10.0 | V | 9 |
| $V_{LCD1}$ Current | | $I_{LCD1}$ | $V_{LCD1}$-$V_{SS}$=8.0V, Ta=25°C | - | - | 1 | mA | |

Note 4) Apply to the $OSC_1$, SCL, DATA, CSb, RESETb Terminals.
Note 5) "Pull-up MOS Current 1" : Apply to the DATA Terminals.
"Pull-up MOS Current 2" and "Input Voltage 2" : Apply to the $K_0$ to $K_3$ Terminals.
Note 6) Apply to the $P_0$ to $P_3$, REQ, DATA Terminals.
Note 7) If the input level is medium, current consumption will increase due to the penetration current. Therefore,
the input level must be fixed to "H" or "L".

- Operating Current Measurement Circuit




Note 8) $R_{COM}$ and $R_{COM}$ are the resistance values between power supply terminals ($V_{SS}$, $V_{LCD2}$ or $V_1$,$V_2$,$V_4$) and each common terminal ($COM_1$ to $COM_7$/COMMK) and supply voltage ($V_{SS}$, $V_{LCD2}$ or $V_1$,$V_2$,$V_4$) and each segment terminal ($SEG_1$ to $SEG_{71}$) respectively, and measured when the current Id is flown on every common and segment terminals at a same time.
Note 9) Apply to the output voltage from each COM and SEG are less than +0.15V against the LCD driving constant voltage ($V_{DD}$, $V_{LCD1}$) at no load condition.
Note 10) Apply to the SCL, CSb, RESETb Terminals.
Note 11) The external clock frequency is half divided by the built-in frequency divider, therefore the frame frequency is as the same as when the internal oscillation circuit is used.

## ■ Bus timing characteristics

• Serial Interface Sequence

($V_{DD}$=4.5V to 5.5V、$V_{LCD1}$=$V_{SS}$+8.0V、Ta=-40 to +85°C)

| PARAMETER | SYMBOL | MIN | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|
| Serial clock cycle time | $t_{CYCE}$ | 1 | - | us | Fig.1 |
| Serial clock width | $t_{SC}$ | 300 | - | ns | Fig.1 |
| Chip select pulse width | $PW_{CS}$ | 100 | - | us | Fig.1 |
| Chip select set up time | $t_{CSU}$ | 300 | - | ns | Fig.1 |
| Chip select hold time 1 | $t_{CHI}$ | 300 | - | ns | Fig.1 |
| Serial input data set up time | $t_{SISU}$ | 300 | - | ns | Fig.1 |
| Serial input data hold time | $t_{SIH}$ | 300 | - | ns | Fig.1 |
| Key data output delay time | $t_{KDD}$ | - | 300 | ns | Fig.2 |
| Data port direction change time from input to output | $t_{SRWD}$ | - | 300 | ns | Fig.2 |
| Data port direction change time From output to input | $t_{CRWD}$ | - | 300 | ns | Fig.2 |
| Chip select hold time 2 | $t_{CH2}$ | 1 | - | us | Fig.2 |

Fig.1 Input Data Sequence

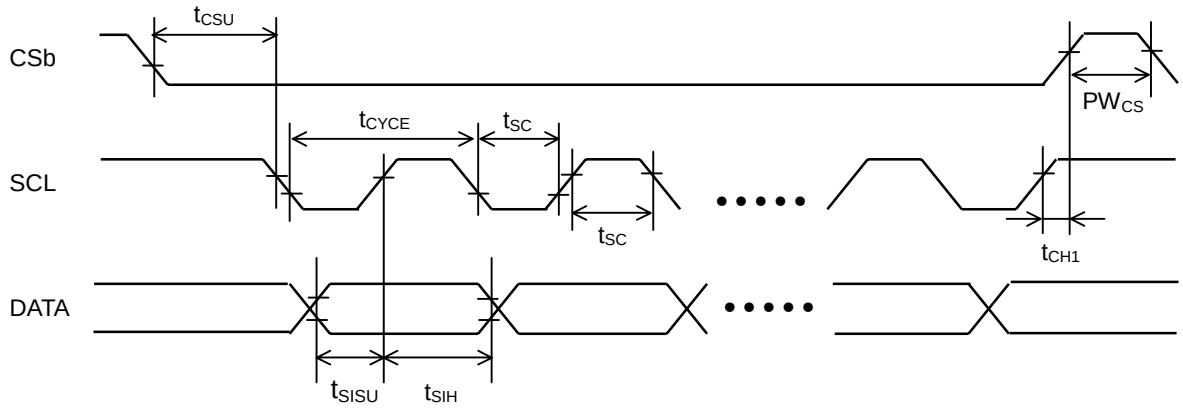
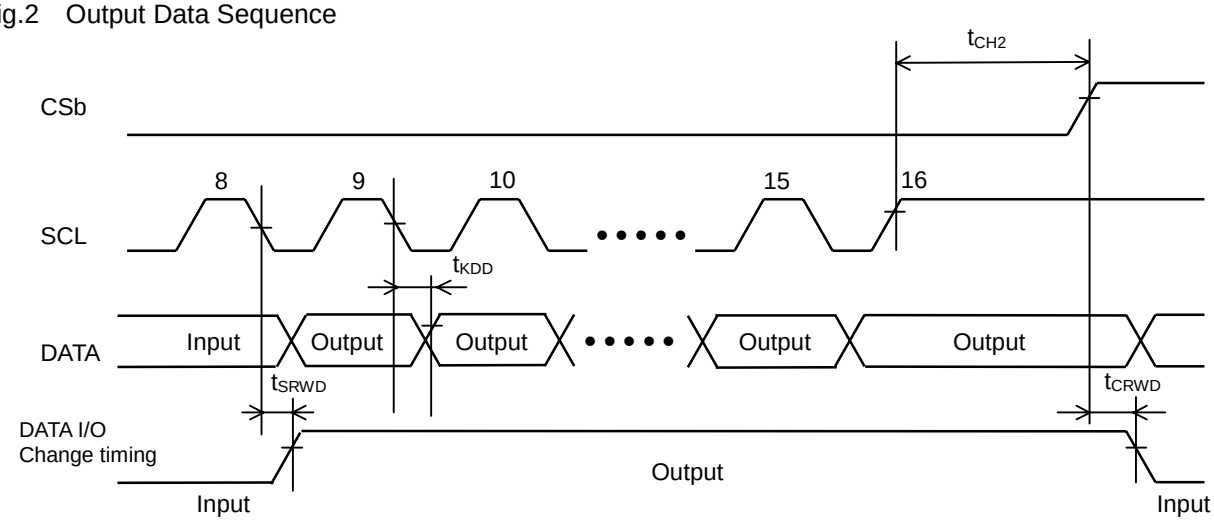


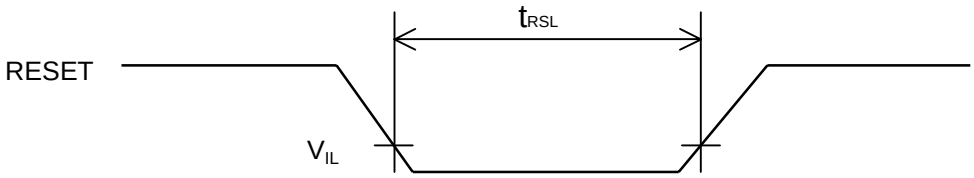

Fig.2 Output Data Sequence



• The Input Condition when using the Hardware Reset Circuit

(Ta=25°C)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Reset input "L" level width ($f_{OSC}$=145KHz) | $t_{RSL}$ | 1.2 | - | - | ms | |

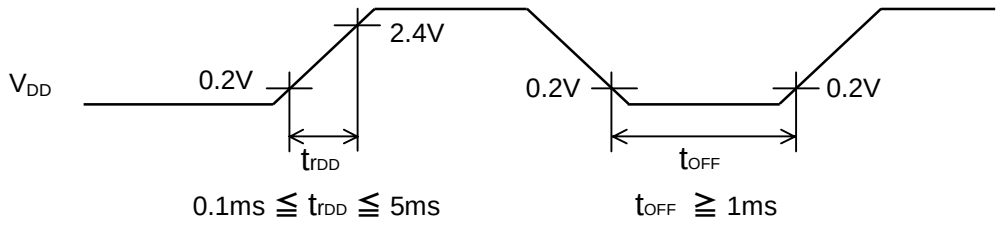



• Power Supply Condition when using the internal initialization circuit

(Ta=25°C)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Power supply rise time | $t_{rDD}$ | 0.1 | - | 5 | ms | |
| Power supply OFF time | $t_{OFF}$ | 1 | - | - | ms | |

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction. (Refer to initialization by the instruction)

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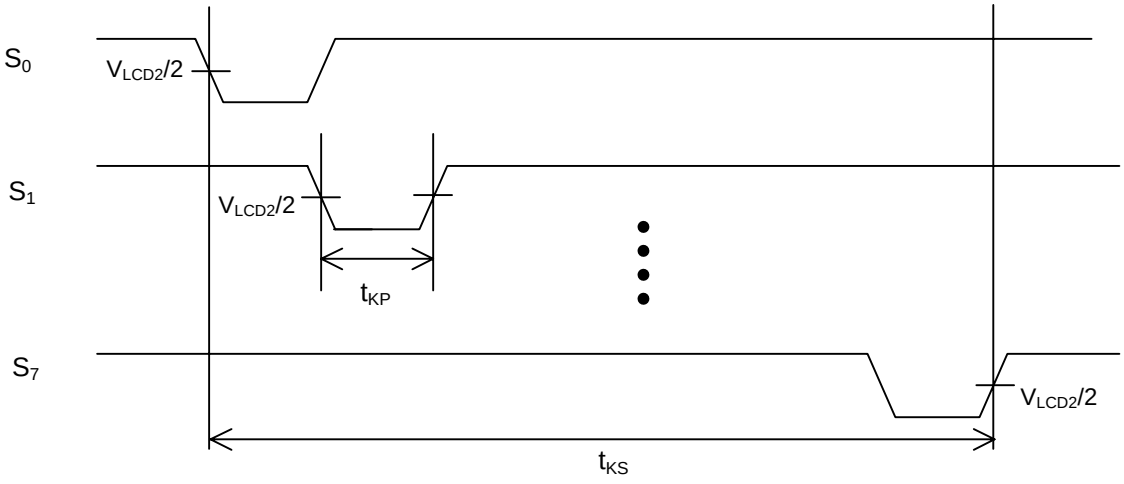
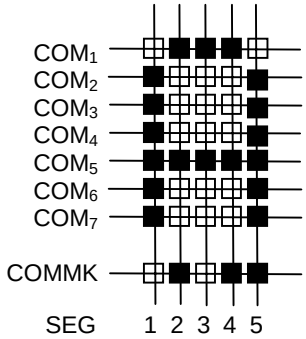
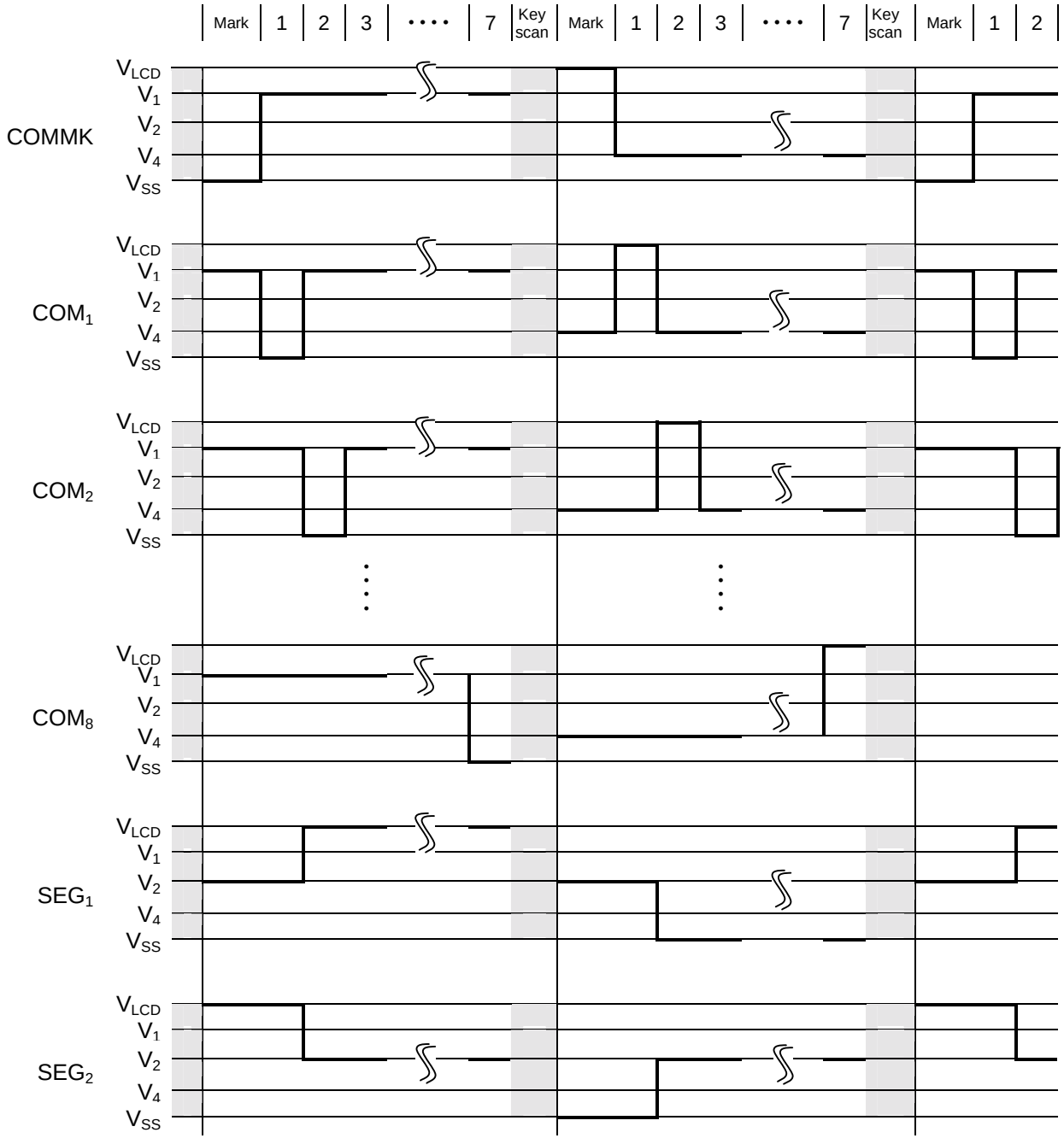
($f_{OSC}$=145KHz)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|
| Keyscan time | $t_{KS}$ | - | 221 | - | us | |
| Keyscan palse width | $t_{KP}$ | - | 27.6 | - | us | |



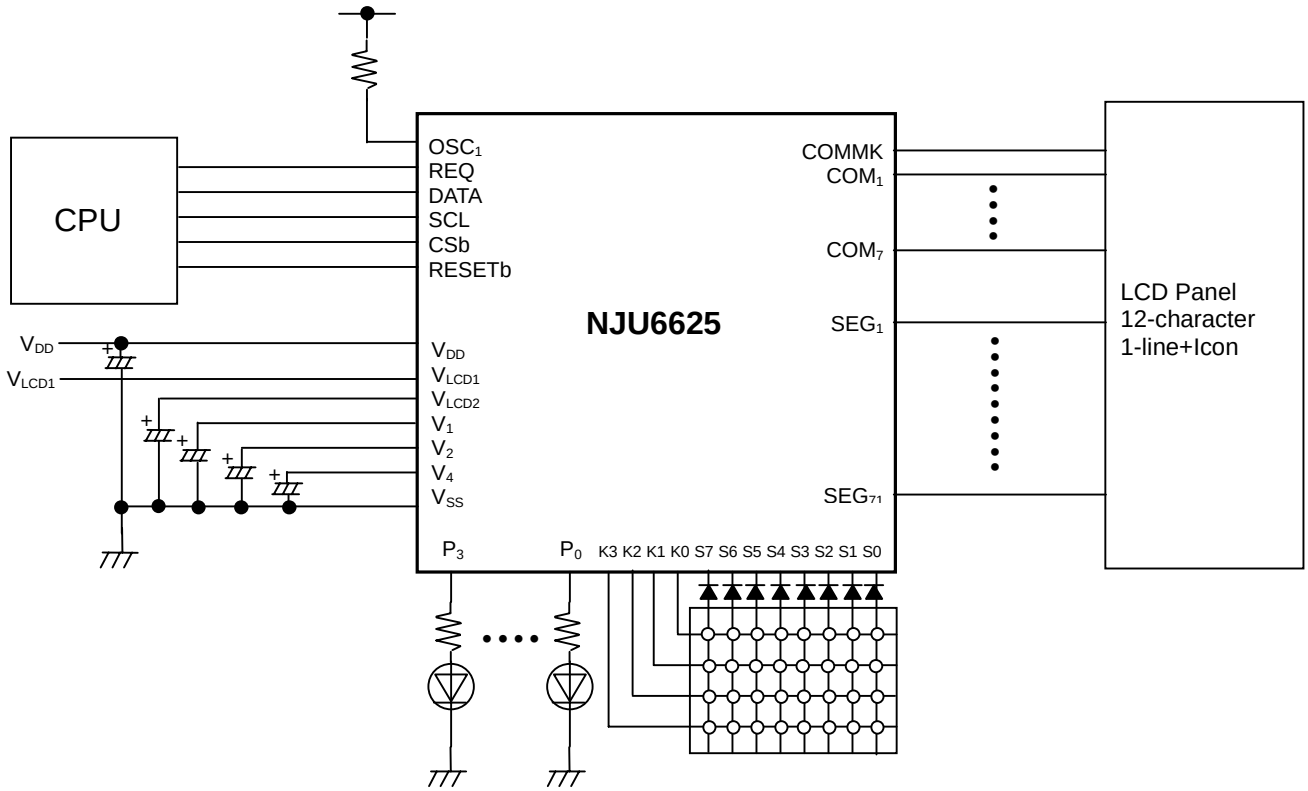
## ■ LCD DRIVING WAVE FORM




Is Keyscan waveform

## ■ APPLICATION CIRCUITS

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