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NewVision

NV3035C Data Sheet

960X240 TFT LCD Single Chip Digital Driver

Version 0.5
Aug.27, 2013

Contents

1. General Description

NV3035C is a single chip digital driver for 320RGB×240 dot color TFT-LCD panels. It contains 960 channels source driver and 240 channels gate driver with timing controller and build-in power circuits.

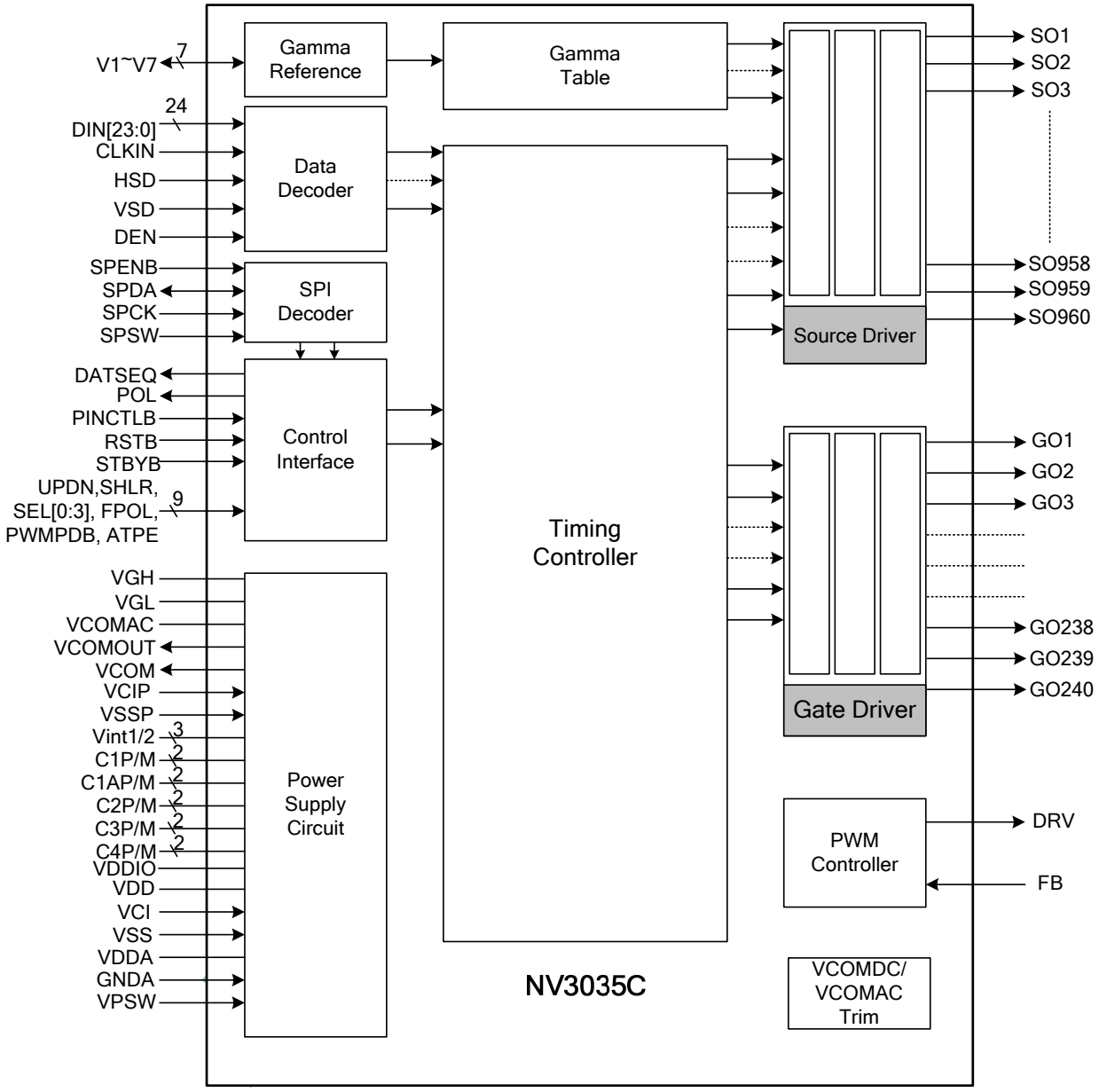
NV3035C incorporates 8-bit serial and 24-bit parallel RGB interface to receive digital display data. It generates 64-level gamma-corrected gray scale voltages and supports maximum 16M colors display with dithering function. The system function control commands can be set by using 3-wire serial peripheral interface.

NV3035C is designed for wide voltage supply range and small output deviation for better display quality. With advanced design, the NV3035C incorporates special designed architecture to achieve lower power dissipation, making this driver best suitable for small or mid sized portable devices such as cell phones, PDAs, mobile TV devices, etc.

2. Features

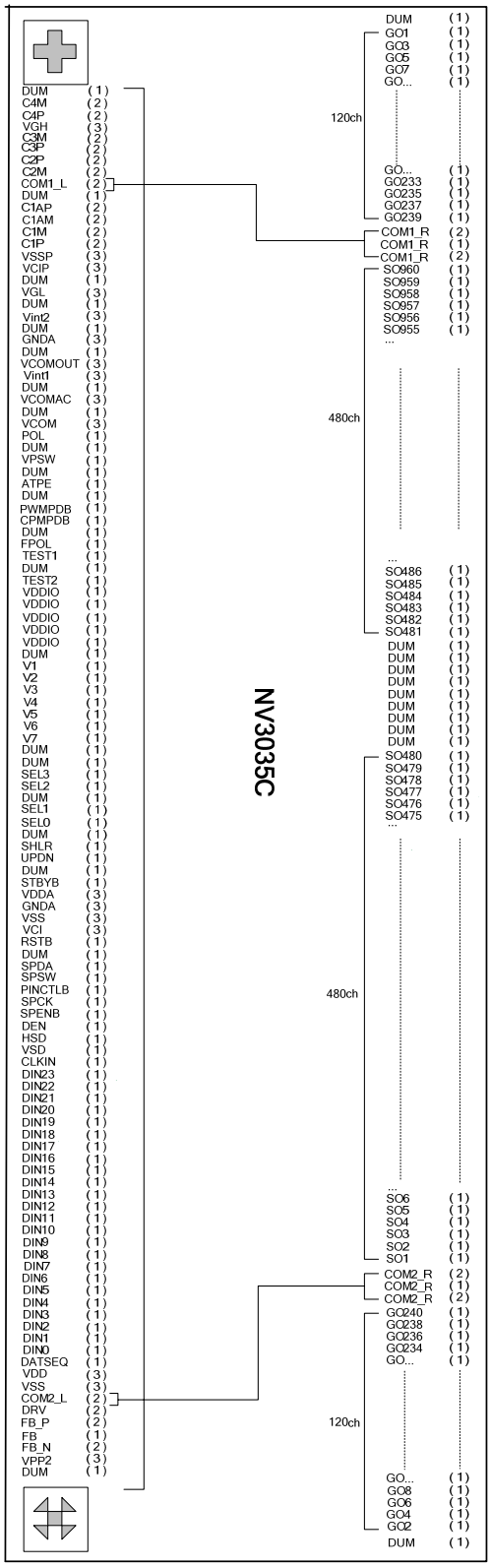
- One-Chip solution for 960×240 dot TFT LCD Driver
- 8-bit resolution 256 gray scale with Dithering
- 8-bit/24-bit digital(RGB) data interface
- 3-Wire SPI for parameters programming
- 1.8~3.6V power supply for I/O circuits
- 3.0~3.6V power supply for charge pump circuits
- Build-in 1.8V LDO for internal circuits
- Build-In DC-DC for power circuits (VGH/VGL/VCOMAC/VCOMDC voltage supply)
- Configurable color filter type for both Delta and Stripe type
- Operating frequency: 30MHz(max)
- Right/Left shift, Up and Down scan function selectable
- One Line / Two Line / Frame Inversion driving method selectable
- Support Cs on Common structure
- Build-In PWM circuit for LED Back-light
- Stand-by mode for super low power consumption
- Built-in Auto Test Pattern
- OTP trimming for VCOMAC/VCOMDC with internal burning supply
- COG package

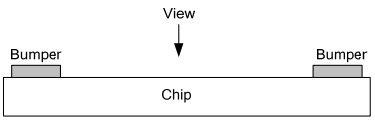
3. Block Diagram



4. Pad Description

4.1. Pad Sequence (Bump Side)





4.2. Pad Description

Designation	I/O	Description
DIN[23..0]	I	Data Input. 8-bit mode: DIN7:MSB; DIN0:LSB; the remainder should be connect to GND. 24-bit mode: DIN[7:0]=R[7:0] data; DIN[15:8]=G[7:0] data; DIN[23:16]=B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data bus to GND.
CLKIN	I	Clock for Input Data. Data latched at rising/falling edge of this signal. Default positive edge latch data.
HSD	I	Horizontal Sync input. Default Negative polarity, can be change by HSDPOL register.
VSD	I	Vertical Sync input. Default Negative polarity, can be change by VSDPOL register.
DEN	I (Pull Low)	Data Input Enable. Active High to enable the data input Bus under "DE Mode". Normally pull low.
DATSEQ	O	Data sequence control pin for external T-CON. Output "1": for Odd line, "0": for Even line.
POL	O	Frame polarity output. Amplitude of signal is from 0V to 3.3V.
V1~V7	I/O	Gamma correction reference voltage. When VSET="1" is used. The voltage of pins V1~V7 must be swing and must be AVDD-0.1V>V1>V2>V3 V5>V6>V7>AGND+0.1V when POL="1" and AGND+0.1V<V1'<V2'<V3' V5'<V6'<V7'<AVDD-0.1V when POL="0", Where V1-V2=V2'-V1', V2-V3=V3'-V2',…, V5-V6=V6'-V5',V6-V7=V7'-V6'. **Note:** V1~V7 must be supplied voltage external when VSET="1". Vx is external power of positive polarity and Vx' is external power of negative polarity.
SPENB	I (Pull High)	3-Wire Communication Enable. Active Low. Normally pull high. **Please pull high or floating under PINCTLB=0 mode.**
SPDA	I/O	3-Wire Communication Data input/output.
SPCK	I	3-Wire Communication Clock input. Rising edge latch.
SPSW	I (Pull Low)	3-Wire register map select. "0" for default 3-Wire register map, "1" is useless.
RSTB	I (Pull High)	Global reset pin. Active Low to enter Reset State. Suggest connecting with a RC reset circuit for stability. Normally pull high.
PINCTLB	I (Pull High)	Enable pin control function. Normally pull high. PINCTLB="0", Enable pin control function. (STBYB,UPDN,SHLR,SEL[0…3],FPOL) and (PWMPDB,ATPE) active as input pin for function control propose. Refer to the (STBYB,UPDN, SHLR,SEL[0…3],FPOL, PWMPDB,ATPE) description for more information. PINCTLB="1", Default mode. (STBYB,UPDN,SHLR,SEL[0…3],FPOL) and (PWMPDB,ATPE) active as unknown state; Don't connect (STBYB, UPDN, SHLR, SEL[0…3], FPOL) and (PWMPDB,ATPE) to any state under this mode. **Note:** The 3-wire control register will be disabled under PINCTLB=0 mode.
SO1~SO960	O	Source Driver Output Signals.

GO1~GO240	O	Gate Driver Output Signals.
ALIGN_T/B	M	For assembly alignment.
CPMPDB	I	Charge pump on/off control pin. TP15=CPMPDB. CPMPDB="0", internal charge pump will be shut down; CPMPDB="1", internal charge pump normal operating. TP15 active as input pin under any state of PINCTLB. If floating this pin, the charge pump will turn off.
(STBYB,UPDN,SHLR,SEL[0…3],FPOL) (PWMPDB,ATPE)	T I	TEST Pin/Function control pin. When PINCTLB="1", (STBYB,UPDN,SHLR,SEL[0…3],FPOL), (PWMPDB,ATPE) act as test pin. Floaating those pins for normal operation. When PINCTLB="0", (STBYB,UPDN,SHLR,SEL[0…3],FPOL), (PWMPDB,ATPE) act as function control input pin. All the input pin should be connect to GND or VDD. Floating those pins will result in input unknown problem.
VPSW	I (Pull Low)	Voltage control switch. Normally pull low. VPSW="0". Default mode. VGH、VGL、VCOMAC and VCOMDC active as normal use and control by 3-wire. VPSW="1". Voltage fix mode. VGH=15V,VGL=-7V, VCOMAC=5.0V and VCOMDC=1.86V. Under the mode voltage can't control by 3-wire.
VGH	PS	Capacitor pin. Positive power supply for Gate Driver output.
VGL	PS	Capacitor pin. Negative power supply for Gate Driver ouput.
VCOMAC	PS	Capacitor pin. Power supply for VCOMOUT output.
VCOM	PS	VCOM DC voltage output pin for DC re-construction.
VCOMOUT	O	Frame polarity output for panel VCOM. Amplitude of signal is from GNDA1 to VDDA1. The polarity of VCOMOUT is inversed with internal signal "POL" when "FPOL"=0.
VDDA	PO	Power supply for source driver and gamma circuit.
GNDA	PI	Ground pins for source driver and gamma circuit.
VCI	PI	Power supply for digital and analog circuits.
VSS	PI	Ground pins for digital circuits.
VCIP	PI	Power supply for charge pump circuits.
VSSP	PI	Ground pins for charge pump circuits.
VDD	C	Capacitor connect pin for internal regulator. Refer to the section of "Power Circuit" for the application.
C1P/M, C1AP/M, C2P/M, C3P/M, C4P/M, Vint1/2	C	Capacitor connect pin for internal charge pump. Refer to the section of "Power Circuit" for the application.
FB_P	I	Internal power switch current input pad. Note: Voltage on this pad should be <5.5V. Pull low in more than one LED case.
FB_N	O	Internal power switch current output pad. Note: Voltage on this pad should be <5.5V. Pull low in more than one LED case.
FB	VI	PWM controller feedback input. FB threshold is 0.6V nominal.
DRV	O	PWM output driver signal for the boost converter.
COM1_L/R	S	The internal link together between input side and Output side.
COM2_L/R	S	The internal link together between input side and Output side.
TOSC,TVREF, T-1U	T	Test pin .Float these pins for normal operation.

DUM	D	Don't connect to any signal or pull high/low.
ATPE	I	Auto Test Pattern Enable.
VPP2	P	Customer OTP power input pin.

Note:

I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, T: Testing I/O: Input/Output. PS: Power Setting, C: Capacitor pin.

NV3035C Align Mark:

ALIGN_T	M	For assembly alignment.
ALIGN_B	M	For assembly alignment.

NV3035C Pass Line Description:

Pass Line No:	Pad Name	
1	COM1_L	COM1_R
2	COM2_L	COM2_R

TP0~14 and TP16~18 Function Control Pin Mapping Table (When PINCTLB="0"):

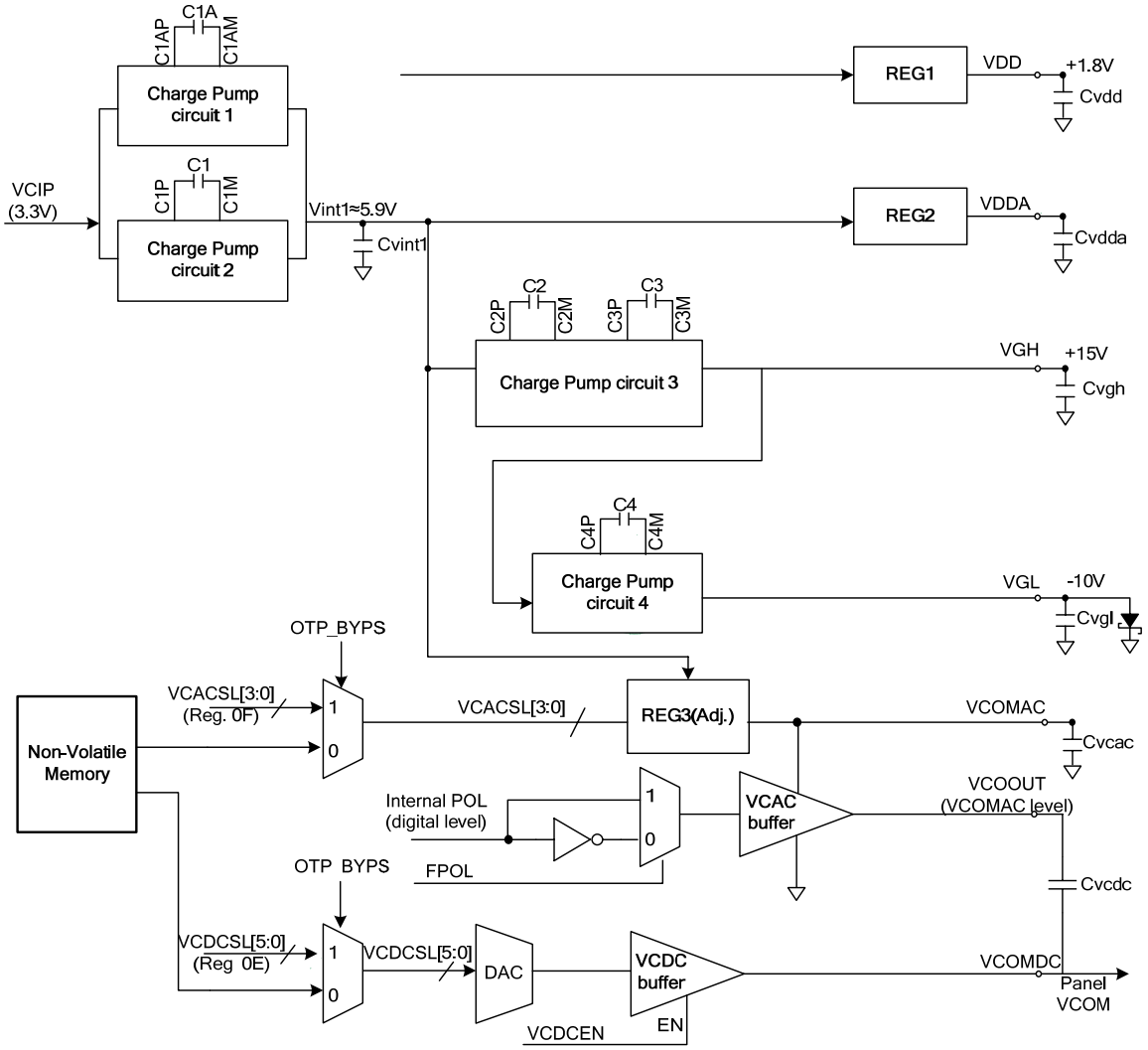
TPX	PINCTLB="0"
	Input control function (Related to 3-wire control register)
0	STBYB
1	UPDN
2	SHLR
3	SEL0
4	SEL1
5	SEL2
6	SEL3
7	DUM
8	VDDIO
9	VDDIO
10	VDDIO
11	VDDIO
12	TEST2
13	TEST1
14	FPOL
16	PWMPDB
17	DUM
18	Auto Test Pattern Enable

*Note:
PINCTLB function has higher priority then the 3-wire command. The 3-wire control register will be disabled when PINCTLB="0". Please pull high or floating SPENB under PINCTLB=0 mode.
Remark:
TP15=CPMPDB, Charge pump on/off control pin.
CPMPDB="0", internal charge pump will be shut down.
CPMPDB="1", internal charge pump normal operating.
TP15 active as input pin under any state of PINCTLB.

5. Function Descriptions

5.1. Power Supply Circuits

NV3035C built in charge pump circuit for gate driver VGH/VGL voltage and panel VCOMAC/VCOMDC voltage.Following block diagram illustrate how the charge pump circuit works.



< Value of wiring resistance and Cap. >

Pin name	Resistor of wiring (ohm)	Cap no.	CAP (uF)
C1P	<10	C1	≥1uF
C1M	<10		
C2P	<10	C2	
C2M	<10		
C3P	<10	C3	
C3M	<10		
C4P	<10	C4	
C4M	<10		
C1AP	<10	C1A	
C1AM	<10		

*Note: Others Cap. Suggest value≥4.7uF;
Schottky diode turn-on voltage=0.2V.

5.2. Input Data VS Output

Source Driver data output sequence can be control by “SHLR”.

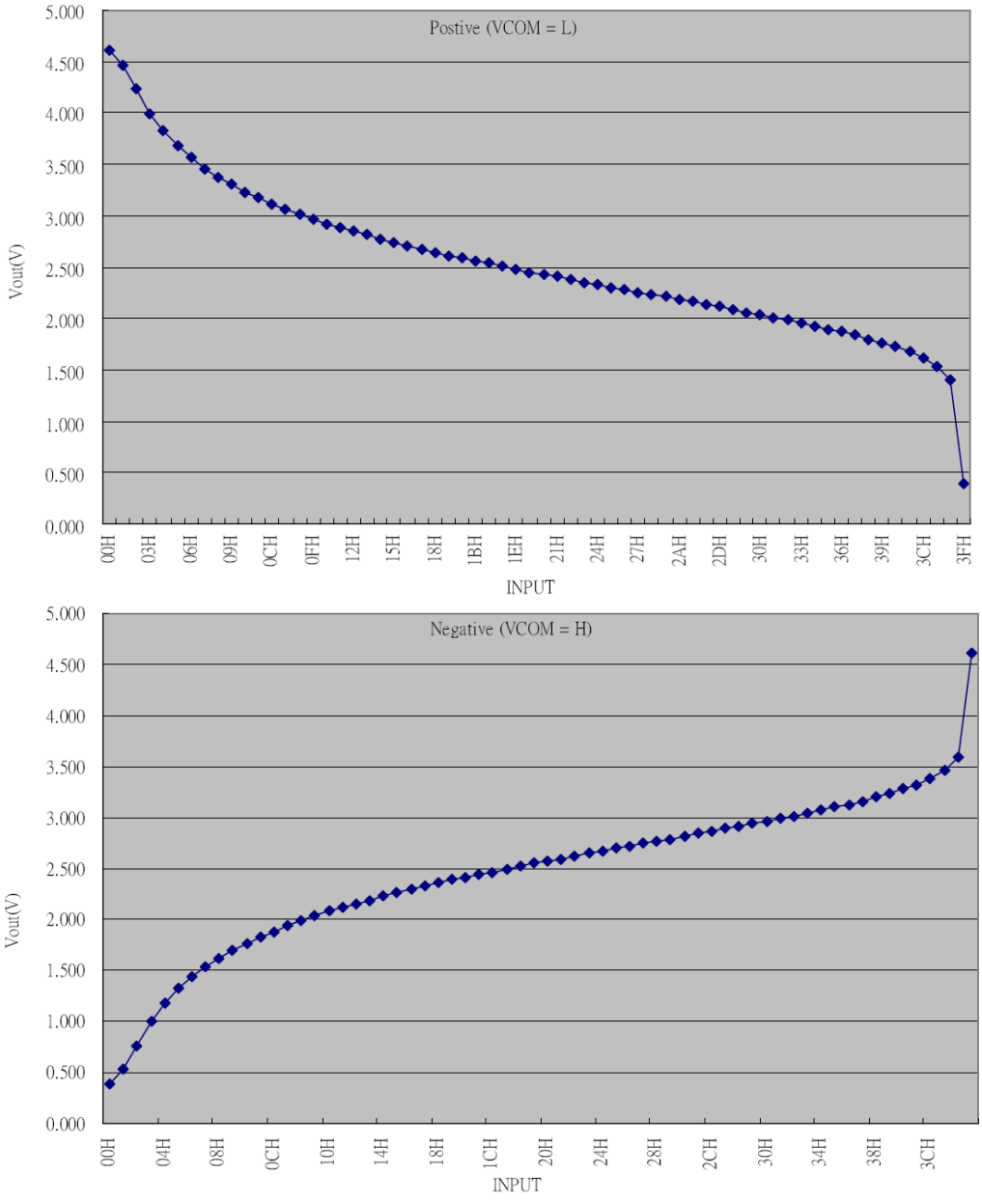
Output	SO1	SO2	SO3	…	SO958	SO959	SO960
SHLR=”1”	First data			→			Last data
SHLR=”0”	Last data			←			First data

Gate Driver scan output sequence can be control by “UPDN”.

Scan	GO1	GO2	GO3	…	GO238	GO239	GO240
UPDN=”1”	First data			→			Last data
UPDN=”0”	Last data			←			First data

5.3. Gamma Adjustment Function

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages to get the relative resistor value and voltage calculation method, please.



Input Data and Output Voltage Reference Table(VSET="0")

@VDDA=5V,VCOMOUT=L,POL=H	
Vno.	**Unit=V**
V1	4.610
V2	3.680
V3	3.115
V4	2.585
V5	2.185
V6	1.790
V7	0.390

@VDDA=5V,VCOMOUT=H,POL=L	
Vno.	**Unit=V**
V1	0.390
V2	1.320
V3	1.885
V4	2.415
V5	2.815
V6	3.210
V7	4.610

Data	VCOMOUT=H,POL=L
(V1)00H	VDDA×0.078
01H	VDDA×0.107
02H	VDDA×0.153
03H	VDDA×0.201
04H	VDDA×0.236
(V2)05H	VDDA×0.264
06H	VDDA×0.288
07H	VDDA×0.308
08H	VDDA×0.325
09H	VDDA×0.340
0AH	VDDA×0.354
0BH	VDDA×0.366
(V3)0CH	VDDA×0.377
0DH	VDDA×0.388
0EH	VDDA×0.398
0FH	VDDA×0.408
10H	VDDA×0.416
11H	VDDA×0.424
12H	VDDA×0.431
13H	VDDA×0.438
14H	VDDA×0.446
15H	VDDA×0.453
16H	VDDA×0.459
17H	VDDA×0.465
18H	VDDA×0.472
19H	VDDA×0.478
(V4)1AH	VDDA×0.483
1BH	VDDA×0.488
1CH	VDDA×0.493
1DH	VDDA×0.499
1EH	VDDA×0.505
1FH	VDDA×0.510
20H	VDDA×0.514
21H	VDDA×0.519
22H	VDDA×0.525
23H	VDDA×0.530
24H	VDDA×0.535
25H	VDDA×0.540
26H	VDDA×0.545
27H	VDDA×0.550
28H	VDDA×0.554
29H	VDDA×0.558
(V5)2AH	VDDA×0.563
2BH	VDDA×0.568
2CH	VDDA×0.573
2DH	VDDA×0.578
2EH	VDDA×0.583
2FH	VDDA×0.588
30H	VDDA×0.593
31H	VDDA×0.598
32H	VDDA×0.603
33H	VDDA×0.609
34H	VDDA×0.615
35H	VDDA×0.621
36H	VDDA×0.626
37H	VDDA×0.632
(V6)38H	VDDA×0.642
39H	VDDA×0.648
3AH	VDDA×0.656
3BH	VDDA×0.665
3CH	VDDA×0.677
3DH	VDDA×0.693
3EH	VDDA×0.719
(V7)3FH	VDDA×0.922

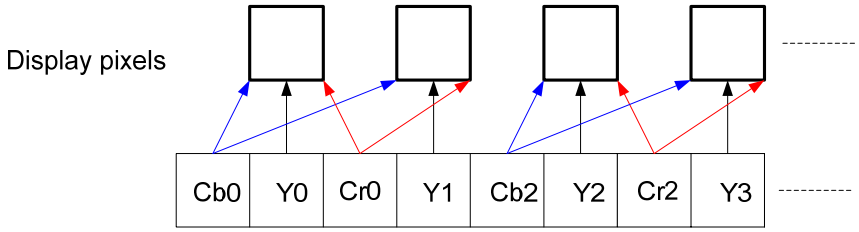
Data	VCOMOUT=L,POL=H
(V1)00H	VDDA×0.922
01H	VDDA×0.893
02H	VDDA×0.847
03H	VDDA×0.799
04H	VDDA×0.764
(V2)05H	VDDA×0.736
06H	VDDA×0.712
07H	VDDA×0.692
08H	VDDA×0.675
09H	VDDA×0.660
0AH	VDDA×0.646
0BH	VDDA×0.634
(V3)0CH	VDDA×0.623
0DH	VDDA×0.612
0EH	VDDA×0.602
0FH	VDDA×0.592
10H	VDDA×0.584
11H	VDDA×0.576
12H	VDDA×0.569
13H	VDDA×0.562
14H	VDDA×0.554
15H	VDDA×0.547
16H	VDDA×0.541
17H	VDDA×0.535
18H	VDDA×0.528
19H	VDDA×0.522
(V4)1AH	VDDA×0.517
1BH	VDDA×0.512
1CH	VDDA×0.507
1DH	VDDA×0.501
1EH	VDDA×0.495
1FH	VDDA×0.490
20H	VDDA×0.486
21H	VDDA×0.481
22H	VDDA×0.475
23H	VDDA×0.470
24H	VDDA×0.465
25H	VDDA×0.460
26H	VDDA×0.455
27H	VDDA×0.450
28H	VDDA×0.446
29H	VDDA×0.442
(V5)2AH	VDDA×0.437
2BH	VDDA×0.432
2CH	VDDA×0.427
2DH	VDDA×0.422
2EH	VDDA×0.417
2FH	VDDA×0.412
30H	VDDA×0.407
31H	VDDA×0.402
32H	VDDA×0.397
33H	VDDA×0.391
34H	VDDA×0.385
35H	VDDA×0.379
36H	VDDA×0.374
37H	VDDA×0.368
(V6)38H	VDDA×0.358
39H	VDDA×0.352
3AH	VDDA×0.344
3BH	VDDA×0.335
3CH	VDDA×0323
3DH	VDDA×0.307
3EH	VDDA×0.281
(V7)3FH	VDDA×0.078

5.4. Input Video Formats

NV3035C should support 22 types of input video formats:

#	Format	Sub-type1	Sub-type2	Comments
(1)	RGB (NTSC only)	8-bit serial	HV mode	
(2)			DE mode	
(3)		24-bit parallel	HV mode	
(4)			DE mode	
(5)	CCIR656 (YUV)	1440 only, NTSC	Mode A	Cb/Y/Cr/Y
(6)			Mode B	Cr/Y/Cb/Y
(7)		1440 only, PAL 280 lines	Mode A	Cb/Y/Cr/Y
(8)			Mode B	Cr/Y/Cb/Y
(9)		1440 only, PAL 288 lines	Mode A	Cb/Y/Cr/Y
(10)			Mode B	Cr/Y/Cb/Y
(11)	CCIR601 (YUV)	1440, NTSC	Mode A	Cb/Y/Cr/Y
(12)			Mode B	Cr/Y/Cb/Y
(13)		1440, PAL 280 lines	Mode A	Cb/Y/Cr/Y
(14)			Mode B	Cr/Y/Cb/Y
(15)		1440, PAL 288 lines	Mode A	Cb/Y/Cr/Y
(16)			Mode B	Cr/Y/Cb/Y
(17)		1280, NTSC	Mode A	Cb/Y/Cr/Y
(18)			Mode B	Cr/Y/Cb/Y
(19)		1280, PAL 280 lines	Mode A	Cb/Y/Cr/Y
(20)			Mode B	Cr/Y/Cb/Y
(21)		1280, PAL 288 lines	Mode A	Cb/Y/Cr/Y
(22)			Mode B	Cr/Y/Cb/Y

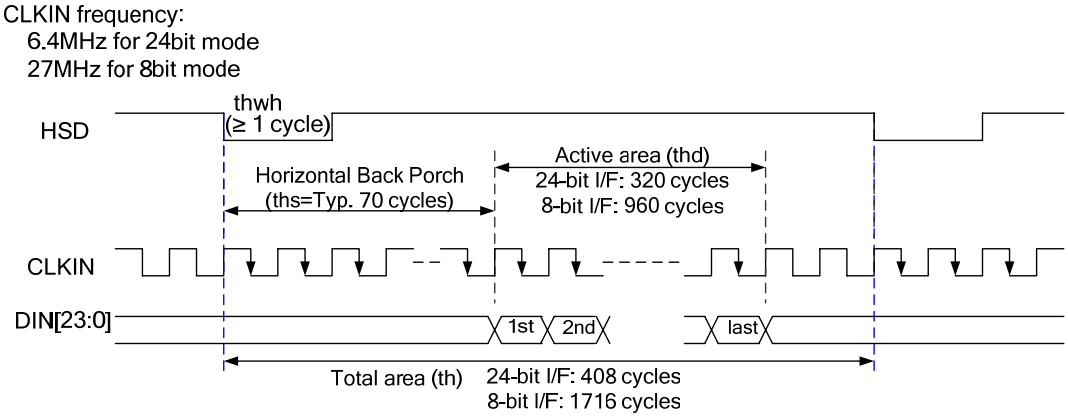
Support 2 type of color encode systems: RGB (8-8-8) and YUV (YCbCr) 4:2:2.
YUV4:2:2:



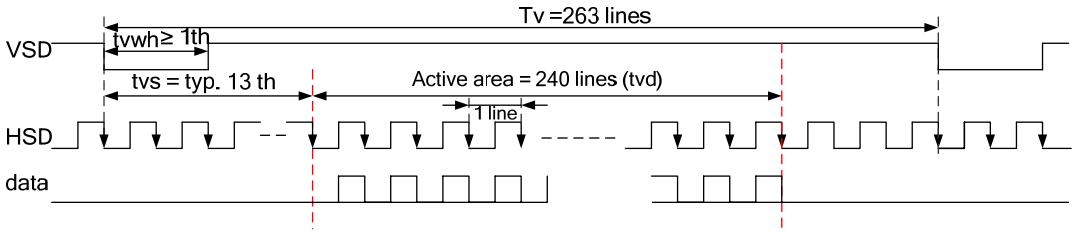
Y is the luminance (Luma) factor, it is the brightness of the pixel. Cb and Cr is the chrominance (Chroma) for "blue" and "red" sub respectively.

5.4.1. RGB (NTSC) input timing

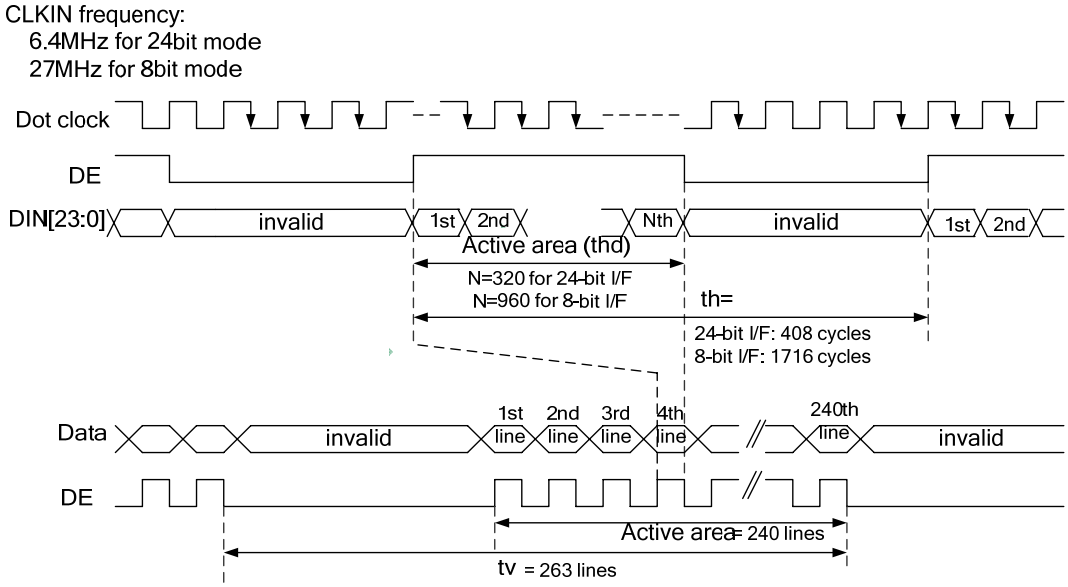
(1) HV mode timing: DE signal is not necessary, host float this pin.
Horizontal:



Vertical:



(2) DE mode: Hsync and Vsync are not needed in DE mode, host float these pins.



*Notes:

(1) both CLKIN, HSD, VSD and DE supports active polarity selection. In the diagrams above, the VSD and HSD is low active, CLKIN samples data at negedge, DE is high active, and however, other kinds of polarity of these signals are also supported.

(2) signal relationship timing specification please refers the reference datasheet.

5.4.2. CCIR601 input timing

Features of the CCIR601 supported by this chip:

(1) only 8-bit I/F supported.

(2) Both PAL and NTSC support. For PAL, both 280 and 288 lines supported.

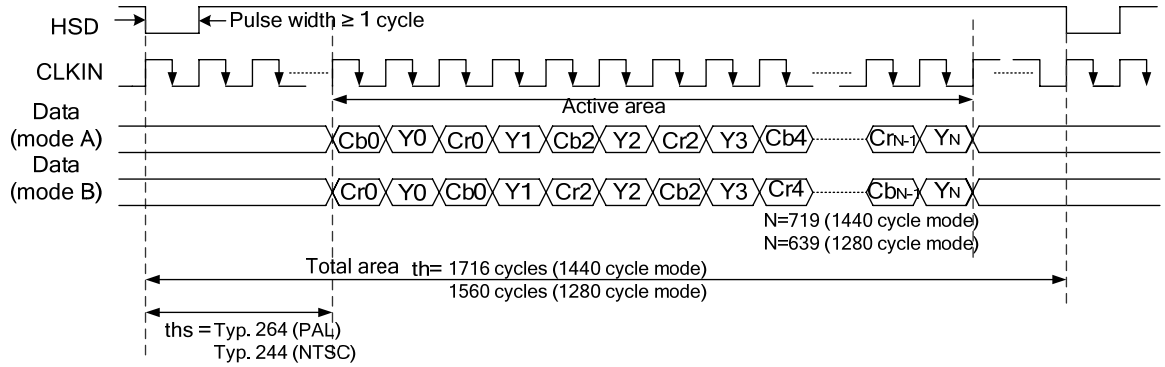
(3) Both 1440 and 1280 horizontal cycles are supported.

(4) For all supported CCIR601 input format, the data sequence can be two types: mode A is Cb/Y/Cr/Y, mode

B is Cr/Y/Cb/Y.

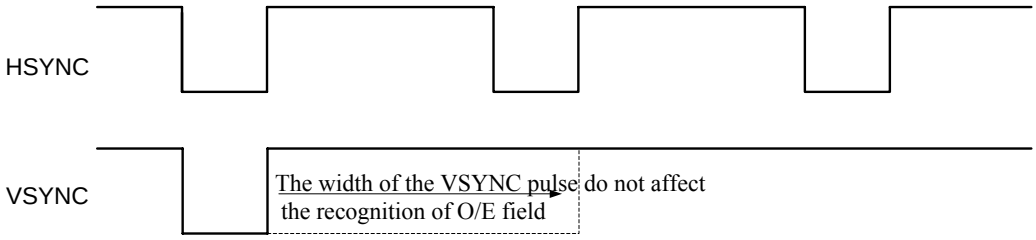
Horizontal signal:

CLKIN frequency:
24.54MHz for 1280-cycle mode
27MHz for 1440-cycle mode

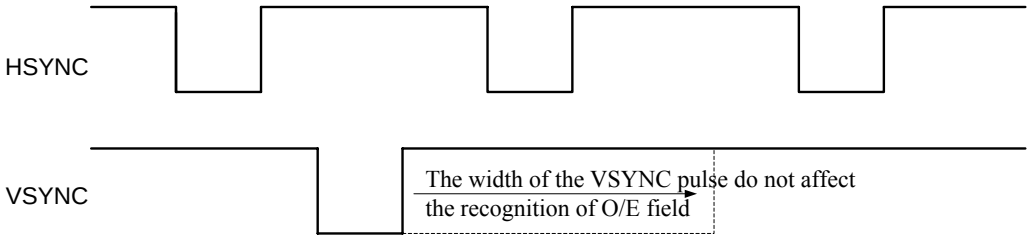


For CCIR601, 1 image frame = 1 odd field + 1 even field.
The odd/even filed is recognized by the inter relationship of Hsync and Vsync signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an odd field. A VSYNC low transition when HSYNC is high indicates the start of an even field.

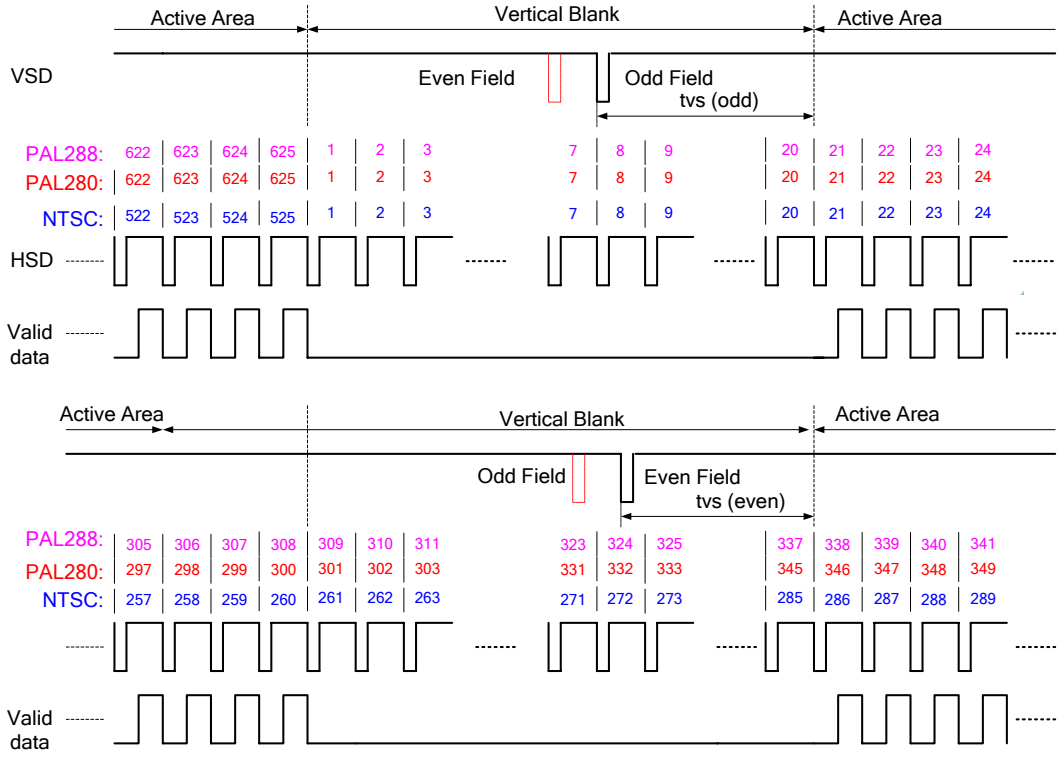
Odd Field



Even Field



Vertical signal:

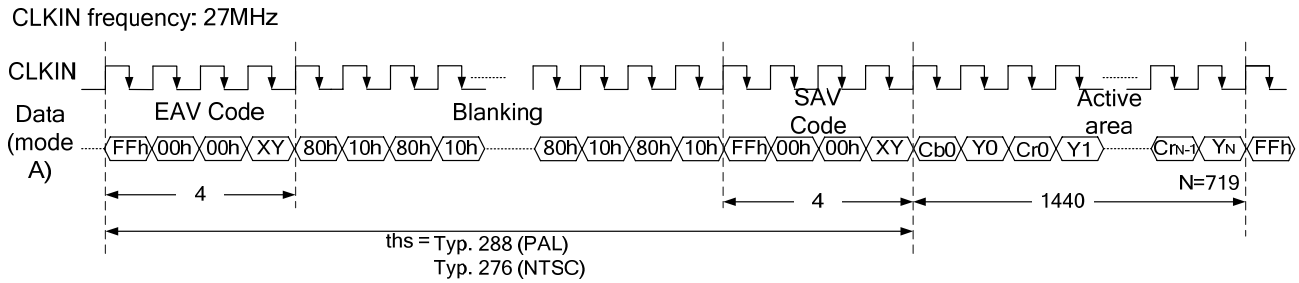


NTSC mode: active area=240 lines; PAL 280 mode: active area=280 lines; PAL 288 mode: active area=288 lines.

5.4.3. CCIR656 input timing

The CCIR656 use the YUV color encoding too. The difference of CCIR656 is that sync signals are embedded into the code stream. By this mode, VSD, HSD, DEN signals are not needed.

Horizontal:



EAV/SAV Format:

The "XY" byte in EAV/SAV plays a critical role for synchronization:

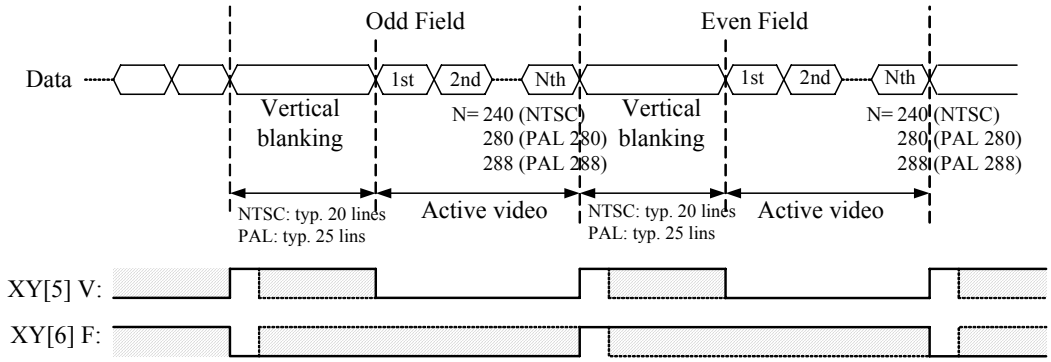
XY	B7	B6	B5	B4	B3	B2	B1	B0
EAV	1	F	V	H	Protection bits by ITU 656			
SAV	1	F	V	H	Protection bits by ITU 656			

F: Field bit. This is for vertical timing. F=0 indicates this is the line of the 1st field (odd field). F=1 indicates this is the line of the 2nd field (even field).

V: Vertical blanking bit. This is for vertical timing. V=1 indicates vertical blanking lines, V=0 indicates an active video line.

H: Horizontal recognizing bit. H=0: SAV, H=1: EAV.

Vertical:



5.5. CCIR601/656 Input Video Resizing

Input image size (1 field):

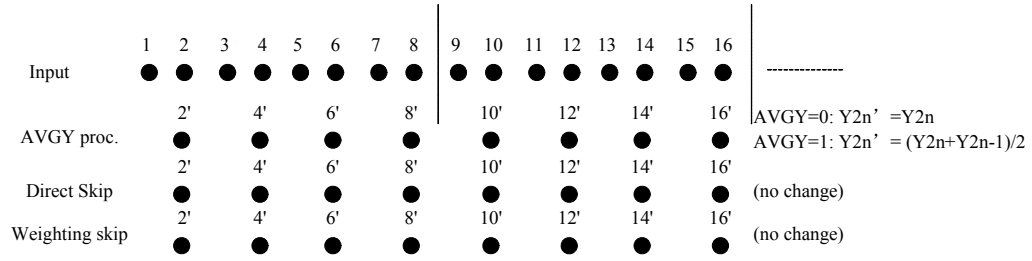
	NTSC	PAL-280	PAL-288	Display
CCIR601-1440	720RGB*240	720RGB*280	720RGB*288	320RGB*240
CCIR601-1280	640RGB*240	640RGB*280	640RGB*288	320RGB*240
CCIR656-1440	720RGB*240	720RGB*280	720RGB*288	320RGB*240

5.5.1. Horizontal (X-direction) scale down method

For 640RGB (1280 clocks) source input: 640RGB→scale down to 320RGB (2:1).
For 720RGB (1440 clocks) source input, there are four types of skip & scaling method for choice:

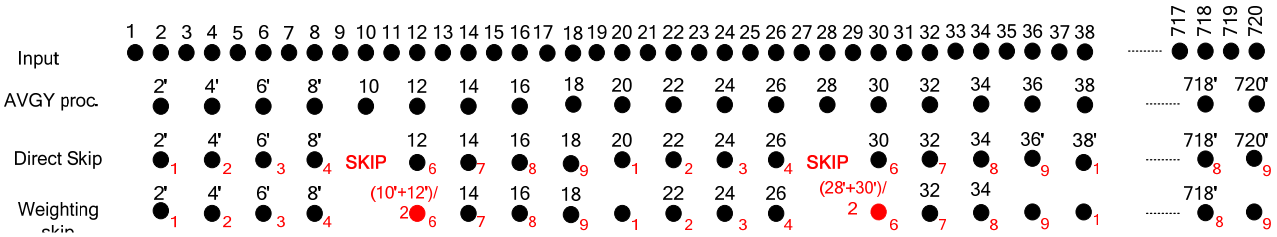
HDNC1-0		Scaling Ratio
00	720RGB→(scale down) 320RGB	9:4
01	720RGB→(skip L/R 10RGB) 700RGB→(scale down) 320RGB	35:16
10	720RGB→(skip L/R 20RGB) 680RGB→(scale down) 320RGB	17:8
11	720RGB→(skip L/R 40RGB) 640RGB→(scale down) 320RGB	2:1

✓ **HDNC[1:0]=2'b00 (1280 clocks)**
1280 clk → 640 RGB → 320 RGB
Scale ratio: 2:1



No skip.

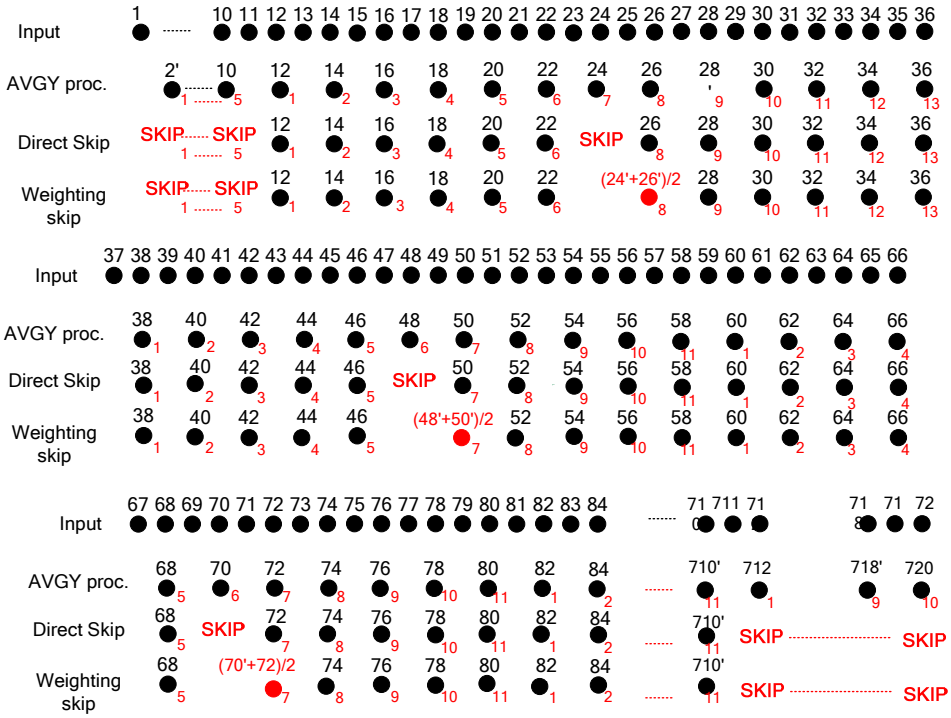
✓ **HDNC[1:0]=2'b00 (1440 clocks)**
1440 clk → 720 RGB → 320 RGB
Scale ratio: 9:4



AVGY=0, Y2n'=Y2n; AVGY=1, Y2n'=(Y2n+Y2n-1)/2.
After AVGY process, the scale ratio is 9:8 (360 → 320).
For direct skip, skip the 5th data every 9 counts; for weighting skip, skip the 5th data every 9 counts, and the 6th data is the average of the 5th and 6th data. (This average include Y, Cb and Cr factors.)

✓ **HDNC[1:0]=2'b01**

1440 clk → 720 RGB → (Skip right/left 10 RGB) 700 RGB → 320 RGB
Scale ratio: 35:16

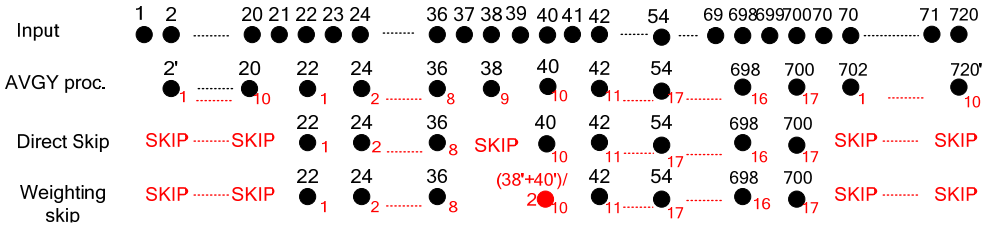


AVGY=0, Y2n'=Y2n; AVGY=1, Y2n'= (Y2n+Y2n-1)/2.
After AVGY process, the scale ratio is 35:32 (350 → 320).
For direct skip, skip the 6th , 19th, 30th data every 35 counts;
For weighting skip, skip the 6th , 19th, 30th data every 35 counts and the 7th, 20th, 31st data are:

$D(7^{th}) = [D(6^{th})+D(7^{th})]/2$
$D(20^{th}) = [D(19^{th})+D(20^{th})]/2$
$D(31^{st}) = [D(30^{th})+D(31^{st})]/2$

✓ **HDNC[1:0]=2'b10**

1440 clk → 720 RGB → (Skip right/left 20 RGB) 680 RGB → 320 RGB
Scale ratio: 17:8



AVGY=0, Y2n'=Y2n; AVGY=1, Y2n'=(Y2n+Y2n-1)/2.
After AVGY process, the scale ratio is 17:16 (340 → 320).
For direct skip, skip the 9th data every 17 counts; for weighting skip, skip the 9th data every 9 counts, and the 10th data is the average of the 9th and 10th data.

✓ **HDNC[1:0]=2'b11**
1440 clk → 720 RGB → (Skip right/left 40 RGB) 640 RGB → 320 RGB
Scale ratio: 2:1
The same as HDNC[1:0]=2'b00, 1280 clk mode.

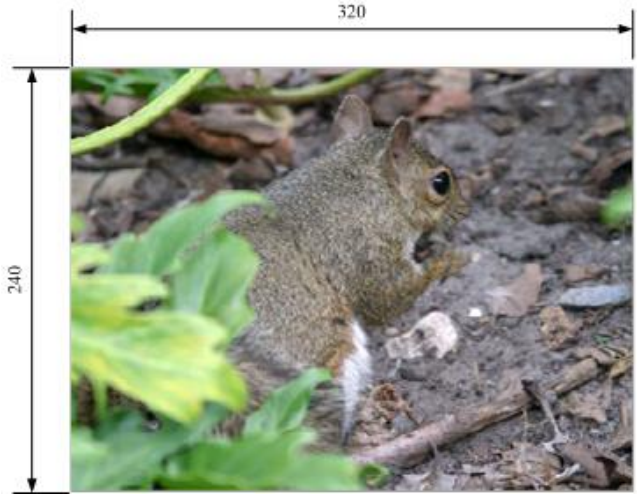
5.5.2. PAL Decimation for CCIR601/656 mode

PAL280: direct skip up/down 40 lines.
PAL288: direct skip up/down 44 lines.

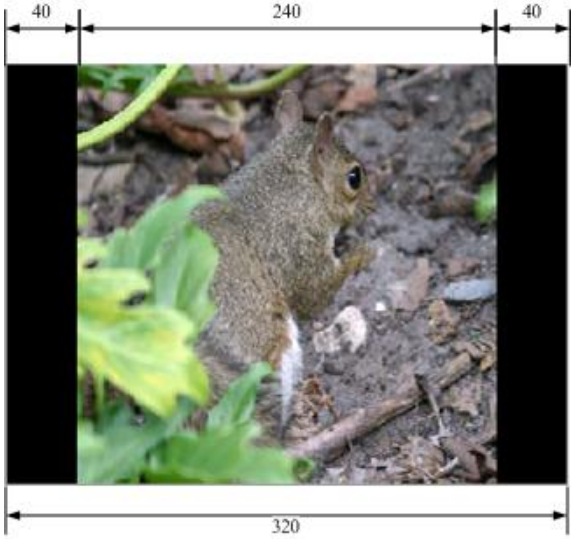
5.5.3. Display mode for CCIR601/656

WNSEL1	WNSEL0	Display Mode
0	0	Normal display(Default)
0	1	Narrow display
1	0	Wide display
1	1	234-Line

Normal display:



Narrow display:
Remove the fourth column in every four columns (initial 40 columns and last 40 columns display black).



Wide display:
Remove the fourth line in every four lines. (initial 30 lines and last 30 lines display black)

234-Line:
The initial 3 lines and last 3 lines are removed and display black.

5.6. 3-Wire SPI

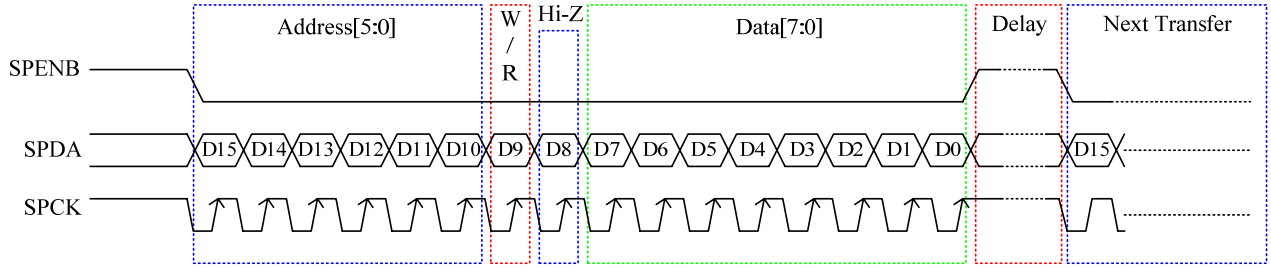
3-Wire Command Format

NV3035C uses the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the "R/W" bit in address field. NV3035C 3-Wire engine act as a "slave mode" for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during "Data phase". The returned data should be latched at the rising edge of SPCK by external controller. Data in the "Hi-Z phase" will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SPDA pin under "Hi-Z phase" and "Data phase".

Refer to the section of "3-Wire Timing Diagram" for the detail timing, please.



3-Wire Command Format:

Bit	Description
D15-D10	
D9	W/R control bit:"1" for Write; "0" for Read.
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode.
D7-D0	Data for the W/R operation to the address indicated by Address phase.

3-Wire Writer Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	X	DATA (Issue by external controller)							

3-Wire Read Format:

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	Hi-Z	DATA (Issue by NV3035C)							

6. Command Description

6.1. Registers Table

Following table list the default 3-Wire control registers and bit name definition for NV3035C. Refer to the next section for detail register function description, please.

NV3035C 3-Wire Control Register List (Default)

3-Wire Registers		Register Description		
D[15:10]	Name	Init.	R/W	Function Description
000000b	R00	03h	R/W	System control register
000001b	R01	00h	R/W	Timing Controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	CCh	R/W	Input data Format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB Contrast control register
001001b	R09	40h	R/W	RGB Brightness control register
001011b	R0B	88h	R/W	R/B Sub-Contrast control register
001100b	R0C	20h	R/W	R Sub-Brightness control register
001101b	R0D	20h	R/W	B Sub-Brightness control register
001110b	R0E	2bh	R/W	VCOMDC Level Control Register
001111b	R0F	A5h	R/W	VCOMAC Level Control Register
010000b	R10	04h	R/W	VGAM2 level Control Register
010001b	R11	24h	R/W	VGAM3/4 level control register
010010b	R12	24h	R/W	VGAM5/6 level control register
011101b	R1D	00h	R/W	OTP operation control register
011110b	R1E	00h	R/W	OTP operation control register
011111b	R1F	00h	R/W	OTP operation control register

NV3035C 3-Wire Register Bit Definition (Default)

3-Wire Control Register Bit Map								
Reg.	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
R00	PAT3	PAT2	PAT1	PAT0	PWMPDB	X	STBYB	RESETB
R01	X	X	X	SWD2	SWD1	SWD0	DITHB	CFTYP
R02	SKIPMOD	HDNC1	HDNC0	X	FPOL	VSET	UPDN	SHLR
R03	DENPOL	CLKPOL	HSDPOL	VSDPOL	SEL3	SEL2	SEL1	SEL0
R04	DDLY7	DDLY6	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R05	X	HDLY6	HDLY5	HDLY4	HDLY3	HDLY2	HDLY1	HDLY0
R07	FRAD1	FRAD[0]	INVSL[1]	INVSL[0]	PAL	PALM		AVGY
R08	X	X	X	CON4	CON3	CON2	CON1	CON0

R09	X	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRI0
R0A	HUE[3]	HUE[2]	HUE[1]	HUE[0]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
R0B	SCONB1	SCONB0			SCONR1	SCONR0		
R0C	X	X	SBRIR5	SBRIR4	SBRIR3	SBRIR2	SBRIR1	SBRIR0
R0D	X	X	SBRIB5	SBRIB4	SBRIB3	SBRIB2	SBRIB1	SBRIB0
R0E	X	OTP_BYPS	VCDCSL5	VCDCSL4	VCDCSL3	VCDCSL2	VCDCSL1	VCDCSL0
R0F	VGLSL1	VGLSL0	VGHSL1	VGHSL0	VCACSL3	VCACSL2	VCACSL1	VCACSL0
R10	X	X	X	GAMEN	X	V2GAM2	V2GAM1	V2GAM0
R11	X	X	V4GAM2	V4GAM1	V4GAM0	V3GAM2	V3GAM1	V3GAM0
R12	X	X	V6GAM2	V6GAM1	V6GAM0	V5GAM2	V5GAM1	V5GAM0
R1D	PDIN[7]	PDIN[6]	PDIN[5]	PDIN[4]	PDIN[3]	PDIN[2]	PDIN[1]	PDIN[0]
R1E	PPROG	PSWSL	PWE	POR	PTM[1]	PTM[0]	PA[1]	PA[0]
R1F								OTPSEL
R20							WNSEL[1]	WNSEL[0]

*Note: Register function active at the falling edge of VSD except STBYB, RESETB register bits.
Registers list below require Vsync trigger:
DITHB, CFTYP, FPOL, VSET, UPDN, SHLR, DDLY, HDLY, INVSL, CON, BRI, HUE, SAT, SCONB, SCONR, SBRIR, SBRIB.

6.2. Command Descriptions

R00: System Control Register

Bit	Name	Initial	R/W	Description
Bit [7:4]	PAT[3:0]	0000b	R/W	Internal Test Pattern Selection. PAT[3:0]: Select chip embedded test pattern.
Bit [3]	PWMPDB	0b	(R) R/W	Internal PWM controller Power Down bit. PWMPDB="0", internal PWM controller will be shut down; PWMPDB="1", internal PWM controller normal operating.
Bit [2]	-	-	-	
Bit [1]	STBYB	1b	(R) R/W	Standby Mode function control. STBYB="0", TCON, Source output will turn off and outputs are High-Z. STBYB="1", Normal operation.
Bit [0]	RESETB	1b	R/W	Global Reset Register. Write "0" to reset whole chip. This bit will set to "1" automatically after chip was reset.

PAT[3:0]: Embedded Auto Test Pattern Selection Register

PAT[3:0]	Test Pattern	Note
00H	Disable Internal Test Pattern Function	Default
01H	White	
02H	Black	
03H	Red	
04H	Green	
05H	Blue	
06H	Yellow	
07H	Cyan	
08H	Magenta	
09H	Gray Level 8	

0AH	Gray Level 16	
0BH	Color Bar	
0CH	Checker Board	
0DH	Cross Talk Pattern	
0EH	Horizontal Flick Pattern	
0FH	Test Pattern Auto Run Mode	

R01: Timing Controller Function Register

Bit	Name	Initial	R/W	Description
Bit[4:2]	SWD[2:0]	000b	R/W	Control and switch the relationship between the R, G, B and outputs. This register is used to match different types of color filters on LCD panel.
Bit[1]	DITHB	0b	R/W	Dithering enable. Active low. DITHB="0", Dithering on, (Pseudo 8-bits resolution). (Default mode). DITHB="1", Dithering off, (6-bits resolution, truncation last 2-bits of the input data). **Note :** Recommend user to enable this function under all modes except for 18 bit RGB input application.
Bit[0]	CFTYP	0b	R/W	Color Filter Type Select. Select Delta or Stripe mode for data arrangement. CFTYP="0", Stripe mode, Data arrangement keep in the "odd line" state of SWD[2:0] selection. CFTYP="1", Data arrangement controlled by SWD[2:0] setting.

SWD [2:0] function control:

SWD2	SWD1	SWD0	Output (n=0 to 319)				Condition
			3n+1	3n+2	3n+3		
0	0	0	R	G	B	Odd Line	SHLR="1" UPDN="1"
			G	B	R	Even Line	
0	0	1	G	B	R	Odd Line	
			B	R	G	Even Line	
0	1	X	B	R	G	Odd Line	
			R	G	B	Even Line	
1	0	0	G	B	R	Odd Line	
			R	G	B	Even Line	
1	0	1	B	R	G	Odd Line	
			G	B	R	Even Line	
1	1	X	R	G	B	Odd Line	
			B	R	G	Even Line	

Note 1: X= Don't care.
Note 2: Data arrangement will keep in the "odd line" state when CFTYP=0 for stripe mode.

R02: Operation Control Register

Bit	Name	Initial	R/W	Description
Bit [7]	SKIPMOD	0b	(R) R/W	Horizontal data processing algorithms select register. SKIPMOD = "0": Horizontal data weighting skip mode. (Default mode) . SKIPMOD = "1": Horizontal data direct skip mode.
Bit [6:5]	HDNC[1:0]	00b	(R) R/W	Horizontal Data scaling mode select register. This function is active under CCIR601 and CCIR656 mode only.

Bit [4]	-	-	-	Reserve .
Bit[3]	FPOL	0b	R/W	VCOMOUT polarity inverse control. FPOL="0": VCOMOUT normal polarity (Default mode). FPOL="1": VCOMOUT inverse polarity.
Bit[2]	VSET	0b	R/W	Gamma correction source select. VSET="0",used internal Gamma Reference voltage (VDDA). (Default mode); VSET="1",used external Gamma Reference Input (V1~V7).
Bit[1]	UPDN	1b	(R) R/W	Gate Driver Up/down scan control of gate driver. UPDN="0", Shift from down to up, First line=L240→L239→…→L2→L1=Last line. UPDN="1", Shift from up to down, First line=L1→L2→…→L239→L240=Last line (Default mode).
Bit[0]	SHLR	1b	(R) R/W	Right/Left sequence control of source driver. SHLR="0", shift left: Last data=S1←S2←S3…←S960= First data. SHLR="1", shift right: First data=S1→S2→S3…→S960= Last data.

HDNC [1:0] function setting for different horizontal data skip mode

HDNC1	HDNC0	Source Data	Data Skip Mode
0	0	1440/1280 clock	720RGB→(scale down) 320RGB
0	1	1440 clock	720RGB→(skip L/R 10RGB) 700RGB→(scale down) 320RGB
1	0	1440 clock	720RGB→(skip L/R 20RGB) 680RGB→(scale down) 320RGB
1	1	1440 clock	720RGB→(skip L/R 40RGB) 640RGB→(scale down) 320RGB

R03: Input Data Format Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	DENPOL	1b	R/W	DEN input pin polarity control. DENPOL="0", DEN negative polarity. DENPOL="1", DEN positive polarity. (Default mode).
Bit[6]	CLKPOL	0b	R/W	CLKIN pin polarity control. CLKPOL="0", CLKIN negative edge latch data. CLKPOL="1", CLKIN positive edge latch data. (Default mode).
Bit[5]	HSDPOL	0b	R/W	HSD pin polarity control. HSDPOL="0", HSD negative polarity. (Default mode). HSDPOL="1", HSD positive polarity.
Bit[4]	VSDPOL	0b	R/W	VSD pin polarity control. VSDPOL="0", VSD negative polarity. (Default mode). VSDPOL="1", VSD positive polarity.
Bit[3:0]	SEL[3:0]	1100b	(R) R/W	Input data format selection. **Note:** Different SEL[3:0] setting resolution in different AC timing.

SEL [3:0]: Data input mode

SEL3	SEL2	SEL1	SEL0	Data input format	Operating frequency
0	0	0	0	CCIR601 YUV 1280 input format（YUV mode A）	24.54MHz
0	0	0	1	CCIR601 YUV 1280 input format（YUV mode B）	24.54MHz
0	0	1	0	CCIR601 YUV 1440 input format（YUV mode A）	27MHz

0	0	1	1	CCIR601 YUV 1440 input format（YUV modeB）	27MHz
0	1	0	0	CCIR656 YCbCr input format（YCbCr mode A）	27MHz
0	1	0	1	CCIR656 YCbCr input format（YCbCr modeB）	27MHz
0	1	1	0	-	-
0	1	1	1	-	-
1	0	0	0	8-bit digital RGB input format HV Mode (NTSC only)	27MHz
1	0	0	1	8-bit digital RGB input format DE Mode (NTSC only)	27MHz
1	0	1	0	8-bit digital RGB through mode input format HV Mode (NTSC only)	27MHz
1	0	1	1	8-bit digital RGB through mode input format DE Mode (NTSC only)	27MHz
1	1	0	0	24-bit digital RGB input format HV Mode(NTSC only)	6.4MHz
1	1	0	1	24-bit digital RGB input format DE Mode(NTSC only)	6.4MHz
1	1	1	*	-	

*Note: Hsync and Vsync will be ignored in DE mode.
Remark: RGB through mode will bypass 3-wire SWD[2:0] function; TCON will not arrange data color mapping.

R04: Source Timing Delay Control Register

Bit	Name	Initial	R/W	Description
Bit[7:0]	DDLY[7:0]	46h	R/W	Select the HSD signal to 1st input data delay timing Under RGB 8/24 bit mode, Ths=DDLY[7:0], (Unit=CLKIN). The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of 9.3 for the detail, please.

*Note: DDLY function will be disabled under 8/24 bit DE mode and PINCTLB=0 condition. The default value list in the section 9.3 will be used when PINCTLB=0.

R05: Gate Timing Delay Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	-	-	-	Reserve
Bit[6:0]	HDLY[6:0]	0Dh	R/W	Select the Gate start pulse output delay timing Tvs=HDLY[6:0], (Unit=HSD). The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of 9.3 for the detail, please.

*Note: HDLY function will be disabled under 8/24 DE mode and PINCTLB=0 condition. The default value list in the section 9.3 will be used when PINCTLB=0.

R07: Internal Function Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	FRAD[1:0]	00b	R/W	Odd frame or Even frame advance control.
Bit[5:4]	INVSL[1:0]	00b	R/W	Source Driving Mode Selection Register.
Bit[3]	PAL	0b	（R） RW	NTSC or PAL mode selection Only for 601 and 656 mode. PAL="0"，Select NTSC Interface mode.(Default mode). PAL="1"，Select PAL interface mode.
Bit[2]	PALM	0b	（R） RW	PAL mode input date format selection. PAL="0"，Select NTSC Interface mode.(Default mode). PAL="1"，Select PAL interface mode.
Bit[1]	-	-	-	Reserve
Bit[0]	AVGY	0b	R/W	Average YUV interface Luminance Y. AVGY="0",Only used odd Y sample for YUV conversion. AVGY ="1",Used odd and even Y sample for YUV conversion. This function active under YUV mode only!

INVSL [1:0]

INVSL1	INVSL0	Driving Mode	Notes
0	0	1-Line Inversion	Default
0	1	2-Line Inversion	
1	0	Frame Inversion	
1	1	Reserved	

FRAD [1:0]

INVSL1	INVSL0	Driving Mode	Notes
0	0	Default	Odd/Even frame Tstv are the same
0	1	Odd frame	Even frame Tstv=HDLY setting+1
1	0	Even frame	Odd frame Tstv=HDLY setting+1
1	1	Reserve	Reserve

R08: Contrast Control Register

Bit	Name	Initial	R/W	Description
Bit[7:5]	-	-	-	Reserve
Bit[4:0]	CON[4:0]	08h	R/W	Display Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level=0) to 0x1F(level=3.875) Default value 08h(level=1.0)

R09: Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	-	-	-	Reserve
Bit[6:0]	BRI[6:0]	40h	R/W	Display Brightness level adjustment register. (2/Step) Adjust range from 0x00(level=-128) to 0x7F(level=+126). Default value 0x40(level=+0).

R0A: Hue and Saturation Control Register

Bit	Name	Initial	R/W	Description
Bit [7:4]	HUE[3:0]	08h	R/W	YUV Hue level adjustment register. (5 Deg/Step) Adjust range from 0x00(level = -40 Deg) to 0x0F(level = +35 Deg) . Default value 0x08(level = 0 Deg) . $Cb' = Cb * \cos\theta + Cr * \sin\theta$ $Cr = Cr * \cos\theta + Cb * \sin\theta$
Bit [3:0]	SAT[3:0]	08h	R/W	YUV saturation level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0) to 0x0F(level = 1.875). Default value 0x08(level = 1.00)

*Note: Hue and Saturation function was available under YUV input mode only.

R0B: R/B Sub-Contrast Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	SCONB[1:0]	02h	R/W	B Data Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level=0.75) to 0x0F(level=1.125). Default value 08h(level=1.0).
Bit[3:2]	SCONR[1:0]	02h	R/W	R Data Contrast level adjustment register.(0.125/Step) Adjust range from 0x00(level=0.75) to 0x0F(level=1.125). Default value 08h(level=1.0).

R0C: R Sub-Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	-	-	-	Reserve

Bit[5:0]	SBRIR[5:0]	20h	R/W	R Data Brightness level adjustment register.(1/Step) Adjust range from 0x00(level=-32) to 0x3F(level=+31). Default value 20h(level=0).

R0D: B Sub-Brightness Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	-	-	-	Reserve
Bit[5:0]	SBRIB[5:0]	20h	R/W	B Data Brightness level adjustment register.(1/Step) Adjust range from 0x00(level=-32) to 0x3F(level=+31). Default value 20h(level=0).

R0E: VCOMDC Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	-	-	-	Reserve
Bit[6]	OTP_BYPS	0h	R/W	VCDCSL[5:0] data source selection register. OTP_BYPS="0", VCDCSL [5:0] is read from OTP memory. OTP_BYPS="1", VCDCSL [5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for test propose. Refer to the "TRMEN" control register for the proper OTP write operation.
Bit[5:0]	VCDCSL[5:0]	2bh	R/W	VCOMDC level control register (20mV/Step @ VDDA=5.0V). VCDCSL[5:0]=00h, VCOMDC=1.00V VCDCSL[5:0]=01h, VCOMDC=1.02V …… VCDCSL[5:0]=10h, VCOMDC=1.32V …… VCDCSL[5:0]=3eh, VCOMDC=2.24V VCDCSL[5:0]=3fh, VCOMDC=2.26V

*Note: VCOMDC always keep 1.86V When VPSW="1". The OTP value effect in VPSW=0.

R0F VCOMAC Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	VGLSL	10	R/W	VGLSL level control register. VGLSL Level=1V/Step.
Bit[5:4]	VGHSL	10	R/W	VGHSL level control register. VGHSL Level=1V/Step.
Bit[3:0]	VCACSL[3:0]	0101	R/W	VCOMAC level control register. VCOMAC level=0.1V/Step @ VDDA =5.0V

VCACSL [3:0]

VCSL3	VCSL2	VCSL1	VCSL0	Level(V)
0	0	0	0	4.6
0	0	0	1	4.7
0	0	1	0	4.8
0	0	1	1	4.9
0	1	0	0	5.0
0	1	0	1	5.1(Default)
0	1	1	0	5.2
0	1	1	1	5.3
1	0	0	0	5.4
1	0	0	1	**5.5**
1	0	1	0	**5.6**
1	0	1	1	**5.7**
1	1	*	*	-

*Note: When VPSW="1". The register can't be used and VCOMAC always keep 5.0V.

Make sure to set VCOMAC < VINT1-0.3V.

VGHSL [5:4]

VGHSL1	VGHSL0	VGH(V)
0	0	12
0	1	13
1	1	14
1	0	15(default)

*Note: When VPSW="1". The register can't be used and VGH always keep 15V.

VGHSL [7:6]

VGLSL1	VGLSL0	VGL(V)
0	0	-7(default)
0	1	-8
1	1	-9
1	0	-10

*Note: When VPSW="1". The register can't be used and VGL always keep -7V.

R10: VGAM2 Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7:5]	-	-	-	Reserve
Bit[4]	GAMEN	0b	R/W	GAMMA adjustment enable control register. (adjustable voltage for V2-V6). GAEN="0" or VSET=1, Gamma correction disabled. GAEN="1" & VSET=0, Gamma correction enabled.
Bit[3]	-	-	-	Reserve
Bit[2:0]	V2GAM [2:0]	100b	R/W	V2 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level=22mV /Step.

R11: VGAM3/4 Level Control Register

Bit	Name	Initial	R/W	Description
Bit[7:6]	-	-	-	Reserve
Bit[5:3]	V4GAM [2:0]	100b	R/W	V4 GAMMA voltage level setting. Function enabled when VSET="0". Adjust level=22mV/Step.
Bit[2:0]	V3GAM [2:0]	100b	R/W	V3 GAMMA voltage level setting. Function enabled when VSET="0". Adjust level=22mV /Step

R12: VGAM5/6 Level Control Register

Bit	Name	Initial	R/W	Description
Bit[10:6]	-	-	-	Reserve
Bit[5:3]	V6GAM [2:0]	100b	R/W	V6 GAMMA voltage level setting. Function enabled when VSET="0". Adjust level=22mV/Step.
Bit[2:0]	V5GAM [2:0]	100b	R/W	V5 GAMMA voltage level setting. Function enabled when VSET="0". Adjust level=22mV /Step.

V2GAM/ V3GAM/ V4GAM/ V5GAM/ V6GAM Level Control Register Setting Table

VxGMA2	VxGMA1	VxGMA0	Voltage level	Unit	Note
0	0	0	+88	mV	Refer to the Gamma Table for the default voltage level of V2~V6
0	0	1	+66	mV	
0	1	0	+44	mV	
0	1	1	+22	mV	
1	0	0	+0(Default)	mV	

1	0	1	-22	mV	
1	1	0	-44	mV	
1	1	1	-66	mV	

***Note: x=2, 3, 4, 5, 6**

R1D: OTP Operation Control Register

Bit	Name	Initial	R/W	Description
Bit[7:0]	PDIN	00b	R/W	Program data for OTP

R1E: OTP Operation Control Register

Bit	Name	Initial	R/W	Description
Bit[7]	PPROG	0b	R/W	Program mode enabling.
Bit[6]	PSWSL	0b	R/W	Power supply select.
Bit[5]	PWE	0b	R/W	Define program cycle.
Bit[4]	POR	0b	R/W	Generate a pulse to read OTP.
Bit[3:2]	PTM[1:0]	00b	R/W	Test mode.
Bit[1:0]	PA[1:0]	00b	R/W	Programming address.

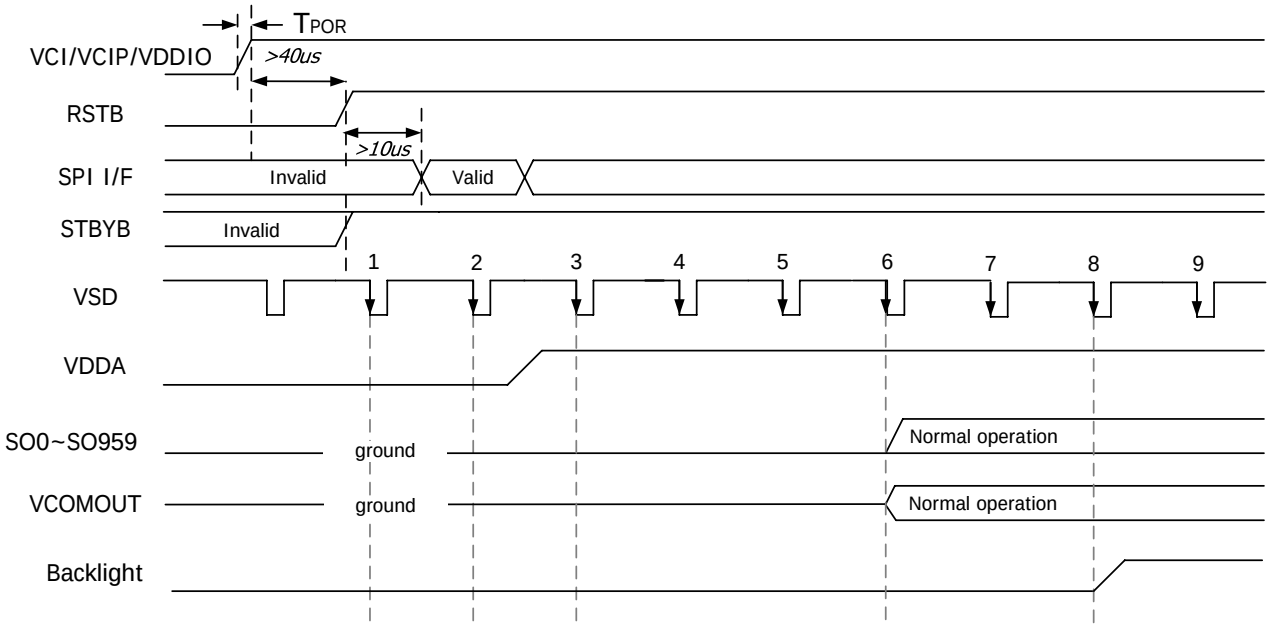
R1F OTP Operation Control Register

Bit	Name	Initial	R/W	Description
Bit[0]	OTPSEL	0b	R/W	OTP bank select.

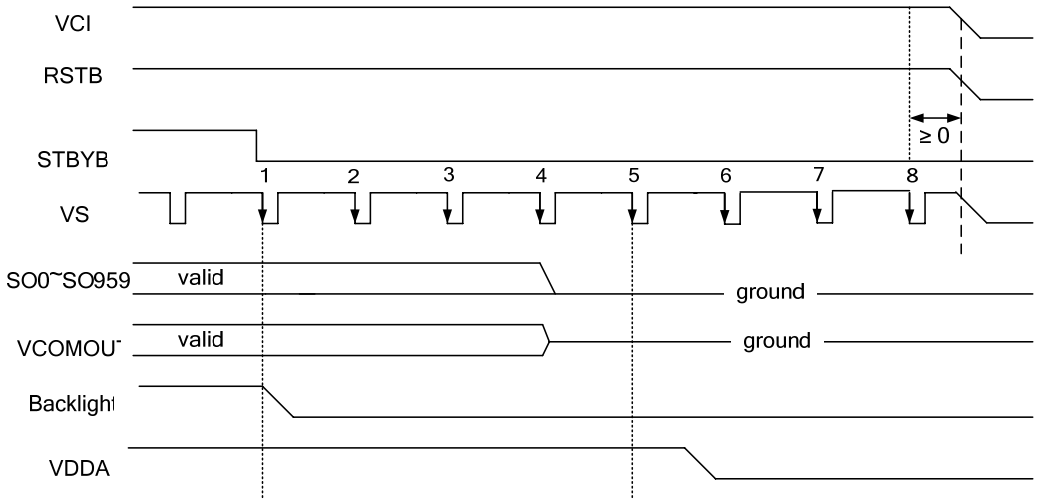
*Note: Burning data for VCDCSL/VCACSL **do not** need external HV power supply and can be programmed 3 times.

7. Power On/Off Sequence

7.1. Power-On Timing Sequence



7.2 Power-Off Timing Sequence



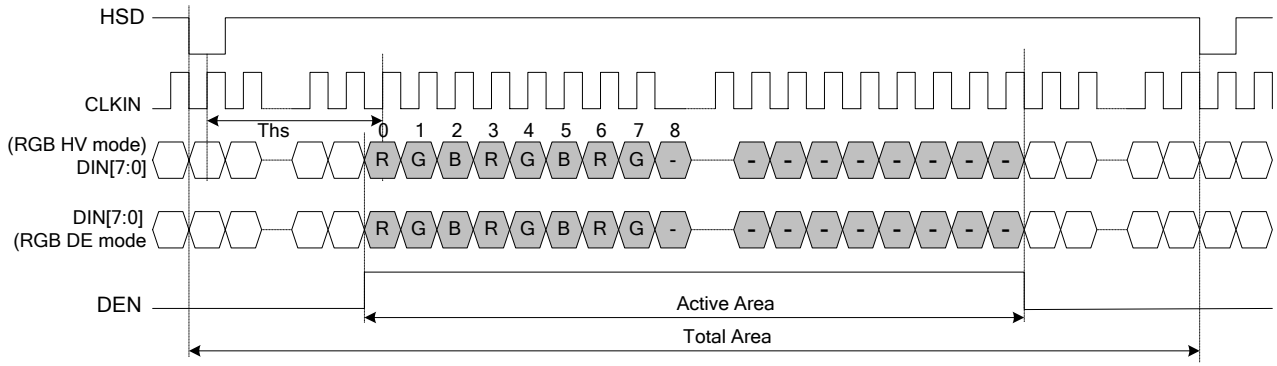
8. DC Electrical Characteristics

(Test Condition: VCI=VCIP=3.3V, VDDA=5.0V, VSS=GNDA=VSSP=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply Voltage	VCI	3.0	3.3	3.6	V	
I/O power supply	VDDIO	VDD	3.3	3.6	V	
Pump circuits supply	VCIP	3.0	3.3	3.6	V	
Low power supply	VDD	1.6	1.8	2.0	V	
Low Level Input Voltage	Vil	VSS	-	0.2xVDDIO	V	Digital input pins TA=25℃
High Level Input Voltage	Vih	0.8xVDDIO	-	VDDIO	V	Digital input pins TA=25℃
Input Leakage Current	Ii	-	-	±1	μA	Digital input pins
High Level Output Voltage	Voh	VDDIO-0.4	-	VDDIO	V	Digital output pins; Ioh=400μA
Low Level Output Voltage	Vol	VSS	-	VSS+0.4	V	Digital output pins; Iol= -400μA
2xVCI pump output level	VINT1	5.2	5.5	5.8	V	VCIP=3.3V, w/o panel loading
Analog power voltage	VDDA	4.5	5.0	VINT1-0.3	V	Analog circuit power from Power Block
VCOMAC output level	VCOMAC	4.6	-	VINT1-0.3		By VCSL[2:0] setting VCOMAC=$V_{(VCSL[3:0])}$±100mV
VCOMDC output level	VCOMDC	1.0	-	2.26		By VCDCSL[5:0] setting VCOMDC= $V_{(VCDCSL[5:0])}$±50mV
Positive power supply	VGH	14.5	15	15.5	V	Gate driver load + procard load
Negative power supply	VGL	-10	-8	-6	V	Gate driver load + procard load
Base drive current	IDRV	-	-	10	mA	VCIP=3.3V, DRV=0.7V
DRV output voltage	VDRV	VSS+0.1	-	VCI-0.1	V	
Feed back voltage	VFB	0.55	0.6	0.65	V	DC/DC operating, VBL current=20mA
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V~0.5V & VDDA-0.5V~VDDA-0.1V
			±15	±25	mV	Vo=0.5V~VDDA-0.5V
Low-Level Output Current of VCOMOUT	IOLF	-	-10	-	mA	Force VCOMAC=6.0V VCOMOUT output=0V V.S 0.9V
High-Level Output Current of VCOMOUT	IOHF	-	10	-	mA	Force VCOMAC=6.0V VCOMOUT output=6.0V V.S 5.1V
Source Low-Level Output Current	I_{OLS}	-	-30	-	μA	Son=Vo V.S. (Vo+0.9)
Source High-Level Output Current	I_{OHS}	-	30	-	μA	Son=Vo V.S. (Vo-0.9)
Gate Low-Level Output Current	IOLG	-	-250	-	μA	GOn; Vo=VGL V.S. (VGL+0.5)
Gate High-Level Output Current	IOHG	-	250	-	μA	GOn; Vo=VGL V.S. (VGH-0.5)
Chip Stand-by Current	Idds	-	15	50	μA	STBYB="0", all function are shutdown, CLKIN/VSD/HSD halted
Chip Operating Current	Idda	-	10	-	mA	No load, CLKIN=27MHz, Fld=15KHz

9. AC Electrical Characteristics

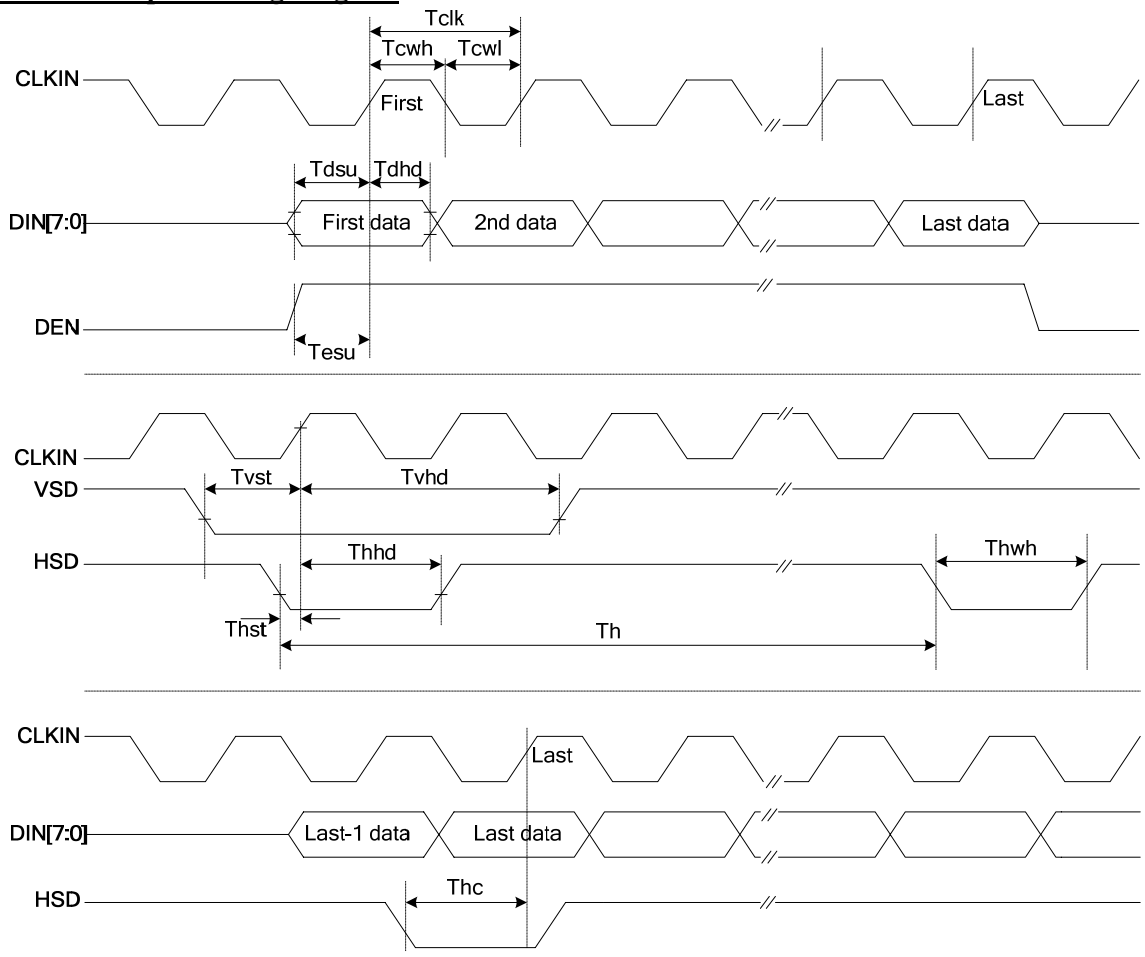
9.1 Input Data Format



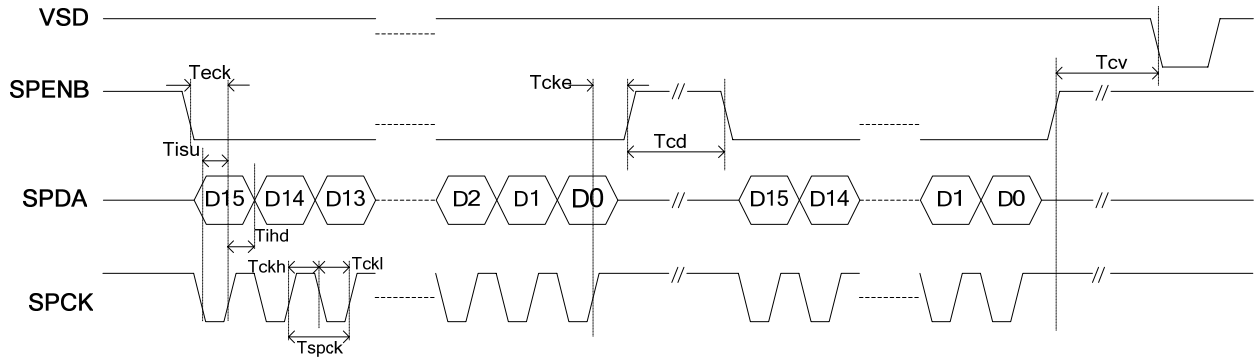
Input Format	Format Standard	CLKIN(MHz)	HSD(CLKIN)	Total Area (CLKIN)	Active Area (CLKIN)	Note
8bit RGB	8bit RGB	27	1	1716	960	960×240
24bit RGB	24bit RGB	6.4	1	408	320	

9.2. Time Diagram

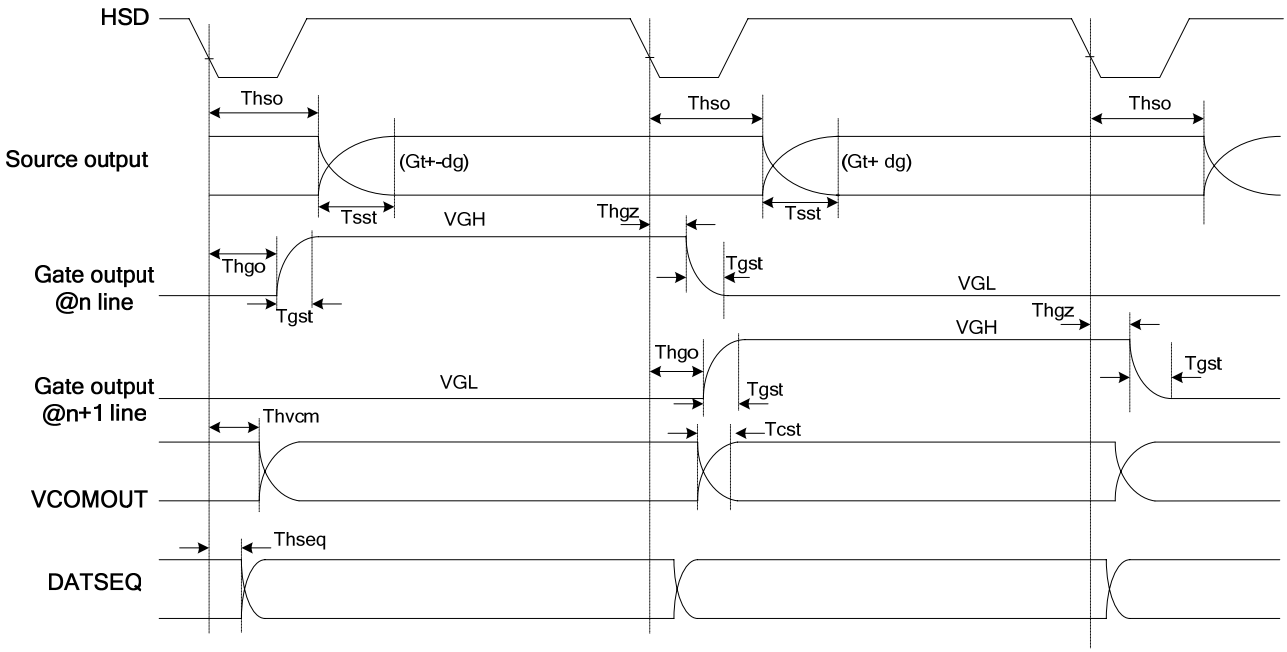
Clock and Data Input Timing Diagram



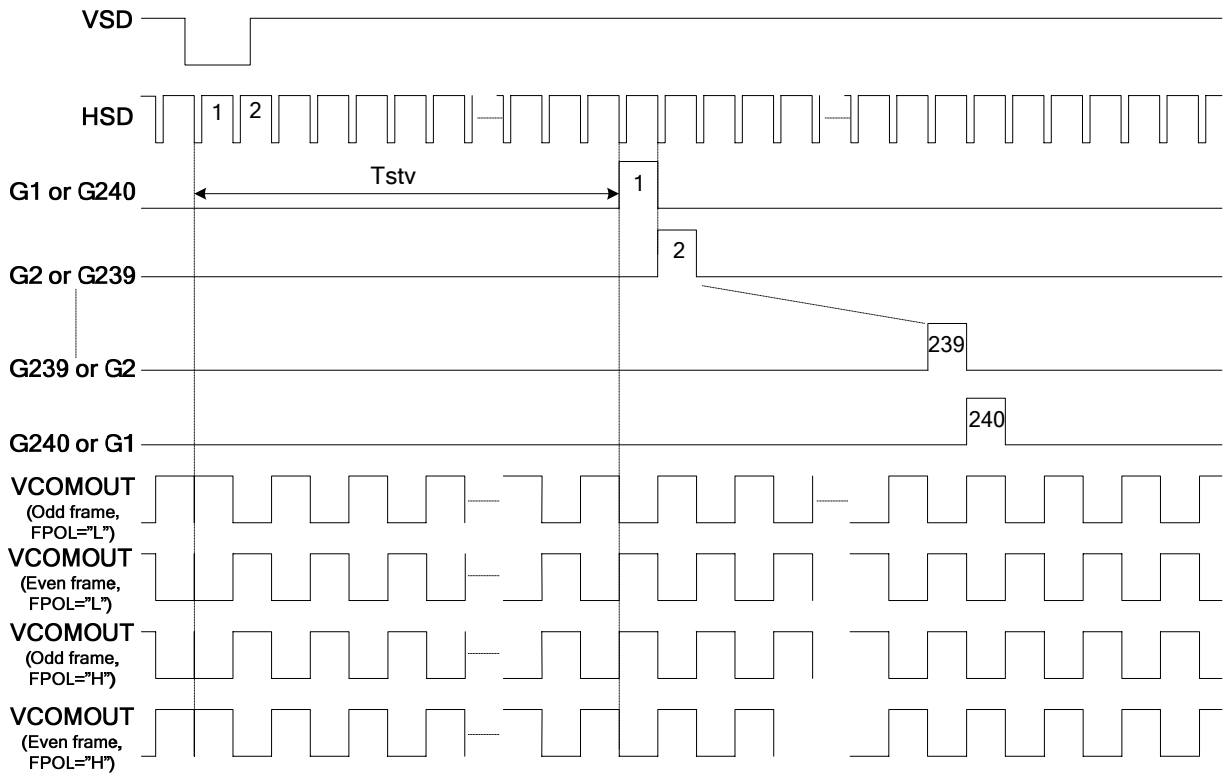
3-Wire Timing Diagram



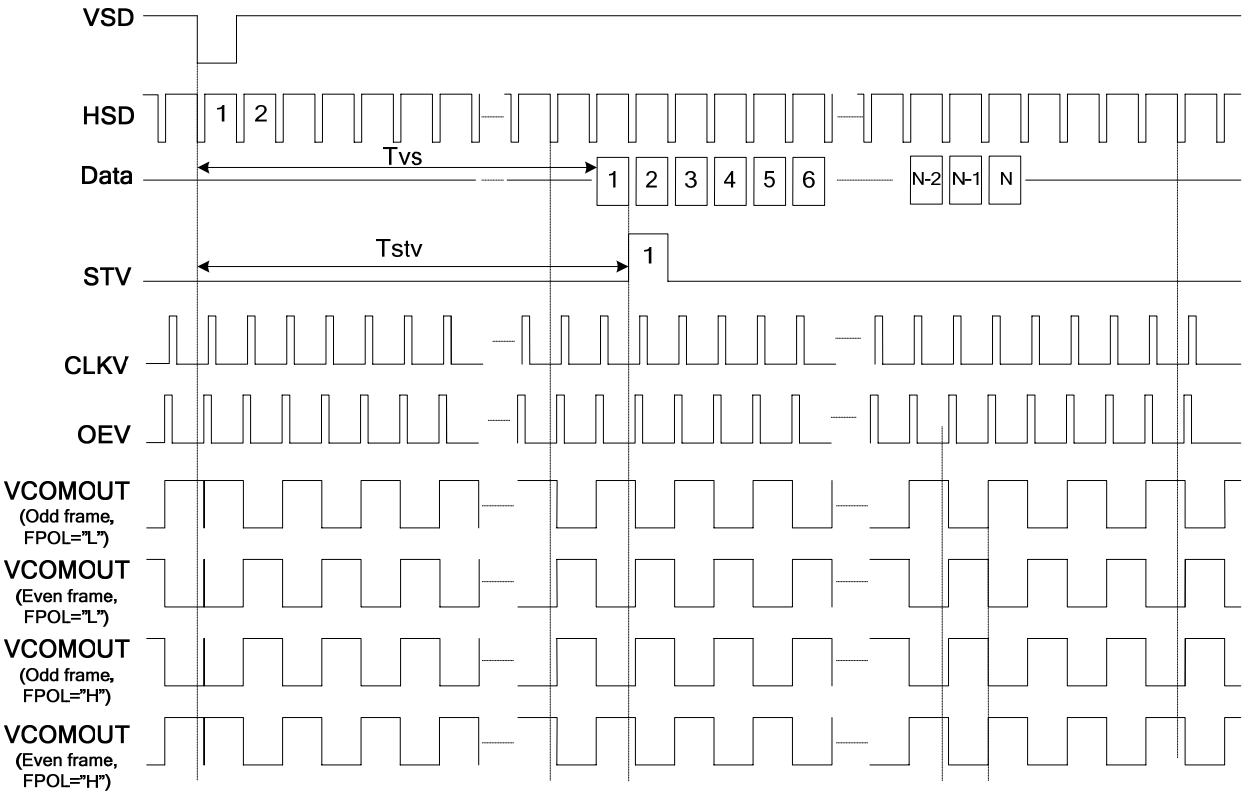
Source Driver Output Timing Diagram



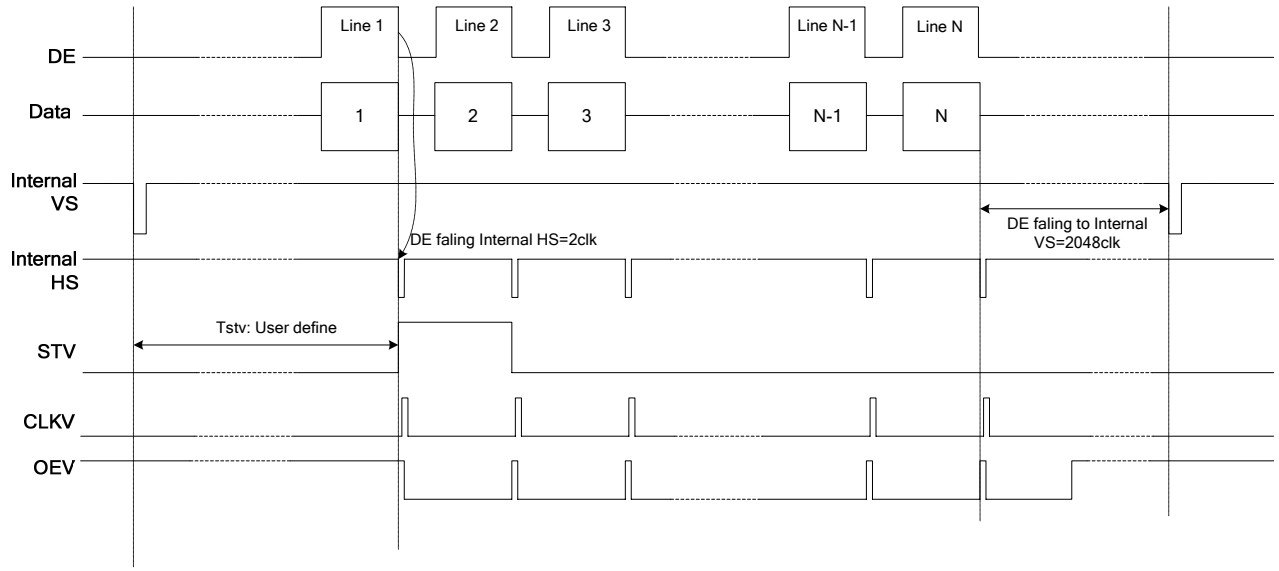
Gate Driver Output Timing Diagram



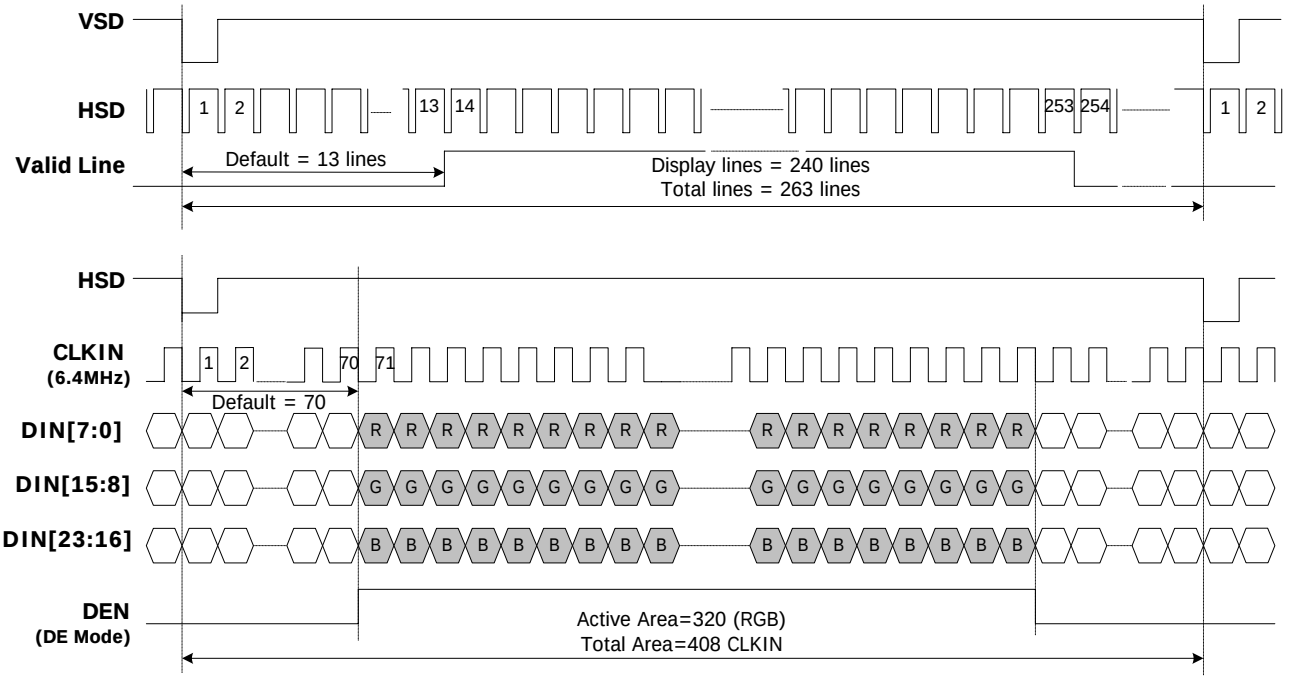
Vertical Timing Diagram (HV Mode)



Vertical Timing Diagram (DE Mode)



Input Data Timing (24 bit RGB mode for 960×240 @ SEL[3:0]=1100b)



9.3. Specifications

Test Condition: (VCI=VCIP=3.3V,VDDA=5.0V,VSS=GNDA=VSSP=0V,TA=25℃)

8 Bit RGB 960 CH Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27	30	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	35	70	255	CLKIN	DDLY=70,Offset=0(fixed)

24 Bit RGB Mode (@ SEL[3:0]=1100 or 1101)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	6.1	6.4	8.0	MHz	VDD=3.0~3.6V
CLKIN cycle time	Tclk	125	156	164	ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time that HSD to 1st data input(NTSC)	Ths	40	70	255	CLKIN	DDLY=70,Offset=0(fixed)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
System Operation Timing						
VDD power source slew time	T_{POR}			1000	us	From 0V to 90% VDD
RSTB active pulse width	T_{RSTB}	40			us	VDD=3.3V
Input Output Timing						
CLKIN clock time	Tclk	-		35.7	ns	Please refer to timing table(P25)
HSD to CLKIN	Thc	-	-	1	CLKIN	
HSD width	Thwh	1	-	-	CLKIN	
VSD width	Tvwh	1	-	-	Th	
HSD period time	Th	60	63.56	67	us	
VSD setup time	Tvst	12	-	-	ns	
VSD hold time	Tvhd	12	-	-	ns	
HSD setup time	Thst	12	-	-	ns	
HSD hold time	Thhd	12	-	-	ns	
Data set-up time	Tdsu	12	-	-	ns	DIN[23:0] to CLKIN
Data hold time	Tdhd	12	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	Tesd	12	-		ns	DEN to CLKIN
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@CIR601/8bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that CCIR_V to 1st line data input	Tvs	17	25	33	Th	@CCIR656 PAL mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Time that VSD to 1st line data input	Tvs	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting Tvs=HDLY[6:0]
Source output stable time 1	Tst	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	Tgst	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	Tcst	-	4	8	us	96% final, CL=33nF, RL=100ohm
3-wire serial communication AC timing						
Serial clock	Tspck	320	-	-	ns	
SPCK pulse duty	Tscdut	40	50	60	%	Tckh/Tspck
Serial data setup time	Tisu	120	-	-	ns	
Serial data hold time	Tihd	120	-	-	ns	
Serial clock high/low	Tssw	120	-	-	ns	
Chip select distinguish	Tcd	1	-	-	us	
SPENA to VSD	Tcv	1	-	-	us	
SPENB input setup time	Teck	150	-	-	Ns	
SPENB input hold time	Tcke	150	-	-	ns	

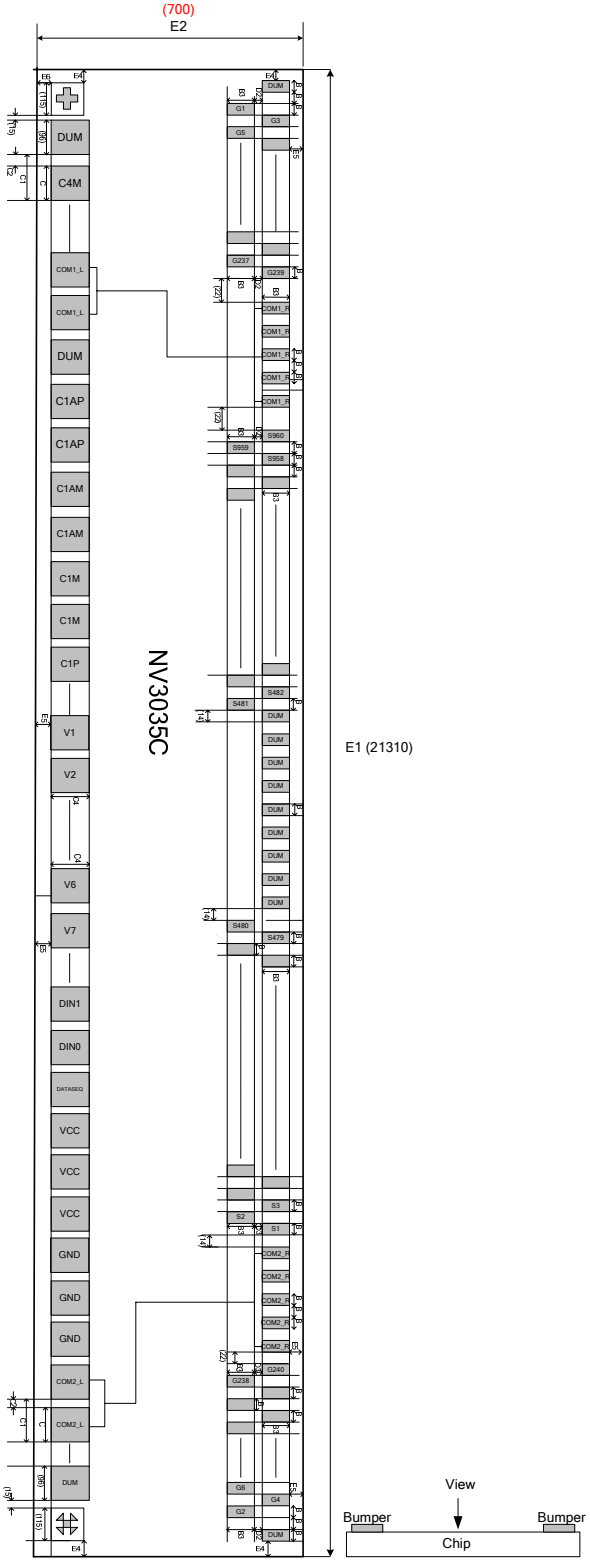
10. Absolute Maximum Ratings

Logic supply voltage, VCI	-0.5V to +5V
Analog supply voltage, VDDA	-0.5V to +7.5V
Supply voltage, VCIP	-0.5V to +5.5V
Supply voltage, V1~V6	-0.3~VDDA+0.3
VGH~VGL	-0.3~+25V
Storage temperature	-55℃ to +125℃
Operating temperature	-20℃ to +85 ℃

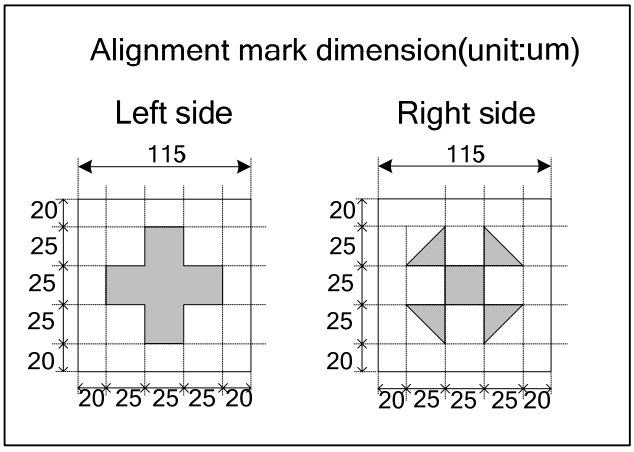
Stress above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11. Chip Bump Information

11.1. Pad Location



Alignment Mark



Bump Information

Symbol	Dimension(um)
B	17
B3	83
C	100
C1	127
C2	27
C4	90
D2	57
E1	21290(Max)
E2	680(Max)
E4	65(Max)
E5	57(Max)
E6	40

*Remark: Chip dimension include scribe line

Revision history

Version No.	Date	Page	Introduction
0.1	2012-12-6	All	New build.
0.2	2013-1-25	P29	DC Electrical Characteristics : VGL：-10（Min）；-8（Typ.）
0.3	2013-2-1	P46	Add Pad coordination： Alignment_L:（-10532.5，-222.5） Alignment_R:（-10532.5，-222.5）
0.4	2013-3-13	P26	VCACSL [3:0]：0101，level：5.1V(Default).
0.5	2013-08-27	P4	Revise SPSW descriptions: “1” is useless.
		P5	Add ATPE & VPP2 descriptions.
		P4,P5,P46	instead of TP0~TP18 with (STBYB,UPDN,SHLR,SEL[0…3],DUM, VDDIO,TEST2,TEST1,FPOL,CPMPDB,PWMPDB,DUM,ATPE).
		P19	Revise registers R03 init.: “CCh”.

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