**NOVATEK**

# NT3882

## Dot Matrix LCD 40-Channel Driver

### Features

- Provides a 40 channel LCD driver
- Internal serial to parallel conversion circuits:
  - 20-bit shift register X 2
  - 40-bit latch X 1
  - 40-bit 4 level driver X 1
- Logic circuit supply voltage range: 4.5V - 5.5V

- LCD driving voltage range ($V_{DD}$ - $V_{EE}$): 3.5V to 11V
- Applicable LCD duty cycle: 1/2 to 1/16
- Interfaces with a NT3881C/D LCD controller
- LCD bias voltage can be supplied externally
- Available in 64-pin QFP and in CHIP FORM

### General Description

The NT3882 is a dot matrix LCD 40 channel driver fabricated by low power CMOS technology. This IC consists of two 20-bit shift registers, a 40-bit latch, and a 40-bit 4 level LCD driver. The NT3882 converts serial data which is 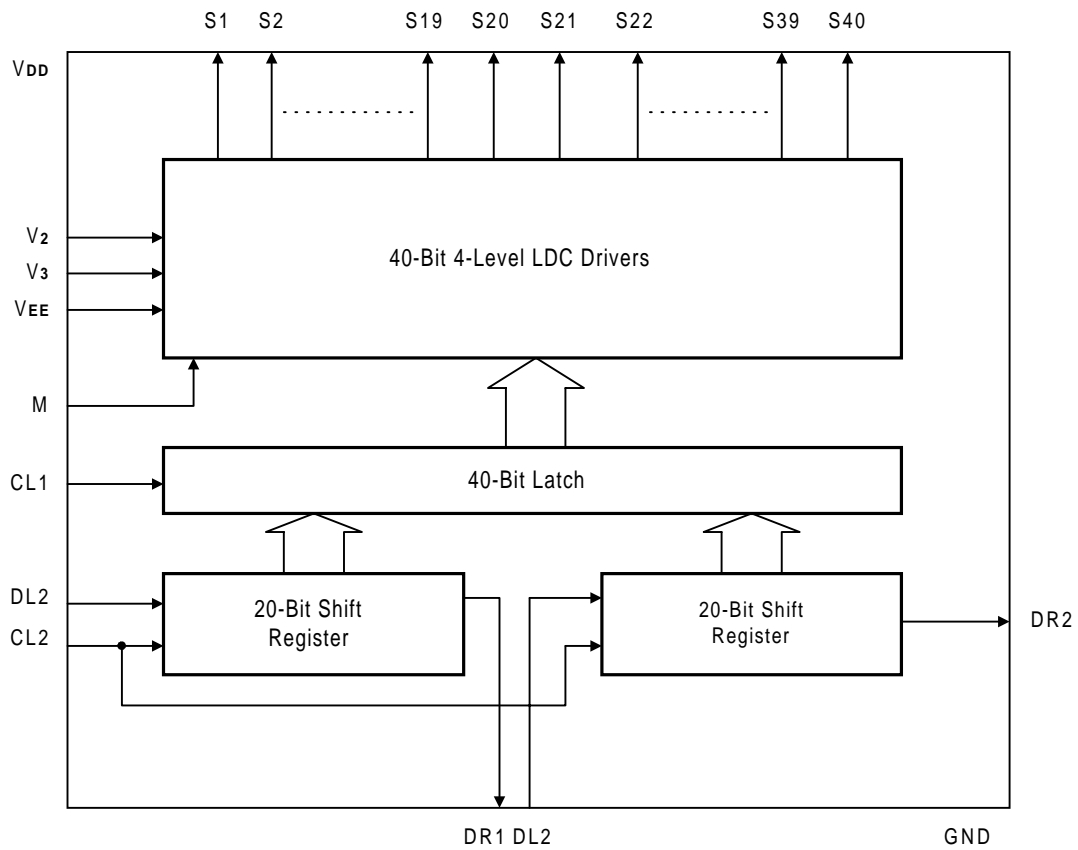received from the LCD controller (NT3881C/D) to parallel data and then outputs LCD driving waveforms to drive LCD. Expansion of character-type liquid crystal display can be easily obtained according to the number and structure of characters.

### Pin Configuration
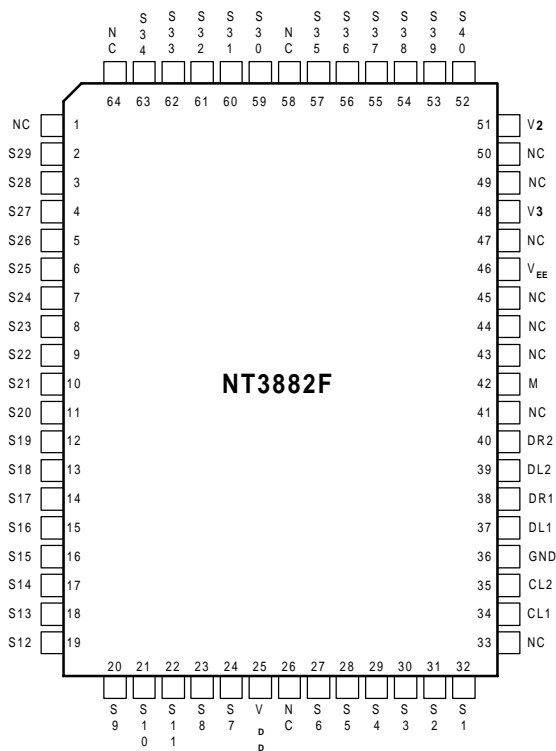


### Pad Configuration
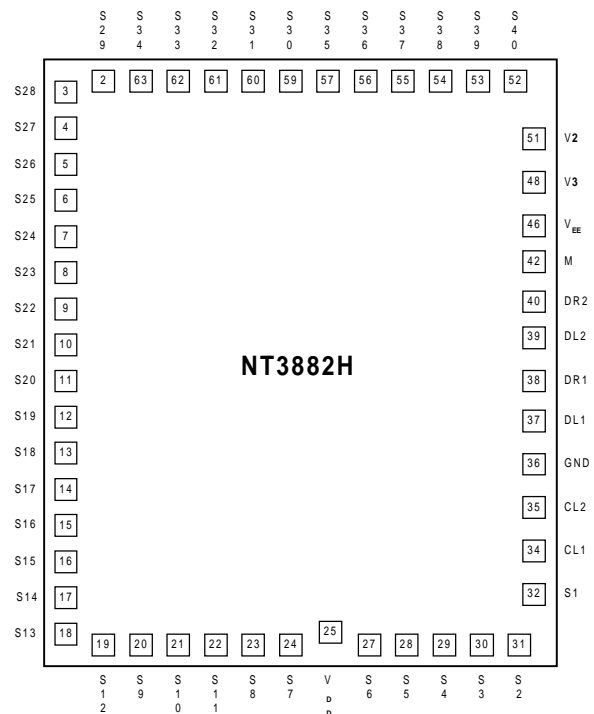
**Block Diagram**

## Pin and Pad Descriptions

| Pin No. | Pad No. | Designation | I/O | External Connection | Description |
|---|---|---|---|---|---|
| 2- 24, 27 - 32, 52 - 57, 59 - 63 | 27 - 32, 2 - 24, 52 - 57, 59 - 63 | S29 - S7, S6 - S1, S40 - S35, S30 - S34 | O | LCD panel | Segment signal output pins |
| 25 | 25 | V$_{DD}$ | P | Power supply | Power for logic circuits |
| 34 | 34 | CL1 | I | Controller | Clock to latch serial data |
| 35 | 35 | CL2 | I | Controller | Clock to shift serial data |
| 36 | 36 | GND | P | Power Supply | 0V |
| 37 | 37 | DL1 | I | Controlleror NT3882 | Data input of 1 - 20 bits from controller |
| 38 | 38 | DR1 | O | NT3882 | Data output of 20 bit shift register |
| 39 | 39 | DL2 | I | Controlleror NT3882 | Data input of 21 - 40 bits from controller |
| 40 | 40 | DR2 | O | NT3882 | Data output of 40 bit shift register |
| 42 | 42 | M | I | Controller | Alternate signal for LCD drivers |
| 46, 48,  51 | 46, 48, 51 | V$_{EE}$, V$_3$, V$_2$ | P | Power Supply | Power for LCD drivers |
| 1, 26, 33, 41, 43 - 45, 47, 49, 50, 58, 64 | - | NC | - | - | No connection |

## Functional Description

NT3882 is a dot matrix LCD segment driver LSI. It operates with the controller, such as NT3881C/D, and/or another segment driver LSI NT3882. NT3882 receives serial data from the controller or another NT3882, converts it to parallel data and then supplies the LCD driving waveforms to the LCD panel.

### 1. CL1

This signal is used for latching the shift register contents. When CL1 is set at high, the shift register contents are transferred to the 40-bit 4level LCD driver. When CL1 is set at low, the last display output data (S1 to S40) is held.

### 2. CL2

Clock pulse inputs for the two 20-bit shift registers. The data is shifted to a 40-bit latch at the falling edge of CL2. The clock singal CL2 must be active when operating to refresh shift registers' contents.

### 3. DL1

The 1 - 20 bit data from LCD controller is fed into the first 20-bit shift register through DL1.

### 4. DR1

The 20th bit data of first 20-bit shift register output from DR1. The data shifted out from DR1 after 20 bit delay are synchronized with the clock pulse (CL2). By connecting DR1 to DL2, two 20-bit shift registers can be cascaded to one 40-bit  shift register.

### 5. DL2

The 21 - 40 bit data from the LCD controller is fed into the second 20-bit shift register through DL2.

### 6. DR2

The 40th bit data of the second 20-bit shift register output is from DR2. The data shifted out from DR2 after a 20-bit delay is synchronized with the clock pulse (CL2). By connecting DR2 to the next NT3882 DL1, the cascade construction is obtained to drive a wider LCD panel.

### 7. S1 to S40

These 40 bits represent the 40 data bits in the 40-bit latch. One of V$_{DD}$, V$_2$, V$_3$ and V$_{EE}$ is selected as a LCD driving voltage source according to the combination of latched data level and the alternate signal (M).

**The truth table is listed as follows:**

| Latched Data | M | Output level of S1 to S40 |
|---|---|---|
| 1(High) | 1(High) | $V_{EE}$ |
| (Selected) | 0(Low) | $V_{DD}$ |
| 0(Low) | 1(High) | $V_3$ |
| (Nonselected) | 0(Low) | $V_2$ |

## Absolute Maximum Ratings*

Power Supply Voltage ($V_{DD}$-GND) . . . . . . . -0.3V to 7.0V
Power Supply Voltage ($V_{DD}$-$V_{EE}$) . . . . . . . . . . . . . . . . .
. . . . . . . . . . . . . . . . . . . . . $V_{DD}$ - 13.5V to $V_{DD}$ + 0.3V
Input Voltage . . . . . . . . . . . . . . . . .-0.3V to $V_{DD}$ + 0.3V
Operating Temperature . . . . . . . . . . . . . -20°C to + 75°C
Storage Temperature . . . . . . . . . . . . . .-55°C to + 125°C

## *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposed to the absolute maximum rating conditions for extended periods may affect device reliability.

## DC Electrical Characteristics  ($V_{DD}$ = 5.0V, GND = 0V, $V_{EE}$ = 0V, $T_A$ = 25°C)

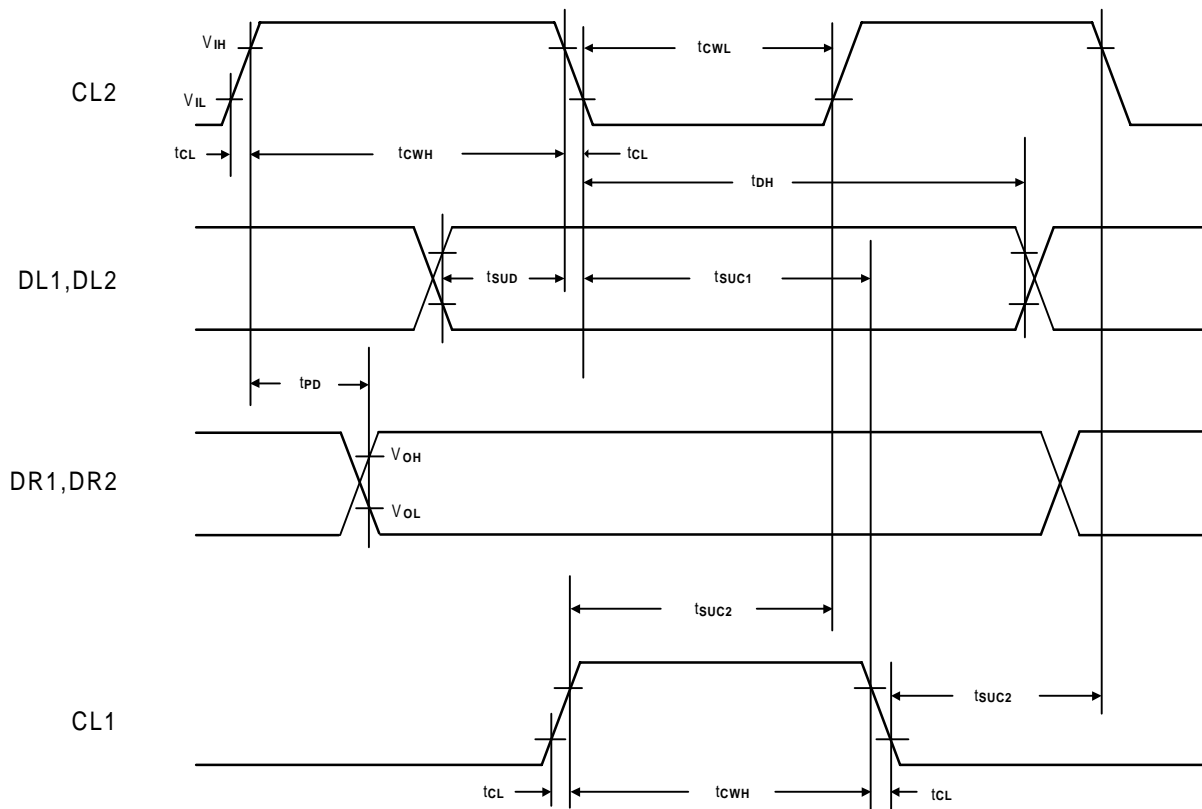| Symbol | Parameter | Terminal | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input Voltage | CL1, CL2 | 0.7 X $V_{DD}$ | - | $V_{DD}$ | V | |
| $V_{IL}$ | | DL1, DL2 | 0 | - | 0.3 X $V_{DD}$ | V | |
| $V_{OH}$ | Output Voltage | DR1, DR2 | $V_{DD}$ - 0.4 | - | - | V | $I_{OH}$ = -0.4mA |
| $V_{OL}$ | | | - | - | 0.4 | V | $I_{OL}$ = 0.4mA |
| $V_{D1}$ | Vi-Sj Voltage | Note 1 | - | - | 1.1 | V | $I_{ON}$ = 0.1mA for one of Sj |
| $V_{D2}$ | Descending | | | | 105 | V | $I_{ON}$ = 0.05mA for each of Sj |
| $I_{IL}$ | Input Leakage Current | CL1, CL2 DL1, DL2 | -5 | - | 5 | μA | $V_{IN}$ = 0 or VDD |
| $I_{VL}$ | Vi Leakage Current | $V_2$, $V_3$, $V_{EE}$ | -10 | - | 10 | μA | S1 to S40 open |
| $I_{DD}$ | Power Supply Current | Note 2 | - | - | 200 | μA | $f_{CL1}$ = 1KH $f_{CL2}$ = 400KHz |

Note 1: $V_i$ - $S_j$ ($V_i$ = $V_{DD}$, $V_2$, $V_3$, $V_{EE}$; j = 1 to 40) equivalent circuit.
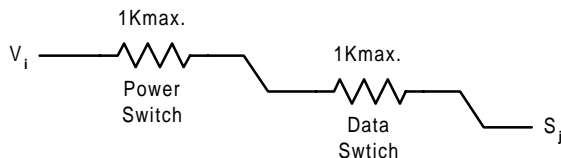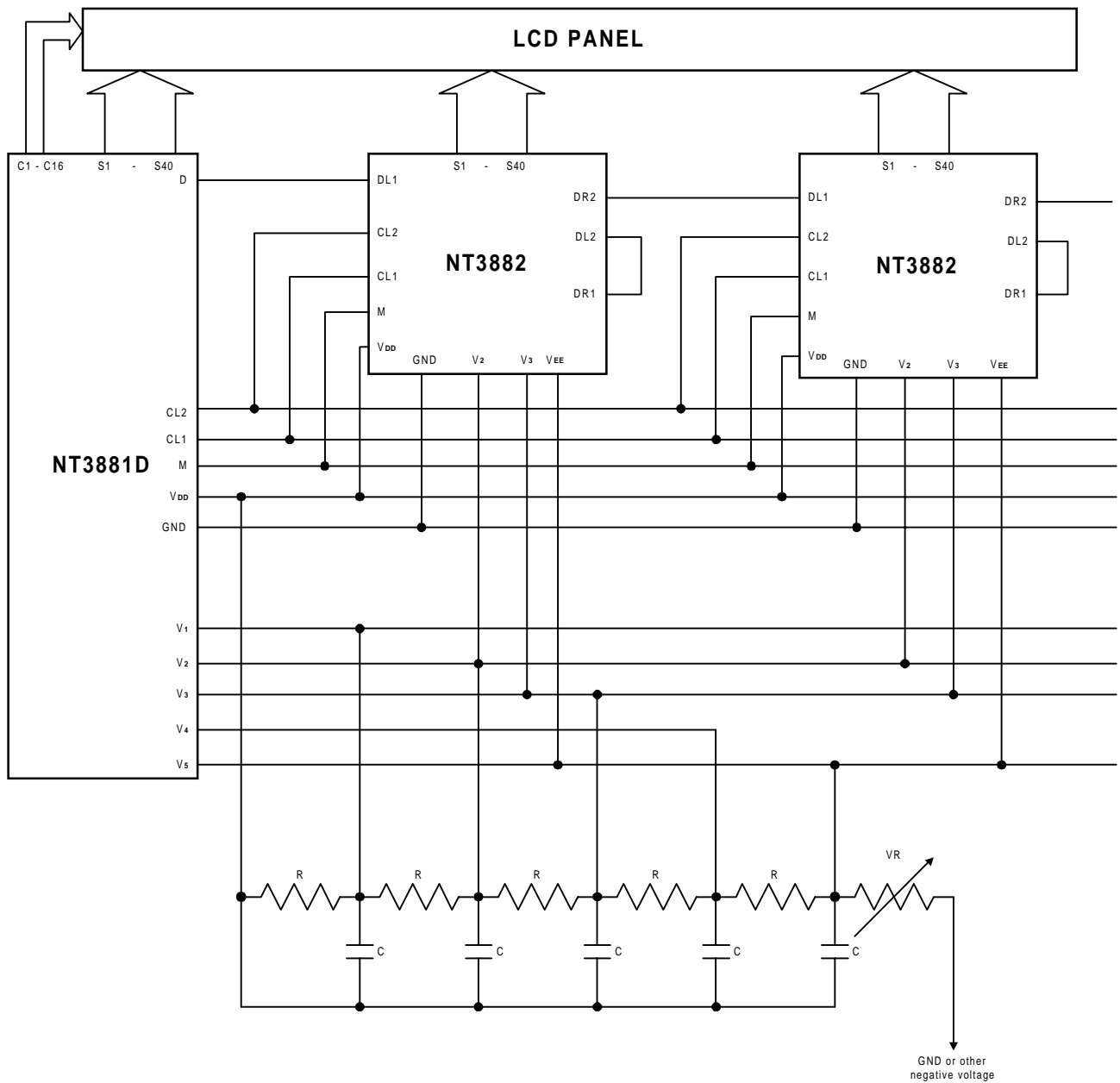


Note 2:  Input/output current is excluded. When the input is at the intermediate level with CMOS, some excessive current will flow through the input circuit to the power supply. To avoid this, the input level must be fixed at a high or low state.

**AC Characteristics** ($V_{DD}$ = 5.0V, GND = 0V, $V_{EE}$ = 0V, $T_A$ = 25°C)

| Symbol | Parameter | | Terminal | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $f_{CL2}$ | Data Shift Frequency | | CL2 | - | - | 400 | KHz |
| $t_{CWH}$ | Clock Width | High | CL1, CL2 | 800 | - | - | ns |
| $t_{CWL}$ | | Low | CL2 | 800 | - | - | ns |
| $t_{DH}$ | Data Hold Time | | DL1, DL2 | 300 | - | - | ns |
| $t_{SUD}$ | Data Set-up Time | | DL1, DL2 | 300 | - | - | ns |
| $t_{SUC1}$ | Clock Set-up Time (CL2 $\rightarrow$ CL1) | | CL1, CL2 | 500 | - | - | ns |
| $t_{SUC2}$ | Clock Set-up Time (CL1 $\rightarrow$ CL2) | | CL1, CL2 | 500 | - | - | ns |
| $t_{CL}$ | Clock Rise/Fall Time | | CL1, CL2 | - | - | 200 | ns |
| $t_{PD}$ | Data Delay Time | | - | 75 | - | 500 | ns |

**Timing Waveforms**



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**Application Circuit** (for reference only)

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## Bonding Diagram



\* Connecting IC substrate to $V_{DD}$ or keeping floating is recommended.

\* Pad window area120μm X 100μm.

## Bonding Dimensions

unit: µm

| Pad No. | Designation | X | Y | Pad No. | Designation | X | Y |
|---|---|---|---|---|---|---|---|
| 2 | S29 | -729 | 1148 | 29 | S4 | 621 | -1148 |
| 3 | S28 | -985 | 1125 | 30 | S3 | 771 | -1148 |
| 4 | S27 | -985 | 975 | 31 | S2 | 921 | -1148 |
| 5 | S26 | -985 | 825 | 32 | S1 | 985 | -859 |
| 6 | S25 | -985 | 675 | 34 | CL1 | 985 | -705 |
| 7 | S24 | -985 | 525 | 35 | CL2 | 985 | -555 |
| 8 | S23 | -985 | 375 | 36 | GND | 985 | -373 |
| 9 | S22 | -985 | 225 | 37 | DL1 | 985 | -204 |
| 10 | S21 | -985 | 75 | 38 | DR1 | 985 | -54 |
| 11 | S20 | -985 | -75 | 39 | DL2 | 985 | 96 |
| 12 | S19 | -985 | -225 | 40 | DR2 | 985 | 246 |
| 13 | S18 | -985 | -375 | 42 | M | 985 | 396 |
| 14 | S17 | -985 | -525 | 46 | $V_{EE}$ | 985 | 562 |
| 15 | S16 | -985 | -675 | 48 | $V_3$ | 985 | 722 |
| 16 | S15 | -985 | -825 | 51 | $V_2$ | 985 | 882 |
| 17 | S14 | -985 | -975 | 52 | S40 | 921 | 1148 |
| 18 | S13 | -985 | -1125 | 53 | S39 | 771 | 1148 |
| 19 | S12 | -729 | -1148 | 54 | S38 | 621 | 1148 |
| 20 | S9 | -579 | -1148 | 55 | S37 | 471 | 1148 |
| 21 | S10 | -429 | -1148 | 56 | S36 | 321 | 1148 |
| 22 | S11 | -279 | -1148 | 57 | S35 | 171 | 1148 |
| 23 | S8 | -129 | -1148 | 59 | S30 | 21 | 1148 |
| 24 | S7 | 21 | -1148 | 60 | S31 | -129 | 1148 |
| 25 | $V_{DD}$ | 171 | -1090 | 61 | S32 | -279 | 1148 |
| 27 | S6 | 321 | -1148 | 62 | S33 | -429 | 1148 |
| 28 | S5 | 471 | -1148 | 63 | S34 | -579 | 1148 |

## Ordering Information

| Part No. | Package |
|---|---|
| NT3882H | CHIP FORM |
| NT3882F | 64L QFP |

## Package Information

### QFP 64L Outline Dimensions
unit: inches/mm
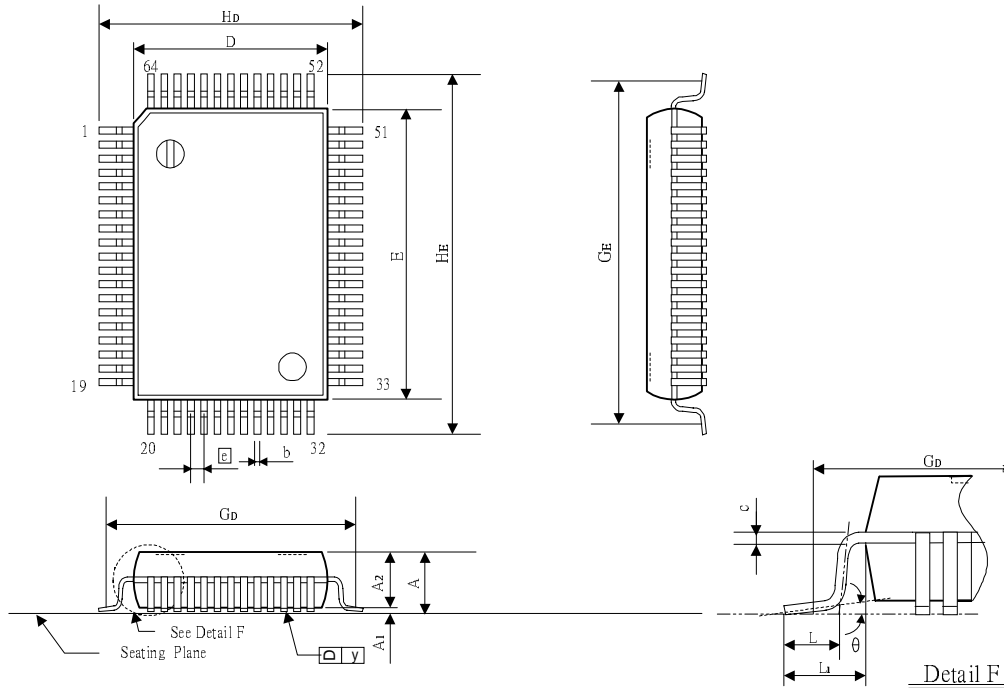


| Symbol | Dimensions in inches | Dimensions in mm |
|---|---|---|
| A | 0.130 Max. | 3.30 Max. |
| A1 | 0.004 Min. | 0.10 Min. |
| A2 | 0.112 ± 0.005 | 2.85 ± 0.13 |
| b | 0.016  +0.004 -0.002 | 0.40  +0.10 -0.05 |
| c | 0.006  +0.004 -0.002 | 0.15  +0.10 -0.05 |
| D | 0.551 ± 0.005 | 14.00 ± 0.13 |
| E | 0.787 ± 0.005 | 20.00 ± 0.13 |
| e | 0.039 ± 0.006 | 1.00 ± 0.15 |
| GD | 0.693 NOM. | 17.60 NOM. |
| GE | 0.929 NOM. | 23.60 NOM. |
| HD | 0.740 ± 0.012 | 18.80 ± 0.31 |
| HE | 0.976 ± 0.012 | 24.79 ± 0.31 |
| L | 0.047 ± 0.008 | 1.19 ± 0.20 |
| L1 | 0.095 ± 0.008 | 2.41 ± 0.20 |
| y | 0.006 Max. | 0.15 Max. |
| θ | 0° ~ 12° | 0° ~ 12° |

**Notes:**

1. Dimensions D & E do not include resin fins.
2. Dimensions $G_D$ & $G_E$ are for PC Board surface mount pad pitch design reference only.

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