NOVATEK
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Data Sheet

NT39411

TFT LCD Source Driver

V0.6

Preliminary Spec

Index

Revise History

NT39411 Specification Revision History			
Version	**Content**	**Page**	**Date**
0.6	Modify DIO1/DIO2 description	7	2007/8/17
0.5	Revise Timing Diagram 1.2 TTL mode Revise DC Electrical Characteristics Revise Document Format	17 14 All	2006/7/24 2006/8/25 2006/8/30
0.4	Modify Features and General Description Add Pin and Pad Descriptions “CLKN” Modify Pin and Pad Description “CHNSL”, “CHNDS” Modify Output Voltage VS Input Data Modify DC Electrical Characteristics	4 7 8 11,12 13,14	2006/7/11 2006/7/12
0.3	Revise all	All	2006/6/13
0.2	Revise Pin Assignment Chip Outline Dimension (Bump size) Align Mark and Dimension Table Block Diagram	5 16 17 6	2006/4/14
0.1	New Release	-	2006/4/12

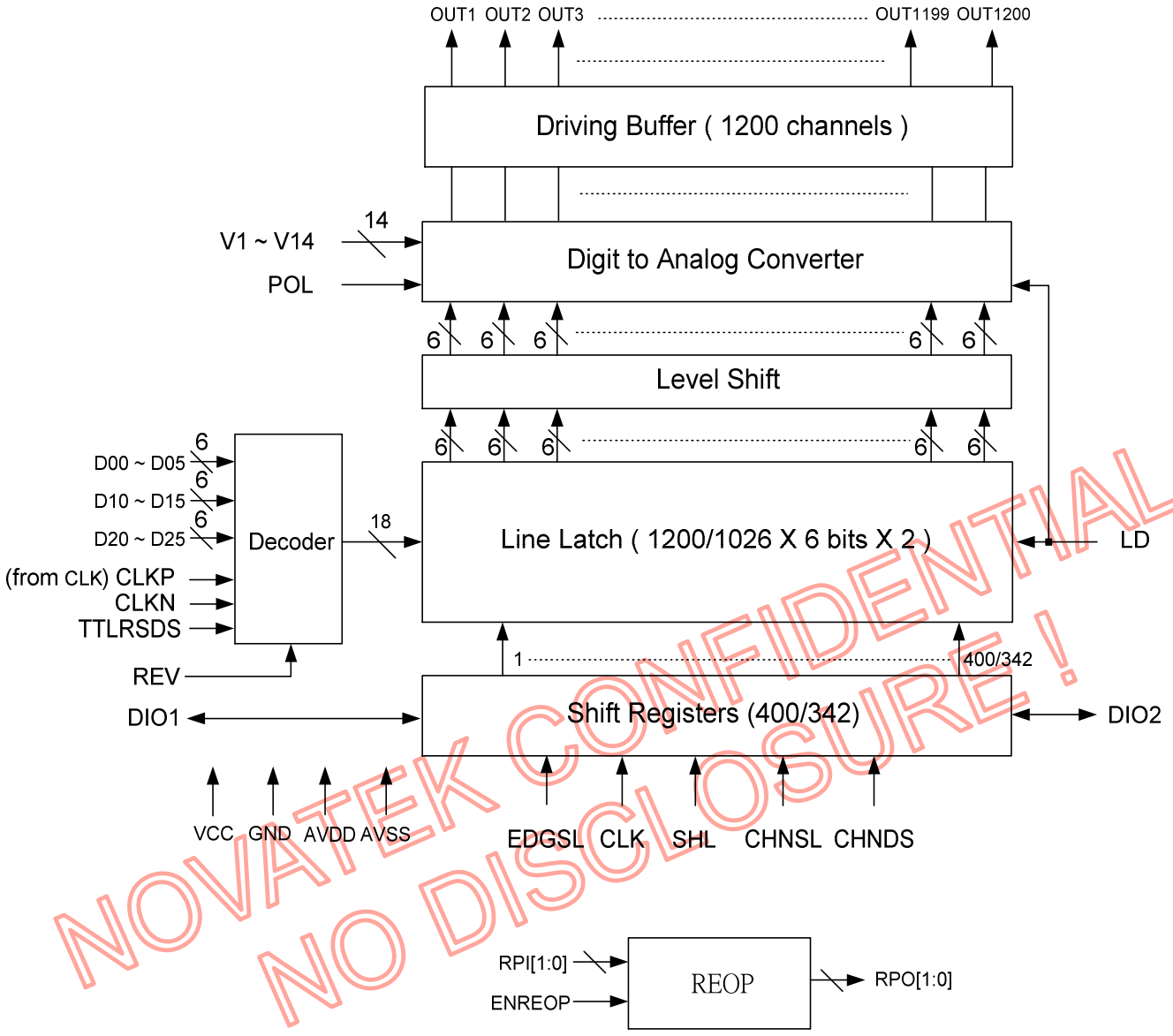
Features

- Output: 1200/1026 output channels
- 6-bit resolution / 64 gray scale
- Dot inversion with polarity control
- V1 ~ V14 for adjusting Gamma correction
- Power of LCD driving voltage: 6.5 ~ 13.5V
- Output dynamic range: 0.1 ~ AVDD-0.1V
- Power consumption of analog circuit: 12mA
- Power for interface circuit: 2.7 ~ 3.6V
- Operating frequency: 50 MHz
- Output deviation: ±20mV
- Data inverting for reducing EMI
- Cascade function with bi-direction shift control
- Build in 2 repair OP
- CMOS silicon gate (p-type substrate)
- COG package

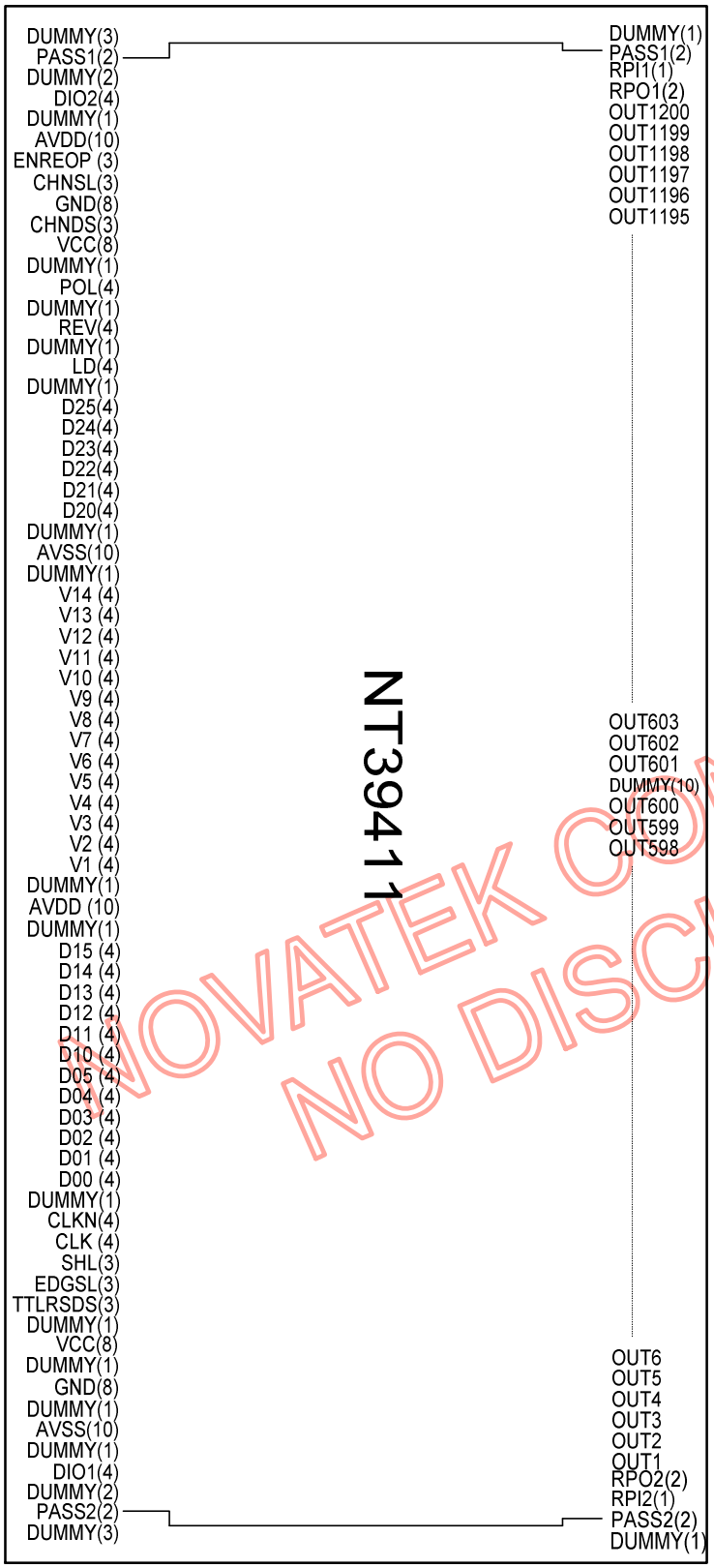
General Description

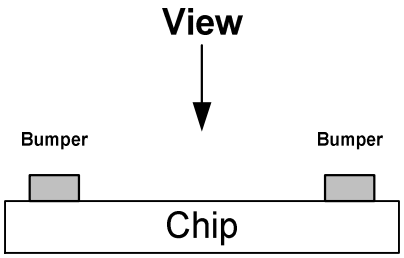
NT39411 is a 1200/1026 channel data driver IC with TTL/RSDS interface for color TFT LCD panels . For lower power dissipation , the circuit architecture with a special method is designed , and dot inversion is suggested on application. For better performance, a wide range of supply voltages and small output deviations are designed in this chip. This chip also supplies 14 sections of voltage-reference select for gamma correction. And the power dissipation on the gamma correction resistors is also concerned, making this chip more suitable for mid or small sized color TFT panels.

Function Block Diagram



Pad Sequence (Bump Side)





Pad Description

<table>
<tr><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">Input signal</td></tr>
<tr><td>D05 ~ D00
D15 ~ D10
D25 ~ D20</td><td>I</td><td>These pins can be used as TTL or RSDS data input by TTLRSDS pin setting. For RSDS input mode, the 3-bit differential input pairs generate the internal 6-bit data through the comparison between DxxP and DxxN. For TTL input mode as D00 ~ D05, D10 ~ D15, D20 ~ D25 input pin.
<table>
<tr><th>Pin name</th><th>RSDS input mode
TTLRSDS = H</th><th>TTL input mode
TTLRSDS = L</th></tr>
<tr><td>D04 , D02 , D00</td><td>D0[2:0]N</td><td>D04 , D02 , D00</td></tr>
<tr><td>D05 , D03 , D01</td><td>D0[2:0]P</td><td>D05 , D03 , D01</td></tr>
<tr><td>D14 , D12 , D10</td><td>D1[2:0]N</td><td>D14 , D12 , D10</td></tr>
<tr><td>D15 , D13 , D11</td><td>D1[2:0]P</td><td>D15 , D13 , D11</td></tr>
<tr><td>D24 , D22 , D20</td><td>D2[2:0]N</td><td>D24 , D22 , D20</td></tr>
<tr><td>D25 , D23 , D21</td><td>D2[2:0]P</td><td>D25 , D23 , D21</td></tr>
</table></td></tr>
<tr><td>REV</td><td>I</td><td>Controls whether the data of D00~D25 are inverted or not, normally pulled low. When “REV”=1 these data will be inverted. EX. “00” → “ 3F”, “07”→ “ 38”, “15”→ “2A”, and so on.</td></tr>
<tr><td>CLK</td><td>I</td><td>Clock input. When RSDS input mode, CLK is used as CLKP input pin. Latching source data onto the line latches at the rising or falling edge by EDGSL signal selected.</td></tr>
<tr><td>CLKN</td><td>I</td><td>The RSDS clock input pairs generate the internal shift clock through the comparison between CLKP and CLKN. When TTL mode , tie to GND.</td></tr>
<tr><td>V1 ~ V14</td><td>I</td><td>Gamma correction reference voltage. The voltage of these pins must be AVSS<V14<V13<V12<V11<V10<V9< V8; V7< V6<V5<V4<V3<V2<V1< AVDD</td></tr>
<tr><td>SHL</td><td>I</td><td>Select left or right shift, normally pulled high.
SHL=“1” : DIO1→ OUT1,2,3 → OUT4,5,6 --→ OUT1198,1199,1200 = DIO2
SHL=“0” : DIO1= OUT1,2,3 ← OUT4,5,6 ←- OUT1198,1199,1200 ← DIO2
<table>
<tr><th>SHL</th><th>DIO1</th><th>DIO2</th><th>SHIFT</th></tr>
<tr><td>1</td><td>Input</td><td>Output</td><td>Right</td></tr>
<tr><td>0</td><td>Output</td><td>Input</td><td>Left</td></tr>
</table></td></tr>
<tr><td>DIO1
DIO2</td><td>I/O</td><td>Start pulse signal input/output.
When SHL is applied high (SHL=”1”), a start high-pulse on DIO1 is latched at the rising edge of the CLK. Then the data are latched serially onto internal latches at the rising or falling edge of the CLK. After all line latches are full with data, 340/342/400 or 170/171/200 clocks, a pulse is shifted out through the DIO2 pin at the rising edge of the CLK. This function can cascade two or more devices for dot-size expansion. In normal applications, the DIO2 signal of the first device is connected to the DIO1 of the second stage, and the DIO2 of the second one is connected to the DIO1 of the third, and so on like a daisy chain. In contrast , when SHL is applied low, a start pulse inputs on DIO2, and a pulse outputs through DIO1.
*Remark: The input pulse-width of DIO1/2 may be over 1 clock-cycle.</td></tr>
<tr><td>EDGSL</td><td>I</td><td>Clock edge selected, normally pulled low.
When EDGSL= “0”, Latching source data onto the line latches at the rising edge.
When EDGSL= “1”, Latching source data onto the line latches at the rising edge and falling edge.
*Remark: Please reference Timing Diagram 2.1 Clock and data input timing diagram 1.</td></tr>
</table>

<table>
<tr><td>LD</td><td>I</td><td>Latches the polarity of outputs and switches the new data to outputs.
1. At the rising edge, latches the “POL” signal to control the polarity of the outputs.
2. The pin also controls the switch of the line registers that switches the new incoming data to outputs.
*Remark: The LD may switch the new data to outputs at any time even if the line data are not completely full.</td></tr>
<tr><td>POL</td><td>I</td><td>Polarity selector for the dot-inversion control. Available at the rising edge of LD. “POL” value is latched at the rising edge of “LD” to control the polarity of the even or odd outputs. “POL=1” represents that even outputs are of positive polarity with a voltage ranging from V1 to V7, and odd outputs are of negative polarity with a voltage ranging from V8 to V14. On the other hand, if LD has low level “POL”, even outputs are of negative polarity and odd outputs are of positive.
POL=1: Even outputs range from V1~V7, and Odd outputs range from V8~V14
POL=0: Even outputs range from V8~V14, and Odd outputs range from V1~V7</td></tr>
<tr><td>ENREOP</td><td>I</td><td>ENREOP = H : Enable repair line OP RPI1/2 , RPO1/2.
ENREOP = L or open : Disable repair line OP RPI1/2 , RPO1/2.
(default ENREOP = L)</td></tr>
<tr><td>TTLRSDS</td><td>I</td><td>TTLRSDS = H : RSDS data input
TTLRSDS = L or open : TTL data input (default TTLRSDS = L)</td></tr>
<tr><td>CHNSL</td><td>I</td><td>Output channel selection , default CHNSL = H,
<table>
<tr><th>CHNSL</th><th>Output channel</th><th>Disable channel</th></tr>
<tr><td>H</td><td>1200</td><td>none</td></tr>
<tr><td>L</td><td>1026(CHNDS = L)</td><td>OUT514 ~ OUT687</td></tr>
</table></td></tr>
<tr><td>CHNDS</td><td>I</td><td>Additional disable channel selection for 1026 channel mode only, default CHNDS = L(none additional disable channel).
<table>
<tr><th>CHNSL</th><th>CHNDS</th><th>Output channel</th><th>Disable channel</th></tr>
<tr><td>H</td><td>L</td><td>1200</td><td>none</td></tr>
<tr><td rowspan="2">L</td><td>L</td><td>1026</td><td>OUT514 ~ OUT687</td></tr>
<tr><td>H</td><td>1020</td><td>OUT514 ~ OUT687,
OUT1195 ~ OUT1200</td></tr>
</table>
Note : CHNSL = “H” and CHNDS = “H” is inhibited.</td></tr>
<tr><td colspan="3">Power</td></tr>
<tr><td>AVDD</td><td>PI</td><td>Power supply for analog circuits</td></tr>
<tr><td>AVSS</td><td>PI</td><td>Ground pins for analog circuits</td></tr>
<tr><td>VCC</td><td>PI</td><td>Power supply for digital circuits</td></tr>
<tr><td>GND</td><td>PI</td><td>Ground pins for digital circuits</td></tr>
<tr><td colspan="3">Others</td></tr>
<tr><td>OUT1 ~OUT1200</td><td>O</td><td>Output driver signals.</td></tr>
<tr><td>RPO1,RPO2</td><td>O</td><td>RPI1 (RPI2) → impedance changed → RPO1 (RPO2)</td></tr>
<tr><td>DUMMY0 ~ DUMMY35</td><td>D</td><td>Dummy pads. Not connected</td></tr>
</table>

I: Input, O: Output, D: Dummy, PI: Power input, I/O: Input / Output.

Pass line name:

PASS LINE NO.	PIN NAME	
1	PASS1	PASS1
2	PASS2	PASS2

Function Description

1. Power on/off sequence

This IC is a high-voltage LCD driver, so may be damaged by a large current flow when an incorrect power sequence is used. The recommended sequence should be : digital power (VCC&GND) ➔ logic signals➔analog power (AVDD&AVSS) ➔Gamma correction reference voltage(V1~V14). Reverse this sequence to shut down, or turn off all signals and power simultaneously.

2. RSDS Receiver and Demultiplexer

The device adapts the RSDS interface for EMI solution. The internal RSDS receiver block operates the comparison between the transmitted differential input pair data. The input data line from the timing controller to the RSDS receiver consist of 6-bit digital , 3 color, 1 port, 9 differential data pair (DxxP/DxxN) and 1 differential clock pair(CLKP/CLKN). The input common mode voltage range at the RSDS reveiver is 1.2V.The differential data and clock signals from the panel timing controller arrive at the NT39411 as multi- plexed , even and odd data fields. The nominal peak to peak swing of the data is 200mV across a termination resistor.

3. Relationship between the order of input data and output channels

(1) SHL="1" , shift right, a start pulse from DIO1

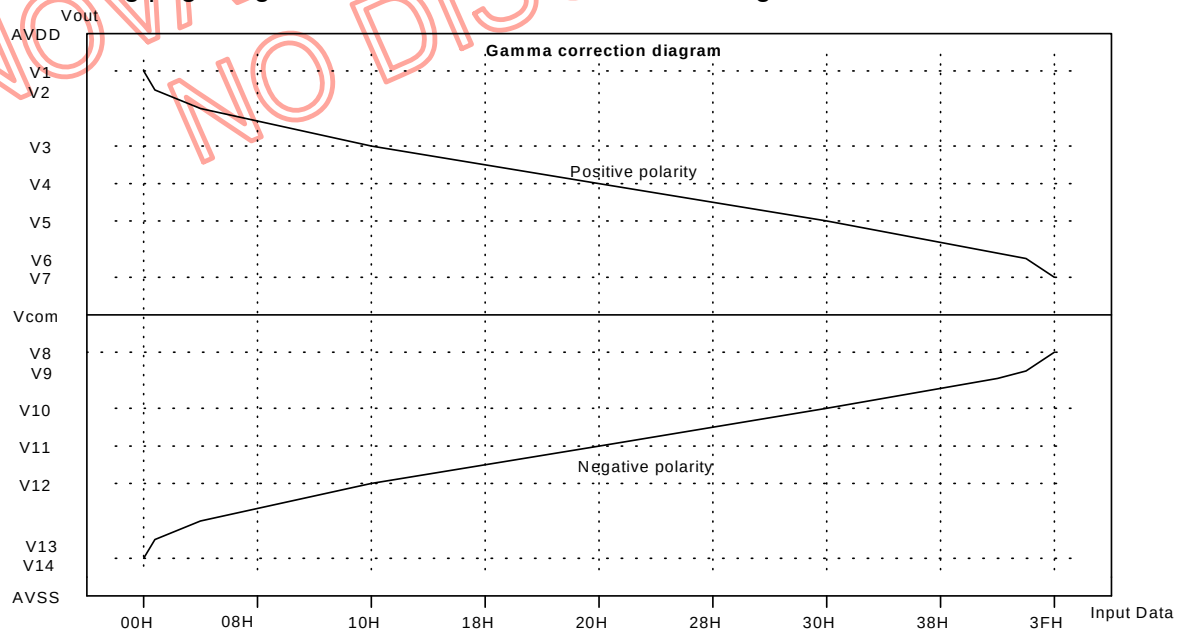
Output	OUT1	OUT2	OUT3	- - -	OUT1198	OUT1199	OUT1200
Order	First data			---→	Last data		
Data	D05~D00	D15~D10	D25~D20	- - -	D05~D00	D15~D10	D25~D20

(2) SHL="0", shift left, a start pulse from DIO2

Output	OUT1	OUT2	OUT3	- - -	OUT1198	OUT1199	OUT1200
Order	Last data			←---	First data		
Data	D05~D00	D15~D10	D25~D20	- - -	D05~D00	D15~D10	D25~D20

4. Relationship between input data and output voltage

The figure below shows the relationship between the input data and the output voltage with the polarity. The range of V1~ V7 is for positive polarity, and V8 ~ V14 for negative polarity. Please refer to the following page to get the relative resister value and voltage calculation method.



Remark: AVDD-0.1 ≥ V1 ≥ V2≥ V3 ≥ V4 ≥ V5 ≥ V6 ≥ V7; V8 ≥ V9 ≥ V10 ≥ V11 ≥ V12 ≥ V13 ≥ V14 ≥ AVSS+0.1V

5. Gamma correction resistor ratio

	Name	Resistor	Name	Resistor	
V1, V14 →	R0	6.4	R32	0.8	← V4, V11
V2, V13 →	R1	6	R33	0.8	
	R2	5.6	R34	0.8	
	R3	5.2	R35	0.8	
	R4	4.8	R36	0.8	
	R5	4.4	R37	0.8	
	R6	4.4	R38	0.8	
	R7	4	R39	0.8	
	R8	4	R40	0.8	
	R9	3.2	R41	0.8	
	R10	3.2	R42	0.8	
	R11	2.8	R43	0.8	
	R12	2.8	R44	0.8	
	R13	2.8	R45	0.8	
	R14	2.4	R46	0.8	
	R15	2.4	R47	0.8	
V3, V12 →	R16	2.4	R48	0.8	← V5, V10
	R17	2	R49	0.8	
	R18	2	R50	0.8	
	R19	2	R51	0.8	
	R20	1.6	R52	0.8	
	R21	1.6	R53	1.2	
	R22	1.6	R54	1.2	
	R23	1.2	R55	1.2	
	R24	1.2	R56	1.6	
	R25	1.2	R57	1.6	
	R26	1.2	R58	2	
	R27	0.8	R59	2	
	R28	0.8	R60	2.4	
	R29	0.8	R61	4	← V6, V9
	R30	0.8	R62	6.4	← V7, V8
V4, V11 →	R31	0.8			

6. Output Voltage VS Input Data

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	V2	V13
02H	V3 + (V2 – V3)X 52 / 58	V13+ (V12 – V13)X 6 / 58
03H	V3 + (V2 – V3)X 46.4 / 58	V13+ (V12 – V13)X 11.6 / 58
04H	V3 + (V2 – V3)X 41.2 / 58	V13 + (V12 – V13)X 16.8 / 58
05H	V3 + (V2 – V3)X 36.4 / 58	V13 + (V12 – V13)X 21.6 / 58
06H	V3 + (V2 – V3)X 32 / 58	V13 + (V12 – V13)X 26 / 58
07H	V3 + (V2 – V3)X 27.6 / 58	V13 + (V12 – V13)X 30.4 / 58
08H	V3 + (V2 – V3)X 23.6 / 58	V13 + (V12 – V13)X 34.4 / 58
09H	V3 + (V2 – V3)X 19.6 / 58	V13 + (V12 – V13)X 38.4 / 58
0AH	V3 + (V2 – V3)X 16.4 / 58	V13 + (V12 – V13)X 41.6 / 58
0BH	V3 + (V2 – V3)X 13.2 / 58	V13 + (V12 – V13)X 44.8 / 58
0CH	V3 + (V2 – V3)X 10.4 / 58	V13 + (V12 – V13)X 47.6 / 58
0DH	V3 + (V2 – V3)X 7.6 / 58	V13 + (V12 – V13)X 50.4 / 58
0EH	V3 + (V2 – V3)X 4.8 / 58	V13 + (V12 – V13)X 53.2 / 58
0FH	V3 + (V2 – V3)X 2.4 / 58	V13 + (V12 – V13)X 55.6 / 58
10H	V3	V12
11H	V4 + (V3 – V4) X 19.6 / 22	V12 + (V11 – V12)X 2.4 / 22
12H	V4 + (V3 – V4) X 17.6 / 22	V12 + (V11 – V12)X 4.4 / 22
13H	V4 + (V3 – V4) X 15.6 / 22	V12 + (V11 – V12)X 6.4 / 22
14H	V4 + (V3 – V4) X 13.6 / 22	V12 + (V11 – V12)X 8.4 / 22
15H	V4 + (V3 – V4) X 12 / 22	V12 + (V11 – V12)X 10 / 22
16H	V4 + (V3 – V4) X 10.4 / 22	V12 + (V11 – V12)X 11.6 / 22
17H	V4 + (V3 – V4) X 8.8 / 22	V12 + (V11 – V12)X 13.2 / 22
18H	V4 + (V3 – V4) X 7.6 / 22	V12 + (V11 – V12)X 14.4 / 22
19H	V4 + (V3 – V4) X 6.4 / 22	V12 + (V11 – V12)X 15.6 / 22
1AH	V4 + (V3 – V4) X 5.2 / 22	V12 + (V11 – V12)X 16.8 / 22
1BH	V4 + (V3 – V4) X 4 / 22	V12 + (V11 – V12)X 18 / 22
1CH	V4 + (V3 – V4) X 3.2 / 22	V12 + (V11 – V12)X 18.8 / 22
1DH	V4 + (V3 – V4) X 2.4 / 22	V12 + (V11 – V12)X 19.6 / 22
1EH	V4 + (V3 – V4) X 1.6 / 22	V12 + (V11 – V12)X 20.4 / 22
1FH	V4 + (V3 – V4) X 0.8 /22	V12 + (V11 – V12)X 21.2 / 22

(continued)

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	V5 + (V4 – V5) X 12 / 12.8	V11 + (V10 – V11) X 0.8 / 12.8
22H	V5 + (V4 – V5) X 11.2 / 12.8	V11 + (V10 – V11) X 1.6 / 12.8
23H	V5 + (V4 – V5) X 10.4 / 12.8	V11 + (V10 – V11) X 2.4 / 12.8
24H	V5 + (V4 – V5) X 9.6 / 12.8	V11 + (V10 – V11) X 3.2 / 12.8
25H	V5 + (V4 – V5) X 8.8 / 12.8	V11 + (V10 – V11) X 4 / 12.8
26H	V5 + (V4 – V5) X 8 / 12.8	V11 + (V10 – V11) X 4.8 / 12.8
27H	V5 + (V4 – V5) X 7.2 / 12.8	V11 + (V10 – V11) X 5.6 / 12.8
28H	V5 + (V4 – V5) X 6.4 / 12.8	V11 + (V10 – V11) X 6.4 / 12.8
29H	V5 + (V4 – V5) X 5.6 / 12.8	V11 + (V10 – V11) X 7.2 / 12.8
2AH	V5 + (V4 – V5) X 4.8 / 12.8	V11 + (V10 – V11) X 8 / 12.8
2BH	V5 + (V4 – V5) X 4 / 12.8	V11 + (V10 – V11) X 8.8 / 12.8
2CH	V5 + (V4 – V5) X 3.2 / 12.8	V11 + (V10 – V11) X 9.6 / 12.8
2DH	V5 + (V4 – V5) X 2.4 / 12.8	V11 + (V10 – V11) X 10.4 / 12.8
2EH	V5 + (V4 – V5) X 1.6 / 12.8	V11 + (V10 – V11) X 11.2 / 12.8
2FH	V5 + (V4 – V5) X 0.8 / 12.8	V11 + (V10 – V11) X 12 / 12.8
30H	V5	V10
31H	V6 + (V5 – V6) X 20.4 / 21.2	V10 + (V9 – V10) X 0.8 / 21.2
32H	V6 + (V5 – V6) X 19.6 / 21.2	V10 + (V9 – V10) X 1.6 / 21.2
33H	V6 + (V5 – V6) X 18.8 / 21.2	V10 + (V9 – V10) X 2.4 / 21.2
34H	V6 + (V5 – V6) X 18 / 21.2	V10 + (V9 – V10) X 3.2 / 21.2
35H	V6 + (V5 – V6) X 17.2 / 21.2	V10 + (V9 – V10) X 4 / 21.2
36H	V6 + (V5 – V6) X 16 / 21.2	V10 + (V9 – V10) X 5.2 / 21.2
37H	V6 + (V5 – V6) X 14.8 / 21.2	V10 + (V9 – V10) X 6.4 / 21.2
38H	V6 + (V5 – V6) X 13.6 / 21.2	V10 + (V9 – V10) X 7.6 / 21.2
39H	V6 + (V5 – V6) X 12 / 21.2	V10 + (V9 – V10) X 9.2 / 21.2
3AH	V6 + (V5 – V6) X 10.4 / 21.2	V10 + (V9 – V10) X 10.8 / 21.2
3BH	V6 + (V5 – V6) X 8.4 / 21.2	V10 + (V9 – V10) X 12.8 / 21.2
3CH	V6 + (V5 – V6) X 6.4 / 21.2	V10 + (V9 – V10) X 14.8 / 21.2
3DH	V6 + (V5 – V6) X 4 / 21.2	V10 + (V9 – V10) X 17.2 / 21.2
3EH	V6	V9
3FH	V7	V8

Absolute Maximum Ratings

	MIN.	MAX.	UNIT
Logic supply voltage, VCC Digital input voltage Output voltage, DIO1 & DIO2	**-0.5**	**5**	**V**
Analog supply voltage, AVDD Gamma voltage , V1~V14 OUT1 ~ OUT1200	**-0.5**	**15**	**V**

TEMPREATURE

	MIN.	MAX.	UNIT
Operating temperature	**-30**	**85**	**°C**
Storage temperature	**-55**	**125**	**°C**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

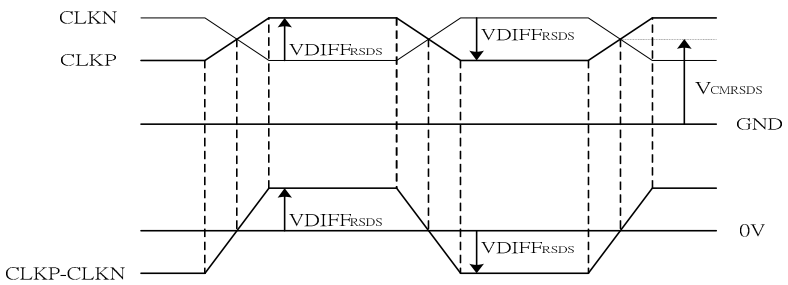
(For the digital circuit: Test Condition VCC =3.3V , AVDD= 10V, AVSS=GND=0V, TA=25℃)

TTL mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	2.7	3.3	3.6	V	Digital power : default 3.3V
Low Level Input Voltage	Vil	0	-	0.3xVCC	V	For the digital circuit
High Level Input Voltage	Vih	0.7xVCC	-	VCC	V	For the digital circuit
High Level Output Voltage	Voh	VCC-0.4	-	-	V	DIO1, DIO2, Ioh=1mA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	DIO1, DIO2, Iol=-1mA
Input Leakage Current	Ii	-	-	±1	uA	For the digital circuit
Digital Stand-by Current	Ist	-	10	50	uA	DCLK is stopped, Inputs are default, Outputs are High-Z.
Digital Operating Current	Icc	-	3	4	mA	Fclk=50 MHz, FLD=50KHz, VCC=3.3V
Pull low/ high resistor	Ri	150K	300K	-	ohm	Digital signal

RSDS mode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC	2.7	3.3	3.6	V	Digital power : default 3.3V
RSDS Low Level Input Voltage	Vilrsds	-	-200	-100	mV	D2[2:0]P,D2[2:0]N,CLKP,CLKN
RSDS High Level Input Voltage	Vihrsds	100	200	-	mV	D2[2:0]P,D2[2:0]N,CLKP,CLKN
RSDS reference Voltage	Vcmrsds	GND+0.1	1.2	VCC-1.2	V	D2[2:0]P,D2[2:0]N,CLKP,CLKN
Low Level Input Voltage	Vil	0	-	0.3xVCC	V	Other input pins
High Level Input Voltage	Vih	0.7xVCC	-	VCC	V	Other input pins
High Level Output Voltage	Voh	VCC-0.4	-	-	V	DIO1,DIO2,Ioh=1mA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	DIO1,DIO2,Iol=-1mA
RSDS input Leakage Current	Iirsds	-	-	10	uA	D2[2:0]P,D2[2:0]N,CLKP,CLKN
Input Leakage Current	Ii	-	-	±1	uA	Other input pins
RSDS Digital Stand-by Current	Istrsds	-	-	600	uA	DCLK is stopped, Inputs are default, Outputs are High-Z.
RSDS Digital Operating Current	Iccrsds	-	-	7.5	mA	Fclk=50 MHz, FLD=50KHz, VCC=3.3V
Pull low/ high resistor	Ri	150K	300K	-	ohm	Digital signal



NOTES: 1. VCMRSDS=(VCLKP+VCLKN)/2 OR VCMRSDS=(VDxxP+VDxxN)/2
2. VDIFFRSDS=VCLKP-VCLKN or VDIFFRSDS=VDxxP-VDxxN

(For the analog circuit: Test Condition VCC =3.3V , AVDD= 10V, AVSS=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	AVDD	6.5	10	13.5	V	For the analog circuit power
Input level of V1 ~ V7	Vref	0.4AVDD	-	AVDD-0.1	V	Gamma correction voltage
Input level of V8 ~ V14	Vref	0.1	-	0.6AVDD	V	Gamma correction voltage
Output Voltage deviation	Vod	-	±20	-	mV	
Voltage Output Offset between Chips	Voc	-	±20	-	mV	
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	OUT1 ~ OUT1200
Sinking Current of Outputs	IOLy	80	-	-	uA	OUT1 ~ OUT1200; Vo=0.1V v.s 1.0V , AVDD=13.5V
	IOLr	400				RPO1,RPO2; Vo=0.1V v.s 1.0V , AVDD=13.5V
Driving Current of Outputs	IOHy	80	-	-	uA	OUT1 ~ OUT1200; Vo=13.4V v.s 12.5V , AVDD=13.5V
	IOHr	400				RPO1,RPO2; Vo=13.4V v.s 12.5V , AVDD=13.5V
Impedance of Gamma Correction	Rg	0.8*Rn	1.1*Rn	1.4*Rn	ohm	Rn: Internal gamma resistor
Analog Stand-by Current	Isc	-	8 .5	10	mA	No load, AVDD=10V, and all operating is stopped
Analog Operating Current	Ioc	-	10	12	mA	No load, Fclk=50MHz, FLD=50KHz AVDD=10V,V1=8V, V14=0.4V

AC Electrical Characteristics

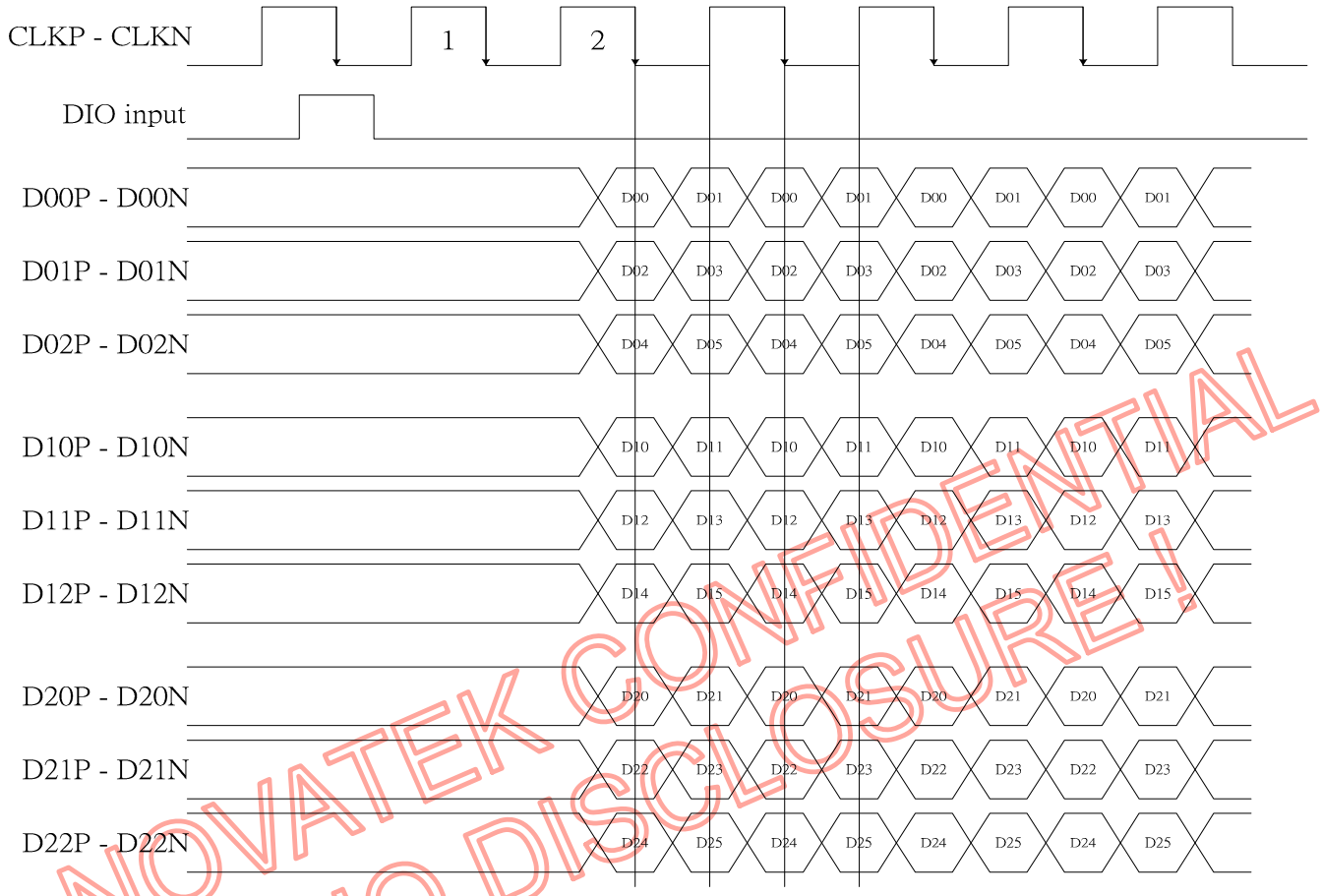
(VCC =3.3V, AVDD=10V, AVSS=GND=0V, TA= 25℃)

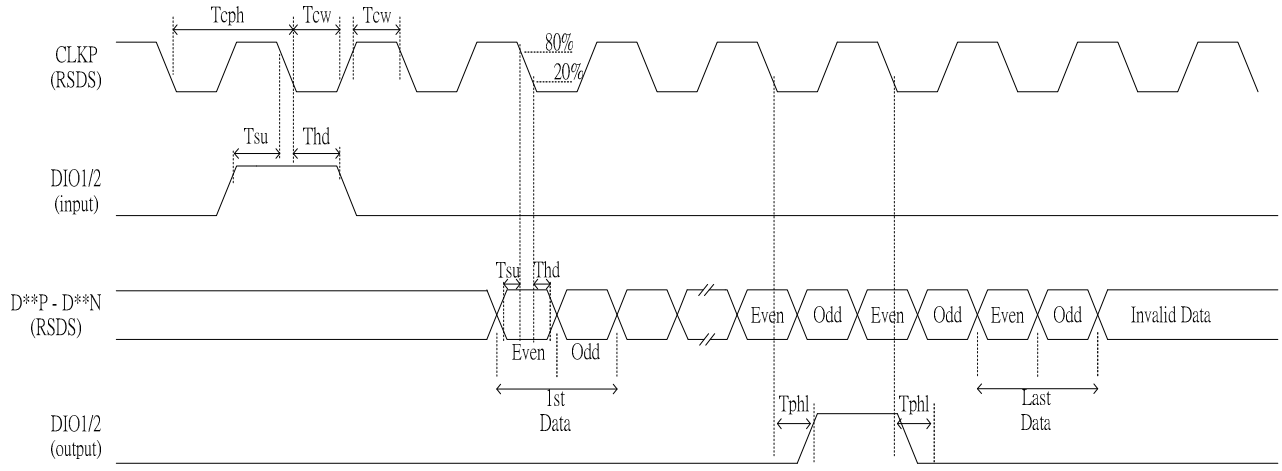
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	50	55	MHz	EDGSL = '0'
	Fclk	-	25	27.5	MHz	EDGSL = '1'
CLK pulse width	Tcw	40%	-	60%	Tcph	
Data set-up time	Tsu	4	-	-	ns	D00 ~ D25, REV and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	D00 ~ D25, REV and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	6	10	15	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to DIO1/2	Tlds	5	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	-	9	us	10% or 90% target voltage. CL=60pF, R=2K ohm
Repair output delay stable time	Tst1	-	-	20	us	CL=190pF, R=5.5K ohm

Timing Diagram

1. Clock and data input timing diagram 1

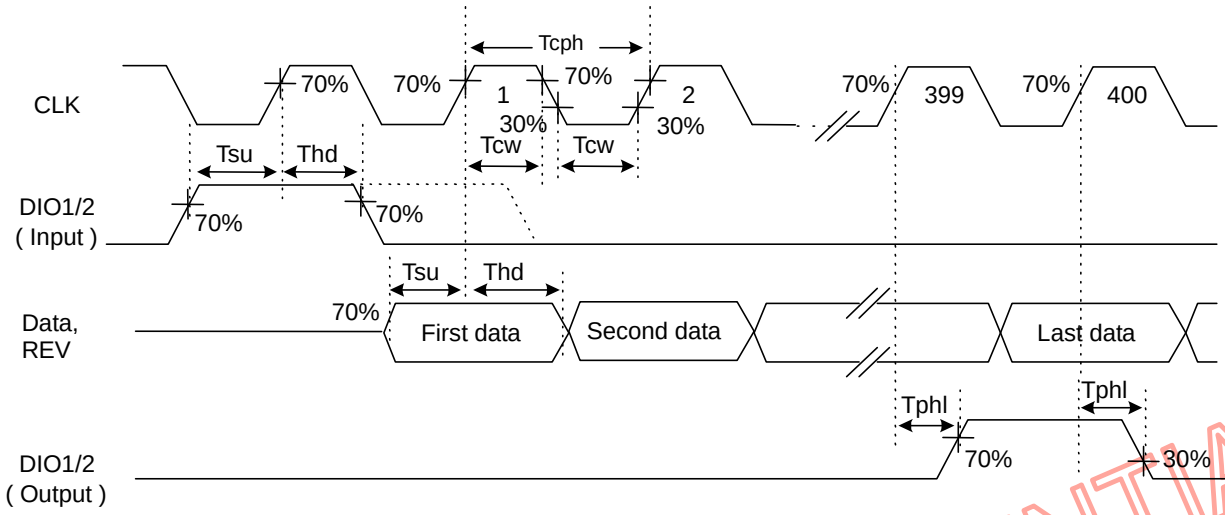
1.1 RSDS mode



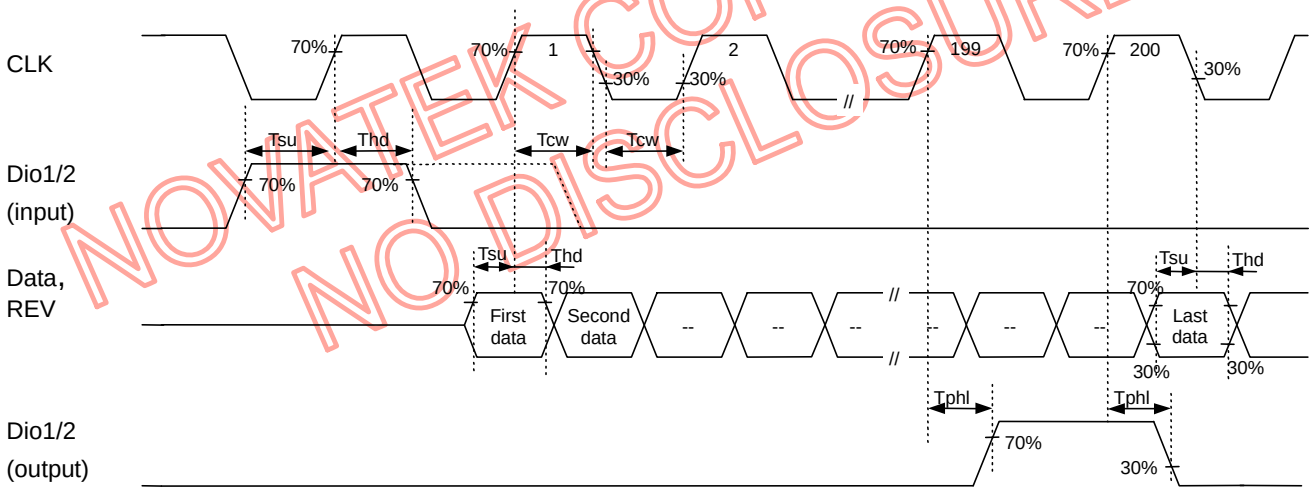


1.2 TTL mode

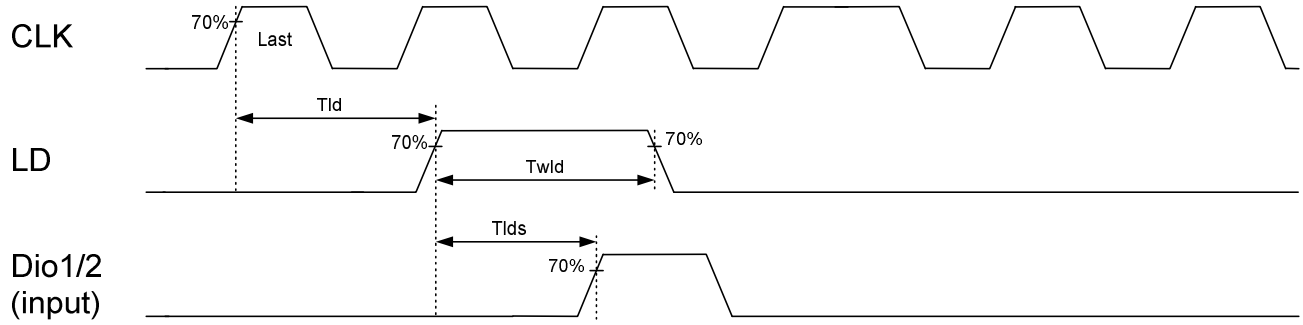
<< EDGSL= ”0”, Default >>

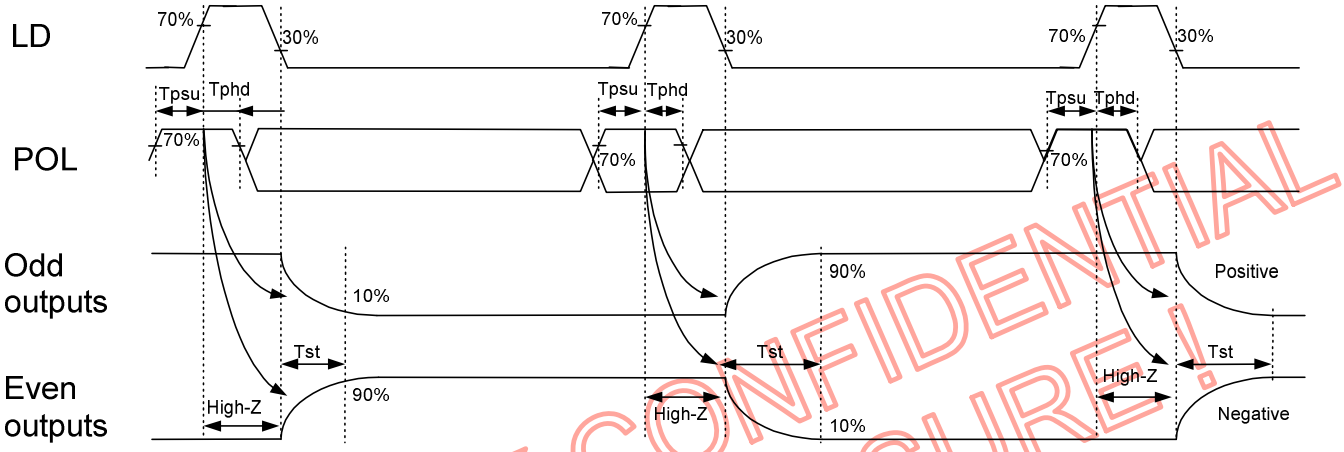


<< EDGSL= ”1”>>

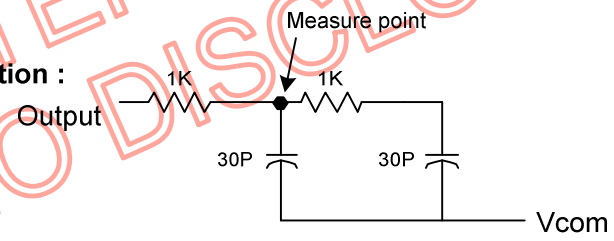


2. Clock and data input timing diagram 2

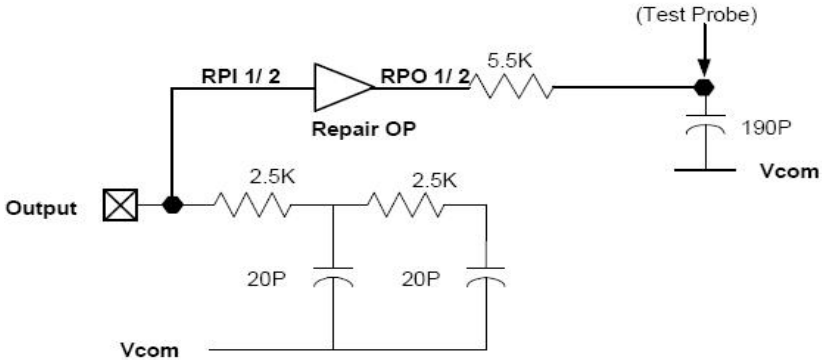




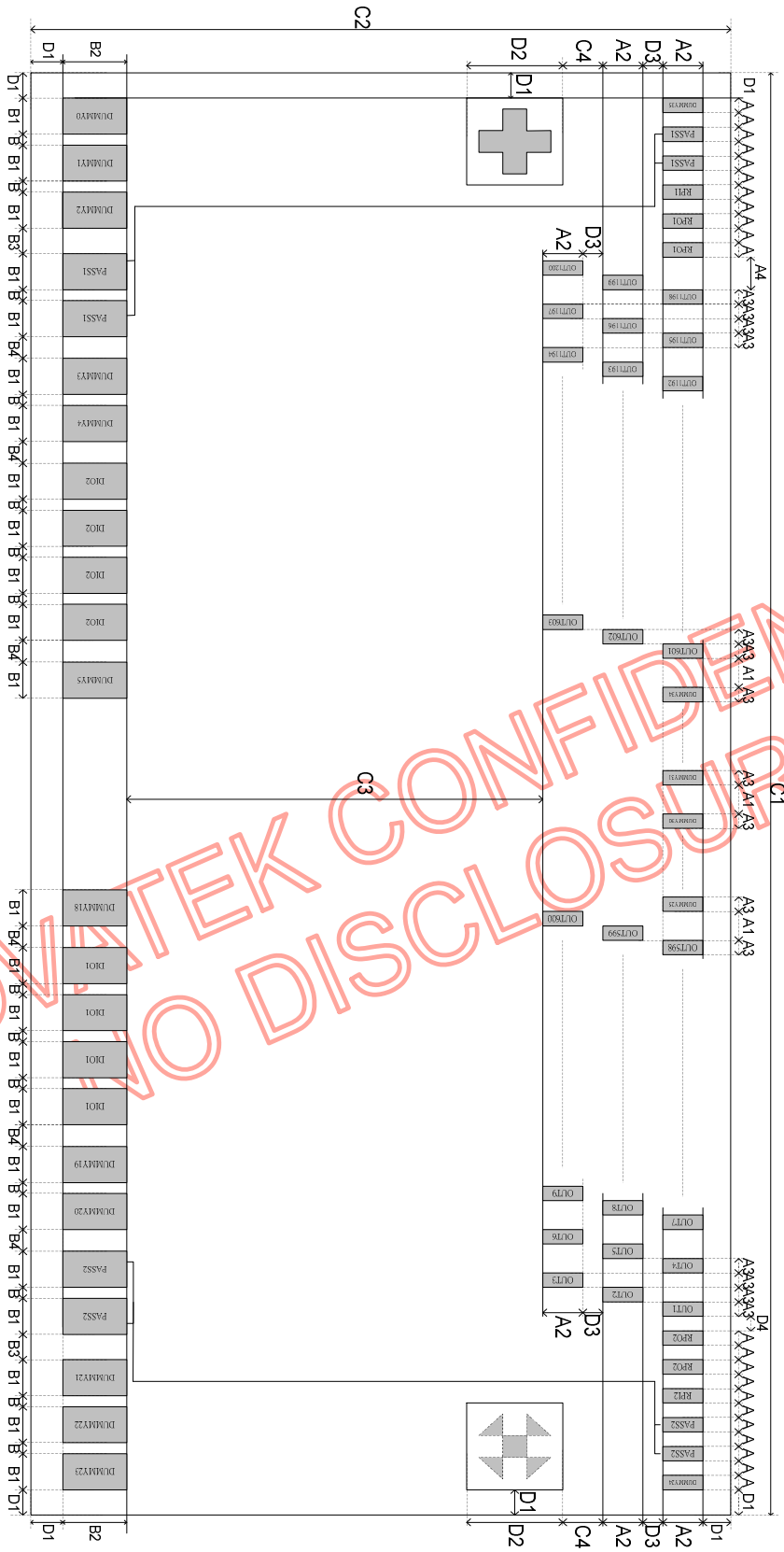
Output load condition :



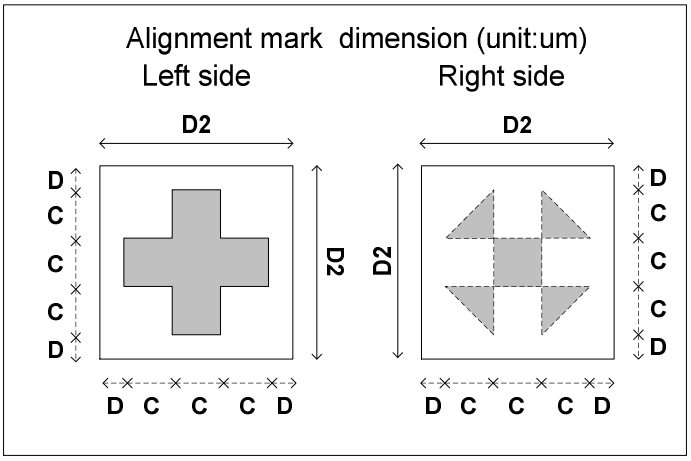
Repair OP output load condition :



Pad Outline Dimension (Bump Side)



1. Alignment Mark

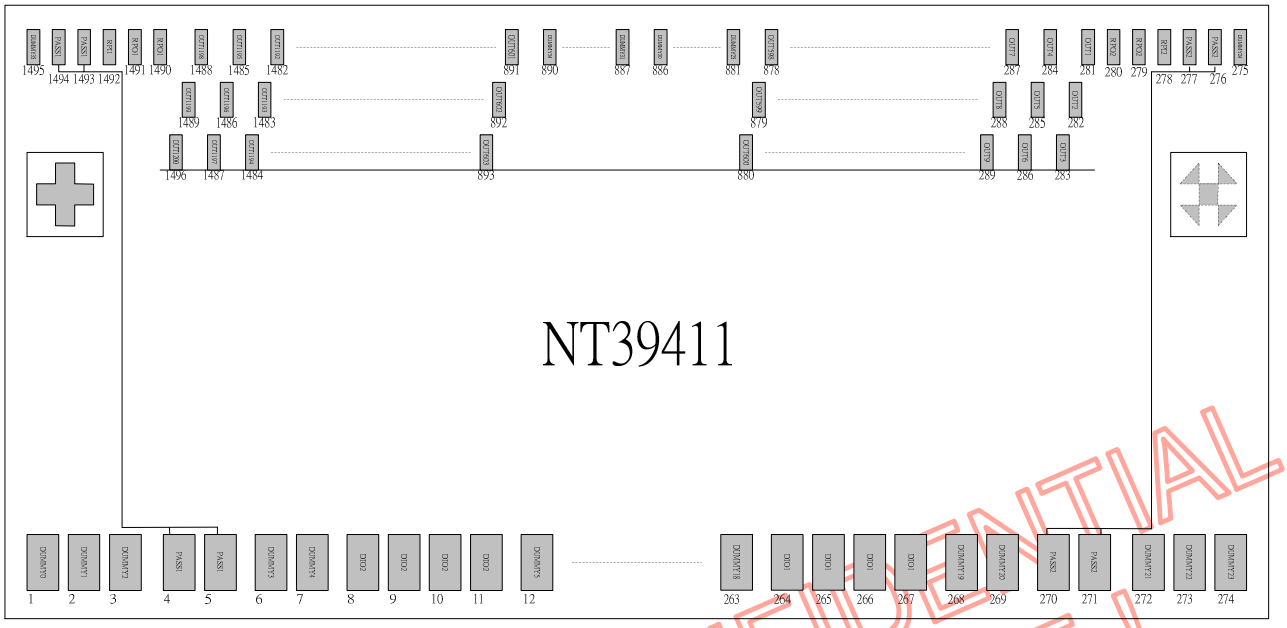


2. Pad Information

Symbol	Dimension in um	Symbol	Dimension in um
A	22	C	30
A1	38	C1	24056
A2	100	C2	1100
A3	19	C3	490
A4	59	C4	80
B	16	D	15
B1	66	D1	80
B2	90	D2	120
B3	38	D3	30
B4	36	D4	21

Chip size: 24056(X) x 1100(Y) um^2 (scribe line included)

Appendix A: Pad Coordinate



Pad	TextName	CX	CY
1	DUMMY[0]	-11915	-425
2	DUMMY[1]	-11833	-425
3	DUMMY[2]	-11751	-425
4	PASS1	-11647	-425
5	PASS1	-11565	-425
6	DUMMY[3]	-11463	-425
7	DUMMY[4]	-11381	-425
8	DIO2	-11279	-425
9	DIO2	-11197	-425
10	DIO2	-11115	-425
11	DIO2	-11033	-425
12	DUMMY[5]	-10931	-425
13	AVDD	-10829	-425
14	AVDD	-10747	-425
15	AVDD	-10665	-425
16	AVDD	-10583	-425
17	AVDD	-10501	-425
18	AVDD	-10419	-425
19	AVDD	-10337	-425
20	AVDD	-10255	-425
21	AVDD	-10173	-425
22	AVDD	-10091	-425
23	ENREOP	-9989	-425
24	ENREOP	-9907	-425
25	ENREOP	-9825	-425
26	CHNSL	-9723	-425
27	CHNSL	-9641	-425
28	CHNSL	-9559	-425
29	GND	-9457	-425
30	GND	-9375	-425
31	GND	-9293	-425
32	GND	-9211	-425
33	GND	-9129	-425
34	GND	-9047	-425
35	GND	-8965	-425
36	GND	-8883	-425
37	CHNDS	-8781	-425
38	CHNDS	-8699	-425
39	CHNDS	-8617	-425
40	VCC	-8515	-425
41	VCC	-8433	-425
42	VCC	-8351	-425
43	VCC	-8269	-425
44	VCC	-8187	-425
45	VCC	-8105	-425
46	VCC	-8023	-425
47	VCC	-7941	-425
48	DUMMY[6]	-7839	-425
49	POL	-7737	-425
50	POL	-7655	-425
51	POL	-7573	-425
52	POL	-7491	-425
53	DUMMY[7]	-7389	-425
54	REV	-7287	-425
55	REV	-7205	-425
56	REV	-7123	-425
57	REV	-7041	-425
58	DUMMY[8]	-6939	-425
59	LD	-6837	-425
60	LD	-6755	-425
61	LD	-6673	-425
62	LD	-6591	-425
63	DUMMY[9]	-6489	-425
64	D25	-6387	-425
65	D25	-6305	-425
66	D25	-6223	-425
67	D25	-6141	-425
68	D24	-6039	-425
69	D24	-5957	-425
70	D24	-5875	-425
71	D24	-5793	-425
72	D23	-5691	-425
73	D23	-5609	-425
74	D23	-5527	-425
75	D23	-5445	-425
76	D22	-5343	-425
77	D22	-5261	-425

78	D22	-5179	-425
79	D22	-5097	-425
80	D21	-4995	-425
81	D21	-4913	-425
82	D21	-4831	-425
83	D21	-4749	-425
84	D20	-4647	-425
85	D20	-4565	-425
86	D20	-4483	-425
87	D20	-4401	-425
88	DUMMY[10]	-4299	-425
89	AVSS	-4197	-425
90	AVSS	-4115	-425
91	AVSS	-4033	-425
92	AVSS	-3951	-425
93	AVSS	-3869	-425
94	AVSS	-3787	-425
95	AVSS	-3705	-425
96	AVSS	-3623	-425
97	AVSS	-3541	-425
98	AVSS	-3459	-425
99	DUMMY[11]	-3357	-425
100	V14	-3255	-425
101	V14	-3173	-425
102	V14	-3091	-425
103	V14	-3009	-425
104	V13	-2907	-425
105	V13	-2825	-425
106	V13	-2743	-425
107	V13	-2661	-425
108	V12	-2559	-425
109	V12	-2477	-425
110	V12	-2395	-425
111	V12	-2313	-425
112	V11	-2211	-425
113	V11	-2129	-425
114	V11	-2047	-425
115	V11	-1965	-425
116	V10	-1863	-425
117	V10	-1781	-425
118	V10	-1699	-425
119	V10	-1617	-425
120	V9	-1515	-425
121	V9	-1433	-425
122	V9	-1351	-425
123	V9	-1269	-425
124	V8	-1167	-425
125	V8	-1085	-425
126	V8	-1003	-425
127	V8	-921	-425
128	V7	-819	-425
129	V7	-737	-425
130	V7	-655	-425
131	V7	-573	-425
132	V6	-471	-425
133	V6	-389	-425
134	V6	-307	-425
135	V6	-225	-425
136	V5	-123	-425
137	V5	-41	-425
138	V5	41	-425
139	V5	123	-425
140	V4	225	-425
141	V4	307	-425
142	V4	389	-425
143	V4	471	-425
144	V3	573	-425
145	V3	655	-425
146	V3	737	-425
147	V3	819	-425
148	V2	921	-425
149	V2	1003	-425
150	V2	1085	-425
151	V2	1167	-425
152	V1	1269	-425
153	V1	1351	-425
154	V1	1433	-425
155	V1	1515	-425
156	DUMMY[12]	1617	-425
157	AVDD	1719	-425
158	AVDD	1801	-425
159	AVDD	1883	-425
160	AVDD	1965	-425
161	AVDD	2047	-425
162	AVDD	2129	-425
163	AVDD	2211	-425
164	AVDD	2293	-425
165	AVDD	2375	-425
166	AVDD	2457	-425
167	DUMMY[13]	2559	-425
168	D15	2661	-425
169	D15	2743	-425
170	D15	2825	-425
171	D15	2907	-425
172	D14	3009	-425
173	D14	3091	-425
174	D14	3173	-425
175	D14	3255	-425
176	D13	3357	-425
177	D13	3439	-425
178	D13	3521	-425
179	D13	3603	-425
180	D12	3705	-425
181	D12	3787	-425
182	D12	3869	-425
183	D12	3951	-425
184	D11	4053	-425
185	D11	4135	-425
186	D11	4217	-425
187	D11	4299	-425
188	D10	4401	-425
189	D10	4483	-425
190	D10	4565	-425
191	D10	4647	-425
192	D05	4749	-425
193	D05	4831	-425
194	D05	4913	-425
195	D05	4995	-425
196	D04	5097	-425
197	D04	5179	-425
198	D04	5261	-425
199	D04	5343	-425
200	D03	5445	-425
201	D03	5527	-425
202	D03	5609	-425
203	D03	5691	-425
204	D02	5793	-425
205	D02	5875	-425
206	D02	5957	-425
207	D02	6039	-425
208	D01	6141	-425
209	D01	6223	-425
210	D01	6305	-425
211	D01	6387	-425
212	D00	6489	-425
213	D00	6571	-425
214	D00	6653	-425
215	D00	6735	-425
216	DUMMY[14]	6837	-425
217	CLKN	6939	-425
218	CLKN	7021	-425
219	CLKN	7103	-425
220	CLKN	7185	-425
221	CLK	7287	-425
222	CLK	7369	-425
223	CLK	7451	-425
224	CLK	7533	-425
225	SHL	7635	-425
226	SHL	7717	-425
227	SHL	7799	-425
228	EDGSL	7901	-425
229	EDGSL	7983	-425
230	EDGSL	8065	-425
231	TTLRSDS	8167	-425
232	TTLRSDS	8249	-425
233	TTLRSDS	8331	-425
234	DUMMY[15]	8433	-425
235	VCC	8535	-425
236	VCC	8617	-425
237	VCC	8699	-425
238	VCC	8781	-425
239	VCC	8863	-425
240	VCC	8945	-425
241	VCC	9027	-425
242	VCC	9109	-425
243	DUMMY[16]	9211	-425
244	GND	9313	-425
245	GND	9395	-425
246	GND	9477	-425
247	GND	9559	-425
248	GND	9641	-425
249	GND	9723	-425
250	GND	9805	-425
251	GND	9887	-425
252	DUMMY[17]	9989	-425
253	AVSS	10091	-425
254	AVSS	10173	-425
255	AVSS	10255	-425
256	AVSS	10337	-425
257	AVSS	10419	-425
258	AVSS	10501	-425
259	AVSS	10583	-425
260	AVSS	10665	-425
261	AVSS	10747	-425
262	AVSS	10829	-425
263	DUMMY[18]	10931	-425
264	DIO1	11033	-425
265	DIO1	11115	-425
266	DIO1	11197	-425
267	DIO1	11279	-425
268	DUMMY[19]	11381	-425
269	DUMMY[20]	11463	-425
270	PASS2	11565	-425
271	PASS2	11647	-425
272	DUMMY[21]	11751	-425
273	DUMMY[22]	11833	-425
274	DUMMY[23]	11915	-425
275	DUMMY[24]	11937	420

276	PASS2	11893	420
277	PASS2	11849	420
278	RPI2	11805	420
279	RPO2	11761	420
280	RPO2	11717	420
281	OUT[1]	11675.5	420
282	OUT[2]	11656.5	290
283	OUT[3]	11637.5	160
284	OUT[4]	11618.5	420
285	OUT[5]	11599.5	290
286	OUT[6]	11580.5	160
287	OUT[7]	11561.5	420
288	OUT[8]	11542.5	290
289	OUT[9]	11523.5	160
290	OUT[10]	11504.5	420
291	OUT[11]	11485.5	290
292	OUT[12]	11466.5	160
293	OUT[13]	11447.5	420
294	OUT[14]	11428.5	290
295	OUT[15]	11409.5	160
296	OUT[16]	11390.5	420
297	OUT[17]	11371.5	290
298	OUT[18]	11352.5	160
299	OUT[19]	11333.5	420
300	OUT[20]	11314.5	290
301	OUT[21]	11295.5	160
302	OUT[22]	11276.5	420
303	OUT[23]	11257.5	290
304	OUT[24]	11238.5	160
305	OUT[25]	11219.5	420
306	OUT[26]	11200.5	290
307	OUT[27]	11181.5	160
308	OUT[28]	11162.5	420
309	OUT[29]	11143.5	290
310	OUT[30]	11124.5	160
311	OUT[31]	11105.5	420
312	OUT[32]	11086.5	290
313	OUT[33]	11067.5	160
314	OUT[34]	11048.5	420
315	OUT[35]	11029.5	290
316	OUT[36]	11010.5	160
317	OUT[37]	10991.5	420
318	OUT[38]	10972.5	290
319	OUT[39]	10953.5	160
320	OUT[40]	10934.5	420
321	OUT[41]	10915.5	290
322	OUT[42]	10896.5	160
323	OUT[43]	10877.5	420
324	OUT[44]	10858.5	290
325	OUT[45]	10839.5	160
326	OUT[46]	10820.5	420
327	OUT[47]	10801.5	290
328	OUT[48]	10782.5	160
329	OUT[49]	10763.5	420
330	OUT[50]	10744.5	290
331	OUT[51]	10725.5	160
332	OUT[52]	10706.5	420
333	OUT[53]	10687.5	290
334	OUT[54]	10668.5	160
335	OUT[55]	10649.5	420
336	OUT[56]	10630.5	290
337	OUT[57]	10611.5	160
338	OUT[58]	10592.5	420
339	OUT[59]	10573.5	290
340	OUT[60]	10554.5	160
341	OUT[61]	10535.5	420
342	OUT[62]	10516.5	290
343	OUT[63]	10497.5	160
344	OUT[64]	10478.5	420
345	OUT[65]	10459.5	290
346	OUT[66]	10440.5	160
347	OUT[67]	10421.5	420
348	OUT[68]	10402.5	290
349	OUT[69]	10383.5	160
350	OUT[70]	10364.5	420
351	OUT[71]	10345.5	290
352	OUT[72]	10326.5	160
353	OUT[73]	10307.5	420
354	OUT[74]	10288.5	290
355	OUT[75]	10269.5	160
356	OUT[76]	10250.5	420
357	OUT[77]	10231.5	290
358	OUT[78]	10212.5	160
359	OUT[79]	10193.5	420
360	OUT[80]	10174.5	290
361	OUT[81]	10155.5	160
362	OUT[82]	10136.5	420
363	OUT[83]	10117.5	290
364	OUT[84]	10098.5	160
365	OUT[85]	10079.5	420
366	OUT[86]	10060.5	290
367	OUT[87]	10041.5	160
368	OUT[88]	10022.5	420
369	OUT[89]	10003.5	290
370	OUT[90]	9984.5	160
371	OUT[91]	9965.5	420
372	OUT[92]	9946.5	290
373	OUT[93]	9927.5	160
374	OUT[94]	9908.5	420
375	OUT[95]	9889.5	290
376	OUT[96]	9870.5	160
377	OUT[97]	9851.5	420
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380	OUT[100]	9794.5	420
381	OUT[101]	9775.5	290
382	OUT[102]	9756.5	160
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386	OUT[106]	9680.5	420
387	OUT[107]	9661.5	290
388	OUT[108]	9642.5	160
389	OUT[109]	9623.5	420
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391	OUT[111]	9585.5	160
392	OUT[112]	9566.5	420
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394	OUT[114]	9528.5	160
395	OUT[115]	9509.5	420
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400	OUT[120]	9414.5	160
401	OUT[121]	9395.5	420
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403	OUT[123]	9357.5	160
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406	OUT[126]	9300.5	160
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408	OUT[128]	9262.5	290
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412	OUT[132]	9186.5	160
413	OUT[133]	9167.5	420
414	OUT[134]	9148.5	290
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417	OUT[137]	9091.5	290
418	OUT[138]	9072.5	160
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421	OUT[141]	9015.5	160
422	OUT[142]	8996.5	420
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460	OUT[180]	8274.5	160
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469	OUT[189]	8103.5	160
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671	OUT[391]	4265.5	420

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677	OUT[397]	4151.5	420
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730	OUT[450]	3144.5	160
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736	OUT[456]	3030.5	160
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741	OUT[461]	2935.5	290
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745	OUT[465]	2859.5	160
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749	OUT[469]	2783.5	420
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754	OUT[474]	2688.5	160
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774	OUT[494]	2308.5	290
775	OUT[495]	2289.5	160
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782	OUT[502]	2156.5	420
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789	OUT[509]	2023.5	290
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791	OUT[511]	1985.5	420
792	OUT[512]	1966.5	290
793	OUT[513]	1947.5	160
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823	OUT[543]	1377.5	160
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859	OUT[579]	693.5	160
860	OUT[580]	674.5	420
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869	OUT[589]	503.5	420

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875	OUT[595]	389.5	420
876	OUT[596]	370.5	290
877	OUT[597]	351.5	160
878	OUT[598]	332.5	420
879	OUT[599]	313.5	290
880	OUT[600]	294.5	160
881	DUMMY[25]	275.5	420
882	DUMMY[26]	218.5	420
883	DUMMY[27]	161.5	420
884	DUMMY[28]	104.5	420
885	DUMMY[29]	47.5	420
886	DUMMY[30]	-9.5	420
887	DUMMY[31]	-66.5	420
888	DUMMY[32]	-123.5	420
889	DUMMY[33]	-180.5	420
890	DUMMY[34]	-237.5	420
891	OUT[601]	-294.5	420
892	OUT[602]	-313.5	290
893	OUT[603]	-332.5	160
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895	OUT[605]	-370.5	290
896	OUT[606]	-389.5	160
897	OUT[607]	-408.5	420
898	OUT[608]	-427.5	290
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900	OUT[610]	-465.5	420
901	OUT[611]	-484.5	290
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903	OUT[613]	-522.5	420
904	OUT[614]	-541.5	290
905	OUT[615]	-560.5	160
906	OUT[616]	-579.5	420
907	OUT[617]	-598.5	290
908	OUT[618]	-617.5	160
909	OUT[619]	-636.5	420
910	OUT[620]	-655.5	290
911	OUT[621]	-674.5	160
912	OUT[622]	-693.5	420
913	OUT[623]	-712.5	290
914	OUT[624]	-731.5	160
915	OUT[625]	-750.5	420
916	OUT[626]	-769.5	290
917	OUT[627]	-788.5	160
918	OUT[628]	-807.5	420
919	OUT[629]	-826.5	290
920	OUT[630]	-845.5	160
921	OUT[631]	-864.5	420
922	OUT[632]	-883.5	290
923	OUT[633]	-902.5	160
924	OUT[634]	-921.5	420
925	OUT[635]	-940.5	290
926	OUT[636]	-959.5	160
927	OUT[637]	-978.5	420
928	OUT[638]	-997.5	290
929	OUT[639]	-1016.5	160
930	OUT[640]	-1035.5	420
931	OUT[641]	-1054.5	290
932	OUT[642]	-1073.5	160
933	OUT[643]	-1092.5	420
934	OUT[644]	-1111.5	290
935	OUT[645]	-1130.5	160
936	OUT[646]	-1149.5	420
937	OUT[647]	-1168.5	290
938	OUT[648]	-1187.5	160
939	OUT[649]	-1206.5	420
940	OUT[650]	-1225.5	290
941	OUT[651]	-1244.5	160
942	OUT[652]	-1263.5	420
943	OUT[653]	-1282.5	290
944	OUT[654]	-1301.5	160
945	OUT[655]	-1320.5	420
946	OUT[656]	-1339.5	290
947	OUT[657]	-1358.5	160
948	OUT[658]	-1377.5	420
949	OUT[659]	-1396.5	290
950	OUT[660]	-1415.5	160
951	OUT[661]	-1434.5	420
952	OUT[662]	-1453.5	290
953	OUT[663]	-1472.5	160
954	OUT[664]	-1491.5	420
955	OUT[665]	-1510.5	290
956	OUT[666]	-1529.5	160
957	OUT[667]	-1548.5	420
958	OUT[668]	-1567.5	290
959	OUT[669]	-1586.5	160
960	OUT[670]	-1605.5	420
961	OUT[671]	-1624.5	290
962	OUT[672]	-1643.5	160
963	OUT[673]	-1662.5	420
964	OUT[674]	-1681.5	290
965	OUT[675]	-1700.5	160
966	OUT[676]	-1719.5	420
967	OUT[677]	-1738.5	290
968	OUT[678]	-1757.5	160
969	OUT[679]	-1776.5	420
970	OUT[680]	-1795.5	290
971	OUT[681]	-1814.5	160
972	OUT[682]	-1833.5	420
973	OUT[683]	-1852.5	290
974	OUT[684]	-1871.5	160
975	OUT[685]	-1890.5	420
976	OUT[686]	-1909.5	290
977	OUT[687]	-1928.5	160
978	OUT[688]	-1947.5	420
979	OUT[689]	-1966.5	290
980	OUT[690]	-1985.5	160
981	OUT[691]	-2004.5	420
982	OUT[692]	-2023.5	290
983	OUT[693]	-2042.5	160
984	OUT[694]	-2061.5	420
985	OUT[695]	-2080.5	290
986	OUT[696]	-2099.5	160
987	OUT[697]	-2118.5	420
988	OUT[698]	-2137.5	290
989	OUT[699]	-2156.5	160
990	OUT[700]	-2175.5	420
991	OUT[701]	-2194.5	290
992	OUT[702]	-2213.5	160
993	OUT[703]	-2232.5	420
994	OUT[704]	-2251.5	290
995	OUT[705]	-2270.5	160
996	OUT[706]	-2289.5	420
997	OUT[707]	-2308.5	290
998	OUT[708]	-2327.5	160
999	OUT[709]	-2346.5	420
1000	OUT[710]	-2365.5	290
1001	OUT[711]	-2384.5	160
1002	OUT[712]	-2403.5	420
1003	OUT[713]	-2422.5	290
1004	OUT[714]	-2441.5	160
1005	OUT[715]	-2460.5	420
1006	OUT[716]	-2479.5	290
1007	OUT[717]	-2498.5	160
1008	OUT[718]	-2517.5	420
1009	OUT[719]	-2536.5	290
1010	OUT[720]	-2555.5	160
1011	OUT[721]	-2574.5	420
1012	OUT[722]	-2593.5	290
1013	OUT[723]	-2612.5	160
1014	OUT[724]	-2631.5	420
1015	OUT[725]	-2650.5	290
1016	OUT[726]	-2669.5	160
1017	OUT[727]	-2688.5	420
1018	OUT[728]	-2707.5	290
1019	OUT[729]	-2726.5	160
1020	OUT[730]	-2745.5	420
1021	OUT[731]	-2764.5	290
1022	OUT[732]	-2783.5	160
1023	OUT[733]	-2802.5	420
1024	OUT[734]	-2821.5	290
1025	OUT[735]	-2840.5	160
1026	OUT[736]	-2859.5	420
1027	OUT[737]	-2878.5	290
1028	OUT[738]	-2897.5	160
1029	OUT[739]	-2916.5	420
1030	OUT[740]	-2935.5	290
1031	OUT[741]	-2954.5	160
1032	OUT[742]	-2973.5	420
1033	OUT[743]	-2992.5	290
1034	OUT[744]	-3011.5	160
1035	OUT[745]	-3030.5	420
1036	OUT[746]	-3049.5	290
1037	OUT[747]	-3068.5	160
1038	OUT[748]	-3087.5	420
1039	OUT[749]	-3106.5	290
1040	OUT[750]	-3125.5	160
1041	OUT[751]	-3144.5	420
1042	OUT[752]	-3163.5	290
1043	OUT[753]	-3182.5	160
1044	OUT[754]	-3201.5	420
1045	OUT[755]	-3220.5	290
1046	OUT[756]	-3239.5	160
1047	OUT[757]	-3258.5	420
1048	OUT[758]	-3277.5	290
1049	OUT[759]	-3296.5	160
1050	OUT[760]	-3315.5	420
1051	OUT[761]	-3334.5	290
1052	OUT[762]	-3353.5	160
1053	OUT[763]	-3372.5	420
1054	OUT[764]	-3391.5	290
1055	OUT[765]	-3410.5	160
1056	OUT[766]	-3429.5	420
1057	OUT[767]	-3448.5	290
1058	OUT[768]	-3467.5	160
1059	OUT[769]	-3486.5	420
1060	OUT[770]	-3505.5	290
1061	OUT[771]	-3524.5	160
1062	OUT[772]	-3543.5	420
1063	OUT[773]	-3562.5	290
1064	OUT[774]	-3581.5	160
1065	OUT[775]	-3600.5	420
1066	OUT[776]	-3619.5	290
1067	OUT[777]	-3638.5	160

1068	OUT[778]	-3657.5	420
1069	OUT[779]	-3676.5	290
1070	OUT[780]	-3695.5	160
1071	OUT[781]	-3714.5	420
1072	OUT[782]	-3733.5	290
1073	OUT[783]	-3752.5	160
1074	OUT[784]	-3771.5	420
1075	OUT[785]	-3790.5	290
1076	OUT[786]	-3809.5	160
1077	OUT[787]	-3828.5	420
1078	OUT[788]	-3847.5	290
1079	OUT[789]	-3866.5	160
1080	OUT[790]	-3885.5	420
1081	OUT[791]	-3904.5	290
1082	OUT[792]	-3923.5	160
1083	OUT[793]	-3942.5	420
1084	OUT[794]	-3961.5	290
1085	OUT[795]	-3980.5	160
1086	OUT[796]	-3999.5	420
1087	OUT[797]	-4018.5	290
1088	OUT[798]	-4037.5	160
1089	OUT[799]	-4056.5	420
1090	OUT[800]	-4075.5	290
1091	OUT[801]	-4094.5	160
1092	OUT[802]	-4113.5	420
1093	OUT[803]	-4132.5	290
1094	OUT[804]	-4151.5	160
1095	OUT[805]	-4170.5	420
1096	OUT[806]	-4189.5	290
1097	OUT[807]	-4208.5	160
1098	OUT[808]	-4227.5	420
1099	OUT[809]	-4246.5	290
1100	OUT[810]	-4265.5	160
1101	OUT[811]	-4284.5	420
1102	OUT[812]	-4303.5	290
1103	OUT[813]	-4322.5	160
1104	OUT[814]	-4341.5	420
1105	OUT[815]	-4360.5	290
1106	OUT[816]	-4379.5	160
1107	OUT[817]	-4398.5	420
1108	OUT[818]	-4417.5	290
1109	OUT[819]	-4436.5	160
1110	OUT[820]	-4455.5	420
1111	OUT[821]	-4474.5	290
1112	OUT[822]	-4493.5	160
1113	OUT[823]	-4512.5	420
1114	OUT[824]	-4531.5	290
1115	OUT[825]	-4550.5	160
1116	OUT[826]	-4569.5	420
1117	OUT[827]	-4588.5	290
1118	OUT[828]	-4607.5	160
1119	OUT[829]	-4626.5	420
1120	OUT[830]	-4645.5	290
1121	OUT[831]	-4664.5	160
1122	OUT[832]	-4683.5	420
1123	OUT[833]	-4702.5	290
1124	OUT[834]	-4721.5	160
1125	OUT[835]	-4740.5	420
1126	OUT[836]	-4759.5	290
1127	OUT[837]	-4778.5	160
1128	OUT[838]	-4797.5	420
1129	OUT[839]	-4816.5	290
1130	OUT[840]	-4835.5	160
1131	OUT[841]	-4854.5	420
1132	OUT[842]	-4873.5	290
1133	OUT[843]	-4892.5	160
1134	OUT[844]	-4911.5	420
1135	OUT[845]	-4930.5	290
1136	OUT[846]	-4949.5	160
1137	OUT[847]	-4968.5	420
1138	OUT[848]	-4987.5	290
1139	OUT[849]	-5006.5	160
1140	OUT[850]	-5025.5	420
1141	OUT[851]	-5044.5	290
1142	OUT[852]	-5063.5	160
1143	OUT[853]	-5082.5	420
1144	OUT[854]	-5101.5	290
1145	OUT[855]	-5120.5	160
1146	OUT[856]	-5139.5	420
1147	OUT[857]	-5158.5	290
1148	OUT[858]	-5177.5	160
1149	OUT[859]	-5196.5	420
1150	OUT[860]	-5215.5	290
1151	OUT[861]	-5234.5	160
1152	OUT[862]	-5253.5	420
1153	OUT[863]	-5272.5	290
1154	OUT[864]	-5291.5	160
1155	OUT[865]	-5310.5	420
1156	OUT[866]	-5329.5	290
1157	OUT[867]	-5348.5	160
1158	OUT[868]	-5367.5	420
1159	OUT[869]	-5386.5	290
1160	OUT[870]	-5405.5	160
1161	OUT[871]	-5424.5	420
1162	OUT[872]	-5443.5	290
1163	OUT[873]	-5462.5	160
1164	OUT[874]	-5481.5	420
1165	OUT[875]	-5500.5	290
1166	OUT[876]	-5519.5	160
1167	OUT[877]	-5538.5	420
1168	OUT[878]	-5557.5	290
1169	OUT[879]	-5576.5	160
1170	OUT[880]	-5595.5	420
1171	OUT[881]	-5614.5	290
1172	OUT[882]	-5633.5	160
1173	OUT[883]	-5652.5	420
1174	OUT[884]	-5671.5	290
1175	OUT[885]	-5690.5	160
1176	OUT[886]	-5709.5	420
1177	OUT[887]	-5728.5	290
1178	OUT[888]	-5747.5	160
1179	OUT[889]	-5766.5	420
1180	OUT[890]	-5785.5	290
1181	OUT[891]	-5804.5	160
1182	OUT[892]	-5823.5	420
1183	OUT[893]	-5842.5	290
1184	OUT[894]	-5861.5	160
1185	OUT[895]	-5880.5	420
1186	OUT[896]	-5899.5	290
1187	OUT[897]	-5918.5	160
1188	OUT[898]	-5937.5	420
1189	OUT[899]	-5956.5	290
1190	OUT[900]	-5975.5	160
1191	OUT[901]	-5994.5	420
1192	OUT[902]	-6013.5	290
1193	OUT[903]	-6032.5	160
1194	OUT[904]	-6051.5	420
1195	OUT[905]	-6070.5	290
1196	OUT[906]	-6089.5	160
1197	OUT[907]	-6108.5	420
1198	OUT[908]	-6127.5	290
1199	OUT[909]	-6146.5	160
1200	OUT[910]	-6165.5	420
1201	OUT[911]	-6184.5	290
1202	OUT[912]	-6203.5	160
1203	OUT[913]	-6222.5	420
1204	OUT[914]	-6241.5	290
1205	OUT[915]	-6260.5	160
1206	OUT[916]	-6279.5	420
1207	OUT[917]	-6298.5	290
1208	OUT[918]	-6317.5	160
1209	OUT[919]	-6336.5	420
1210	OUT[920]	-6355.5	290
1211	OUT[921]	-6374.5	160
1212	OUT[922]	-6393.5	420
1213	OUT[923]	-6412.5	290
1214	OUT[924]	-6431.5	160
1215	OUT[925]	-6450.5	420
1216	OUT[926]	-6469.5	290
1217	OUT[927]	-6488.5	160
1218	OUT[928]	-6507.5	420
1219	OUT[929]	-6526.5	290
1220	OUT[930]	-6545.5	160
1221	OUT[931]	-6564.5	420
1222	OUT[932]	-6583.5	290
1223	OUT[933]	-6602.5	160
1224	OUT[934]	-6621.5	420
1225	OUT[935]	-6640.5	290
1226	OUT[936]	-6659.5	160
1227	OUT[937]	-6678.5	420
1228	OUT[938]	-6697.5	290
1229	OUT[939]	-6716.5	160
1230	OUT[940]	-6735.5	420
1231	OUT[941]	-6754.5	290
1232	OUT[942]	-6773.5	160
1233	OUT[943]	-6792.5	420
1234	OUT[944]	-6811.5	290
1235	OUT[945]	-6830.5	160
1236	OUT[946]	-6849.5	420
1237	OUT[947]	-6868.5	290
1238	OUT[948]	-6887.5	160
1239	OUT[949]	-6906.5	420
1240	OUT[950]	-6925.5	290
1241	OUT[951]	-6944.5	160
1242	OUT[952]	-6963.5	420
1243	OUT[953]	-6982.5	290
1244	OUT[954]	-7001.5	160
1245	OUT[955]	-7020.5	420
1246	OUT[956]	-7039.5	290
1247	OUT[957]	-7058.5	160
1248	OUT[958]	-7077.5	420
1249	OUT[959]	-7096.5	290
1250	OUT[960]	-7115.5	160
1251	OUT[961]	-7134.5	420
1252	OUT[962]	-7153.5	290
1253	OUT[963]	-7172.5	160
1254	OUT[964]	-7191.5	420
1255	OUT[965]	-7210.5	290
1256	OUT[966]	-7229.5	160
1257	OUT[967]	-7248.5	420
1258	OUT[968]	-7267.5	290
1259	OUT[969]	-7286.5	160
1260	OUT[970]	-7305.5	420
1261	OUT[971]	-7324.5	290
1262	OUT[972]	-7343.5	160
1263	OUT[973]	-7362.5	420
1264	OUT[974]	-7381.5	290
1265	OUT[975]	-7400.5	160

1266	OUT[976]	-7419.5	420
1267	OUT[977]	-7438.5	290
1268	OUT[978]	-7457.5	160
1269	OUT[979]	-7476.5	420
1270	OUT[980]	-7495.5	290
1271	OUT[981]	-7514.5	160
1272	OUT[982]	-7533.5	420
1273	OUT[983]	-7552.5	290
1274	OUT[984]	-7571.5	160
1275	OUT[985]	-7590.5	420
1276	OUT[986]	-7609.5	290
1277	OUT[987]	-7628.5	160
1278	OUT[988]	-7647.5	420
1279	OUT[989]	-7666.5	290
1280	OUT[990]	-7685.5	160
1281	OUT[991]	-7704.5	420
1282	OUT[992]	-7723.5	290
1283	OUT[993]	-7742.5	160
1284	OUT[994]	-7761.5	420
1285	OUT[995]	-7780.5	290
1286	OUT[996]	-7799.5	160
1287	OUT[997]	-7818.5	420
1288	OUT[998]	-7837.5	290
1289	OUT[999]	-7856.5	160
1290	OUT[1000]	-7875.5	420
1291	OUT[1001]	-7894.5	290
1292	OUT[1002]	-7913.5	160
1293	OUT[1003]	-7932.5	420
1294	OUT[1004]	-7951.5	290
1295	OUT[1005]	-7970.5	160
1296	OUT[1006]	-7989.5	420
1297	OUT[1007]	-8008.5	290
1298	OUT[1008]	-8027.5	160
1299	OUT[1009]	-8046.5	420
1300	OUT[1010]	-8065.5	290
1301	OUT[1011]	-8084.5	160
1302	OUT[1012]	-8103.5	420
1303	OUT[1013]	-8122.5	290
1304	OUT[1014]	-8141.5	160
1305	OUT[1015]	-8160.5	420
1306	OUT[1016]	-8179.5	290
1307	OUT[1017]	-8198.5	160
1308	OUT[1018]	-8217.5	420
1309	OUT[1019]	-8236.5	290
1310	OUT[1020]	-8255.5	160
1311	OUT[1021]	-8274.5	420
1312	OUT[1022]	-8293.5	290
1313	OUT[1023]	-8312.5	160
1314	OUT[1024]	-8331.5	420
1315	OUT[1025]	-8350.5	290
1316	OUT[1026]	-8369.5	160
1317	OUT[1027]	-8388.5	420
1318	OUT[1028]	-8407.5	290
1319	OUT[1029]	-8426.5	160
1320	OUT[1030]	-8445.5	420
1321	OUT[1031]	-8464.5	290
1322	OUT[1032]	-8483.5	160
1323	OUT[1033]	-8502.5	420
1324	OUT[1034]	-8521.5	290
1325	OUT[1035]	-8540.5	160
1326	OUT[1036]	-8559.5	420
1327	OUT[1037]	-8578.5	290
1328	OUT[1038]	-8597.5	160
1329	OUT[1039]	-8616.5	420
1330	OUT[1040]	-8635.5	290
1331	OUT[1041]	-8654.5	160
1332	OUT[1042]	-8673.5	420
1333	OUT[1043]	-8692.5	290
1334	OUT[1044]	-8711.5	160
1335	OUT[1045]	-8730.5	420
1336	OUT[1046]	-8749.5	290
1337	OUT[1047]	-8768.5	160
1338	OUT[1048]	-8787.5	420
1339	OUT[1049]	-8806.5	290
1340	OUT[1050]	-8825.5	160
1341	OUT[1051]	-8844.5	420
1342	OUT[1052]	-8863.5	290
1343	OUT[1053]	-8882.5	160
1344	OUT[1054]	-8901.5	420
1345	OUT[1055]	-8920.5	290
1346	OUT[1056]	-8939.5	160
1347	OUT[1057]	-8958.5	420
1348	OUT[1058]	-8977.5	290
1349	OUT[1059]	-8996.5	160
1350	OUT[1060]	-9015.5	420
1351	OUT[1061]	-9034.5	290
1352	OUT[1062]	-9053.5	160
1353	OUT[1063]	-9072.5	420
1354	OUT[1064]	-9091.5	290
1355	OUT[1065]	-9110.5	160
1356	OUT[1066]	-9129.5	420
1357	OUT[1067]	-9148.5	290
1358	OUT[1068]	-9167.5	160
1359	OUT[1069]	-9186.5	420
1360	OUT[1070]	-9205.5	290
1361	OUT[1071]	-9224.5	160
1362	OUT[1072]	-9243.5	420
1363	OUT[1073]	-9262.5	290
1364	OUT[1074]	-9281.5	160
1365	OUT[1075]	-9300.5	420
1366	OUT[1076]	-9319.5	290
1367	OUT[1077]	-9338.5	160
1368	OUT[1078]	-9357.5	420
1369	OUT[1079]	-9376.5	290
1370	OUT[1080]	-9395.5	160
1371	OUT[1081]	-9414.5	420
1372	OUT[1082]	-9433.5	290
1373	OUT[1083]	-9452.5	160
1374	OUT[1084]	-9471.5	420
1375	OUT[1085]	-9490.5	290
1376	OUT[1086]	-9509.5	160
1377	OUT[1087]	-9528.5	420
1378	OUT[1088]	-9547.5	290
1379	OUT[1089]	-9566.5	160
1380	OUT[1090]	-9585.5	420
1381	OUT[1091]	-9604.5	290
1382	OUT[1092]	-9623.5	160
1383	OUT[1093]	-9642.5	420
1384	OUT[1094]	-9661.5	290
1385	OUT[1095]	-9680.5	160
1386	OUT[1096]	-9699.5	420
1387	OUT[1097]	-9718.5	290
1388	OUT[1098]	-9737.5	160
1389	OUT[1099]	-9756.5	420
1390	OUT[1100]	-9775.5	290
1391	OUT[1101]	-9794.5	160
1392	OUT[1102]	-9813.5	420
1393	OUT[1103]	-9832.5	290
1394	OUT[1104]	-9851.5	160
1395	OUT[1105]	-9870.5	420
1396	OUT[1106]	-9889.5	290
1397	OUT[1107]	-9908.5	160
1398	OUT[1108]	-9927.5	420
1399	OUT[1109]	-9946.5	290
1400	OUT[1110]	-9965.5	160
1401	OUT[1111]	-9984.5	420
1402	OUT[1112]	-10003.5	290
1403	OUT[1113]	-10022.5	160
1404	OUT[1114]	-10041.5	420
1405	OUT[1115]	-10060.5	290
1406	OUT[1116]	-10079.5	160
1407	OUT[1117]	-10098.5	420
1408	OUT[1118]	-10117.5	290
1409	OUT[1119]	-10136.5	160
1410	OUT[1120]	-10155.5	420
1411	OUT[1121]	-10174.5	290
1412	OUT[1122]	-10193.5	160
1413	OUT[1123]	-10212.5	420
1414	OUT[1124]	-10231.5	290
1415	OUT[1125]	-10250.5	160
1416	OUT[1126]	-10269.5	420
1417	OUT[1127]	-10288.5	290
1418	OUT[1128]	-10307.5	160
1419	OUT[1129]	-10326.5	420
1420	OUT[1130]	-10345.5	290
1421	OUT[1131]	-10364.5	160
1422	OUT[1132]	-10383.5	420
1423	OUT[1133]	-10402.5	290
1424	OUT[1134]	-10421.5	160
1425	OUT[1135]	-10440.5	420
1426	OUT[1136]	-10459.5	290
1427	OUT[1137]	-10478.5	160
1428	OUT[1138]	-10497.5	420
1429	OUT[1139]	-10516.5	290
1430	OUT[1140]	-10535.5	160
1431	OUT[1141]	-10554.5	420
1432	OUT[1142]	-10573.5	290
1433	OUT[1143]	-10592.5	160
1434	OUT[1144]	-10611.5	420
1435	OUT[1145]	-10630.5	290
1436	OUT[1146]	-10649.5	160
1437	OUT[1147]	-10668.5	420
1438	OUT[1148]	-10687.5	290
1439	OUT[1149]	-10706.5	160
1440	OUT[1150]	-10725.5	420
1441	OUT[1151]	-10744.5	290
1442	OUT[1152]	-10763.5	160
1443	OUT[1153]	-10782.5	420
1444	OUT[1154]	-10801.5	290
1445	OUT[1155]	-10820.5	160
1446	OUT[1156]	-10839.5	420
1447	OUT[1157]	-10858.5	290
1448	OUT[1158]	-10877.5	160
1449	OUT[1159]	-10896.5	420
1450	OUT[1160]	-10915.5	290
1451	OUT[1161]	-10934.5	160
1452	OUT[1162]	-10953.5	420
1453	OUT[1163]	-10972.5	290
1454	OUT[1164]	-10991.5	160
1455	OUT[1165]	-11010.5	420
1456	OUT[1166]	-11029.5	290
1457	OUT[1167]	-11048.5	160
1458	OUT[1168]	-11067.5	420
1459	OUT[1169]	-11086.5	290
1460	OUT[1170]	-11105.5	160
1461	OUT[1171]	-11124.5	420
1462	OUT[1172]	-11143.5	290
1463	OUT[1173]	-11162.5	160

1464	OUT[1174]	-11181.5	420
1465	OUT[1175]	-11200.5	290
1466	OUT[1176]	-11219.5	160
1467	OUT[1177]	-11238.5	420
1468	OUT[1178]	-11257.5	290
1469	OUT[1179]	-11276.5	160
1470	OUT[1180]	-11295.5	420
1471	OUT[1181]	-11314.5	290
1472	OUT[1182]	-11333.5	160
1473	OUT[1183]	-11352.5	420
1474	OUT[1184]	-11371.5	290

1475	OUT[1185]	-11390.5	160
1476	OUT[1186]	-11409.5	420
1477	OUT[1187]	-11428.5	290
1478	OUT[1188]	-11447.5	160
1479	OUT[1189]	-11466.5	420
1480	OUT[1190]	-11485.5	290
1481	OUT[1191]	-11504.5	160
1482	OUT[1192]	-11523.5	420
1483	OUT[1193]	-11542.5	290
1484	OUT[1194]	-11561.5	160
1485	OUT[1195]	-11580.5	420

1486	OUT[1196]	-11599.5	290
1487	OUT[1197]	-11618.5	160
1488	OUT[1198]	-11637.5	420
1489	OUT[1199]	-11656.5	290
1490	RPO1	-11717	420
1491	RPO1	-11761	420
1492	RPI1	-11805	420
1493	PASS1	-11849	420
1494	PASS1	-11893	420
1495	DUMMY[35]	-11937	420
1496	OUT[1200]	-11675.5	160