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NOVATEK

NOVATEK

NT7603

Single-Chip 16C X 2L Dot-Matrix LCD Controller / Driver

Features

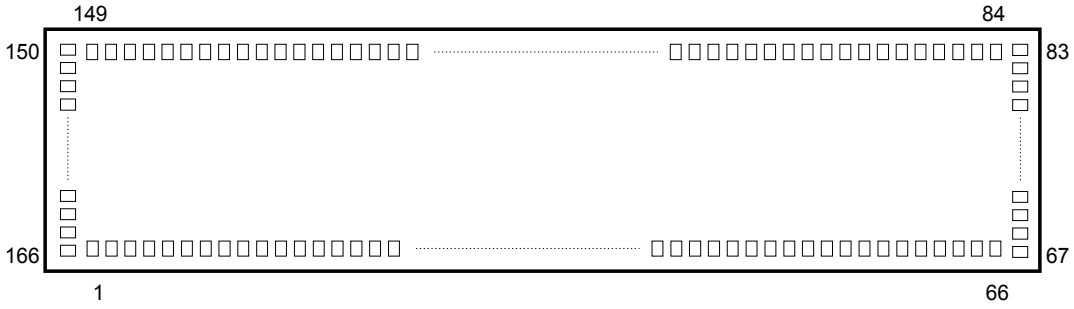
- Internal LCD drivers
  16 common signal drivers
  80 segment signal drivers
- Maximum display dimensions
  16 characters X 2 lines or
  32 characters X 1 line
- Interfaces with 4-bit or 8-bit MPU
- Versatile display functions provided on chip:
  Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Character Blinking, Cursor Shift, and Display Shift
- Three duty factors, selected by PROGRAM:
  1/8, 1/11, and 1/16
- Displays Data RAM (DD RAM): 80 X 8 bits
  (Displays up to 80 characters)
- Character Generator RAM (CG RAM):
  64 X 8 bits for general data,
  8 5 X 8 programmable dot patterns, or
  4 5 X 10 programmable dot patterns
- Low voltage reset
- ITO option for A-type and B-type LCD waveform
- Character Generator ROM (CG ROM):
  2 kinds of CG ROM sizes:
  192 characters:
  160 5 X 8 dot patterns
  32 5 X 10 dot patterns
  240 characters:
  192 5 X 8 dot patterns
  48 5 X 10 dot patterns
  Custom CG ROM is also available
- Built-in power-on reset function
- Logic power supply: 2.8V ~ 5.5V
- LCD driver power supply: V1 ~ V5
  (V_{DD} + 0.3 - V_{DD} - 7.0), divided by Built-in LCD power division resister.
- Two oscillator operations
  (Freq. = 500KHz - 540KHz):
  - Built-in RC oscillation
  - External clock
- CMOS Process
- Available in COG FORM

General Description

The NT7603 is a dot matrix LCD controller and driver LSI that can operate with either a 4-bit or an 8-bit microprocessor (MPU). The NT7603 receives control character codes from the MPU, stores them in an internal RAM (up to 80 characters) before transforming each character code into a 5 X 7, 5 X 8, or 5 X 10 dot matrix character pattern and then displaying the codes on the LCD panel. The built-in Character Generator ROM consists of 256 different character patterns.

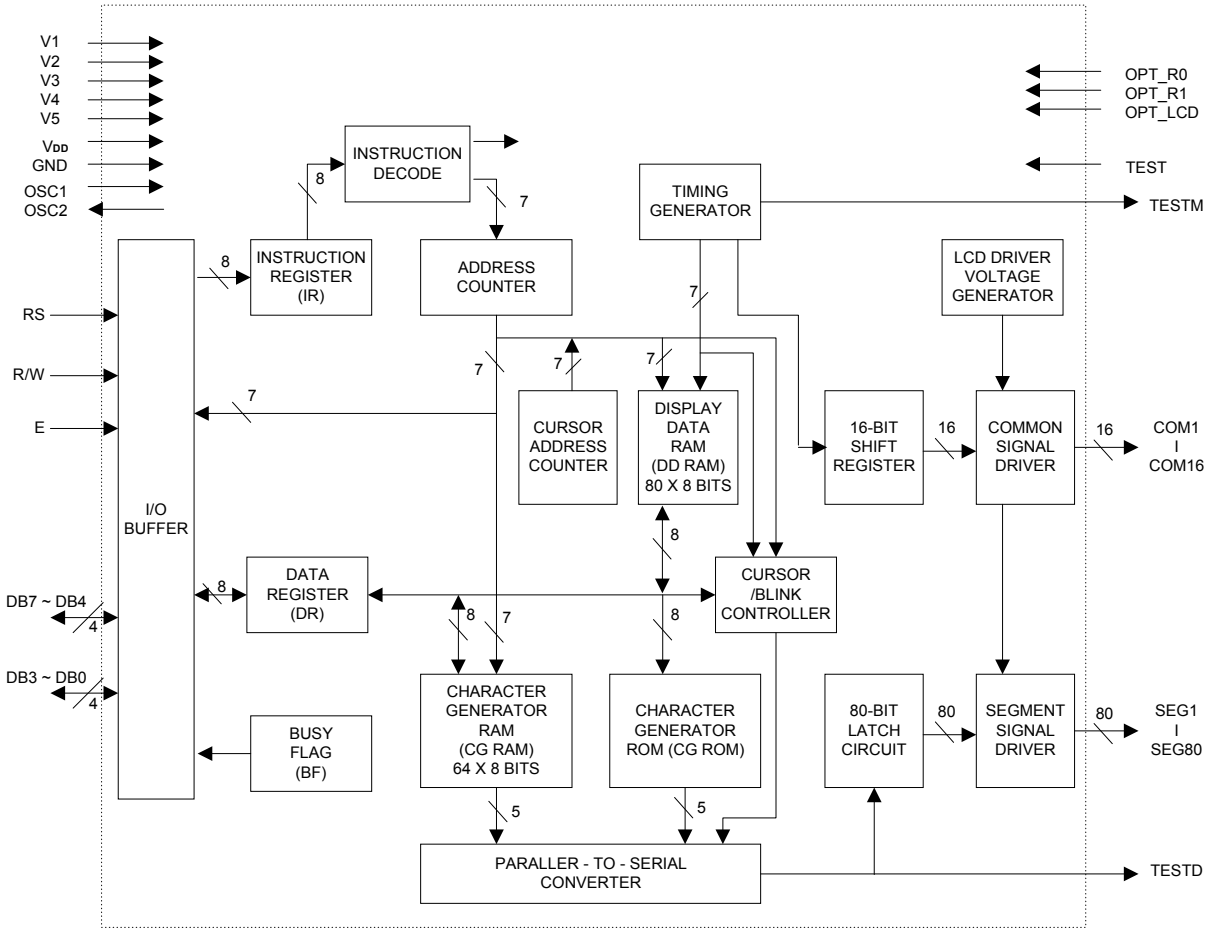
The NT7603 also contains Character Generator RAM where the user can store 8 different character patterns at run time. These memory features make the character display flexible. NT7603 also provides many display instructions to achieve versatile LCD display functions. The NT7603 is fabricated on a single LSI chip using the CMOS process, resulting in very low power requirements.

Pad Configuration



Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	5156	1349	μm
Pad pitch	1 - 166	70		

Block Diagram



Pad Description (Total 166 pads for COG type)

Pad No.	Designation	I/O	External Connection	Description
1 - 15	GND	P	Power supply	GND: 0V
16	OSC1	I		For external clock operation, clock inputs to OSC1
17	OSC2	O		Clock output
18	V1	P	Power supply	Power supply for LCD driver. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq GND$
19	V2	P	Power supply	Power supply for LCD driver
20	V3	P	Power supply	Power supply for LCD driver
21	V4	P	Power supply	Power supply for LCD driver
22 - 25	V5	P	Power supply	Power supply for LCD driver
26, 28	OPT_R0, OPT_R1	I	ITO Option	The built-in bias resister select: OPT_R1, OPT_R0: No ITO = 1. ITO on = 0 1, 1: 2.2KΩ; 1, 0: 4KΩ; 0, 1: 6.8KΩ; 0, 0:No built-in bias resistor
29 - 43	V_{DD}	P	Power supply	V_{DD}: +5V
44, 45	RS	I	MPU	Register select signal 0: Instruction register (write), Busy flag, address counter (read) 1: Data register (write, read)
46, 47	R/W	I	MPU	Read/Write control signal 0: Write 1: Read
48, 49	E	I	MPU	Read/Write start signal
50, 51	DB0	I/O	MPU	Lower 4 tri-state bi-directional data bus for transmitting data between MPU and NT7603. Not used during 4-bit operation.
52, 53	DB1			
54, 55	DB2			
56, 57	DB3			
58, 59	DB4	I/O	MPU	Higher 4 tri-state bi-directional data bus for transmitting data between MPU and NT7603. DB7 is also used as a busy flag.
60, 61	DB5			
62, 63	DB6			
64, 65	DB7			
66	OPT_LCD	I	ITO Option	No ITO. (Option = 1): B-Type waveform ITO On. (Option = 0): A-Type waveform
68	TESTD	O	Test output	Test data output. (No connect for user)
164 - 157	COM1 - 8	O	LCD panel	Common signal output pins, for place on the upper glass (IC face up)
69 - 76,	COM9 - 16	O	LCD panel	
156 - 77	SEG1 - 80	O	LCD panel	Segment signal output pins
165	TEST	I	Test pin	Test pin (internal pull down) (No connection for user)
166	TESTM	O	Test output	LCD driver clock output. (No connection for user)
67, 27	GND_OUT	P		GND output pin, used for pull-down ITO option

Functional Description

The NT7603 is a dot-matrix LCD controller and driver LSI. It operates with either a 4-bit or an 8-bit microprocessor (MPU). The NT7603 receives both instructions and data from the MPU. Some instructions set operation modes, such as the function mode, data entry mode, and display mode; as well as some control LCD display functions, such as clear display, restore display, shift display, and cursor. Other instructions include reading and writing both data and addresses. All instructions allow users convenient and powerful functions to control the LCD dot-matrix displays.

Data is written into, and read from the Data Display RAM (DD RAM) or the Character Generator RAM (CG RAM). As display character codes, the data stored in the DD RAM decodes a set of dot-matrix character patterns that are built into the Character Generator ROM (CG ROM). The CG ROM, with many character patterns (up to 256 patterns), defines the character pattern fonts. The NT7603 regularly scans the character patterns through the segment drivers. The CG RAM stores character pattern fonts at run time if users intend to show character patterns that are not defined in the CG ROM. This feature makes character display flexible. Other unused bytes can be used as general-purpose data storage.

The LCD driver circuit consists of 16 common signal drivers and 80 segment signal drivers allowing a variety of application configurations to be implemented.

Character Generator ROM (CG ROM)

The character generator ROM generates LCD dot character patterns from the 8-bit character pattern codes. The NT7603 provides 2 CG ROM configurations:

1. 192 Characters:

The CG ROM contains 160 5 X 8 dot character patterns and 32 5 X 10 dot character patterns. The relation between the character codes and character patterns is shown in Table 1. The character codes from 00H to 0FH are used to get character patterns from the CG RAM. Character codes from 10H to 1FH, from 80H to 9FH and 20H map to null character patterns. Character codes from E0H to FFH are assigned to generate 5 X 10 dot character patterns, and other codes are used to generate 5x8 dot character patterns.

2. 240 Characters:

The CG ROM contains 192 5 X 8 dot character patterns and 48 5 X 10 dot character patterns. The relation between the character codes and character patterns is shown in Table 2. The character codes from 00H to 0FH are used to get character patterns from the CG RAM. Character codes from 10H to 1FH and from E0H to FFH are assigned to generate 5 X 10 dot character patterns, and other codes to generate 5 X 8 dot character patterns. Only one null character pattern exists in this type. Note that the underlined cursor, displayed on the 8th duty may be obscure if the 8th row of a dot character pattern is coded. We recommend that users display the cursor in the blinking mode if they code 5x8 dot character patterns as their custom CG ROM.

Custom character patterns are available by mask-programming ROM. For convenience of character pattern development, NOVATEK has developed a user-friendly editor program for the NT7603 to help determine the character patterns users prefer. By executing the program on the computer, users can easily create and modify their character patterns. By transferring the resulting files generated by the program through a modem or some other communication method, the user and NOVATEK will have established a reliable, fast link for programming the CG ROM.

Absolute Maximum Ratings*

Power Supply Voltage (V_{DD}) . . . . . -0.3V to + 7.0V
Power Supply Voltage (V_1 to V_5) . . . . . GND to V_{DD} + 0.3V
Input Voltage (V_I) . . . . . -0.3V to V_{DD} + 0.3V
Operating Temperature (T_{OPR}) . . . . . -20°C to + 70°C
Storage Temperature (T_{STG}) . . . . . -55°C to + 125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

- All voltage values are referenced to GND = 0V
- V_1 to V_5, must maintain $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq GND$

DC Electrical Characteristics (V_{DD} = 5.0V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin
V_{DD}	Operating Voltage	2.8	5.0	5.5	V		
V_{IH1}	"H" Level Input Voltage (1)	0.8 V_{DD}	-	V_{DD}	V		DB0 - DB7, RS, R/W,
V_{IL1}	"L" Level Input Voltage (1)	-0.3	-	0.2 V_{DD}	V		E,OSC1
V_{OH1}	"H" Level Output Voltage (1)	V_{DD} - 0.6	-	-	V	I_{OH} = -1.2mA	DB0 - DB7
V_{OL1}	"L" Level Output Voltage (1)	-	-	GND + 0.6	V	I_{OL} = 1.2mA	(CMOS)
V_{COM}	Driver Voltage Descending (COM)	-	-	0.3	V	I_D = 5μA	COM1 - 16
V_{SEG}	Driver Voltage Descending (SEG)	-	-	0.3	V	I_D = 5μA	SEG1 - 80
I_{IL}	Input Leakage Current	-1	-	1	μA	V_{IN} = 0 to V_{DD}	Not include OSC1
-I_P	Pull-up MOS Current	50	125	250	μA	V_{DD} = 5V	RS, R/W, DB0-DB7
I_{OP}	Power Supply Current	-	1	1.5	mA	Rf oscillation, from external clock V_{DD} = 5V, f_{OSC} = f_{CP} = 540KHz, include LCD bias current.	V_{DD}
External Clock Operation							
fCP	External Clock Operating Frequency	380	540	750	KHz		
tDUTY	External Clock Duty Cycle	45	50	55	%		
tRCP	External Clock Rising Time	0.1	-	0.5	μS		
tFCP	External Clock Falling Time	0.1	-	0.5	μS		
Internal Clock Operation (Built-in RC Oscillator)							
fOSC	Oscillator Frequency	380	540	750	KHz	V_{DD} = 2 .8V ~ 5.5V	
VLCD	LCD Driving Voltage	3.0	-	V_{DD}	V	V_{DD} - V5	

DC Electrical Characteristics (continued) (V_{DD} = 3.0V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin
V_{DD}	Operating Voltage	2.8	3.0	5.5	V		
V_{IH1}	"H" Level Input Voltage (1)	0.8 V_{DD}	-	V_{DD}	V		DB0 - DB7, RS, R/W,
V_{IL1}	"L" Level Input Voltage (1)	-0.3	-	0.2 V_{DD}	V		E,OSC1
V_{OH1}	"H" Level Output Voltage (1)	V_{DD} - 0.4	-	-	V	I_{OH} = -0.8mA	DB0 - DB7
V_{OL1}	"L" Level Output Voltage (1)	-	-	GND + 0.4	V	I_{OL} = 0.8mA	(CMOS)
V_{COM}	Driver Voltage Descending (COM)	-	-	0.3	V	I_D = 5μA	COM1 - 16
V_{SEG}	Driver Voltage Descending (SEG)	-	-	0.3	V	I_D = 5μA	SEG1 - 80
I_{IL}	Input Leakage Current	-1	-	1	μA	V_{IN} = 0 to V_{DD}	Not include OSC1
-I_P	Pull-up MOS Current	30	75	150	μA	V_{DD} = 3V	RS, R/W, DB0-DB7
I_{OP}	Power Supply Current	-	1	1.5	mA	Rf oscillation, from external clock V_{DD} = 3.0V, f_{OSC} = f_{CP} = 540KHz, include LCD bias current.	V_{DD}
External Clock Operation							
fCP	External Clock Operating Frequency	380	540	750	KHz		
tDUTY	External Clock Duty Cycle	45	50	55	%		
tRCP	External Clock Rising Time	0.1	-	0.5	μS		
tFCP	External Clock Falling Time	0.1	-	0.5	μS		
Internal Clock Operation (Built-in RC Oscillator)							
fOSC	Oscillator Frequency	380	540	750	KHz	Rf = 50KΩ (reference only) V_{DD} = 2 .8V ~ 5.5V	
VLCD	LCD Driving Voltage	2.5	-	V_{DD}	V	V_{DD} - V5	

AC Characteristics

Read Cycle (V_{DD} = 5.0V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 1
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 1
t_{RE}, t_{FE}	Enable Rising/Falling Time	-	-	25	ns	Figure 1
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 1
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 1
t_{RD}	Read Data Output Delay	-	-	190	ns	Figure 1
t_{DHR}	Read Data Hold Time	20	-	-	ns	Figure 1

Write Cycle (V_{DD} = 5.0V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 2
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 2
t_{RE}, t_{FE}	Enable Rising/Falling Time	-	-	25	ns	Figure 2
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 2
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 2
t_{DS}	Data Output Delay	100	-	-	ns	Figure 2
t_{DHW}	Data Hold Time	10	-	-	ns	Figure 2

Notes: 1: 8-bit operation mode
2: 4-bit operation mode

Power Supply Conditions Using Internal Reset Circuit

(VDD = 5.0V, GND = 0V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{RON}	Power Supply Rising Time	0.1	-	10	ms	Figure 3
t_{OFF}	Power Supply OFF Time	1	-	-	ms	Figure 3

AC Characteristics (continued)

Read Cycle (V_{DD} = 3.0V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 1
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 1
t_{RE}, t_{FE}	Enable Rising/Falling Time	-	-	25	ns	Figure 1
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 1
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 1
t_{RD}	Read Data Output Delay	-	-	190	ns	Figure 1
t_{DHR}	Read Data Hold Time	20	-	-	ns	Figure 1

Write Cycle (V_{DD} = 3.0V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 2
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 2
t_{RE}, t_{FE}	Enable Rising/Falling Time	-	-	25	ns	Figure 2
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 2
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 2
t_{DS}	Data Output Delay	150	-	-	ns	Figure 2
t_{DHW}	Data Hold Time	10	-	-	ns	Figure 2

Notes: 1: 8-bit operation mode
2: 4-bit operation mode

Power Supply Conditions Using Internal Reset Circuit

(V_{DD} = 3.0V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{RON}	Power Supply Rising Time	0.1	-	10	ms	Figure 3
t_{OFF}	Power Supply OFF Time	1	-	-	ms	Figure 3

Timing Waveforms

Read Operation

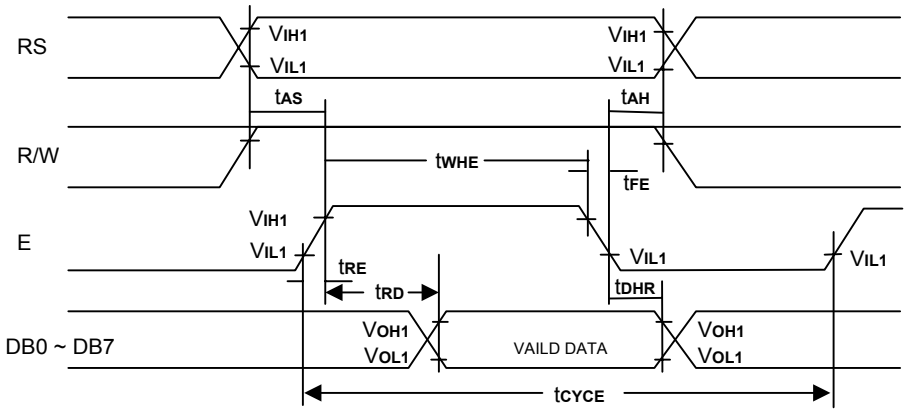


Figure 1. Bus Read Operation Sequence
(Reading out data from NT7603 to 8-bit MPU)

Write Operation

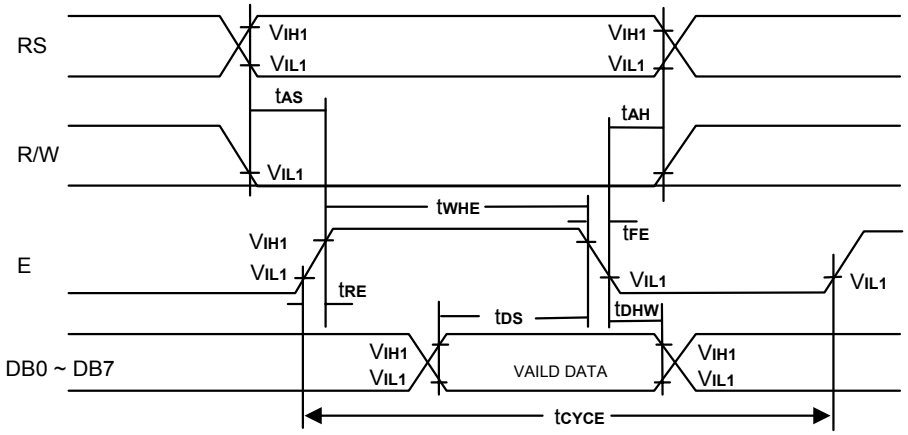


Figure 2. Bus Write Operation Sequence
(Writing data from 8-bit MPU to NT7603)

Interface Signals with Segment Driver LSI

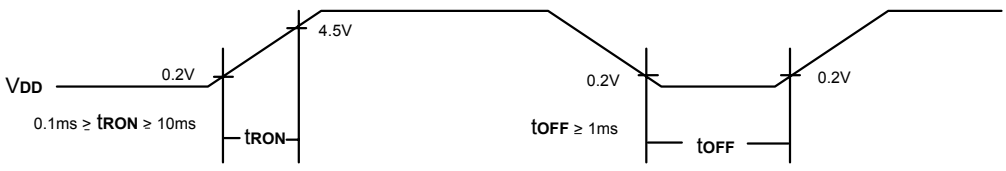
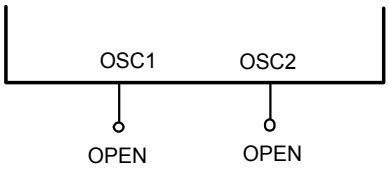


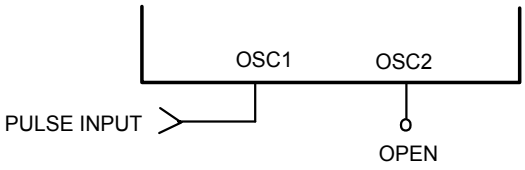
Figure 3. t_{OFF} stipulates the time of power OFF for instantaneous
Power supply to or when power supply repeats ON and OFF

Note 1: The NT7603 has two clock options:

A. Internal Oscillator (Built-in RC)



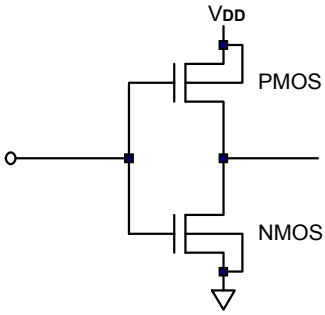
B. External Clock Operation



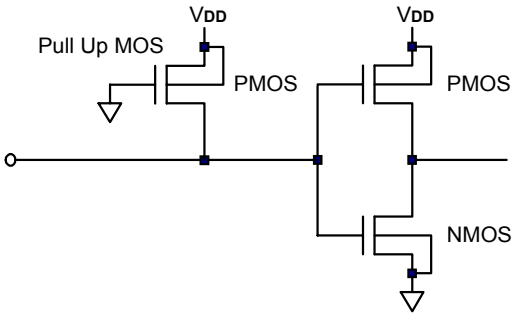
Note 2: Input/Output Terminals:

A. Input Terminal

Applicable Terminal: E (No Pull Up MOS)

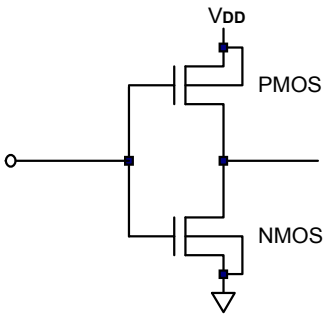


Applicable Terminal: RS, R/W (with Pull Up MOS)



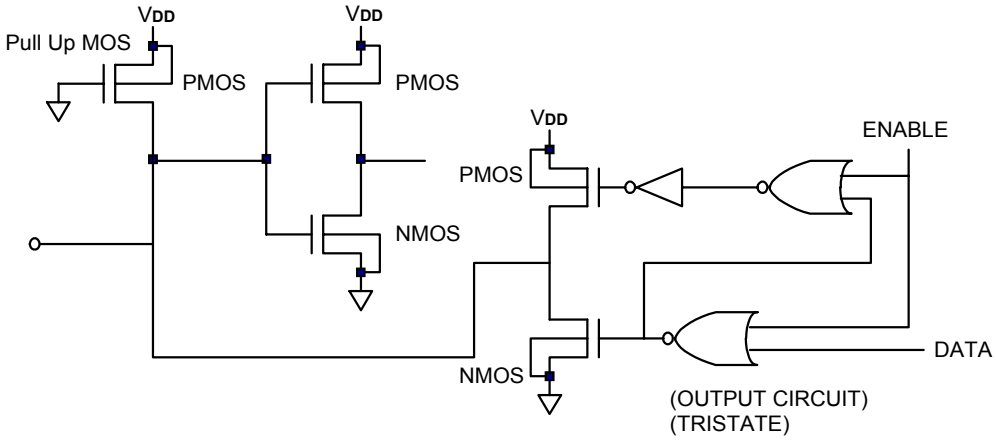
B. Output Terminal

Applicable Terminal: TESTM



C I/O Terminal

Applicable Terminal: DB0 to DB7



Note 3: ITO Options:

Set Option = 0: Place ITO on the Option Pad
Set Option = 1: No ITO on the Option Pad

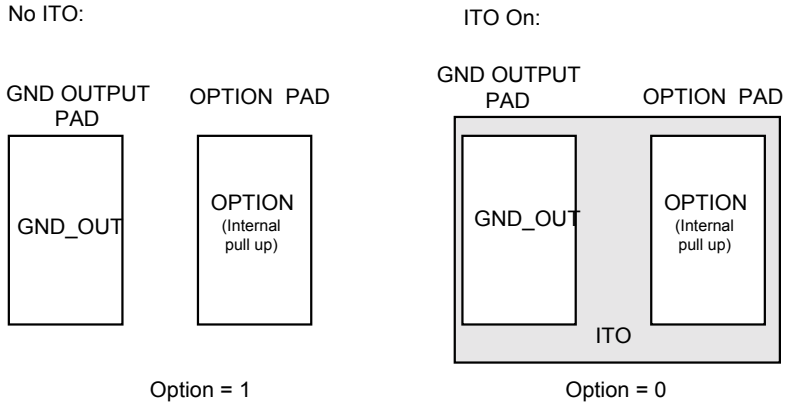


Table 1. NT7603H-BDT01 Correspondence between Character Codes and Character Patterns (NOVATEK Standard 192 Character CG ROM)

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

Instruction Set

Instruction	Code										Function	Execution time (max) (fOSC = 540KHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area, Restore display from shift, and load address counter with DD RAM address 00H.	1.64ms
Display/ Cursor Home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00H.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specify direction of cursor movement and display shift mode. This operation takes place after each data transfer (read/write).	40μs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D) cursor (C) and blinking of character at cursor position (B).	40μs
Display/ Cursor Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor.	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Set interface data length (DL), number of display line (N), and character font (F).	40μs
RAM Address Set	0	0	0	1	ACG						Load the address counter with a CG RAM address. Subsequent data access is for CG RAM data.	40μs
DD RAM Address Set	0	0	1	ADD							Load the address counter with a DD RAM address. Subsequent data access is for DD RAM data.	40μs
Busy Flag/ Address Counter Read	0	1	BF	AC							Read Busy Flag (BF) and contents of Address Counter (AC).	1μs
CG RAM/ DD RAM Data Write	1	0	Write data								Write data to CG RAM or DD RAM.	40μs
CG RAM/ DD RAM Data Read	1	1	Read data								Read data from CG RAM or DD RAM.	40μs
	I/D = 1 : Increment S = 1 : Display Shift On D = 1 : Display On C = 1 : Cursor Display On B = 1 : Cursor Blink On S/C = 1 : Shift Display R/L = 1 : Shift Right DL = 1 : 8-Bit N = 1 : Dual Line F = 1 : 5x10 dots BF = 1 : Internal Operation BF = 0 : Ready for Instruction						I/D = 0 : Decrement S/C = 0 : Move Cursor R/L = 0 : Shift Left DL = 0 : 4-Bit N = 0 : Signal Line F = 0 : 5 X 8 dots				DD RAM : Display Data RAM CG RAM : Character Generator RAM ACG : Character Generator RAM Address ADD : Display Data RAM Address AC : Address Counter	

Note 1: Symbol "*" signifies an insignificant bit (disregard).
Note 2: Correct input value for "N" is predetermined for each model.
Note 3: The variation of execution time depends on the change of oscillator frequency; for example:
if fOSC = 380KHz, then execution time = 40μs✕ (540KHz / 380KHz) = 57μs

Interface to LCD

(1) Character Font and Number of Lines

The NT7603 provides a 5 X 7 dot character font 1-line mode, a 5 X 10 dot character font 1-line mode and a 5 X 7 dot character font 2-line mode, as shown in the table below.

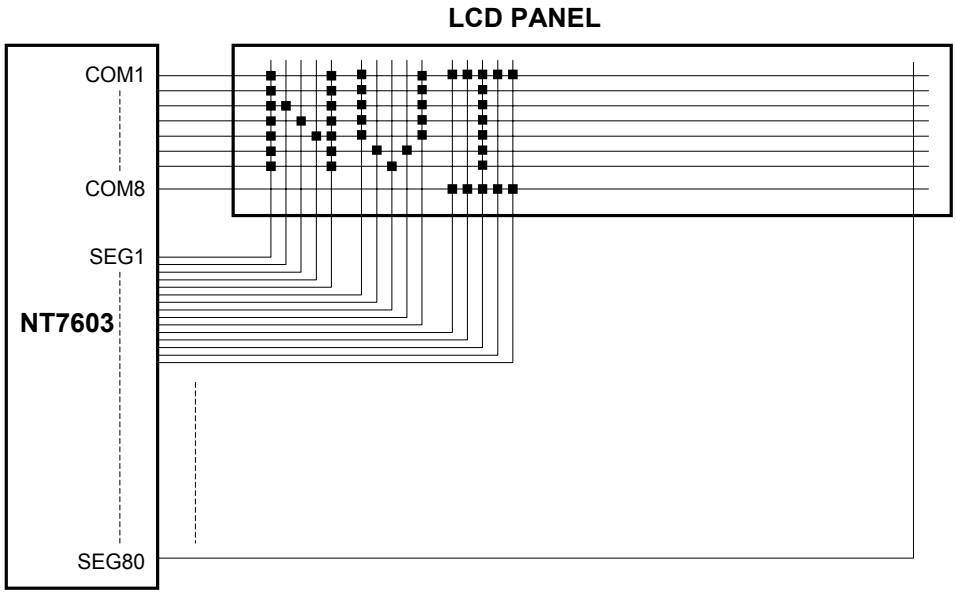
Three types of common signals are available as displayed in the table. The number of lines and the font type can be selected by the program.

Number of Lines	Character Font	Number of Common Signals	Duty Factor	Bias
1	5 X 7 dots + Cursor (or 5 X 8 dots)	8	1/8	1/4
1	5 X 10 dots + Cursor	11	1/11	1/4
2	5 X 7 dots + Cursor (or 5 X 8 dots)	16	1/16	1/5

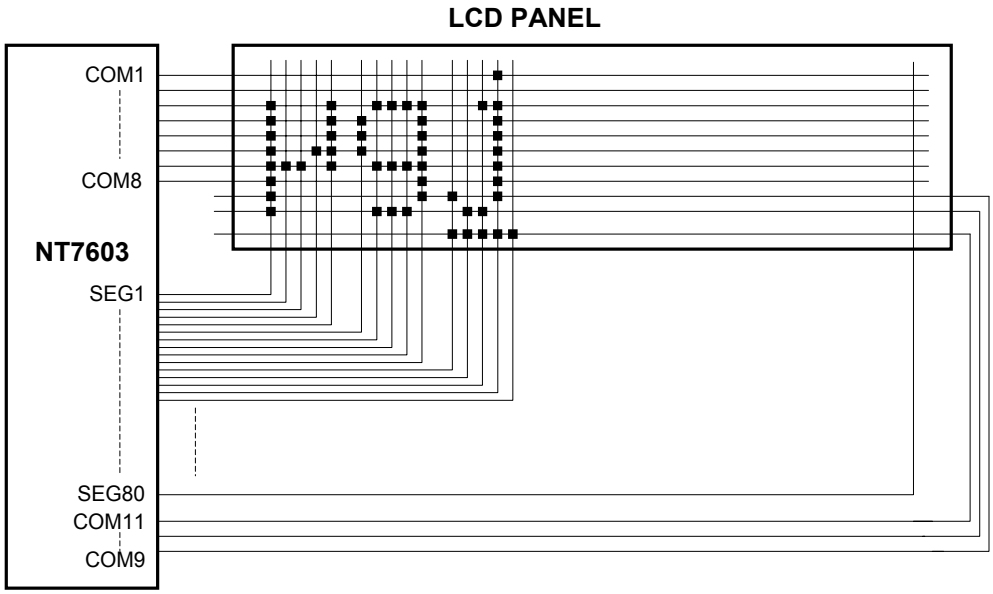
(2) Connection to LCD

The following 4 LCD connection examples show the various combinations between characters and lines. NT7603 can directly drive the following combinations:

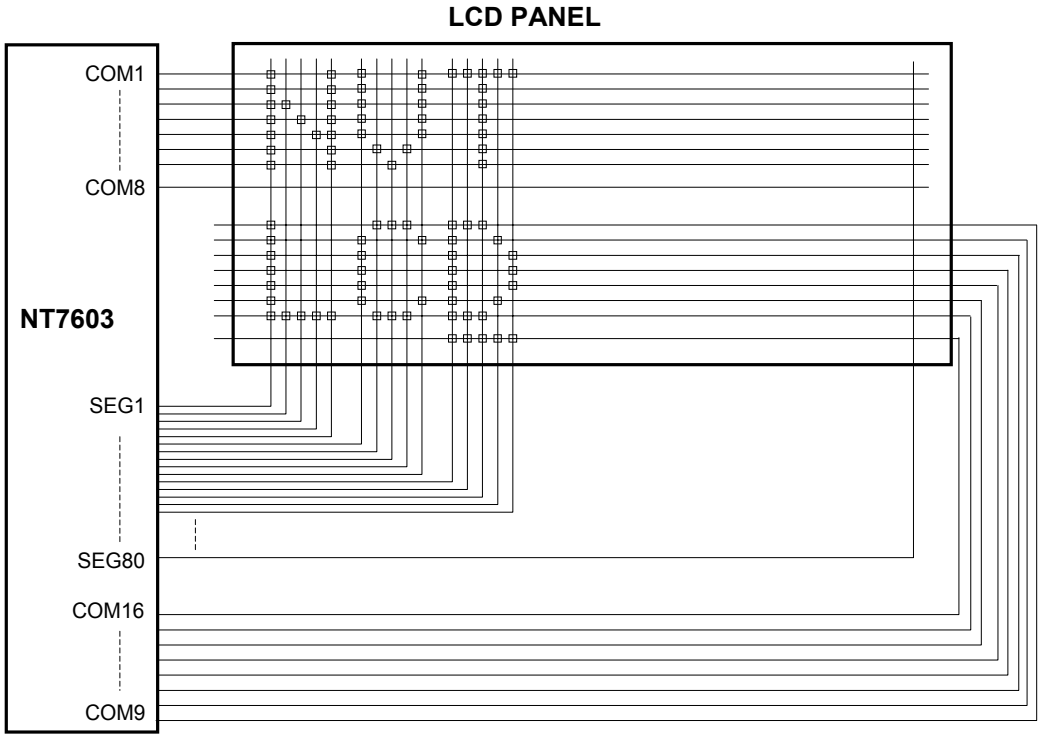
(a) 5 X 8 Font - 16 character X 1 line (1/8 duty cycle, 1/4 bias)



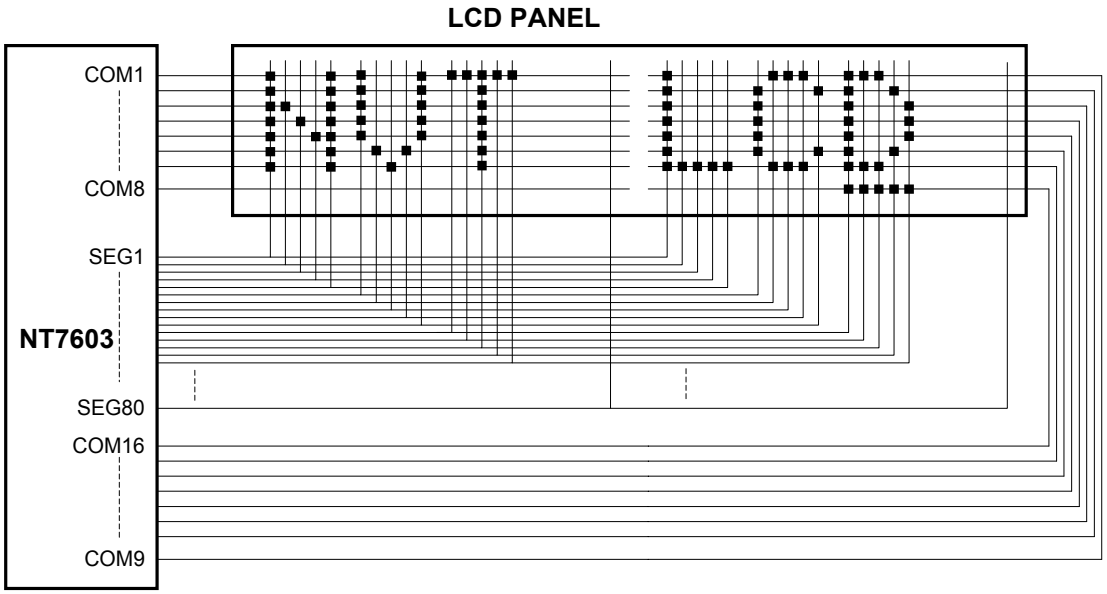
(b) 5 X 10 Font - 16 character X 1 line (1/11 duty cycle, 1/4 bias)



(c) 5 X 8 Font - 16 character X 2 line (1/16 duty cycle, 1/5 bias)

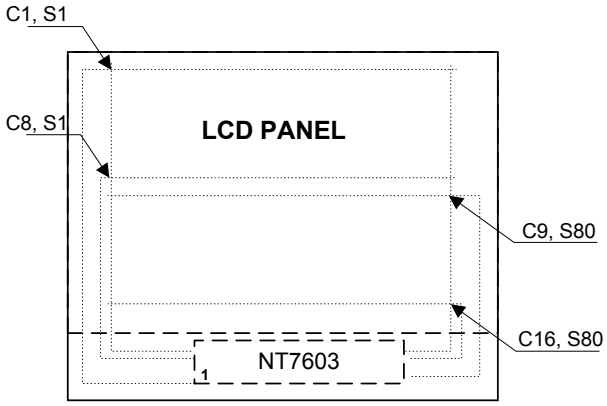


(d) 5 X 8 Font - 32 character X 1 line (1/16 duty cycle, 1/5bias)



(3) Orientation type of NT7603:

Place the chip on the upper glass (IC face up)



(4) Bias Power Connection

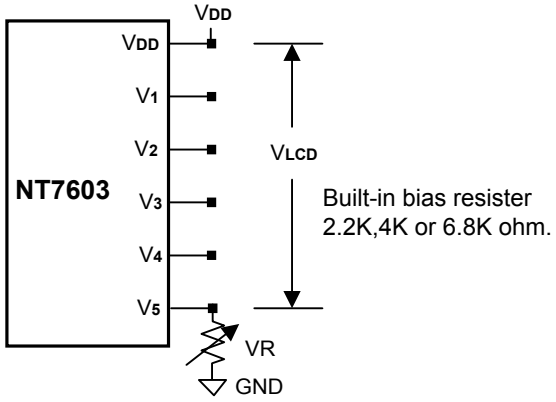
NT7603 provides 1/4 or 1/5 bias for various duty cycle applications. The built-in power division resistor divide voltage is described in the following table. The division resistor is the connection of the NT7603, power supply, and resistors are also shown as follows:

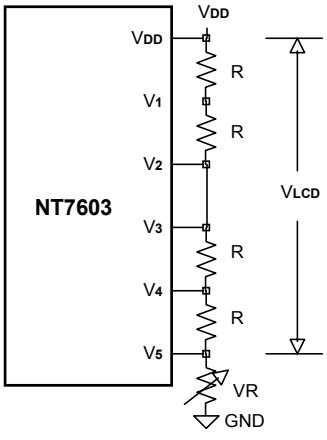
Power Division	1/8, 1/11 Duty Cycle - 1/4 Bias	1/16 Duty Cycle - 1/5 Bias
V_1	V_{DD} - 1/4 V_{LCD}	V_{DD} - 1/5 V_{LCD}
V_2	V_{DD} - 1/2 V_{LCD}	V_{DD} - 2/5 V_{LCD}
V_3	V_{DD} - 1/2 V_{LCD}	V_{DD} - 3/5 V_{LCD}
V_4	V_{DD} - 3/4 V_{LCD}	V_{DD} - 4/5 V_{LCD}
V_5	V_{DD} - V_{LCD}	V_{DD} - V_{LCD}

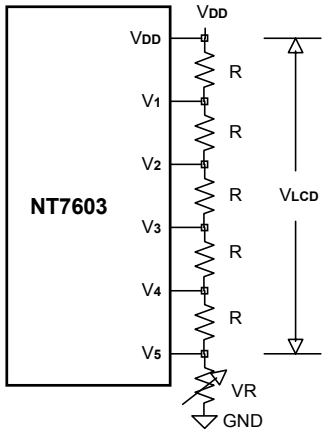
The bias is auto selected by duty cycle. When the LCD is set to 1/16 duty, the bias is set to 1/5. Otherwise, the bias is set to 1/4.

The ITO Option can then select the division resistor value:

OPT_R1	OPT_R0	Division Resister
No ITO (1)	No ITO (1)	2.2KΩ
No ITO (1)	ITO On (0)	4KΩ
ITO On (0)	No ITO (1)	6.8KΩ
ITO On (0)	No ITO (0)	No built-in resister (external input)



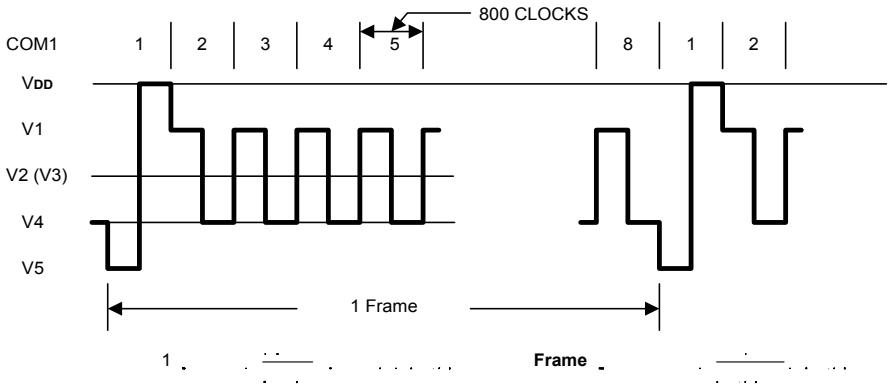




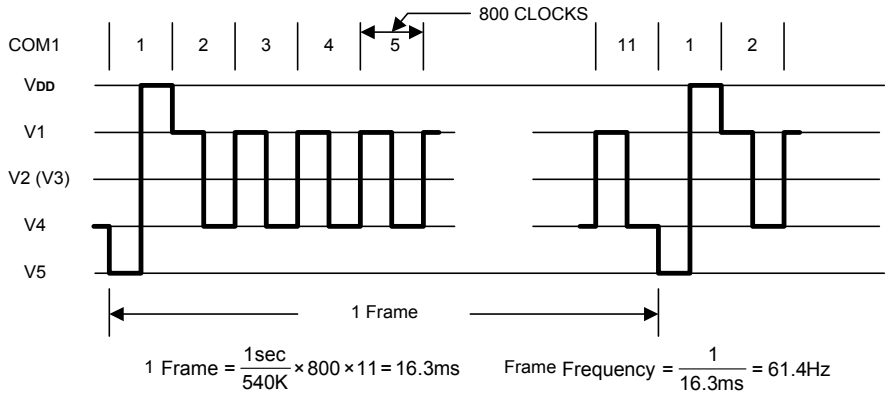
Exit Power division. (The resistance value depends on the LCD panel size)

(4) LCD Waveform

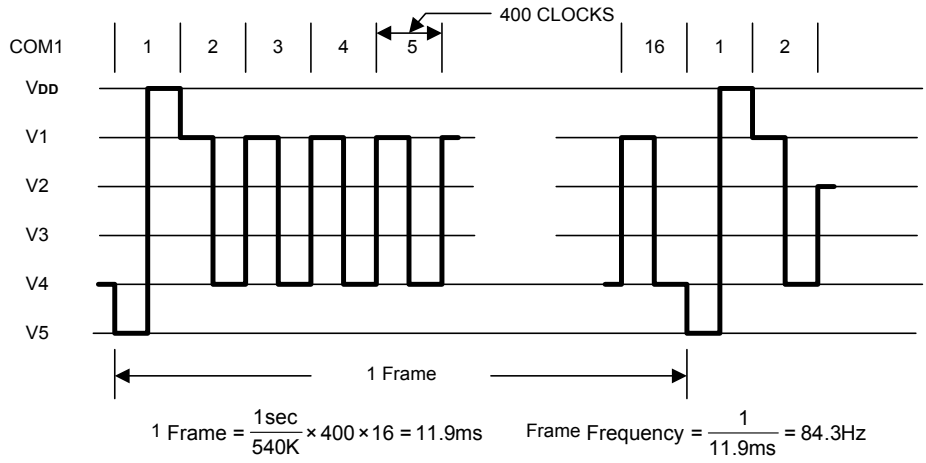
A-type, 1/8 Duty Cycle, 1/4 Bias



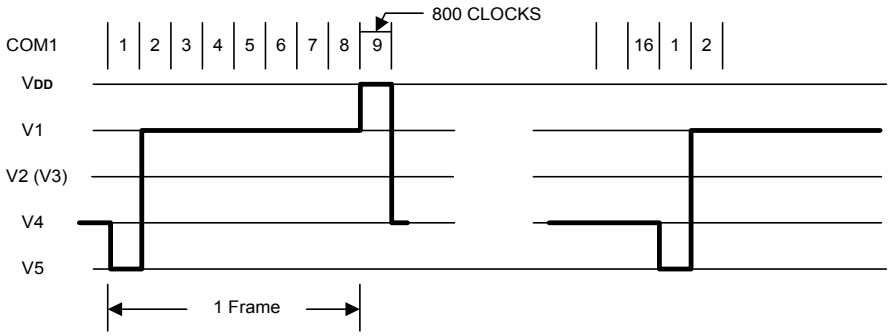
A-type, 1/11 Duty Cycle, 1/4 Bias



A-type, 1/16 Duty Cycle, 1/5 Bias

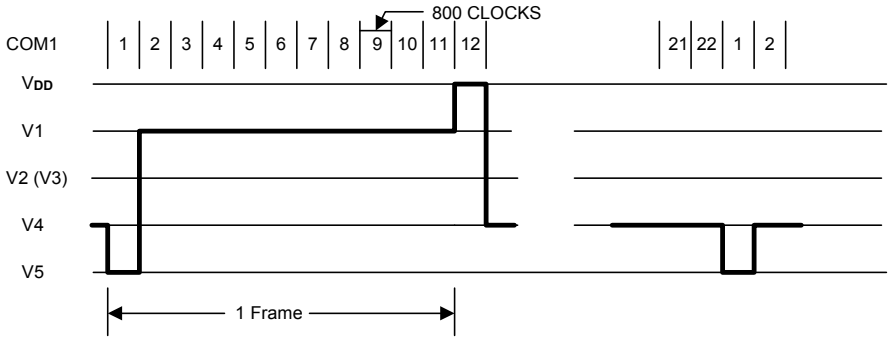


B-type, 1/8 Duty Cycle, 1/4 Bias



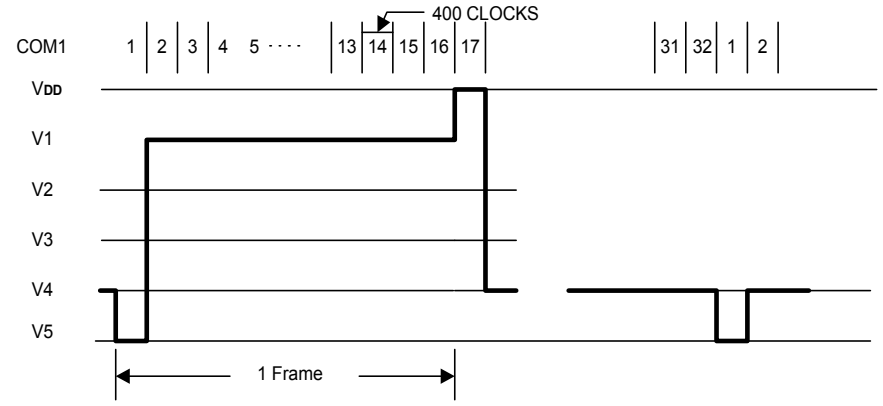
$$1\text{Frame} = \frac{1\text{sec}}{540\text{K}} \times 800 \times 8 = 11.9\text{ms} \qquad \text{Frame Frequency} = \frac{1}{11.9\text{ms}} = 84.3\text{Hz}$$

B-type, 1/11 Duty Cycle, 1/4 Bias



$$1\text{Frame} = \frac{1\text{sec}}{540\text{K}} \times 800 \times 11 = 16.3\text{ms} \qquad \text{Frame Frequency} = \frac{1}{16.3\text{ms}} = 61.4\text{Hz}$$

B-type, 1/16 Duty Cycle, 1/5 Bias



Low Voltage Reset

The Low voltage reset function is used to monitor the supply voltage and applies an internal reset at the time when low voltage is detected.

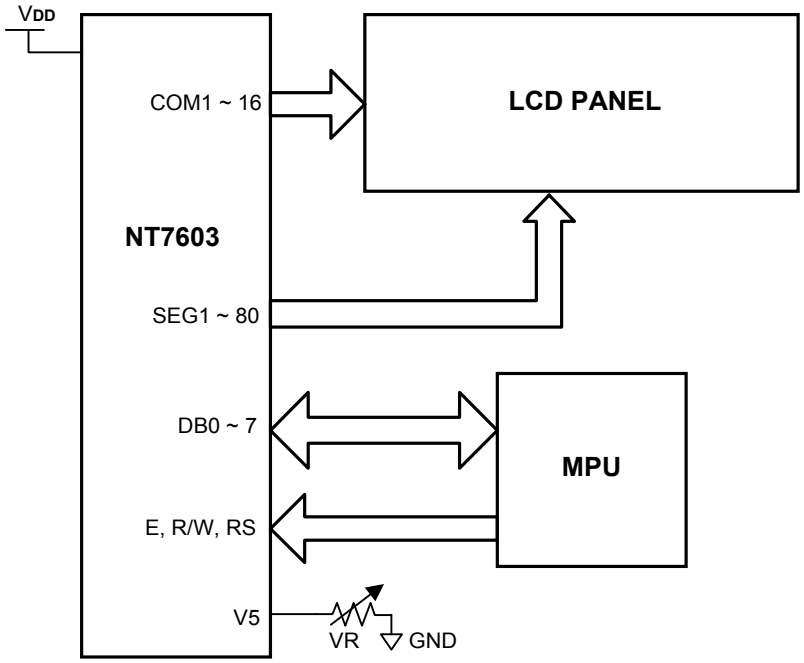
Functions of the Low Voltage Reset Circuit

The Low voltage reset circuit has the following functions:

- Generates an internal reset signal when $V_{DD} \leq V_{LVR}$
- Cancels the internal reset signal when $V_{DD} > V_{LVR}$

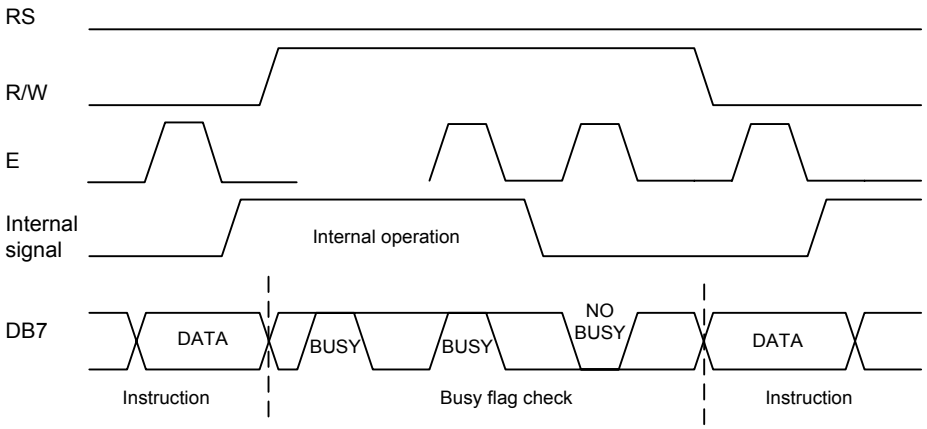
Here, V_{DD}: power supply voltage, V_{LVR}: Low voltage reset detect voltage, about 2.0V.

Application Circuit (for reference only)

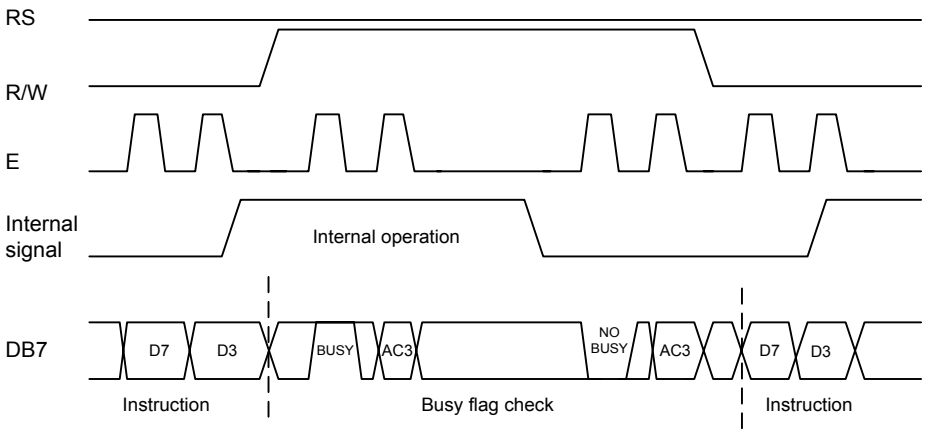


Example (for reference only)

Interface with 8-bit MPU

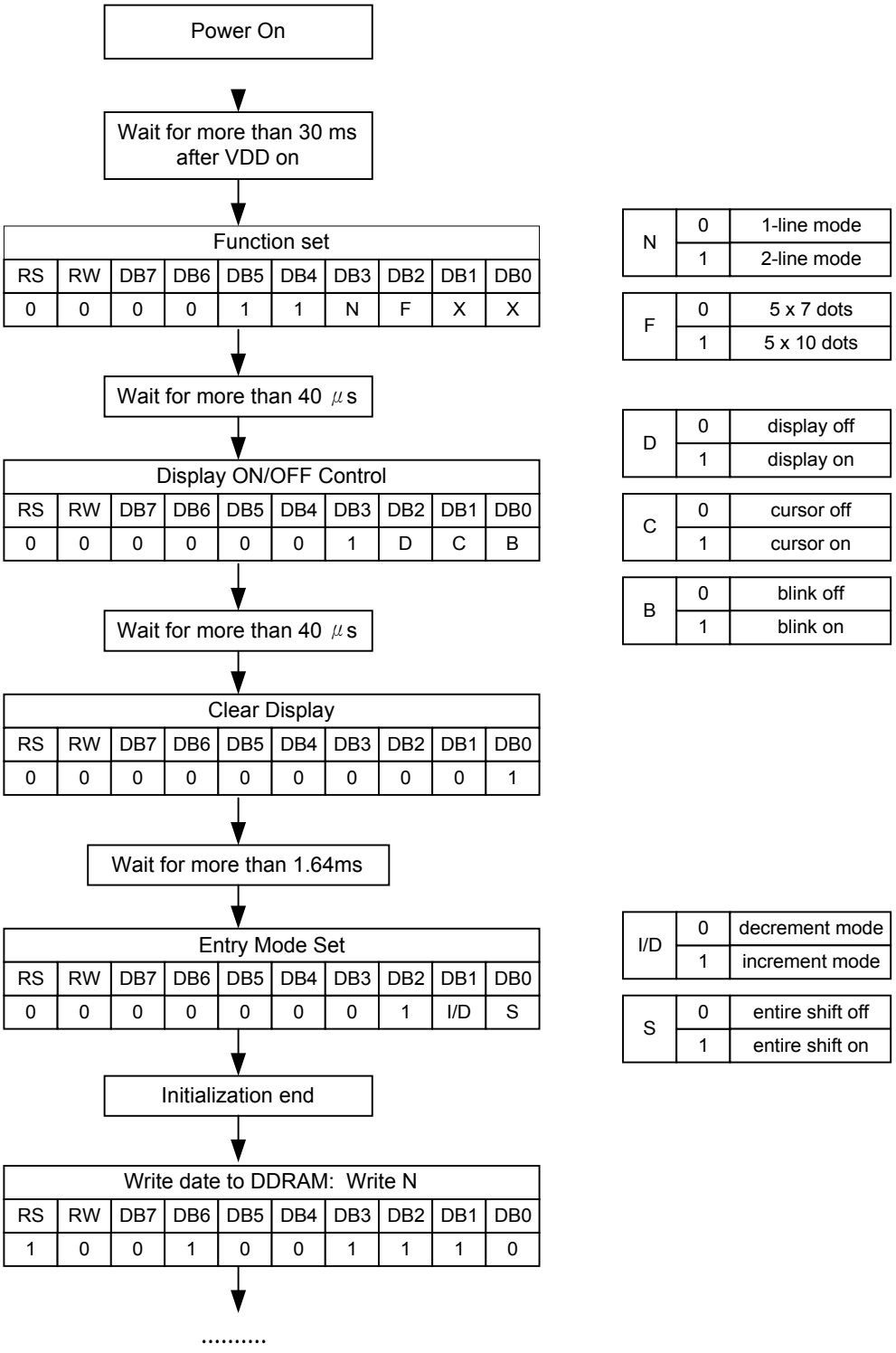


Interface with 4-bit MPU

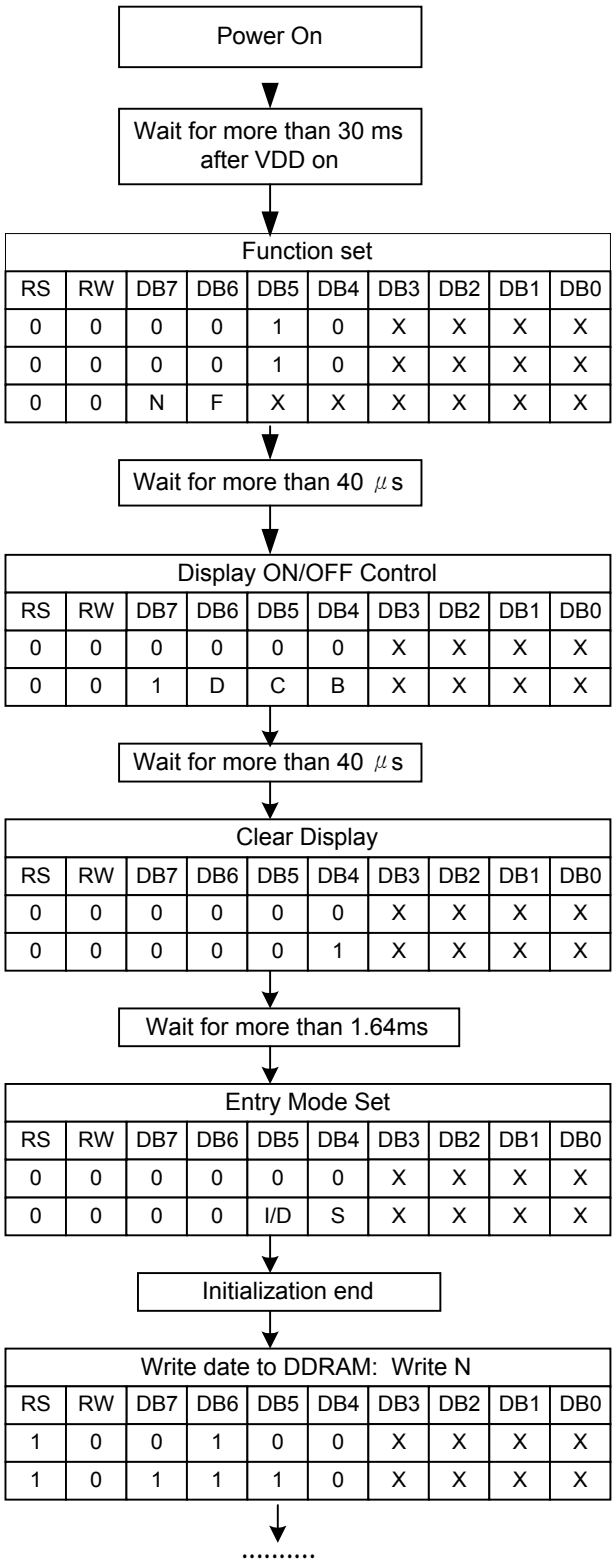


Initializing by instruction

1. 8-bit interface



2. 4-bit interface



N	0	1-line mode
	1	2-line mode
F	0	5 x 7 dots
	1	5 x 10 dots
D	0	display off
	1	display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on
I/D	0	decrement mode
	1	increment mode
S	0	entire shift off
	1	entire shift on

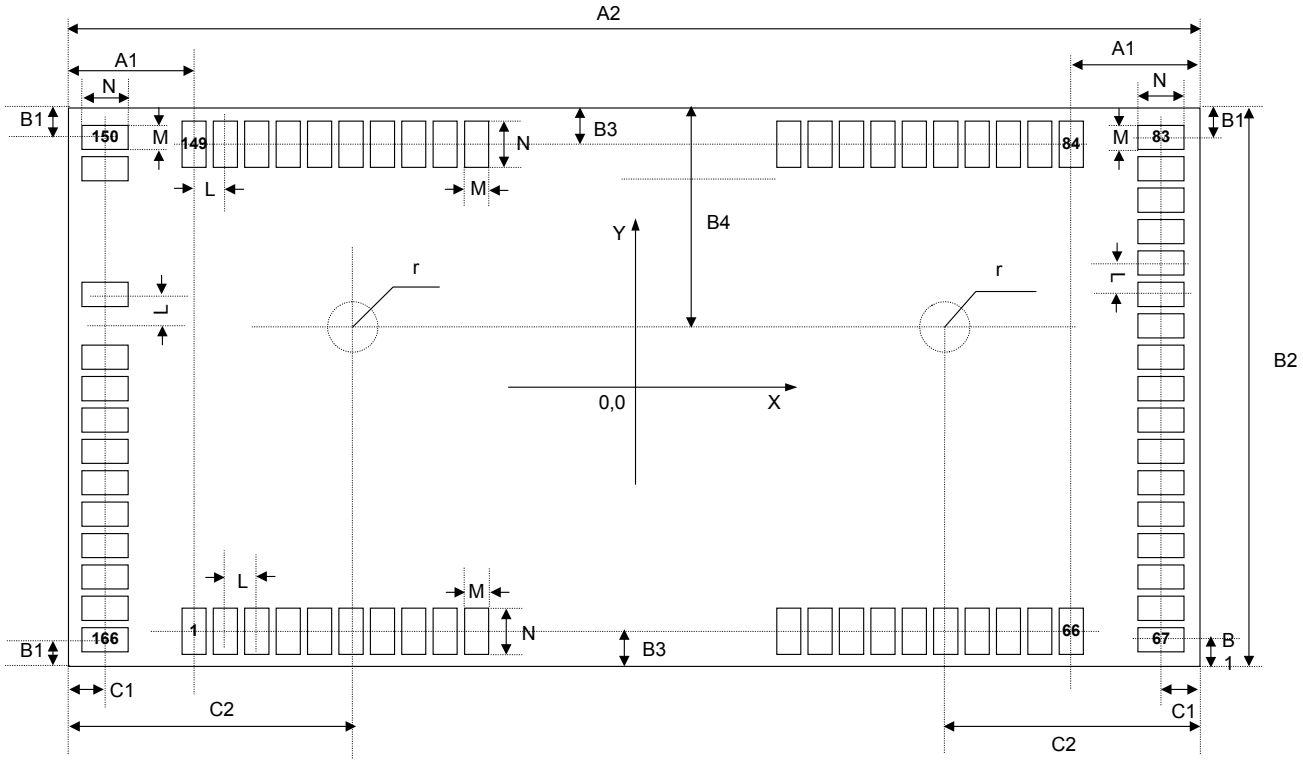
Ordering Information

Part No.	CG ROM	Package	Shipment Style
NT7603H-BDB01	192 CGROM (ref P13)	COG CHIP FORM	Bumped Die on Blue tape
NT7603H-BDT01	192 CGROM (ref P13)	COG CHIP FORM	Bumped Die on chip Tray
NT7603-BDW01	192 CGROM (ref P13)	COG CHIP FORM	Bumped Die on Wafer

Pad Configuration of NT7603

Unit: μm

Chip Window: 1220 X 5010 μm^2



A1	230	C1	66
A2	5010	C2	511.55
B1	50	r	35
B2	1220	M	42
B3	70	N	90
B4	500.2	L	70

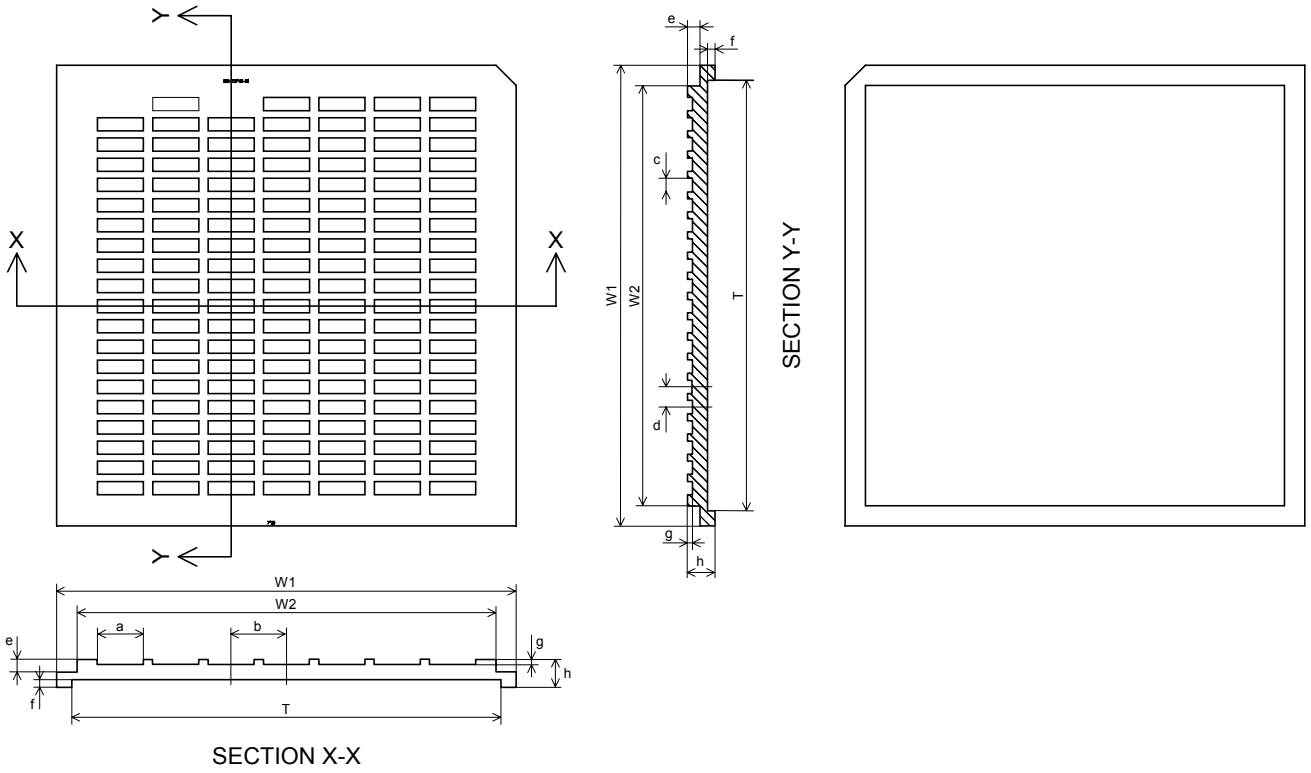
PAD Location

NO.	PAD NAME	X	Y	NO.	PAD NAME	X	Y
1	GND	-2275	-540	13	GND	-1435	-540
2	GND	-2205	-540	14	GND	-1365	-540
3	GND	-2135	-540	15	GND	-1295	-540
4	GND	-2065	-540	16	OSC1	-1225	-540
5	GND	-1995	-540	17	OSC2	-1155	-540
6	GND	-1925	-540	18	V1	-1085	-540
7	GND	-1855	-540	19	V2	-1015	-540
8	GND	-1785	-540	20	V3	-945	-540
9	GND	-1715	-540	21	V4	-875	-540
10	GND	-1645	-540	22	V5	-805	-540
11	GND	-1575	-540	23	V5	-735	-540
12	GND	-1505	-540	24	V5	-665	-540

NO.	PAD NAME	X	Y	NO.	PAD NAME	X	Y
21	V4	-875	-540	67	GND	2439	-560
22	V5	-805	-540	68	TESTD	2439	-490
23	V5	-735	-540	69	COM[9]	2439	-420
24	V5	-665	-540	70	COM[10]	2439	-350
25	V5	-595	-540	71	COM[11]	2439	-280
26	OPT_R0	-525	-540	72	COM[12]	2439	-210
27	GND	-455	-540	73	COM[13]	2439	-140
28	OPT_R1	-385	-540	74	COM[14]	2439	-70
29	V_{DD}	-315	-540	75	COM[15]	2439	0
30	V_{DD}	-245	-540	76	COM[16]	2439	70
31	V_{DD}	-175	-540	77	SEG[80]	2439	140
32	V_{DD}	-105	-540	78	SEG[79]	2439	210
33	V_{DD}	-35	-540	79	SEG[78]	2439	280
34	V_{DD}	35	-540	80	SEG[77]	2439	350
35	V_{DD}	105	-540	81	SEG[76]	2439	420
36	V_{DD}	175	-540	82	SEG[75]	2439	490
37	V_{DD}	245	-540	83	SEG[74]	2439	560
38	V_{DD}	315	-540	84	SEG[73]	2275	540
39	V_{DD}	385	-540	85	SEG[72]	2205	540
40	V_{DD}	455	-540	86	SEG[71]	2135	540
41	V_{DD}	525	-540	87	SEG[70]	2065	540
42	V_{DD}	595	-540	88	SEG[69]	1995	540
43	V_{DD}	665	-540	89	SEG[68]	1925	540
44	RS	735	-540	90	SEG[67]	1855	540
45	RS	805	-540	91	SEG[66]	1785	540
46	RW	875	-540	92	SEG[65]	1715	540
47	RW	945	-540	93	SEG[64]	1645	540
48	E	1015	-540	94	SEG[63]	1575	540
49	E	1085	-540	95	SEG[62]	1505	540
50	DB[0]	1155	-540	96	SEG[61]	1435	540
51	DB[0]	1225	-540	97	SEG[60]	1365	540
52	DB[1]	1295	-540	98	SEG[59]	1295	540
53	DB[1]	1365	-540	99	SEG[58]	1225	540
54	DB[2]	1435	-540	100	SEG[57]	1155	540
55	DB[2]	1505	-540	101	SEG[56]	1085	540
56	DB[3]	1575	-540	102	SEG[55]	1015	540
57	DB[3]	1645	-540	103	SEG[54]	945	540
58	DB[4]	1715	-540	104	SEG[53]	875	540
59	DB[4]	1785	-540	105	SEG[52]	805	540
60	DB[5]	1855	-540	106	SEG[51]	735	540
61	DB[5]	1925	-540	107	SEG[50]	665	540
62	DB[6]	1995	-540	108	SEG[49]	595	540
63	DB[6]	2065	-540	109	SEG[48]	525	540
64	DB[7]	2135	-540	110	SEG[47]	455	540
65	DB[7]	2205	-540	111	SEG[46]	385	540
66	OPT_LCD	2275	-540	112	SEG[45]	315	540

NO.	PAD NAME	X	Y	NO.	PAD NAME	X	Y
113	SEG[44]	245	540	141	SEG[16]	-1715	540
114	SEG[43]	175	540	142	SEG[15]	-1785	540
115	SEG[42]	105	540	143	SEG[14]	-1855	540
116	SEG[41]	35	540	144	SEG[13]	-1925	540
117	SEG[40]	-35	540	145	SEG[12]	-1995	540
118	SEG[39]	-105	540	146	SEG[11]	-2065	540
119	SEG[38]	-175	540	147	SEG[10]	-2135	540
120	SEG[37]	-245	540	148	SEG[9]	-2205	540
121	SEG[36]	-315	540	149	SEG[8]	-2275	540
122	SEG[35]	-385	540	150	SEG[7]	-2439	560
123	SEG[34]	-455	540	151	SEG[6]	-2439	490
124	SEG[33]	-525	540	152	SEG[5]	-2439	420
125	SEG[32]	-595	540	153	SEG[4]	-2439	350
126	SEG[31]	-665	540	154	SEG[3]	-2439	280
127	SEG[30]	-735	540	155	SEG[2]	-2439	210
128	SEG[29]	-805	540	156	SEG[1]	-2439	140
129	SEG[28]	-875	540	157	COM[8]	-2439	70
130	SEG[27]	-945	540	158	COM[7]	-2439	0
131	SEG[26]	-1015	540	159	COM[6]	-2439	-70
132	SEG[25]	-1085	540	160	COM[5]	-2439	-140
133	SEG[24]	-1155	540	161	COM[4]	-2439	-210
134	SEG[23]	-1225	540	162	COM[3]	-2439	-280
135	SEG[22]	-1295	540	163	COM[2]	-2439	-350
136	SEG[21]	-1365	540	164	COM[1]	-2439	-420
137	SEG[20]	-1435	540	165	TEST	-2439	-490
138	SEG[19]	-1505	540	166	TESTM	-2439	-560
139	SEG[18]	-1575	540		ALK_L	-1993.45	109.8
140	SEG[17]	-1645	540		ALK_R	1993.45	109.8

Tray Information



Tray Outline Dimensions

unit: mm

Symbol	Dimensions in mm	Symbol	Dimensions in mm
a	5.33	g	0.85
b	5.93	h	4.05
c	1.52	W1	50.70
d	2.12	W2	45.50
e	1.75	T	45.75
f	1.45		

Product Spec. Change Notice

NT7603 Specification Revision History		
Version	**Content**	**Date**
2.2	Adding Note 3 and modified fosc from 270KHz to 540KHz (Page 14 , Document mistake corrected) Modify the number of clock in single duty from 400 to 800 (1/8 duty and 1/11 duty),200 to 400(1/16 duty) and fosc from 270K to 540K(Page 21) (Document mistake corrected)	Jun.2002
2.1	ROM Table deleted(Page 14) B-type waveform content modified(Page 20 , Document mistake corrected)	Apr.2002
2.0		Nov.2001
1.0	Original	Feb.2001