NOVATEK
聯 詠 科 技

Data Sheet

NT7606

16 Characters X 3 Lines + 80 icons

STN LCD Controller/Driver

V1.0

Revision History

NT7606 Specification Revision History		
Version	**Content**	**Data**
1.0	Released	December 2003

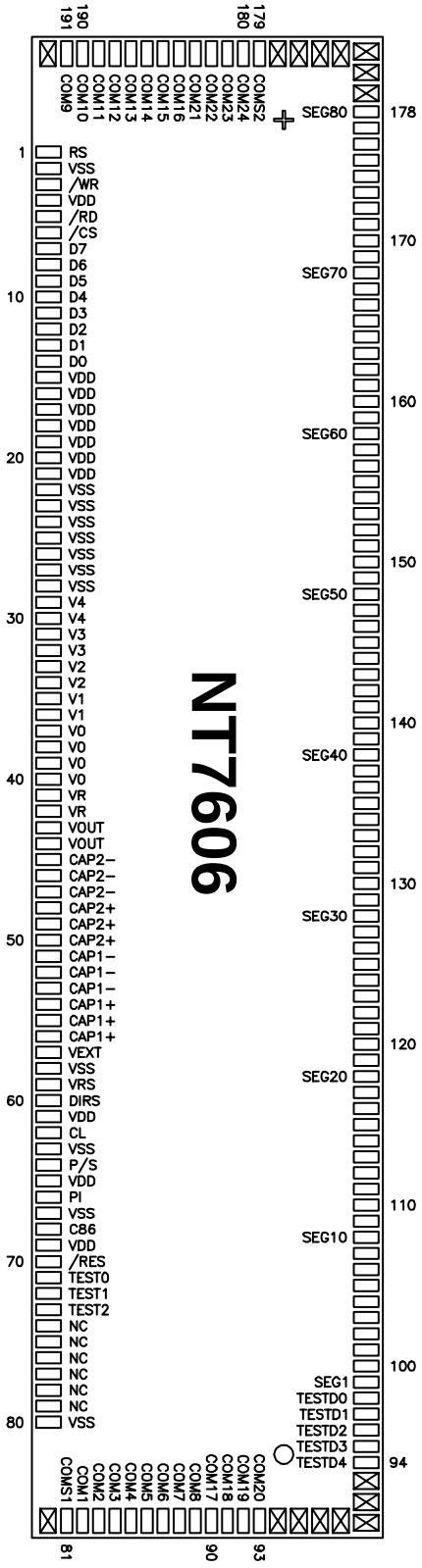
Features

- Single-chip LCD controller / driver
  - 26 common outputs
  - 80 segment outputs
- Applicable display panel
  - 2-line x 16 characters + 80 icons (1/17 duty)
  - 3-line x 16 characters + 80 icons (1/25 duty)
- 5 x 7 character format plus cursor; 5 x 8 for user defined symbols
- Character Generator ROM (CGROM)
  - 10,240 bits (256 characters x 5 x 8 dots)
  - Custom CGROM is also available
- Character Generator RAM (CGRAM): 320 bits (8 characters x 5 x 8 dots)
- Display Data RAM (DDRAM): 512 bits (16 characters x 4 lines x 8)
- Segment Icon Ram (ICONRAM): 80 bits (80 icons)
- Versatile functions provided on chip: Return home, Display control, Power save, Power control, etc.
- COM / SEG bi-directional (4-type LCD application available)
- On-chip oscillator requires no external components (external clock also possible)
- 2X / 3X DC-DC converter generation of LCD supply voltage
- Voltage regulator with electronic volume for contrast control (32 steps)
- Voltage follower & bias circuit
- Very low current consumption (VDD = 3.0 V):
  - Sleep mode: < 5 μA
  - Normal mode: < 80 μA
- Power supply voltage: VDD = 2.4~3.3 V
- Display supply voltage range (VLCD = V0 - VSS): VLCD = 4.0 to 6.0 V
- No busy check or no execution waiting time
- 4-bit or 8-bit parallel bus: 6800 and 8080
- Serial interface
- CMOS process
- Available in COG form

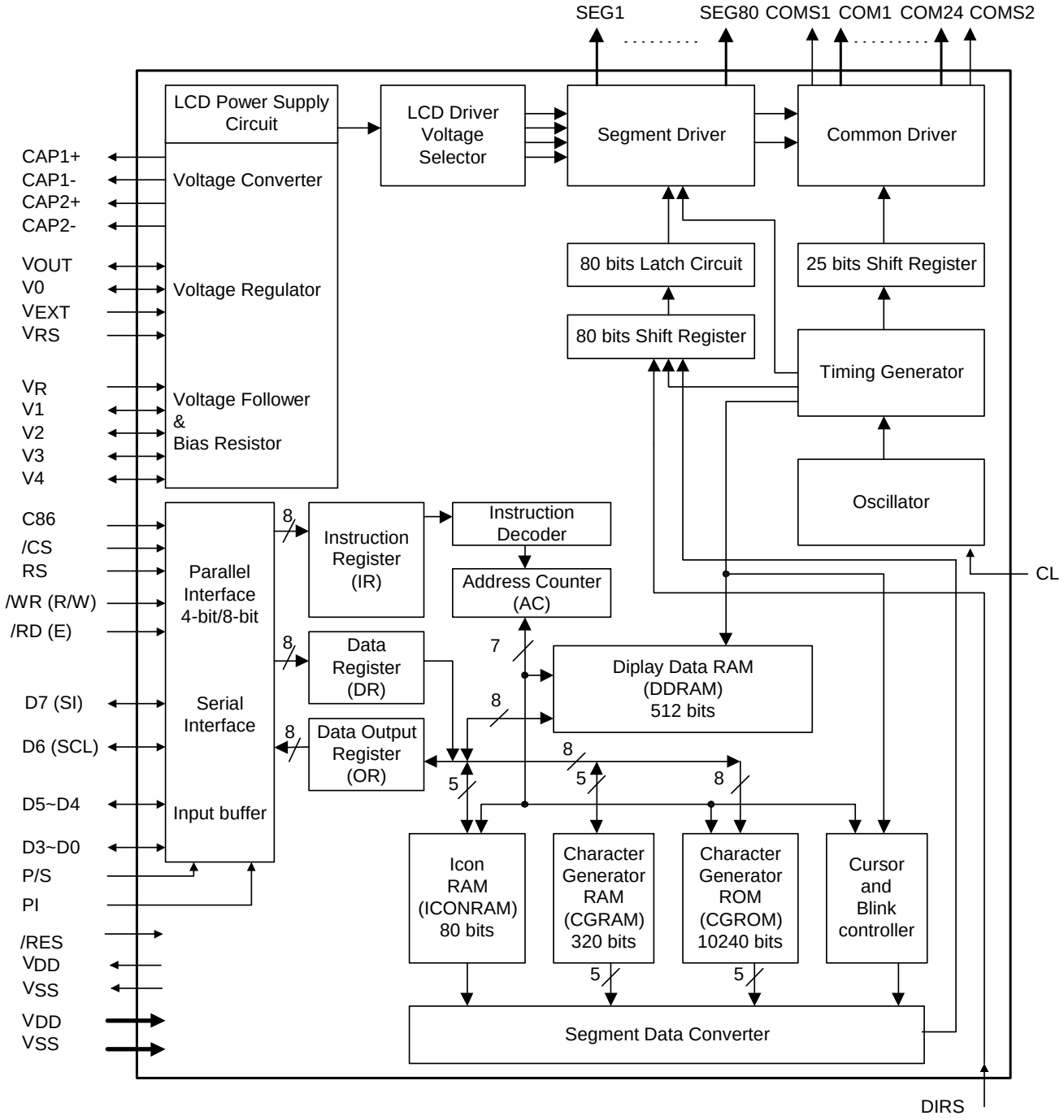
General Description

The NT7606 is a low power CMOS LCD controller and driver designed to drive a dot matrix LCD display of 2-line or 3-line by 16 characters with 5 × 8-dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The NT7606 interfaces to most micro-controllers via a 4-bit / 8-bit parallel bus or via the serial interface. The chip contains a character generator and displays alphanumeric character.

Pad Configuration



Block Diagram



Pad Descriptions

Power Supply

Pad No.	Designation	I/O	Description
15 – 21	VDD	P	2.4 - 3.3 V power supply input
22 – 28	VSS	P	Ground
4, 61, 65, 69	VDD	O	2.4 - 3.3 V power supply output for pad option
2, 58, 63, 67, 80	VSS	O	Ground output for pad option
37 – 40 35, 36 33, 34 31, 32 29, 30	V0 V1 V2 V3 V4	P	LCD driver supply voltages. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be the following relationship: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS When the on-chip operating power circuit is on, the following voltages are given to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the Set LCD Bias instruction.

LCD bias	V1	V2	V3	V4
1/4 bias	3/4 V0	2/4 V0		1/4 V0
1/5 bias	4/5 V0	3/5 V0	2/5 V0	1/5 V0

LCD Driver Supply

Pad No.	Designation	I/O	Description
51 – 53	CAP1-	O	Capacitor 1- pad for internal DC/DC voltage converter
54 – 56	CAP1+	O	Capacitor 1+ pad for internal DC/DC voltage converter
45 – 47	CAP2-	O	Capacitor 2- pad for internal DC/DC voltage converter
48 – 50	CAP2+	O	Capacitor 2+ pad for internal DC/DC voltage converter
43, 44	VOUT	I/O	DC/DC voltage converter output.
41, 42	VR	I	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.
57	VEXT	I	This is the external input reference voltage (VREF) instead of the internal voltage regulator, 2 V. It is valid only when external VREF is used. When using internal VREF, this pad must be NC.
59	VRS	I	Select the internal voltage regulator or external voltage regulator, VRS = “L”: using the internal VREF (2 V). VRS = “H”: using the external VREF, through VEXT pad input.

System Bus Connection Pads

Pad No.	Designation	I/O	Description
62	CL	I	External clock input. It must be fixed to “H” or “L” when the internal oscillation circuit is used. In case of the external clock mode, CL is used as the clock and OS bit should be OFF.
66	PI	I	Interface data length selection pin for parallel data input PI = “L”: 4-bit data input mode. PI = “H”: 8-bit data input mode.
68	C86	I	This is the MPU interface switch terminal. C86 = “L”: 8080 Series MPU interface. C86 = “H”: 6800 Series MPU interface.
64	P/S	I	This is the parallel data input/serial data input switch terminal. P/S = “L”: Serial data input. P/S = “H”: Parallel 4-bit / 8-bit data input. When P/S = “L”, D0 to D5 are HZ. D0 to D5 may be “H”, “L” or Open. /RD (E) and /WR (R/W) are fixed to either “H” or “L”. With serial data input, RAM display data reading is not supported.
60	DIRS	I	SEG direction selection input DIRS = “L”: SEG1-> SEG2->·····-> SEG79-> SEG80 DIRS = “H”: SEG80-> SEG79->·····-> SEG2-> SEG1
6	/CS	I	This is the chip select signal. When /CS = “L”, then the chip select becomes active, and data/instruction I/O is enabled
70	/RES	I	When /RES is set to “L”, the settings are initialized. The reset operation is performed by the /RES signal level.
5	/RD (E)	I	When connected to an 8080 Series MPU, it is low active. This pad is connected to the /RD signal of the 8080 MPU, and the NT7606 data bus is in an output status when this signal is “L”. When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
3	/WR (R/W)	I	When connected to an 8080 Series MPU, this is low active. This terminal connects to the 8080 Series MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. R/W = “L”: Write. R/W = “H”: Read.

System Bus Connection Pads (continue)

1	RS	I	Register selects signal input. RS = “L”: selects the instruction register RS = “H”: selects the data register
11 – 14 9 – 10 8 7	D0 – D3 D4 – D5 D6 (SCL) D7 (SI)	I/O	When 8-bit bus mode (P/S = “H” and PI = “H”), D0 – D7 are used as bi-directional data bus that connects to an 8-bit MPU data bus. When 4-bit bus mode (P/S = “H” and PI = “L”), D4 – D7 are used as bi-directional data bus that connects to a 4bit MPU data bus. And in this case D0 – D3 pins are not used and set to HZ. When the serial interface is selected (P/S = “L”), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to HZ. When the chip select is inactive, D0 to D7 are set to HZ.

System Bus Connection

Pad No.	Designation	I/O	Description
99 – 178	SEG1 – 80	O	Segment signal output for LCD display
82 – 89, 184 – 191, 90 – 93, 180 – 183	COM1 –24	O	Common signal output for LCD display.
81, 179	COMS1, COMS2	O	Common signal output for icon display COMS1 and COMS2 are the same signal, but name is different.

Test Pads

Pad No.	Designation	I/O	Description
71, 73	TEST0, TEST2	I	Test pads, no connection for user.
72	TEST1	I	Test pad, must connected to VDD.
94 – 98	TESTD0 – 4	O	Test data output, no connection for user.

No Connected Pads

Pad No.	Designation	I/O	Description
74 – 79	NC	I	No connection.

Functional Descriptions

Microprocessor Interface

NT7606 has two kinds of interface type with MPU: parallel mode, serial mode. Parallel or serial mode is selected by P/S pad. In parallel mode, 4-bit data bus or 8-bit data bus is selected by PI pad, and 6800 or 8080 MPU mode is selected by C86 pad.

Interface type selection

The NT7606 can transfer data via 4-bit bi-directional data bus (D7 to D4) / 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI).
When high or low is selected for the parity of P/S pad, either 4-bit/ 8-bit parallel data input or serial data input can be selected. When serial data input is selected, the RAM data cannot be read out.

Table 1. Parallel or Serial MPU Interface according to P/S

P/S	Type	/CS	RS	/RD (E)	/WR (R/W)	C86	PI	D7	D6	D5, D4	D0 to D3
H	Parallel Input	/CS	RS	/RD (E)	/WR (R/W)	C86	H (8-bit)	D7	D6	D5, D4	D0 to D3
							L (4-bit)	D7	D6	D5, D4	(HZ)
L	Serial Input	/CS	RS	-	-	-	-	SI	SCL	(HZ)	

Note: “-“ must always be fixed “H” or “L”.

Parallel Input (P/S is high)

When the NT7606 selects parallel input (P/S = high), the 4-bit or 8-bit parallel input mode can be selected by causing the PI pad to go high or low.

When the NT7606 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low.
The NT7606 identifies the data bus signal according to RS, /RD (E) and /WR (R/W) signals.

Table 2. Various Kinds of Parallel MPU interface according to PI and C86

PI	C86	Type	/CS	RS	/RD (E)	/WR (R/W)	D0 to D3	D4 to D7
H	H	8-bit 6800 MCU bus	/CS	RS	E	R/W	D0 to D7	
L		4-bit 6800 MCU bus	/CS	RS	E	R/W	(HZ)	D4 to D7
H	L	8-bit 8080 MCU bus	/CS	RS	/RD	/WR	D0 to D7	
L		4-bit 8080 MCU bus	/CS	RS	/RD	/WR	(HZ)	D4 to D7

Serial Interface (P/S is low)

When the serial interface has been selected (P/S = “L”) then when the chip is in active state (/CS = “L”) the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order.
At the rising edge fo the 8the serial clock, the serial data (D7 – D0) is converted into 8 bit bus mode data. The RS input of the DR/IR selection is latched in the rising edge of eighth serial clock (SCL) for the processing.
Figure 1 is serial interface signal diagram.

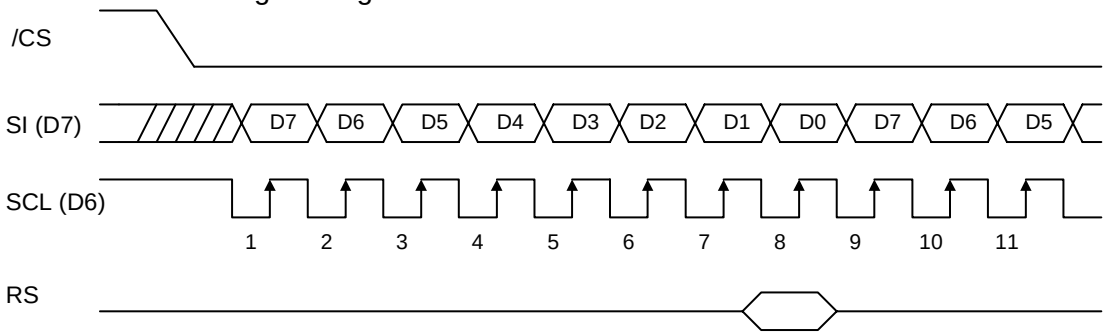


Figure 1. Diagram of Serial Data Transfer

Chip Select Inputs

The NT7606 has one chip select pads. /CS can interface to a microprocessor when /CS is low . When this pads are set to high, D0 to D7 are high impedance and RS, /RD (E), /WR (R/W) inputs are disabled.

Registers

The NT7606 has three 8-bit registers, an Instruction Register (IR), and Data Register (DR) and an output data register (OR).

During writing operation, the Register Select signal (RS) determines which register will be accessed. The instruction register stores instruction codes and address information for the Display Data RAM (DDRAM), Character Generator RAM (CGRAM) and Segment Icon RAM (ICONRAM).

During reading operation, output data register (OR) is used. The output data register temporarily stores data to be read from the DDRAM, CGRAM and ICONRAM and one of these RAM are selected by RAM address setting instruction. After RAM address setting, first reading is a dummy cycle in 8-bit bus mode. The valid data comes from second reading. In 4-bit bus mode, after RAM address setting, first and second reading is dummy cycles. The valid data comes from third reading. The dummy read make the address counter (AC) increased by 1.So it is recommended to set address again before writing, The instruction read cycle is not supported and it is regarded as a no operation cycle.

In 4-bit bus mode, it is needed to transfer 4-bit data (through D7~ D4) by two times .The high order bits (for 8-bit mode D7~D4) are written before the low order bits (for 8-bit mode D3~D0) in write and low order bits (for 8-bit mode D3~D0) are read before the high order bits (8-bit mode D3~D0) in read transaction. The D0~D3 pins are floated in this 4-bits bus mode. After /RES resets, NT7606 considers first 4-bit data from MPU as high order bits.

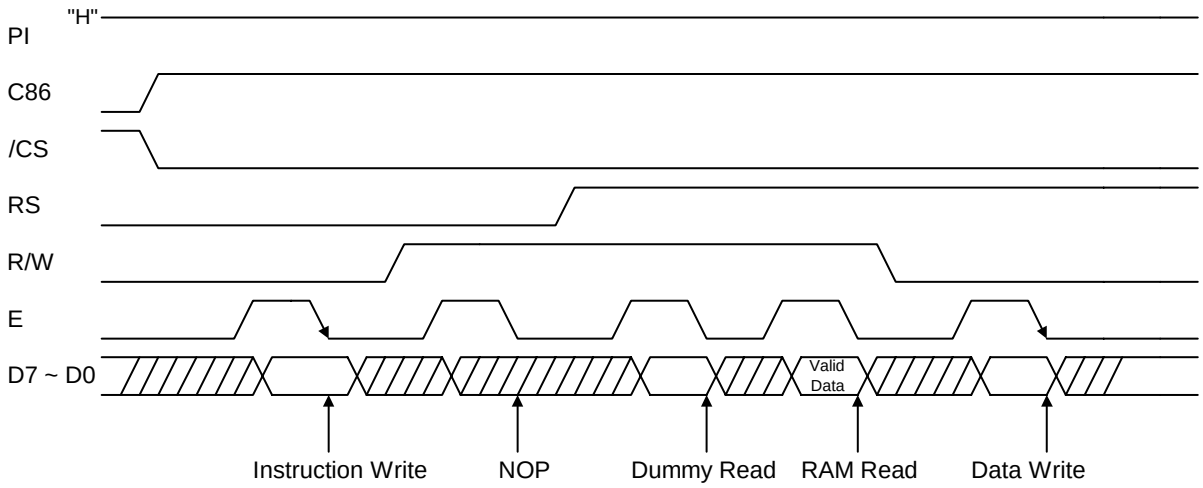


Figure 2. Diagram of 8-bit Parallel Bus Mode Data Transfer (6800 MPU Mode)

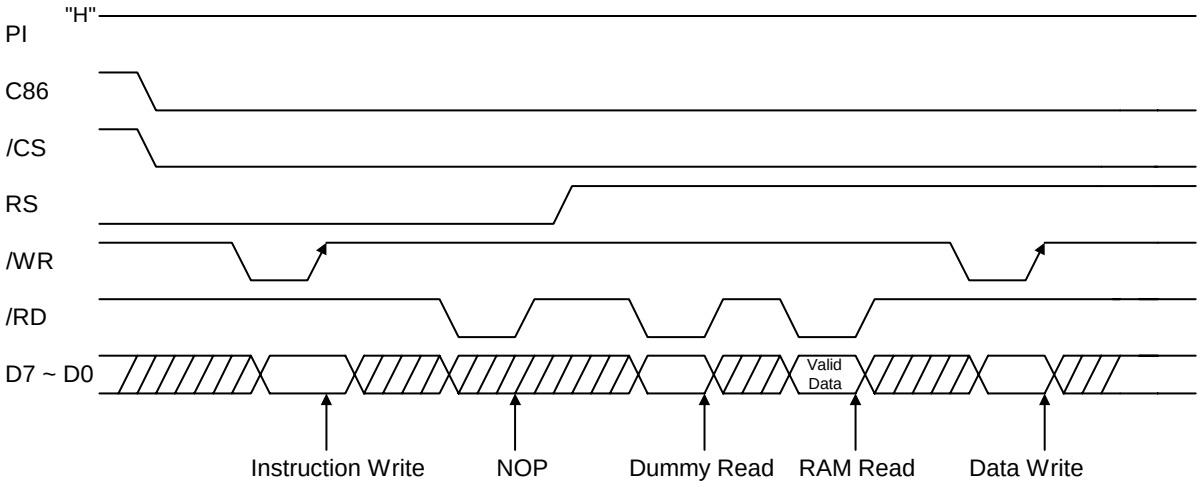


Figure 3. Diagram of 8-bit Parallel Bus Mode Data Transfer (8080 MPU Mode)

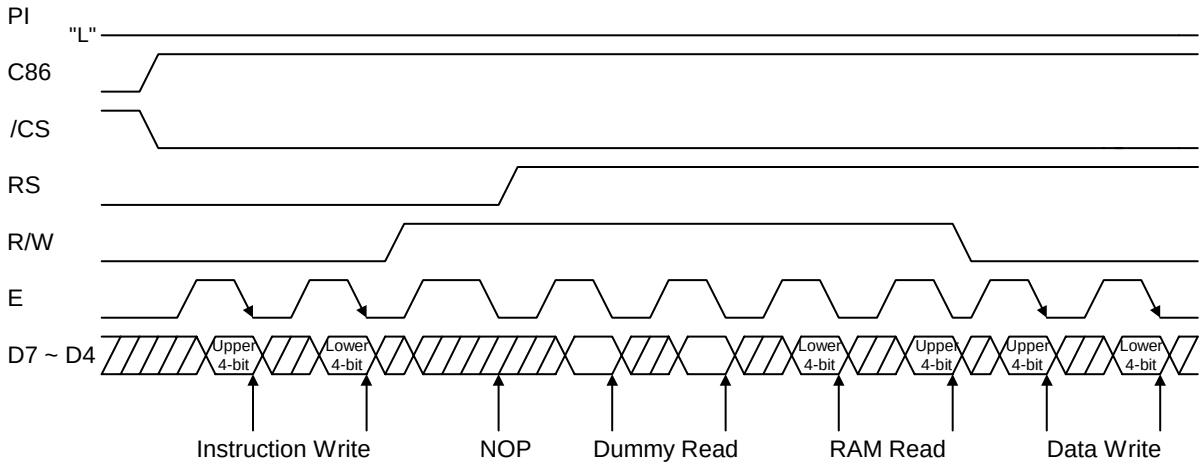


Figure 4. Diagram of 4-bit Parallel Bus Mode Data Transfer (6800 MPU Mode)

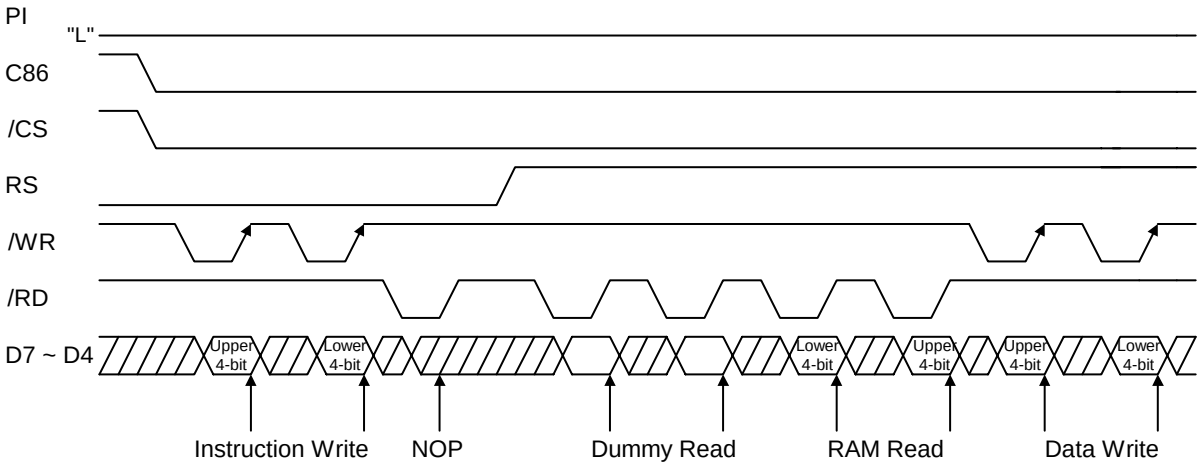


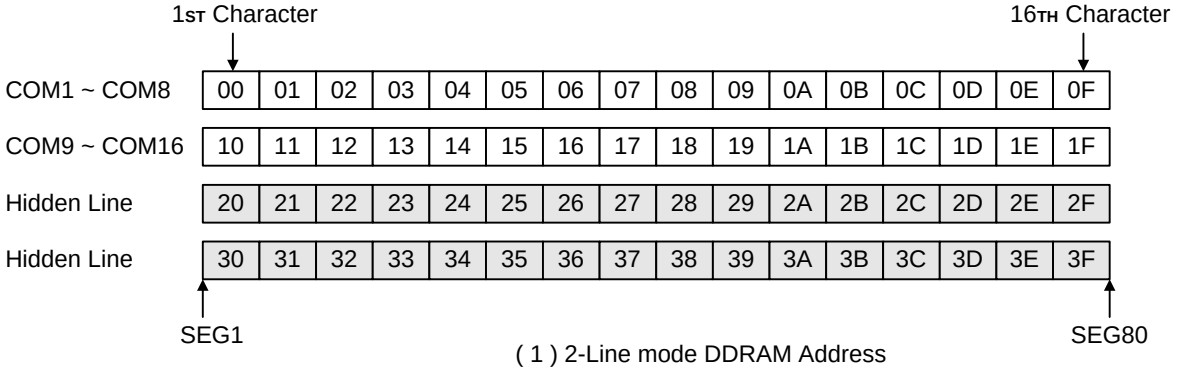
Figure 5. Diagram of 4-bit Parallel Bus Mode Data Transfer (8080 MPU Mode)

Address Counter (AC)

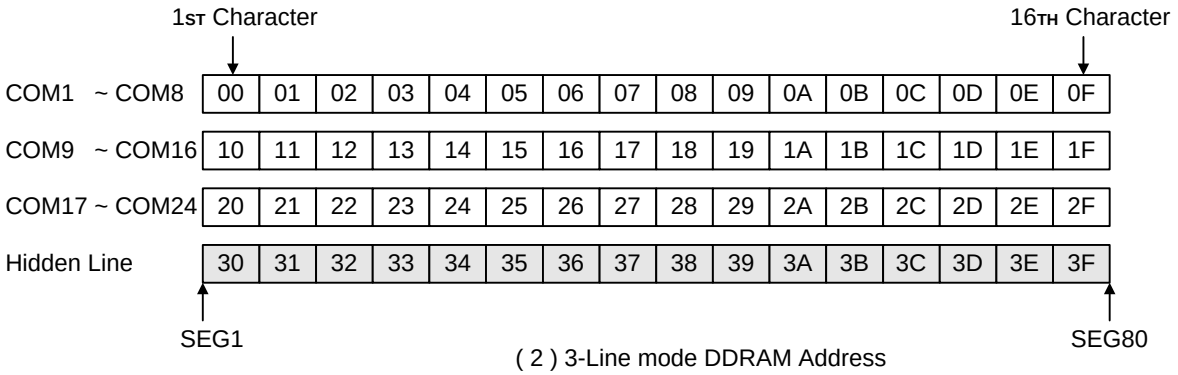
The address counter assigns addresses to the DDRAM CGRAM and ICONRAM for reading and writing and is set by the instructions ‘CGRAM address set’, ‘DDRAM address set’ and ‘ICONRAM address set’. After a read/write operation, the address counter is automatically incremented by 1. The address counter content are only one and stores the address among DDRAM / CGRAM / ICONRAM.

Display Data RAM (DDRAM)

The DDRAM stores up to 64 characters of display data represented by 8-bit character codes. DDRAM address is set in the address counter (AC) as a hexadecimal number.



(1) 2-Line mode DDRAM Address



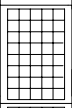
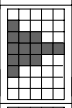
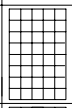
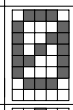
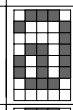
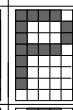
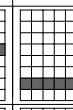
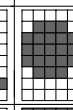
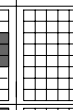
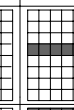
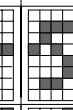
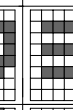
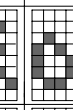
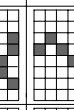
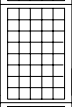
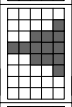
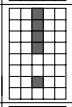
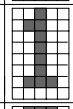
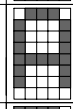
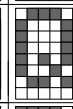
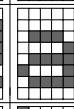
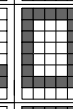
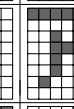
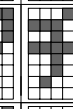
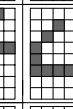
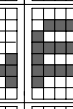
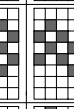
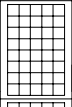
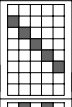
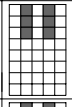
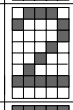
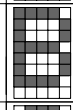
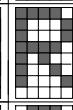
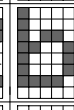
(2) 3-Line mode DDRAM Address

Figure 6. DDRAM Address

Character Generator ROM (CGROM)

The Character Generator ROM generates 256 character patterns in a 5 × 8-dot format from 8-bit character codes. The CG bit of the instruction table selects the 8 characters (00H ~ 07H) of CGROM or CGRAM. Table 3 shows the character set that is currently implemented.
User can define self-CGROM through changing MASK ROM.

Table 3. Character Standard Code in CGROM

High 4-bit / Low 4-bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000																
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

Character Generator RAM (CGRAM)

CGRAM has up to 5 × 8 dot 8 characters. By writing font data to CGRAM, use defined character can be used. CGRAM can be written regardless of CG bit.

Table 4. Relationship between CGRAM addresses data and display patterns

Character codes (DDRAM data)								DD / CGRAM address							CGRAM data (example)										Pattern No.
Higher			Order bits		Lower			Higher			Order bits		Lower		Character patterns					Character code					
D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	A0	4	3	2	1	0	4	3	2	1	0	
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0						0	1	0	1	0	Pattern 0
												0	0	1						1	0	1	0	1	
												0	1	0						0	1	0	1	0	
			(00H)									0	1	1						1	0	1	0	1	
												1	0	0						0	1	0	1	0	
												1	0	1						1	0	1	0	1	
												1	1	0						0	1	0	1	0	
												1	1	1						1	0	1	0	1	
0	0	0	0	0	0	0	1	1	0	0	1	0	0	0						0	0	0	0	0	Pattern 1
												0	0	1						1	1	1	1	1	
												0	1	0						0	0	0	0	0	
			(01H)									0	1	1						1	1	1	1	1	
												1	0	0						0	0	0	0	0	
												1	0	1						1	1	1	1	1	
												1	1	0						0	0	0	0	0	
												1	1	1						1	1	1	1	1	
0	0	0	0	0	0	1	0	1	0	1	0	0	0	0						0	1	0	1	0	Pattern 2
												0	0	1						0	1	0	1	0	
												0	1	0						0	1	0	1	0	
			(02H)									0	1	1						0	1	0	1	0	
												1	0	0						0	1	0	1	0	
												1	0	1						0	1	0	1	0	
												1	1	0						0	1	0	1	0	
												1	1	1						0	1	0	1	0	
0	0	0	0	0	0	1	1	1	0	1	1	0	0	0						0	1	1	1	0	Pattern 3
												0	0	1						1	0	1	0	1	
												0	1	0						1	1	0	1	1	
			(03H)									0	1	1						1	0	1	0	1	
												1	0	0						0	1	1	1	0	
												1	0	1						1	1	1	1	1	
												1	1	0						1	1	1	1	1	
												1	1	1						1	1	1	1	1	
0	0	0	0	0	1	0	0	1	1	0	0	0	0	0						1	1	0	1	1	Pattern 4
												0	0	1						1	0	0	0	1	
												0	1	0						0	0	0	0	0	
			(04H)									0	1	1						1	0	0	0	1	
												1	0	0						1	1	0	1	1	
												1	0	1						1	1	1	1	1	
												1	1	0						1	1	1	1	1	
												1	1	1						1	1	1	1	1	
0	0	0	0	0	1	0	1	1	1	0	1	0	0	0						1	1	1	1	1	Pattern 5
												0	0	1						1	1	1	1	1	
												0	1	0						0	0	0	0	0	
			(05H)									0	1	1						0	0	0	0	0	
												1	0	0						1	1	1	1	1	
												1	0	1						1	1	1	1	1	
												1	1	0						0	0	0	0	0	
												1	1	1						0	0	0	0	0	

Table 4. Relationship between CGRAM addresses data and display patterns (Continued)

Character codes (DDRAM data)								DD / CGRAM address							CGRAM data (example)										Pattern No.
Higher			Order bits		Lower			Higher			Order bits		Lower		Character patterns					Character code						
D7	D6	D5	D4	D3	D2	D1	D0	A6	A5	A4	A3	A2	A1	A0	4	3	2	1	0	4	3	2	1	0	
0	0	0	0	0	1	1	0	1	1	1	0	0	0	0						0	0	1	1	0	Pattern 6
			(06H)									0	0	1						0	0	1	1	0	
												0	1	0						0	0	1	1	0	
												0	1	1						0	0	1	1	0	
												1	0	0						0	0	1	1	0	
												1	0	1						0	0	1	1	0	
												1	1	0						0	0	1	1	0	
												1	1	1						0	0	1	1	0	
0	0	0	0	0	1	1	1	1	1	1	1	0	0	0						0	0	0	0	0	Pattern 7
			(07H)									0	0	1						1	0	0	0	1	
												0	1	0						1	1	0	1	1	
												0	1	1						1	0	0	0	1	
												1	0	0						0	0	0	0	0	
												1	0	1						1	0	0	0	1	
												1	1	0						1	1	0	1	1	
												1	1	1						1	1	1	1	1	

Segment ICON RAM (ICONRAM)

The ICONRAM has segment control data and segment pattern data. COMS1 and COMS2 are the same signals, but the name is different. The number of icons is 80.

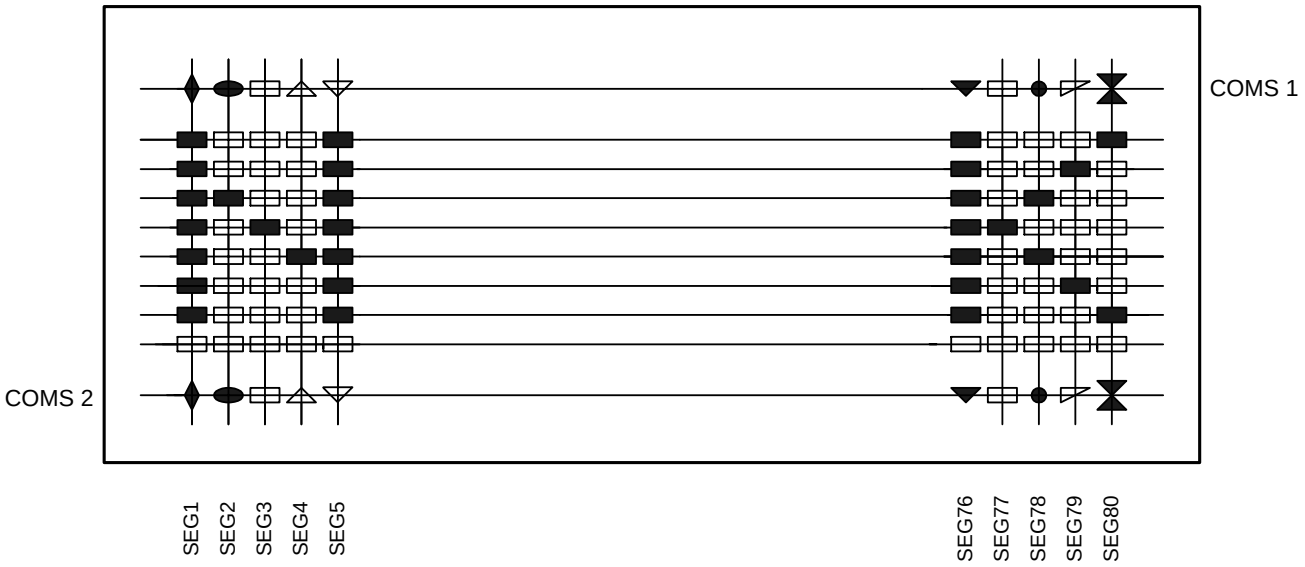


Figure 7. Relationship between ICONRAM and Icon Display

Table 5. Relationship between ICONRAM addresses data and display patterns

ICONRAM address	ICONRAM Bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	-	-	S1	S2	S3	S4	S5
01H	-	-	-	S6	S7	S8	S9	S10
.	.	.	.	.	.	.	.	.
0EH	-	-	-	S71	S72	S73	S74	S75
0FH	-	-	-	S76	S77	S78	S79	S80

Note: "-" Don't care.

Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the CL pad must be connected to "H" or "L" when the internal oscillation circuit is used. In case of the external clock mode, CL is used as the clock and OS bit should be OFF.

Frame frequency

- 1/17 Duty (2-line mode)

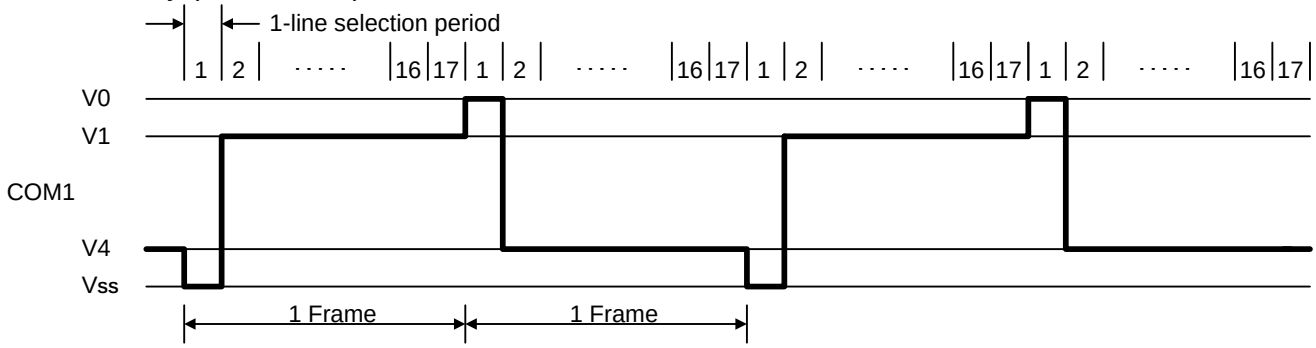


Figure 8. 2-Line Mode Frame Frequency

1-line Selection Period = 16 clocks
One Frame = 16 × 17 × 46.0 μs = 12.5 ms (1 Clock = 46.0μs at Fosc = 21.76 KHz)
Frame Frequency = 1/12.5 ms = 80 Hz

- 1/25 Duty (3-line mode)

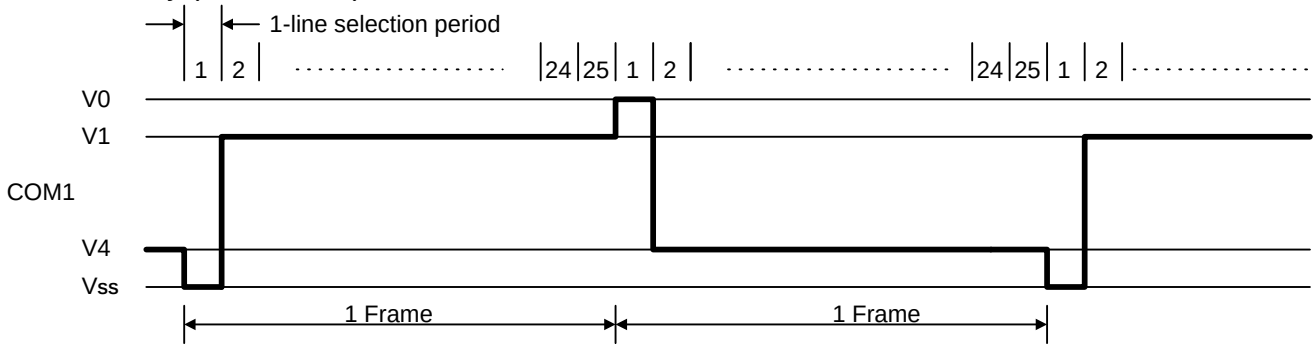


Figure 9. 3-Line Mode Frame Frequency

1-line Selection Period = 16 clocks
One Frame = 16 × 25× 31.25 μs = 12.5 ms (1 Clock = 31.25μs at Fosc = 32 KHz)
Frame Frequency = 1/12.5 ms = 80 Hz

Sleep mode (Power Save Bit ON, Oscillation Bit OFF)

NT7606 provides with sleep mode for saving power consumption during standby period.
To enter the sleep mode, the power circuit and oscillation circuit should be turned off by using the power save instruction and the power control instruction. This mode helps to save power consumption by reducing current to reset level.

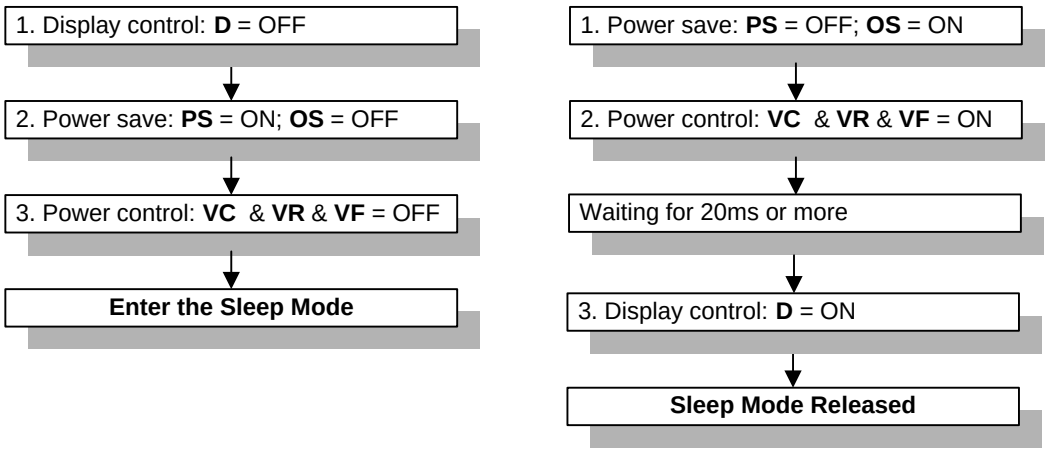


Figure 10. Sleep Mode Set or Release by Instructions

1. Liquid Crystal Display Output
   COM1 ~ COM24, COMS1, COMS2: VSS level. SEG1 ~ SEG80: VSS level
2. Data written in DDRAM, CGRAM, ICONRAM and registers are remained as previous value.
3. Operation mode is retained the same as it was prior to execution of the sleep mode.
   All internal circuits are stopped.
4. Power Circuit and Oscillation Circuit.
   The build-in power supply circuit and oscillation circuit are turned off by power save instruction and power control instruction.

LCD common and segment drivers

The NT7606 contains 26 common and 80 segment drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. COMS1 and COMS2 drive the icon common. The bias voltages and the timing are selected automatically when the number of lines in the display is selected.

Table 6. SEG Data Shift Direction

DIRS pad	SEG data shift direction
L	SEG1 -> SEG2 -> SEG3 ->·····-> SEG78 -> SEG79 -> SEG80
H	SEG80 -> SEG79 -> SEG78 ->·····-> SEG3 -> SEG2 -> SEG1

Table 7. COM Data Shift Direction

Line mode	S	COM data shift direction
2-Line mode	0 (left)	COM1 -> COM2 ->····· -> COM16 -> COMS1 (COMS2)
	1 (right)	COMS1 (COMS2) -> COM16 ->····· -> COM2 -> COM1
3-Line mode	0 (left)	COM1 -> COM2 ->····· -> COM24 -> COMS1 (COMS2)
	1 (right)	COMS1 (COMS2) -> COM24 ->····· -> COM2 -> COM1

LCD supply voltage generator

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise DC-DC converter circuits, voltage regulator circuits, and voltage follower circuits. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set instruction. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 8 shows the Power Control Set Instruction 3-bit data control function, and Table 9 shows reference combinations.

Table 8. The Control Details of Each Bit of the Power Control Set Instruction

Item	Status	
	"1"	"0"
VC: DC-DC converter (V/C) circuit control bit	ON	OFF
VR: Voltage regulator circuit (V/R) control bit	ON	OFF
VF: Voltage follower circuit (V/F) control bit	ON	OFF

Table 9. LCD Power Supply Combinations

Use Settings	VC	VR	VF	Step-up circuit	Voltage regulator circuit	V/F circuit	VOUT pin	VR pin	V0 ~ V4 pin
Only the internal power supply is used	1	1	1	ON	ON	ON	Internal voltage input	Used for voltage adjustment	Internal voltage output
Only the V regulator circuit and the V/F circuit are used	0	1	1	OFF	ON	ON	External voltage input	Used for voltage adjustment	Internal voltage output
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	Open	Open	V0: external voltage input V1~V4: Internal voltage output
Only the external power supply is used	0	0	0	OFF	OFF	OFF	Open	Open	V0~V4: Internal voltage output

*The “step-up system terminals” refer CAP1+, CAP1-, CAP2+ and CAP2-.

*While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Voltage DC-DC Converter Circuits

Using the step-up voltage circuits equipped within the NT7606 chips it is possible to product 2X, 3X Step-up of the VDD - VSS voltage levels. V_{OUT} is generated from the voltage converter. And this conversion voltage is used in the build-in Voltage Regulator circuit. Figure 11 shows the application circuit of 2-time and 3-time DC-DC converter.

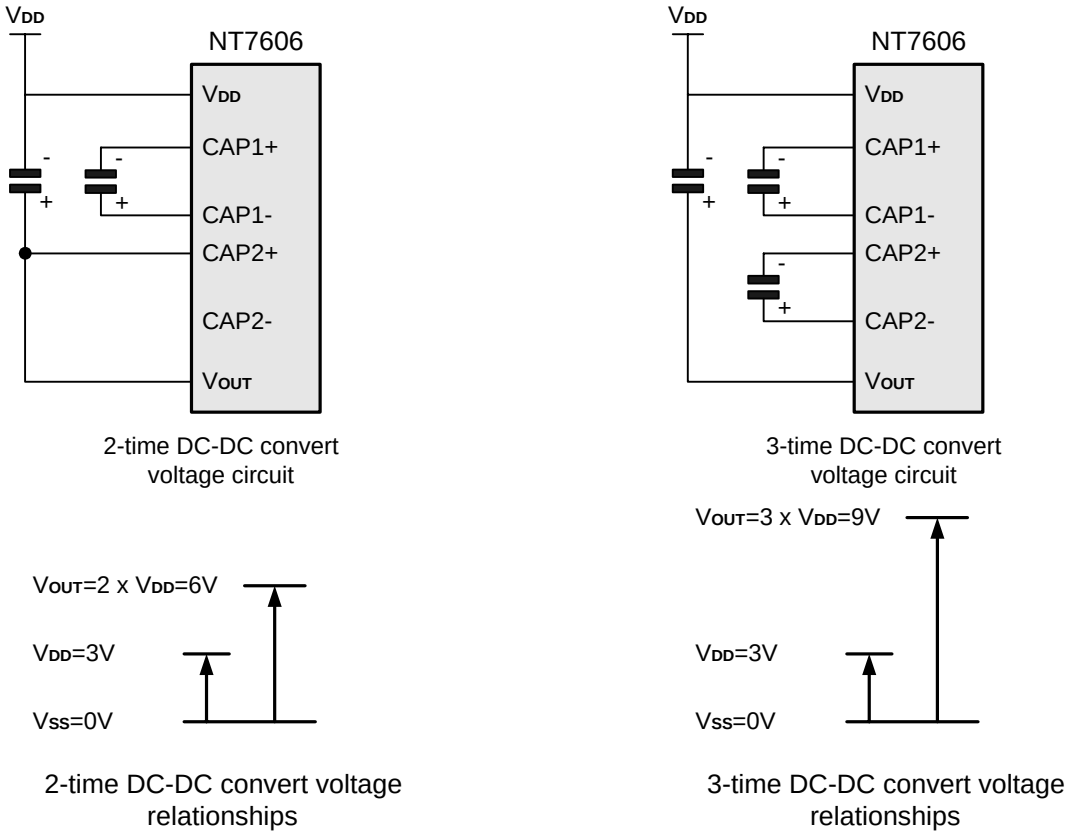


Figure 11. Voltage DC-DC Converter Circuit and Output

The Voltage regulator circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V0 through the voltage regulator circuit. Because the NT7606 chips have an internal high-accuracy fixed voltage power supply with a 32-level electronic volume function and external resistors for the V0 voltage regulator. Moreover, in the NT7606, two types of selections have been prepared as VREF options:

(1) When VRS is "L": internal VREF (2 V).The internal VREF of voltage regulator has the temperature compensation function, and the temperature coefficient is about 0.0%/℃.

(2) When VRS is "H", VREF external input (supplied to the VEXT terminal).

Using External Resistors to Adjust V0 Voltage Regulator

Through the use of the V0 voltage regulator external resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled (with adding two external resistors: Ra and Rb), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where V0 < VOUT.

$V0 = (1+Rb/Ra)*V_{EV} = (1+Rb/Ra)* (1-\alpha/150)*VREF$ (Equation A-1)

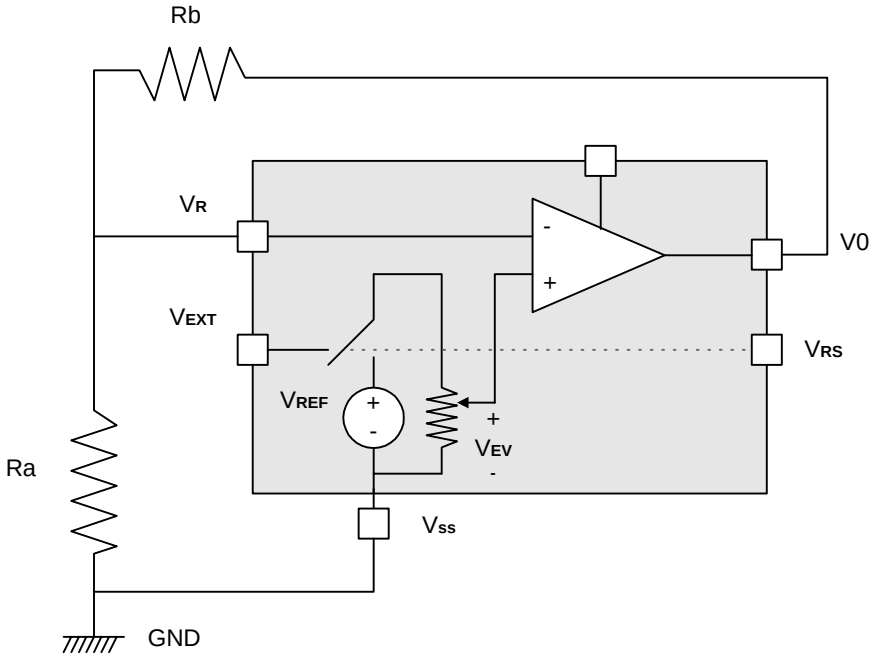


Figure 12. Voltage Regulator and Electronic Contrast Control Circuit

VREF is the IC internal fixed voltage supply, and its voltage at Ta = 25℃ is as shown in Table 10.

Table 10. Voltage VREF Selection

Equipment Type	VRS	Thermal Gradient	Units	VREF
Internal power Supply	0	-0.0	%/℃	2.0
External input	1	-	-	VEXT

α is set to 1 level of 32 possible levels by the electronic volume function depending on the data set in the 5-bit electronic volume register. Table 11 shows the value for α depending on the electronic volume register settings

Table 11. Electronic Contrast Control

C7	C6	C5	C4	C3	C2	C1	C0	α	V0	Contrast
-	-	-	0	0	0	0	0	0 (default)	Maximum	High
-	-	-	0	0	0	0	1	1	:	:
-	-	-	0	0	0	1	0	2	:	:
				:			:	:	:	:
				:			:	:	:	:
-	-	-	1	1	1	1	0	30	:	:
-	-	-	1	1	1	1	1	31	Minimum	Low

Note: "-" Don't care.

The V0 voltage as a function of the V0 voltage regulator external resistor ratio register and the electronic volume register.
Setup example: When selecting Ta = 25℃ and V0 = 5V for an NT7606 model on which internal VREF is used. The equation A-1, the following setup is enabled.

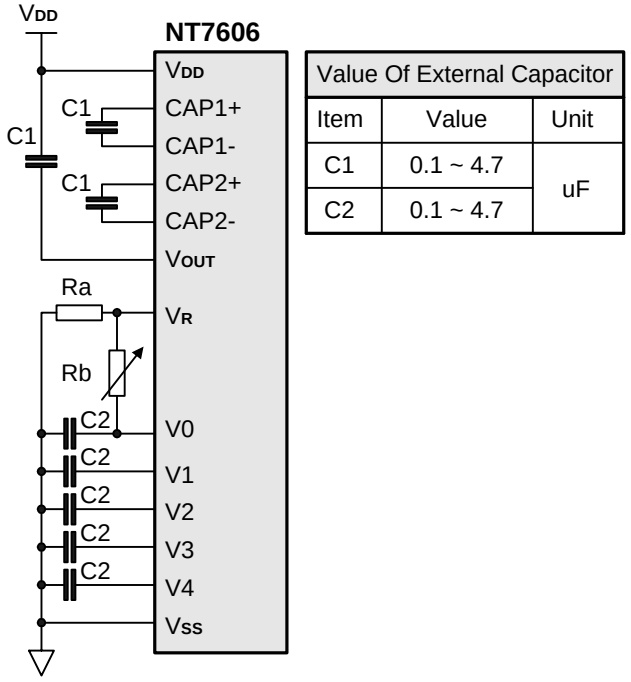
Table 12. Example of V0 Voltage Adjust

Contents	Adjust							
External Rb/Ra resistor is adjusted	Rb/Ra = 1.5							
Electronic Volume	D7	D6	D5	D4	D3	D2	D1	D0
	-	-	-	0	0	0	0	0

The Liquid Crystal Voltage Generator circuit (Volatage Follower & Bias)

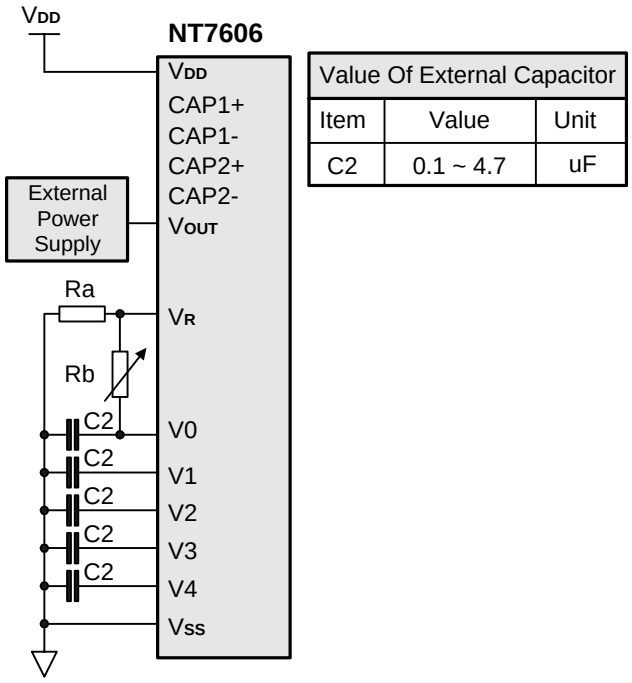
The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3, and V4 to the liquid crystal drive circuit. 1/4 bias or 1/5 bias for NT7606 can be selected by instruction.

Reference power supply circuit for driving LCD panel



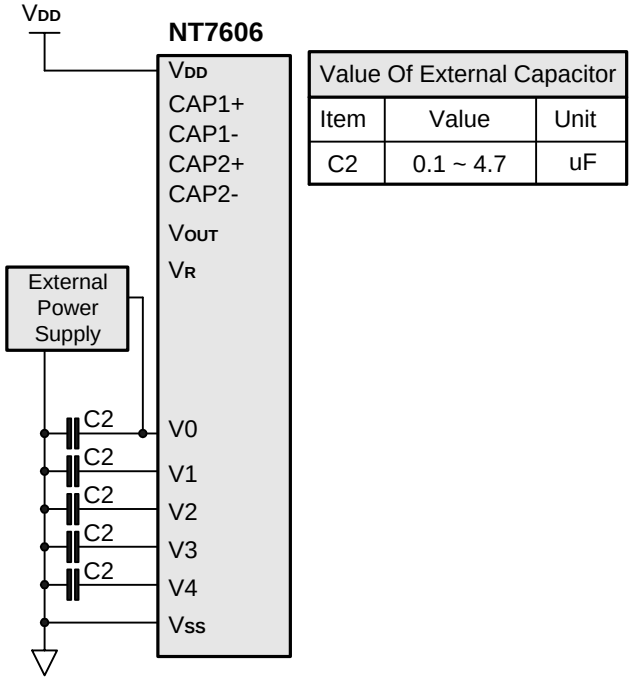
Value Of External Capacitor		
Item	Value	Unit
C1	0.1 ~ 4.7	uF
C2	0.1 ~ 4.7	

Figure 13. When using all LCD power circuits (VC, VR, VF = 1, 1, 1)



Value Of External Capacitor		
Item	Value	Unit
C2	0.1 ~ 4.7	uF

Figure 14. When not using voltage booster circuits (VC, VR, VF = 0, 1, 1)



Value Of External Capacitor		
Item	Value	Unit
C2	0.1 ~ 4.7	uF

Figure 15. When only using voltage follower (VC, VR, VF = 0, 0, 1)

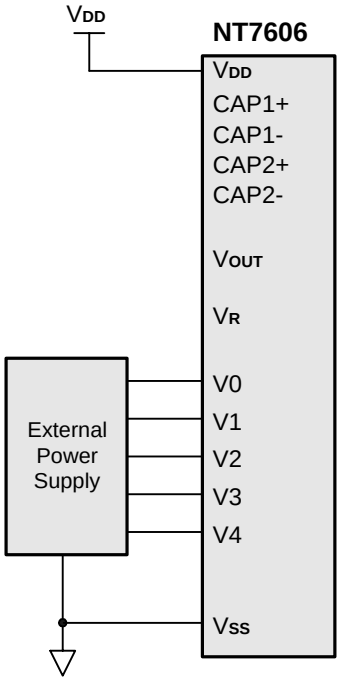


Figure 16. When not using internal LCD power supply circuits (VC, VR, VF = 0, 0, 0)

Power-on reset and Initial State

The NT7606 must be reset externally by /RES pin when power is turned on. The external reset is low active. After the reset the chip has the state shown in Table 13.

Table 13. State after reset

Function	Control bit state	Remarks
Display control set	D = 0	Display off
	C = 0	Cursor off
	B = 0	Cursor character blink off
Power save set	OS = 0	Oscillator off
	PS = 0	Power save off
Power control set	VC = 0	Voltage DC-DC converter OFF
	VR = 0	Voltage regulator OFF
	VF = 0	Voltage follower OFF
Function set	N = 0	2-line display
	S = 0	COM left shift
	CG = 0	CGRAM is not used. CGROM is used.
Return home		Address counter (AC) = 00H
Electronic contrast control register		10H = (0,0,0,0,0)
In case of 4-bit mode		NT7606 considers the first 4-bit data from MPU as the high order bits.

Note: If initialization is not done by /RES pin at application, unknown condition might result.

INSTRUCTIONS

Only the Instruction Register (IR), the Data Register (DR) and output Data Register (OR) can be directly controlled by the MPU. Before internal operation, control information is stored temporarily in these registers, to allow interfacing to various types of MPU that operates at different speeds or to allow interface to peripheral control ICs.

Instruction set

1. Return home

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	0	0	1	-	02h to 03h

Return home instruction field makes cursor return home.
DDRAM address is set to 00H from AC and the cursor returns to 00H position. The contents of DDRAM are not changed

2. Double height mode

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	1	0	DH2	DH1	08h to 0Bh

Double height mode instruction field selects double height line type.
When DH2 DH1 = 00: normal display (default)
01: COM1 ~ COM16 is a double height, COM17 ~ COM24 is normal
10:1) 2-line mode: normal display
2) 3-line mode: COM1 ~ COM8 is normal, COM9 ~ COM24 is a double height.
11: normal display

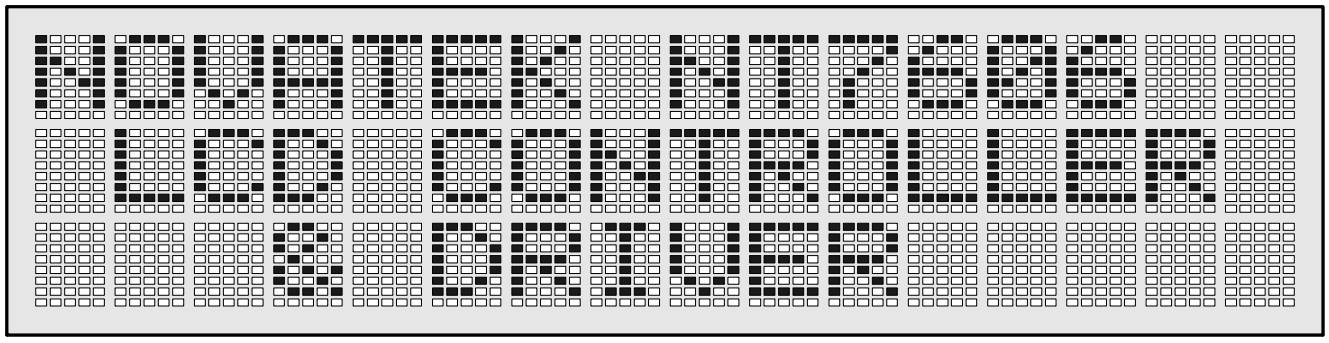


Figure 17. 3-Line Normal Mode Display (DH2, DH1 = 00)

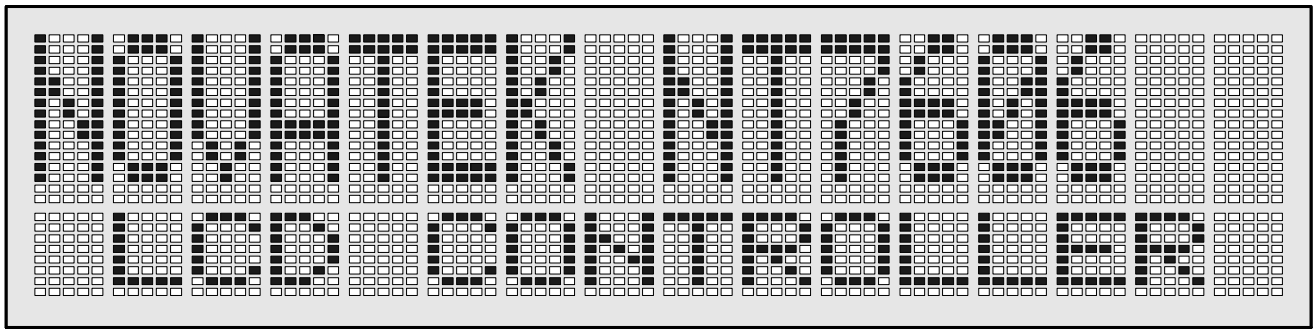


Figure 18. COM1 ~ COM16 is a Double Height Line, COM17 ~ COM24 is Normal (DH2, DH1 = 01)

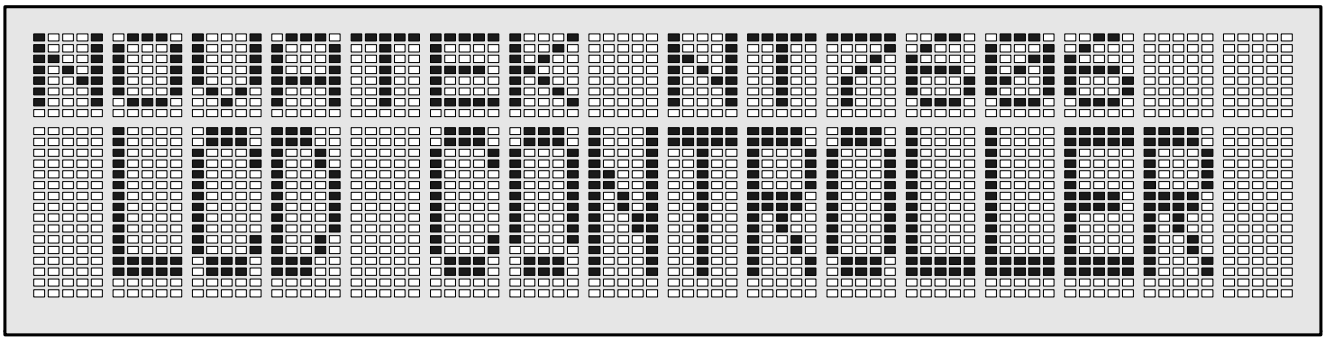


Figure 19. COM1 ~ COM8 is Normal, COM9 ~ COM24 is a Double Height Line (DH2, DH1 = 10)

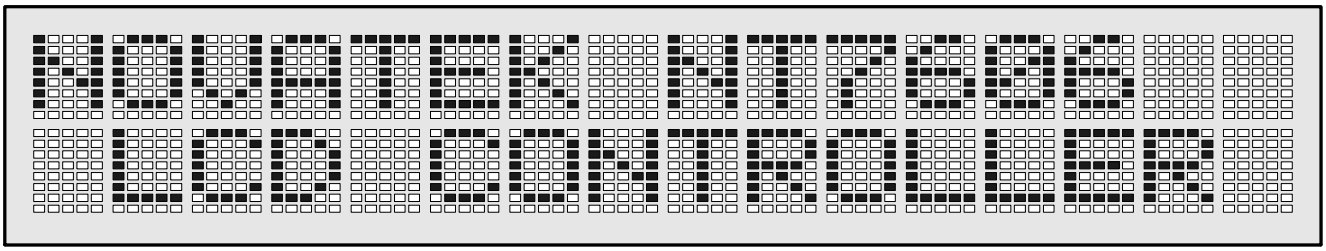


Figure 20. 2-Line Normal Mode Display (DH2, DH1 = 00)

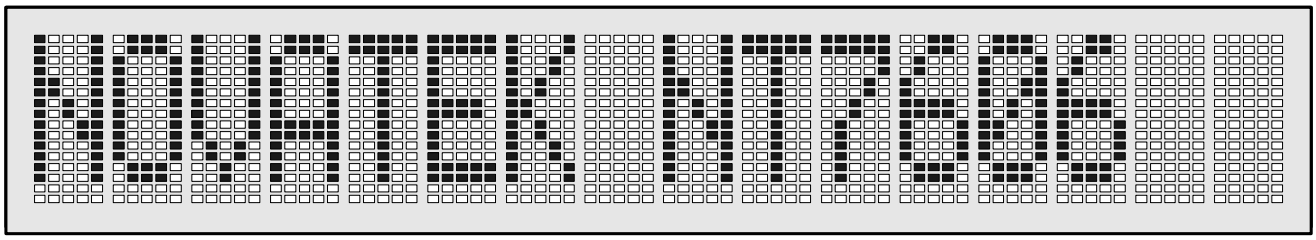


Figure 21. COM1 ~ COM16 is a Double Height Line (DH2, DH1 = 01)

3. Power save set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	1	1	OS	PS	0Ch to 0Fh

Power save instruction field is used to control the oscillator and set or to reset the power save mode.

OS: oscillator ON/OFF control bit

When OS = “L”, oscillator is turned OFF (default)

When OS = “H”, oscillator is turned ON.

PS: power save ON/OFF control bit

When PS = “L”: power save is turned OFF (default).

When PS = “H”: power save is turned ON.

4. Function Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	1	0	N	S	CG	10h to 17h

N: display line mode instruction field selects 2-line or 3-line display mode
When N = “L”: 2-line display mode (default)
When N = “H”: 3-line display mode
S: data shift direction of common, S sets the shift direction of common display data
When S = “L”, COM left shift (default)
When S = “H”, COM right shift (Refer to Table 7)
CG: CGRAM enable bit
When CG = “L”, CGRAM is disable. CGROM (00H~07H) can be accessed and additional current consumption is saved by using this mode (default). (00H~07H = CGROM font display)
When CG = “H”, CGRAM can be accessed and you can use this RAM for eight special character area. (00H~07H = CGRAM font display)

5. Line shift mode

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	1	1	0	LS2	LS1	18h to 1Bh

Line shift mode instruction field selects the DDRAM to be displayed in the first line.
When LS2, LS1 = 00: DDRAM line 1 shows at the first line of LCD (default).
01: DDRAM line 2 shows at the first line of LCD.
10: DDRAM line 3 shows at the first line of LCD.
11: DDRAM line 4 shows at the first line of LCD.

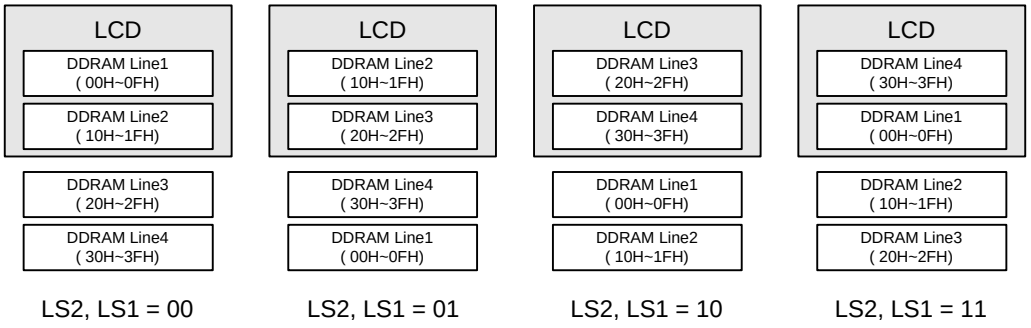


Figure 22. 2-Line Shift Mode Display at 2 Line LCD

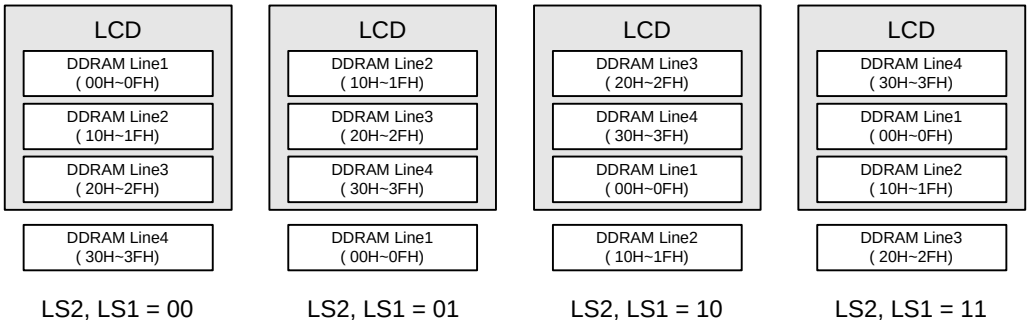


Figure 23. 3-Line Shift Mode Display at 3 Line LCD

6. Line shift mode

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	1	1	1	-	BS	1Ch to 1Fh

Bias Control instruction field sets LCD bias voltages generated internally.
BS: The bit is used when the internal voltage follower is ON
When BS = “L”: 1/5 bias (default)
When BS = “H”: 1/4 bias (V2 = V3)

7. Power Control Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	1	0	0	VC	VR	VF	20h to 27h

Power Control instruction field sets voltage converter / regulator / follower ON / OFF.

VC: voltage converter circuit control bit
When VC = “L”: voltage booster is turned OFF (default)
When VC = “H”: voltage booster is turned ON

VR: voltage regulator circuit control bit
When VR = “L”: voltage regulator is turned OFF (default)
When VR = “H”: voltage regulator is turned ON

VF: voltage follower circuit control bit
When VF = “L”: voltage follower is turned OFF (default)
When VF = “H”: voltage follower ON

Note: The oscillation circuit must be turned on for the voltage converter circuit to be active.

8. Display control

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	1	0	1	C	B	D	28h to 2Fh

Display control instruction field controls cursor /blink/display ON/OFF.

C: cursor ON /OFF control bit
When C = “L”, cursor is disappeared in current display (default).
When C = “H”, cursor is turned ON.

B: cursor blink ON/OFF control bit
When C = “H” and B = “H”, NT7606 make LCD alternate between inverting display character and normal display character at the cursor position with about a half second.
On the contrary, if C = “L”, only a normal character is displayed regardless of “B” flag.
When B = “L”, blink is OFF (default).

D: display ON/OFF control bit
When D = “L”, Display is turned OFF. But display data are remained in DDRAM (default).
When D = “H”, Entire display in turned ON.

Table 14. Cursor Attributes

C	B	Display State
1	0	
1	1 Blinking Mode	
0	0 0 1	

9. DD/CG RAM Address set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	80h to FFh

DD/CG RAM Address set instruction fields DDRAM/CGRAM address

Before writing / reading data into /from RAM, set address by RAM Address Set Instruction. Next when data are written / read in succession. The address is automatically increased by 1. For accessing DD/ CGRAM, the DD/CGRAM Address Set Instruction should be set before. After accessing 7FH, the address of AC is 00H.

The address range are 00H ~ 7FH.

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	DDRAM line 1(00H ~ 0FH)															
10H	DDRAM line 2(10H ~ 1FH)															
20H	DDRAM line 3(20H ~ 2FH)															
30H	DDRAM line 4(30H ~ 3FH)															
40H	CGRAM (pattern 0)								CGRAM (pattern 1)							
50H	CGRAM (pattern 2)								CGRAM (pattern 3)							
60H	CGRAM (pattern 4)								CGRAM (pattern 5)							
70H	CGRAM (pattern 6)								CGRAM (pattern 7)							

10. ICONRAM Address Set

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	1	0	IA4	IA3	IA2	IA1	IA0	40h to 5Fh

ICONRAM Address Set instruction fields ICONRAM / Registers address.
Before writing / reading data into /from ICON RAM, set the address by ICONRAM Address Set Instruction. Next when data are written / read in succession. The address is automatically increased by 1. For accessing ICONRAM, the ICONRAM Address Set Instruction should be set before. After accessing 0FH, the address of ICONRAM address is 00H.The ICONRAM address range are 00H ~ 1FH.
The 5 icons at a time can blink, if C and B bits of the display instructions are enabled. The blink attributes of ICON are same as the cursor blink.

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00H	ICONRAM (00H ~ 0FH)															
10H	EV	TE	Reserved													

EV: electronic volume register (10H) ~ default (00000)
TE: test register (Do not use)(11H)
When the EV and TE registers are written, the address counter (AC) is not increased.

11. Write Data

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
1	D7	D6	D5	D4	D3	D2	D1	D0	XX

The instruction field makes NT7606 write binary 8-bit data to DDRAM/CGRAM/ICONRAM or register. The RAM address to be written into is determined by previous DD/CGRAM Address Set instruction. After writing operation, the address is automatically increased by 1.

12. Read Data

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
1	D7	D6	D5	D4	D3	D2	D1	D0	XX

DDRAM/CGRAM/ICONRAM data read instruction.
Each RAM is selected by address set instruction. And then you can read the RAM data. You can get correct RAM data from second read transaction. The first read data after setting RAM address is dummy data; so the correct RAM data come from the second read transaction. After reading operation, the address is increase by 1 automatically.

13. NOP

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	0	0	0	0	0	0	00h

Non-Operation Instruction

14. Test Instruction

RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	0	0	1	1	*	*	*	*	30h to 3Fh

This is the dedicate IC chip test instruction. It must not be used for normal operation.

Table 15. Instruction Table

Instruction	Code										Function
	RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Return home	0	0	0	0	0	0	0	1	-	02h to 03h	DDRAM address is set to 00h from AC and the cursor returns to 00h position. The contents of DDRAM are not changed
Double height Mode	0	0	0	0	0	1	0	DH2	DH1	08h to 0Bh	Double height mode DH2 DH1 = 00: normal display (default) 01: COM1 ~ COM16 is a double height. COM17 ~ COM24 is normal 10: 1) 2-line mode: normal display 2) 3-line mode: COM1 ~ COM8 is normal and COM9 ~ COM24 is a double height. 11: normal display
Power save	0	0	0	0	0	1	1	OS	PS	0Ch to 0Fh	Power save/oscillation circuit ON/OFF OS = 0: oscillator OFF (default) OS = 1: oscillator ON PS = 0: power save OFF (default) PS = 1: power save ON
Function set	0	0	0	0	1	0	N	S	CG	10h to 17h	Display line mode N = 0: 2-line display mode (default) N = 1: 3-line display mode Shifting direction of COM S = 0: 1) 2-line mode: COM1 -> COM16 (default) 2) 3-line mode: COM1 -> COM24 S = 1: 1) 2-line mode: COM16 -> COM1 2) 3-line mode: COM24 -> COM1 Select CGRAM or CGROM CG = 0: CGROM (default) CG = 1: CGRAM
Line shift mode	0	0	0	0	1	1	0	LS2	LS1	18h to 1Bh	Determination of the DDRAM line, which is displayed at the first line at LCD. LS2, LS1 = 00: DDRAM line 1 shows at (default) the first line of LCD. LS2, LS1 = 01: DDRAM line 2 shows at the first line of LCD. LS2, LS1 = 10: DDRAM line 3 shows at the first line of LCD. LS2, LS1 = 11: DDRAM line 4 shows at the first line of LCD.
Bias control	0	0	0	0	1	1	1	-	BS	1Ch to 1Fh	Determination of Bias BS = 0: 1/5 bias (default) BS = 1: 1/4 bias

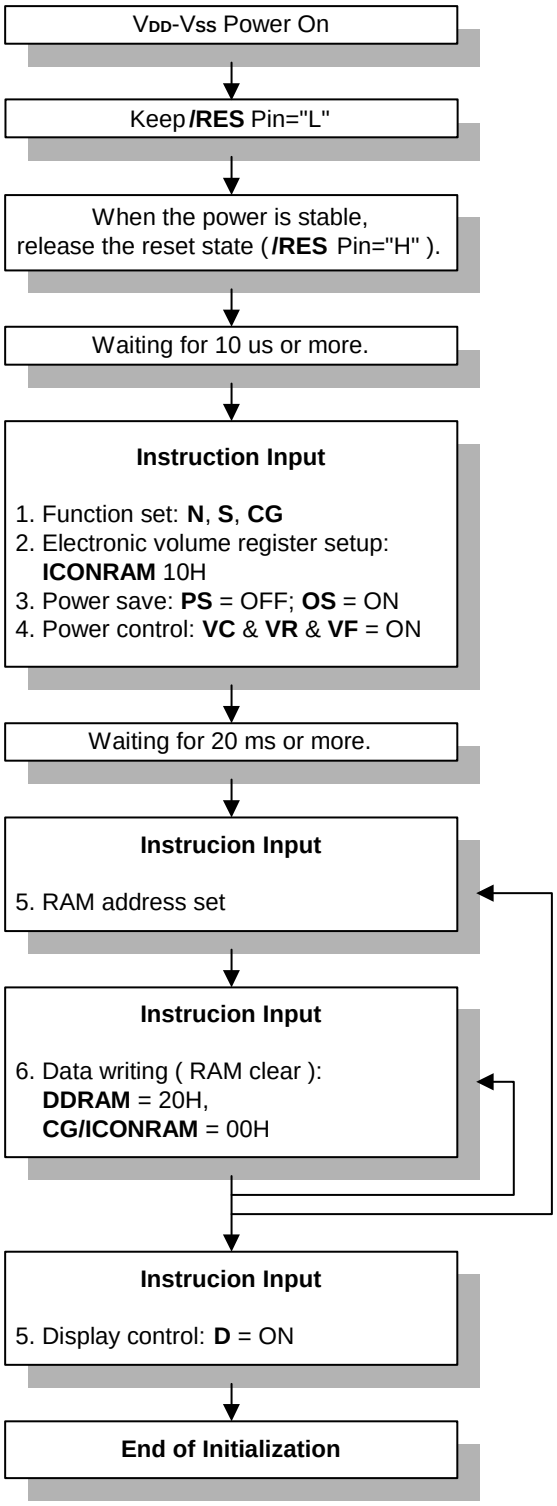
Table 15. Instruction Table (continued)

Instruction	Code										Function
	RS	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
Power control	0	0	0	1	0	0	VC	VR	VF	20h to 27h	LCD power control VC = 0: voltage converter OFF (default) VC = 1: voltage converter ON VR = 0: voltage regulator OFF (default) VR = 1: voltage regulator ON VF = 0: voltage follower OFF (default) VF = 1: voltage follower ON
Display control	0	0	0	1	0	1	C	B	D	28h to 2Fh	Cursor/ blink /display ON/OFF C = 0: cursor OFF (default) 1: cursor ON B = 0: blink OFF (default) 1:blink ON D = 0: display OFF (default) 1:display ON
DD/CGRAM address set	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	80h to FFh	DDRAM/CGRAM Range: DDRAM 00h~3FH CGRAM 40h~7FH
ICONRAM address set	0	0	1	0	IA4	IA3	IA2	IA1	IA0	40h to 5Fh	ICONRAM address, electronic volume and test byte address Range: ICONRAM 00H~0FH EV 10H (Electronic volume byte) TE 11H (Test byte)
Write Data	1	D7	D6	D5	D4	D3	D2	D1	D0	XX	Write DDRAM/CGRAM/ICONRAM
Read Data	1	D7	D6	D5	D4	D3	D2	D1	D0	XX	Read DDRAM/CGRAM/ICONRAM or register data
NOP	0	0	0	0	0	0	0	0	0	00h	Non-operation Instruction
Test Instruction	0	0	0	1	1	*	*	*	*	30h to 3Fh	Don't use this Instruction

Note:
1. "-" Don't care.
2. "* "Don't use.
3. Instruction execution time depends on the internal process time of NT7606; therefore it is necessary to provide a time larger than one MPU interface cycle time (T_{CYC}) between executions of two successive instructions.

Instruction Description (for reference only)

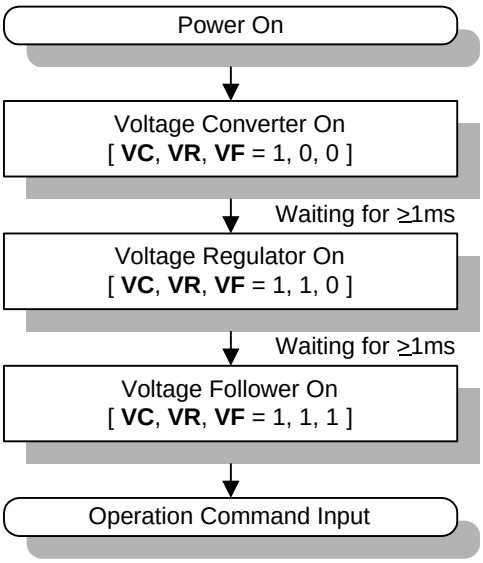
1. Initialization



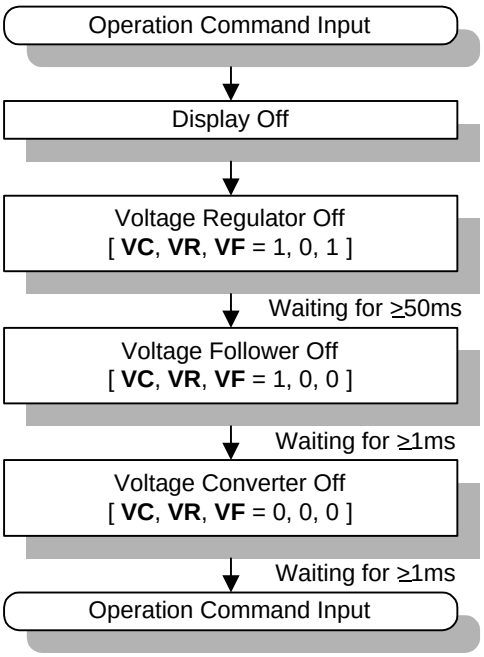
Note:
At command 5 and 6, the internal RAM should be cleared.
To clear DDRAM, set address at 00H (first DDRAM) and then write 20H (space character code) 64 times.
To clear CGRAM, set address at 40H (first CGRAM) and then write 00H (NULL data) 64 times.
To clear ICONRAM, set address at 00H (first ICONRAM) and then write 00H (NULL data) 16 times.

2. Recommendation of Power On/Off Sequence

Power On Sequence



Power Off Sequence



Absolute Maximum Rating

DC Supply Voltage (VDD, VDD2)..... -0.3V to +3.6V
DC Supply Voltage (VLCD, VOUT) ..... -0.3V to +11.0V
Input Voltage (Vin) ..... -0.3V to +3.6V
Operating Ambient Temperature ..... -40°C to +85°C
Storage Temperature ..... -55°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

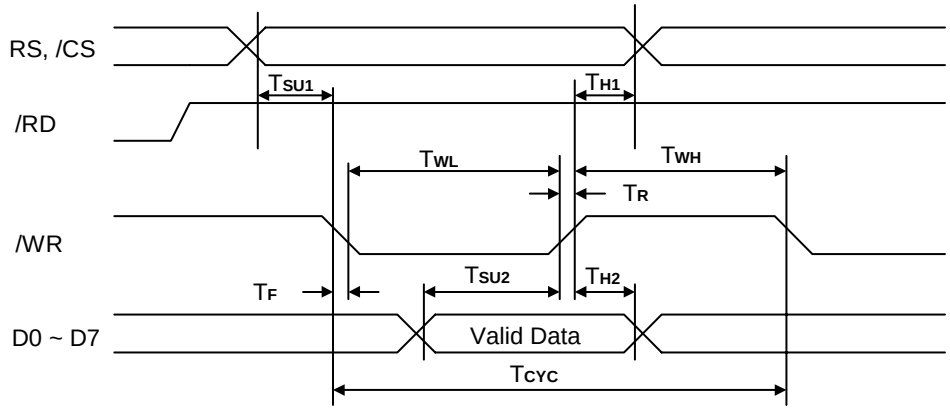
DC Characteristics (VSS = 0V, VDD = 2.4 ~ 3.3 V, Ta = -40 ~ 85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Operating Voltage	2.4	-	3.3	V	
VOUT	Converter output voltage	6.0	-	10.0	V	Ta = 25°C, C = 1μF
VLCD	Voltage regulator operation voltage	4.0	-	6.0	V	VLCD = V0 - VSS
VREF	Reference voltage	1.94	2.00	2.06	V	Ta = 25°C
IDD1	Dynamic current consumption 1	-	-	80	μA	Display operation, Ra = 500KΩ, VLCD = 6V, without load. No access from MPU.
IDD2	Dynamic current consumption 2	-	-	500	μA	Access operation from MPU. (Fcyc = 200KHz)
ISP	Sleep mode current consumption	-	-	5	μA	During power save mode, Ta = 25°C
VIHC1	High-level input voltage	0.7×VDD	-	VDD	V	RS, D0 – D7, /RD (E), /WR (R/W), /CS, CL, C86, P/S, PI, VRS and DIRS.
VILC1	Low-level input voltage	VSS	-	0.3×VDD	V	
VIHC2	High-level input voltage	0.8×VDD	-	VDD	V	/RES pin is schmitt input.
VILC2	Low-level input voltage	VSS	-	0.2×VDD	V	
VOHC	High-level output voltage	VDD - 0.4	-	-	V	VDD = 2.4V, IOH = -1mA (D0 – D7)
VOLC	Low -level output voltage	-	-	VSS + 0.4	V	VDD = 2.4V, IOL = 1mA (D0 – D7)
ILI	Input leakage current	-1.0	-	1.0	μA	VIN = VDD or VSS (RS, /RD (E), /WR (R/W), /CS, CL, C86, P/S,VRS, DIRS and /RES)
IHZ	HZ leakage current	-3.0	-	3.0	μA	When the D0 - D7 are in high impedance.
RON1	COM driver ON resistance	-	-	5	KΩ	IO = ±50 μA
RON2	SEG driver ON resistance	-	-	10	KΩ	IO = ±50 μA
FFR	LCD Frame frequency	70	80	90	Hz	TA = 25°C

Notes: Voltages V0≧V1≧V2≧V3≧V4≧VSS must always be satisfied.

AC Characteristics

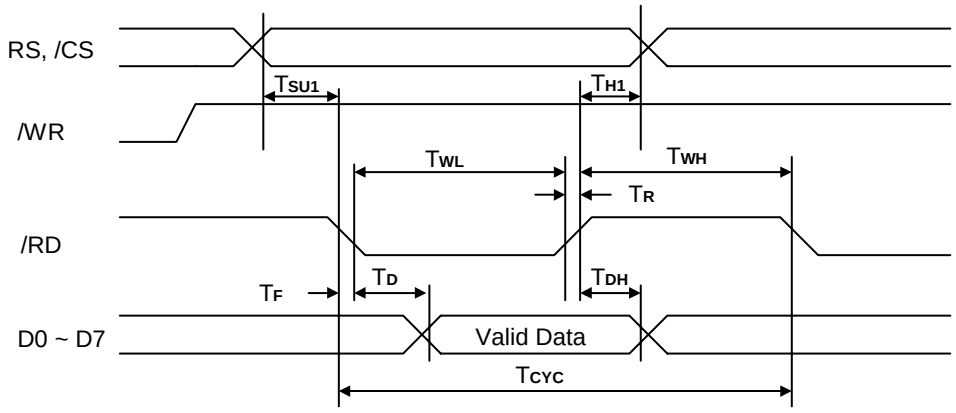
1. System Buses Read/Write Characteristics (for 8080 Series MPU)
   - Write timing



(VDD = 2.4 ~ 3.3 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	/WR cycle time	650	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_{WH}	/WR high pulse width	150	-	-	ns	
T_{WL}	/WR low pulse width	450	-	-	ns	
T_{SU1}	RS and /CS setup time	60	-	-	ns	
T_{H1}	RS and /CS hold time	30	-	-	ns	
T_{SU2}	Data setup time	100	-	-	ns	
T_{H2}	Data hold time	50	-	-	ns	

■ Read timing

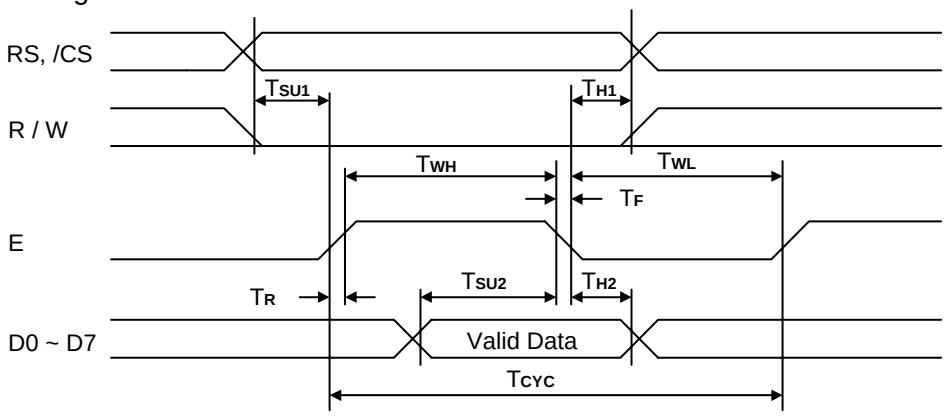


(VDD = 2.4 ~ 3.3 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	/RD cycle time	650	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_{WH}	/RD high pulse width	150	-	-	ns	
T_{WL}	/RD low pulse width	450	-	-	ns	
T_{SU}	RS and /CS setup time	60	-	-	ns	
T_H	RS and /CS hold time	30	-	-	ns	
T_D	Data output delay time	100	-	-	ns	
T_{DH}	Data output hold time	50	-	-	ns	

2. System Buses Read/Write Characteristics (for 6800 Series MPU)

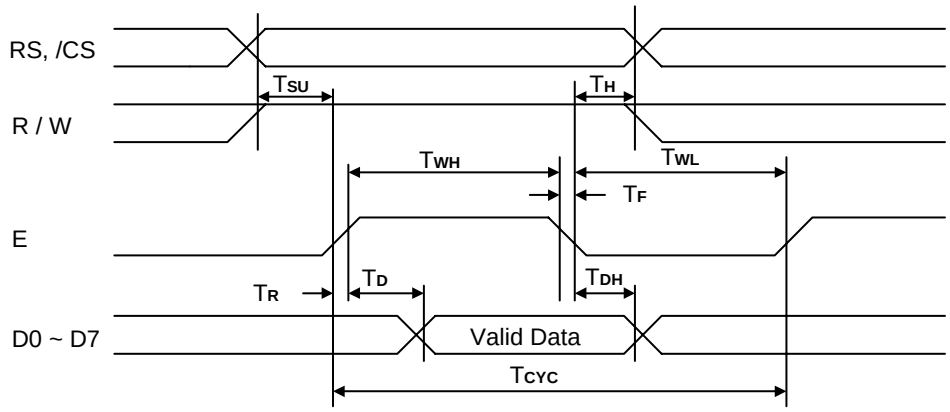
■ Write timing



(VDD = 2.4 ~ 3.3 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	E cycle time	650	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_{WH}	E high pulse width	450	-	-	ns	
T_{WL}	E low pulse width	150	-	-	ns	
T_{SU1}	RS and /CS setup time	60	-	-	ns	
T_{H1}	RS and /CS hold time	30	-	-	ns	
T_{SU2}	Data setup time	100	-	-	ns	
T_{H2}	Data hold time	50	-	-	ns	

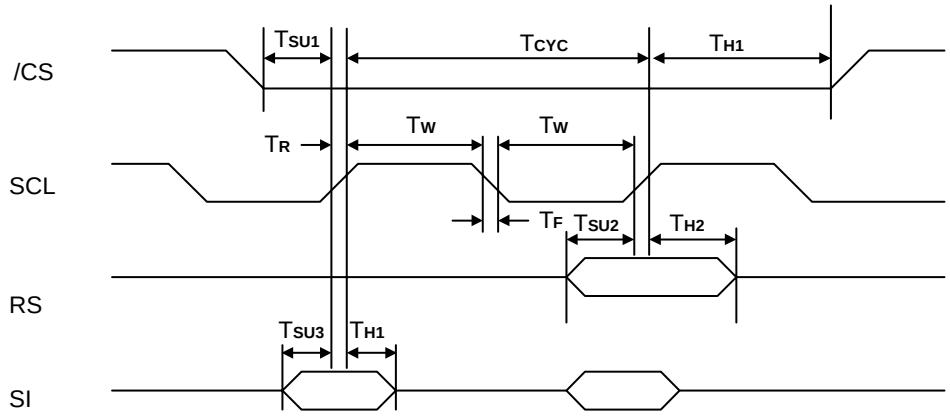
■ Read timing



(VDD = 2.4 ~ 3.3 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	E cycle time	650	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_{WH}	E high pulse width	450	-	-	ns	
T_{WL}	E low pulse width	150	-	-	ns	
T_{SU}	RS and /CS setup time	60	-	-	ns	
T_H	RS and /CS hold time	30	-	-	ns	
T_D	Data output delay time	100	-	-	ns	
T_{H2}	Data output hold time	50	-	-	ns	

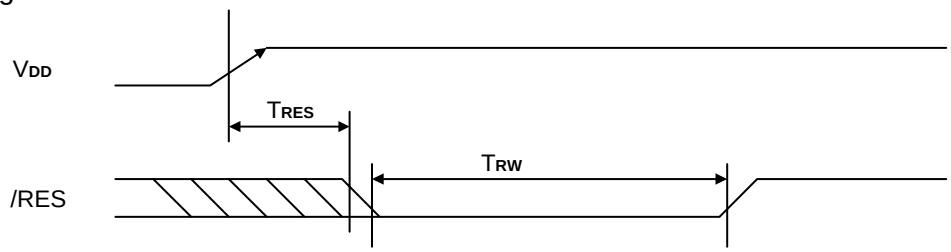
3. Serial Interface Timing



(VDD = 2.4 ~ 3.3 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{CYC}	SCL clock cycle time	1000	-	-	ns	
T_R, T_F	Pulse rise / fall time	-	-	25	ns	
T_W	SCL clock width (high to low)	300	-	-	ns	
T_{SU1}	/CS setup time	150	-	-	ns	
T_{H1}	/CS hold time	700	-	-	ns	
T_{SU2}	RS data setup time	50	-	-	ns	
T_{H2}	RS data hold time	300	-	-	ns	
T_{SU3}	SI data setup time	50	-	-	ns	
T_{H3}	SI data hold time	50	-	-	ns	

4. Reset Timing



(VDD = 2.4 ~ 3.3 V, Ta = -40 ~ 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{RES}	Reset start time	50	-	-	ns	
T_{RW}	Reset low pulse width	1	-	-	µs	

Microprocessor Interface (for reference only)

1. 8080-series microprocessors

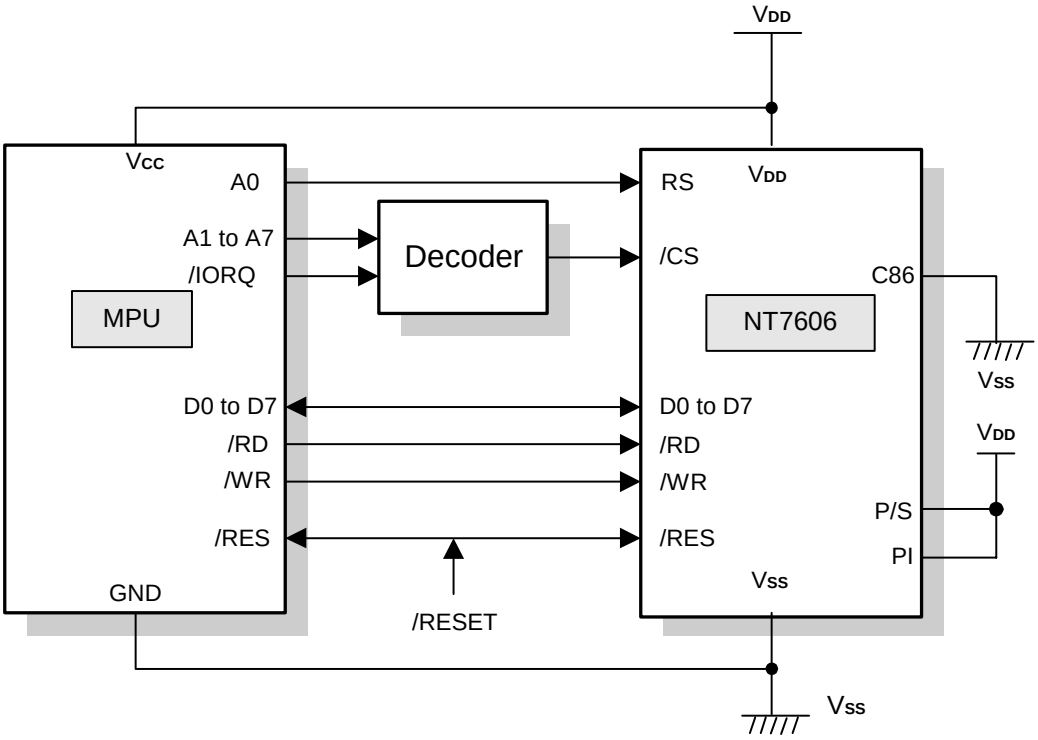


Figure 24

2. 6800-series microprocessors

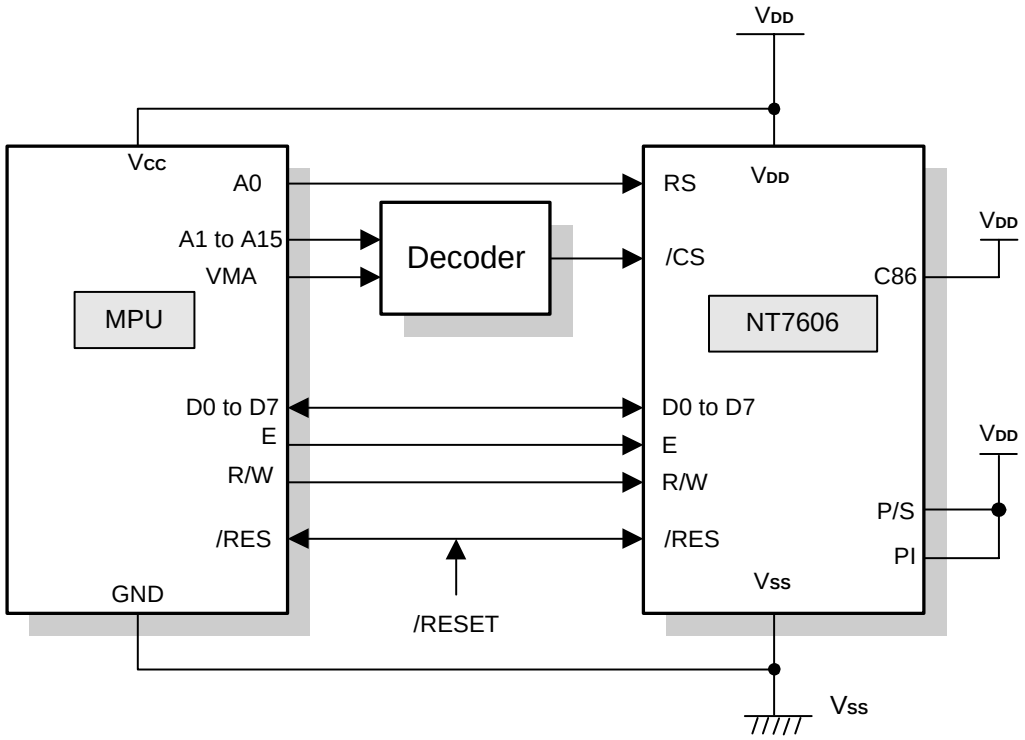
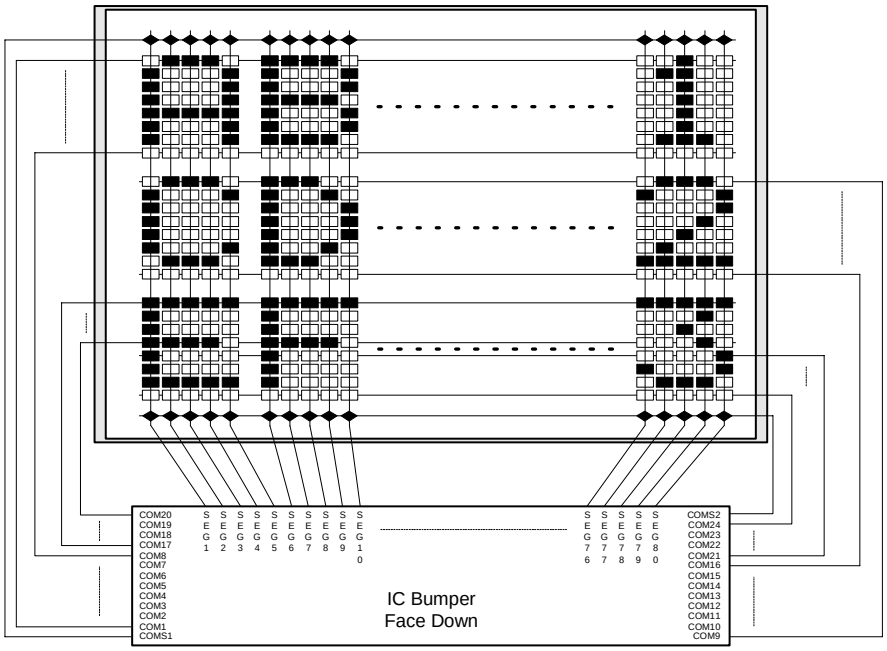


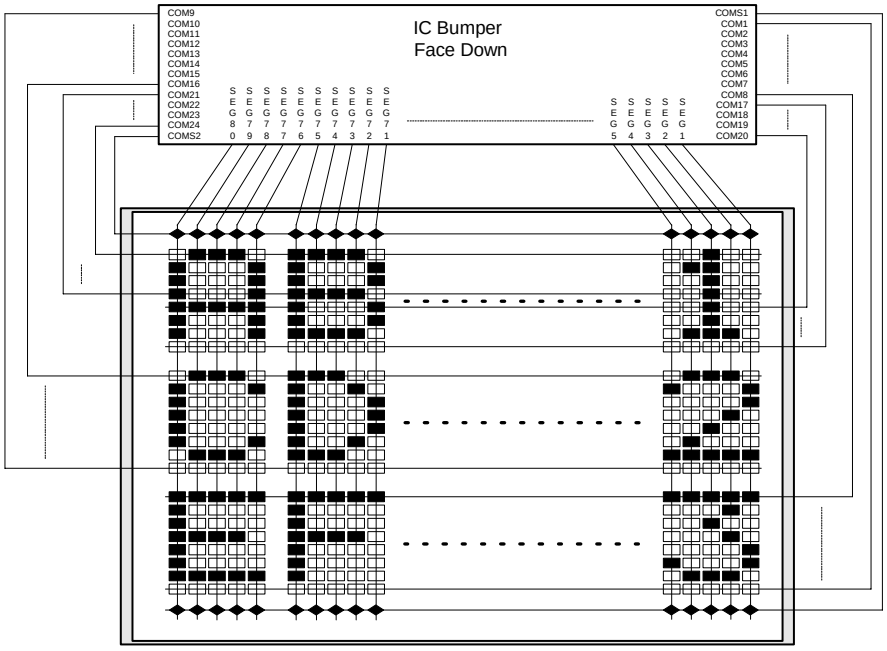
Figure 25

Application Information for LCD panel (for reference only)

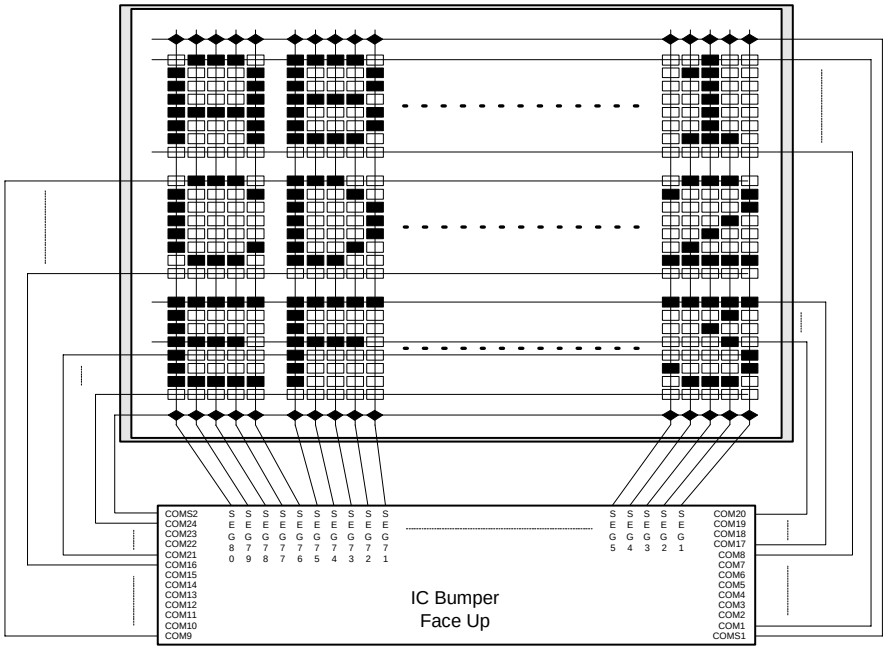
1. IC Bumper Face Down and Lower View (S bit = ’0’, DIRS = ’0’)



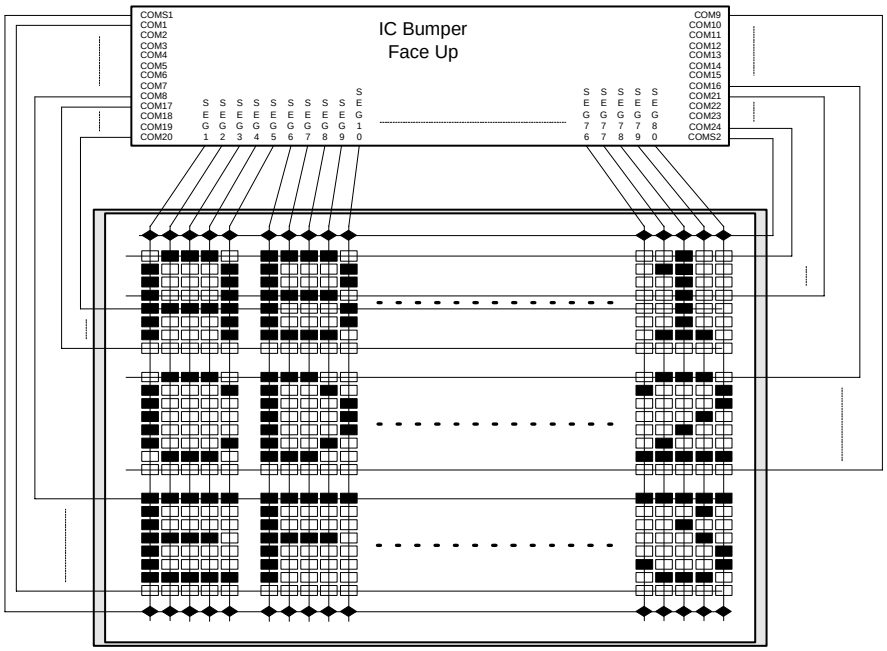
2. IC Bumper Face Down and Upper View (S bit = ’1’, DIRS = ’1’)



3. IC Bumper Face Up and Lower View (S bit = ’0’, DIRS = ’1’)



4. IC Bumper Face Up and Upper View (S bit = ’1’, DIRS = ’0’)

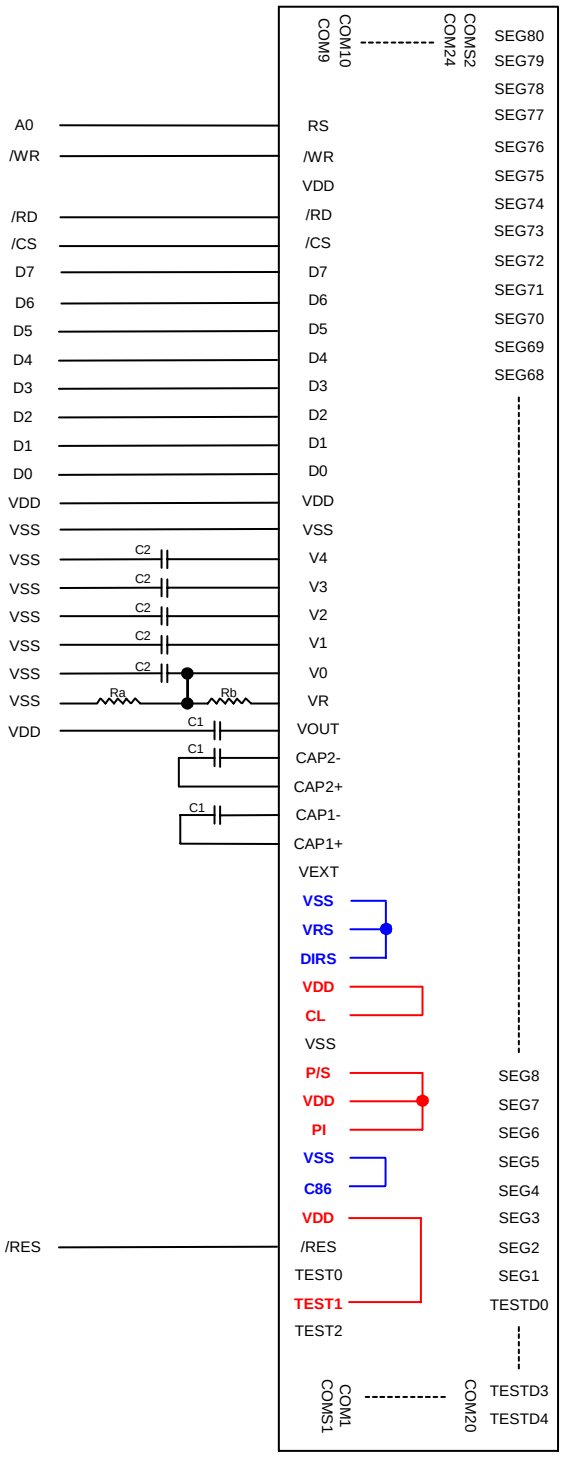


Application Information for Pin Connection to MPU (for reference only)

1. 8-bit 8080 MPU Mode:

   VRS=VSS: Internal Reference Voltage

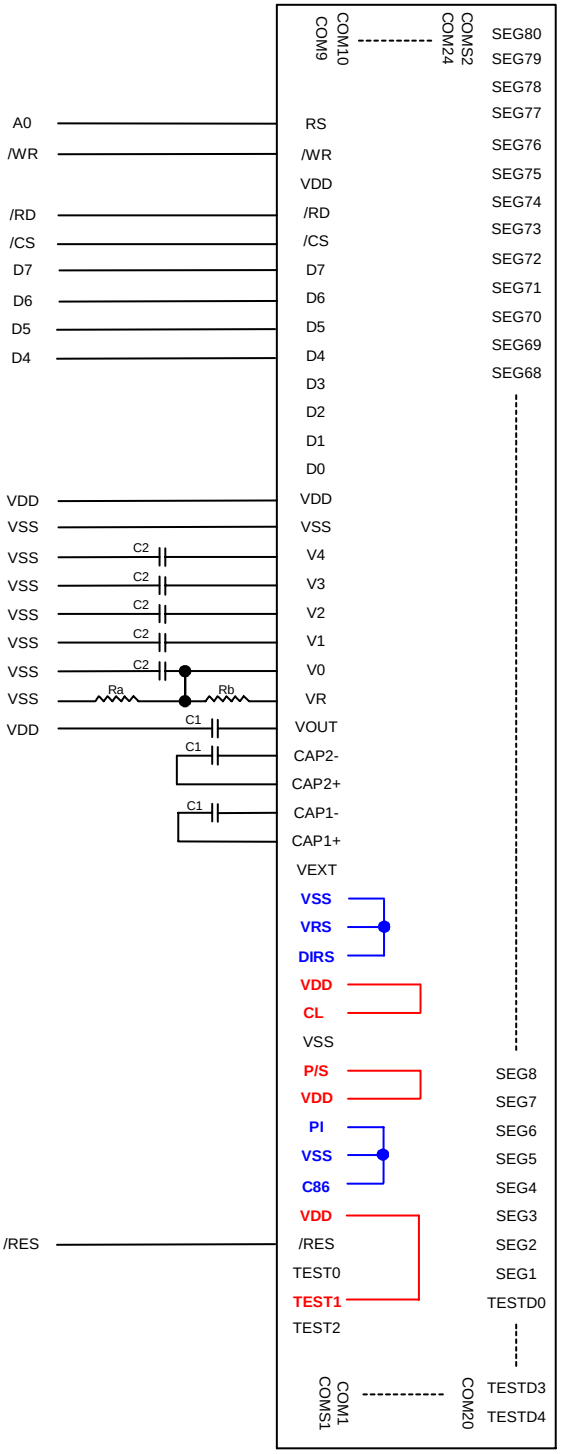
   DIRS=VSS: SEG DIR from SEG1 to SEG80



2. 4-bit 8080 MPU Mode:

   VRS=VSS: Internal Reference Voltage

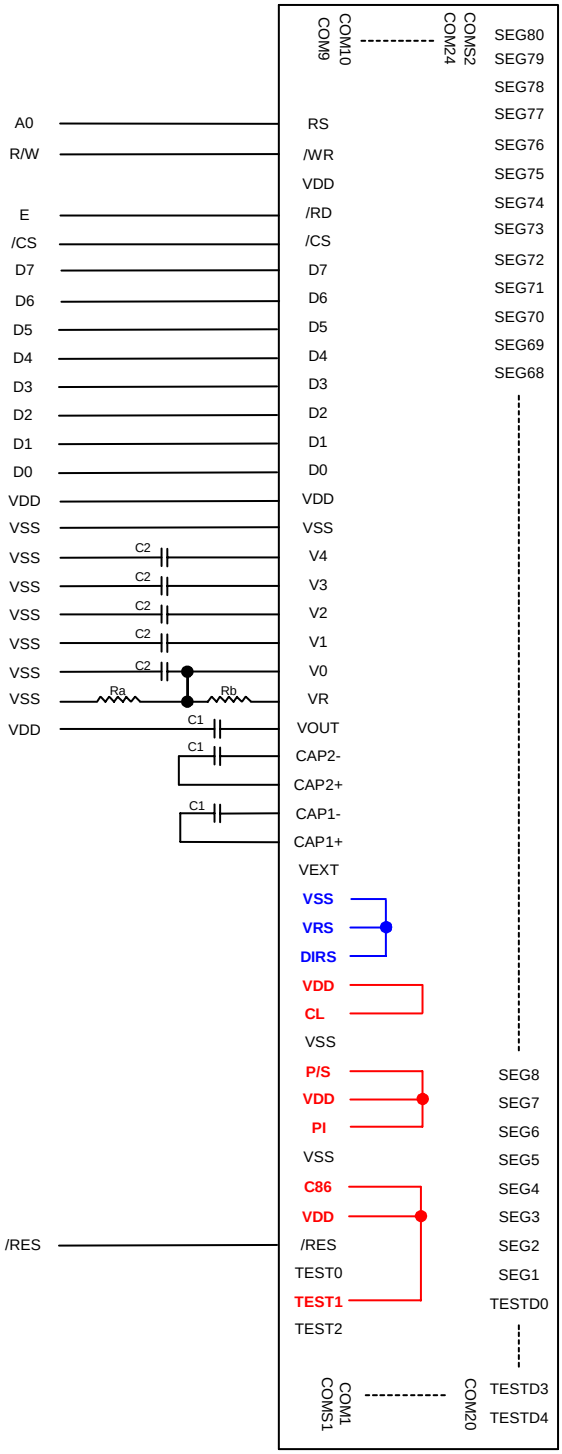
   DIRS=VSS: SEG DIR from SEG1 to SEG80



3. 8-bit 6800 MPU Mode:

VRS=VSS: Internal Reference Voltage

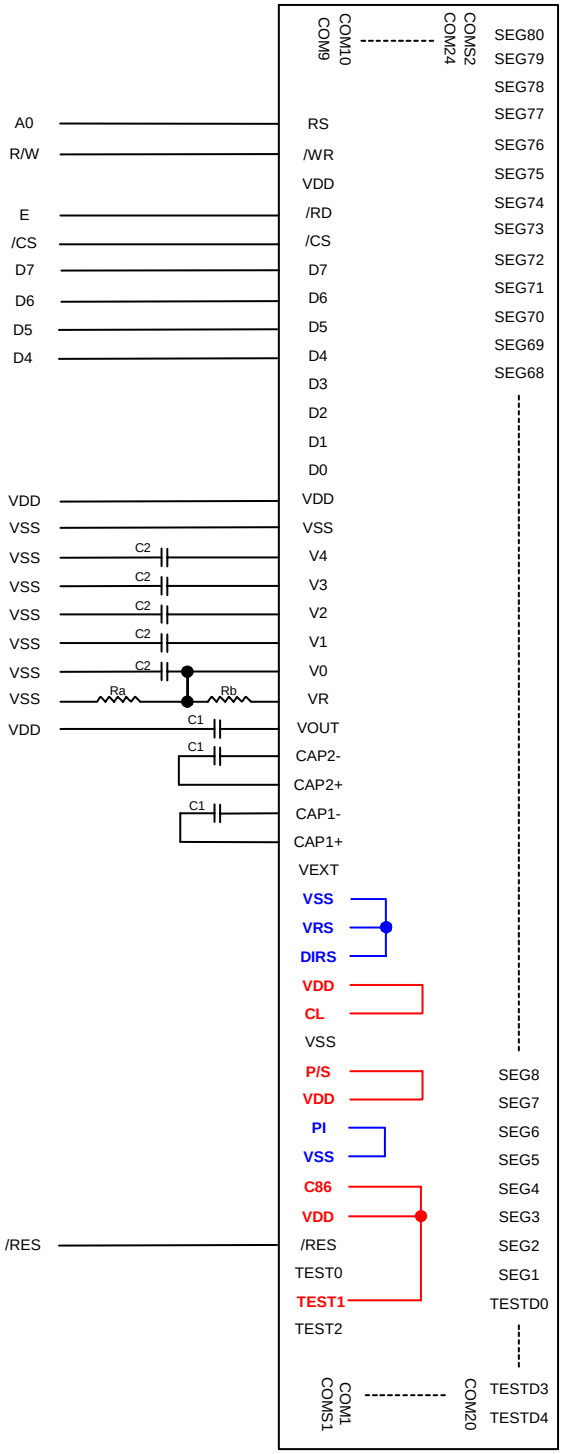
DIRS=VSS: SEG DIR from SEG1 to SEG80



4. 4-bit 6800 MPU Mode:

VRS=VSS: Internal Reference Voltage

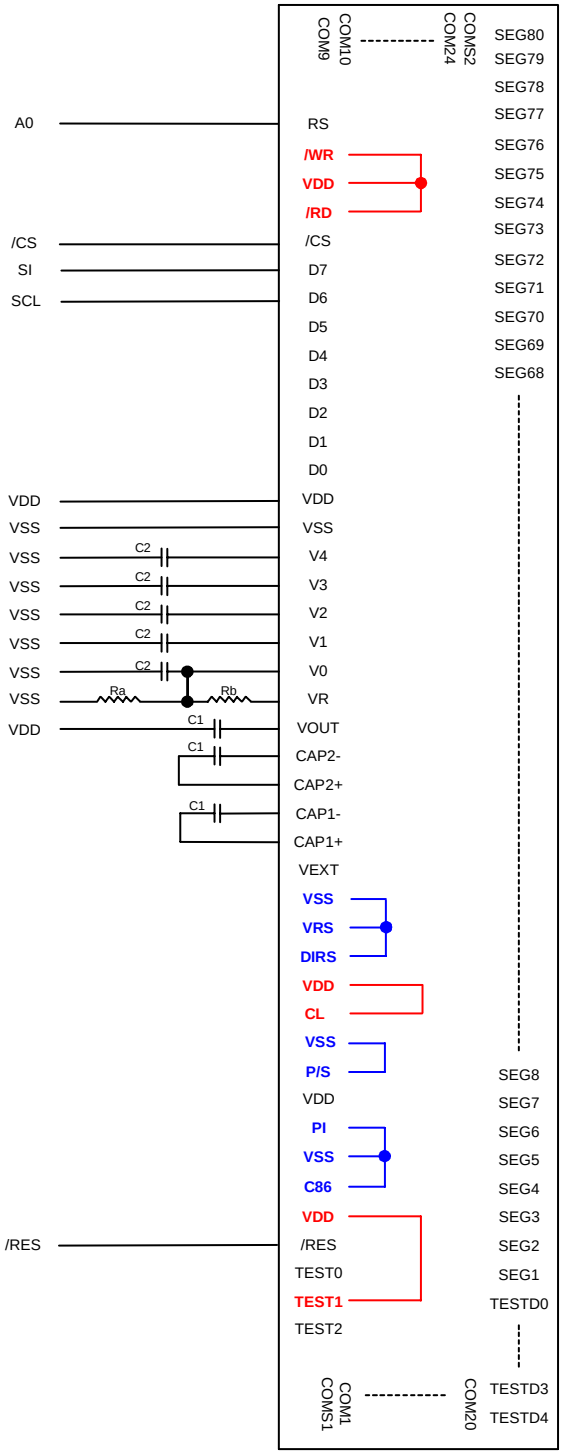
DIRS=VSS: SEG DIR from SEG1 to SEG80



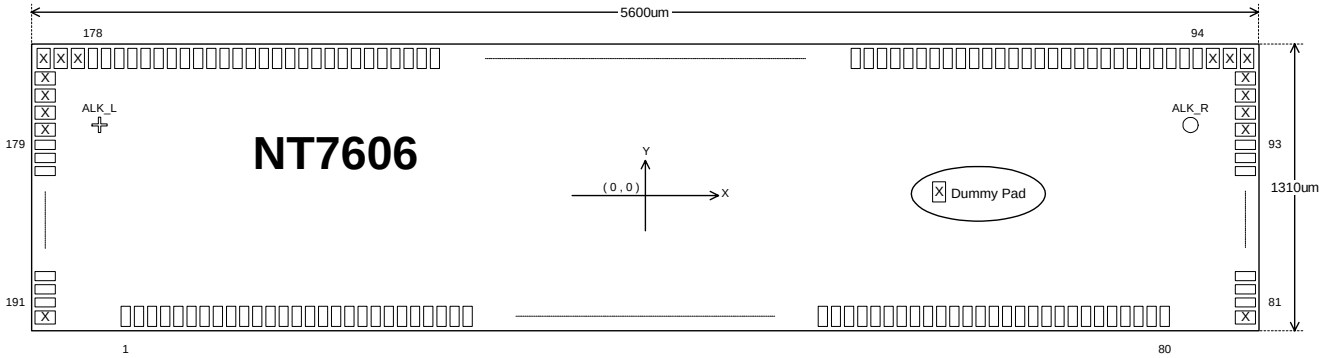
5. Serial Mode:

VRS=VSS: Internal Reference Voltage

DIRS=VSS: SEG DIR from SEG1 to SEG80



Bonding Diagram



Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	RS	-2370	-592.55	31	V3	-570	-592.55
2	VSS	-2310	-592.55	32	V3	-510	-592.55
3	/WR	-2250	-592.55	33	V2	-450	-592.55
4	VDD	-2190	-592.55	34	V2	-390	-592.55
5	/RD	-2130	-592.55	35	V1	-330	-592.55
6	/CS	-2070	-592.55	36	V1	-270	-592.55
7	D7	-2010	-592.55	37	V0	-210	-592.55
8	D6	-1950	-592.55	38	V0	-150	-592.55
9	D5	-1890	-592.55	39	V0	-90	-592.55
10	D4	-1830	-592.55	40	V0	-30	-592.55
11	D3	-1770	-592.55	41	VR	30	-592.55
12	D2	-1710	-592.55	42	VR	90	-592.55
13	D1	-1650	-592.55	43	VOUT	150	-592.55
14	D0	-1590	-592.55	44	VOUT	210	-592.55
15	VDD	-1530	-592.55	45	CAP2-	270	-592.55
16	VDD	-1470	-592.55	46	CAP2-	330	-592.55
17	VDD	-1410	-592.55	47	CAP2-	390	-592.55
18	VDD	-1350	-592.55	48	CAP2+	450	-592.55
19	VDD	-1290	-592.55	49	CAP2+	510	-592.55
20	VDD	-1230	-592.55	50	CAP2+	570	-592.55
21	VDD	-1170	-592.55	51	CAP1-	630	-592.55
22	VSS	-1110	-592.55	52	CAP1-	690	-592.55
23	VSS	-1050	-592.55	53	CAP1-	750	-592.55
24	VSS	-990	-592.55	54	CAP1+	810	-592.55
25	VSS	-930	-592.55	55	CAP1+	870	-592.55
26	VSS	-870	-592.55	56	CAP1+	930	-592.55
27	VSS	-810	-592.55	57	VEXT	990	-592.55
28	VSS	-750	-592.55	58	VSS	1050	-592.55
29	V4	-690	-592.55	59	VRS	1110	-592.55
30	V4	-630	-592.55	60	DIRS	1170	-592.55

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	VDD	1230	-592.55	101	SEG3	2100	592.55
62	CL	1290	-592.55	102	SEG4	2040	592.55
63	VSS	1350	-592.55	103	SEG5	1980	592.55
64	P/S	1410	-592.55	104	SEG6	1920	592.55
65	VDD	1470	-592.55	105	SEG7	1860	592.55
66	PI	1530	-592.55	106	SEG8	1800	592.55
67	VSS	1590	-592.55	107	SEG9	1740	592.55
68	C86	1650	-592.55	108	SEG10	1680	592.55
69	VDD	1710	-592.55	109	SEG11	1620	592.55
70	/RES	1770	-592.55	110	SEG12	1560	592.55
71	TEST0	1830	-592.55	111	SEG13	1500	592.55
72	TEST1	1890	-592.55	112	SEG14	1440	592.55
73	TEST2	1950	-592.55	113	SEG15	1380	592.55
74	NC	2010	-592.55	114	SEG16	1320	592.55
75	NC	2070	-592.55	115	SEG17	1260	592.55
76	NC	2130	-592.55	116	SEG18	1200	592.55
77	NC	2190	-592.55	117	SEG19	1140	592.55
78	NC	2250	-592.55	118	SEG20	1080	592.55
79	NC	2310	-592.55	119	SEG21	1020	592.55
80	VSS	2370	-592.55	120	SEG22	960	592.55
81	COMS1	2737.5	-525.45	121	SEG23	900	592.55
82	COM1	2737.5	-465.45	122	SEG24	840	592.55
83	COM2	2737.5	-405.45	123	SEG25	780	592.55
84	COM3	2737.5	-345.45	124	SEG26	720	592.55
85	COM4	2737.5	-285.45	125	SEG27	660	592.55
86	COM5	2737.5	-225.45	126	SEG28	600	592.55
87	COM6	2737.5	-165.45	127	SEG29	540	592.55
88	COM7	2737.5	-105.45	128	SEG30	480	592.55
89	COM8	2737.5	-45.45	129	SEG31	420	592.55
90	COM17	2737.5	14.55	130	SEG32	360	592.55
91	COM18	2737.5	74.55	131	SEG33	300	592.55
92	COM19	2737.5	134.55	132	SEG34	240	592.55
93	COM20	2737.5	194.55	133	SEG35	180	592.55
94	TESTD4	2520	592.55	134	SEG36	120	592.55
95	TESTD3	2460	592.55	135	SEG37	60	592.55
96	TESTD2	2400	592.55	136	SEG38	0	592.55
97	TESTD1	2340	592.55	137	SEG39	-60	592.55
98	TESTD0	2280	592.55	139	SEG40	-120	592.55
99	SEG1	2220	592.55	139	SEG41	-180	592.55
100	SEG2	2160	592.55	140	SEG42	-240	592.55

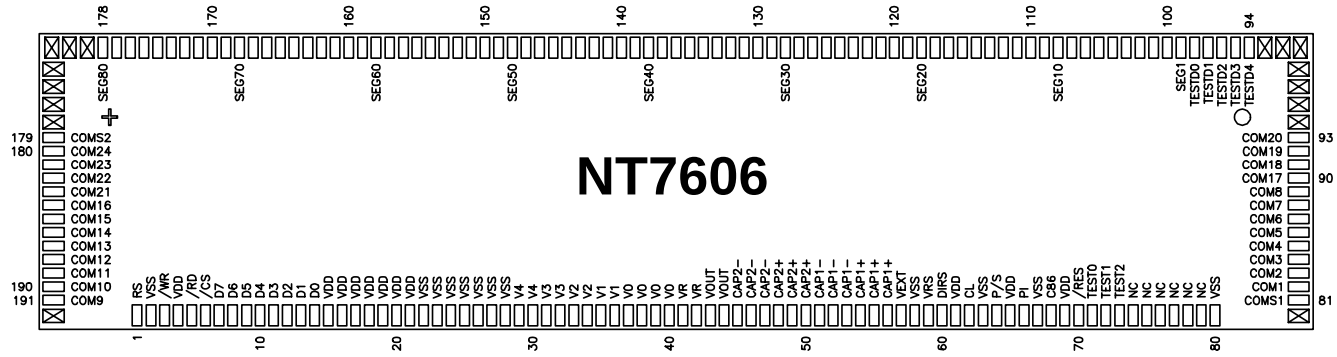
Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	SEG43	-300	592.55	168	SEG70	-1920	592.55
142	SEG44	-360	592.55	169	SEG71	-1980	592.55
143	SEG45	-420	592.55	170	SEG72	-2040	592.55
144	SEG46	-480	592.55	171	SEG73	-2100	592.55
145	SEG47	-540	592.55	172	SEG74	-2160	592.55
146	SEG48	-600	592.55	173	SEG75	-2220	592.55
147	SEG49	-660	592.55	174	SEG76	-2280	592.55
148	SEG50	-720	592.55	175	SEG77	-2340	592.55
149	SEG51	-780	592.55	176	SEG78	-2400	592.55
150	SEG52	-840	592.55	177	SEG79	-2460	592.55
151	SEG53	-900	592.55	178	SEG80	-2520	592.55
152	SEG54	-960	592.55	179	COMS2	-2737.5	194.55
153	SEG55	-1020	592.55	180	COM24	-2737.5	134.55
154	SEG56	-1080	592.55	181	COM23	-2737.5	74.55
155	SEG57	-1140	592.55	182	COM22	-2737.5	14.55
156	SEG58	-1200	592.55	183	COM21	-2737.5	-45.45
157	SEG59	-1260	592.55	184	COM16	-2737.5	-105.45
158	SEG60	-1320	592.55	185	COM15	-2737.5	-165.45
159	SEG61	-1380	592.55	186	COM14	-2737.5	-225.45
160	SEG62	-1440	592.55	187	COM13	-2737.5	-285.45
161	SEG63	-1500	592.55	188	COM12	-2737.5	-345.45
162	SEG64	-1560	592.55	189	COM11	-2737.5	-405.45
163	SEG65	-1620	592.55	190	COM10	-2737.5	-465.45
164	SEG66	-1680	592.55	191	COM9	-2737.5	-525.45
165	SEG67	-1740	592.55		ALK_L	-2490	285.25
166	SEG68	-1800	592.55		ALK_R	2490	285.25
167	SEG69	-1860	592.55				

Dummy Pad Location (Total: 16 pin)

NO	X	Y	NO	X	Y	NO	X	Y	NO	X	Y
0	2737.5	-594.45	4	2737.5	497.55	8	-2589	592.55	12	-2737.5	419.55
1	2737.5	263.55	5	2745	592.55	9	-2667	592.55	13	-2737.5	341.55
2	2737.5	341.55	6	2667	592.55	10	-2745	592.55	14	-2737.5	263.55
3	2737.5	419.55	7	2589	592.55	11	-2737.5	497.55	15	-2737.5	-594.45

Package Information



Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	5600	1310	μm
Pad pitch	1 ~ 80, 81 ~ 93, 94 ~ 178, 179 ~ 191	60		μm
	Dummy0 ~ Pad81, Pad93 ~ Dummy1, Dummy7 ~ Pad 94, Pad178 ~ Dummy8, Dummy14 ~ Pad179, Pad191 ~ Dummy15	69		
	Dummy1 ~ 4, Dummy5 ~ 7, Dummy8 ~ 10, Dummy11 ~ 14	78		
Bump size	1 ~ 80, 94 ~ 178	42	92	μm
	81 ~ 93, 179 ~ 191	92	42	
	Dummy0 ~ 4, Dummy11 ~ 15	92	60	
	Dummy5 ~ 10	60	92	
Bump height	All pads	15 ± 3		μm

Ordering Information

Part No.	Packages
NT7606H-BDT01	Gold Bump on Chip Tray