NOVATEK

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NT7702

240 Output LCD Segment/Common Driver

Features

(Segment mode)

- Shift Clock frequency:
  20 MHz (Max.) (V_{DD} = 5 V ± 10%)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function with an enable signal
- Automatic counting function when in the chip select mode, causes the internal clock to be stopped by automatically counting 240 bits of input data

(Common mode)

- Shift clock frequency :
  4.0 MHz (Max.)
- Built-in 240-bits bidirectional shift register (divisible into 120-bits x 2)
- Available in a single mode (240-bits shift register) or in a dual mode(120-bits shift register x 2)
  1. Y1 → Y240 Single mode
  2. Y240 → Y1 Single mode
  3. Y1 → Y120, Y121 → Y240 Dual mode
  4. Y240 → Y121, Y120 → Y1 Dual mode

  The above 4 shift directions are pin-selectable

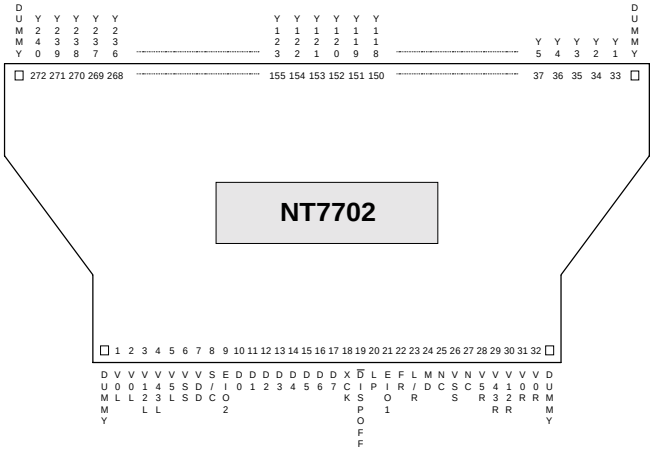
(Both for segment mode and common mode)

- Supply voltage for LCD driver: 15.0 to 30.0 V
- Number of LCD driver outputs: 240
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5 V
- COMS process
- Package: 272pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

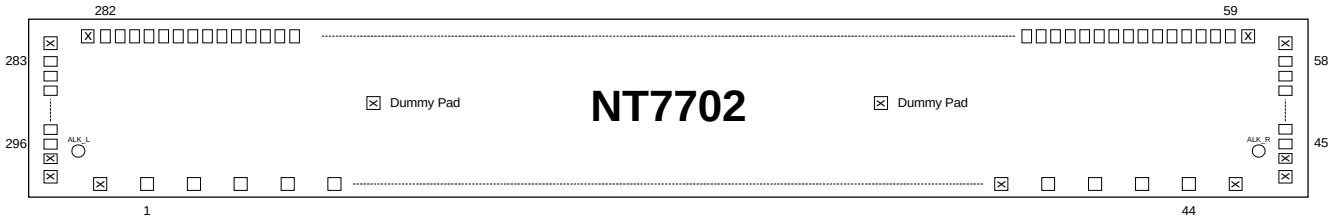
General Description

The NT7702 is a 240-bit output segment/common driver LSI suitable for driving large scale dot matrix LCD panels using as PDA/personal computers/work stations. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module. The NT7702 is good as both a segment driver and as a common driver, and a low power consuming, high-precision LCD panel display can be assembled using the NT7702. In the segment mode, the data input is selected as 4bit parallel input mode or as 8bit parallel input mode by a mode (MD) pin. In the common mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

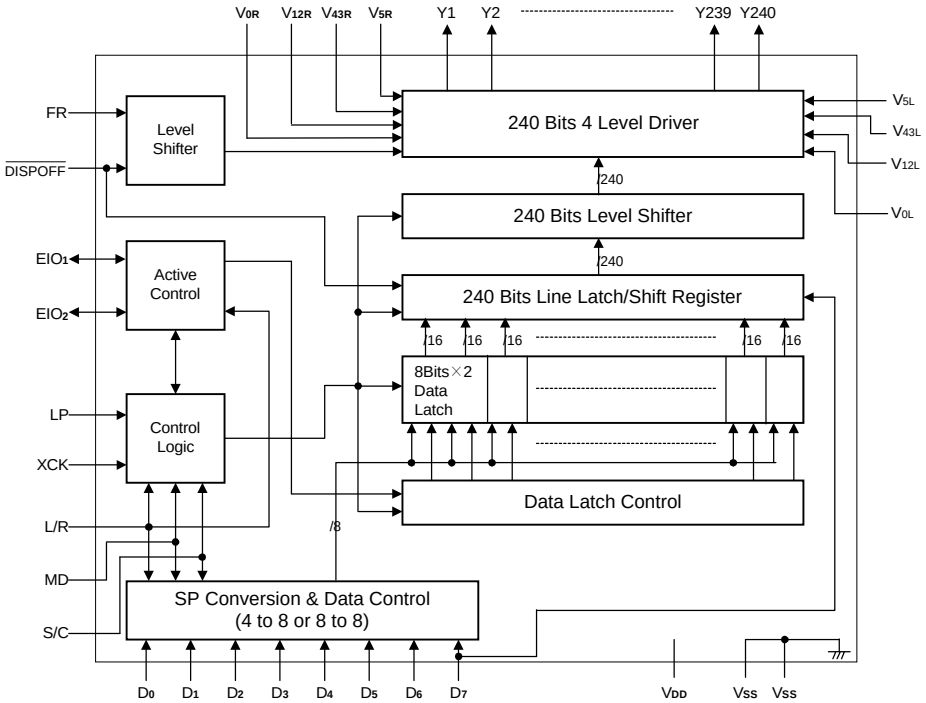
Pin Configuration



Pad Configuration



Block Diagram



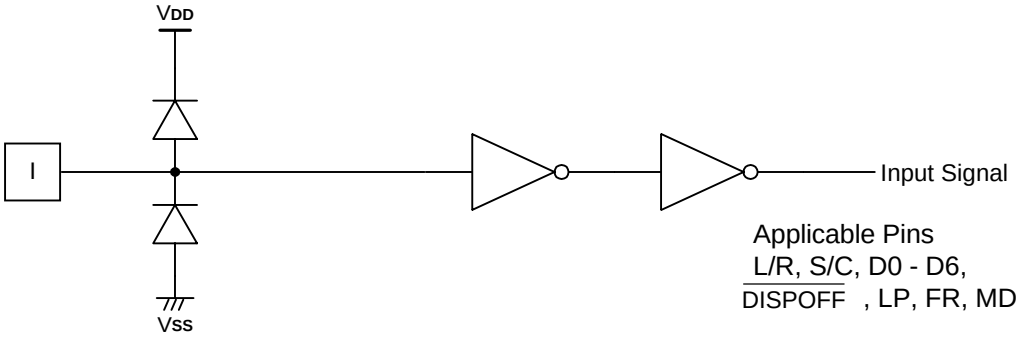
Pin Description

Pin No.	Designation	I/O	Description
1, 2	V_{0L}	P	Power supply for LCD driver
3	V_{12L}	P	Power supply for LCD driver
4	V_{43L}	P	Power supply for LCD driver
5	V_{5L}	P	Power supply for LCD driver
6	V_{SS}	P	Ground (0V), these two pads must be connected to each other
7	V_{DD}	P	Power supply for the logic system (+2.5 to +5.5V)
8	S/C	I	Segment mode/common mode selection
9	EIO_2	I/O	Input/output for chip select or data of the shift register
10 - 16	D0 - D6	I	Display data input for segment mode
17	D7	I	Display data input for Segment mode/ Dual mode data input
18	XCK	I	Display data shift clock input for segment mode
19	$\overline{DISPOFF}$	I	Control input for deselect output level
20	LP	I	Latch pulse input/shift clock input for the shift register
21	EIO_1	I/O	Input/output for chip select or data of the shift register
22	FR	I	AC-converting signal input for LCD driver waveform
23	L/R	I	Display data shift direction selection
24	MD	I	Mode selection input
25, 27	NC	-	No connected
26	V_{SS}	P	Ground (0V), these two pads must be connected to each other
28	V_{5R}	P	Power supply for LCD driver
29	V_{43R}	P	Power supply for LCD driver
30	V_{12R}	P	Power supply for LCD driver
31, 32	V_{0R}	P	Power supply for LCD driver
33 - 272	Y1 - Y240	O	LCD driver output

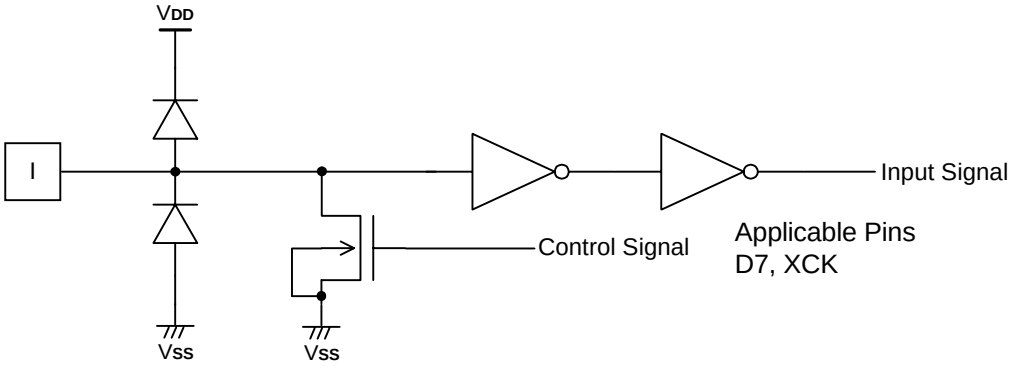
Pad Description

Pad No.	Designation	I/O	Description
1, 2	V_{5L}	P	Power supply for LCD driver
3, 4	V_{SS}	P	Ground (0V), these two pads must be connected to each other
5, 6	V_{DD}	P	Power supply for the logic system (+2.5 to +5.5V)
7, 8	S/C	I	Segment mode/common mode selection
9, 10	EIO_2	I/O	Input/output for chip select or data of the shift register
11, 12 - 23, 24	D0 - D6	I	Display data input for segment mode
25, 26	D7	I	Display data input for Segment mode/ Dual mode data input
27, 28	XCK	I	Display data shift clock input for segment mode
29, 30	$\overline{DISPOFF}$	I	Control input for deselect output level
31, 32	LP	I	Latch pulse input/shift clock input for the shift register
33, 34	EIO_1	I/O	Input/output for chip select or data of the shift register
35, 36	FR	I	AC-converting signal input for LCD driver waveform
37, 38	L/R	I	Display data shift direction selection
39, 40	MD	I	Mode selection input
41, 42	V_{SS}	P	Ground (0V), these two pads must be connected to each other
43, 44	V_{5R}	P	Power supply for LCD driver
45, 46	V_{43R}	P	Power supply for LCD driver
47, 48	V_{12R}	P	Power supply for LCD driver
49, 50	V_{0R}	P	Power supply for LCD driver
51 - 290	Y1 - Y240	O	LCD driver output
291, 292	V_{0L}	P	Power supply for LCD driver
293, 294	V_{12L}	P	Power supply for LCD driver
295, 296	V_{43L}	P	Power supply for LCD driver

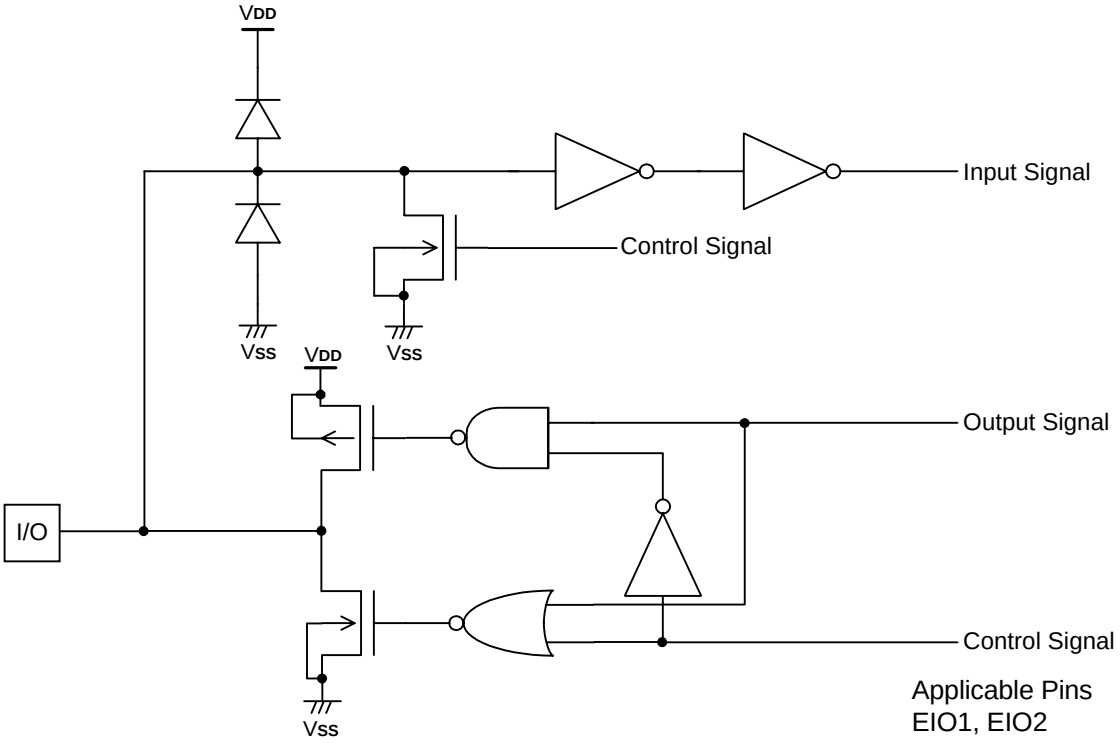
Input / Output Circuits



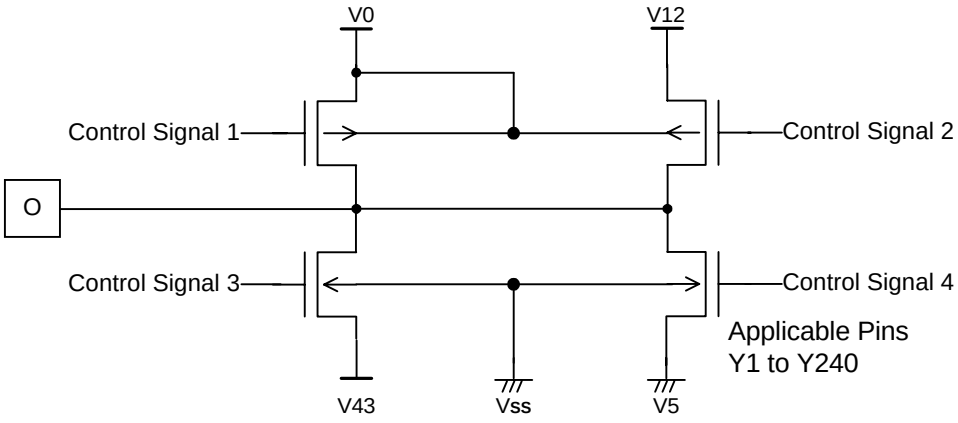
Input Circuit (1)



Input Circuit (2)



Input / Output Circuit



LCD Driver Output circuit

Pad Description

Segment mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{OR}, V_{OL} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43, 5)
D_0 - D_7	Input pin for display data ● In 4-bit parallel input mode, input data into the 4 pins D_0 - D_3. Connect D_4 - D_7 to V_{SS} or V_{DD} ● In 8-bit parallel input mode, input data into the 8 pins D_0 - D
XCK	Clock input pin for taking display data ● Data is read on the falling edge of the clock pulse
LP	Latch pulse input pin for display data ● Data is latched on the falling edge of the clock pulse
L/R	Direction selection pin for reading display data ● When set to V_{SS} level "L", data is read sequentially from Y240 to Y1 ● When set to V_{DD} level "H", data is read sequentially from Y1 to Y240
$\overline{\text{DISPOFF}}$	Control input pin for output deselect level ● The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD driver circuit. ● When set to V_{SS} level “L”, the LCD driver output pins (Y1-Y240) are set to level V_5 ● While $\overline{\text{DISPOFF}}$ set to “L”, the contents of the line latch are reset, but read the display data in the data latch are read regardless of the condition of $\overline{\text{DISPOFF}}$. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the date latch onto the next falling edge of the LP. That time, if $\overline{\text{DISPOFF}}$ removal time can not keep regulation what is shown AC characteristics, can not output the reading data correctly
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from the logic voltage level to the driver voltage level and controls the LCD driver circuit. ● Normally inputs a frame inversion signal The LCD driver output pin’s output voltage level can be set to the line latch output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level “L”, 8-bit parallel input mode is set ● When set to V_{DD} level “H", 4-bit parallel input mode is set

Segment mode continued

Symbol	Function
S/C	Segment mode/common mode selection pin ● When set to V_{DD} level "H", segment mode is set ● When set to V_{SS} level "L", common mode is set
EIO_1, EIO_2	Input/output pin for chip selection ● When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input ● When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output ● During output, it is set to "H" while LP* $\overline{XCK}$ is "H" and after 240-bits of data have been read, it is set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H" ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 240-bits of data have been read, the chip is deselected
Y_1 - Y_{240}	LCD driver output pins These correspond directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Common mode

Symbol	Function
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5V
V_{SS}	Ground pin connects to 0V
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias. ● Normally, the bias voltage used is set by a resistor divider ● Ensure the voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$ To further reduce the differences between the output waveforms of the LCD driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL} (I = 0, 12, 43, 5)
EIO_1	Bi-directional shift register shift data input/output pin ● Is an output pin when L/R is at V_{SS} level "L" and an input pin when L/R is at V_{DD} level "H" ● When EIO_1 is used as an input pin, it will be pulled-down ● When EIO_1 is used as an output pin, it won't be pulled-down
EIO_2	Bi-directional shift register shift data input/output pin ● Is an input pin when L/R is at V_{SS} level "L" and an output pin when L/R is at V_{DD} level "H" ● When EIO_2 is used as input pin, it will be pulled-down ● When EIO_2 is used as output pin, it won't be pulled-down
LP	Bi-directional shift register shift clock pulse input pin ● Data is shifted on the falling edge of the clock pulse
L/R	Bi-directional shift register shift direction selection pin ● Data is shifted from Y_{240} to Y_1 when it is set to V_{SS} level "L", and data is shifted from Y_1 to Y_{240} when it is set to V_{DD} level "H"

Common mode continued

Symbol	Function
$\overline{\text{DISPOFF}}$	Control input pin for output deselect level ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level, and controls the LCD driver circuit ● When set to V_{SS} level "L", the LCD driver output pins (Y_1-Y_{240}) are set to level V_5 ● While set to "L", the contents of the shift resister are reset and are not reading data. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}), and the shift data is read on the falling edge of the LP. That time, if $\overline{\text{DISPOFF}}$ removal time can not keep regulation what is shown AC characteristics, the shift data is not reading correctly
FR	AC signal input for LCD driving waveform ● The input signal is level-shifted from logic voltage level to the LCD driver voltage level, and it controls the LCD driver circuit ● Normally, inputs a frame inversion signal The LCD driver output pin's output voltage level can be set using the shift register output signal and the FR signal
MD	Mode selection pin ● When set to V_{SS} level "L", Single Mode operation is selected. When set to V_{DD} level "H", Dual Mode operation is selected
D_7	Dual Mode data input pin ● According to the data shift direction of the data shift register, data can be input starting from the 121st bit When the chip is used as Dual Mode, D_7 will be pulled-down When the chip is used as Single Mode, D_7 won't be pulled-down
S/C	Segment mode/common mode selection pin ● When set to V_{SS} level "L", common mode is set
D_0 - D6	Not used ● Connect D_0-D_6 to V_{SS} or V_{DD}. Avoiding floating
XCK	Not used ● XCK is pull-down in common mode, so connect to V_{SS} or open
Y_1 - Y_{240}	LCD driver output pins ● These correspond directly Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output

Functional Description

1. Block description

1.1 Active Control

In the case of the segment mode, it controls the selection or deselection of the chip. Following a LP signal input, and after the select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the ship is deselected.

In the case of the common mode, it controls the input/output data of the bi-directional pins.

1.2. SP Conversion & Data Control

In the case of the segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

1.3. Data Latch Control

In the case of the segment mode, selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

1.4. Data Latch

In the case of the segment mode, latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control 240 bits of data are read in 20 sets of 8 bits.

1.5. Line Latch/Shift Register

In the case of the segment mode, all 240 bits which have been read into the data latch, are simultaneously latched on to the falling edge of the LP signal, and output to the level shift block.

In the case of the common mode, it shifts data from the data input pin on to the falling edge of the LP signal.

1.6. Level Shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

1.7. 4-Level Driver

It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0, V_{12}, V_{43}, V_5) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

1.8. Control Logic

Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 240 bits of data are read in, and the chip is deselected.

In the case of the common mode, it controls the direction of data shift.

2. LCD Driver Output Voltage Level

The relationship amongst the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

2.1. Segment Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

2.2. Common Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y_1 - Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H: V_{DD} (+2.5 to +5.5V), L: V_{SS} (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage which assigned by specification for each power pin.
That time "Don't care" should be fixed to "H" or "L", avoiding floating.

3. Relationship between the Display Data and Driver Output pins

3.1. Segment Mode:

(a) 4-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Number of Clock						
					60clock	59clock	58clcok	~	3clock	2clock	1clock
H	L	Output	Input	D_0	Y1	Y5	Y9	~	Y229	Y233	Y237
				D_1	Y2	Y6	Y10	~	Y230	Y234	Y238
				D_2	Y3	Y7	Y11	~	Y231	Y235	Y239
				D_3	Y4	Y8	Y12	~	Y232	Y236	Y240
H	H	Input	Output	D_0	Y240	Y236	Y232	~	Y12	Y8	Y4
				D_1	Y239	Y235	Y231	~	Y11	Y7	Y3
				D_2	Y238	Y234	Y230	~	Y10	Y6	Y2
				D_3	Y237	Y233	Y229	~	Y9	Y5	Y1

(b) 8-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Number of Clock						
					30clock	29clock	28clcok	~	3clock	2clock	1clock
L	L	Output	Input	D_0	Y1	Y9	Y17	~	Y217	Y225	Y233
				D_1	Y2	Y10	Y18	~	Y218	Y226	Y234
				D_2	Y3	Y11	Y19	~	Y219	Y227	Y235
				D_3	Y4	Y12	Y20	~	Y220	Y228	Y236
				D_4	Y5	Y13	Y21	~	Y221	Y229	Y237
				D_5	Y6	Y14	Y22	~	Y222	Y230	Y238
				D_6	Y7	Y15	Y23	~	Y223	Y231	Y239
				D_7	Y8	Y16	Y24	~	Y224	Y232	Y240
L	H	Input	Output	D_0	Y240	Y232	Y224	~	Y24	Y16	Y8
				D_1	Y239	Y231	Y223	~	Y23	Y15	Y7
				D_2	Y238	Y230	Y222	~	Y22	Y14	Y6
				D_3	Y237	Y229	Y221	~	Y21	Y13	Y5
				D_4	Y236	Y228	Y220	~	Y20	Y12	Y4
				D_5	Y235	Y227	Y219	~	Y19	Y11	Y3
				D_6	Y234	Y226	Y218	~	Y18	Y10	Y2
				D_7	Y233	Y225	Y217	~	Y17	Y9	Y1

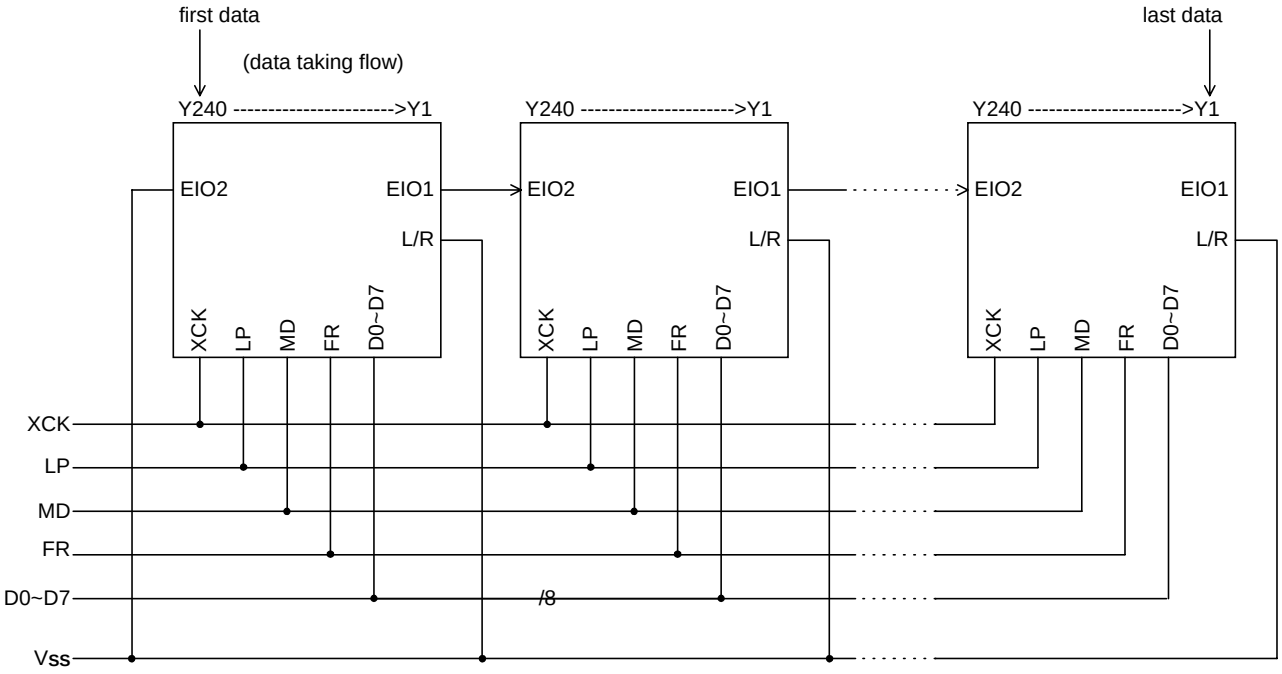
3.2. Common Mode

MD	L/R	Data Transfer Direction	EIO_1	EIO_2	D_7
L (Single)	L (shift to left)	Y240 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y240	Input	Output	X
H (Dual)	L (shift to left)	Y240 to Y121 Y120 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y120 Y121 to Y240	Input	Output	Input

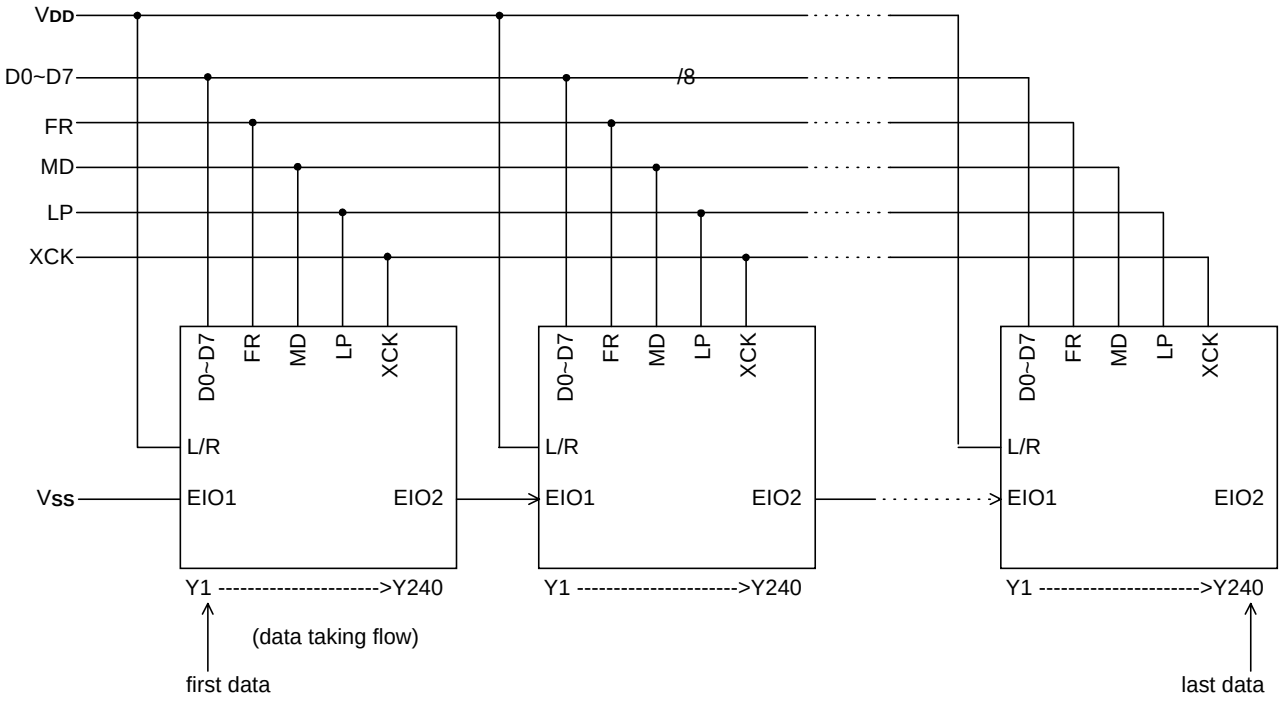
Here, L: V_{SS} (0V), H: V_{DD} (+2.5V to +5.5V), X: Don't care
Note: "Don't care" should be fixed to "H" or "L", avoiding floating.

4. Connection Examples of Segment Drivers

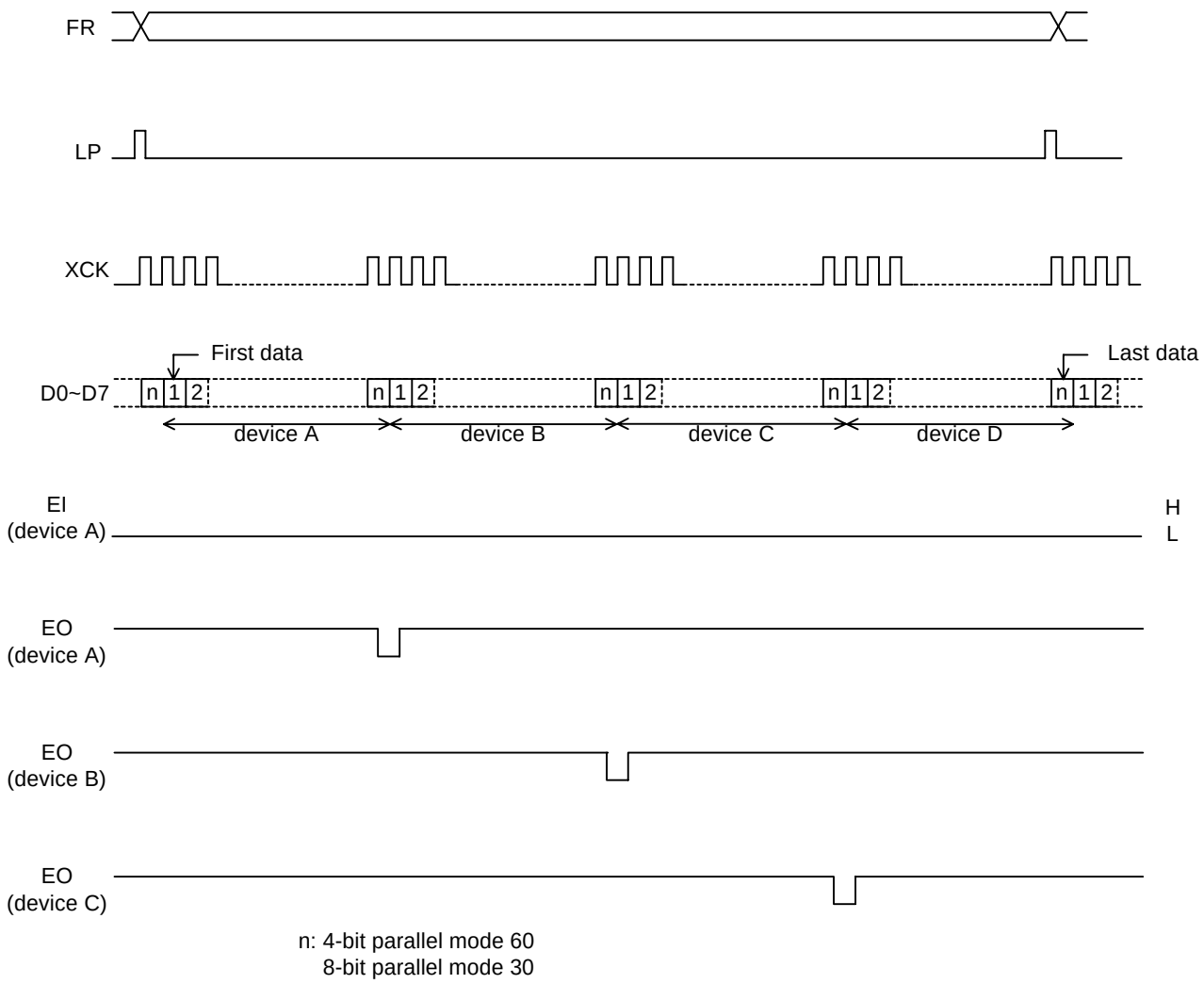
4.1. Case of L/R = “L”



4.2. Case of L/R = “H”

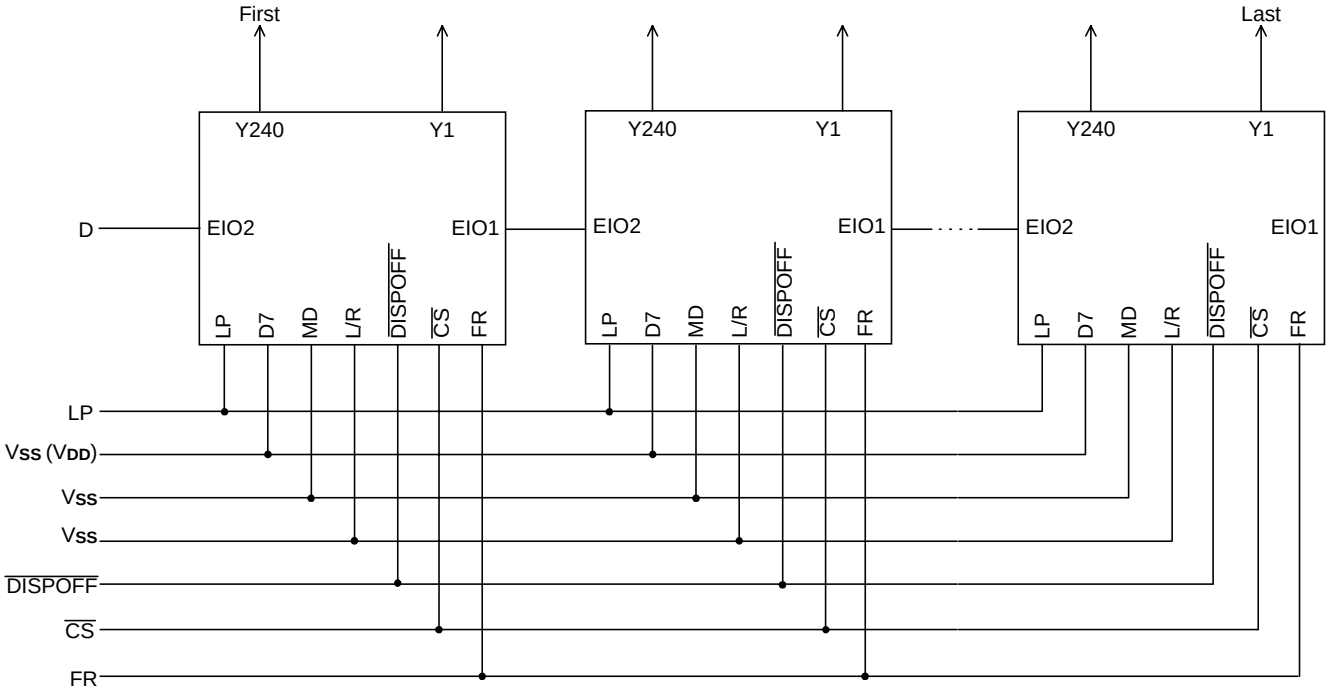


5. Timing waveform of 4-Device cascade Connection of Segment Drivers

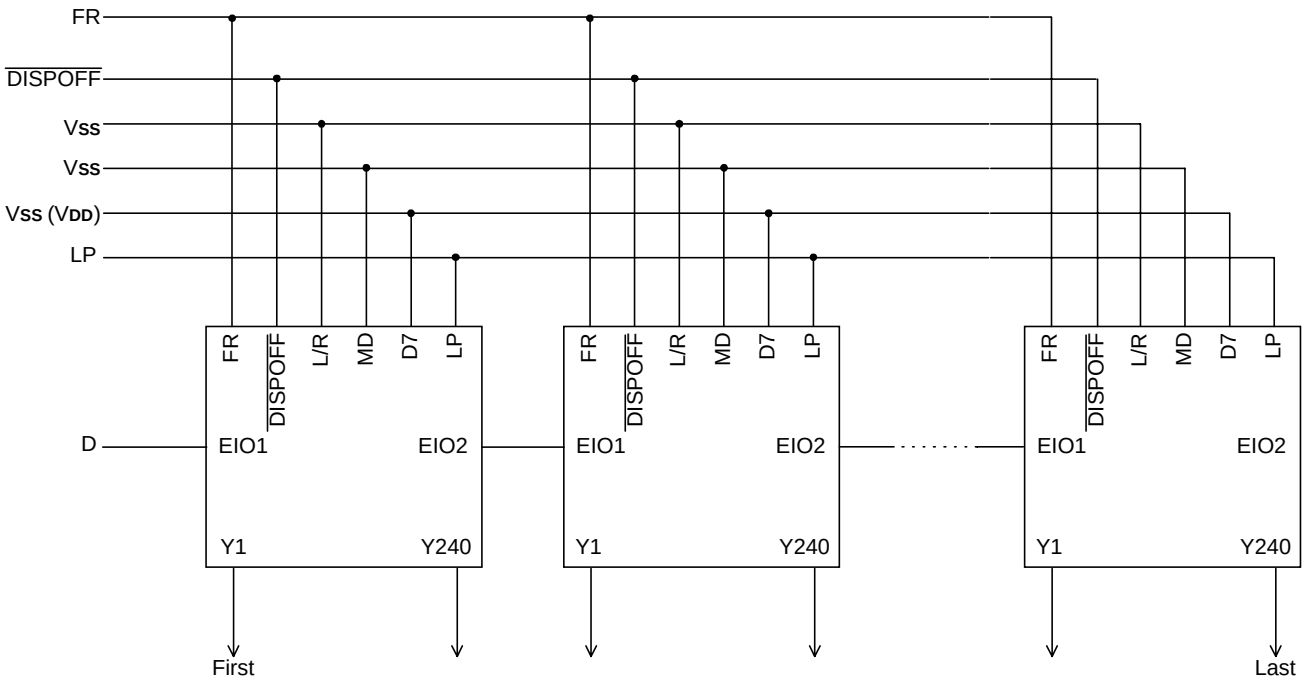


n: 4-bit parallel mode 60
8-bit parallel mode 30

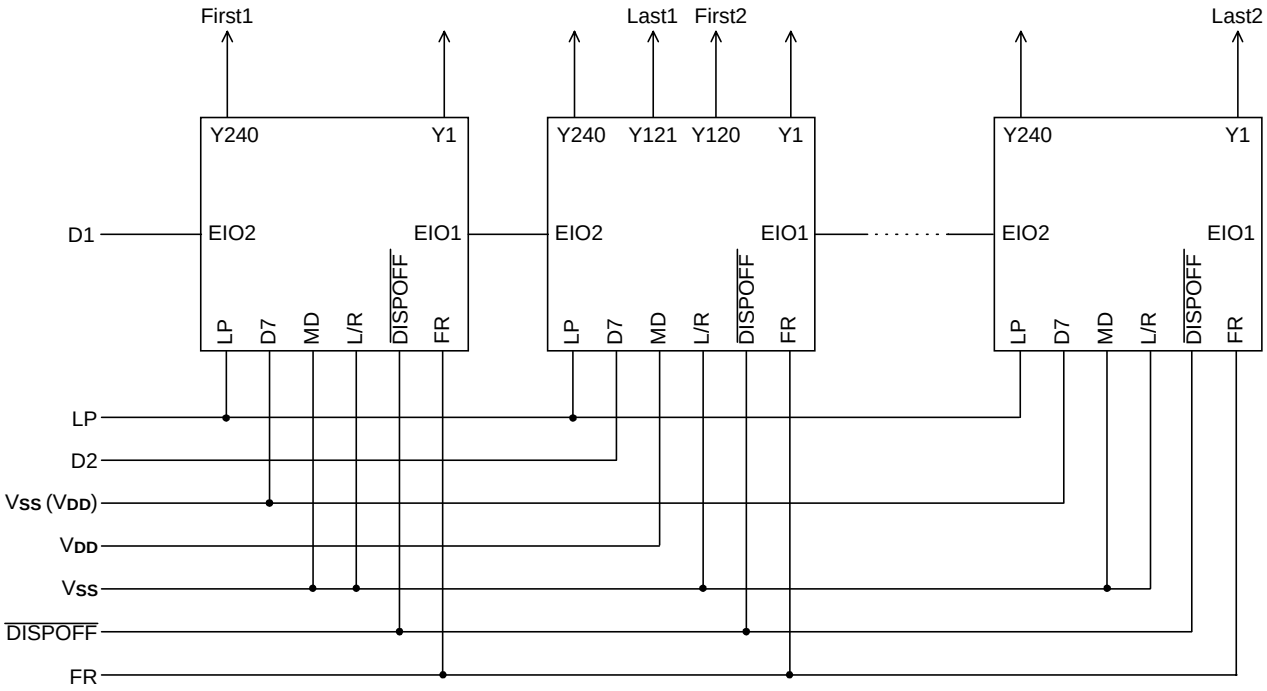
6. Connection Examples for Common Drivers



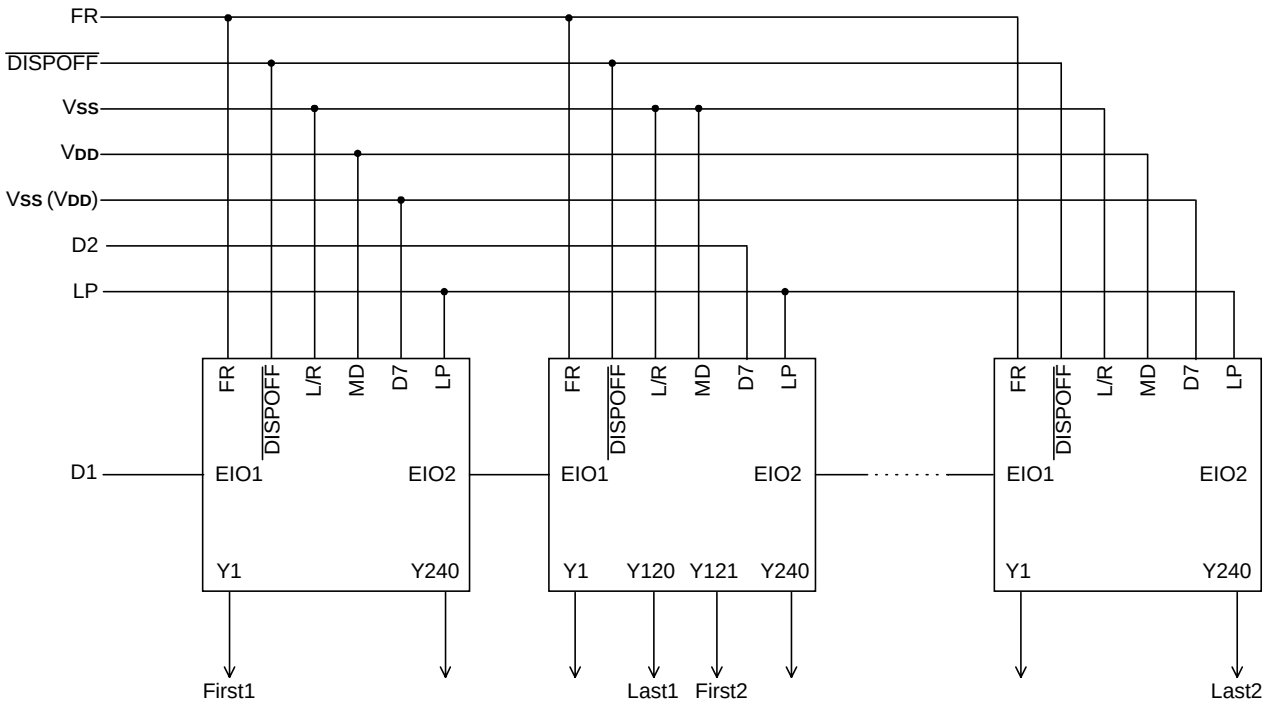
Single Mode (Shifting towards the left)



Single Mode (Sifting towards the right)



Dual mode (Shifting towards the left)



Dual mode (Shifting towards the right)

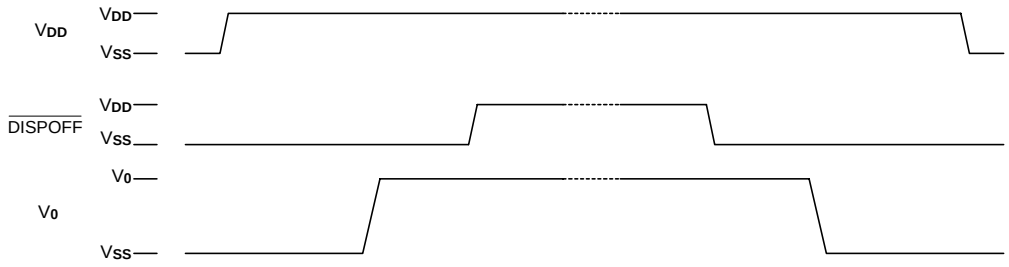
7. Precaution

Be careful when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occar, if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.
The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50-100 Ω) or fuse to the LCD driver power V_0 of the system as a current limiting device. Also, set a suitable value of the resistor in consideration of LCD display grade.

In addition, when connecting the logic power supply, the logic condition of this LSI inside is insecure. Therefore connect the LCD driver power supply after resetting the logic condition of this LSI inside to $\overline{\text{DISPOFF}}$ function. After that, the $\overline{\text{DISPOFF}}$ cancel the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level V_5 on the $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD driver power.
When connecting the power supply, follow the recommended sequence shown.



Absolute Maximum Rating*

DC Supply Voltage V_{DD} . . . . . -0.3V to +7.0V

DC Supply Voltage V_0 . . . . . -0.3V to +30V

Input Voltage . . . . . -0.3V to V_{DD} +0.3V

Operating Ambient Temperature . . . . -30°C to +85°C

Storage Temperature . . . . . .-45°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics

Segment Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30 V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Operating Voltage 1	V_{DD}	2.5	-	5.5	V		
Operating Voltage 2	V_0	15	-	30	V		
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins	
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V		
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA	
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA	
Input leakage current 1	I_{IH}	-	-	+1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins, V_I = V_{DD}	
Input leakage current 2	I_{IL}	-	-	-1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins, V_I = V_{SS}	
Output resistance	R_{ON}	-	1.5	2.0	kΩ	V0 = +30.0V	Y_1 - Y_{240} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	2.0	2.5		V0 = +20.0V	
Stand-by current	I_{SB}	-	-	10	μA	V_{SS} pin, Note 1	
Consumed current (1) (Deselection)	I_{DD1}	-	-	2	mA	V_{DD} pin, Note 2	
Consumed current (2) (Selection)	I_{DD2}	-	-	12	mA	V_{DD} pin, Note 3	
Consumed current	I_0	-	-	1.5	mA	V_0 pin, Note 4	

Note:

1. V_{DD} = +5.0V, V_0 = +30V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, No-load, EI = V_{DD}
   The input data is turned over by the data taking clock (4-bit Parallel input mode)
3. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, No-load. EI = V_{SS}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
4. V_{DD} = +5.0V, V_0 = +30V, f_{XCK} = 20MHz, f_{LP} = 41.6kHz. f_{FR} = 80 Hz, No-load
   The input data is turned over by the data taking clock (4-bit parallel-input mode)

Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30 V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Operating Voltage	V_{DD}	2.5	-	5.5	V		
Operating Voltage	V_0	15	-	30	V		
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$ pins	
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V		
Output high voltage	V_{OH}	V_{DD} - 0.4	-	-	V	EIO_1, EIO_2 pins, I_{OH} = -0.4mA	
Output low voltage	V_{OL}	-	-	+0.4	V	EIO_1, EIO_2 pins, I_{OL} = +0.4mA	
Input leakage current 1	I_{IH}	-	-	+10.0	µA	D0 - 6, LP, L/R, FR, MD, S/C and $\overline{DISPOFF}$ pins, V_I = V_{DD}	
Input leakage current 2	I_{IL}	-	-	-10.0	µA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2, $\overline{DISPOFF}$ pins, V_I = V_{SS}	
Input pull down current	I_{PD}	-	-	100	µA	XCK, EIO_1, EIO_2, D7 pins	
Output resistance	R_{ON}	-	1.5	2.0	kΩ	V0 = +30.0V	Y_1 - Y_{240} pins, $\lvert\Delta V_{ON}\rvert$ = 0.5V
		-	2.0	2.5		V0 = +20.0V	
Stand-by current	I_{SB}	-	-	75	µA	V_{SS} pin, Note 1	
Consumed current (1)	I_{DD}	-	-	120	µA	V_{DD} pin, Note 2	
Consumed current (2)	I_0	-	-	240	µA	V_0 pin, Note 2	

Note:

1. V_{DD} = +5.0V, V_0 = +30.0V, V_I = V_{SS}
2. V_{DD} = +5.0V, V_0 = +30.0V, f_{LP} = 41.6KHz, f_{FR} = 80Hz, case of 1/480 duty operation, No-load

AC Characteristics

Segment Mode 1 (V_{SS} = V_5 = 0V, V_{DD} = 4.5 - 5.5V, V_0 = 15 to 30V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	50	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	15	-		ns	
Shift clock "L" pulse width	t_{WCKL}	15	-		ns	
Data setup time	t_{DS}	10	-		ns	
Data hole time	t_{DH}	12	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	15	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	30	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	25	-		ns	
Latch pulse fall to Shift clock rise time	t_{LH}	25	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	10	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	30	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKII}-t_{wckl})/2 is the maximum in the case of high speed operation.

Segment Mode 2 (V_{SS} = V_5 = 0V, V_{DD} = 3.0 - 4.5V, V_0 = 15 to 30V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	66	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	23	-		ns	
Shift clock "L" pulse width	t_{WCKL}	23	-		ns	
Data setup time	t_{DS}	15	-		ns	
Data hole time	t_{DH}	23	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	30	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	50	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	30	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	30	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	41	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKII}-t_{WCKL})/2 is the maximum in the case of high speed operation.

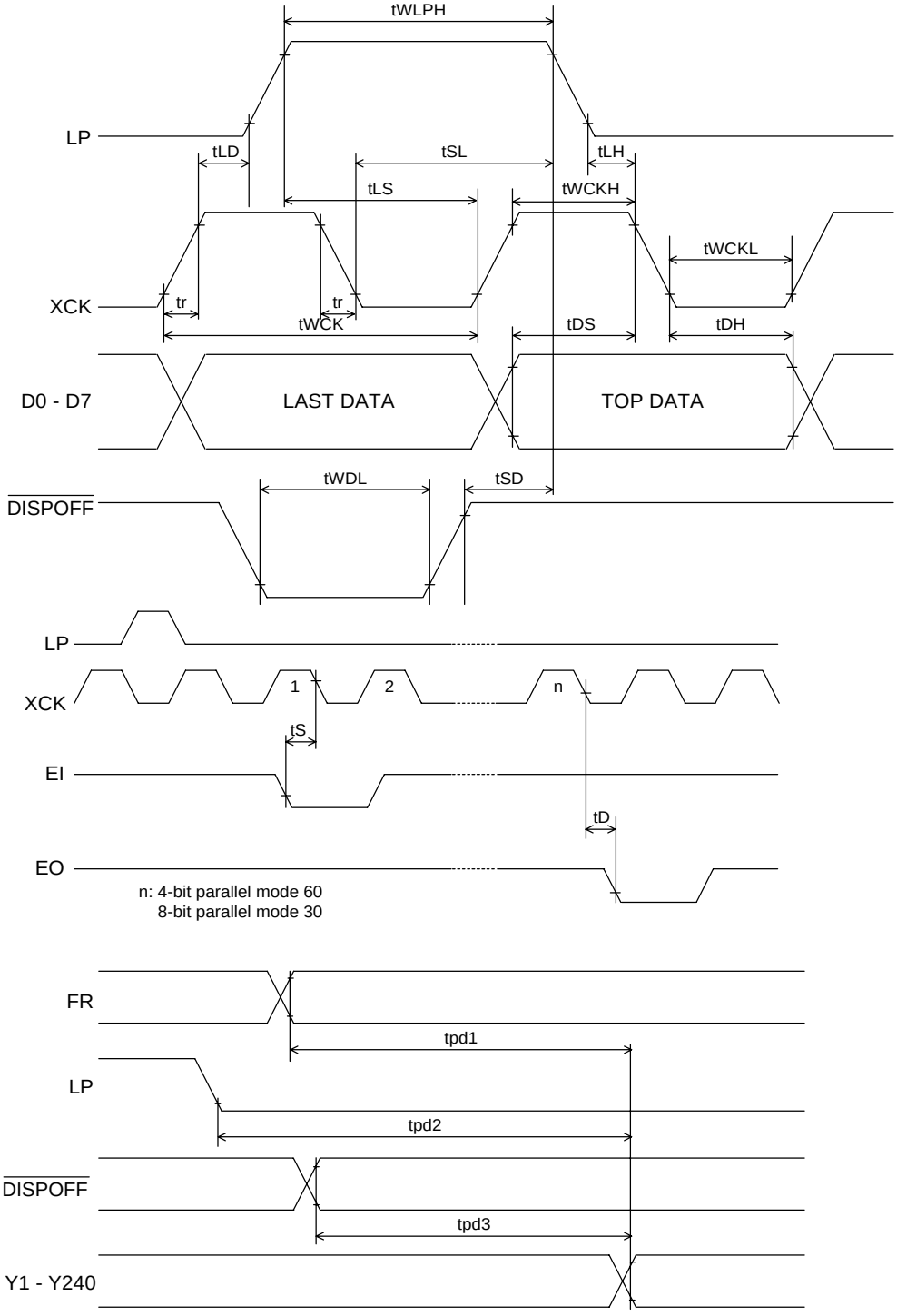
Segment Mode 3 (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 3.0V, V_0 = 15 to 30V, and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	82	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	28	-		ns	
Shift clock "L" pulse width	t_{WCKL}	28	-		ns	
Data setup time	t_{DS}	20	-		ns	
Data hole time	t_{DH}	23	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	30	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	65	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	30	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	30	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		μs	
Output delay time (1)	t_D		-	57	ns	CL = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t_{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKII}-t_{WCKL})/2 is the maximum in the case of high speed operation.

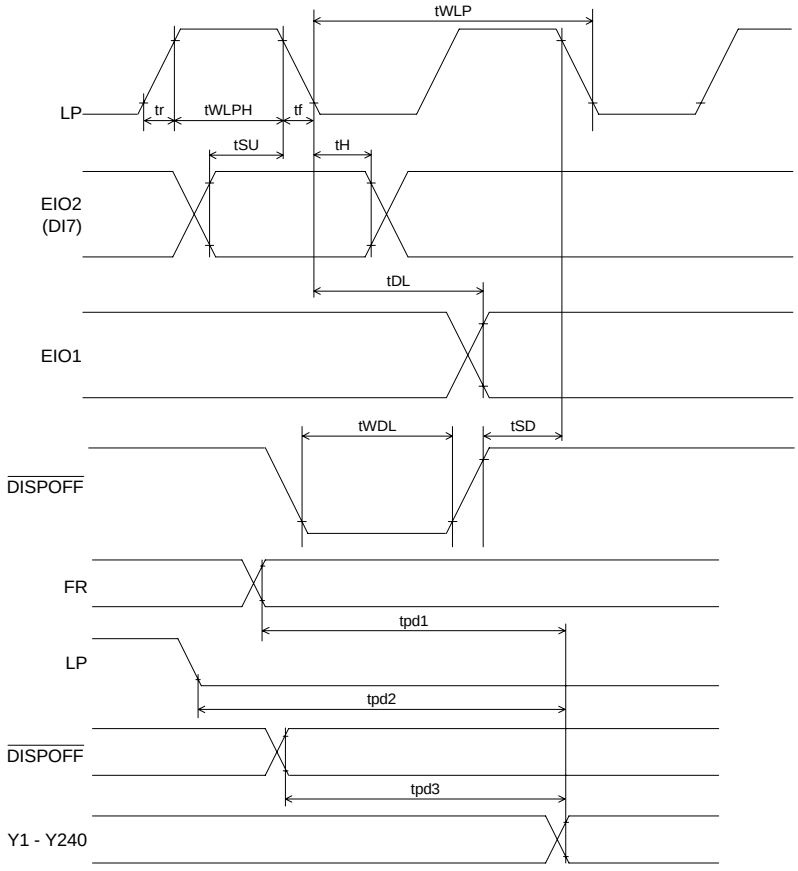
Timing waveform of the Segment Mode



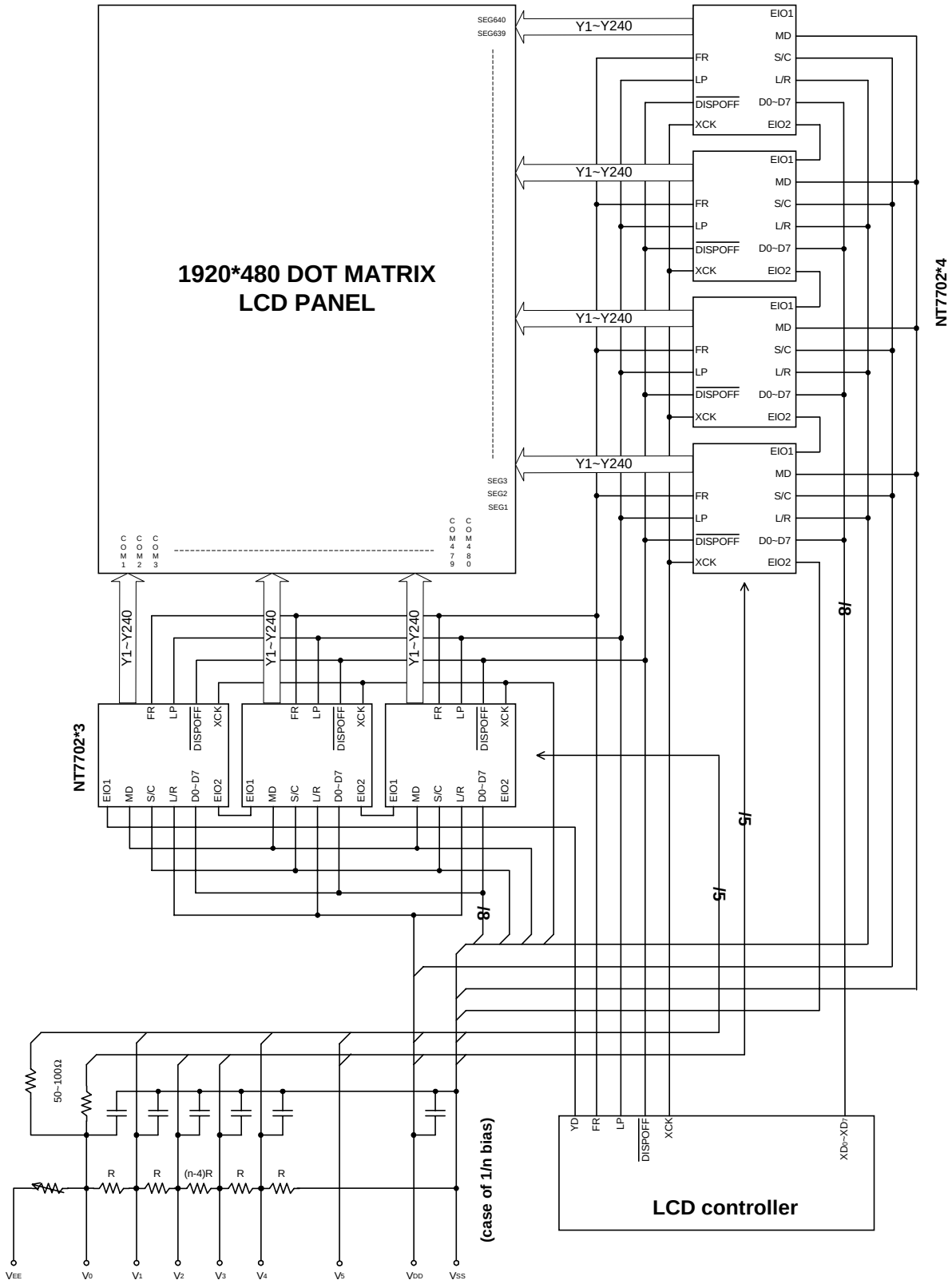
Common Mode (V_{SS} = V_5 = 0V, V_{DD} = 2.5 - 5.5V, V_0 = 15 to 30V and T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WLP}	250	-	-	ns	t_r, t_f ≦ 20ns
Shift clock "H" pulse width	t_{WLPH}	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	t_{SU}	30	-	-	ns	
Data hole time	t_H	50	-	-	ns	
Input signal rise time	t_r		-	50	ns	
Input signal fall time	t_f		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-	-	µs	
Output delay time (1)	t_{DL}	-	-	200	ns	C_L = 15pF
Output delay time (2)	t_{pd1}, t_{pd2}	-	-	1.2	µs	C_L = 15pF
Output delay time (3)	t_{pd3}	-	-	1.2	µs	C_L = 15pF

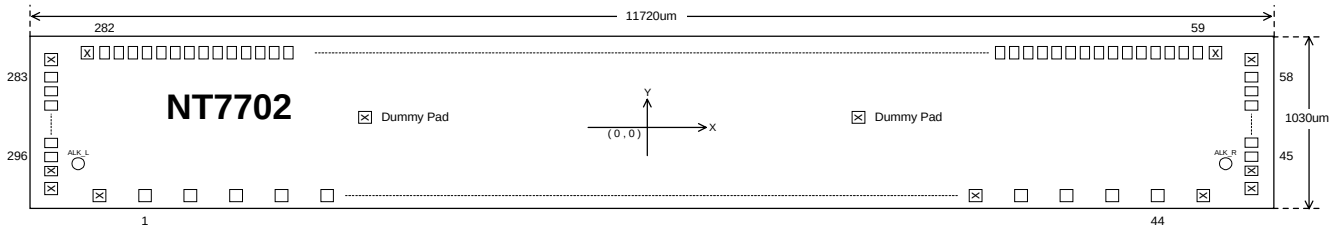
Timing Characteristics of Common Mode



Application Circuit (for reference only)



Bonding Diagram



Pad Location

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	V5L	-5440	-440	31	LP	1440	-440
2	V5L	-5280	-440	32	LP	1600	-440
3	VSS	-5120	-440	33	EIO1	1760	-440
4	VSS	-4960	-440	34	EIO1	1920	-440
5	VDD	-4800	-440	35	FR	2080	-440
6	VDD	-4640	-440	36	FR	2240	-440
7	SC	-2400	-440	37	L/R	2400	-440
8	SC	-2240	-440	38	L/R	2560	-440
9	EIO2	-2080	-440	39	MD	2720	-440
10	EIO2	-1920	-440	40	MD	2880	-440
11	D0	-1760	-440	41	VSS	4960	-440
12	D0	-1600	-440	42	VSS	5120	-440
13	D1	-1440	-440	43	V5R	5280	-440
14	D1	-1280	-440	44	V5R	5440	-440
15	D2	-1120	-440	45	V43R	5779	-300
16	D2	-960	-440	46	V43R	5779	-250
17	D3	-800	-440	47	V12R	5779	-200
18	D3	-640	-440	48	V12R	5779	-150
19	D4	-480	-440	49	V0R	5779	-100
20	D4	-320	-440	50	V0R	5779	-50
21	D5	-160	-440	51	Y1	5779	0
22	D5	0	-440	52	Y2	5779	50
23	D6	160	-440	53	Y3	5779	100
24	D6	320	-440	54	Y4	5779	150
25	D7	480	-440	55	Y5	5779	200
26	D7	640	-440	56	Y6	5779	250
27	XCK	800	-440	57	Y7	5779	300
28	XCK	960	-440	58	Y8	5779	350
29	$\overline{\text{DISPOFF}}$	1120	-440	59	Y9	5575	440
30	$\overline{\text{DISPOFF}}$	1280	-440	60	Y10	5525	440

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	Y11	5475	440	101	Y51	3475	440
62	Y12	5425	440	102	Y52	3425	440
63	Y13	5375	440	103	Y53	3375	440
64	Y14	5325	440	104	Y54	3325	440
65	Y15	5275	440	105	Y55	3275	440
66	Y16	5225	440	106	Y56	3225	440
67	Y17	5175	440	107	Y57	3175	440
68	Y18	5125	440	108	Y58	3125	440
69	Y19	5075	440	109	Y59	3075	440
70	Y20	5025	440	110	Y60	3025	440
71	Y21	4975	440	111	Y61	2975	440
72	Y22	4925	440	112	Y62	2925	440
73	Y23	4875	440	113	Y63	2875	440
74	Y24	4825	440	114	Y64	2825	440
75	Y25	4775	440	115	Y65	2775	440
76	Y26	4725	440	116	Y66	2725	440
77	Y27	4675	440	117	Y67	2675	440
78	Y28	4625	440	118	Y68	2625	440
79	Y29	4575	440	119	Y69	2575	440
80	Y30	4525	440	120	Y70	2525	440
81	Y31	4475	440	121	Y71	2475	440
82	Y32	4425	440	122	Y72	2425	440
83	Y33	4375	440	123	Y73	2375	440
84	Y34	4325	440	124	Y74	2325	440
85	Y35	4275	440	125	Y75	2275	440
86	Y36	4225	440	126	Y76	2225	440
87	Y37	4175	440	127	Y77	2175	440
88	Y38	4125	440	128	Y78	2125	440
89	Y39	4075	440	129	Y79	2075	440
90	Y40	4025	440	130	Y80	2025	440
91	Y41	3975	440	131	Y81	1975	440
92	Y42	3925	440	132	Y82	1925	440
93	Y43	3875	440	133	Y83	1875	440
94	Y44	3825	440	134	Y84	1825	440
95	Y45	3775	440	135	Y85	1775	440
96	Y46	3725	440	136	Y86	1725	440
97	Y47	3675	440	137	Y87	1675	440
98	Y48	3625	440	139	Y88	1625	440
99	Y49	3575	440	139	Y89	1575	440
100	Y50	3525	440	140	Y90	1525	440

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	Y91	1475	440	181	Y131	-525	440
142	Y92	1425	440	182	Y132	-575	440
143	Y93	1375	440	183	Y133	-625	440
144	Y94	1325	440	184	Y134	-675	440
145	Y95	1275	440	185	Y135	-725	440
146	Y96	1225	440	186	Y136	-775	440
147	Y97	1175	440	187	Y137	-825	440
148	Y98	1125	440	188	Y138	-875	440
149	Y99	1075	440	189	Y139	-925	440
150	Y100	1025	440	190	Y140	-975	440
151	Y101	975	440	191	Y141	-1025	440
152	Y102	925	440	192	Y142	-1075	440
153	Y103	875	440	193	Y143	-1125	440
154	Y104	825	440	194	Y144	-1175	440
155	Y105	775	440	195	Y145	-1225	440
156	Y106	725	440	196	Y146	-1275	440
157	Y107	675	440	197	Y147	-1325	440
158	Y108	625	440	198	Y148	-1375	440
159	Y109	575	440	199	Y149	-1425	440
160	Y110	525	440	200	Y150	-1475	440
161	Y111	475	440	201	Y151	-1525	440
162	Y112	425	440	202	Y152	-1575	440
163	Y113	375	440	203	Y153	-1625	440
164	Y114	325	440	204	Y154	-1675	440
165	Y115	275	440	205	Y155	-1725	440
166	Y116	225	440	206	Y156	-1775	440
167	Y117	175	440	207	Y157	-1825	440
168	Y118	125	440	208	Y158	-1875	440
169	Y119	75	440	209	Y159	-1925	440
170	Y120	25	440	210	Y160	-1975	440
171	Y121	-25	440	211	Y161	-2025	440
172	Y122	-75	440	212	Y162	-2075	440
173	Y123	-125	440	213	Y163	-2125	440
174	Y124	-175	440	214	Y164	-2175	440
175	Y125	-225	440	215	Y165	-2225	440
176	Y126	-275	440	216	Y166	-2275	440
177	Y127	-325	440	217	Y167	-2325	440
178	Y128	-375	440	218	Y168	-2375	440
179	Y129	-425	440	219	Y169	-2425	440
180	Y130	-475	440	220	Y170	-2475	440

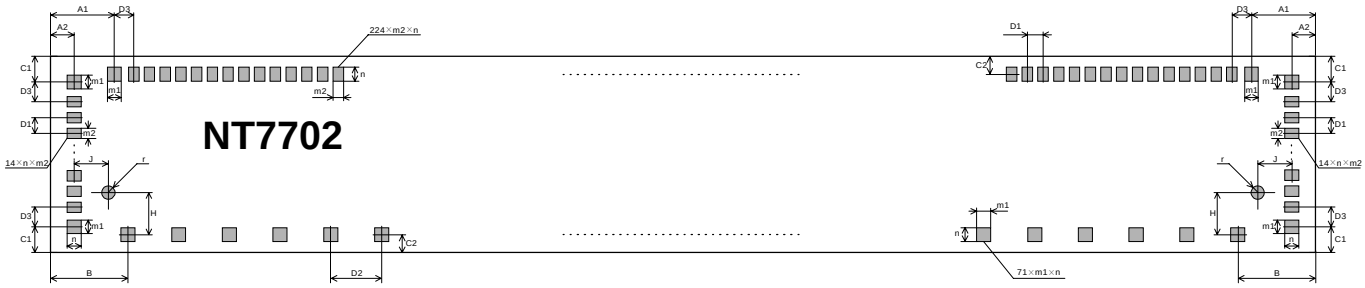
Pad Location (continued)

Pad No.	Designation	X	Y
221	Y171	-2525	440
222	Y172	-2575	440
223	Y173	-2625	440
224	Y174	-2675	440
225	Y175	-2725	440
226	Y176	-2775	440
227	Y177	-2825	440
228	Y178	-2875	440
229	Y179	-2925	440
230	Y180	-2975	440
231	Y181	-3025	440
232	Y182	-3075	440
233	Y183	-3125	440
234	Y184	-3175	440
235	Y185	-3225	440
236	Y186	-3275	440
237	Y187	-3325	440
238	Y188	-3375	440
239	Y189	-3425	440
240	Y190	-3475	440
241	Y191	-3525	440
242	Y192	-3575	440
243	Y193	-3625	440
244	Y194	-3675	440
245	Y195	-3725	440
246	Y196	-3775	440
247	Y197	-3825	440
248	Y198	-3875	440
249	Y199	-3925	440
250	Y200	-3975	440
251	Y201	-4025	440
252	Y202	-4075	440
253	Y203	-4125	440
254	Y204	-4175	440
255	Y205	-4225	440
256	Y206	-4275	440
257	Y207	-4325	440
258	Y208	-4375	440
259	Y209	-4425	440
260	Y210	-4475	440
261	Y211	-4525	440
262	Y212	-4575	440
263	Y213	-4625	440
264	Y214	-4675	440
265	Y215	-4725	440
266	Y216	-4775	440
267	Y217	-4825	440
268	Y218	-4875	440
269	Y219	-4925	440
270	Y220	-4975	440
271	Y221	-5025	440
272	Y222	-5075	440
273	Y223	-5125	440
274	Y224	-5175	440
275	Y225	-5225	440
276	Y226	-5275	440
277	Y227	-5325	440
278	Y228	-5375	440
279	Y229	-5425	440
280	Y230	-5475	440
281	Y231	-5525	440
282	Y232	-5575	440
283	Y233	-5779	350
284	Y234	-5779	300
285	Y235	-5779	250
286	Y236	-5779	200
287	Y237	-5779	150
288	Y238	-5779	100
289	Y239	-5779	50
290	Y240	-5779	0
291	V0L	-5779	-50
292	V0L	-5779	-100
293	V12L	-5779	-150
294	V12L	-5779	-200
295	V43L	-5779	-250
296	V43L	-5779	-300
	ALK_R	5668	-323
	ALK_L	-5668	-323

Dummy Pad Location (Total: 35 pad)

NO	X	Y	NO	X	Y	NO	X	Y	NO	X	Y
1	-5600	-440	10	-3200	-440	19	3680	-440	28	5779	-410
2	-4480	-440	11	-3040	-440	20	3840	-440	29	5779	-350
3	-4320	-440	12	-2880	-440	21	4000	-440	30	5779	410
4	-4160	-440	13	-2720	-440	22	4160	-440	31	5635	440
5	-4000	-440	14	-2560	-440	23	4320	-440	32	-5635	440
6	-3840	-440	15	3040	-440	24	4480	-440	33	-5779	410
7	-3680	-440	16	3200	-440	25	4640	-440	34	-5779	-350
8	-3520	-440	17	3360	-440	26	4800	-440	35	-5779	-410
9	-3360	-440	18	3520	-440	27	5600	-440			

Package Information

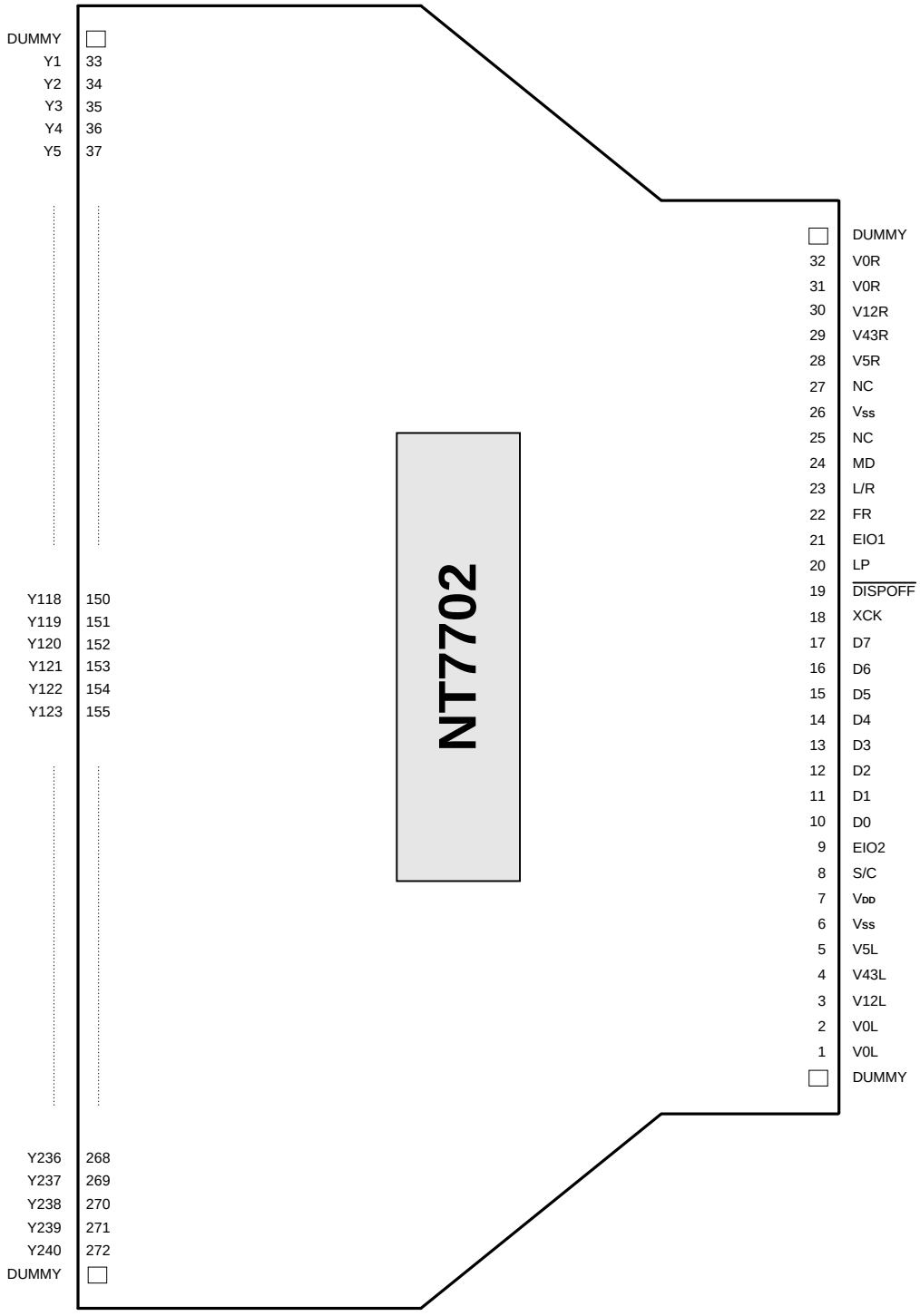


Chip Outline Dimensions

unit: um

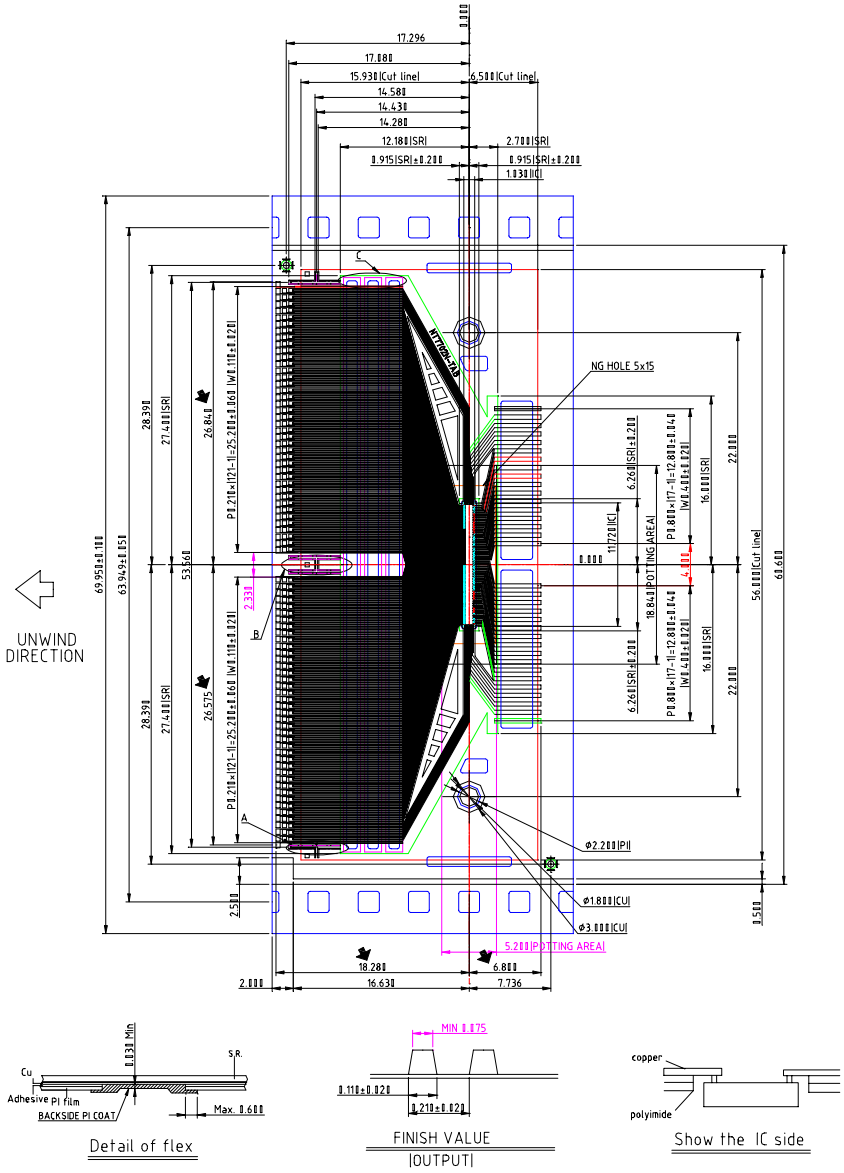
Symbol	Dimensions in um	Symbol	Dimensions in um
A1	225	D3	60
A2	81	m1	57
B	260	m2	37
C1	105	n	59
C2	75	r	35
D1	50	H	117
D2	160	J	111

TCP Pin Layout



(Copper Side View)

External view of TCP pins



COPPER VIEW

NOTE:

1.GENERAL TOLERANCE: ±0.050MM

2.ALL CHAMFER IS R0.200

3.MATERIAL

PI: UPILEX-S 75±6umTHICKNESS

ADHESIVE: TORAY #7100 12±2um THICKNESS

CU: MITSUI 1/2 OZ

FLEX COATING: FS-100L

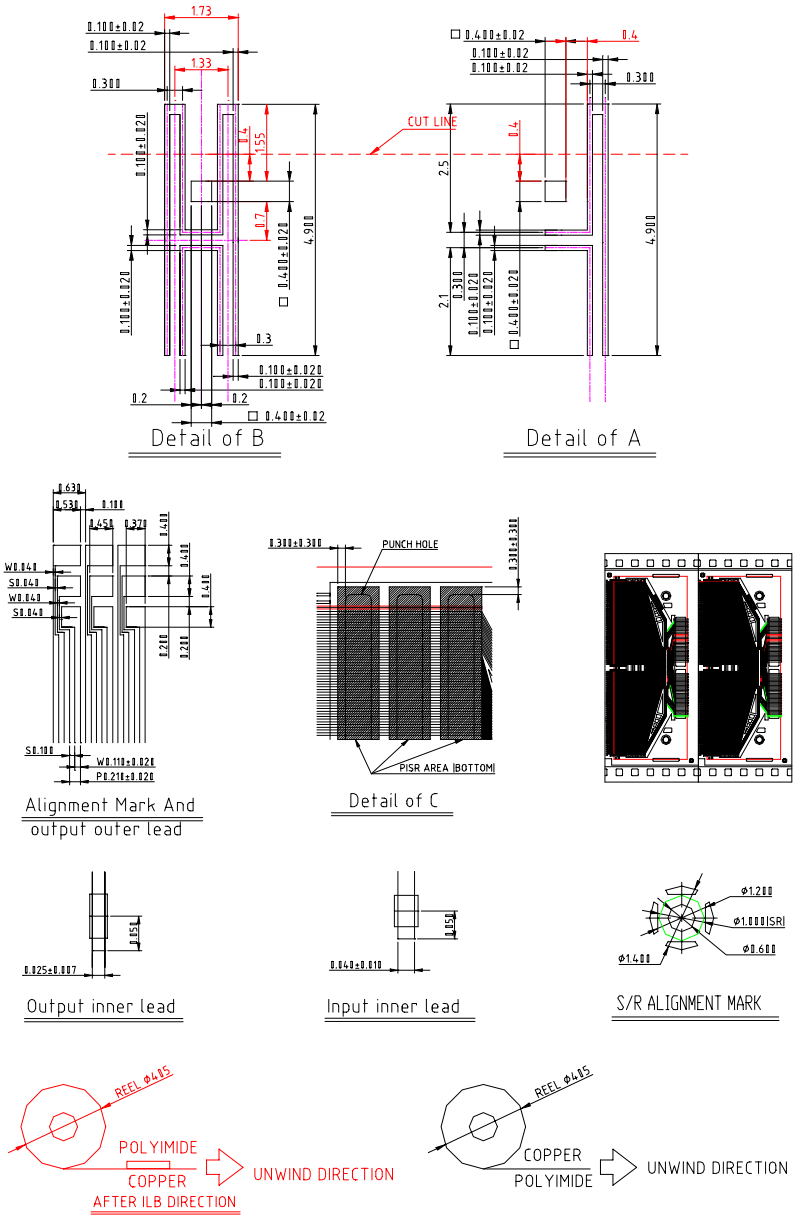
SOLDER RESIST :AE-70-M11 20±15um

OTHER TOLERANCE IS±0.300

4.PLATING

SN: 0.15±0.05um

5. 6 SPROCKET HOLES(28.5mm) FOR 1 TAPESITE



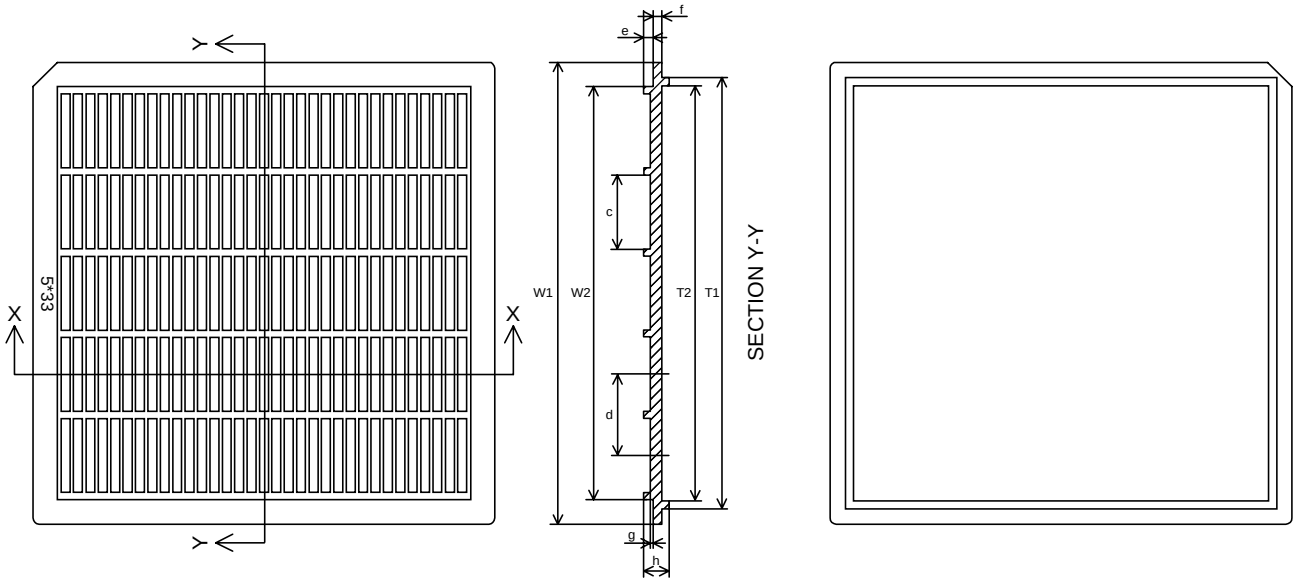
Cautions concerning storage:

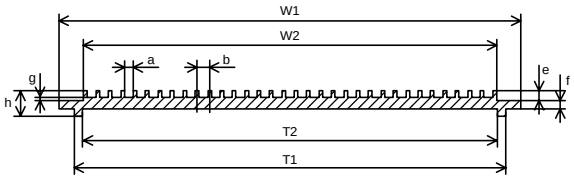
1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions :

Storage state	Storage conditions
unopened **(less than 90 days)**	Temperature: 5 to 30℃; humidity: 80%RH or less.
After seal of broken **(less than 30 days)**	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it is subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

Tray Information





SECTION X-X

Symbol	Dimensions in mm	Symbol	Dimensions in mm
a	1.46	g	0.84
b	2.04	h	4.20
c	12.14	W1	76.0
d	13.35	W2	68.0
e	1.60	T1	71.0
f	1.40	T2	68.3

Ordering Information

Part No.	Package
NT7702H-BDT	Au bump on chip tray
NT7702H-TABF4	TCP Form