

OTM3225C

**720-channel 6-bit source driver and
320-channel gate driver
with System-On-Chip (SOC) for color
amorphous TFT LCD**

Preliminary

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720-channel 6-bit source driver and 320-channel gate driver with System-On-Chip (SOC) for color amorphous TFT LCD

1. GENERAL DESCRIPTION

The OTM3225C, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 240xRGBx320 in resolution which can be achieved by the designated RAM for graphic data. The 720-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The OTM3225C is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

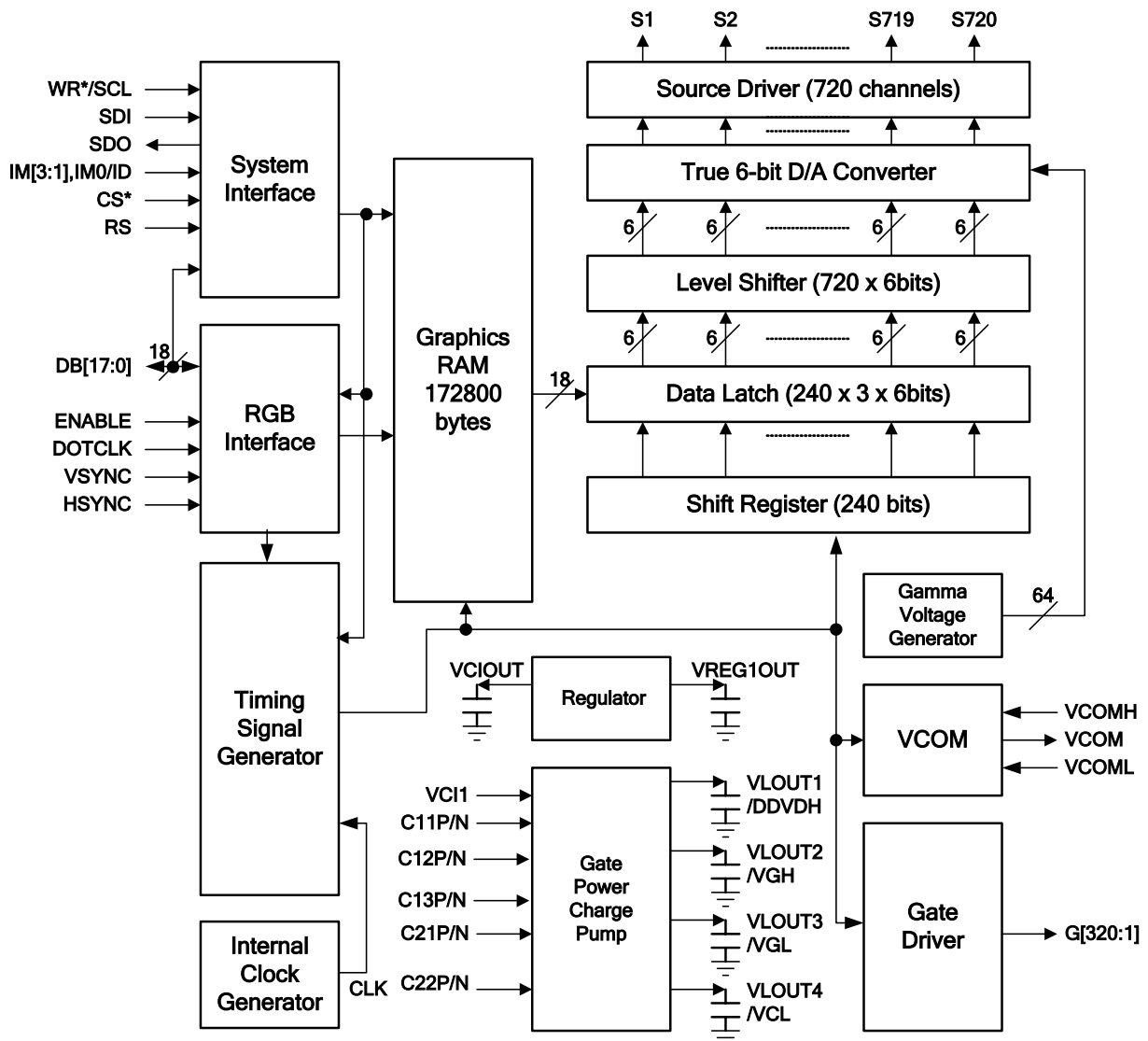
The built-in timing controller in OTM3225C can support several interfaces for the diverse request of medium or small size portable display. OTM3225C provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the OTM3225C incorporates 6, 8, 16, and 18-bit RGB interfaces for picture movement display. The OTM3225C also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURE

- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 240xRGBx320, incorporating a 720-channel source driver and a 320-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 172800 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
 - Intel 80-system with 8-, 9-, 16-, and 18-bit parallel ports
 - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
 - 6-, 8-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
 - Window address function to display at any area on the screen via a moving picture display interface
 - Window address function to limit the data rewriting area and reduce data transfer
 - Moving and still picture can display at the same time
 - Vertical scrolling function
 - Partial screen display
- Power supply
 - I/O interface supply voltage (IOVCC): 1.65 ~ 3.3 V
 - Analog power supply voltage (VCI): 2.5 ~ 3.3 V
- Resize function(x 1/2, x 1/4)
- On-chip power management system
 - Power saving mode (standby / 8-color mode, etc)
 - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
 - Source driver voltage level: DDVDH-GND=4.5V ~ 6V.
 - Gate driver voltage level (VGH, VGL)
 - VGH = 10.0V ~20.0V
 - VGL = -4.5V ~ -16.5V
 - VGH – VGL < 30.0V
 - Built-in internal oscillator and hardware reset

3. BLOCK DIAGRAM

3.1. Block Function



3.2. System Interface

3.2.1. Interface

The OTM3225C supports two kinds of system interfaces:

Intel 80-system interfaces with 8-, 9-, 16-, 18-bits parallel port.

1. Serial Peripheral Interface (SPI).

The OTM3225C has a 16-bit index register (IR) and two 18-bit data registers; a write-data register (WDR) and a read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM or control register.

When graphic data is written to the internal GRAM from MCU's graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the OTM3225C executes the 1st read operation. Thus, valid data can be read out after the OTM3225C executes the 2nd read operation.

3.2.2. External Display Interface

The OTM3225C supports external RGB interface for picture movement display.

The OTM3225C allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (ENABLE) enabling.

3.2.3. Address Counter (AC)

OTM3225C features an Address Counter (AC) giving an address

to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

3.2.4. Graphics RAM (GRAM)

OTM3225C features a 172800-byte (240 x 320 x 18 / 8) Graphic RAM (GRAM).

3.2.5. Grayscale Voltage Generating Circuit

OTM3225C has true 6-bit resolution D/A converter, which generates 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ -correction register.

3.2.6. Timing Controller

OTM3225C has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, RAM accessing timing, etc.

3.2.7. Oscillator (OSC)

The OTM3225C also features an internal oscillator to generate RC oscillation with an internal resistor. In standby mode, RC oscillation is halted to reduce power consumption.

3.2.8. Source Driver Circuit

OTM3225C consists of a 720-output source driver circuit (S1 ~ S720). Data in the GRAM are latched when the 720th bit data is input. The latched data controls the source driver and generates a drive waveform.

3.2.9. Gate Driver Circuit

OTM3225C consists of a 320-output gate driver circuit (G1~G320). The gate driver circuit outputs gate driver signals at either VGH or VGL level.

3.2.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels DDVDH, VGH, VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

4. SIGNAL DESCRIPTIONS

Signal	I/O	Connected with	Function																																																																																																																
System Configuration Input Signal																																																																																																																			
IM3~1, IM0/ID	I	GND/ IOVCC	Select an interface mode to MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.																																																																																																																
			<table border="1"> <thead> <tr> <th>IM3</th> <th>IM2</th> <th>IM1</th> <th>IM0/ID</th> <th>Interface Mode</th> <th>DB Pin</th> <th>Colors</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>80-system 16-bit interface</td> <td>DB17-10, DB8-1</td> <td>262,144 or 65,536</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>80-system 8-bit interface</td> <td>DB17-10</td> <td>262,144 or 65,536</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>*(ID)</td> <td>Clock synchronous serial interface</td> <td>-</td> <td>262,144 or 65,536</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>80-system 18-bit interface</td> <td>DB17-0</td> <td>262,144 only</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>80-system 9-bit interface</td> <td>DB17-9</td> <td>262,144 only</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>Setting disabled</td> <td>-</td> <td>-</td> </tr> </tbody> </table>	IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin	Colors	0	0	0	0	Setting disabled	-	-	0	0	0	1	Setting disabled	-	-	0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144 or 65,536	0	0	1	1	80-system 8-bit interface	DB17-10	262,144 or 65,536	0	1	0	*(ID)	Clock synchronous serial interface	-	262,144 or 65,536	0	1	1	0	Setting disabled	-	-	0	1	1	1	Setting disabled	-	-	1	0	0	0	Setting disabled	-	-	1	0	0	1	Setting disabled	-	-	1	0	1	0	80-system 18-bit interface	DB17-0	262,144 only	1	0	1	1	80-system 9-bit interface	DB17-9	262,144 only	1	1	0	0	Setting disabled	-	-	1	1	0	1	Setting disabled	-	-	1	1	1	0	Setting disabled	-	-	1	1	1	1	Setting disabled	-	-
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/RESET	I	MPU	RESET pin. This is an active low signal.																																																																																																																
Interface input Signals																																																																																																																			
/CS	I	MPU	Chip select signal. Low: the OTM3225C is accessible. High: the OTM3225C is not accessible. Must connect to MPU.																																																																																																																
RS	I	MPU	Register select signal. Low: Index register or internal status is selected. High: Control register is selected. Must connect to the GND or IOVCC level when not used.																																																																																																																
(/WR) / (SCL)	I	MPU	(A) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low. (B) In SPI mode, served as a synchronizing clock signal.																																																																																																																
/RD	I	MPU	In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. Must connect to the GND or IOVCC level when not in use.																																																																																																																
SDI	I	MPU	Serial Data is the input on the rising edge of the SCL signal in SPI mode. Must connect to the GND or IOVCC level when not in use.																																																																																																																
SDO	O	MPU	Serial Data is the output on the rising edge of the SCL signal in SPI mode. Must keep this pin open (floating) when not used. Can not connect to the GND or IOVCC level when not in use.																																																																																																																

Signal	I/O	Connected with	Function																				
DB0-DB17	I/O	MPU	<p>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:</p> <table border="1"> <thead> <tr> <th>Mode</th> <th>Pin Assignment</th> </tr> </thead> <tbody> <tr> <td>8-bit system interface</td> <td>DB17-DB10</td> </tr> <tr> <td>9-bit system interface</td> <td>DB17-DB9</td> </tr> <tr> <td>16-bit system interface</td> <td>DB17-DB10, DB8-DB1</td> </tr> <tr> <td>18-bit system interface</td> <td>DB17-DB0</td> </tr> <tr> <td>6-bit External (RGB) interface</td> <td>DB17-DB12</td> </tr> <tr> <td>8-bit External (RGB) interface</td> <td>DB17-DB10</td> </tr> <tr> <td>16-bit External (RGB) interface</td> <td>DB17-13, DB11-DB1</td> </tr> <tr> <td>18-bit External (RGB) interface</td> <td>DB17-DB0</td> </tr> <tr> <td>Serial interface(SPI)</td> <td>Not use</td> </tr> </tbody> </table> <p>Must connect to the GND or IOVCC level when not in use.</p>	Mode	Pin Assignment	8-bit system interface	DB17-DB10	9-bit system interface	DB17-DB9	16-bit system interface	DB17-DB10, DB8-DB1	18-bit system interface	DB17-DB0	6-bit External (RGB) interface	DB17-DB12	8-bit External (RGB) interface	DB17-DB10	16-bit External (RGB) interface	DB17-13, DB11-DB1	18-bit External (RGB) interface	DB17-DB0	Serial interface(SPI)	Not use
Mode	Pin Assignment																						
8-bit system interface	DB17-DB10																						
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6-bit External (RGB) interface	DB17-DB12																						
8-bit External (RGB) interface	DB17-DB10																						
16-bit External (RGB) interface	DB17-13, DB11-DB1																						
18-bit External (RGB) interface	DB17-DB0																						
Serial interface(SPI)	Not use																						
VSYNC	I	MPU	<p>In external RGB interface mode, served as a vertical synchronize signal input Must connect to the IOVCC or GND level when not in use.</p>																				
HSYNC	I	MPU	<p>In external RGB interface mode, served as a horizontal synchronized signal input Must connect to the IOVCC or GND level when not used.</p>																				
ENABLE	I	MPU	<p>In external RGB interface mode, polarity of ENABLE signal is synchronized with valid graphic data input. Low: Valid data on DB17-DB0 (relative to different interface modes) High: Invalid data on DB17-DB0 (relative to different interface modes) Moreover, setting EPL bit can change the polarity of the ENABLE signal. Must connect to the GND or IOVCC level when not in use.</p>																				
DOTCLK	I	MPU	<p>In external RGB interface mode, served as a dot clock signal. When DPL = "0": Input data on the rising edge of DOTCLK When DPL = "1": Input data on the falling edge of DOTCLK It is fixed to the IOVCC or GND level when not in use.</p>																				
FMARK	O	MPU	<p>Frame head pulse signal, which is used when writing data to the internal RAM. Must keep this pin open(floating) when not used. Can not connect to the GND or IOVCC level when not in use.</p>																				
Charge Pump and Power Supply Signal																							
C11P/N, C12P/N C13P/N C21P/N, C22P/N	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins.																				
VC11	I/O	Stabilizing capacitor	Reference voltage of step-up circuit 1. Make sure the output voltage levels from DDVDH, VGH, and VGL do not exceed the respective setting ranges.																				
DDVDH	I	Stabilizing capacitor	Power supply for the source driver liquid crystal drive unit and VCOM drive. DDVDH = 4.5V ~ 6.0V																				
VGH	I	Stabilizing capacitor	Liquid crystal driving power supply.																				
VGL	I	Stabilizing capacitor	Liquid crystal driving power supply.																				
VCL	O	Stabilizing capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = -1.9V ~ -3.0V																				

Signal	I/O	Connected with	Function
LEDPWM/ TESTO1	O	LED Driver	Output PWM signal, which control LED driver for backlight dimming. Must connect to the GND level or Open (floating) when not in use.
LEDON/ TESTO2	O	LED Driver	Output control signal for turn ON/OFF LED backlight. Must connect to the GND level or Open (floating) when not in use.
Source/Gate Driver and VCOM Signals			
G1~G320	O	LCD	Output gate driver signals, which has the swing from VGH to VGL
S1~S720	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage are output.
VREG1OUT	O	Stabilizing capacitor	Output voltage generated from the reference voltage (VCI or VCIR). The factor is determined by instruction (VRH bits). VREG1OUT is used for : (1) Source driver grayscale reference voltage (2) VCOMH level reference voltage (3) VCOM amplitude reference voltage Connect to a stabilizing capacitor when in use. VREG1OUT = 4.0V ~ (DDVDH – 0.5)V
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register. Also, the VCOM output can be started and halted by register setting.
VCOMH	O	Stabilizing capacitor	The High level of VCOM amplitude. The output level can be adjusted by electronic volume. Make sure to connect to stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VDV bits). VCOML = (VCL+0.5) V ~ 0V. Make sure to connect to stabilizing capacitor.
VGS	I	GND	Reference level for the grayscale voltage generating circuit. Must connect to the GND level for normal usage.
GND	P	Power supply	Internal logic GND: GND = 0V.
RGND	P	Power supply	Internal RAM GND. RGND must be at the same electrical potential as GND. In case of COG, connect to GND on the FPC to prevent noise.
VDDD	O	Stabilizing capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect to stabilizing capacitor.
IOVCC	P	Power supply	Power supply to the interface pins: /RESET, /CS, /WR, /RD, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. IOVCC = 1.65V ~ 3.3V. Note: Must keep VCI ≥ IOVCC.
AGND	P	Power supply	Analog GND (for logic regulator and liquid crystal power supply circuit): AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	P	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.
Misc. Signal			
IOGNDDUM	I/O	Open	Test pins. Leave them open.
DUMMY1~15 DUMMY20~27	I/O	Open	Test pins. Leave them open.
TESTO3~16	I/O	Open	Test pins. Leave them open.
TEST1~3	I/O	Open	Test pins. Leave them open.
TS0~8	I/O	Open	Test pins. Leave them open.

5. INSTRUCTIONS

5.1. Outline

The OTM3225C supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for OTM3225C to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 80-system and SPI). The corresponding pin assignment of different system interface are shown in Figure 5-1 to Figure 5-5

The instruction can be categorized into 9 groups. And the 9 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ -correction
9. CABC Function (CABC= Content Adaptive Brightness Control)

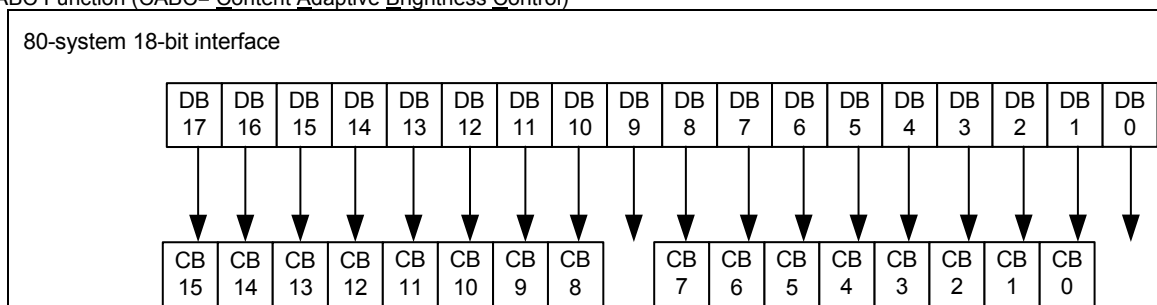


Figure 5-1 : I80-system 18bits interface data transfer format

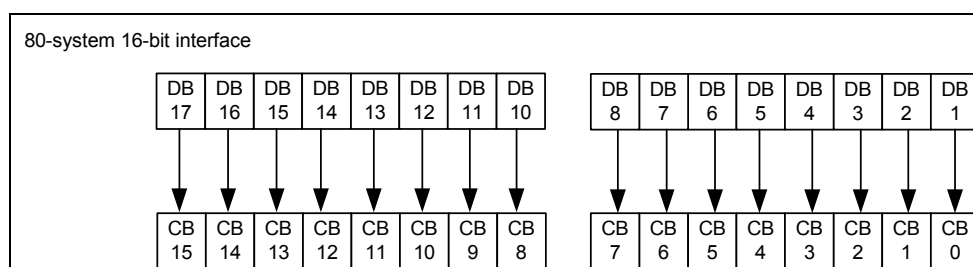


Figure 5-2 : I80-system 16bits interface data transfer format

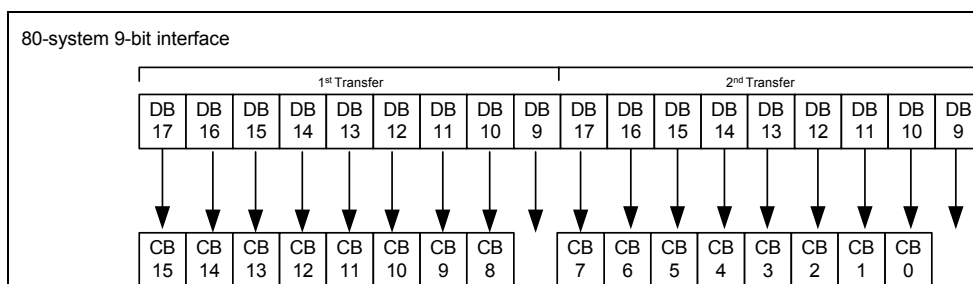


Figure 5-3 : I80-system 9bits interface data transfer format

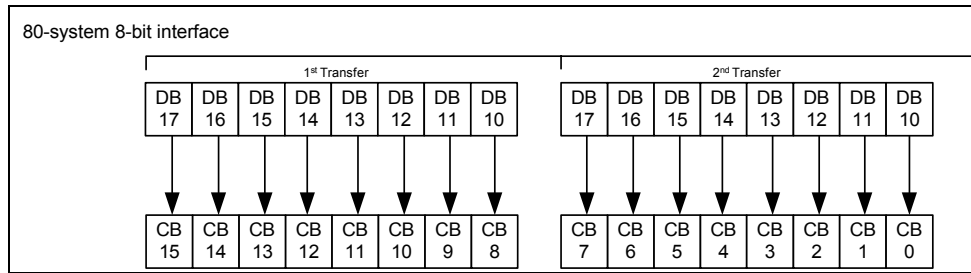
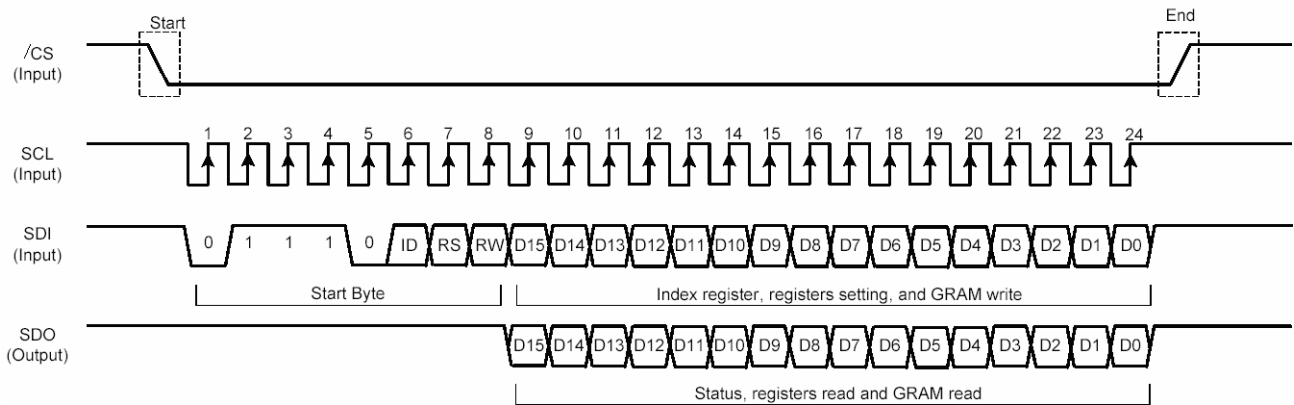


Figure 5-4 : I80 8bits interface data transfer format

(a) Basic data transmission through SPI



(b) Consecutive data transmission through SPI

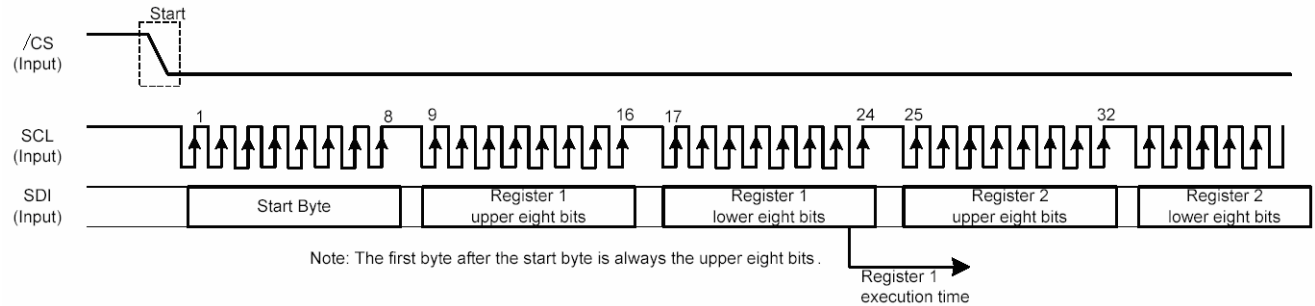


Figure 5-5 : Serial interface data transfer format

5.2. Instruction
Table 5-1 Instruction List Table

Register No	Register	Upper 8-bit								Lower 8-bit								
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	
00h	ID Read	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0		
01h	Driver Output Control	0	0	0	0	0	SM (0)	0	SS (0)	0	0	0	0	0	0	0		
02h	LCD Drive Waveform Control	0	0	0	0	0	1	B/C (0)	EOR (0)	0	0	0	0	0	0	0		
03h	Entry Mode	TRI (0)	DFM (0)	0	BGR (0)	0	0	0	0	ORG (0)	0	I/D1 (1)	I/D0 (1)	AM (0)	0	0		
04h	Scaling Control	0	0	0	0	0	0	RCV1 (0)	RCV0 (0)	0	0	RCH1 (0)	RCH0 (0)	0	0	RSZ1 (0)	RSZ0 (0)	
07h	Display Control (1)	0	0	PTDE1 (0)	PTDE0 (0)	0	0	0	BASEE (0)	0	0	GON (0)	DTE (0)	CL (0)	0	D1 (0)	D0 (0)	
08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
09h	Display Control (3)	0	0	0	0	0	PTS2 (0)	PTS1 (0)	PTS0 (0)	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISCO (0)	
0Ah	Frame Cycle Control	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE (0)	FMI2 (0)	FMI1 (0)	FMI0 (0)	
0Ch	External Display interface control (1)	0	ENC2 (0)	ENC1 (0)	ENC0 (0)	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	
0Dh	Frame Maker Position	0	0	0	0	0	0	0	FMP8 (0)	FMP7 (0)	FMP6 (0)	FMP5 (0)	FMP4 (0)	FMP3 (0)	FMP2 (0)	FMP1 (0)	FMP0 (0)	
0Fh	External Display interface control (2)	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	0	EPL (0)	DPL (0)	
10h	Power Control (1)	0	0	0	SAP (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	APE (0)	AP2 (1)	AP1 (0)	AP0 (0)	0	0	SLP (1)	STB (0)	
11h	Power Control (2)	0	0	0	0	0	DC12 (1)	DC11 (1)	DC10 (1)	0	DC02 (1)	DC01 (1)	DC00 (1)	0	0	VC2 (0)	VC1 (0)	VC0 (0)
12h	Power Control (3)	0	0	0	0	0	0	0	0	VCIRE (0)	0	0	1	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
13h	Power Control (4)	0	0	0	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	0	0	0	0	0	
20h	GRAM address Set Horizontal Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
21h	GRAM address Set Vertical Address	0	0	0	0	0	0	0	AD16 (0)	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	
22h		Write Data to GRAM Read Data from GRAM																
29h	Power Control (7)	0	0	0	0	0	0	0	0	0	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)
2Bh	Frame Rate Control	0	0	0	0	0	0	0	0	0	0	0	0	FRS3 (1)	FRS2 (0)	FRS1 (1)	FRS0 (1)	
30h	γ Control (1)	0	0	0	0	0	0	KP1[2] (0)	KP1[1] (0)	KP1[0] (0)	0	0	0	0	0	KP0[2] (1)	KP0[1] (0)	KP0[0] (0)
31h	γ Control (2)	0	0	0	0	0	0	KP3[2] (0)	KP3[1] (1)	KP3[0] (1)	0	0	0	0	0	KP2[2] (1)	KP2[1] (1)	KP2[0] (0)
32h	γ Control (3)	0	0	0	0	0	0	KP5[2] (0)	KP5[1] (0)	KP5[0] (0)	0	0	0	0	0	KP4[2] (0)	KP4[1] (1)	KP4[0] (1)
35h	γ Control (4)	0	0	0	0	0	0	RP1[2] (0)	RP1[1] (1)	RP1[0] (1)	0	0	0	0	0	RP0[2] (0)	RP0[1] (1)	RP0[0] (1)
36h	γ Control (5)	0	0	0	VRP1[4] (0)	VRP1[3] (1)	VRP1[2] (1)	VRP1[1] (1)	VRP1[0] (0)	0	0	0	0	VRP0[4] (0)	VRP0[3] (0)	VRP0[2] (1)	VRP0[1] (1)	VRP0[0] (0)
37h	γ Control (6)	0	0	0	0	0	KN1[2] (1)	KN1[1] (0)	KN1[0] (0)	0	0	0	0	0	0	KN0[2] (1)	KN0[1] (1)	KN0[0] (1)
38h	γ Control (7)	0	0	0	0	0	KN3[2] (0)	KN3[1] (0)	KN3[0] (1)	0	0	0	0	0	0	KN2[2] (1)	KN2[1] (1)	KN2[0] (0)
39h	γ Control (8)	0	0	0	0	0	KN5[2] (0)	KN5[1] (1)	KN5[0] (1)	0	0	0	0	0	0	KN4[2] (1)	KN4[1] (1)	KN4[0] (1)
3Ch	γ Control (9)	0	0	0	0	0	0	RN1[2] (0)	RN1[1] (1)	RN1[0] (1)	0	0	0	0	0	RN0[2] (0)	RN0[1] (1)	RN0[0] (10)
3Dh	γ Control (10)	0	0	0	VRN1[4] (0)	VRN1[3] (0)	VRN1[2] (1)	VRN1[1] (0)	VRN1[0] (0)	0	0	0	0	VRN0[4] (0)	VRN0[3] (1)	VRN0[2] (0)	VRN0[1] (1)	VRN0[0] (1)
50h	Window Horizontal RAM Address Start	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
51h	Window Horizontal RAM Address End	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	
52h	Window Vertical RAM Address Start	0	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
53h	Window Vertical RAM Address End	0	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)
60h	Driver Output Control	GS (0)	0	NL5 (1)	NL4 (0)	NL3 (0)	NL2 (1)	NL1 (1)	NL0 (1)	0	0	SCN5 (0)	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	
61h	Driver Output Control	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL (0)	VLE (0)	REV (0)	
6Ah	Vertical Scroll Control	0	0	0	0	0	0	0	0	VL8 (0)	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)
80h	Display Position - Partial Display 1	0	0	0	0	0	0	0	0	PTDP08 (0)	PTDP07 (0)	PTDP06 (0)	PTDP05 (0)	PTDP04 (0)	PTDP03 (0)	PTDP02 (0)	PTDP01 (0)	PTDP00 (0)
81h	RAM Address Start - Partial Display 1	0	0	0	0	0	0	0	0	PTSA08 (0)	PTSA07 (0)	PTSA06 (0)	PTSA05 (0)	PTSA04 (0)	PTSA03 (0)	PTSA02 (0)	PTSA01 (0)	PTSA00 (0)
82h	RAM Address End - Partial Display 1	0	0	0	0	0	0	0	0	PTEA08 (0)	PTEA07 (0)	PTEA06 (0)	PTEA05 (0)	PTEA04 (0)	PTEA03 (0)	PTEA02 (0)	PTEA01 (0)	PTEA00 (0)
83h	Display Position - Partial Display 2	0	0	0	0	0	0	0	0	PTDP18 (0)	PTDP17 (0)	PTDP16 (0)	PTDP15 (0)	PTDP14 (0)	PTDP13 (0)	PTDP12 (0)	PTDP11 (0)	PTDP10 (0)

Register No	Register	Upper 8-bit								Lower 8-bit											
		CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0				
84h	RAM Address Start - Partial Display 2	0	0	0	0	0	0	0	0	PTSA18 (0)	PTSA17 (0)	PTSA16 (0)	PTSA15 (0)	PTSA14 (0)	PTSA13 (0)	PTSA12 (0)	PTSA11 (0)	PTSA10 (0)			
85h	RAM Address End - Partial Display 2	0	0	0	0	0	0	0	0	PTEA18 (0)	PTEA17 (0)	PTEA16 (0)	PTEA15 (0)	PTEA14 (0)	PTEA13 (0)	PTEA12 (0)	PTEA11 (0)	PTEA10 (0)			
90h	Panel interface Control 1	0	0	0	0	0	0	0	0	DIV11 (0)	DIV10 (0)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)		
92h	Panel Interface Control 2	0	0	0	0	0	0	0	0	NOWI2 (1)	NOWI1 (1)	NOWI0 (0)	0	0	0	0	0	0	0		
95h	Panel Interface Control 4	0	0	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	0	0	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (0)	RTNE0 (0)		
97h	Panel Interface Control 5	0	0	0	0	0	0	0	0	NOWE3 (1)	NOWE2 (1)	NOWE1 (0)	NOWE0 (0)	0	0	0	0	0	0		
B1h	Write Display Brightness Value	0	0	0	0	0	0	0	0	0	0	0	0	DBV7 (0)	DBV6 (0)	DBV5 (0)	DBV4 (0)	DBV3 (0)	DBV2 (0)	DBV1 (0)	DBV0 (0)
B2h	Read Display Brightness Value	0	0	0	0	0	0	0	0	0	0	0	0	DBV7 (0)	DBV6 (0)	DBV5 (0)	DBV4 (0)	DBV3 (0)	DBV2 (0)	DBV1 (0)	DBV0 (0)
B3h	Write Control Display Value	0	0	0	0	0	0	0	0	LED_ON (0)	BC_OUT_INV (0)	0	0	BCTRL (0)	0	DD (0)	BL (0)	0	0		
B4h	Read Control Display Value	0	0	0	0	0	0	0	0	LED_ON	BC_OUT_INV			BCTRL		DD	BL				
B5h	Write Content Adaptive Brightness Control Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1 (0)	C0 (0)		
B6h	Read Content Adaptive Brightness Control Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0		
BEh	Write CABC minimum brightness	0	0	0	0	0	0	0	0	0	CMB7 (0)	CMB6 (0)	CMB5 (0)	CMB4 (0)	CMB3 (0)	CMB2 (0)	CMB1 (0)	CMB0 (0)			
BFh	Read CABC minimum brightness	0	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0			

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

5.2.1. Index Register (IR)

R/W	RS	CB15	CCB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h ~ RFFh) of a control register or RAM. The index range is from "0000_0000" to "1111_1111" in binary format.

5.2.2. Read ID Register

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

The IC code of OTM3225C can be accessed by read operation. The 16-bits ID Code can be read out when read ID operation is executed. The ID information can be set from 0x0000h to 0xFFFFh by IC metal option or Trim option for customer's request.

5.2.3. Driver Output Control Register (R01h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0	0

SS: Shift direction of the source driver output selection.

When SS = "0", source driver shift from S1 to S720.

When SS = "1", source driver shift from S720 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 5-2**.

★**Note:** After changing SS bit or BGR bit, display data must be rewritten.

Table 5-2

SS=0;BGR=0;	S1	S2	S3	S718	S719	S720
SS=0;BGR=1;	S1	S2	S3	S718	S719	S720
SS=1;BGR=0;	S1	S2	S3	S718	S719	S720
SS=1;BGR=1;	S1	S2	S3	S718	S719	S720

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Table 5-3** and **Figure 5-6**

Table 5-3

SM	GS	Gate output sequence (Begin,.....,End)
0	0	G1→G2→G3→G4→.....→G317→G318→G319→G320
0	1	G320→G319→G318→G317→.....→G4→G3→G2→G1
1	0	G1→G3→G5→.....→G317→G319→ →G2→G4→G6→.....→G318→G320
1	1	G320→G318→G316→.....→G4→G2→ →G319→G317→G315→.....→G3→G1

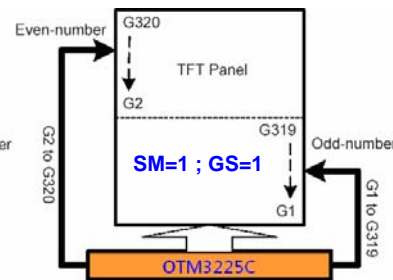
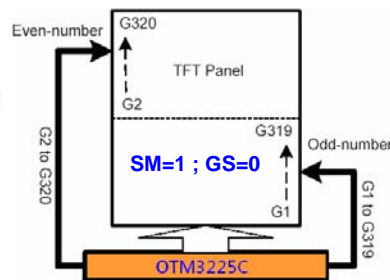
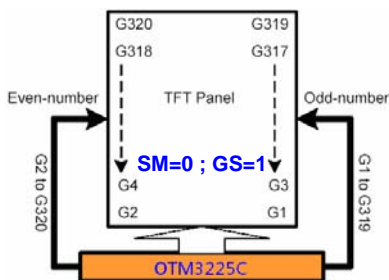
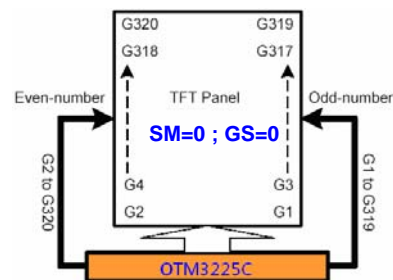


Figure 5-6{ TC }: Panel layout for SM & GS bit

5.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	1	BC0	EOR	0	0	0	0	0	0	0	0

BC0: This bit can set the VCOM toggle at ever frame format or N-line inversion format.

BC0=0: Frame inversion waveform is selected.

BC0=1: Line inversion waveform is selected. (Must combine EOR=1 for Line inversion)

EOR: Enables Line-inversion when EOR=1 and BC0=1.

5.2.5. Entry Mode (R03h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I/D1	I/D0	AM	0	0	0

Table 5-4

Operation mode	ORG	AM	I/D1	I/D0	Function
Mode 1	0	0	0	0	Replace horizontal data
Mode2	0	1	0	1	Replace vertical data
Mode3	1	0	1	0	Conditionally replace horizontal data
Mode4	1	1	1	1	Conditionally replace vertical data

★**Note:** After changing ORG;AM;I/D1 or I/D0 bit, display data must be rewritten.

AM: To set the update direction when writing data to GRAM.

If AM=1, data will write in vertical direction. (Address counter will automatic update in vertical direction)

If AM=0, data will write in horizontal direction. (Address counter will automatic update in horizontal direction)

When setting a window area by register R50h~R53h, the data is written only within the area based on by I/D[1:0],AM bit.

I/D1-0: To specify address counter(AC) automatically increment or decrement while update one pixel display data to GRAM.

I/D[0] indicates the increment or decrement in horizontal direction.

I/D[0]=0: decrement in horizontal direction automatically

I/D[0]=1: increment in horizontal direction automatically

I/D[1] indicates the increment or decrement in vertical direction.

I/D[1]=0: decrement in vertical direction automatically

I/D[1]=1: increment in vertical direction automatically

ID[1-0] setting can cooperate with AM bit to set the data updating direction.

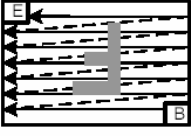
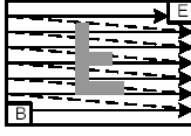
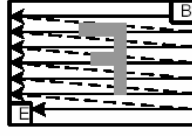
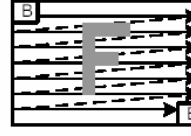
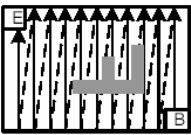

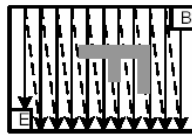

	I/D[1:0] = 00 Horizontal : decrement Vertical : decrement	I/D[1:0] = 01 Horizontal : increment Vertical : decrement	I/D[1:0] = 10 Horizontal : decrement Vertical : increment	I/D[1:0] = 11 Horizontal : increment Vertical : increment
AM = 0 Horizontal				
AM = 1 Vertical				

Figure 5-7

ORG: OTM3225C provides the option of start address definition when window function is selected.

ORG=0: RAM address setting (R20h, R21h) should set to the window start address, as normal operation case.

In this case, the origin address is not move.

ORG=1: RAM address setting (R20h, R21h) should set to (0x0000h) no matter where the window start address is.

Setting other addresses is inhibited.

In this case, the window start position is treated as (0x0000h), regardless the physical location in GRAM.

★**Note:** In GRAM read operation(R22h), make sure to set ORG=0.

★**Note:** In RGB mode with Full-Screen operation, make sure to set ORG=1.

BGR: To set the order of RGB sub-pixel in GRAM.

The combination of SS and BGR bit are summarized at **Table 5-2**.

BGR=0: same assignment of RGB allocation of DB17-0.																	
DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
BGR=1: inverse assignment of RGB allocation of DB17-0.																	
DB17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

Figure 5-8

DFM: In combination with TRI setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface. Make sure to set DFM=0 when not transferring data via 16-bit or 8-bit interface.

TRI: to set 1–3 time transfer mode for system interface. TRI bit should cooperate with DFM to meet the specific transfer mode.

For 8-bit data bus interface mode:

TRI=0: 2 time transfer mode for 16-bit GRAM data.

TRI=1: 3 time transfer mode for 18-bit GRAM data

For 16-bit data bus interface mode:

TRI=0: 1 time transfer mode for 16-bit GRAM data.

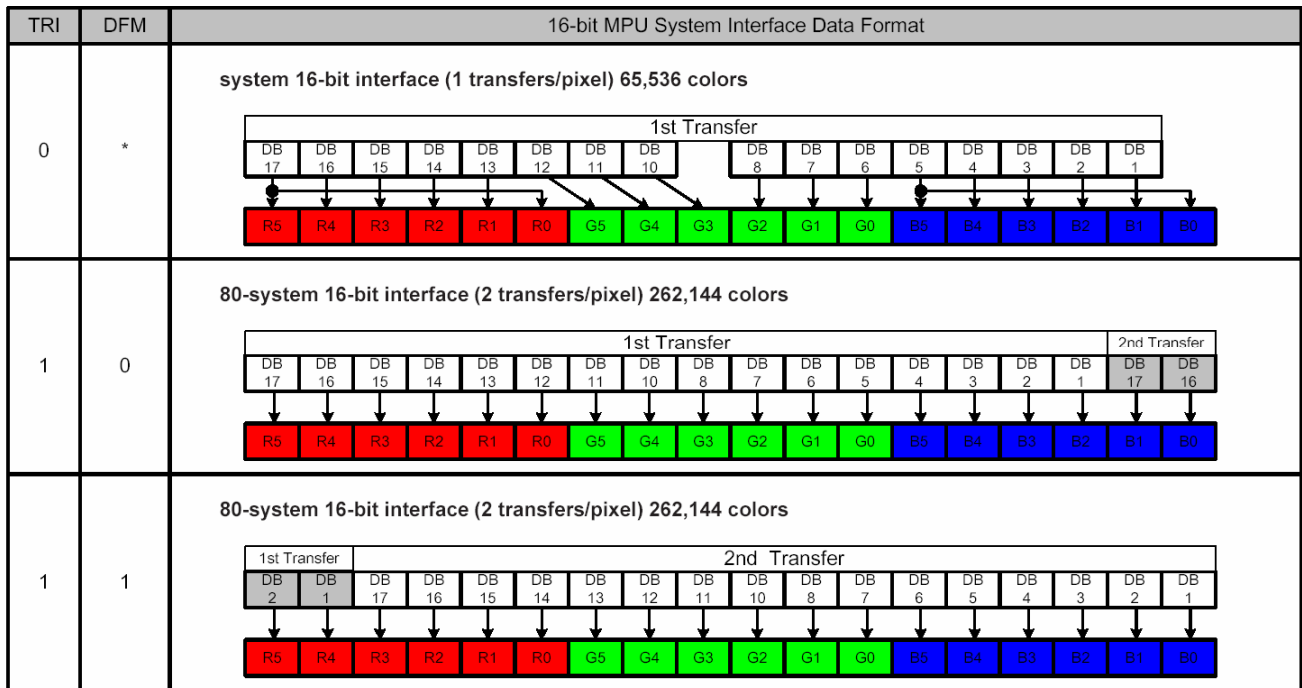
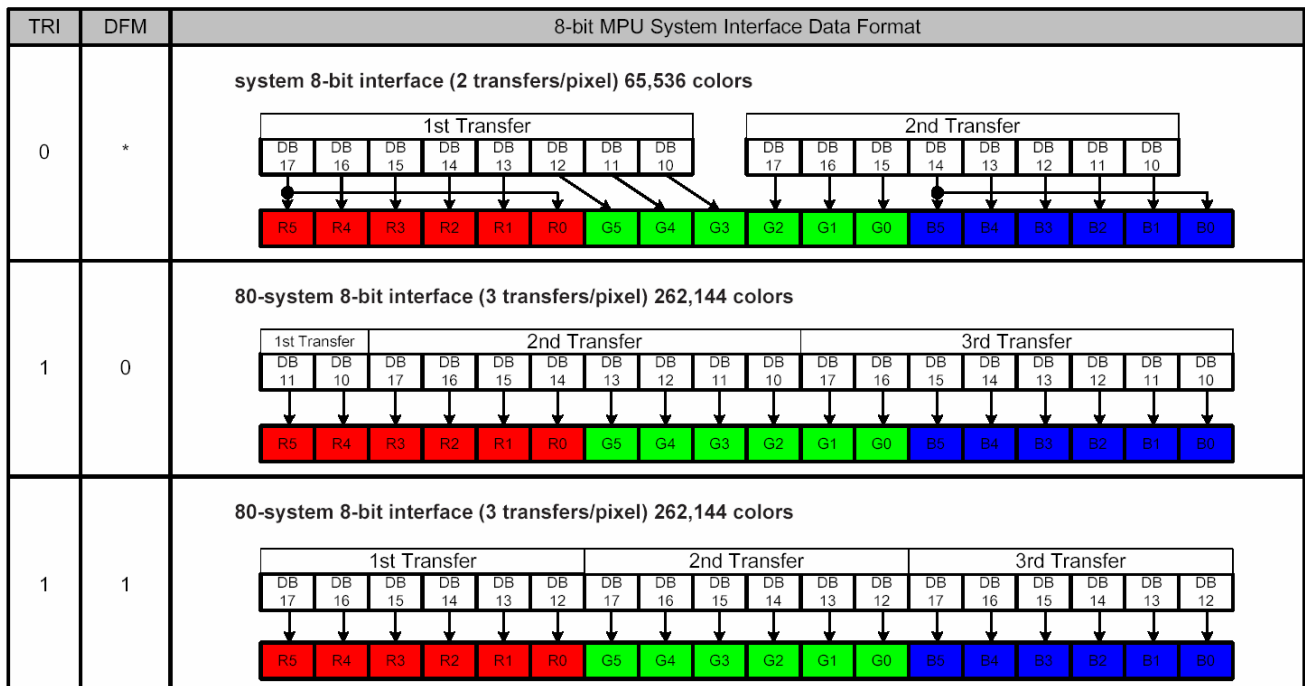
TRI=1: 2 time transfer mode for 18-bit GRAM data

★**Note:** Set TRI=0, when using 18-bits bus width or 9-bits bus width.

★**Note:** The combination of DFM and TRI bit are summarized at **Figure 5-9 & 5-10**.

★**Note:** Must set TRI=0, when reading back data from GRAM. (Hint: Read GRAM data will be 16-bits only)

★**Note:** Set TRI=0, when using 65536 color format.


Figure 5-9

Figure 5-10

5.2.6. Scaling Control register (R04h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	RCV1	RCV0	0	0	RCH1	RCH0	0	0	RSZ1	RSZ0

RSZ [1:0]: OTM3225C provides scaling factor to give the display more flexibility to show different picture size. For detail, refer to “Scaling function”.

RSZ1	RSZ0	Scaling Factor
0	0	No Scaling
0	1	1/2 times
1	0	No Scaling
1	1	1/4 times



No Scaling

1/2 times

1/4 times

RCH [1:0]: To set the surplus pixel number in horizontal direction when scaling mode is selected. When scaling mode is not selected, make sure RCH [1:0]= “00”

RCH1	RCH0	Surplus pixel number in Horizontal direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

RCV [1:0]: To set the surplus pixel number in Vertical direction when scaling mode is selected. When scaling mode is not selected, make sure RCV [1:0]= “00”

RCV1	RCV0	Surplus pixel number in Vertical direction
0	0	0 Pixel
0	1	1 Pixel
1	0	2 Pixels
1	1	3 Pixels

5.2.7. Display Control (R07h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	COL	0	D1	D0

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; OTM3225C is set to standby mode.

COL: 8-color mode selection. When COL=1 OTM3225C enter to 8-color mode. When COL=0, OTM3225C is in normal operation mode.

The combination of D1-0, COL and BASEE bit is summarized at [錯誤! 書籤的自我參照不正確。](#)

Table 5-5

D1-0	BASEE	COL	Source output	VCOM output	Internal Operation	Display Mode
00	*	*	GND	GND	Halt (Standby)	OFF
01	*	*	GND	GND	Halt (Standby)	OFF
10	*	*	V0 & V63 (Full)	Toggle	Normal Operation	8 Color
11	0	0	Non-lit display & Partial	Toggle	Normal Operation	Partial
	0	1	Non-lit display & Partial	Toggle	Normal Operation	Partial + 8 Color
	1	0	Normal display (Full)	Toggle	Normal Operation	Normal
	1	1	V0 & V63 (Full)	Toggle	Normal Operation	8 Color

DTE: Specify the high/low level of gate driver output signal. The meaning of DTE bit is summarized at [Table 5-6](#)

Table 5-6

APE	DTE	Gate Output
1	0	VGL
	1	VGH/VGL

BASEE: To enable Base image display

BASEE	Display
0	(1) Non-lit display (2) Partial image display
1	Base image is display on the LCD

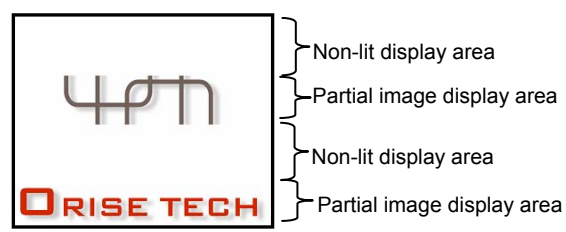
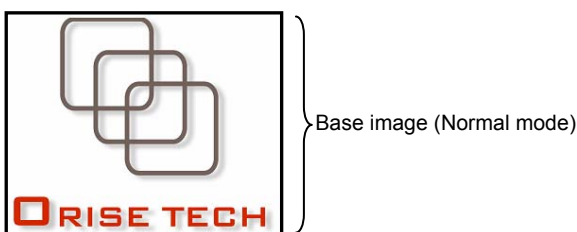
PTDE1-0: To set the partial-display enables function.

PTDE [0]: "0" Partial image 1 display "Off".

"1" Partial image 1 display "On".

PTDE [1]: "0" Partial image 2 display "Off".

"1" Partial image 2 display "On".



For detail information, refer to section "Partial Display function."

5.2.8. Display Control 2 (R08h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 5-7 summarized the function of FP3-0/BP3-0 setting.

When setting this register, we recommend that:

$$BP + FP \leq 16 \text{ lines}$$

$$FP \geq 2 \text{ lines}$$

$$BP \geq 2 \text{ lines}$$

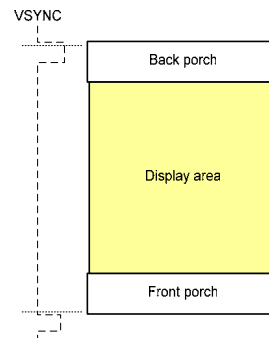


Figure 5-11 Front porch and back porch function diagram

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Table 5-8** summarized the setting for each interface mode.

Table 5-7

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	BP2	BP1	BP0	Number of lines for the Back Porch
0	0	0	0	1 lines
0	0	0	1	1 lines
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	15 lines

Table 5-8 Recommend setting for BP & FP

Operation of Internal clock	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

5.2.9. Display Control 3 (R09h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	PTS2	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0

ISC3-0: To set the gate driver scan cycle in non-lit display area.

Table 5-9 summarized the function of ISC3-0 setting

Table 5-9

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	0	0	0	1 Frames	16ms
0	0	0	1	1 Frames	16ms
0	0	1	0	3 Frames	50 ms
0	0	1	1	5 Frames	84 ms
0	1	0	0	7 Frames	117 ms
0	1	0	1	9 Frames	150 ms
0	1	1	0	11 Frames	184 ms

ISC3	ISC2	ISC1	ISC0	Scan cycle	fFLM=60Hz
0	1	1	1	13 Frames	217 ms
1	0	0	0	15 Frames	251 ms
1	0	0	1	17 Frames	317 ms
1	0	1	0	19 Frames	351 ms
1	0	1	1	21 Frames	384 ms
1	1	0	0	23 Frames	418 ms
1	1	0	1	25 Frames	451 ms
1	1	1	0	27 Frames	484 ms
1	1	1	1	29 Frames	518 ms

PTG1-0: To set the gate driver scan mode in non-display area.

Table 5-10 summarized the function of PTG1-0 setting

Table 5-10

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
0	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	0	Interval scan	Based on the PTS2-0 bits setting	VCOMH/VCOML
1	1	Normal scan	Based on the PTS2-0 bits setting	VCOMH/VCOML

PTS2-0: To set the source driver output level in non-display area of partial display mode. Table 5-11 summarized the function of PTS2-0 setting.

Table 5-11

PTS2	PTS1	PTS0	Source output in non-display area		Operation amplifier in non-display area	Display in non-display area (Normally White panel)
			+ polarity	- polarity		
0	0	0	V63	V0	V0~V63	White
0	0	1	V0	V63	V0~V63	Black
0	1	0	GND	GND	V0~V63	White (With Flicker)
0	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)
1	0	0	V63	V0	V0~V63	White
1	0	1	V0	V63	V0~V63	Black
1	1	0	GND	GND	V0~V63	White (With Flicker)
1	1	1	High impedance	High impedance	V0~V63	Abnormal (Crosstalk)

5.2.10. Frame Cycle Control (R0Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARK OE	FMI2	FMI1	FMI0

FMI [2:0]: (FMARK Interval) OTM3225C provide FMARK signal to prevent tearing effect. FMI [2:0] can set FMARK output interval.

FMI2	FMI1	FMI0	Output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	0	3 frames
0	1	1	4 frames
1	0	0	5 frames
1	0	1	6 frames
1	1	0	7 frames
1	1	1	8 frames

FMARKOE: (FMARK Output Enable) Set the output signal FMARK from FMARK pin.

FMARK="0": Stop to output FMARK signal.

FMARK="1": Start to output FMARK signal.

5.2.11. External Display Interface Control 1 (R0Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM1-0: To set the different transfer modes of RGB interface. **Table 5-12** summarized the function of RIM1-0 setting.

Table 5-12

RIM1	RIM0	RGB Interface Mode	Colors	Data Bus	Number of transfer during 1 line
0	0	18-bit RGB interface (one transfer/pixel)	262K	DB 17-0	240x18-bits (AM bit=0) 320x18-bits (AM bit=1)
0	1	16-bit RGB interface (one transfer/pixel)	65K	DB 17-13; DB 11-1	240x16-bits (AM bit=0) 320x16-bits (AM bit=1)
1	0	6-bit RGB interface (three transfers/pixel)	262K	DB17-12	720x6-bits (AM bit=0) 960x6-bits (AM bit=1)
1	1	8-bit RGB interface (two transfers/pixel)	65K	DB17-10	480x8-bits (AM bit=0) 640x8-bits (AM bit=1)

DM1-0: To specify the display interface mode. DM1-0 Setting can switch the display interface among system interface, RGB interface and VSYNC interface. **Table 5-13** summarized the function of DM1-0 setting.

Table 5-13

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Select the interface to access the OTM3225C's internal GRAM. Set RM to "1" when writing display data via the RGB interface. The OTM3225C allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 5-14 summarized the function of RM bit setting.

Table 5-14

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Table 5-15

Display State	Operation Mode	RAM access Mode(RM)	Display operation Mode (DM1-0)
Still pictures	Internal clock	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)
Low Speed moving picture	RGB interface	RGB interface (RM = 1)	Internal clock operation (DM1-0 = 00)

Note1: Instructions are set only via the system interface.

Note2: Do not make changes to the RGB-I/F mode setting (RIM-0) while the RGB I/F is in operation.

Note3: See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

5.2.12. Frame Maker Position (R0Dh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0

FMP 8-0: Indicates the output position of frame cycle signal (FMARK).

A high-active pulse is output from FMARK pin and relate with back porch.

When FMP[8:0] = 9'h000, FMARK is outputted at the start of back porch for 1line period.

When FMP[8:0] = 9'h001, FMARK is outputted one line after the start of back porch.

Please reference section "FMARK function" for detail description.

FMP [8:0]	FMARK Output Position
9'h000	Immediate (Delay 0 line period)
9'h001	Delay 1 line period
9'h002	Delay 2 lines period
	~
Max. Vaule	$9'h000 \leq \text{FMP}[8:0] \leq \text{BP} + \text{NL} + \text{FP}$

5.2.13. External Display Interface Control 2 (R0Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL

EPL: The polarity of ENABLE signal selection in RGB interface mode.

EPL = "0": ENABLE: Low active

EPL = "1": ENABLE: High active

DPL: Select the data latch edge of the DOTCLK signal in RGB interface mode.

DPL = "0": rising edge of the DOTCLK.

DPL = "1": falling edge of the DOTCLK.

VSPL: The polarity of VSYNC signal selection in RGB interface mode.

VSPL = "0": Low active.

VSPL = "1": High active.

HSPL: The polarity of HSYNC signal selection in RGB interface mode.

HSPL = "0": Low active.

HSPL = "1": High active.

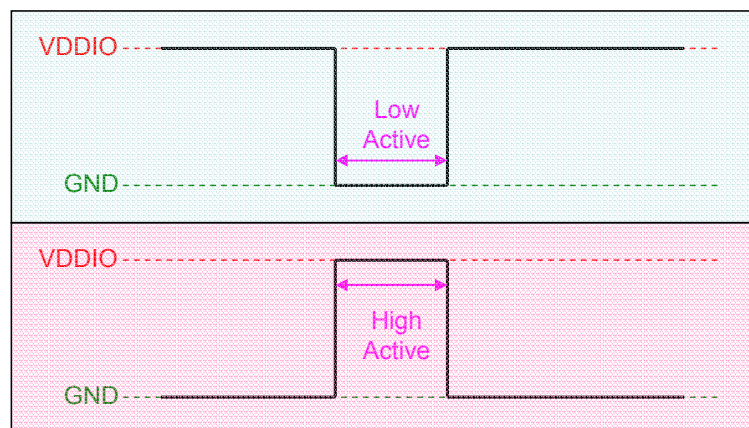


Figure 5-12

5.2.14. Power Control 1 (R10h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB

SLP: Sleep mode selection. When SLP =1, OTM3225C set to sleep mode. In sleep mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set SLP to "1". Set SLP=0 can exit sleep mode. Moreover, when exit from sleep mode, data in GRAM and in instruction registers are keep the same with these before set to SLP mode.

STB: Standby mode selection. When STB =1, OTM3225C set to standby mode. In this mode, all internal operations are terminated including internal RC oscillation. Be sure that a display off sequence should be executed before set STB to "1". Set STB=0 can exit standby mode. Moreover, when exit from standby mode, data in GRAM and register will not lost, reset and re-sending command and data into GRAM is not necessary.

AP2-0: Operational amplifier DC bias current adjustment. Set AP2-0 = "000" to stop operational amplifier and DC/DC charge pump circuits to reduce current consumption during no display period.

APE: Enable bit for both liquid crystal power supply and gamma voltage generation circuit.
 APE="0", Halt liquid crystal power supply and gamma voltage generation circuit.
 APE="1", Enable liquid crystal power supply and gamma voltage generation circuit.

BT3-0: Set the voltage level of DDVDH, VGH, VGL and VCL.

Table 5-16 summarized the function of BT3-0 setting

BT2	BT1	BT0	DDVDH	VGH	VGL	VCL
0	0	0	VCI1 x 2	VCI1 x 6	VCI1x -5	-VCI1
0	0	1	VCI1 x 2	VCI1 x 6	VCI1x -4	-VCI1
0	1	0	VCI1 x 2	VCI1 x 6	VCI1x -3	-VCI1
0	1	1	VCI1 x 2	VCI1 x 5	VCI1x -5	-VCI1
1	0	0	VCI1 x 2	VCI1 x 5	VCI1x -4	-VCI1
1	0	1	VCI1 x 2	VCI1 x 5	VCI1x -3	-VCI1
1	1	0	VCI1 x 2	VCI1 x 4	VCI1x -4	-VCI1
1	1	1	VCI1 x 2	VCI1 x 4	VCI1x -3	-VCI1

SAP: Enable bit for gamma voltage generation circuit.
 SAP="0", Halt gamma voltage generation circuit.
 SAP="1", Enable gamma voltage generation circuit

5.2.15. Power Control 2 (R11h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

VC2-0: Set the voltage of VCIOUT. VCIOUT is generated by VCI. **Table 5-17** summarized the function of VC2-0 setting

Table 5-17

VC2	VC1	VC0	VCIOUT
0	0	0	0.95 x VCI
0	0	1	0.9 x VCI
0	1	0	0.85 x VCI
0	1	1	0.8 x VCI
1	0	0	0.75 x VCI
1	0	1	0.7 x VCI
1	1	0	0.65 x VCI
1	1	1	1.00 x VCI

DC02-00: Set DC/DC charge pump circuit 1 operating frequency. **Table 5-18** summarized the function of DC02-00 setting

Table 5-18

DC02	DC01	DC00	DC/DC charge pump circuit 1 frequency (fDCDC1)
0	0	0	2H
0	0	1	1H
0	1	0	1/2H
0	1	1	1/4H
1	0	0	1/8H
1	0	1	1/16H
1	1	0	1/32H
1	1	1	1/64H

DC12-10: Set DC/DC charge pump circuit 2 operating frequency. **Table 5-19** summarized the function of DC02-00 setting

Note: Be aware that DC/DC charge pump 1 frequency \geq DC/DC charge pump 2 frequency

Table 5-19

DC12	DC11	DC10	Step-up circuit 2 step-up frequency (fDCDC2)
0	0	0	1H
0	0	1	1/2H
0	1	0	1/4H
0	1	1	1/8H
1	0	0	1/16H
1	0	1	1/32H
1	1	0	1/64H
1	1	1	1/128H

Note: Be sure $fDCDC1 \geq fDCDC2$ when setting DC02-00, DC12-10.

CPU mode : 1H= Fosc / RTNI*DIVI

RGB mode : 1H= Fosc / RTNE*DIVE

5.2.16. Power Control 3 (R12h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	1	VRH3	VRH2	VRH1	VRH0

VCIRE: Select reference voltage for VREG1OUT

VCIRE = "0" (default): External VCI as reference voltage for VREG1OUT.

VCIRE = "1": Internal VCIR as reference voltage for VREG1OUT. (VCIR=2.5V)

VRH3-0: Set the voltage level of VCI. VCI is generated by VREG1OUT. **Table 5-20** summarized the function of VRH3-0 setting

Table 5-20

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	
				VCIRE=0	VCIRE=1
0	0	0	0	Halt	Halt
0	0	0	1	VCIx2.00	2.5Vx2.00 = 5.000V
0	0	1	0	VCIx2.05	2.5Vx2.05 = 5.125V
0	0	1	1	VCIx2.10	2.5Vx2.10 = 5.250V
0	1	0	0	VCIx2.20	2.5Vx2.20 = 5.500V
0	1	0	1	VCIx2.30	2.5Vx2.30 = 5.750V
0	1	1	0	VCIx2.40	2.5Vx2.40 = 6.000V
0	1	1	1	VCIx2.40	2.5Vx2.40 = 6.000V
1	0	0	0	VCIx1.60	2.5Vx1.60 = 4.000V
1	0	0	1	VCIx1.65	2.5Vx1.65 = 4.125V
1	0	1	0	VCIx1.70	2.5Vx1.70 = 4.250V
1	0	1	1	VCIx1.75	2.5Vx1.75 = 4.375V
1	1	0	0	VCIx1.80	2.5Vx1.80 = 4.500V
1	1	0	1	VCIx1.85	2.5Vx1.85 = 4.625V
1	1	1	0	VCIx1.90	2.5Vx1.90 = 4.750V
1	1	1	1	VCIx1.95	2.5Vx1.95 = 4.875V

5.2.17. Power Control 4 (R13h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VDV4-0: Set the Vcom amplitude. Vcom amplitude is generated by VREG1OUT.

Table 5-21

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.70
0	0	0	0	1	VREG1OUT x 0.72
0	0	0	1	0	VREG1OUT x 0.74
0	0	0	1	1	VREG1OUT x 0.76
0	0	1	0	0	VREG1OUT x 0.78
0	0	1	0	1	VREG1OUT x 0.80
0	0	1	1	0	VREG1OUT x 0.82
0	0	1	1	1	VREG1OUT x 0.84
0	1	0	0	0	VREG1OUT x 0.86
0	1	0	0	1	VREG1OUT x 0.88
0	1	0	1	0	VREG1OUT x 0.90
0	1	0	1	1	VREG1OUT x 0.92
0	1	1	0	0	VREG1OUT x 0.94
0	1	1	0	1	VREG1OUT x 0.96
0	1	1	1	0	VREG1OUT x 0.98
0	1	1	1	1	VREG1OUT x 1.00
1	0	0	0	0	VREG1OUT x 0.94
1	0	0	0	1	VREG1OUT x 0.96
1	0	0	1	0	VREG1OUT x 0.98
1	0	0	1	1	VREG1OUT x 1.00
1	0	1	0	0	VREG1OUT x 1.02
1	0	1	0	1	VREG1OUT x 1.04
1	0	1	1	0	VREG1OUT x 1.06
1	0	1	1	1	VREG1OUT x 1.08
1	1	0	0	0	VREG1OUT x 1.10
1	1	0	0	1	VREG1OUT x 1.12
1	1	0	1	0	VREG1OUT x 1.14
1	1	0	1	1	VREG1OUT x 1.16
1	1	1	0	0	VREG1OUT x 1.18
1	1	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 1.22
1	1	1	1	1	VREG1OUT x 1.24

5.2.18. GRAM Address Set (Horizontal Address) (R20h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

5.2.19. GRAM Address Set (Vertical Address) (R21h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16-0: To set the initial address counter for GRAM address. Based on AM and I/D[1:0] setting, the address counter is automatically increment or decrement while data are written to the internal GRAM. There is no need to updated AD16-0 every data transfer if AD16-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the OTM3225C is in standby mode.

Table 5-22 summarized the function of AD15-0 setting

Table 5-22

AD[16:0]	GRAM data map
17'h00000 – 17'h000EF	1 st line GRAM data
17'h00100 – 17'h001EF	2 nd line GRAM data
17'h00200 – 17'h002EF	3 rd line GRAM data
17'h00300 – 17'h003EF	4 th line GRAM data
:	:
17'h13600 – 17'h13CEF	317 th line GRAM data
17'h13700 – 17'h13DEF	318 th line GRAM data
17'h13800 – 17'h13EEF	319 th line GRAM data
17'h13900 – 17'h13FEF	320 th line GRAM data

5.2.20. Write Data to GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different interface modes.															

WD17-0: OTM3225C supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, OTM3225C will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected. **Table 5-23** summarized the source driver grayscale voltage output versus graphic data in GRAM.

Figure 5-13 ~Figure 5-26 illustrates the pin assignment among data bus (DB17-0), R22 (WD17-0) and GRAM.

Table 5-23

Data in GRAM RGB	Source Driver Grayscale Output	
	Negative	Positive
000000	V0	V63
000001	V1	V62
000010	V2	V61
000011	V3	V60
000100	V4	V59
000101	V5	V58
000110	V6	V57
000111	V7	V56
001000	V8	V55
001001	V9	V54
001010	V10	V53
001011	V11	V52
001100	V12	V51
001101	V13	V50
001110	V14	V49
001111	V15	V48
010000	V16	V47
010001	V17	V46
010010	V18	V45
010011	V19	V44
010100	V20	V43
010101	V21	V42
010110	V22	V41
010111	V23	V40
011000	V24	V39
011001	V25	V38
011010	V26	V37
011011	V27	V36
011100	V28	V35

Data in GRAM RGB	Source Driver Grayscale Output	
	Negative	Positive
011101	V29	V34
011110	V30	V33
011111	V31	V32
100000	V32	V31
100001	V33	V30
100010	V34	V29
100011	V35	V28
100100	V36	V27
100101	V37	V26
100110	V38	V25
100111	V39	V24
101000	V40	V23
101001	V41	V22
101010	V42	V21
101011	V43	V20
101100	V44	V19
101101	V45	V18
101110	V46	V17
101111	V47	V16
110000	V48	V15
110001	V49	V14
110010	V50	V13
110011	V51	V12
110100	V52	V11
110101	V53	V10
110110	V54	V9
110111	V55	V8
111000	V56	V7
111001	V57	V6
111010	V58	V5
111011	V59	V4
111100	V60	V3
111101	V61	V2
111110	V62	V1
111111	V63	V0

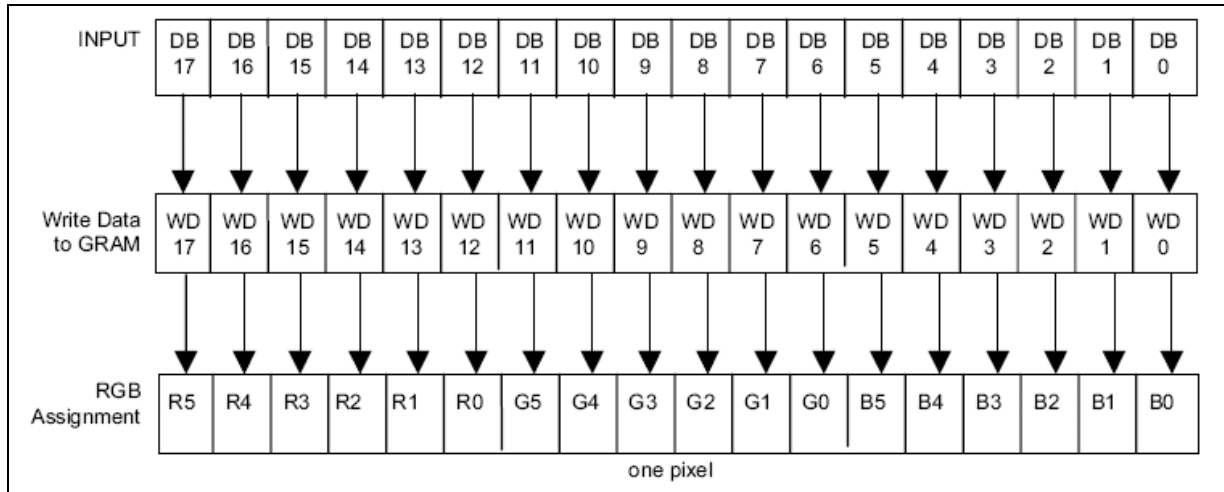


Figure 5-13 18-bit interface (262,144 colors) TRI = 0, DFM=x.

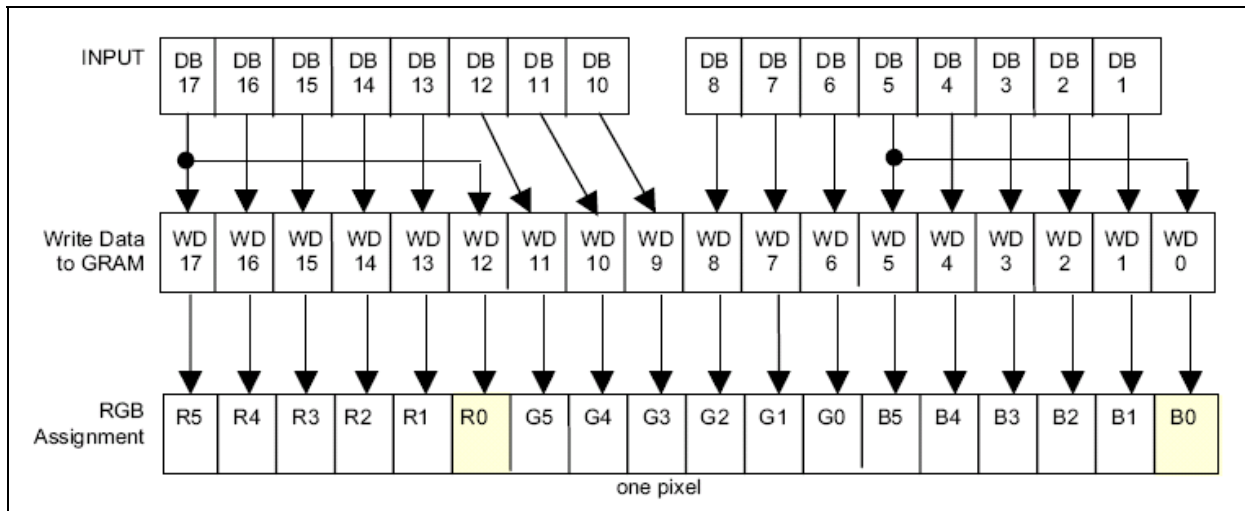


Figure 5-14 16-bit interface (65,536 colors) TRI= 0, DFM=x

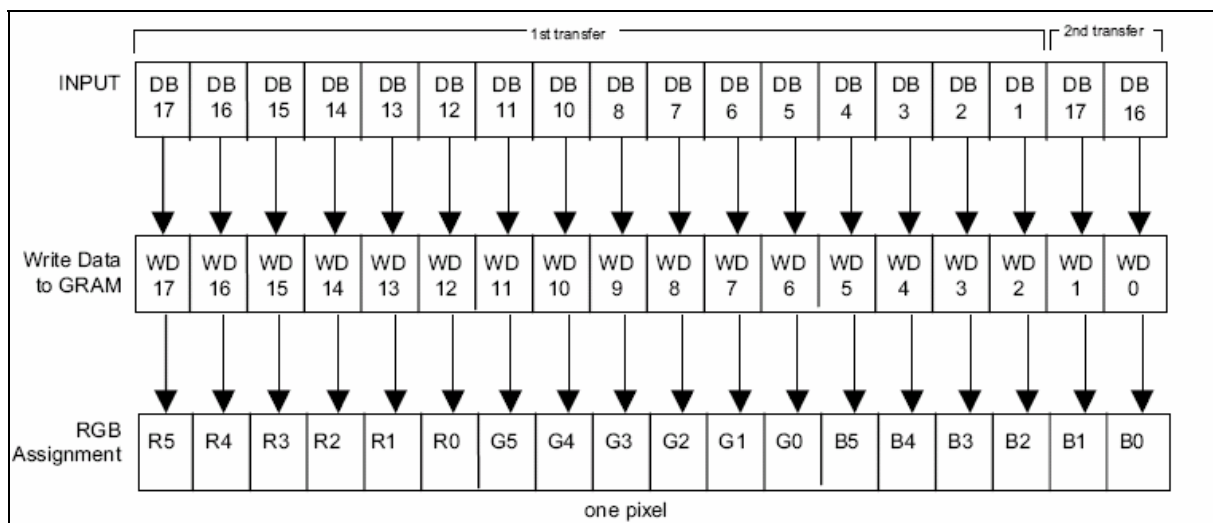


Figure 5-15 16-bit interface (262,144 colors) TRI = 1, DFM = 0

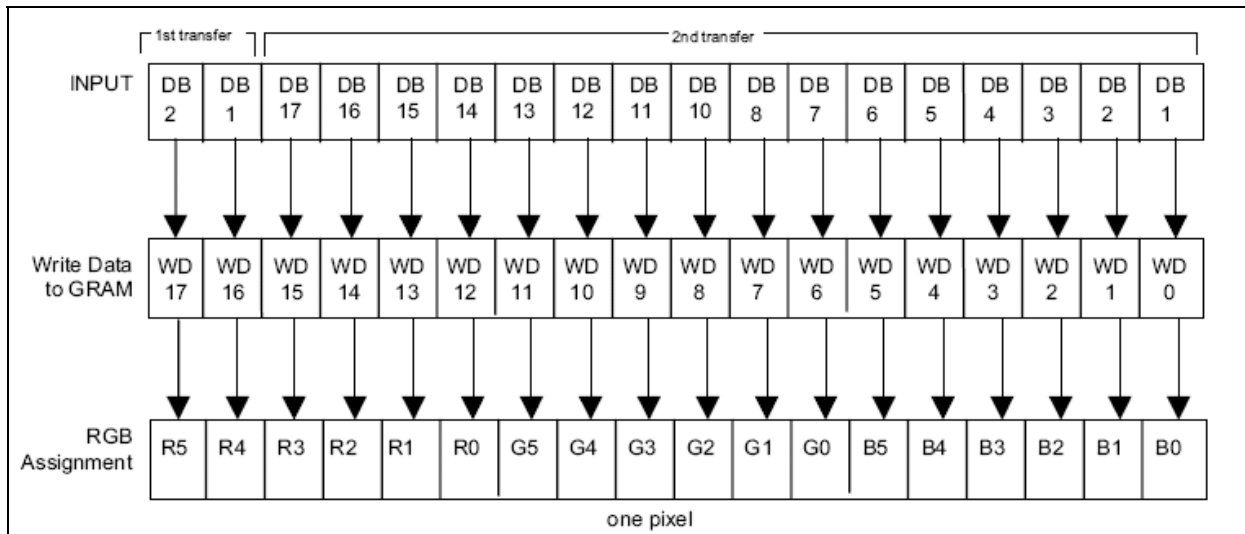


Figure 5-16 16-bit interface (262,144 colors) TRI = 1, DFM = 1

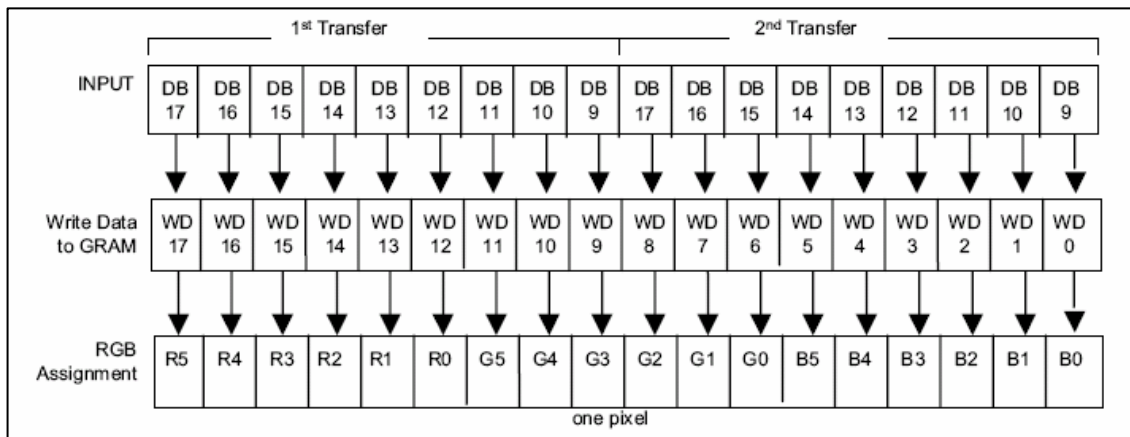


Figure 5-17 9-bit interface (262,144 colors) TRI= 0, DFM=x

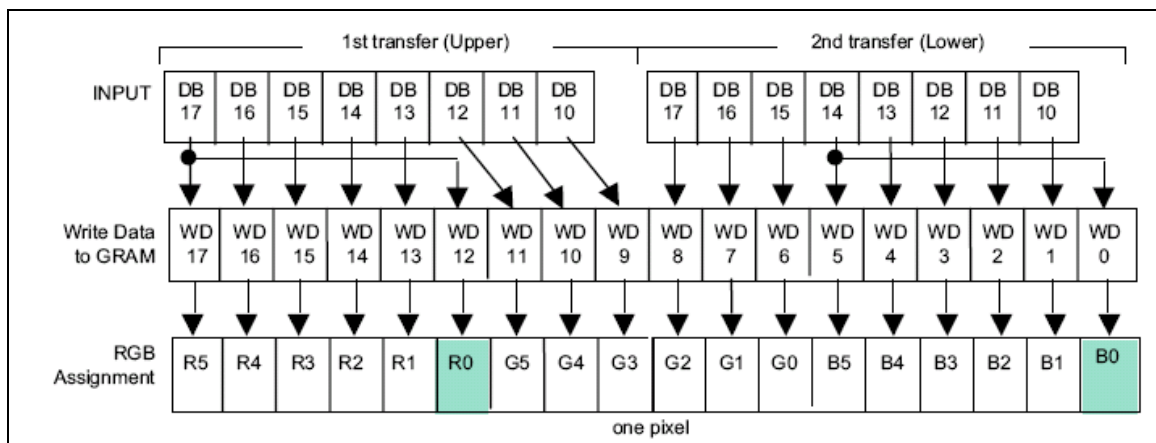


Figure 5-18 8-bit interface (65,536 colors) TRI = 0, DFM=x

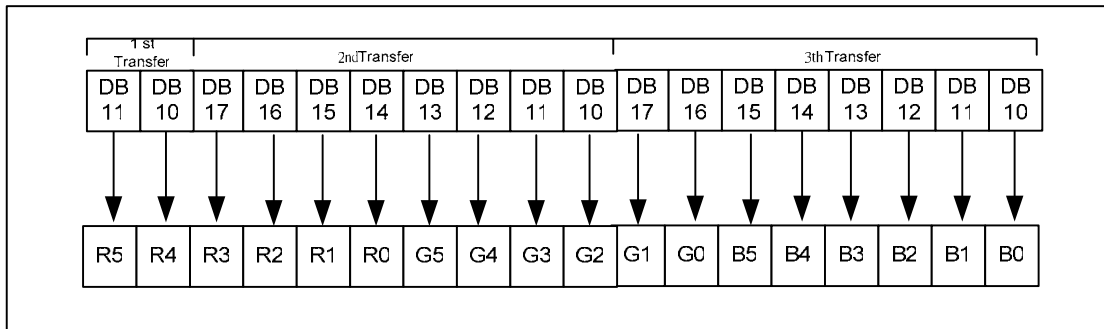


Figure 5-19 8-bit interface (262,144 colors) TRI = 1, DFM=0.

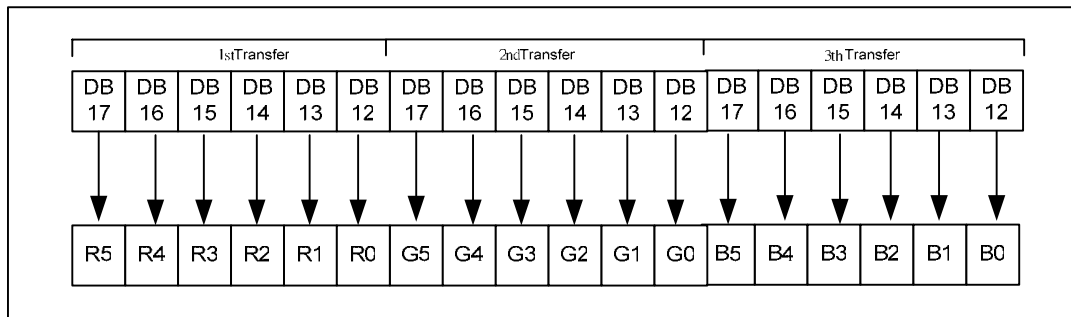
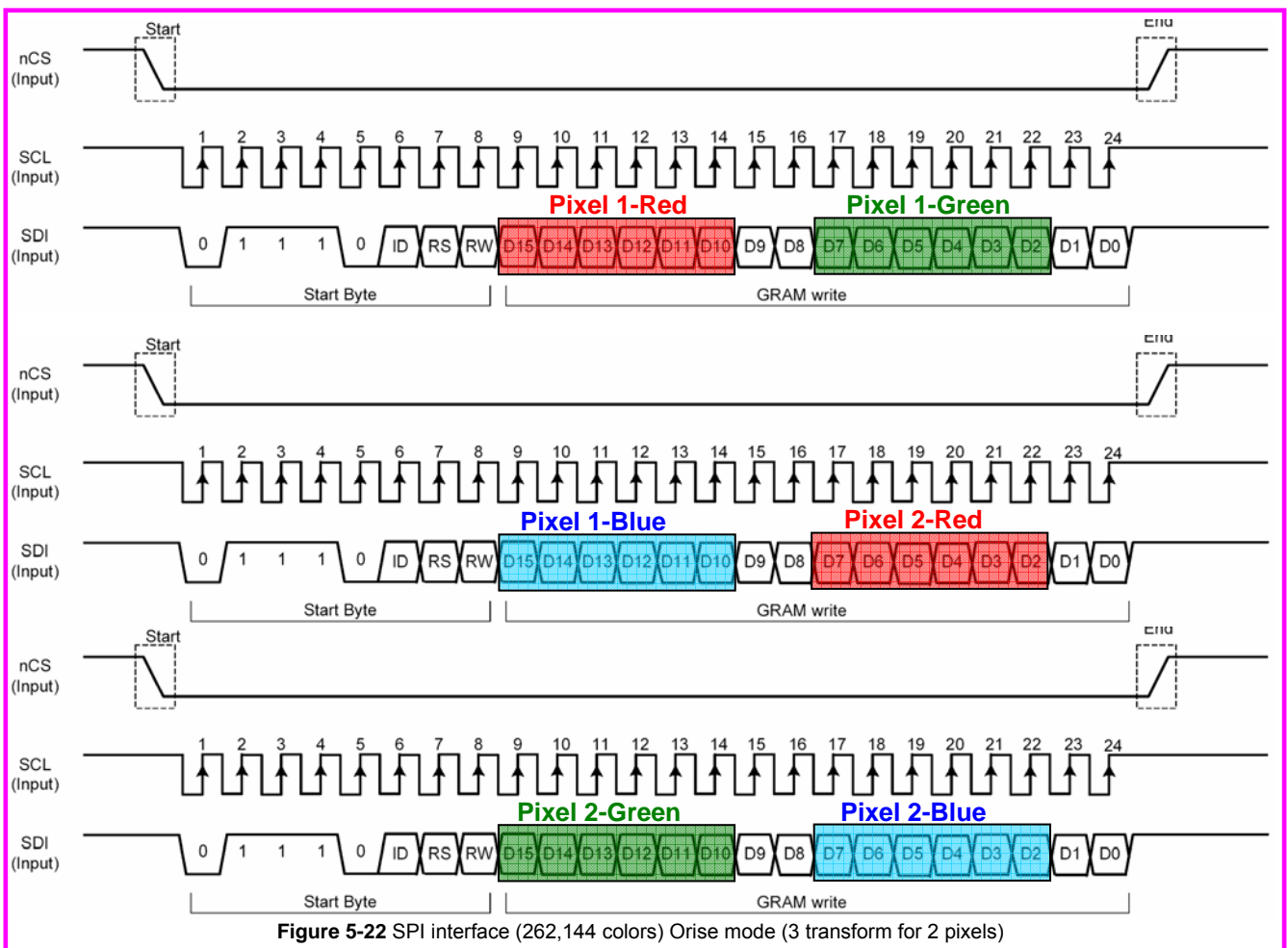
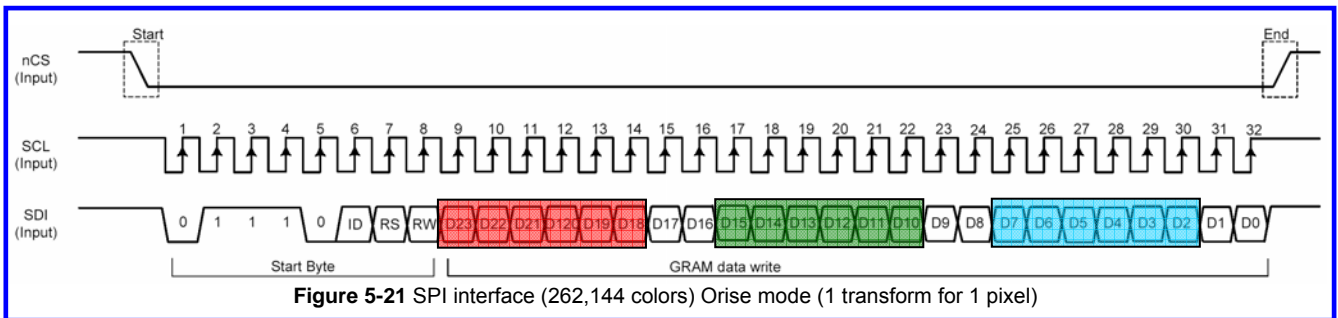


Figure 5-20 8-bit interface (262,144 colors) TRI = 1, DFM=1



★Orise Mode: Please contact OriseTech and request the initial code for the SPI 262K mode.

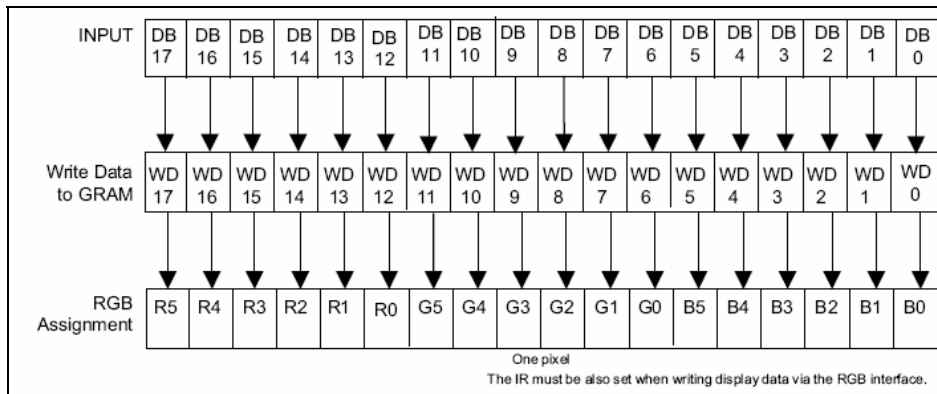


Figure 5-23 18-bit RGB interface (262,144 colors) ; RIM=00

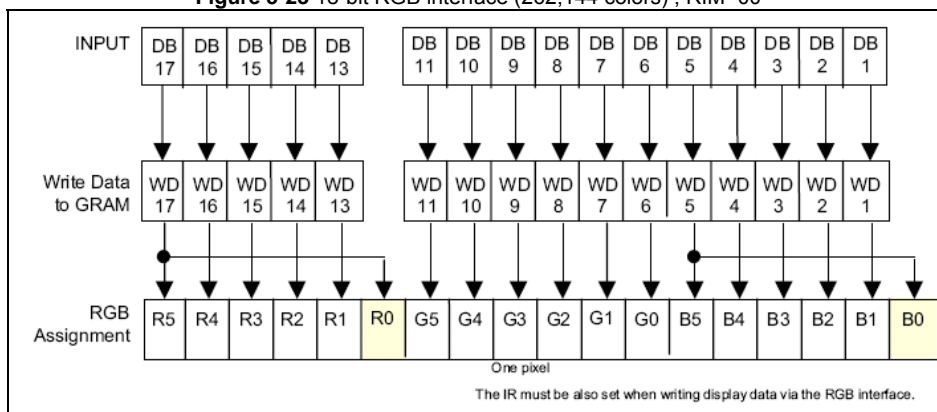


Figure 5-24 16-bit RGB interface (65,563 colors) ; RIM=01

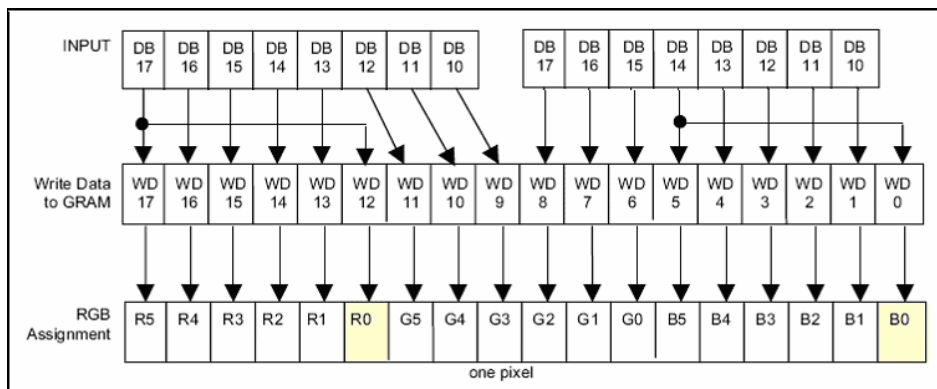


Figure 5-25 8-bit RGB interface (65,563 colors) ; RIM=11

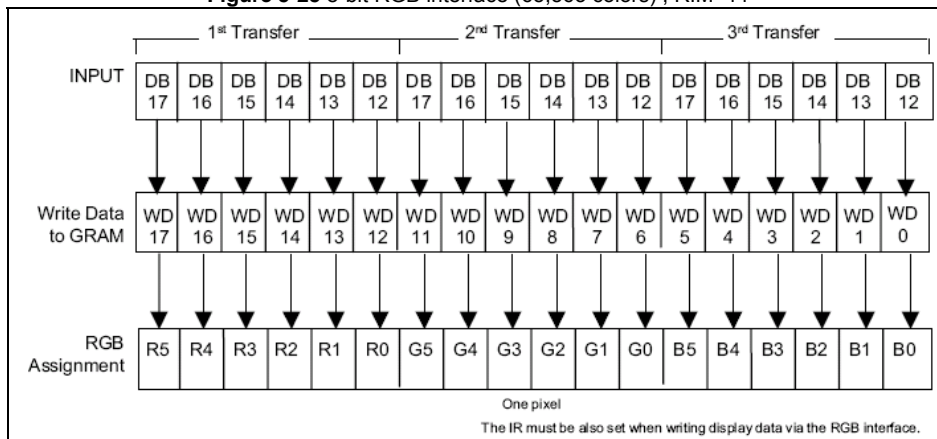


Figure 5-26 6-bit RGB interface (262,144 colors) ; RIM=10

OTM3225C supports external (RGB) interface. In RGB interface mode, all graphic data are stored in GRAM. To meet the diverse requirement of small size LCD panel, OTM3225C also supports in a fix window using RGB interface and outside the window still use system interface.

In RGB interface mode, data writing to the internal RAM is synchronized with DOTCLK during ENABLE = "Low". Set ENABLE "High" to terminate writing data to RAM. Wait for a write/read bus cycle time. If accessing internal RAM using the RGB interface is desired after accessing the RAM via the system interface. **Figure 5-27** illustrates the timing diagram while RGB and system interface are both use in the same time.

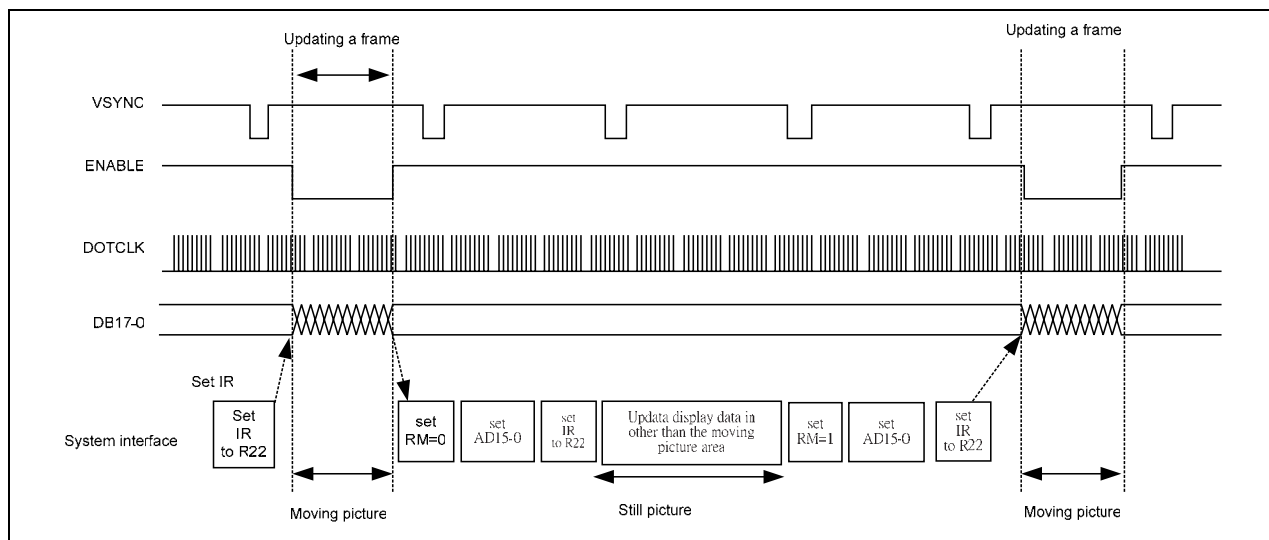


Figure 5-27

5.2.21. Read Data Read from GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	RAM Read data (RD17-0) The DB17-0 pin assignment is different in different interface modes.															

R22 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

Note 1: The LSBs of R and B dots cannot read out, when the 8 or 16-bit interface is selected,

Note 2: This register is not available with the RGB interface. **Figure 5-28 ~ Figure 5-31** illustrates the pin assignment among data bus (DB17-0), R22 (RD17-0) and GRAM in read data instruction.

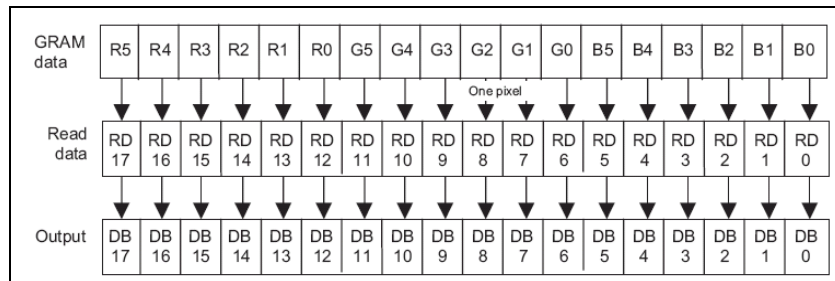


Figure 5-28 18-bit interface

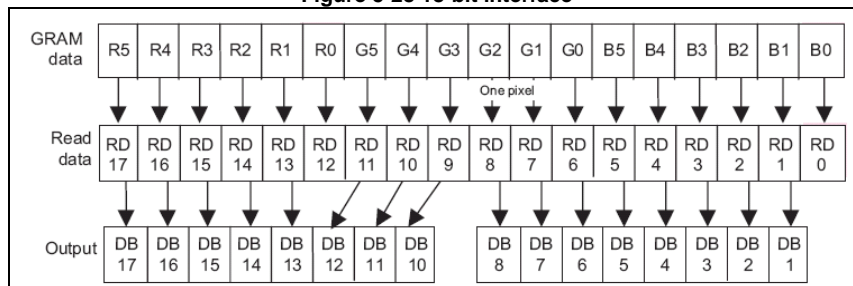


Figure 5-29 16-bit interface

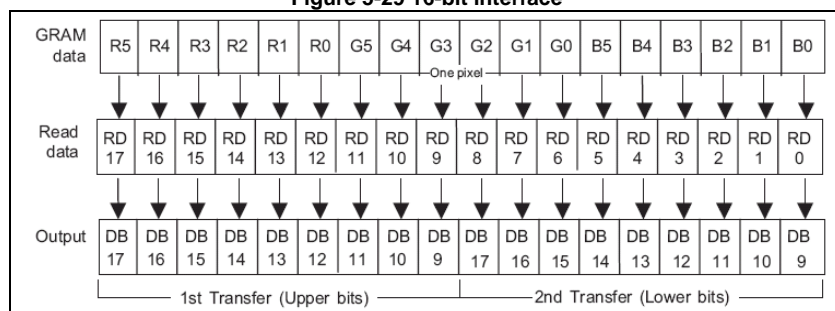


Figure 5-30 9-bit interface

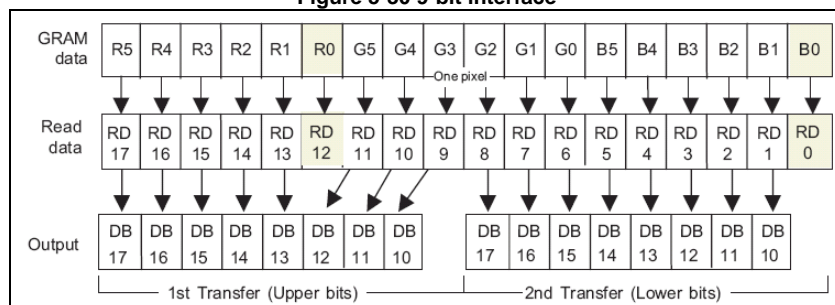


Figure 5-31 8-bit interface / SPI(65K color)

5.2.22. Power Control 7 (R29h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

VCM [5:0]: These pins are to set the factor for generating VCOMH.

Table 5-24 summarized the factor of VREG1OUT

Table 5-24

VCM[5:0]	VCOMH voltage
6'h00	VREG1OUT x 0.685
6'h01	VREG1OUT x 0.690
6'h02	VREG1OUT x 0.695
6'h03	VREG1OUT x 0.700
6'h04	VREG1OUT x 0.705
6'h05	VREG1OUT x 0.710
6'h06	VREG1OUT x 0.715
6'h07	VREG1OUT x 0.720
6'h08	VREG1OUT x 0.725
6'h09	VREG1OUT x 0.730
6'h0A	VREG1OUT x 0.735
6'h0B	VREG1OUT x 0.740
6'h0C	VREG1OUT x 0.745
6'h0D	VREG1OUT x 0.750
6'h0E	VREG1OUT x 0.755
6'h0F	VREG1OUT x 0.760
6'h10	VREG1OUT x 0.765
6'h11	VREG1OUT x 0.770
6'h12	VREG1OUT x 0.775
6'h13	VREG1OUT x 0.780
6'h14	VREG1OUT x 0.785
6'h15	VREG1OUT x 0.790
6'h16	VREG1OUT x 0.795
6'h17	VREG1OUT x 0.800
6'h18	VREG1OUT x 0.805
6'h19	VREG1OUT x 0.810
6'h1A	VREG1OUT x 0.815
6'h1B	VREG1OUT x 0.820
6'h1C	VREG1OUT x 0.825
6'h1D	VREG1OUT x 0.830
6'h1E	VREG1OUT x 0.835
6'h1F	VREG1OUT x 0.840

VCM[5:0]	VCOMH voltage
6'h20	VREG1OUT x 0.845
6'h21	VREG1OUT x 0.850
6'h22	VREG1OUT x 0.855
6'h23	VREG1OUT x 0.860
6'h24	VREG1OUT x 0.865
6'h25	VREG1OUT x 0.870
6'h26	VREG1OUT x 0.875
6'h27	VREG1OUT x 0.880
6'h28	VREG1OUT x 0.885
6'h29	VREG1OUT x 0.890
6'h2A	VREG1OUT x 0.895
6'h2B	VREG1OUT x 0.900
6'h2C	VREG1OUT x 0.905
6'h2D	VREG1OUT x 0.910
6'h2E	VREG1OUT x 0.915
6'h2F	VREG1OUT x 0.920
6'h30	VREG1OUT x 0.925
6'h31	VREG1OUT x 0.930
6'h32	VREG1OUT x 0.935
6'h33	VREG1OUT x 0.940
6'h34	VREG1OUT x 0.945
6'h35	VREG1OUT x 0.950
6'h36	VREG1OUT x 0.955
6'h37	VREG1OUT x 0.960
6'h38	VREG1OUT x 0.965
6'h39	VREG1OUT x 0.970
6'h3A	VREG1OUT x 0.975
6'h3B	VREG1OUT x 0.980
6'h3C	VREG1OUT x 0.985
6'h3D	VREG1OUT x 0.990
6'h3E	VREG1OUT x 0.995
6'h3F	VREG1OUT x 0.1000

5.2.23. Frame rate control (R2Bh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS3	FRS2	FRS1	FRS0

FRS[4:0] Set the oscillator frequency to change frame rate.

Table 5-25 summarized the oscillator frequency and the frame rate.

Note 1: The frame rate is relative to DIVI[1:0] ; RTNI[4:0] ; NL[5:0] ; BP[3:0] and FP[3:0] bits.

Table 5-25 (BP+FP=9; RTNI=0 ; DIVI=0)

FRS[3:0]	OSC frequency	Frame rate
6'h00	375K	30 Hz
6'h01	387K	31 Hz
6'h02	413K	33 Hz
6'h03	437K	35 Hz
6'h04	475K	38 Hz
6'h05	500K	40 Hz
6'h06	537K	43 Hz
6'h07	587K	47 Hz

FRS[3:0]	OSC frequency	Frame rate
6'h08	637K	51 Hz
6'h09	700K	56 Hz
6'h0A	775K	62 Hz
6'h0B	875K	70 Hz
6'h0C	1000K	80 Hz
6'h0D	1162K	93 Hz
6'h0E	1400K	112 Hz
6'h0F	1400K	112 Hz

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{f_{osc}}{\text{Clock cycles per line} \times \text{Division ratio} \times (\text{Line} + \text{BP} + \text{LP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillator (FRS bits)

Line: number of lines for driving liquid crystal (NL bits)

Division ratio: DIVI bits

Clock cycles per line: RTNI bits

FP: the number of lines for the front porch period (FP bits)

BP: the number of lines for the back porch period (BP bits)

5.2.24. γ Control (R30h to R3Dh)

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R30	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP5[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN5[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3C	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3D	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

γ Control (R30h to R3Dh): OTM3225C provides 10 gamma registers to fine tune gamma output voltage.

KP5-0[2:0]: γ fine tune registers for positive polarity.

RP1-0[2:0]: γ gradient registers for positive polarity.

VRP1-0[4:0]: γ amplitude registers for positive polarity.

KN5-0[2:0]: γ fine tune registers for positive polarity.

RN1-0[2:0]: γ gradient registers for positive polarity.

VRN1-0[4:0]: γ amplitude registers for positive polarity.

5.2.25. Window Horizontal RAM Address Start (R50h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

5.2.26. Window Horizontal RAM Address End (R51h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0

5.2.27. Window Vertical RAM Address Start (R52h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

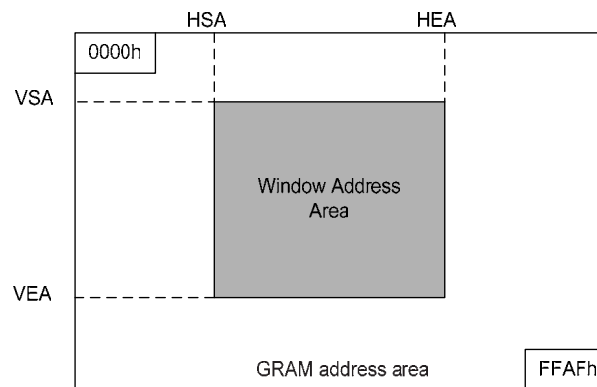
5.2.28. Window Vertical RAM Address End (R53h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0

HSA7-0/HEA7-0: OTM3225C provides window access function. Set HSA7-0 and HEA7-0 represent the start address and end address of the window function in horizontal direction. To use window-accessing function, HSA and HEA bits must be set before starting RAM write operation. Be aware that "00" h ≤ HSA7-0 < HEA7-0 ≤ "EF" h and HEA-HSA ≥ "01" h.

VSA8-0/VEA8-0: OTM3225C provides window access function. Set VSA8-0 and VEA8-0 represent the start address and end address of the window in vertical direction. To use window accessing function, VSA and VEA bits must be set before starting RAM write operation. Be aware that "00" h ≤ VSA8-0 < VEA8-0 ≤ 9'h13F.

Figure 5-32. illustrates the window-accessing function using R50h~R53h.


5.2.29. Gate Driver Scan Control (R60h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the SCN5-0 bits can specify the starting position of the gate driver. The start position of gate driver is determined by the combination of the setting of GS and SM.

Table 5-26 summarized the starting position for each SCN5-0 setting.

Table 5-26

SCN[5:0]	Scan Start Position (Gate line)			
	SM=0		SM=1	
	GS = "0"	GS = "1"	GS = "0"	GS = "1"
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G2	G96
6'h0F	G121	G200	G18	G80
6'h10	G129	G192	G34	G64
6'h11	G137	G184	G50	G48
6'h12	G145	G176	G66	G32
6'h13	G153	G168	G82	G16
6'h14	G161	G160	G98	G319
6'h15	G169	G152	G114	G303
6'h16	G177	G144	G130	G287
6'h17	G185	G136	G146	G271
6'h18	G193	G128	G162	G255
6'h19	G201	G120	G178	G239
6'h1A	G209	G112	G194	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28~3F	Setting disabled			

NL5-0: Set the number of gate lines for different resolution of display panel. The combination of NL5-NL0 represents the gate line number are summarized at **Table 5-27**.

Table 5-27

NL[5:0]	Display Size	Drive lines
6'h00	720 x 8 dots	8
6'h01	720 x 16 dots	16
6'h02	720 x 24 dots	24
...
6'h1F	720 x 256 dots	256
6'h20	720 x 264 dots	264
6'h21	720 x 272 dots	272
6'h22	720 x 280 dots	280
6'h23	720 x 288 dots	288
6'h24	720 x 296 dots	296
6'h25	720 x 304 dots	304
6'h26	720 x 312 dots	312
6'h27	720 x 320 dots	320

Note 1: Be sure that $NL[5:0] \geq SCN[5:0]$.

Note 2: Be sure that $NL[5:0] \leq 6'h27$.

GS: Shift direction of the gate driver output selection. When GS="0", gate driver shift from G1 to G320. When GS = "1", gate driver shift from G320 to G1.

5.2.30. Driver Output Control (R61h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input.

Table 5-28 summarized REV bit function.

Table 5-28

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	18'h3FFFF	V63	V0

VLE: OTM3225C provides vertical scrolling function which can be set by VLE bit.

VLE = "1", vertical scrolling function enable. The amount of scrolling line from the first line is determined by VL[8:0].

VLE = "0", normal display.

NDL: set the source diver output level in non-lit area..

NDL = "1", .

NDL = "0", .

5.2.31. Vertical Scroll Control (R6Ah)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL8-0: OTM3225C provides scrolling function. The start position for displaying the image is shifted vertically by the number of lines based on the setting of the VL8-0 bits. Be aware that the vertical scrolling function is not available in the external (RGB) display interface mode. **Table 5-29** summarized the function of VL8-0 setting.

Table 5-29

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	0	1	0	2 lines
	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	1	319 lines
1	0	1	0	0	0	0	0	0	320 lines

Note 1: Be sure that VL[8:0] ≤ 9'h140.

5.2.32. Display Position – Partial Display 1 (R80h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P08	PTD P07	PTD P06	PTD P05	PTD P04	PTD P03	PTD P02	PTD P01	PTD P00

5.2.33. RAM Address Start – Partial Display 1 (R81h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A08	PTS A07	PTS A06	PTS A05	PTS A04	PTS A03	PTS A02	PTS A01	PTS A00

5.2.34. RAM Address End – Partial Display 1 (R82h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A08	PTE A07	PTE A06	PTE A05	PTE A04	PTE A03	PTE A02	PTE A01	PTE A00

5.2.35. Display Position – Partial Display 2 (R83h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTD P18	PTD P17	PTD P16	PTD P15	PTD P14	PTD P13	PTD P12	PTD P11	PTD P10

5.2.36. RAM Address Start – Partial Display 2 (R84h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTS A18	PTS A17	PTS A16	PTS A15	PTS A14	PTS A13	PTS A12	PTS A11	PTS A10

5.2.37. RAM Address End – Partial Display 2 (R85h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	PTE A18	PTE A17	PTE A16	PTE A15	PTE A14	PTE A13	PTE A12	PTE A11	PTE A10

PTDP0[8:0]: Set the physical starting position of partial display 1 on the LCD panel

PTDP1[8:0]: Set the physical starting position of partial display 2 on the LCD panel

The partial display 1 and partial display 2 should not overlap with each other. And make sure the PTDP0[8:0] < PTDP1[8:0].

PTSA0[8:0]: Set the start line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

PTEA0[8:0]: Set the end line address of display RAM of partial display 1 which will be display according to PTDP0[8:0].

Note 1:Make sure PTSA0<=PTEA0

PTSA1[8:0]: Set the start line address of display RAM of partial display2 which will be display according to PTDP1[8:0].

PTEA1[8:0]: Set the end line address of display RAM of partial display2 which will be display according to PTDP1[8:0]

Note 1:Make sure PTSA1<=PTEA1

5.2.38. Panel Interface Control 1 (R90h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIV11	DIV10	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0

RTNI4-0: Set the clock cycle per line **Table 5-30** summarized the function of RTNI4-0 setting.

Table 5-30

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Clock Cycles per line
0	0	0	0	0	38 clocks
0	0	0	0	1	40 clocks
0	0	0	1	0	42 clocks
0	0	0	1	1	44 clocks
0	0	1	0	0	46 clocks
0	0	1	0	1	48 clocks
0	0	1	1	0	50 clocks
0	0	1	1	1	52 clocks
0	1	0	0	0	54 clocks
0	1	0	0	1	56 clocks
0	1	0	1	0	58 clocks
0	1	0	1	1	60 clocks
0	1	1	0	0	62 clocks
0	1	1	0	1	64 clocks
0	1	1	1	0	66 clocks
0	1	1	1	1	68 clocks
1	0	0	0	0	38 clocks
1	0	0	0	1	40 clocks
1	0	0	1	0	42 clocks
1	0	0	1	1	44 clocks
1	0	1	0	0	46 clocks
1	0	1	0	1	48 clocks
1	0	1	1	0	50 clocks
1	0	1	1	1	52 clocks
1	1	0	0	0	54 clocks
1	1	0	0	1	56 clocks
1	1	0	1	0	58 clocks
1	1	0	1	1	60 clocks
1	1	1	0	0	62 clocks
1	1	1	0	1	64 clocks
1	1	1	1	0	66 clocks
1	1	1	1	1	68 clocks

DIV11-0: To specified the division ratio of internal operation clock frequency. Set the RTNI and DIV1 bits to adjust frame frequency. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In RGB interface mode, the DIV11-0 bits are disabled. **Table 5-31** summarized the function of DIV11-0 setting.

Table 5-31

DIV11	DIV10	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

5.2.39. Panel Interface Control 2 (R92h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	NOWI2	NOWI1	NOWI0	0	0	0	0	0	0	0	0

NOWI [2:0]: Set the adjacent gate driver output non-overlap period. **Table 5-32** summarized the function of NOWI2-0 setting.

Table 5-32

NOWI2	NOWI1	NOWI0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	2 clocks
0	0	1	2 clocks
0	1	0	4 clocks
0	1	1	6 clocks
1	0	0	8 clocks
1	0	1	10 clocks
1	1	0	12 clocks
1	1	1	14 clocks

5.2.40. Panel Interface control 4 (R95h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0

RTNE5-0: Set the clock cycle per line **Table 5-33** summarized the function of RTNE5-0 setting.

Table 5-33

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
0	1/0	0	0	0	0	16 clocks
0	1/0	0	0	0	1	17 clocks
0	1/0	0	0	1	0	18 clocks
0	1/0	0	0	1	1	19 clocks
0	1/0	0	1	0	0	20 clocks
0	1/0	0	1	0	1	21 clocks
0	1/0	0	1	1	0	22 clocks
0	1/0	0	1	1	1	23 clocks
0	1/0	1	0	0	0	24 clocks
0	1/0	1	0	0	1	25 clocks
0	1/0	1	0	1	0	26 clocks
0	1/0	1	0	1	1	27 clocks
0	1/0	1	1	0	0	28 clocks
0	1/0	1	1	0	1	29 clocks
0	1/0	1	1	1	0	30 clocks
0	1/0	1	1	1	1	31 clocks
1	1	0	0	0	0	32 clocks
1	1	0	0	0	1	33 clocks
1	1	0	0	1	0	34 clocks
1	1	0	0	1	1	35 clocks
1	1	0	1	0	0	36 clocks
1	1	0	1	0	1	37 clocks
1	1	0	1	1	0	38 clocks
1	1	0	1	1	1	39 clocks
1	1	1	0	0	0	40 clocks
1	1	1	0	0	1	41 clocks
1	1	1	0	1	0	42 clocks
1	1	1	0	1	1	43 clocks
1	1	1	1	0	0	44 clocks
1	1	1	1	0	1	45 clocks
1	1	1	1	1	0	46 clocks
1	1	1	1	1	1	47 clocks
1	1	0	0	0	0	48 clocks
1	1	0	0	0	1	49 clocks
1	1	0	0	1	0	50 clocks
1	1	0	0	1	1	51 clocks
1	1	0	1	0	0	52 clocks

RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Clock Cycles per line
1	1	0	1	0	1	53 clocks
1	1	0	1	1	0	54 clocks
1	1	0	1	1	1	55 clocks
1	1	1	0	0	0	56 clocks
1	1	1	0	0	1	57 clocks
1	1	1	0	1	0	58 clocks
1	1	1	0	1	1	59 clocks
1	1	1	1	0	0	60 clocks
1	1	1	1	0	1	61 clocks
1	1	1	1	1	0	62 clocks
1	1	1	1	1	1	63 clocks

DIVE1-0: To specified the division ratio of internal operation clock frequency. Set the RTNE and DIVE bits to adjust Source line charge time. Be aware of that if the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. Moreover, In system interface mode, the DIVE1-0 bits are disabled. **Table 5-34** summarized the function of DIVE1-0 setting.

Table 5-34

DIVE1	DIVE0	Division Ratio	Internal Operation Clock Frequency
0	0	4	fosc / 4
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

5.2.41. Panel Interface Control 5 (R97h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	NOW E3	NOW E2	NOW E1	NOW E0	0	0	0	0	0	0	0	0

NOWE [3:0]: Set the adjacent gate driver output non-overlap period in RGB interface. **Table 5-35** summarized the function of NOWE3-0 setting.

Table 5-35

NOWE3	NOWE2	NOWE1	NOWE0	Gate output non-overlap period Internal Operation (reference clock: internal oscillator)
0	0	0	0	2 clocks
0	0	0	1	2 clocks
0	0	1	0	4 clocks
0	0	1	1	6 clocks
0	1	0	0	8 clocks
0	1	0	1	10 clocks
0	1	1	0	12 clocks
0	1	1	1	14 clocks
1	0	0	0	16 clocks
1	0	0	1	18 clocks
1	0	1	0	20 clocks
1	0	1	1	22 clocks
1	1	0	0	24 clocks
1	1	0	1	26clocks
1	1	1	0	28 clocks
1	1	1	1	30 clocks

5.2.42. Write Display Brightness Value (RB1h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to adjust the brightness value of the display.

DBV[7:0]: Set the adjacent brightness value of the display. In principle relationship is that the 00h value means the lowest brightness and FFh value means the highest brightness.

5.2.43. Read Display Brightness Value (RB2h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to return the brightness value of the display.

DBV [7:0] is reset when display is in sleep-in mode.

DBV [7:0] is '0' when bit BCTRL of "5.2.44 Write CTRL Display (B3h)" command is '0'.

DBV [7:0] is manual set brightness specified with "5.2.44 Write CTRL Display (B3h)" command when bit BCTRL is '1'.

When bit BCTRL of "5.2.44 Write CTRL Display (B3h)" command is '1' and bit C1/C0 of "5.2.46 Write Content Adaptive Brightness Control (B5h)" are '0', DBV[7:0] output is the brightness value specified with "5.2.42 Write Display Brightness (B1h)" command.

5.2.44. Write CTRL Display Value (RB3h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	LED_ ON	BC_OUT_ INV	0	0	BCTRL	0	DD	BL	0	0

This command is used to control display brightness.

LED_ON: This bit is used to control LENON pin.

0 = Off

1 = On

BC_OUT_INV: This bit is used to control BC_OUT signal polarity.

0 = Off : Original polarity of BC_OUT signal.

1 = On : Inversed polarity of BC_OUT signal.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display and keyboard.

0 = Off (Brightness registers are 00h, DBV[7..0])

1 = On (Brightness registers are active, according to the other parameters.)

DD: Display Dimming Control:

DD = 0: Display Dimming is off

DD = 1: Display Dimming is on

BL: Backlight Control On/Off

0 = Off (Completely turn off backlight circuit. Control lines must be low.)

1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

5.2.45. Read CTRL Display Value (RB4h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	LED_ON	BC_OUT_INV	0	0	BCTRL	0	DD	BL	0	0

This command returns brightness control values, see chapter: "5.2.44 Write CTRL Display (B3h)".

5.2.46. Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

This command is used to set parameters for image content based adaptive brightness control functionality. **Table 5-36** summarized the function of C1-0 setting.

Table 5-36

C1	C0	Function
0	0	Off
0	1	User Interface Image
1	0	Still Picture
1	1	Moving Image

5.2.47. Read Content Adaptive Brightness Control Value (RB6h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C1	C0

This command is used to read the settings for image content based adaptive brightness control functionality

5.2.48. Write CABC Minimum Brightness Value (RBEh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

This command is used to set the minimum brightness value of the display for CABC function.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

5.2.49. Read CABC Minimum Brightness Value (RBFh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	1	0	0	0	0	0	0	0	0	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. CMB[7:0] is CABC minimum brightness specified with "5.2.48 Write CABC minimum brightness (BEh)" command.

6. GRAM
Table 6-1 GRAM address and display panel position (SS = "0")

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	...	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720	
GS=0	GS=1	DB17-0			DB17-0			DB17-0			DB17-0			...	DB17-0			DB17-0			DB17-0			DB17-0			
G1	G320	"00000"H	"00001"H	"00002"H	"00003"H	"00004"H	"00005"H	"00006"H	"00007"H	"00008"H	"00009"H	"00010"H	"00011"H	"00012"H	...	"000EC"H	"000ED"H	"000EE"H	"000EF"H	"000F0"H	"000F1"H	"000F2"H	"000F3"H	"000F4"H	"000F5"H	"000F6"H	"000F7"H
G2	G319	"00100"H	"00101"H	"00102"H	"00103"H	"00104"H	"00105"H	"00106"H	"00107"H	"00108"H	"00109"H	"00110"H	"00111"H	"00112"H	...	"001EC"H	"001ED"H	"001EE"H	"001EF"H	"001F0"H	"001F1"H	"001F2"H	"001F3"H	"001F4"H	"001F5"H	"001F6"H	"001F7"H
G3	G318	"00200"H	"00201"H	"00202"H	"00203"H	"00204"H	"00205"H	"00206"H	"00207"H	"00208"H	"00209"H	"00210"H	"00211"H	"00212"H	...	"002EC"H	"002ED"H	"002EE"H	"002EF"H	"002F0"H	"002F1"H	"002F2"H	"002F3"H	"002F4"H	"002F5"H	"002F6"H	"002F7"H
G4	G317	"00300"H	"00301"H	"00302"H	"00303"H	"00304"H	"00305"H	"00306"H	"00307"H	"00308"H	"00309"H	"00310"H	"00311"H	"00312"H	...	"003EC"H	"003ED"H	"003EE"H	"003EF"H	"003F0"H	"003F1"H	"003F2"H	"003F3"H	"003F4"H	"003F5"H	"003F6"H	"003F7"H
G5	G316	"00400"H	"00401"H	"00402"H	"00403"H	"00404"H	"00405"H	"00406"H	"00407"H	"00408"H	"00409"H	"00410"H	"00411"H	"00412"H	...	"004EC"H	"004ED"H	"004EE"H	"004EF"H	"004F0"H	"004F1"H	"004F2"H	"004F3"H	"004F4"H	"004F5"H	"004F6"H	"004F7"H
G6	G315	"00500"H	"00501"H	"00502"H	"00503"H	"00504"H	"00505"H	"00506"H	"00507"H	"00508"H	"00509"H	"00510"H	"00511"H	"00512"H	...	"005EC"H	"005ED"H	"005EE"H	"005EF"H	"005F0"H	"005F1"H	"005F2"H	"005F3"H	"005F4"H	"005F5"H	"005F6"H	"005F7"H
G7	G314	"00600"H	"00601"H	"00602"H	"00603"H	"00604"H	"00605"H	"00606"H	"00607"H	"00608"H	"00609"H	"00610"H	"00611"H	"00612"H	...	"006EC"H	"006ED"H	"006EE"H	"006EF"H	"006F0"H	"006F1"H	"006F2"H	"006F3"H	"006F4"H	"006F5"H	"006F6"H	"006F7"H
G8	G313	"00700"H	"00701"H	"00702"H	"00703"H	"00704"H	"00705"H	"00706"H	"00707"H	"00708"H	"00709"H	"00710"H	"00711"H	"00712"H	...	"007EC"H	"007ED"H	"007EE"H	"007EF"H	"007F0"H	"007F1"H	"007F2"H	"007F3"H	"007F4"H	"007F5"H	"007F6"H	"007F7"H
G9	G312	"00800"H	"00801"H	"00802"H	"00803"H	"00804"H	"00805"H	"00806"H	"00807"H	"00808"H	"00809"H	"00810"H	"00811"H	"00812"H	...	"008EC"H	"008ED"H	"008EE"H	"008EF"H	"008F0"H	"008F1"H	"008F2"H	"008F3"H	"008F4"H	"008F5"H	"008F6"H	"008F7"H
G10	G311	"00900"H	"00901"H	"00902"H	"00903"H	"00904"H	"00905"H	"00906"H	"00907"H	"00908"H	"00909"H	"00910"H	"00911"H	"00912"H	...	"009EC"H	"009ED"H	"009EE"H	"009EF"H	"009F0"H	"009F1"H	"009F2"H	"009F3"H	"009F4"H	"009F5"H	"009F6"H	"009F7"H
G11	G310	"00E00"H	"00E01"H	"00E02"H	"00E03"H	"00E04"H	"00E05"H	"00E06"H	"00E07"H	"00E08"H	"00E09"H	"00E10"H	"00E11"H	"00E12"H	...	"00EEC"H	"00EED"H	"00EEE"H	"00EEF"H	"00EF0"H	"00EF1"H	"00EF2"H	"00EF3"H	"00EF4"H	"00EF5"H	"00EF6"H	"00EF7"H
G12	G309	"00B00"H	"00B01"H	"00B02"H	"00B03"H	"00B04"H	"00B05"H	"00B06"H	"00B07"H	"00B08"H	"00B09"H	"00B10"H	"00B11"H	"00B12"H	...	"00BEC"H	"00BED"H	"00BEE"H	"00BEF"H	"00BF0"H	"00BF1"H	"00BF2"H	"00BF3"H	"00BF4"H	"00BF5"H	"00BF6"H	"00BF7"H
G13	G308	"00C00"H	"00C01"H	"00C02"H	"00C03"H	"00C04"H	"00C05"H	"00C06"H	"00C07"H	"00C08"H	"00C09"H	"00C10"H	"00C11"H	"00C12"H	...	"00CEC"H	"00CED"H	"00CEE"H	"00CEF"H	"00CF0"H	"00CF1"H	"00CF2"H	"00CF3"H	"00CF4"H	"00CF5"H	"00CF6"H	"00CF7"H
G14	G307	"00D00"H	"00D01"H	"00D02"H	"00D03"H	"00D04"H	"00D05"H	"00D06"H	"00D07"H	"00D08"H	"00D09"H	"00D10"H	"00D11"H	"00D12"H	...	"00DEC"H	"00DED"H	"00DEE"H	"00DEF"H	"00DF0"H	"00DF1"H	"00DF2"H	"00DF3"H	"00DF4"H	"00DF5"H	"00DF6"H	"00DF7"H
G15	G306	"00E00"H	"00E01"H	"00E02"H	"00E03"H	"00E04"H	"00E05"H	"00E06"H	"00E07"H	"00E08"H	"00E09"H	"00E10"H	"00E11"H	"00E12"H	...	"00EEC"H	"00EED"H	"00EEE"H	"00EEF"H	"00EF0"H	"00EF1"H	"00EF2"H	"00EF3"H	"00EF4"H	"00EF5"H	"00EF6"H	"00EF7"H
G16	G305	"00F00"H	"00F01"H	"00F02"H	"00F03"H	"00F04"H	"00F05"H	"00F06"H	"00F07"H	"00F08"H	"00F09"H	"00F10"H	"00F11"H	"00F12"H	...	"00FEC"H	"00FED"H	"00FEE"H	"00FEF"H	"00FF0"H	"00FF1"H	"00FF2"H	"00FF3"H	"00FF4"H	"00FF5"H	"00FF6"H	"00FF7"H
G17	G304	"01000"H	"01001"H	"01002"H	"01003"H	"01004"H	"01005"H	"01006"H	"01007"H	"01008"H	"01009"H	"01010"H	"01011"H	"01012"H	...	"010EC"H	"010ED"H	"010EE"H	"010EF"H	"010F0"H	"010F1"H	"010F2"H	"010F3"H	"010F4"H	"010F5"H	"010F6"H	"010F7"H
G18	G303	"01100"H	"01101"H	"01102"H	"01103"H	"01104"H	"01105"H	"01106"H	"01107"H	"01108"H	"01109"H	"01110"H	"01111"H	"01112"H	...	"011EC"H	"011ED"H	"011EE"H	"011EF"H	"011F0"H	"011F1"H	"011F2"H	"011F3"H	"011F4"H	"011F5"H	"011F6"H	"011F7"H
G19	G302	"01200"H	"01201"H	"01202"H	"01203"H	"01204"H	"01205"H	"01206"H	"01207"H	"01208"H	"01209"H	"01210"H	"01211"H	"01212"H	...	"012EC"H	"012ED"H	"012EE"H	"012EF"H	"012F0"H	"012F1"H	"012F2"H	"012F3"H	"012F4"H	"012F5"H	"012F6"H	"012F7"H
G20	G301	"01300"H	"01301"H	"01302"H	"01303"H	"01304"H	"01305"H	"01306"H	"01307"H	"01308"H	"01309"H	"01310"H	"01311"H	"01312"H	...	"013EC"H	"013ED"H	"013EE"H	"013EF"H	"013F0"H	"013F1"H	"013F2"H	"013F3"H	"013F4"H	"013F5"H	"013F6"H	"013F7"H
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
G313	G8	"13800"H	"13801"H	"13802"H	"13803"H	"13804"H	"13805"H	"13806"H	"13807"H	"13808"H	"13809"H	"13810"H	"13811"H	"13812"H	...	"138EC"H	"138ED"H	"138EE"H	"138EF"H	"138F0"H	"138F1"H	"138F2"H	"138F3"H	"138F4"H	"138F5"H	"138F6"H	"138F7"H
G314	G7	"13900"H	"13901"H	"13902"H	"13903"H	"13904"H	"13905"H	"13906"H	"13907"H	"13908"H	"13909"H	"13910"H	"13911"H	"13912"H	...	"139EC"H	"139ED"H	"139EE"H	"139EF"H	"139F0"H	"139F1"H	"139F2"H	"139F3"H	"139F4"H	"139F5"H	"139F6"H	"139F7"H
G315	G6	"13A00"H	"13A01"H	"13A02"H	"13A03"H	"13A04"H	"13A05"H	"13A06"H	"13A07"H	"13A08"H	"13A09"H	"13A10"H	"13A11"H	"13A12"H	...	"13AEC"H	"13AED"H	"13AEE"H	"13AEF"H	"13AF0"H	"13AF1"H	"13AF2"H	"13AF3"H	"13AF4"H	"13AF5"H	"13AF6"H	"13AF7"H
G316	G5	"13B00"H	"13B01"H	"13B02"H	"13B03"H	"13B04"H	"13B05"H	"13B06"H	"13B07"H	"13B08"H	"13B09"H	"13B10"H	"13B11"H	"13B12"H	...	"13BEC"H	"13BED"H	"13BEE"H	"13BEF"H	"13BF0"H	"13BF1"H	"13BF2"H	"13BF3"H	"13BF4"H	"13BF5"H	"13BF6"H	"13BF7"H
G317	G4	"13C00"H	"13C01"H	"13C02"H	"13C03"H	"13C04"H	"13C05"H	"13C06"H	"13C07"H	"13C08"H	"13C09"H	"13C10"H	"13C11"H	"13C12"H	...	"13CEC"H	"13CED"H	"13CEE"H	"13CEF"H	"13CF0"H	"13CF1"H	"13CF2"H	"13CF3"H	"13CF4"H	"13CF5"H	"13CF6"H	"13CF7"H
G318	G3	"13D00"H	"13D01"H	"13D02"H	"13D03"H	"13D04"H	"13D05"H	"13D06"H	"13D07"H	"13D08"H	"13D09"H	"13D10"H	"13D11"H	"13D12"H	...	"13DEC"H	"13DED"H	"13DEE"H	"13DEF"H	"13DF0"H	"13DF1"H	"13DF2"H	"13DF3"H	"13DF4"H	"13DF5"H	"13DF6"H	"13DF7"H
G319	G2	"13E00"H	"13E01"H	"13E02"H	"13E03"H	"13E04"H	"13E05"H	"13E06"H	"13E07"H	"13E08"H	"13E09"H	"13E10"H	"13E11"H	"13E12"H	...	"13EEC"H	"13EED"H	"13EEE"H	"13EEF"H	"13EF0"H	"13EF1"H	"13EF2"H	"13EF3"H	"13EF4"H	"13EF5"H	"13EF6"H	"13EF7"H
G320	G1	"13F00"H	"13F01"H	"13F02"H	"13F03"H	"13F04"H	"13F05"H	"13F06"H	"13F07"H	"13F08"H	"13F09"H	"13F10"H	"13F11"H	"13F12"H	...	"13FEC"H	"13FED"H	"13FEE"H	"13FEF"H	"13FF0"H	"13FF1"H	"13FF2"H	"13FF3"H	"13FF4"H	"13FF5"H	"13FF6"H	"13FF7"H

Table 6-2 GRAM address and display panel position (SS = "1")

S/G pin		S1	S2	S3	S4	S5	...	S7	S8	S9	S10	S11	S12	...	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720	
GS=0	GS=1	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	...	DB17-0	DB17-0	DB17-0	DB17-0	...	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0	DB17-0
G1	G320	"000EF"H	"000EE"H	"000ED"H	"000EC"H	...	"00003"H	"00002"H	"00001"H	"00000"H																	
G2	G319	"001EF"H	"001EE"H	"001ED"H	"001EC"H	...	"00103"H	"00102"H	"00101"H	"00100"H																	
G3	G318	"002EF"H	"002EE"H	"002ED"H	"002EC"H	...	"00203"H	"00202"H	"00201"H	"00200"H																	
G4	G317	"003EF"H	"003EE"H	"003ED"H	"003EC"H	...	"00303"H	"00302"H	"00301"H	"00300"H																	
G5	G316	"004EF"H	"004EE"H	"004ED"H	"004EC"H	...	"00403"H	"00402"H	"00401"H	"00400"H																	
G6	G315	"005EF"H	"005EE"H	"005ED"H	"005EC"H	...	"00503"H	"00502"H	"00501"H	"00500"H																	
G7	G314	"006EF"H	"006EE"H	"006ED"H	"006EC"H	...	"00603"H	"00602"H	"00601"H	"00600"H																	
G8	G313	"007EF"H	"007EE"H	"007ED"H	"007EC"H	...	"00703"H	"00702"H	"00701"H	"00700"H																	
G9	G312	"008EF"H	"008EE"H	"008ED"H	"008EC"H	...	"00803"H	"00802"H	"00801"H	"00800"H																	
G10	G311	"009EF"H	"009EE"H	"009ED"H	"009EC"H	...	"00903"H	"00902"H	"00901"H	"00900"H																	
G11	G310	"00AEF"H	"00AEE"H	"00AED"H	"00AEC"H	...	"00E03"H	"00A02"H	"00A01"H	"00A00"H																	
G12	G309	"00BEF"H	"00BEE"H	"00BED"H	"00BEC"H	...	"00B03"H	"00B02"H	"00B01"H	"00B00"H																	
G13	G308	"00CEF"H	"00CEE"H	"00CED"H	"00CEC"H	...	"00C03"H	"00C02"H	"00C01"H	"00C00"H																	
G14	G307	"00DEF"H	"00DEE"H	"00DED"H	"00DEC"H	...	"00D03"H	"00D02"H	"00D01"H	"00D00"H																	
G15	G306	"00EEF"H	"00EEE"H	"00EED"H	"00EEC"H	...	"00E03"H	"00E02"H	"00E01"H	"00E00"H																	
G16	G305	"00FEF"H	"00FEE"H	"00FED"H	"00FEC"H	...	"00F03"H	"00F02"H	"00F01"H	"00F00"H																	
G17	G304	"010EF"H	"010EE"H	"010ED"H	"010EC"H	...	"01003"H	"01002"H	"01001"H	"01000"H																	
G18	G303	"011EF"H	"011EE"H	"011ED"H	"011EC"H	...	"01103"H	"01102"H	"01101"H	"01100"H																	
G19	G302	"012EF"H	"012EE"H	"012ED"H	"012EC"H	...	"01203"H	"01202"H	"01201"H	"01200"H																	
G20	G301	"013EF"H	"013EE"H	"013ED"H	"013EC"H	...	"01303"H	"01302"H	"01301"H	"01300"H																	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
G233	G8	"E8EF"H	"138EE"H	"138ED"H	"138EC"H	...	"13803"H	"13802"H	"13801"H	"13800"H																	
G234	G7	"139EF"H	"139EE"H	"139ED"H	"139EC"H	...	"13903"H	"13902"H	"13901"H	"13900"H																	
G235	G6	"13AEF"H	"13AEE"H	"13AED"H	"13AEC"H	...	"13A03"H	"13A02"H	"13A01"H	"13A00"H																	
G236	G5	"13BEF"H	"13BEE"H	"13BED"H	"13BEC"H	...	"13B03"H	"13B02"H	"13B01"H	"13B00"H																	
G237	G4	"13CEF"H	"13CEE"H	"13CED"H	"13CEC"H	...	"13C03"H	"13C02"H	"13C01"H	"13C00"H																	
G238	G3	"13DEF"H	"13DEE"H	"13DED"H	"13DEC"H	...	"13D03"H	"13D02"H	"13D01"H	"13D00"H																	
G239	G2	"13EEF"H	"13EEE"H	"13EED"H	"13EEC"H	...	"13E03"H	"13E02"H	"13E01"H	"13E00"H																	
G240	G1	"13FEF"H	"13FEE"H	"13FED"H	"13FEC"H	...	"13F03"H	"13F02"H	"13F01"H	"13F00"H																	

7. INTERFACES

The OTM3225C provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, OTM3225C provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)
3. VSYNC interface

System interface is suitable for still picture display while RGB interface and VSYNC interface are suitable for moving picture display. Be aware that RGB or VSYNC interface still can used to display still picture and system interface can also display moving picture. **Table 7-1** summarized different interfaces for different display requirement.

Table 7-1

Display State	Operation Mode	RAM access Mode(RM)	Display operation Mode (DM1-0)
Still pictures	Internal clock	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)
Low Speed moving picture	RGB interface	RGB interface (RM = 1)	Internal clock operation (DM1-0 = 00)

7.1. System Interface

The system interfaces of OTM3225C can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM3/2/1/0 pins. The system interface can set instructions and access RAM. **Table 7-2** summarized the interface corresponding to IM3-0 setting.

Table 7-2

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	0	Setting disabled	-
0	0	0	1	Setting disabled	-
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	* /ID	Serial peripheral interface (SPI)	- (Note: SPI use SDI & SDO)
0	1	1	0	Setting disabled	-
1	0	0	0	Setting disabled	-
1	0	0	1	Setting disabled	-
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled -	-

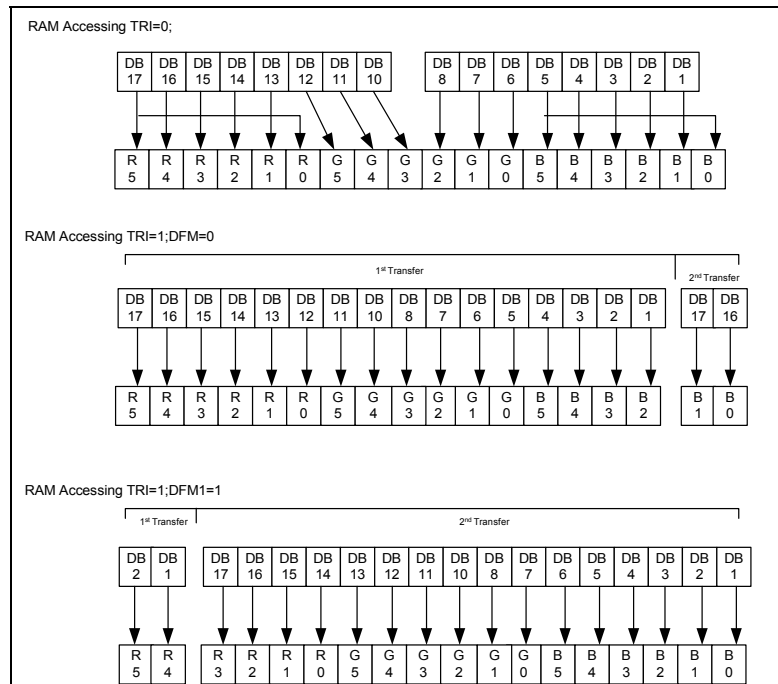


Figure 7-4

7.1.3. 80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 7-5** and **Figure 7-6**, respectively.

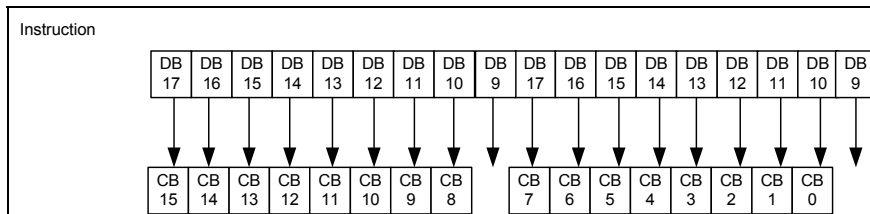


Figure 7-5

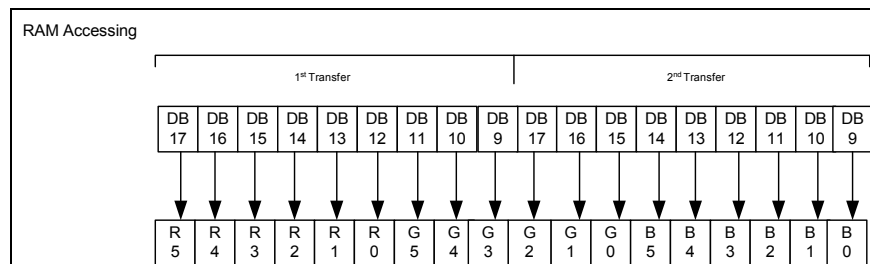


Figure 7-6

7.1.4. 80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 7-7** and **Figure 7-8**, respectively.

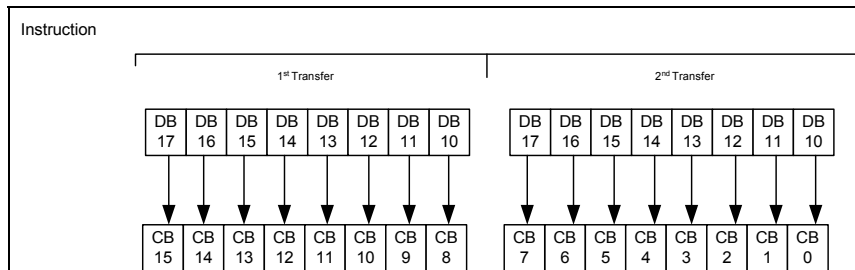


Figure 7-7

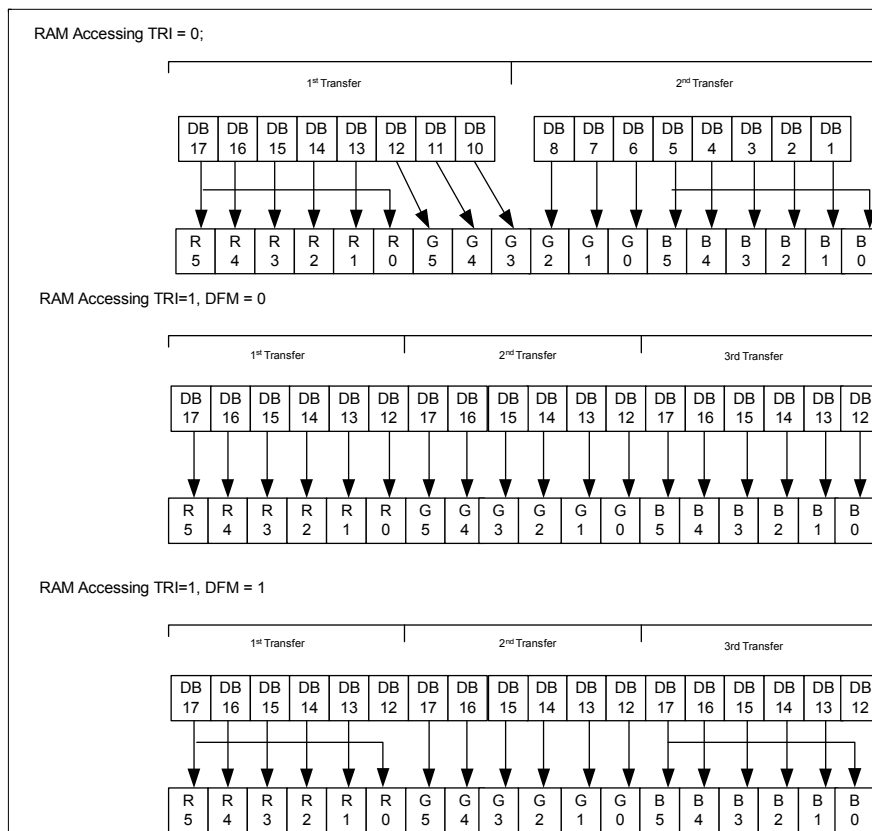


Figure 7-8

7.1.5. Serial Peripheral interface (SPI)

The system interface of OTM3225C also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and OTM3225C. IM0/ID pin served as the ID pin. **Figure 7-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVCC or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 7-10** and **Figure 7-11**, respectively.

When read operation is desired In SPI mode, valid data are read out as the OTM3225C reads out the 6th byte data from the internal GRAM. The RAM data transfer in SPI mode, in SPI mode with status read are illustrated in **Figure 7-12**, , respectively.

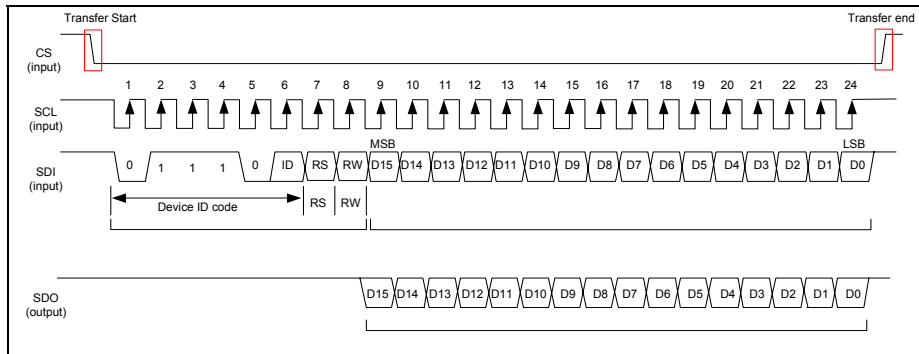


Figure 7-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

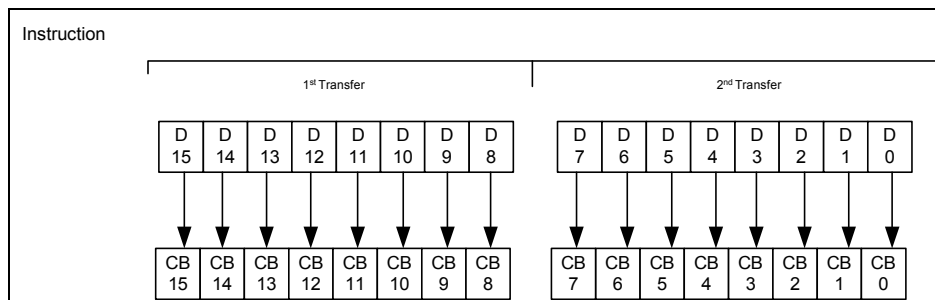


Figure 7-10

7.2. VSYNC Interface

The OTM3225C also supports VSYNC interface for moving picture display, which is the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface can display a moving picture without tremendous modification.

DM1-0 = "10" and RM = "0" can initialize VSYNC interface. In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. In VSYNC interface mode, the graphic data are stored in GRAM to minimize the data transfer to overwrite on the moving picture GRAM area. **Figure 7-13** illustrates moving picture data transfer through VSYNC interface.

In VSYNC mode, Internal operation is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. Therefore the frame rate is determined by the frequency of VSYNC. OTM3225C can access the internal RAM in high speed with less power consumption in VSYNC interface mode while using high-speed write mode

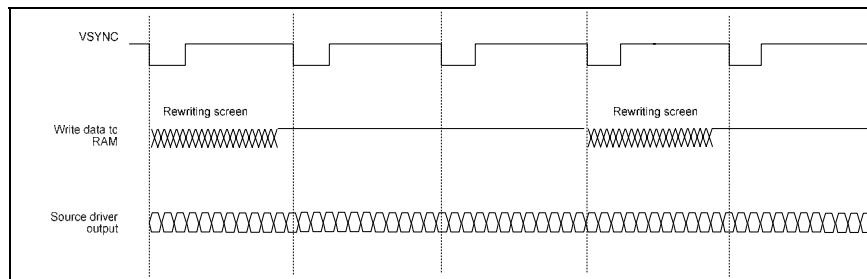


Figure 7-13

In VSYNC interface mode, the formula for Internal clock frequency and frame rate is shown below:

$$\text{Input clock frequency} = \text{FrameRate} \times (\text{DisplayLines}) + \text{FrontPorch} + \text{BackPorch} \times 16 \times \text{variance}$$

Due to the possible cause of variances while set the internal clock frequency; be sure to complete the display operation in one VSYNC cycle.

7.3. External Display Interface

OTM3225C also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 7-3** summarized the corresponding types of RGB interface with RIM1-0 setting.

Table 7-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	8-bit RGB interface	DB17-10

RGB interface can access OTM3225C by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. **Figure 7-14** illustrates the general timing for RGB interface. There are some constrain while using RGB interface. The following summarized the conditions

- Partial display/ scroll function / interlace and graphics operation function are not available for RGB interface
- In RGB interface VSYNC, HSYNC, and DOTCLK signals must be input through a display operation period.
- The setting of the NO1-0 bits, STD1-0 bits and EQ1-0 bits are based on DOTCLK in RGB interface mode. In 6-bit RGB interface mode, it takes 3 DOTCLK inputs to transfer one pixel. Be aware data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode is necessary. Set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB17-0) to input 3x clock to complete data transfer in units of pixels.
- In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
- In RGB interface mode, a GRAM address (DB17-0) is set in the address counter every frame on the falling edge of VSYNC.

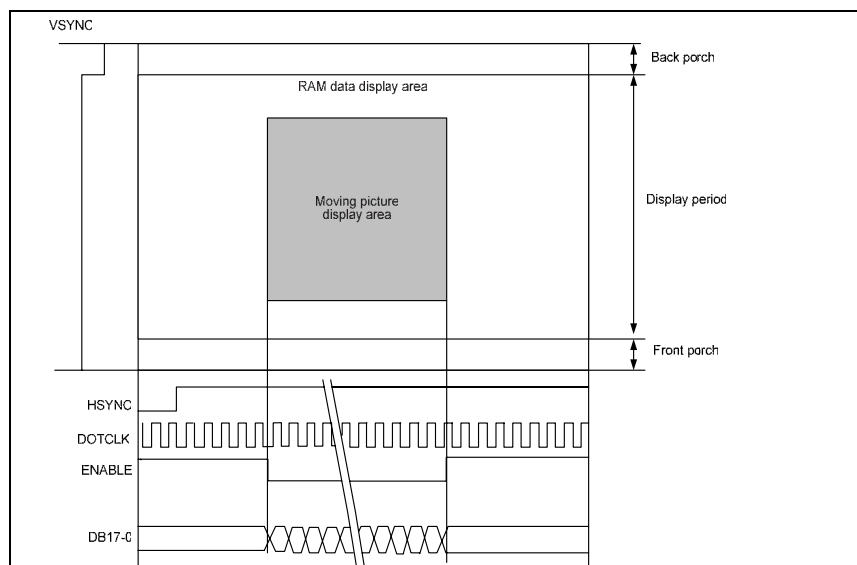


Figure 7-14

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 7-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 7-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

OTM3225C can support 18-bit, 16-bit, 8-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interface are shown in **Figure 7-15** and **Figure 7-16** respectively.

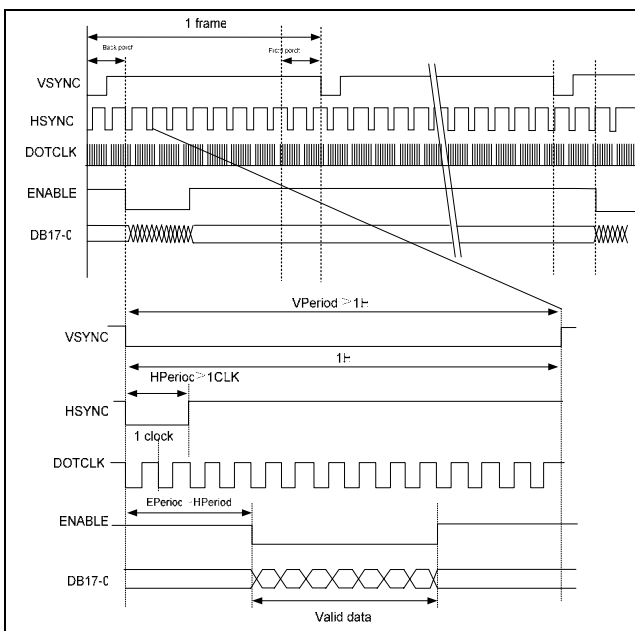


Figure 7-15

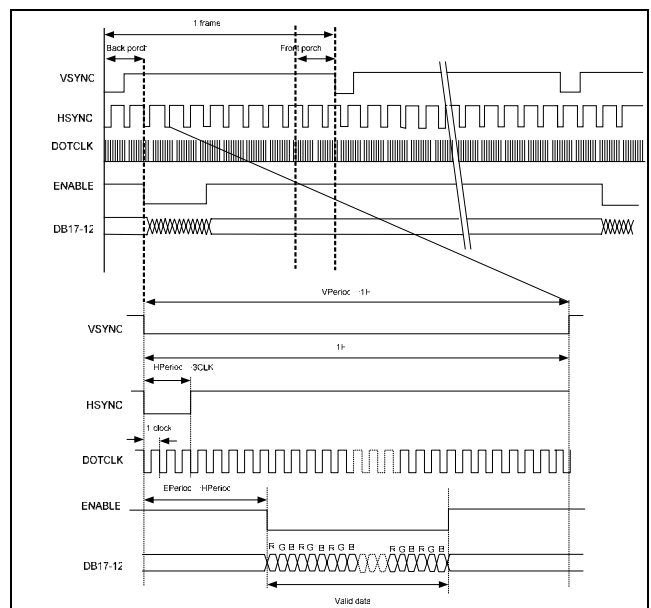


Figure 7-16

The RGB interface also has the window address function to transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting $RM = 0$ while in RGB interface mode can make GRAM access through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by $RM = 1$ setting.

Figure 7-17 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

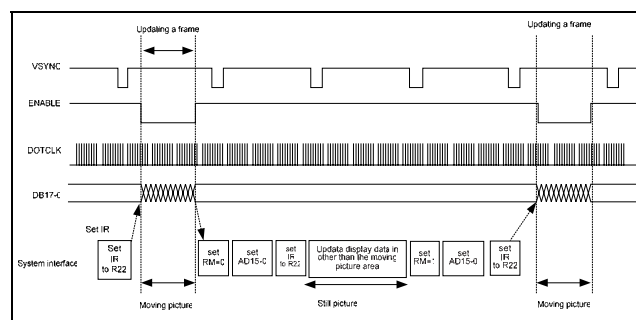


Figure 7-17

7.3.1. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 7-18** and **Figure 7-19**, respectively.

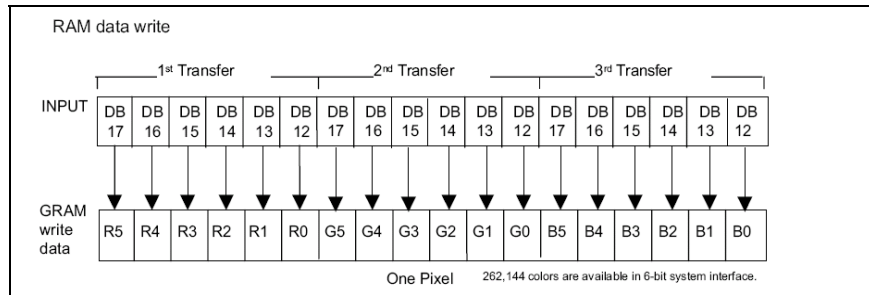


Figure 7-18

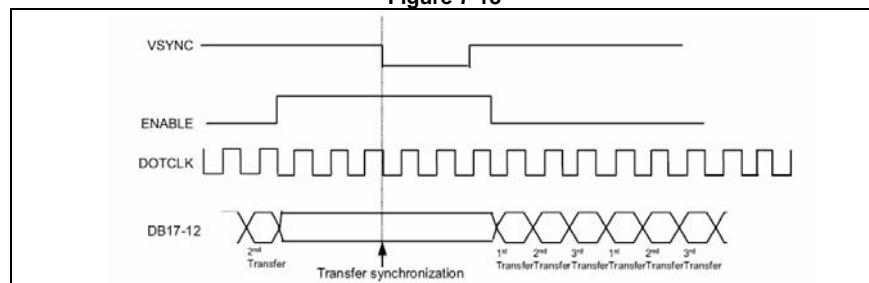


Figure 7-19

7.3.2. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 7-20**.

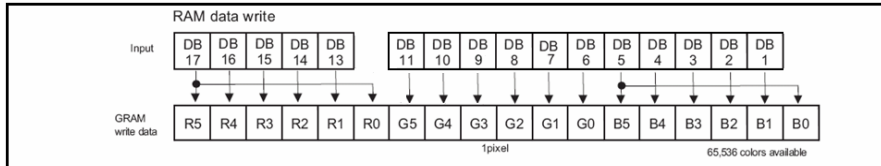


Figure 7-20

7.3.3. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 7-21**.

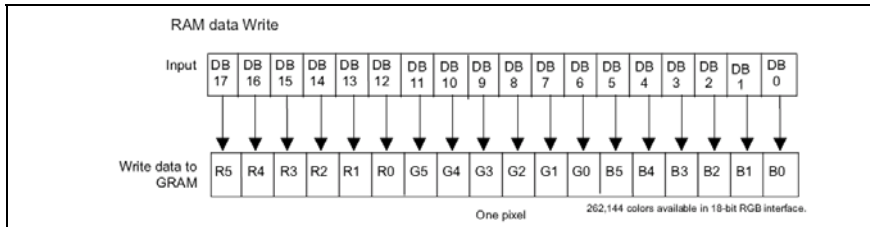
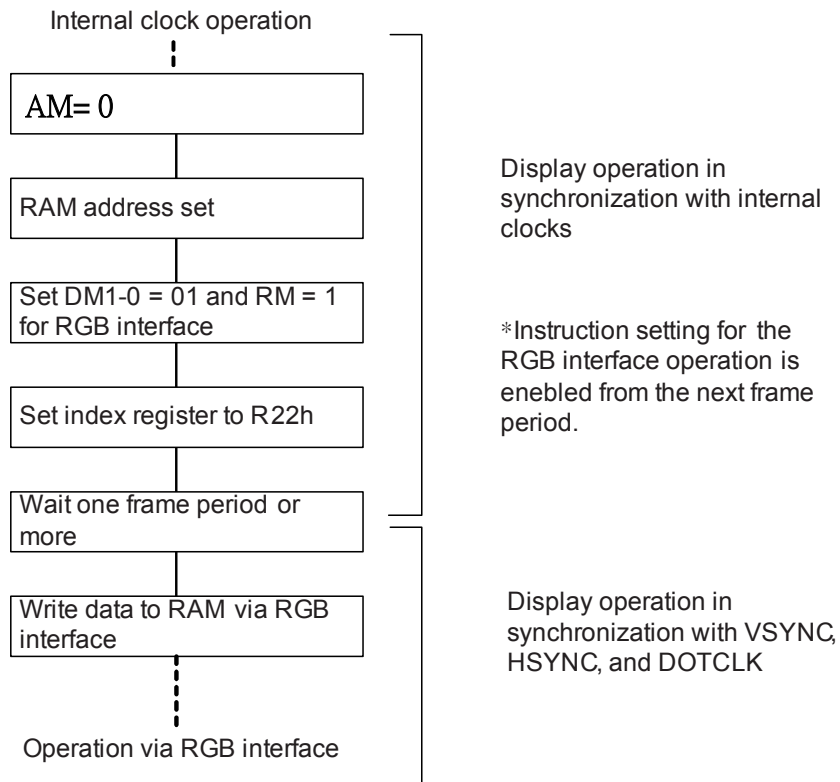


Figure 7-21

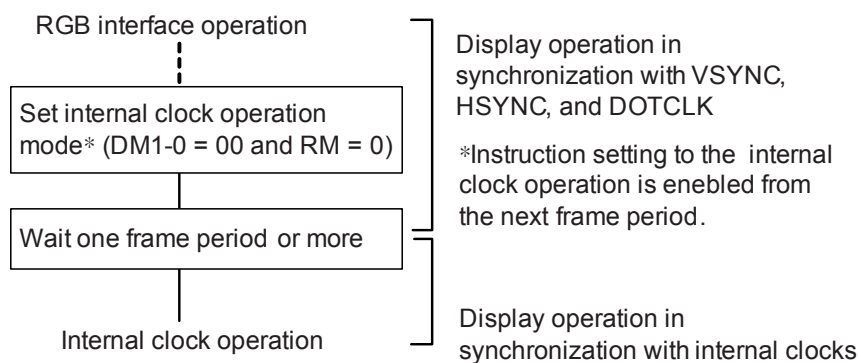
7.4. Sequence to set between system interface and RGB interface:

Internal Clock Operation to RGB Interface (1)



Note: Input the RGB interface signals before setting the DM 1-0 and RM bits to the RGB interface operation .

RGB Interface (1) to Internal Clock Operation



Note: Continue RGB interface signals at least for one frame period after setting DM1-0, RM bits to internal clock operation.

8. Display Feature Function:

8.1. FMARK function:

OTM3225C provided FMARK function which output signal to alert host MCU via FMARK I/O pad so that LCD display can avoid tearing effect. FMARK output position and interval can be set by FMP[8:0] and FMI[2:0], respectively.

Figure 8-1 illustrated the FMARK output position when FMP[8:0]=9'h008.

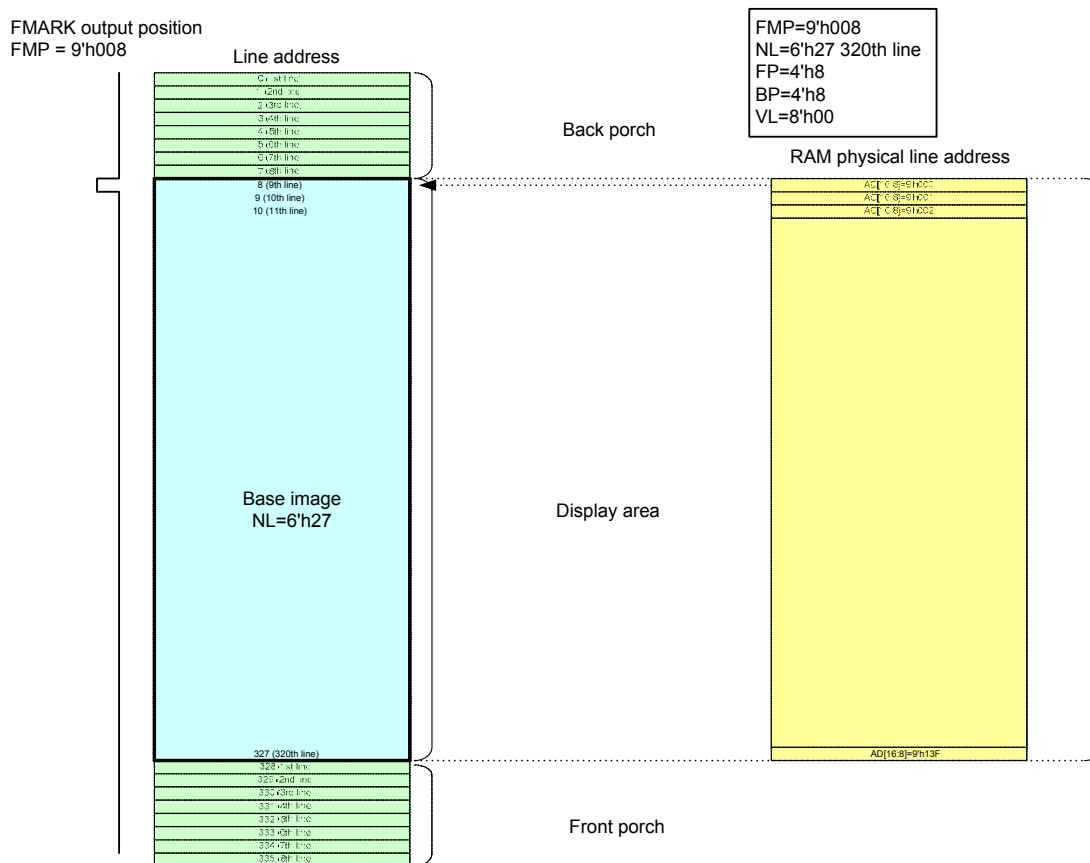
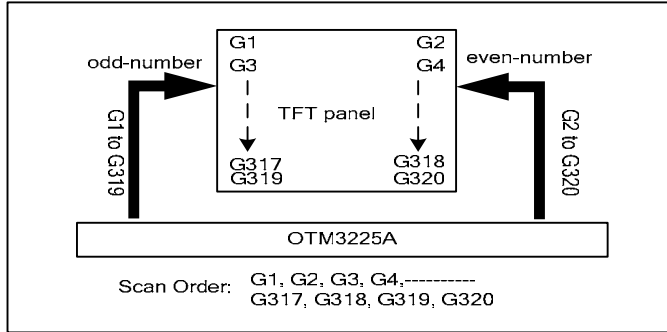
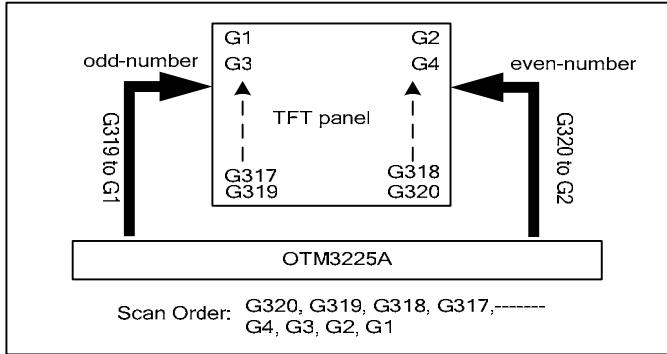
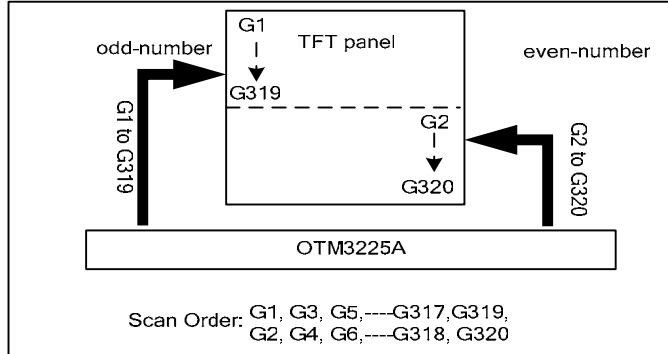
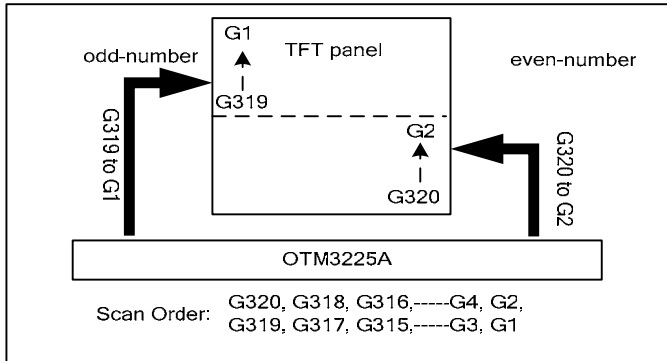


Figure 8-1 Example of FMARK signal.

8.2. Scan Mode function:

SM	GS	Scan Direction
0	0	 <p>Scan Order: G1, G2, G3, G4,----- G317, G318, G319, G320</p>
0	1	 <p>Scan Order: G320, G319, G318, G317,----- G4, G3, G2, G1</p>
1	0	 <p>Scan Order: G1, G3, G5,-----G317, G319, G2, G4, G6,-----G318, G320</p>
1	1	 <p>Scan Order: G320, G318, G316,-----G4, G2, G319, G317, G315,-----G3, G1</p>

