DATA SHEET

旭曜科技 ORISE TECH

OTM2201A

528-channel True 6-bit Source Driver with System-on-chip for Color Amorphous TFT-LCDs

Preliminary

MAY. 05, 2009

Version 0.2

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528-CHANNEL DRIVER WITH SYSTEM-ON-CHIP (SOC) FOR COLOR AMORPHOUS TFT LCD

1. GENERAL DESCRIPTION

The OTM2201A, a 262144-color System-on-Chip (SoC) driver LSI designed for small and medium sizes of TFT LCD display, is capable of supporting up to 176xRGBx220 in resolution which can be achieved by the designated RAM for graphic data. The 528-channel source driver has true 6-bit resolution, which generates 64 Gamma-corrected values by an internal D/A converter.

The OTM2201A is able to operate with low IO interface power supply up to 1.65V and incorporate with several charge pumps to generate various voltage levels that form an on-chip power management system for gate driver and source driver.

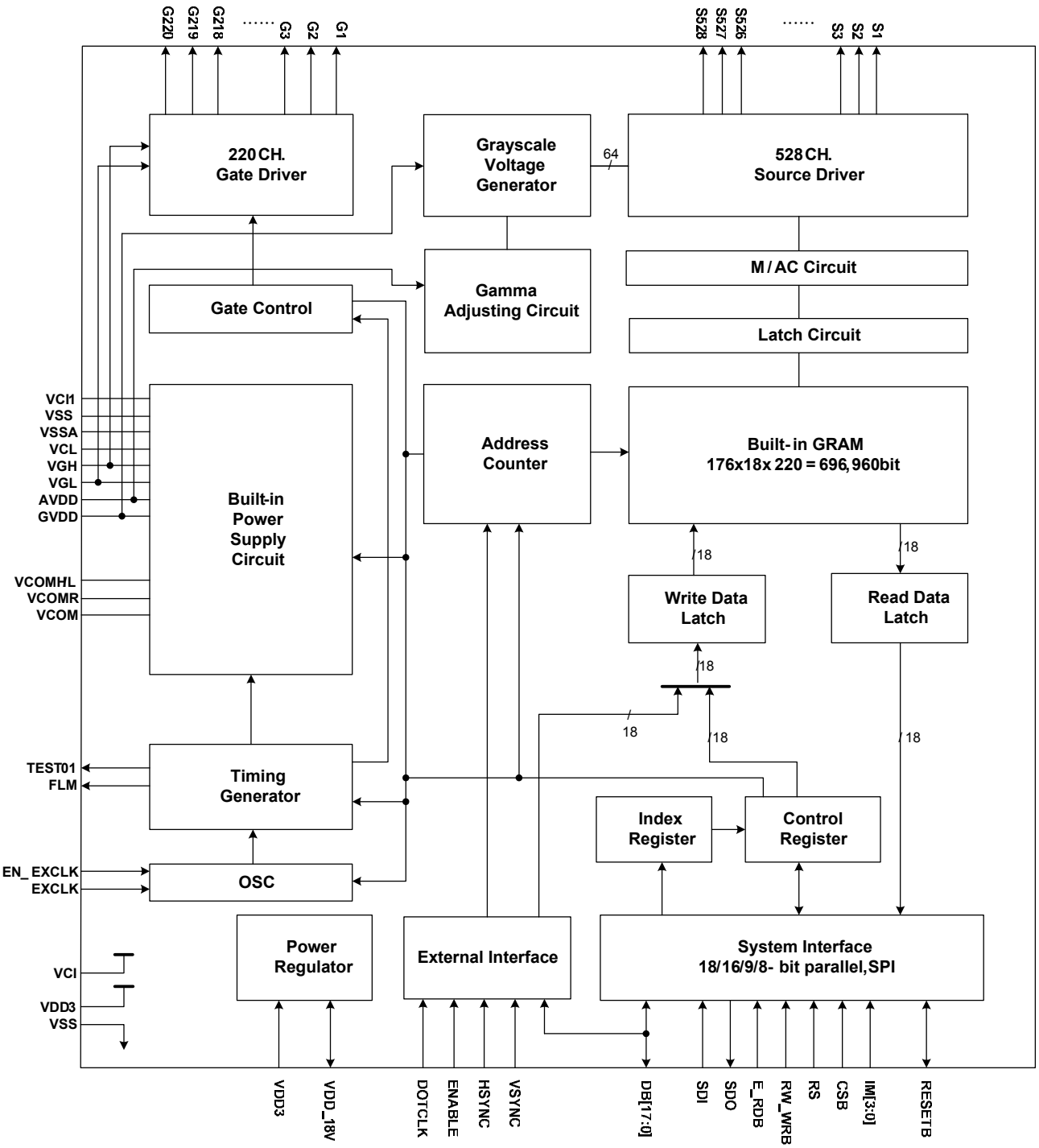
The built-in timing controller in OTM2201A can support several interfaces for the diverse request of medium or small size portable display. OTM2201A provides system interfaces, which include 8-/9-/16-/18-bit parallel interfaces and serial interface (SPI), to configure system. Not only can the system interfaces be used to configure system, they can also access RAM at high speed for still picture display. In addition, the OTM2201A incorporates 6, 16, and 18-bit RGB interfaces for picture movement display. The OTM2201A also supports a function to display eight colors and a standby mode for power control consideration.

2. FEATURES

- One-chip solution for amorphous TFT-LCD.
- Supports resolution up to 176xRGBx220, incorporating a 528-channel source driver and a 220-channel gate driver
- Outputs 64 γ -corrected values using an internal true 6-bit resolution D/A converter to achieve 262K colors
- Built-in 87120 bytes internal RAM
- Line Inversion AC drive / frame inversion AC drive
- System interfaces
  - 80-series high-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - 68-series high-speed interfaces to 8-, 9-, 16-, and 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, and 18-bit RGB interfaces
- Diverse RAM accessing for functional display
  - Window address function to display at any area on the screen via a moving picture display interface
  - Window address function to limit the data rewriting area and reduce data transfer
  - Moving and still picture can display at the same time
  - Vertical scrolling function
  - Partial screen display
- Power supply
  - I/O interface supply voltage (VDD3): 1.65 ~ 3.6 V
  - Analog power supply voltage (VCI): 2.5 ~ 3.6 V
- On-chip power management system
  - Power saving mode (standby / 8-color mode, etc)
  - Low power consumption structure for source driver.
- Built-in Charge Pump circuits
  - Source driver voltage level: AVDD-GND=4.5V ~ 6V.
  - Gate driver voltage level (VGH, VGL)
    VGH = 6.75V ~21.00V
    VGL = -4.05V ~ -15.00V
    VGH – VGL <=36.0V
  - Built-in internal oscillator and hardware reset
- External Component
  - 10 Capacitors for Power and Charge Pump circuits.

3. BLOCK DIAGRAM

3.1. Block Function



3.1.1. System Interface

The OTM2201A supports 2 system high-speed interfaces:

1. 80-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
2. 68-system high-speed interfaces with 8-, 9-, 16-, 18-bit parallel ports.
3. Serial Peripheral Interface (SPI).

The interface mode is selected by setting the pins, RW_WRB, E_RDB & RS. **Table 3-1** and **Table 3-2** indicated register selection function for 68-/80-system interface and SPI, respectively.

The OTM2201A has three 18-bit data registers, index register (IR) data registers, write-data register (WDR) and read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal GRAM. The RDR register is used to temporarily store data read from the GRAM. When graphic data is written to the internal GRAM from MCU/graphic engine, the data is first written to the WDR and then automatically written to the internal GRAM in internal operation. When graphic data read operation is executed, graphic data is read via the RDR from the internal GRAM. Therefore, invalid data is first read out to the data bus when the OTM2201A executes the 1st read operation. Thus, valid data can be read out after the OTM2201A executes the 2nd read operation.

Table 3-1 Register Selection (68-/80-system 8/9/16/18-bit Parallel Interface)

80-system I/F			Function
RW_WRB	E_RDB	RS	
0	1	0	Write an index to IR of 68-system
1	1	0	Read an internal status of 68-system
0	1	1	Write to control registers or the internal GRAM via WDR of 68-system
1	1	1	Read from the internal GRAM via RDR of 68-system
0	1	0	Write an index to IR of 80-system
1	0	0	Read an internal status of 80-system
0	1	1	Write to control registers or the internal GRAM via WDR of 80-system
1	0	1	Read from the internal GRAM via RDR of 80-system

Table 3-2 Register Selection (Serial Peripheral Interface)

Start byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

3.1.2. External Display Interface

The OTM2201A supports RGB interface as external interfaces for displaying moving picture.

The OTM2201A supports external RGB interface for picture movement display.

The OTM2201A allows switching between one of the external display interfaces and the system interface via pin configuration so that the optimum interface is selected for still / moving picture displayed on the screen.

When the RGB interface is chosen, display operations are synchronized with external supplied signals, VSYNC, HSYNC, and DOTCLK. Moreover, valid display data (DB17-0) is written to GRAM, which synchronized with signal (DE) enabling.

3.1.3. Address Counter (AC)

OTM2201A includes an address counter (AC) gives an address to the internal GRAM. The address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

3.1.4. Graphics RAM (GRAM)

OTM2201A includes a Graphic RAM (GRAM) which has the capacity of 87,120 (176 x 220x 18/8) bytes.

3.1.5. Grayscale Voltage Generating Circuit

OTM2201A has true 6-bit resolution D/A converter, which can output 64 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register. For details, see the "γ-Correction Function" section.

3.1.6. Timing Controller

OTM2201A has a timing controller which can generates a timing signal for internal circuits operation such as gate output timing, RAM accessing timing, etc.

3.1.7. Oscillator (OSC)

The OTM2201A include an internal oscillator, which generates RC oscillation without an external resistor. The frequency can be adjusted through the register setting, R0Fh. An operating clock can be input externally. Operating voltage and the frame frequency are related to the oscillation frequency. In standby mode, RC oscillation is halted to reduce power consumption. For details, see "Oscillator".

3.1.8. Source Driver Circuit

OTM2201A consists of a 528-output source driver circuit (S1 ~ S528). Data in the GRAM are latched when the 528th bit data are input. The shift direction of 528-bit source outputs from the source driver is set by register, SS bit. The latched data control the source driver and generate a drive waveform.

3.1.9. Gate Driver Circuit

OTM2201A consists of a 220-output gate driver circuit (G1~G220). The gate driver circuit outputs gate driver signals at either VGH or VGL level. The shift direction of gate outputs from the gate driver is set by register, GS bit. The scan mode by the gate driver is set by register, SM bit.

3.1.10. LCD Driving Power Supply Circuit

The LCD driving power supply circuit generates the voltage levels GVDD, VGH, VGL and Vcom for driving an LCD. All this voltages can be adjusted by register setting.

4. SIGNAL DESCRIPTIONS

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td colspan="4">System Configuration Input Signal</td></tr>
<tr><td>IM3~0 /ID</td><td>I</td><td>GND/ VDD3</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ I D</th><th>Interface Mode</th><th>DB Pin</th><th>Colors</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>68-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>68-system 8-bit interface</td><td>DB17-10</td><td>262,144</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td><td>262,144 see Note 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td><td>262,144 see Note 2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>*(ID)</td><td>Clock synchronous serial interface</td><td>-</td><td>65,536</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>68-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>68-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td><td>262,144</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td><td>262,144</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td><td>-</td></tr>
</table>
Notes: 1. 65,536 colors in one transfer mode
2. 65,536 colors in two transfers mode</td></tr>
<tr><td>RESETB</td><td>I</td><td>MPU or external RC circuit</td><td>RESET pin. This is an active low signal.</td></tr>
<tr><td colspan="4">Interface input Signals</td></tr>
<tr><td>CSB</td><td>I</td><td>MPU</td><td>Chip select signal.
Low: the OTM2201A is accessible
High: the OTM2201A is not accessible
Must connect to VDD3 level when not used.</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal.
Low: Index register or internal status is selected.
High: Control register is selected.
Must connect to the GND or VDD3 level when not used.</td></tr>
<tr><td>RW_WRB/SCL</td><td>I</td><td>MPU</td><td>(A) In 68-system interface mode, it is used to determine read or write operation. (RW)
(B) In 80-system interface mode, a write strobe signal can be input via this pin and initializes a write operation when the signal is low. (WRB)
(C) In SPI mode, served as a synchronizing clock signal. (SCL)</td></tr>
<tr><td>E_RDB</td><td>I</td><td>MPU</td><td>In 68-system interface mode, read or write operation is selected through this pin.(E)
In 80-system interface mode, a read strobe signal can be input via this pin and initializes a read operation when the signal is low. (RDB)</td></tr>
</table>

<table>
<tr><th>Signal</th><th>I/O</th><th>Connected with</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td>Must connect to the GND or VDD3 level when not in use.</td></tr>
<tr><td>SDI</td><td>I</td><td>MPU</td><td>Series Data is the input on the rising edge of the SCL signal in SPI mode.
Must connect to the GND or VDD3 level when not in use.</td></tr>
<tr><td>SDO</td><td>O</td><td>MPU</td><td>Series Data is the output on the rising edge of the SCL signal in SPI mode.</td></tr>
<tr><td>DB0-DB17</td><td>I/O</td><td>MPU</td><td>Served as an 18-bit parallel bi-directional data bus. Data bus pin assignment corresponding to different modes are summarized in the table:
<table>
<tr><th>Mode</th><th>Pin Assignment</th></tr>
<tr><td>8-bit system interface(i80 & M68)</td><td>DB17-DB10</td></tr>
<tr><td>9-bit system interface(i80 & M68)</td><td>DB17-DB9</td></tr>
<tr><td>16-bit system interface(i80 & M68)</td><td>DB17-DB10, DB8-DB1</td></tr>
<tr><td>18-bit system interface(i80 & M68)</td><td>DB17-DB0</td></tr>
<tr><td>6-bit External (RGB) interface</td><td>DB17-DB12</td></tr>
<tr><td>16-bit External (RGB) interface</td><td>DB17-13, DB11-DB1</td></tr>
<tr><td>18-bit External (RGB) interface</td><td>DB17-DB0</td></tr>
</table>
Must connect to the GND or VDD3 level when not in use.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>MPU</td><td>In external interface mode, served as a vertical synchronize signal input
Must connect to the VDD3 or GND level when not in use.</td></tr>
<tr><td>HSYNC</td><td>I</td><td>MPU</td><td>In external interface mode, served as a horizontal synchronized signal input
Must connect to the VDD3 or GND level when not used.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>MPU</td><td>In external interface mode, polarity of ENABLE signal is synchronized with valid graphic data input.
Low: Valid data on DB17-DB0
High: Invalid data on DB17-DB0
Moreover, setting EPL bit can change the polarity of the ENABLE signal.
Must connect to the GND or VDD3 level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>I</td><td>MPU</td><td>In external interface mode, served as a dot clock signal. It is fixed to the VDD3 or GND level when not in use.</td></tr>
<tr><td>FLM</td><td>O</td><td>MPU</td><td>FLM head pulse signal, which is used when writing data to the internal RAM. Keep this pin open when not used.</td></tr>
<tr><td colspan="4">Charge Pump and Power Supply Signal</td></tr>
<tr><td>C11P, C11N</td><td>-</td><td>Step-up capacitor</td><td>Connect boost capacitors for the internal DC/DC converter circuit to these pins.</td></tr>
<tr><td>C12P, C12N</td><td>-</td><td>Step-up capacitor</td><td>Connect boost capacitors for the internal DC/DC converter circuit to these pins.</td></tr>
<tr><td>C13P, C13N</td><td>-</td><td>Step-up capacitor</td><td>Connect boost capacitors for the internal DC/DC converter circuit to these pins.</td></tr>
<tr><td>C21P, C21N</td><td>-</td><td>Step-up capacitor</td><td>Connect boost capacitors for the internal DC/DC converter circuit to these pins.</td></tr>
<tr><td>C22P, C22N</td><td>-</td><td>Step-up capacitor</td><td>Connect boost capacitors for the internal DC/DC converter circuit to these pins.</td></tr>
<tr><td>VCI1</td><td>I/O</td><td>MPU</td><td>Reference voltage of step-up circuit. It does not need capacitor.</td></tr>
<tr><td>AVDD</td><td>I</td><td>Stabilizing capacitor</td><td>Internally generated voltage output pad for source driver block.</td></tr>
<tr><td>VGH</td><td>I</td><td>Stabilizing capacitor</td><td>Liquid crystal drive power supply.</td></tr>
<tr><td>VGL</td><td>I</td><td>Stabilizing capacitor</td><td>Liquid crystal drive power supply.</td></tr>
<tr><td>VCL</td><td>O</td><td>Stabilizing capacitor</td><td>VCOML drive power supply.</td></tr>
<tr><td colspan="4">Source/Gate Driver</td></tr>
<tr><td>G1~G119
G2~G220</td><td>O</td><td>LCD</td><td>Output gate driver signals, which has the swing from VGH to VGL</td></tr>
</table>

Signal	I/O	Connected with	Function
S1~S528	O	LCD	Output source driver signals. The D/A converted 64-gray-scale analog voltage is output.
Pads for power supplies			
GVDD	O	MPU	Reference voltage ofr grayschale voltage generator.
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. *The alternating cycle is set by the pin TEST01.*
VCOMH	O	MPU	The High level of VCOM amplitude. The output level can be adjusted by register setting (VCM bits).
VCOML	O	MPU	The Low level of VCOM amplitude. The output level can be adjusted by instruction (VML bits).
VCOMR	I	Variable resistor or open	Reference voltage for VCOMH. VCOMH voltage can be adjusted externally by inserting a variable resistor between GVDD and VSS. Leave this pin open when not in use.
VGS	-	GND	Reference level for the grayscale voltage generating circuit.
VDD_18V	I/O	Stabilizing capacitor	Power for internal logic circuit from internal Voltage regulator.
VSS	-	GND	Internal logic GND and Charge pump GND.
VDD3	-	Power supply	Power supply to the interface pins: RESET*, CS*, WR, RD*, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE. VDD3 = 1.65V ~ 3.6V. VDD_18V ≥VDD3. In case of COG, connect to VCI on the FPC if VDD3=VDD, to prevent noise.
VSSA	-	GND	Analog GND (for logic regulator and liquid crystal power supply circuit): VSSA = 0V. In case of COG, connect to GND on the FPC to prevent noise.
VCI	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.6V.
VREF	I/O	Reference power supply	Reference voltage for grayscale voltage generator. Stabilizing capacitor may be need if VREF fluctuate.
Misc. Signal			
TEST01	O	Open	Test pin. Leave it open
FLM	O	-	MCU synchronization pin. Leave it open when not in use.
EN_EXCLK	I	-	Enable External Clock. Connect to VSS when not in use.
EXCLK	I	-	External clock input pin. Connect to VSS when not in use.
DUMMY1~2	-	Open	Dummy pins. Leave them open.
DUMMY3~9	-	Open	Dummy pins. Leave them open.
DUMMY10		Open	Dummy pins. Leave them open.
DUMMY11~16		Open	Dummy pins. Leave them open.
DUMMY17~25	-	Open	Dummy pins. Leave them open.
DUMMY26~33		Open	Dummy pins. Leave them open.
DUMMY34~37		Open	Dummy pins. Leave them open.
TEST0~TEST1	I	VSS	Test pins. Connect to VSS.
TEST2~TEST7	I	Open	Test pins. Leave it open.

5. INSTRUCTIONS

5.1. Outline

The OTM2201A supports 18-bit data bus interface to access command register to configure system. When the command register accessing is desired, sending the command information to specify which index register would be accessed and following the data to that control register. Moreover, register accessing operation should cooperate with RS, /WR, /RD signal for OTM2201A to recognize the control instruction. And command instruction can be accomplished by using all system interfaces (18-bit, 16-bit, 9-bit, 8-bit 68-/80- system and SPI). The corresponding pin assignment of different system interface are shown in **Figure 5-1** to **Figure 5-6**

The instruction can be categorized into 8 groups. And the 8 groups are:

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-correction

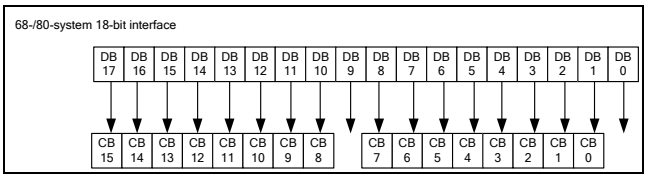


Figure 5-1

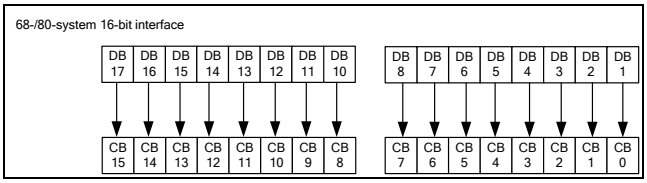


Figure 5-2

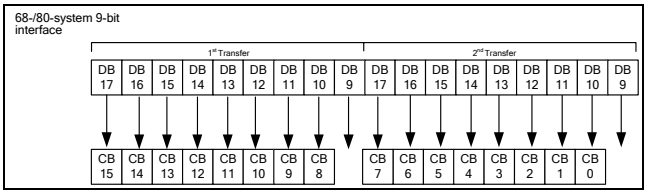


Figure 5-3

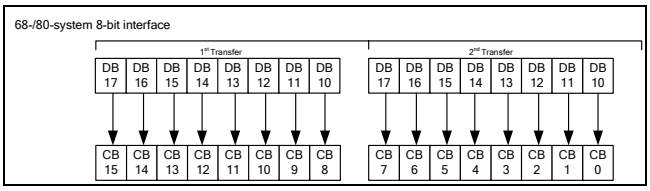


Figure 5-4

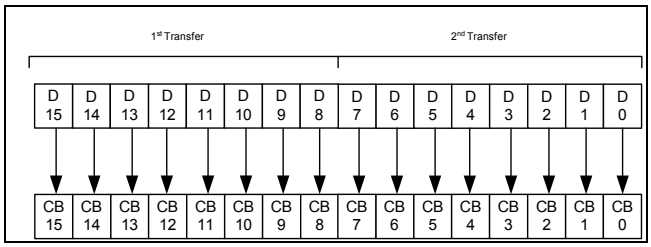


Figure 5-5

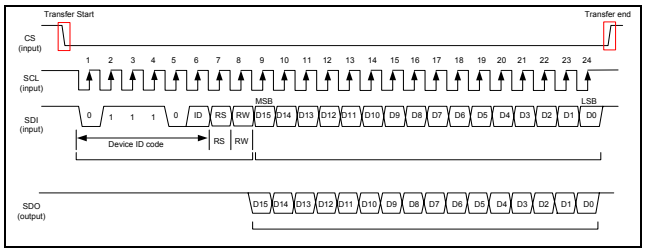


Figure 5-6

5.2. Instruction

Table 5-1 Instruction List Table

R/W	RS	Register No	Register	Upper 8-bit								Lower 8-bit							
				CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	-	Index	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	0	-	Status Read	-	-	-	-	-	-	-	L8	L7	L6	L5	L4	L3	L2	L1	L0
R	1	00h	Device Code Read	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1
W	1	01h	Driver Output Control	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	0	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (0)	NL0 (0)
W	1	02h	LCD AC Drive Control	0	0	0	0	0	0	INV1 (0)	INV0 (1)	0	0	0	0	0	0	0	FLD (0)
W	1	03h	Entry Mode	0	0	0	BGR (0)	0	0	MDT1 (0)	MDT0 (0)	0	0	ID1 (1)	ID0 (1)	AM (0)	0	0	0
W	1	04h-05h	Setting Disabled	-															
W	1	07h	Display control	0	0	0	FLM_MON (0)	0	0	0	0	0	0	0	GON (0)	CL (0)	REV (0)	D1 (0)	D0 (0)
W	1	08h	Blanking Control	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
W	1	09h-0Ah	Setting Disabled	-															
W	1	0Bh	Frame cycle control	NO3 (0)	NO2 (0)	NO1 (0)	NO0 (1)	SDT3 (0)	SDT2 (0)	SDT1 (0)	SDT0 (1)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)
W	1	0Ch	External interface control	0	0	0	0	0	0	0	RM (0)	0	0	0	DM (0)	0	0	RIM1 (0)	RIM0 (0)
W	1	0Dh-0Eh	Setting Disabled																
W	1	0Fh	Oscillator Control	0	0	0	FOSC4 (0)	FOSC3 (0)	FOSC2 (1)	FOSC1 (0)	FOSC0 (1)	0	0	0	0	0	0	0	OSCON (1)
W	1	10h	Power Control (1)	0	0	0	0	SAP (0)	SAP2 (0)	SAP1 (1)	SAP0 (0)	0	0	0	0	0	0	DSTB (0)	STB (0)
W	1	11h	Power Control (2)	0	0	0	APON (0)	PON3 (0)	PON2 (0)	PON1 (0)	PON (0)	0	AB_VCI1 (0)	AON (0)	VCI1_EN (0)	VC3 (0)	VC2 (0)	VC1 (0)	VC0 (0)
W	1	12h	Power Control (3)	0	BT2 (0)	BT1 (0)	BT0 (0)	0	0	DCI1 (0)	DCI0 (0)	0	0	DC21 (0)	DC20 (0)	0	0	DC31 (0)	DC30 (0)
W	1	13h	Power Control (4)	0	0	0	DCR_EX (0)	0	DCR2 (0)	DCR1 (0)	DCR0 (0)	0	GVD6 (0)	GVD5 (0)	GVD4 (0)	GVD3 (0)	GVD2 (0)	GVD1 (0)	GVD0 (0)
W	1	14h	Power Control (5)	VCOMG (1)	VCM6 (0)	VCM5 (0)	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	VCMR (0)	VML6 (0)	VML5 (0)	VML4 (0)	VML3 (0)	VML2 (0)	VML1 (0)	VML0 (0)
W	1	15h	VCI Period Setting	0	0	0	0	0	0	0	0	0	VCIR2 (0)	VCIR1 (0)	VCIR0 (0)	0	0	0	0
-	-	16h-19h	Setting Disabled	-															
W	1	20h	RAM Address	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
W	1	21h	RAM address	0	0	0	0	0	0	0	0	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
W	1	22h	GRAM data	Data format is interface dependent.															
-	-	23h-27h	Setting Disabled	-															
W	1	28h	Software Reset	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0
-	-	29h-2Fh	Setting Disabled	-															
W	1	30h	Gate Scan Start Position	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
W	1	31h	Vertical Scrolling Control 1	0	0	0	0	0	0	0	0	SEA7 (1)	SEA6 (1)	SEA5 (0)	SEA4 (1)	SEA3 (1)	SEA2 (0)	SEA1 (1)	SEA0 (1)
W	1	32h	Vertical Scrolling Control 2	0	0	0	0	0	0	0	0	SSA7 (0)	SSA6 (0)	SSA5 (0)	SSA4 (0)	SSA3 (0)	SSA2 (0)	SSA1 (0)	SSA0 (0)
W	1	33h	Vertical Scrolling Control 3	0	0	0	0	0	0	0	0	SST7 (0)	SST6 (0)	SST5 (0)	SST4 (0)	SST3 (0)	SST2 (0)	SST1 (0)	SST0 (0)
W	1	34h	Partial Screen Area 1	0	0	0	0	0	0	0	0	SE17 (1)	SE16 (1)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (0)	SE11 (1)	SE10 (1)
W	1	35h	Partial Screen Area 2	0	0	0	0	0	0	0	0	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
W	1	36h	Horizontal Window Address 1	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (0)

W	1	37h	Horizontal Window Address 2	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
W	1	38h	Vertical Window Address 1	0	0	0	0	0	0	0	0	VEA7 (1)	VEA6 (1)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (0)	VEA1 (1)	VEA0 (1)
W	1	39h	Vertical Window Address 2	0	0	0	0	0	0	0	0	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
-	-	3Ah-49h	Setting Disabled	-															
W	1	50h	Gamma Control 1	0	0	0	0	PVR3V83	PVR3V82	PVR3V81	PVR3V80	0	0	0	0	PVR3V13	PVR3V12	PVR3V11	PVR3V10
W	1	51h	Gamma Control 2	0	0	0	0	PVR3V433	PVR3V432	PVR3V431	PVR3V430	0	0	0	0	PVR3V203	PVR3V202	PVR3V201	PVR3V200
W	1	52h	Gamma Control 3	0	0	0	0	PVR3V623	PVR3V622	PVR3V621	PVR3V620	0	0	0	0	PVR3V553	PVR3V552	PVR3V551	PVR3V550
W	1	53h	Gamma Control 4	0	0	0	0	PRP13	PRP12	PRP11	PRP10	0	0	0	0	PRP03	PRP02	PRP01	PRP00
W	1	54h	Gamma Control 5	0	0	0	0	NVR3V83	NVR3V82	NVR3V81	NVR3V80	0	0	0	0	NVR3V13	NVR3V12	NVR3V11	NVR3V10
W	1	55h	Gamma Control 6	0	0	0	0	NVR3V433	NVR3V432	NVR3V431	NVR3V430	0	0	0	0	NVR3V203	NVR3V202	NVR3V201	NVR3V200
W	1	56h	Gamma Control 7	0	0	0	0	NVR3V623	NVR3V622	NVR3V621	NVR3V620	0	0	0	0	NVR3V553	NVR3V552	NVR3V551	NVR3V550
W	1	57h	Gamma Control 8	0	0	0	0	PRN13	PRN12	PRN11	PRN10	0	0	0	0	PRN03	PRN02	PRN01	PRN00
W	1	58h	Gamma Control 9	0	0	0	PVR1V634	PVR1V633	PVR1V632	PVR1V631	PVR1V630	0	0	0	PVR1V04	PVR1V03	PVR1V02	PVR1V01	PVR1V00
W	1	59h	Gamma Control 10	0	0	0	NVR1V634	NVR1V633	NVR1V632	NVR1V631	NVR1V630	0	0	0	NVR1V04	NVR1V03	NVR1V02	NVR1V01	NVR1V00
-	-	60h-7Fh	Setting Disabled	-															

The following are detailed explanations of instructions with illustrations of instruction bits (CB15-0) assigned to each interface.

5.2.1. Index Register (IR)

R/W	RS	CB15	CCB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h ~ R8Fh) of a control register. The index range is from “0000_0000” to “1111_1111” in binary format.

5.2.2. Status Register (SR)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0

An internal status of the OTM2201A can be accessed by status read register. L7-0: Indicate the current position of the line which liquid crystal is being driven.

5.2.3. Device code Read (R00h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1

The device code can be changed by modifing metal layer.

5.2.4. Driver Output Control Register (R01h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	VSPL	HSPL	DPL	EPL	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0
Default Value		0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

VSPL: Polarity of Vsync,
VSPL = 0: Vsync is active low.
VSPL = 1: Vsync is active high.

HSPL: Polarity of Hsync,
HSPL = 0: Hsync is active low.
VSPL = 1: Vsync is active high.

DPL: Polarity of DOTCLK,
DPL = 0: Data is fetched at rising edge.
DPL = 1: Data is fetched at falling edge.

EPL: Polarity of ENABLE in RGB interface,
EPL = 0: ENABLE = low; data write enabled.
ENABLE = high, data write disabled.
EPL = 1: ENABLE = high, data write enabled.
ENABLE = low, data write disabled.

Table 5-2

EPL	ENABLE	RAM Write	RAM Address
0	0	Valid	Updated
0	1	Invalid	Held
1	1	Valid	Updated
1	0	Invalid	Held

SM: Set the scan mode of the gate driver output. Moreover, SM can cooperate with GS for different LCD panel gate line layout. The combination of GS and SM bit are summarized at **Figure 5-3**

Note. When SM=1,NL setting is disable.

Table 5-3

SM	GS	Shift Direction (begin,…..,end)
0	0	G1, G2, G3, G4……G217, G218, G219, G220
0	1	G220, G219, G218, G217……G4, G3, G2, G1
1	0	G1, G3, G5, G217, G219, ……G2, G4, G218, G220
1	1	G220, G218, G216, G4, G2, ……G219, G217, G3, G1

GS: Shift direction of the gate driver output selection. When

GS = “0”, gate driver shift from G1 to G220.
GS = “1”, gate driver shift from G220 to G1.

SS: Shift direction of the source driver output selection.
When SS = “0”, source driver shift from S1 to S528. When SS = “1”, source driver shift from S528 to S1. Moreover, SS can cooperate with BGR for different color filter configuration of LCD panel. The combination of SS and BGR bit are summarized at **Table 5-4**.

Table 5-4

SS=0;BGR=0;	S1	S2	S3	⋯⋯▶	S526	S527	S528
SS=0;BGR=1;	S1	S2	S3	⋯⋯▶	S526	S527	S528
SS=1,BGR=0;	S1	S2	S3	◀⋯⋯	S526	S527	S528
SS=1,BGR=1;	S1	S2	S3	◀⋯⋯	S526	S527	S528

NL[4:0]: Set the number of line to be driven, **Table 5-5** shows the details.

Table 5-5

NL4	NL3	NL2	NL1	NL0	Display Size	Lines	Driven gate lines
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	528 x 8 dots	8	G1 ~ G8
0	0	0	1	0	528 x 16 dots	16	G1 ~ G16
0	0	0	1	1	528 x 24 dots	24	G1 ~ G24
0	0	1	0	0	528 x 32 dots	32	G1 ~ G32
0	0	1	0	1	528 x 40 dots	40	G1 ~ G40
0	0	1	1	0	528 x 48 dots	48	G1 ~ G48
0	0	1	1	1	528 x 56 dots	56	G1 ~ G56
0	1	0	0	0	528 x 64 dots	64	G1 ~ G64
0	1	0	0	1	528 x 72 dots	72	G1 ~ G72
0	1	0	1	0	528 x 80 dots	80	G1 ~ G80
0	1	0	1	1	528 x 88 dots	88	G1 ~ G88
0	1	1	0	0	528 x 96 dots	96	G1 ~ G96
0	1	1	0	1	528 x 104 dots	104	G1 ~ G104
0	1	1	1	0	528 x 112 dots	112	G1 ~ G112
0	1	1	1	1	528 x 120 dots	120	G1 ~ G120
1	0	0	0	0	528 x 128 dots	128	G1 ~ G128
1	0	0	0	1	528 x 136 dots	136	G1 ~ G136
1	0	0	1	0	528 x 144 dots	144	G1 ~ G144
1	0	0	1	1	528 x 152 dots	152	G1 ~ G152
1	0	1	0	0	528 x 160 dots	160	G1 ~ G160
1	0	1	0	1	528 x 168 dots	168	G1 ~ G168
1	0	1	1	0	528 x 176 dots	176	G1 ~ G176
1	0	1	1	1	528 x 184 dots	184	G1 ~ G184
1	1	0	0	0	528 x 192 dots	192	G1 ~ G192
1	1	0	0	1	528 x 200 dots	200	G1 ~ G200
1	1	0	1	0	528 x 208 dots	208	G1 ~ G208
1	1	0	1	1	528 x 216 dots	216	G1 ~ G216
1	1	1	0	0	528 x 220 dots	220	G1 ~ G220
1	1	1	0	1	Setting disabled	Setting disabled	Setting disabled
1	1	1	1	0	Setting disabled	Setting disabled	Setting disabled
1	1	1	1	1	Setting disabled	Setting disabled	Setting disabled

Note: Back porch and a front porch (set with BP/FP bits respectively) are inserted before/ after driving all gate lines,

5.2.5. LCD AC Drive Control (R02h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	INV1	INV0	0	0	0	0	0	0	0	FLD
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

INV[1:0]:

Set the interlaced scanning method.

FLD:

Set the inversion method.

Table 5-6

INV[1:0]	FLD	Description
00	0	Frame Inversion
	1	Setting Disable
01	0	Line Inversion
	1	Setting Disable
10	0	Setting Disable
	1	Setting Disable
11	0	No Inversion, active when VCOM is low
	1	No Inversion, active when VCOM is high

5.2.6. Entry Mode (R03h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	BGR	0	0	MDT1	MDT0	0	0	I/D1	I/D0	AM	0	0	0
Default Value		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

BGR: Set the RGB assignment order,
- BGR = 0;
{DB[17:12], DB[11:6], DB[5:0]} is assigned to {R, G, B}.

- BGR = 1;
{DB[17:12], DB[11:6], DB[5:0]} is assigned to {B, G, R}.

MDT1: When MDT1=1, the number of transfer of 1-pixel for 68-/80-system 8-bit mode and 68-/80-system 16-bit mode would be three times and two times respectively. Set MDT1=0 when other interface is in operation.

MDT0: When 8-/16-bit of 68-/80-system interfaces is under use and MDT1 = 1, MDT0 defines the color depth.

More detail see section 7.1.2 and 7.1.4

I/D1-0: To specify address counter increment /decrement automatically function while GRAM is accessing.

I/D1-0=11: increment automatically

I/D1-0=00: decrement automatically.

ID1-0 setting can cooperate with AM bit to set the data updating direction.

AM: To set the update direction when writing data to GRAM. If AM=1, data will write in vertical direction. If AM=0, data will write in horizontal direction. Moreover, if a fixed window GRAM accessing is desired, the writing direction can be set by ID1-0 and AM bits. **Figure 5-6** indicated the data updating direction.

5.2.7. Display Control (R07h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	FLM_MON	0	0	0	0	0	0	0	GON	CL	REV	D1	D0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FLM:

FLM_MON = 1, Enable FLM output.

FLM_MON = 0, Disable FLM output.

GON:

GON = 0, Disable gate output.

GON = 1, Enable gate output.

Table 5-7

GON	Gate Output
0	All gates output equal to VGL
1	Gate output enabled. (VGH/VGL)

CL: 8-color mode selection. When CL=1 OTM2201A enter to 8-color mode. When CL=0, OTM2201A is in normal operation mode.

REV: To set the grayscale corresponding to normally white or normally black LCD panel from same data input.

Table 5-8 summarized REV bit function.

Table 5-8

REV	GRAM data	Source Driver Output	
		Positive Polarity	Negative Polarity
0	18'h00000 ⋮ 18'h3FFFF	V63 ⋮ V0	V0 ⋮ V63
1	18'h00000 ⋮ 18'h3FFFF	V0 ⋮ V63	V63 ⋮ V0

D1-0: To set the internal operation, source driver output and VCOM output function. When D1-0=00; OTM2201A is set to standby mode. The combination of D1-0 and AM bit is summarized at **Table 5-9**.

Table 5-9

D1	D0	GON	Source output	Gate driver	VCOM	Display
0	0	X	VSSA	VGL	VSSA	Off
0	1	0	VSSA	VGL	VSSA	Off
		1	VSSA	Operate	VSSA	On
1	0	0	White(normally White)	VGL	Operate	Off
		1	Black(normally Black)	Operate	Operate	On
1	1	0	Normal display	VGL	Operate	Off
		1	Normal display	Operate	Operate	On

5.2.8. Blanking Control (R08h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default Value		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP3-0: Set the amount of blank period of front porch

BP3-0: Set the amount of blank period of back porch

Table 5-10 summarized the function of FP3-0/BP3-0 setting. When setting this register, make sure that:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal. Be aware that different interface mode, has different BP/ FP setting. **Figure 5-7** summarized the setting for each interface mode.

Table 5-10

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	**BP2**	**BP1**	**BP0**	**Number of lines for the Back Porch**
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

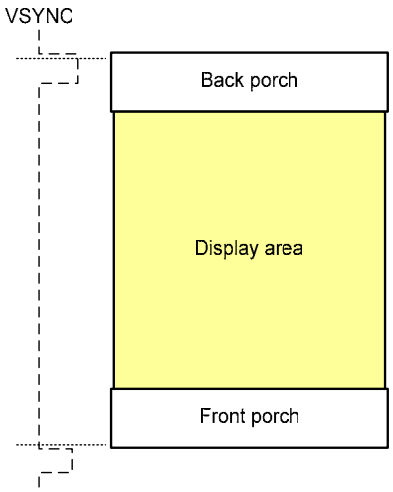


Figure 5-7 Front porch and back porch function diagram

5.2.9. Frame Cycle Control (R0Bh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	NO3	NO2	NO1	NO0	SDT3	SDT2	SDT1	SDT0	0	0	0	0	RTN3	RTN2	RTN1	RTN0
Default Value		0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0

NO[3:0]: Set the amount of non-overlap of gate output.

Table 5-11

NO3	NO2	NO1	NO0	Amount of non-overlap		
				Internal Operation (Internal CLK)	RGB Operation	
					18-bit (dot CLK)	6-bit (dot CLK)
0	0	0	0	Disabled	Disabled	Disabled
0	0	0	1	1	8	24
0	0	1	0	2	16	48
0	0	1	1	3	24	72
0	1	0	0	4	32	96
0	1	0	1	5	40	120
0	1	1	0	6	48	144
0	1	1	1	7	56	168
1	0	0	0	8	64	192
1	0	0	1	9	72	216
1	0	1	0	10	80	240
1	0	1	1	Disabled	88	264
1	1	0	0	Disabled	96	288
1	1	0	1	Disabled	104	312
1	1	1	0	Disabled	112	336
1	1	1	1	Disabled	120	360

SDT[3-0]: Set the delay from gate edge to source output.

Table 5-12

SDT3	SDT2	SDT1	SDT0	Amount of non-overlap		
				Internal Operation (Internal CLK)	RGB Operation	
					18-bit (dot CLK)	6-bit (dot CLK)
0	0	0	0	Disabled	Disabled	Disabled
0	0	0	1	1	8	24
0	0	1	0	2	16	48
0	0	1	1	3	24	72
0	1	0	0	4	32	96
0	1	0	1	5	40	120
0	1	1	0	6	48	144
0	1	1	1	7	56	168
1	0	0	0	8	64	192
1	0	0	1	9	72	216
1	0	1	0	10	80	240
1	0	1	1	Disabled	88	264
1	1	0	0	Disabled	96	288
1	1	0	1	Disabled	104	312
1	1	1	0	Disabled	112	336
1	1	1	1	Disabled	120	360

RTN3-0: Set the clock cycle per line **Table 5-13** summarized the function of PTG1-0 setting.

Table 5-13

RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	32 clocks
0	0	0	1	34 clocks
0	0	1	0	36 clocks
0	0	1	1	38 clocks
0	1	0	0	40 clocks
0	1	0	1	42 clocks
0	1	1	0	44 clocks
0	1	1	1	46 clocks
1	0	0	0	48 clocks
1	0	0	1	50 clocks
1	0	1	0	52 clocks
1	0	1	1	54 clocks
1	1	0	0	56 clocks
1	1	0	1	58 clocks
1	1	1	0	60 clocks
1	1	1	1	62 clocks

5.2.10. External Display Interface Control (R0Ch)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	RM	0	0	0	DM0	0	0	RIM1	RIM0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RM: Select the interface to access the OTM2201A's internal GRAM. Set RM to "1" when writing display data via the RGB interface. The OTM2201A allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface. .

Table 5-14

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

DM: To set the display operation mode.

Table 5-15 summarized the function of DM bit setting.

DM	Interface for RAM Access
0	Internal Clock Operation
1	RGB interface

RIM1-0: To set the different transfer modes of RGB interface. **Table 5-16** summarized the function of RIM1-0 setting.

Table 5-16

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer/pixel)
1	0	6-bit RGB interface (three transfers/pixel)
1	1	Setting disabled

For different display modes, different settings can be chosen so as to achieve the best efficiency.

Table 5-17

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 0)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 1)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM = 1)

Note1: Instructions are set only via the system interface.

Note2: Do not make changes to the RGB-I/F mode setting (RIM-0) while the RGB I/F is in operation.

Note3: See the "External Display Interface" section for the flowcharts to follow when switching from one mode to another.

5.2.11. Oscillator Control (R0Fh)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	FOSC3	FOSC3	FOSC2	FOSC1	FOSC0	0	0	0	0	0	0	0	OSCON
Default Value		0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1

FOSC[3:0]: Set the oscillation frequency.

Table 5-18

FOSC[4:0]	Oscillation Frequency [453kHz x The multiple listed the following]
00000	0.84
00001	0.86
00010	0.88
00011	0.90
00100	0.92
00101	0.95
00110	0.97
00111	1.00
01000	1.03
01001	1.06
01010	1.09
01011	1.13
01100	1.16
01101	1.20
01110	1.24
01111	1.29
10000	1.34

FOSC[4:0]	Oscillation Frequency [453kHz x The multiple listed the following]
10001	1.39
10010	1.44
10011	1.50
10100	1.57
10101	1.64
10110	1.72
10111	1.80
11000	1.90
11001	2.00
11010	2.12
11011	2.25
11100	2.40
11101	2.58
11110	2.77
11111	3.01

5.2.12. Power Control 1 (R10h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	SAP3	SAP2	SAP1	SAP0	0	0	0	0	0	0	DSTB	STB
Default Value		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

SAP3-0: Source driver operational amplifier DC bias current adjustment. Set SAP3-0 = “000” to stop operational amplifier to reduce current consumption during no display period. **Table 5-19** summarized the function of SAP3-0 setting

Table 5-19

SAP3	SAP2	SAP1	SAP0	Constant current in operational amplifier
0	0	0	0	Halt
0	0	0	1	Slow1
0	0	1	0	Slow2
0	0	1	1	Slow 3
0	1	0	0	Medium Slow 1
0	1	0	1	Medium Slow 2
0	1	1	0	Medium Slow 3
0	1	1	1	Medium Slow 4
1	0	0	0	Medium Fast 1
1	0	0	1	Medium Fast 2
1	0	1	0	Medium Fast 3
1	0	1	1	Medium Fast 4
1	1	0	0	Fast 1
1	1	0	1	Fast 2
1	1	1	0	Fast 3
1	1	1	1	Fast 4

STB: Set STB to equal 1 to enter standby mode, in this mode, display operation and all the internal operations including the internal RC oscillator are halted.

DSTB: When DSTB=1, OTM2201A set to deep standby mode. In this mode, all internal operations are terminated including RC oscillation. Set DSTB=0 can exit deep standby mode.

5.2.13. Power Control 2 (R11h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	APON	PON3	PON2	PON1	PON	0	AB_ VCI1	AON	VCI1 _EN	VC3	VC2	VC1	VC0
Default Value		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

APON:

APON = 1: Booster circuits are started automatically and sequentially.

APON = 0: Booster circuits would not start automatically. Instead, they are controlled independently through PON, PON1, PON2 and PON3.

PON3: Starting bit of VCL. Set PON3 equal to 1 to start VCL circuit.

PON2: Starting bit of VGL. Set PON2 equal to 1 to start VGL circuit.

PON1: Starting bit of VGH. Set PON1 equal to 1 to start VGH circuit.

PON: Starting bit of booster circuit 1. Set PON equal 1 to start booster circuit 1.

AB_VCI1: Set VCI1 equal to VCI.

AON: Starting bit of the amplifier. Set AON equal to 1 to start the circuit.

VCI1_EN: Set VCI1_EN = 1 to generate VCI1.

VC3-0: Set the voltage of VCI1. These bits set the VCI1 voltage up to 3V as the nominal output. The VCI1 output upper limit depends on VCI, VCI1 setting should meet VCI1 < VCI – 0.15V.

Table 5-20

VC3	VC2	VC1	VC0	VCI1
0	0	0	0	1.35
0	0	0	0	1.75
0	0	1	0	2.07
0	0	1	1	2.16
0	1	0	0	2.25
0	1	0	1	2.34
0	1	1	0	2.43
0	1	1	1	2.52
1	0	0	0	2.58
1	0	0	1	2.64
1	0	1	0	2.70
1	0	1	1	2.76
1	1	0	0	2.82
1	1	0	1	2.88
1	1	1	0	2.94
1	1	1	1	3

5.2.14. Power Control 3 (R12h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	BT2	BT1	BT0	0	0	DC11	DC10	0	0	DC21	DC20	0	0	DC31	DC30
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BT[2:0]: Control the voltages of VGH and VGL.

BT2	BT1	BT0	VGH	VGL
0	0	0	Vci1 x 5 [13.75V]	Vci1 x -3 [-8.25V]
0	0	1	Vci1 x 5 [13.75V]	Vci1 x -4 [-11V]
0	1	0	Vci1 x 6 [16.5V]	Vci1 x -3 [-8.25V]
0	1	1	Vci1 x 6 [16.5V]	Vci1 x -4 [-11V]
1	0	0	Vci1 x 6 [16.5V]	Vci1 x -5 [-8.25V]
1	0	1	Vci1 x 7 [19.25V]	Vci1 x -4 [-11V]
1	1	0	Setting Disabled	Setting Disabled
1	1	1	Setting Disabled	Setting Disabled

* The values of the voltage in the above table are obtained when Vci1 = 2.75V.

DC[11:10]: Set the operation frequency of the step-up circuit 1, DCCLK1.

DC11	DC10	Internal Operation (Synchronized with internal clock, CL1)	RGB Interface Operation (Synchronized with DOTCLK, DCCLK)
		f(CL1) : f(DCCLK1)	F(DCCLK) : f(DCCLK1)
0	0	1 : 4	1 : 1
0	1	1 : 2	1 : 0.5
1	0	1 : 1	1 : 0.25
1	1	Setting Disabled	Setting Disabled

DC[21:20]: Set the operation frequency of the step-up circuit 2, DCCLK2.

DC21	DC20	Internal Operation (Synchronized with internal clock, CL1)	RGB Interface Operation (Synchronized with DOTCLK, DCCLK)
		f(CL1) : f(DCCLK2)	F(DCCLK) : f(DCCLK2)
0	0	1 : 2	1 : 0.5
0	1	1 : 1	1 : 0.25
1	0	1 : 0.5	1 : 0.125
1	1	1 : 0.25	1 : 0.0625

DC[31-30]: Set the operation frequency of the step-up circuit 3, DCCLK3.

DC31	DC30	Internal Operation (Synchronized with internal clock, CL1)	RGB Interface Operation (Synchronized with DOTCLK, DCCLK)
		f(CL1) : f(DCCLK3)	F(DCCLK) : f(DCCLK3)
0	0	1 : 4	1 : 1
0	1	1 : 2	1 : 0.5
1	0	1 : 1	1 : 0.25
1	1	Setting Disabled	Setting Disabled

5.2.15. Power Control 4 (R13h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	DCR_EX	0	DCR2	DCR1	DCR0	0	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DCR_EX: Used in external interface mode.

DCR_EX = 0: Internal operation clock.

DCR_EX = 1: DOTCLK, if DM = 1, DOTCLK = DDCLK.

DCR[2:0]: Set the clock cycle of the step-up circuit in external interface mode.

DCR2	DCR1	DCR0	Clock cycle for step-up circuits(DCCLK) in external interface mode	
			18-bit RGB	6-bit RGB
0	0	0	6 dot clk	18 dot clk
0	0	1	8 dot clk	24 dot clk
0	1	0	12 dot clk	36 dot clk
0	1	1	16 dot clk	48 dot clk
1	0	0	24 dot clk	72 dot clk
1	0	1	32 dot clk	96 dot clk
1	1	0	48 dot clk	144 dot clk
1	1	1	64 dot clk	192 dot clk

GVD[6:0]: Set the Gamma voltage and setting should meet GVDD < AVDD (VCI1*2) - 0.3V.

GVD[6:0]	GVDD voltage	GVD[6:0]	GVDD Voltage
0000000	2.50V	1000000	3.76V
0000001	2.52V	1000001	3.78V
0000010	2.54V	1000010	3.80V
0000011	2.56V	1000011	3.82V
0000100	2.58V	1000100	3.84V
0000101	2.60V	1000101	3.86V
0000110	2.62V	1000110	3.88V
0000111	2.64V	1000111	3.90V
0001000	2.66V	1001000	3.92V
0001001	2.68V	1001001	3.94V
0001010	2.70V	1001010	3.96V
0001011	2.72V	1001011	3.98V
0001100	2.74V	1001100	4.00V
0001101	2.76V	1001101	4.02V
0001110	2.78V	1001110	4.04V
0001111	2.80V	1001111	4.06V
0010000	2.81V	1010000	4.07V
0010001	2.83V	1010001	4.09V
0010010	2.85V	1010010	4.11V
0010011	2.87V	1010011	4.13V
0010100	2.89V	1010100	4.15V
0010101	2.91V	1010101	4.17V
0010110	2.93V	1010110	4.19V
0010111	2.95V	1010111	4.21V
0011000	2.97V	1011000	4.23V
0011001	2.99V	1011001	4.25V
0011010	3.01V	1011010	4.27V
0011011	3.03V	1011011	4.29V
0011100	3.05V	1011100	4.31V
0011101	3.07V	1011101	4.33V
0011110	3.09V	1011110	4.35V
0011111	3.11V	1011111	4.37V
0100000	3.13V	1100000	4.39V
0100001	3.15V	1100001	4.41V
0100010	3.17V	1100010	4.43V
0100011	3.19V	1100011	4.45V
0100100	3.21V	1100100	4.47V
0100101	3.23V	1100101	4.49V
0100110	3.25V	1100110	4.51V
0100111	3.27V	1100111	4.53V
0101000	3.29V	1101000	4.55V
0101001	3.31V	1101001	4.57V
0101010	3.33V	1101010	4.59V
0101011	3.35V	1101011	4.61V
0101100	3.37V	1101100	4.63V
0101101	3.39V	1101101	4.65V
0101110	3.41V	1101110	4.67V
0101111	3.43V	1101111	4.69V
0110000	3.44V	1110000	4.70V
0110001	3.46V	1110001	4.72V
0110010	3.48V	1110010	4.74V
0110011	3.50V	1110011	4.76V

0110100	3.52V	1110100	4.78V
0110101	3.54V	1110101	4.80V
0110110	3.56V	1110110	4.82V
0110111	3.58V	1110111	4.84V
0111000	3.60V	1111000	4.86V
0111001	3.62V	1111001	4.88V
0111010	3.64V	1111010	4.90V
0111011	3.66V	1111011	4.92V
0111100	3.68V	1111100	4.94V
0111101	3.70V	1111101	4.96V
0111110	3.72V	1111110	4.98V
0111111	3.74V	1111111	5.00V

5.2.16. Power Control 5 (R14h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	VCOMG	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCMR	VML6	VML5	VML4	VML3	VML2	VML1	VML0
Default Value		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCOMG:

VCOMG = 1, VCOML should be fixed to VSSA. Amplitude of VCOM = $|VCOMH - VSSA|$

VCOMG = 0, amplitude of VCOM = $|VCOMH - VCOML|$

VCM[6:0]: Set the voltage of VCOMH and setting should meet VCOMH < AVDD(2*VCI1) - 0.3V.

.

VCM[6:0]	VCOMH	VCM[6:0]	VCOMH
0000000	GVDD x 0.4015	1000000	GVDD x0.7535
0000001	GVDD x 0.4070	1000001	GVDD x0.7590
0000010	GVDD x 0.4125	1000010	GVDD x0.7645
0000011	GVDD x 0.4180	1000011	GVDD x0.7700
0000100	GVDD x 0.4235	1000100	GVDD x0.7755
0000101	GVDD x 0.4290	1000101	GVDD x0.7810
0000110	GVDD x 0.4345	1000110	GVDD x0.7865
0000111	GVDD x 0.4400	1000111	GVDD x0.7920
0001000	GVDD x 0.4455	1001000	GVDD x0.7975
0001001	GVDD x 0.4510	1001001	GVDD x0.8030
0001010	GVDD x 0.4565	1001010	GVDD x0.8085
0001011	GVDD x 0.4620	1001011	GVDD x0.8140
0001100	GVDD x 0.4675	1001100	GVDD x0.8195
0001101	GVDD x 0.4730	1001101	GVDD x0.8250
0001110	GVDD x 0.4785	1001110	GVDD x0.8305
0001111	GVDD x 0.4840	1001111	GVDD x0.8360
0010000	GVDD x 0.4895	1010000	GVDD x0.8415
0010001	GVDD x 0.4950	1010001	GVDD x0.8470
0010010	GVDD x 0.5005	1010010	GVDD x0.8525
0010011	GVDD x 0.5060	1010011	GVDD x0.8580
0010100	GVDD x 0.5155	1010100	GVDD x0.8635
0010101	GVDD x0.5170	1010101	GVDD x0.8690
0010110	GVDD x 0.5225	1010110	GVDD x0.8745
0010111	GVDD x 0.5280	1010111	GVDD x0.8800
0011000	GVDD x0.5335	1011000	GVDD x0.8855
0011001	GVDD x0.5390	1011001	GVDD x0.8910

0011010	GVDD x0.5445	1011010	GVDD x0.8965
0011011	GVDD x0.5500	1011011	GVDD x0.9020
0011100	GVDD x0.5555	1011100	GVDD x0.9075
0011101	GVDD x0.5610	1011101	GVDD x0.9130
0011110	GVDD x0.5665	1011110	GVDD x0.9185
0011111	GVDD x0.5720	1011111	GVDD x0.9240
0100000	GVDD x0.5775	1100000	GVDD x0.9295
0100001	GVDD x0.5830	1100001	GVDD x0.9350
0100010	GVDD x0.5885	1100010	GVDD x0.9405
0100011	GVDD x0.5940	1100011	GVDD x0.9460
0100100	GVDD x0.5995	1100100	GVDD x0.9515
0100101	GVDD x0.6050	1100101	GVDD x0.9570
0100110	GVDD x0.6105	1100110	GVDD x0.9625
0100111	GVDD x0.6160	1100111	GVDD x0.9680
0101000	GVDD x0.6215	1101000	GVDD x0.9735
0101001	GVDD x0.6270	1101001	GVDD x0.9790
0101010	GVDD x0.6325	1101010	GVDD x0.9845
0101011	GVDD x0.6380	1101011	GVDD x0.9900
0101100	GVDD x0.6435	1101100	GVDD x0.9955
0101101	GVDD x0.6490	1101101	GVDD x1.0010
0101110	GVDD x0.6545	1101110	GVDD x1.0065
0101111	GVDD x0.6600	1101111	GVDD x1.0120
0110000	GVDD x0.6655	1110000	GVDD x1.0175
0110001	GVDD x0.6710	1110001	GVDD x1.0230
0110010	GVDD x0.6765	1110010	GVDD x1.0285
0110011	GVDD x0.6820	1110011	GVDD x1.0340
0110100	GVDD x0.6875	1110100	GVDD x1.0395
0110101	GVDD x0.6930	1110101	GVDD x1.0450
0110110	GVDD x0.6985	1110110	GVDD x1.0505
0110111	GVDD x0.7040	1110111	GVDD x1.0560
0111000	GVDD x0.7075	1111000	GVDD x1.0615
0111001	GVDD x0.7150	1111001	GVDD x1.0670
0111010	GVDD x0.7205	1111010	GVDD x1.0725
0111011	GVDD x0.7260	1111011	GVDD x1.0780
0111100	GVDD x0.7315	1111100	GVDD x1.0835
0111101	GVDD x0.7370	1111101	GVDD x1.0890
0111110	GVDD x0.7425	1111110	GVDD x1.0945
0111111	GVDD x0.7480	1111111	GVDD x1.1000

VCMR:

VCMR = 0: VCOMH is determined by VCM[6:0].

VCMR = 1: VCOMH is determined external voltage supply, VCOMR.

VML[6:0]: Set the amplitude of VCOM.

VML[6:0]	VCOM Amplitude	VML[6:0]	VCOM Amplitude
0000000	Setting Disabled	1000111	GVDD x 0.864
…	Setting Disabled	1001000	GVDD x 0.870
0001111	Setting Disabled	1001001	GVDD x 0.876
0010000	GVDD x 0.534	1001010	GVDD x 0.882
0010001	GVDD x 0.540	1001011	GVDD x 0.888
0010010	GVDD x 0.546	1001100	GVDD x 0.894
0010011	GVDD x 0.552	1001101	GVDD x 0.900
0010100	GVDD x 0.558	1001110	GVDD x 0.906

0010101	GVDD x 0.564	1001111	GVDD x 0.912
0010110	GVDD x 0.570	1010000	GVDD x 0.918
0010111	GVDD x 0.576	1010001	GVDD x 0.924
0011000	GVDD x 0.582	1010010	GVDD x 0.930
0011001	GVDD x 0.588	1010011	GVDD x 0.936
0011010	GVDD x 0.594	1010100	GVDD x 0.942
0011011	GVDD x 0.600	1010101	GVDD x 0.948
0011100	GVDD x 0.606	1010110	GVDD x 0.954
0011101	GVDD x 0.612	1010111	GVDD x 0.960
0011110	GVDD x 0.618	1011000	GVDD x 0.966
0011111	GVDD x 0.624	1011001	GVDD x 0.972
0100000	GVDD x 0.630	1011010	GVDD x 0.978
0100001	GVDD x 0.636	1011011	GVDD x 0.984
0100010	GVDD x 0.642	1011100	GVDD x 0.990
0100011	GVDD x 0.648	1011101	GVDD x 0.996
0100100	GVDD x 0.654	1011110	GVDD x 1.002
0100101	GVDD x 0.660	1011111	GVDD x 1.008
0100110	GVDD x 0.666	1100000	GVDD x 1.014
0100111	GVDD x 0.672	1100001	GVDD x 1.020
0101000	GVDD x 0.678	1100010	GVDD x 1.026
0101001	GVDD x 0.684	1100011	GVDD x 1.032
0101010	GVDD x 0.690	1100100	GVDD x 1.038
0101011	GVDD x 0.696	1100101	GVDD x 1.044
0101100	GVDD x 0.702	1100110	GVDD x 1.050
0101101	GVDD x 0.708	1100111	GVDD x 1.056
0101110	GVDD x 0.714	1101000	GVDD x 1.062
0101111	GVDD x 0.720	1101001	GVDD x 1.068
0110000	GVDD x 0.726	1101010	GVDD x 1.074
0110001	GVDD x 0.732	1101011	GVDD x 1.080
0110010	GVDD x 0.738	1101100	GVDD x 1.086
0110011	GVDD x 0.744	1101101	GVDD x 1.092
0110100	GVDD x 0.750	1101110	GVDD x 1.098
0110101	GVDD x 0.756	1101111	GVDD x 1.104
0110110	GVDD x 0.762	1110000	GVDD x 1.110
0110111	GVDD x 0.768	1110001	GVDD x 1.116
0111000	GVDD x 0.774	1110010	GVDD x 1.122
0111001	GVDD x 0.780	1110011	GVDD x 1.128
0111010	GVDD x 0.786	1110100	GVDD x 1.134
0111011	GVDD x 0.792	1110101	GVDD x 1.140
0111100	GVDD x 0.798	1110110	GVDD x 1.146
0111101	GVDD x 0.804	1110111	GVDD x 1.152
0111110	GVDD x 0.810	1111000	GVDD x 1.158
0111111	GVDD x 0.816	1111001	GVDD x 1.164
1000000	GVDD x 0.822	1111010	GVDD x 1.170
1000001	GVDD x 0.828	1111011	GVDD x 1.176
1000010	GVDD x 0.834	1111100	GVDD x 1.182
1000011	GVDD x 0.840	1111101	GVDD x 1.188
1000100	GVDD x 0.846	1111110	GVDD x 1.194
1000101	GVDD x 0.852	1111111	GVDD x 1.200
1000110	GVDD x 0.858		

5.2.17. VCI Period (R15h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	VCIR2	VCIR1	VCR0	0	0	0	0
Default Value		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCIR[2:0]: Set the period of VCI

VCIR2	VCIR1	VCIR0	Period of VCIR			
			Internal Operation (Synchronized with oscillator)			RGB interface operation (Synchronized with DOTCLK)
			Sn	Vcom1	Vcom2	
0	0	0	Off			Off
0	0	1	Setting Disabled			Setting Disabled
0	1	0	2	1/2	2/1	16 dot clock
0	1	1	3	1.5/3	3/1.5	32 dot clock
1	0	0	4	2/4	4/2	48 dot clock
1	0	1	5	2.5/5	5/2.5	64 dot clock
1	1	0	6	3/6	6/3	80 dot clock
1	1	1	7	3.5/7	7/3.5	96 dot clock

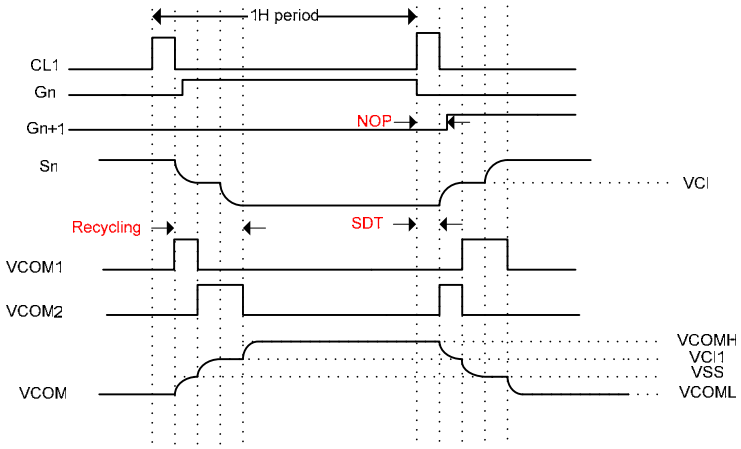


Figure 5-8 Set Delay from Gate Output To Source Output and VCIR Signal

5.2.18. RAM Address (R20h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

5.2.19. RAM Address (R21h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD15–0: To set the initial address counter for GRAM address. Based on AM and ID setting, the address counter is automatically increment or decrement while data are written to the internal GRAM There is no need to updated AD15-0 every data transfer if AD15-0 was set in the beginning of one frame graphic data. Be aware that address counter is not automatically updated if reading

data from the internal GRAM instruction is executed. Moreover, the address counter cannot be accessed when the OTM2201A is in standby mode.

Note1: The address AD15-0 should be set in the address counter every frame on the falling edge of VSYNC if RGB interface mode is selected.

Note2: The address AD15-0 should be set when executing an instruction if system or VSYNC interface mode is selected.

Table 5-21

AD15–AD0	GRAM Setting
“0000”H – “00AF”H	Bitmap data for G1
“0100”H – “01AF”H	Bitmap data for G2
“0200”H – “02AF”H	Bitmap data for G3
“0300”H – “03AF”H	Bitmap data for G4
:	:
“D800”H – “D8AF”H	Bitmap data for G217
“D900”H – “D9AF”H	Bitmap data for G2318
“DA00”H – “DAAF”H	Bitmap data for G219
“DB00”H – “DBAF”H	Bitmap data for G220

5.2.20. GRAM Data (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different interface modes.															

WD17-0: OTM2201A supports 18 bits data format. However, if only 16-bit (565format) is input to GRAM, OTM2201A will expand the 16 bit data into 18-bit format. Same case when RGB interface is selected. Based on the graphic data in GRAM, the grayscale voltage of source driver is selected.

5.2.21. Read Data Read from GRAM (R22h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	RAM write data (WD17-0) The DB17-0 pin assignment is different in different interface modes.															

R22 also served as a register, which store the data read out from GRAM. When data are read out from the GRAM is desired, first sets the RAM address and executes first word read, and issues second word read. When first word read instruction is issued, Invalid data are sent to the data bus DB17-0. Valid data are sent to the data bus as second word data is executed.

5.2.22. Software Reset (R28h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0

Software reset is invoked if the parameter is 00CEh. The reset signal will be set to low while software reset is recognized. And its return to high automatically after reset finished.

5.2.23. Gate Scan Start Position (R30h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[4:0]: Set the start position of gate driver.

SCN4-0	Starting Position	
	GS=0	GS=1
00000	G1	G220
00001	G9	G216
00010	G17	G208
…	…	…
11001	G201	G24
11010	G209	G16
11011	G217	G8

5.2.24. Vertical Scrolling Control 1 (R31h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0
Default Value		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

SEA[7:0]: Set the scrolling end address.

SEA[7:0]	End Address
00000000	0
00000001	1
00000010	2
00000011	3
00000100	4
00000101	5
…	…
11011000	216
11011001	217
11011010	218
11011011	219

Note1: Don't set any higher address than 219(DBh).

Note2: Set SS[7:0]≦SSA[7:0], if out of range, SSA[7:0]=SS[7:0]

Note3: Set SE[7:0]≧SEA[7:0], if out of range, SEA[7:0]=SE[7:0]

5.2.25. Vertical Scrolling Control 2 (R32h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SSA[7:0]: Set the scrolling start address.

SSA[7:0]	Scrolling Start Address
00000000	0
00000001	1
00000010	2
00000011	3
00000100	4
00000101	5
…	…
11011000	216
11011001	217
11011010	218
11011011	219

5.2.26. Vertical Scrolling Control 3 (R33h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SST[8:0]: Define the step size of the scrolling function. When SST[7:0]=00h. Vertical Scroll function is disabled

SST[7:0]	Scrolling step size
00000000	Setting Disabled
00000001	1 row
00000010	2 rows
00000011	3 rows
00000100	4 rows
00000101	5 rows
……	……
11011000	216 rows
11011001	217 rows
11011010	218 rows
11011011	219 rows

Note1: Don't set any higher address than 219(DBh).

Note2: Set SS[7:0] < (SSA[7:0] + SST[7:0]) ≦ SEA[7:0] ≦ SE[7:0], If set out of range, Scroll function is disabled.

5.2.27. Partial Screen Area 1 (R34h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	SE7	SE6	SE5	SE4	SE3	SE2	SE1	SE0
Default Value		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

SE[7:0]: Set the partial screen end address. The gate driver ends at "set value + 1".

5.2.28. Partial Screen Area 2 (R35h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS[7:0]: Set the partial screen start address. The gate driver starts at "set value + 1".

5.2.29. Horizontal Window Address 1 (R36h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
Default Value		0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	0

HSA[7:0]: Set the horizontal start position of a window for memory access. Data can be written to the GRAM from the address specified by **HSA[7:0]** to the address specified by **HEA[7:0]**.

5.2.30. Horizontal Window Address 2 (R37h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

HEA[7:0]: Set the horizontal end position of a window for memory access.

5.2.31. Vertical Window Address 1 (R38h)

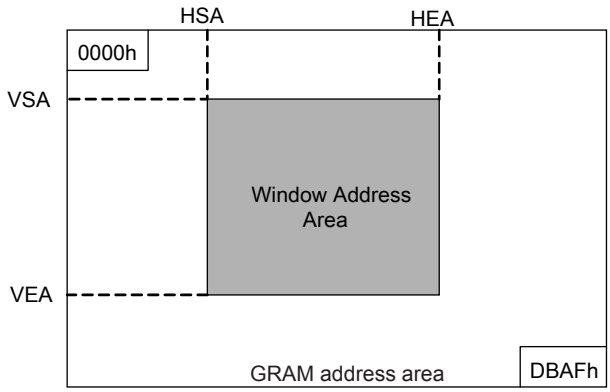
R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
Default Value		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

VSA[7:0]: Set the vertical start position for memory access. Data can be written to the GRAM from the address specified by **VAS[7:0]** to the address specified by **VEA[7:0]**.

5.2.32. Vertical Window Address (R39h)

R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
W	1	0	0	0	0	0	0	0	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
Default Value		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VEA[7:0]: Set the vertical end position of a window for memory access.



Windows address setting range

“00”h ≦ HSA7-0 ≦ HEA7-0 ≦ “AF”h ,

“00”h ≦ VSA7-0 ≦ VEA7-0 ≦ “DB”h

Note1: Ensure that the window address area is within the GRAM address space

5.2.33. γ Control (R50h to R59h)

Table 5-22

	R/W	RS	CB15	CB14	CB13	CB12	CB11	CB10	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
R50	W	1	0	0	0	0	PVR3V83	PVR3V82	PVR3V81	PVR3V80	0	0	0	0	PVR3V13	PVR3V12	PVR3V11	PVR3V10
R51	W	1	0	0	0	0	PVR3V433	PVR3V432	PVR3V431	PVR3V430	0	0	0	0	PVR3V203	PVR3V202	PVR3V201	PVR3V200
R52	W	1	0	0	0	0	PVR3V623	PVR3V622	PVR3V621	PVR3V620	0	0	0	0	PVR3V553	PVR3V552	PVR3V551	PVR3V550
R53	W	1	0	0	0	0	PRP13	PRP12	PRP11	PRP10	0	0	0	0	PRP03	PRP02	PRP01	PRP00
R54	W	1	0	0	0	0	NVR3V83	NVR3V82	NVR3V81	NVR3V80	0	0	0	0	NVR3V13	NVR3V12	NVR3V11	NVR3V10
R55	W	1	0	0	0	0	NVR3V433	NVR3V432	NVR3V431	NVR3V430	0	0	0	0	NVR3V203	NVR3V202	NVR3V201	NVR3V200
R56	W	1	0	0	0	0	NVR3V623	NVR3V622	NVR3V621	NVR3V620	0	0	0	0	NVR3V553	NVR3V552	NVR3V551	NVR3V550
R57	W	1	0	0	0	0	PRN13	PRN12	PRN11	PRN10	0	0	0	0	PRN03	PRN02	PRN01	PRN00
R58	W	1	0	0	0	PVR1V634	PVR1V633	PVR1V632	PVR1V631	PVR1V630	0	0	0	PVR1V04	PVR1V03	PVR1V02	PVR1V01	PVR1V00
R59	W	1	0	0	0	NVR1V634	NVR1V633	NVR1V632	NVR1V631	NVR1V630	0	0	0	NVR1V04	NVR1V03	NVR1V02	NVR1V01	NVR1V00

All of initial values of register are “0”.

6. INTERFACES

The OTM2201A provides different interfaces to meet the diverse need of small/medium size LCD. Based on the application requirement, there are three different display modes which are most used in end product.

1. Still picture display
2. Moving picture display.
3. Re-writing still pictures while moving picture are display.

For above three different display requirements, OTM2201A provides different interfaces to meet the requirement.

1. System interface
2. External interface (RGB interface)

System interface is suitable for still picture display while RGB interface suitable for moving picture display. Be aware that RGB still can used to display still picture and system interface can also display moving picture. **Table 6-1** summarized different interfaces for different display requirement.

Table 6-1

Operation Mode	Display Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
System	Still picture	System interface (RM = 0)	Internal operating clock (DM = 0)
RGB interface (1)	Moving picture	RGB interface (RM = 1)	RGB interface (DM = 1)
RGB interface (2)	Rewriting still pictures while displaying moving pictures	System interface (RM = 0)	RGB interface (DM = 1)

6.1. System Interface

The system interfaces of OTM2201A can support 8-bit, 9-bit, 16-bit, 18-bit 80-system Interface and Serial Peripheral Interface (SPI), which can be set by the IM3/2/1/0 pins. The system interface can set instructions and access RAM. **Table 6-2** summarized the interface corresponding to IM3-0 setting.

Table 6-2

IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pin in use
0	0	0	0	68-system 16-bit interface	DB17-10, DB8-1
0	0	0	1	68-system 8-bit interface	DB17-10
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1
0	0	1	1	80-system 8-bit interface	DB17-10
0	1	0	*	Clock synchronous serial interface	-
0	1	1	0	Setting disabled	-
0	1	1	1	Setting disabled	-
1	0	0	0	68-system 18-bit interface	DB17-0
1	0	0	1	68-system 9-bit interface	DB17-9
1	0	1	0	80-system 18-bit interface	DB17-0
1	0	1	1	80-system 9-bit interface	DB17-9
1	1	*	*	Setting disabled	-

6.1.1. 68-/80-system 18-bit interface

The instruction and GRAM accessing format of 80-system 18-bit interface are shown in **Figure 6-1** and **Figure 6-2**, respectively.

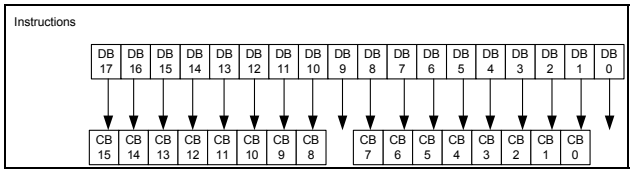


Figure 6-1

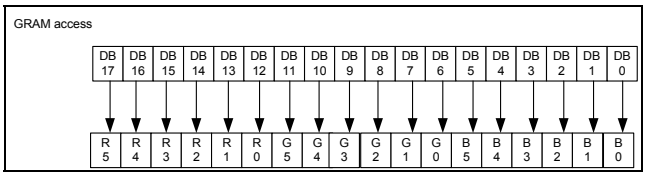


Figure 6-2

6.1.2. 68-/80-system 16-bit interface

The instruction and GRAM accessing format of 80-system 16-bit interface are shown in **Figure 6-3** and **Figure 6-4**, respectively.

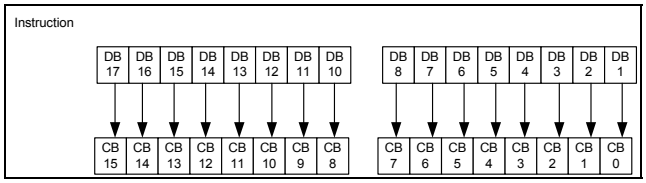


Figure 6-3

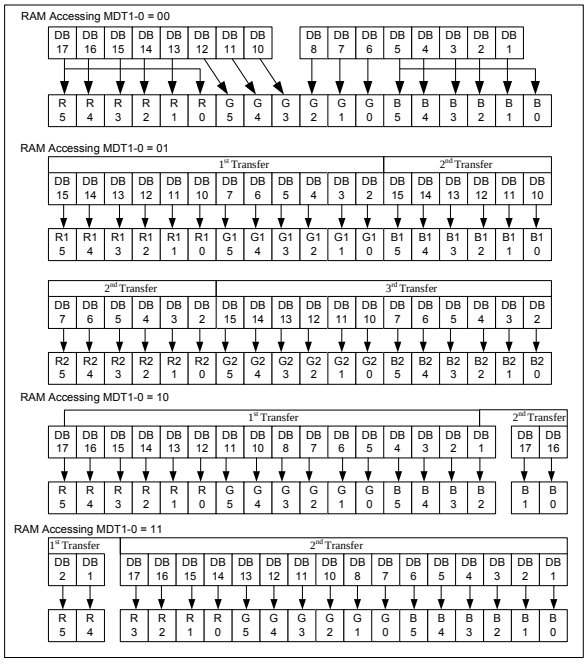


Figure 6-4

6.1.3. 68-/80-system 9-bit interface

The instruction and GRAM accessing format of 80-system 9-bit interface are shown in **Figure 6-5** and **Figure 6-6**, respectively.

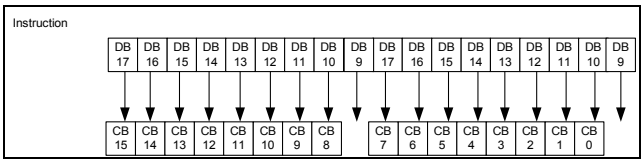


Figure 6-5

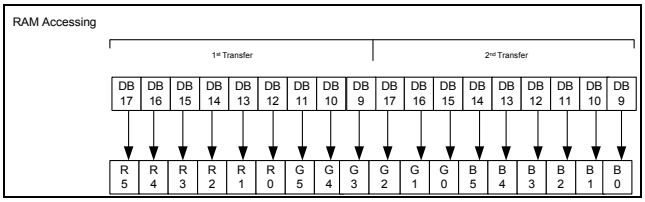


Figure 6-6

6.1.4. 68-/80-system 8-bit interface

The instruction and GRAM accessing format of 80-system 8-bit interface are shown in **Figure 6-7** and **Figure 6-8**, respectively.

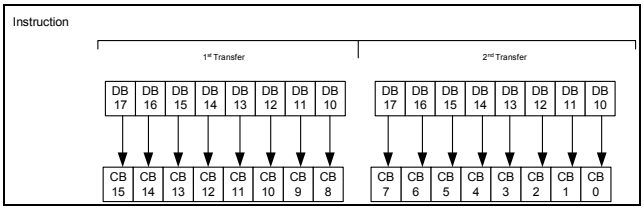


Figure 6-7

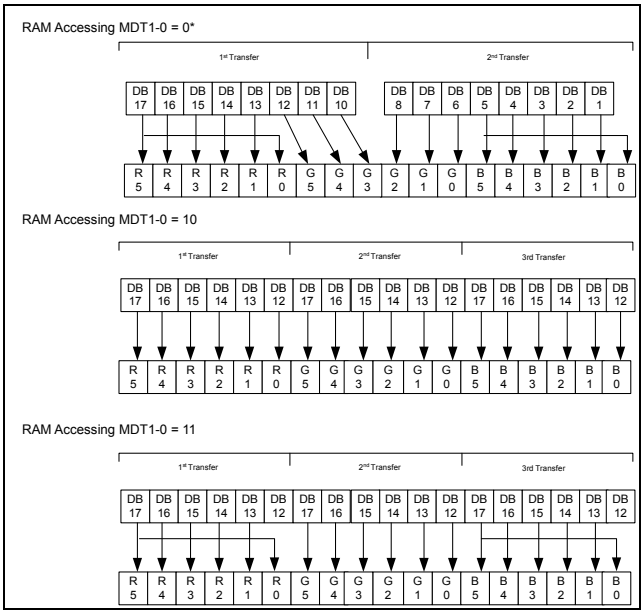


Figure 6-8

6.1.5. Serial Peripheral interface (SPI)

The system interface of OTM2201A also includes the Serial Peripheral Interface (SPI). In SPI mode, /CS, SCL, SDI and SDO are used to transfer data between MCU and OTM2201A. IM0/ID pin served as the ID pin. **Figure 6-9** illustrates the detail timing while using SPI. Be aware that the unused pins such as DB17-0 pins must be fixed at either IOVcc or GND level.

The instruction and GRAM accessing format of SPI interface are shown in **Figure 6-10** and **Figure 6-11**, respectively.

When read operation is desired In SPI mode, valid data are read out as the OTM2201A reads out the 6th byte data from the internal GRAM.

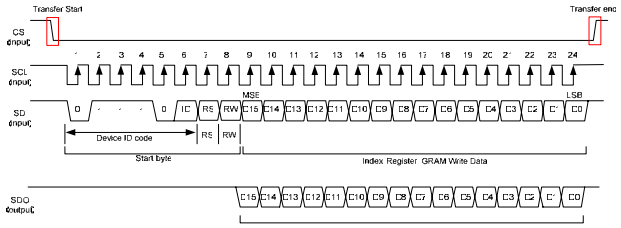


Figure 6-9

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note 1) ID bit is selected by setting the IM0/ID pin.

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

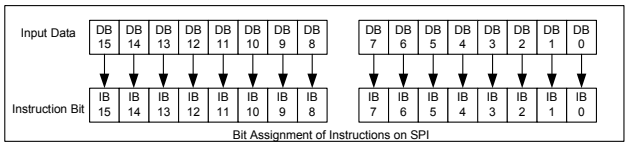


Figure 6-10

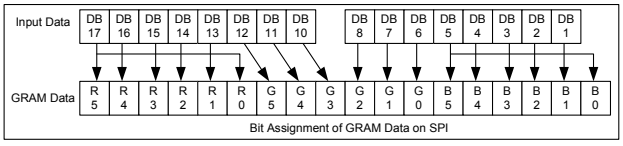


Figure 6-11

External Display Interface

OTM2201A also includes external (RGB) interface for displaying moving picture. External interface can be set by RIM1-0 bit. **Table 6-3** summarized the corresponding types of RGB interface with RIM1-0 setting.

Table 6-3

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, 11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting disabled	

RGB interface can access OTM2201A by VSYNC, HSYNC, ENABLE, DOTCLK and DB17-0 signals, where VSYNC is used for frame synchronization; HSYNC is used for line synchronization and ENABLE is served as the valid data synchronized signals. The RGB interface can be rewriting minimum necessary data to the GRAM area which need to be overwritten with use of window address function and high-speed write mode. It is necessary for RGB interface to set front and back porch periods after and before a display period, respectively. Figure 6-12 illustrates the general timing for RGB interface. In RGB interface VSYNC, HSYNC, and DOTCLK signals must be supplied at much higher resolution than that of the panel.

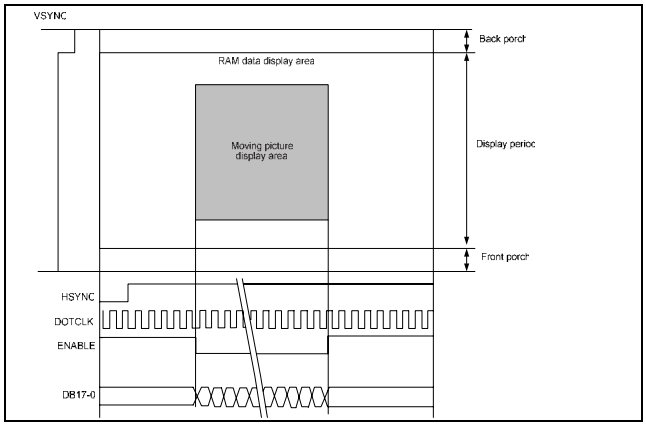


Figure 6-12

RGB interface includes ENABLE signal served as valid data synchronized signals. Moreover, the active level for ENABLE can be set by EPL. The EPL bit inverts the polarity of ENABLE signal. **Table 6-4** summarized the setting of EPL and ENABLE active level for GRAM accessing. Setting both EPL and ENABLE bits to automatically update RAM address in the AC is necessary while writing data to the GRAM.

Table 6-4

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

OTM2201A can support 18-bit, 16-bit and 6-bit RGB interface. The detail timing diagram for 18-bit, 16-bit and 6-bit RGB interface are shown in **Figure 6-13** and **Figure 6-14** respectively.

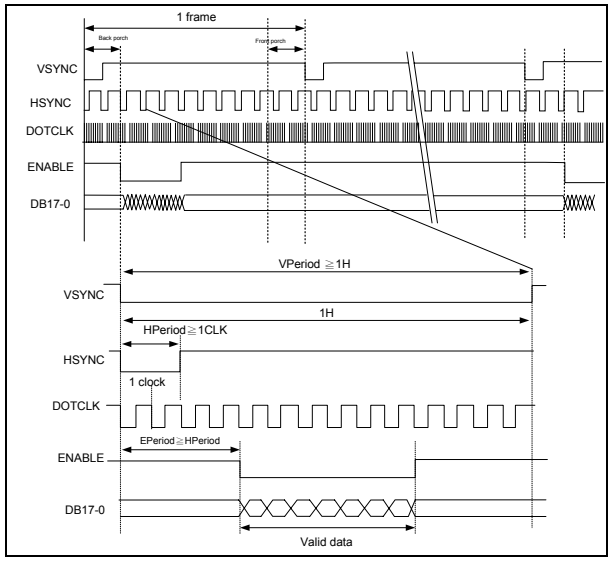


Figure 6-13

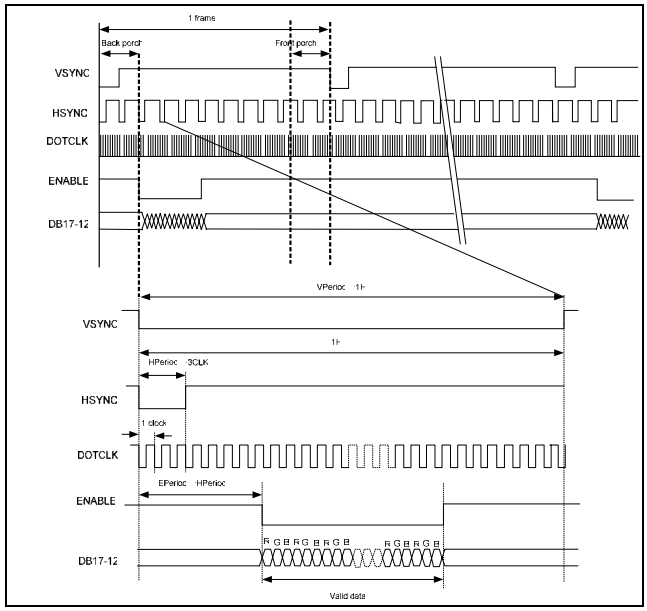


Figure 6-14

The RGB interface also has the window address function to

transfer only minimum necessary data on the moving picture GRAM area, which can lower the power consumption and still can use system interface to rewrite data in still picture RAM area while displaying a moving picture. Setting RM = 0 while in RGB interface mode can make GRAM accessible through the system interface. When RGB interface accessing GRAM is desired, wait for one read/write bus cycle following by RM = 1 setting.

Figure 6-15 illustrates the timing diagram when displaying a moving picture through the RGB interface and rewriting data in the still picture GRAM area through the system interface.

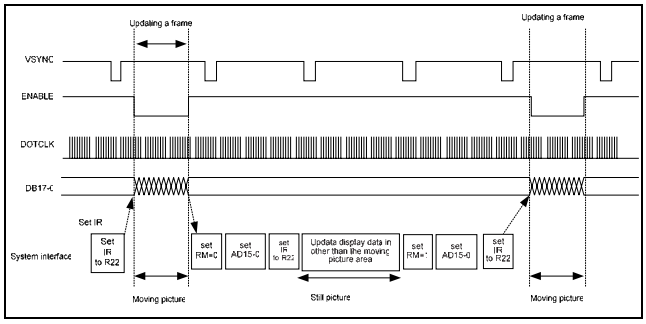


Figure 6-15

6.1.6. 6-bit RGB interface

RAM accessing format and data transmission synchronization of 6-bit RGB interface are shown in **Figure 6-16** and **Figure 6-17**, respectively.

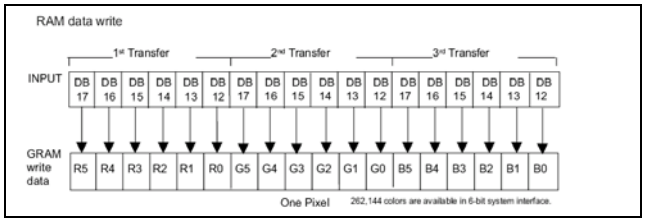


Figure 6-16

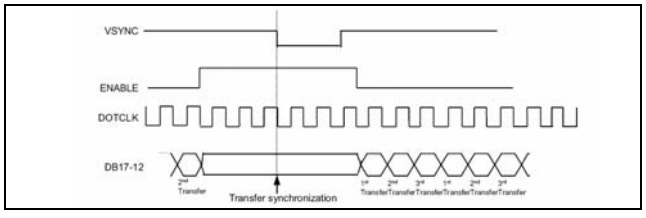


Figure 6-17

6.1.7. 16-bit RGB interface

RAM accessing format of 16-bit RGB interface are shown in **Figure 6-18**.

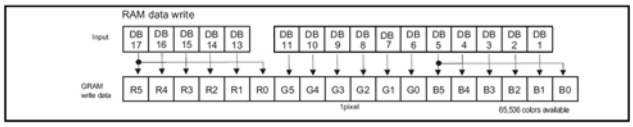


Figure 6-18

6.1.8. 18-bit RGB interface

RAM accessing format of 18-bit RGB interface are shown in **Figure 6-19**.

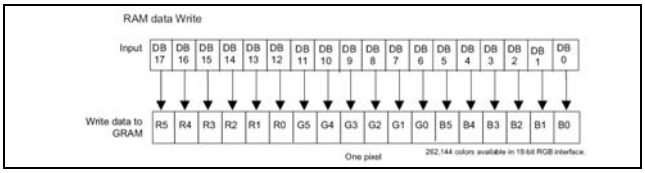


Figure 6-19

7. RESET FUNCTION

The OTM2201A can be reset by hardware (/RESET pin). While /RESET is in low level (RESET period), accessing to instructions or to GRAM data are terminated temporarily. Be sure that /RESET period must last at least 20us for RESET function to be functional. In case of power-on reset, wait at least 10ms for RC oscillation stabilization. Moreover, GRAM data are not initialized automatically during RESET period.

7.1. Initial state of instruction bits

2 Driver Output Control (VSPL =0, HSPL = 0, DPL = 0, EPL = 0, SM = 0, GS = 0, SS = 0, NL4-0 = 11100)
3 LCD Driving AC Control (INV1-0 = 01, FLD = 0))
4 Entry mode set (BGR = 0, MDT1-0 = 00, I/D1-0 = 11, AM = 0)
5 Display Control (FLM_MON = 0, GON = 0, CL = 0, REV = 0, D1-0 = 00: Display off)
6 Blank Period Control (FP3-0 = 1000, BP3-0 = 1000)
7 Frame Cycle Control (NO3-0 = 0001, SDT3-0 = 0001, RTN3-0 = 0000: 16 clock cycle in 1H period)
8 External Display Interface (RIM1-0 = 00: 18 bit RGB interface, DM = 0: operation by internal clock, RM = 0: system interface)
9 Start oscillation (FOSC4-0 = 01111, OSCON = 1)
10 Power Control 1 (SAP3-0 = 0010, STB = 0)
11 Power Control 2 (APON = 0, PON3-0 =0000, AB_VCI1 = 0, AON – 0, VCI1_EN = 0, VC3-0 = 0000)
12 Power Control 3 (BT2-0 = 000, DC11-10 = 00, DC21-2 = 00, DC31-30 = 00)
13 Power Control 4 (DCR_EX = 0, DCR2-0 = 000, GVD6-0 = 0000000)
14 Power Control 5 (VCOMG = 0, VCMR = 0, VCM6-0 = 0000000, VML6-0 = 0000000)
15 VCIR Recycling (VCIR2-0 = 000)
16 RAM Address data (AD7-0 = 00000000, AD15-8 = 00000000)
17 Gate Scan Position (SCN4-0 = 00000)
18 Vertical Scroll Control 1 (SSA7-0 = 00000000, SEA7-0 = 11011011)
19 Vertical Scroll Control 2 (SST7-0 = 00000000 : No Vertical Scroll)
20 Partial Screen Division (SE17-10 = 11011011, SS17-10 = 00000000)
21 Horizontal RAM Address Position (HEA7-0 = 10101111, HSA7-0 = 00000000)
22 Vertical RAM Address Position (VEA7-0 = 11011011, VSA7-0 = 00000000)
23 Gamma Control
24 Test Key Command (00000000)

8. SCAN MODE SETTING

The OTM2201A can change the shift direction of outputting gate signals in 4 different ways with combination of SM and GS bits, allowing various connections between the OTM2201Aand the LCD panel.

9. γ -CORRECTION FUNCTION

OTM2201A adopt Gamma voltage generation circuit which can provide wider output voltage range to fit the different kind of liquid crystal for Gamma curve from 1.0~2.5. The Gamma output voltage can be set by R50h~R59h.

PVR3V1 [3:0]: register for positive VSD1 fine tune adjustment.
PVR3V8 [3:0]: register for positive VSD8 fine tune adjustment.
PVR3V20 [3:0]: register for positive VSD20 fine tune adjustment.
PVR3V43 [3:0]: register for positive VSD43 fine tune adjustment.
PVR3V55 [3:0]: register for positive VSD55 fine tune adjustment.
PRP0 [3:0]: register for positive VSD fine tune adjustment
PRP1 [3:0]: register for positive VSD fine tune adjustment
PVR1V0 [4:0]: register for positive VSD0 fine tune adjustment
PVR1V63 [4:0]: register for positive VSD63 fine tune adjustment

NVR3V1 [3:0]: register for negative VSD1 fine tune adjustment.
NVR3V8 [3:0]: register for negative VSD8 fine tune adjustment.
NVR3V20 [3:0]: register for negative VSD20 fine tune adjustment.
NVR3V43 [3:0]: register for negative VSD43 fine tune adjustment.
NVR3V62 [3:0]: register for negative VSD55 fine tune adjustment.
PRN0 [3:0]: register for negative VSD fine tune adjustment
PRN1 [3:0]: register for negative VSD fine tune adjustment
NVR1V0 [4:0]: register for negative VSD0 fine tune adjustment
NVR1V63 [4:0]: register for negative VSD63 fine tune adjustment

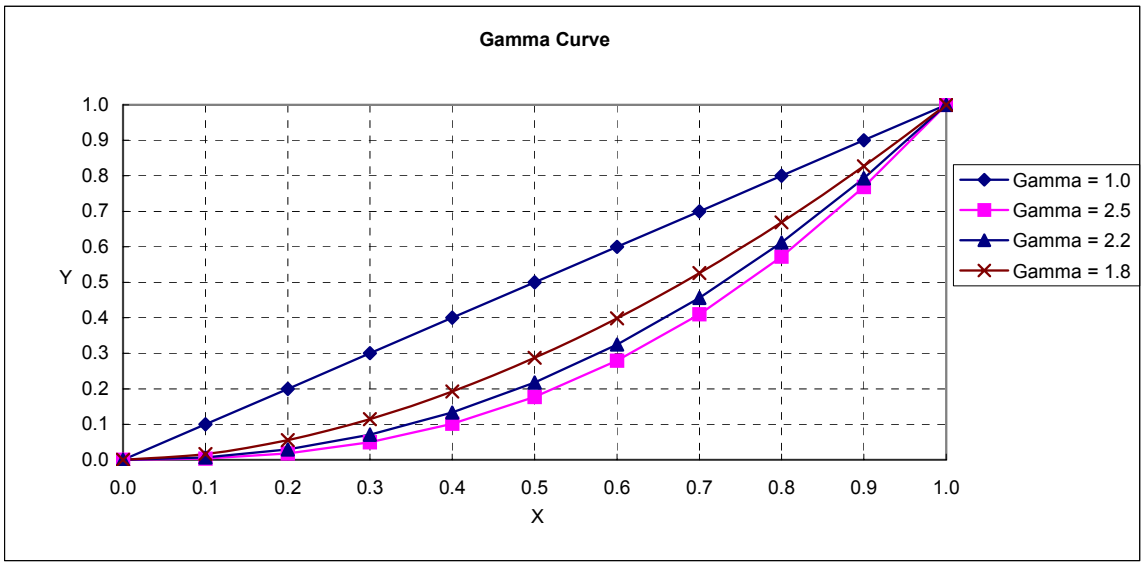
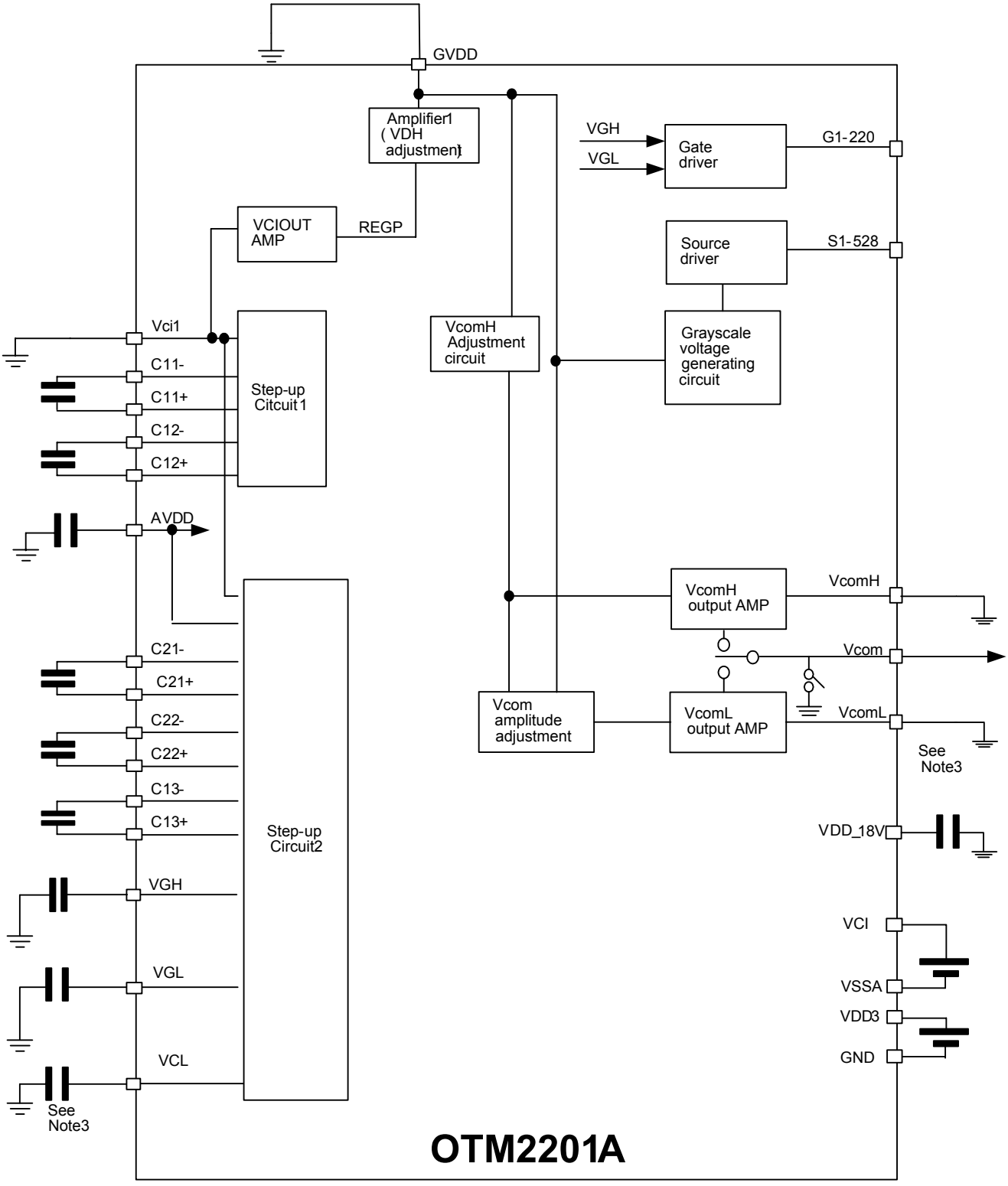


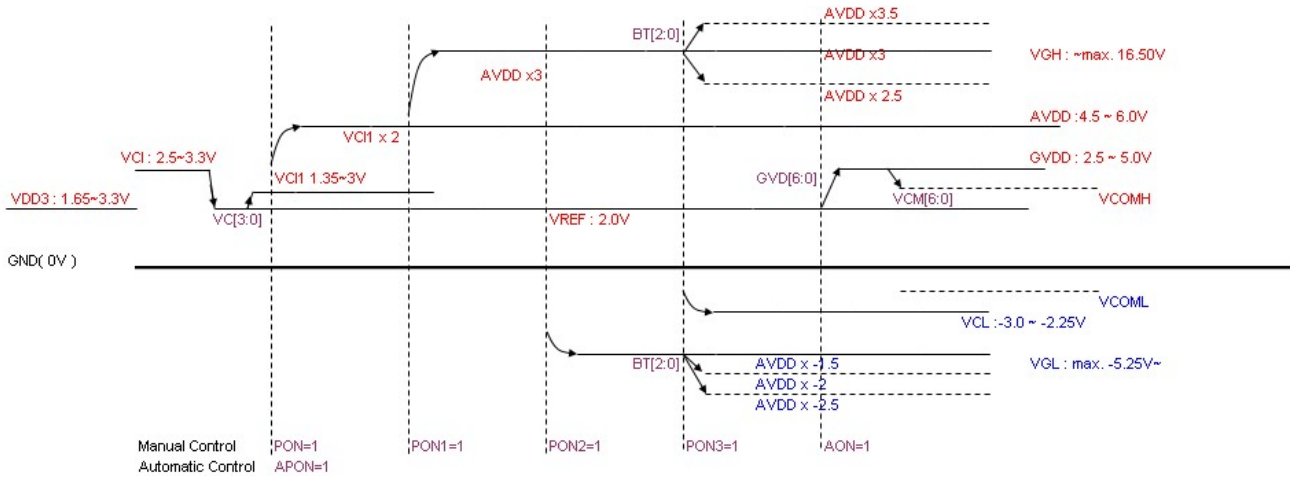
Figure 9-1 illustrated 4 different Gamma Curve.

10. Power Management System:

(a) Power supply circuit



(b) Voltage generation diagram



Note: 1. "VCI1=1.35V (VCI_EN) and 2.07V(PON1)" condition should be set only in the case of power-up Seq. , not a partical condition.

2. Set the conditions of VCI-VCI1 > 0.15V, AVDD > 0.3V and VCOML-VCL > 0.5V with loads because they differ depending on the display laod to be driven.

3. APON instruction is an automatic power-up Seq. operation switch. This operation takes more than 4.5 frame time.

4. VGH voltage should be set under 16.5V, regardless of the BT settings.

11. Electrical Characteristics:

11.1. Absolute Maximum Ratings:

Table 11-1

Item	Symbol	Value	Unit	Note
Power Supply Voltage1	VDD_18V	-0.3 ～+1.8	V	
Power Supply Voltage 2	VDD3	-0.3 ～+5.5	V	
Power Supply Voltage 3	VCI – VSS	-0.3 ～+5.5	V	
Power Supply Voltage 4	AVDD – VSS	-0.3 ～+6.5	V	
Power Supply Voltage 5	VSS – VCL	-0.3 ～+5.5	V	
Power Supply Voltage 6	VGH – VSS	-0.3 ～+22.0	V	
Power Supply Voltage 7	VSS – VGL	-0.3 ～+22.0	V	
Power Supply Voltage 8	VGH– VGL	-0.3 ～+33.0	V	
Input Voltage	Vt	-0.3 ～VDD3 + 0.3	V	
Operating Temperature	Topr	-40 ～+85	℃	
Storage Temperature	Tstg	-55 ～+110	℃	

11.2. DC Characteristics

Table 11-2 VCI= 2.50V～3.60V，VDD3=1.65V～ 3.60V，Ta=-40℃～+85℃

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input High level voltage	V_{IH}	V	VDD3=1.65V～3.60V	0.7xVDD3	-	VDD3	
Input Low level voltage	V_{IL}	V	VDD3=1.65V～3.60V	0	-	0.3xVDD3	
Output ”High” level voltage 1 (DB0-17)	V_{OH}	V	VDD3=1.65V～3.60V, I_{OH}=-0.5mA	0.8xVDD3	-	VDD3	
Output ”Low” level voltage 1 (DB0-17)	V_{OL}	V	VDD3=1.65V～3.60V, I_{OL}=0.5mA	0	-	0.2xVDD3	
I/O leak current	I_{LI}	μA	Vin=0/VDD3	-1	-	1	
Current Consumption (VDD3-IOGND)+(VCC-GND) Normal operation mode (262k-colors, display operation)	I_{OP1}	μA	fosc=453kHz (220line drive), VDD3=VCC=3.00V fFLM=70Hz Ta=25℃ RAM data: 18’h000000	-	TBD	-	
Current Consumption (VDD3-IOGND)+(VCC-GND) 8-color mode, 64-line, partial display operation	I_{op2}	μA	fosc=453kHz (64-line, partial display), VDD3=VCC=3.00V, fFLM=70Hz Ta=25℃ RAM data: 18h’000000	-	TBD	-	

11.3. AC Characteristics

VCI= 2.50V～3.60V，VDD3=1.65V～3.60V，Ta=-40℃～+85℃

11.3.1. Clock Characteristics

Table 11-3

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	kHz	VDD3 = VCC = 3.0V, 25°C	-	332	-	-

11.3.2. 80-System Bus Interface Timing Characteristics (18-/ 16- bit interface)

Table 11-4 Normal write operation (HWM=0 or 1), VDD3=1.65V~3.60V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW80	ns	100	-	-
	Read	tCYCR80	ns	500	-	-
Write low-level pulse width		tWLW80	ns	33	-	-
Read low-level pulse width		tWLR80	ns	250	-	-
Write high-level pulse width		tWHW80	ns	33	-	-
Read high-level pulse width		tWHR80	ns	250	-	-
Write/Read rise/ fall time		tR, tF	ns	-	-	15
Setup time Write (RS to CS*,WR*RD*)		tAS80	ns	10	-	-
Address Hold Time		tAH80	ns	2	-	-
CSB to WRB(RDB) time		tCW80	ns	15	-	-
Write data setup time		tWDS80	ns	20	-	-
Write data hold time		tWDH80	ns	10	-	-
Read data delay time		tRDD80	ns	-	-	200
Read data hold time		tRDH80	ns	10	-	-

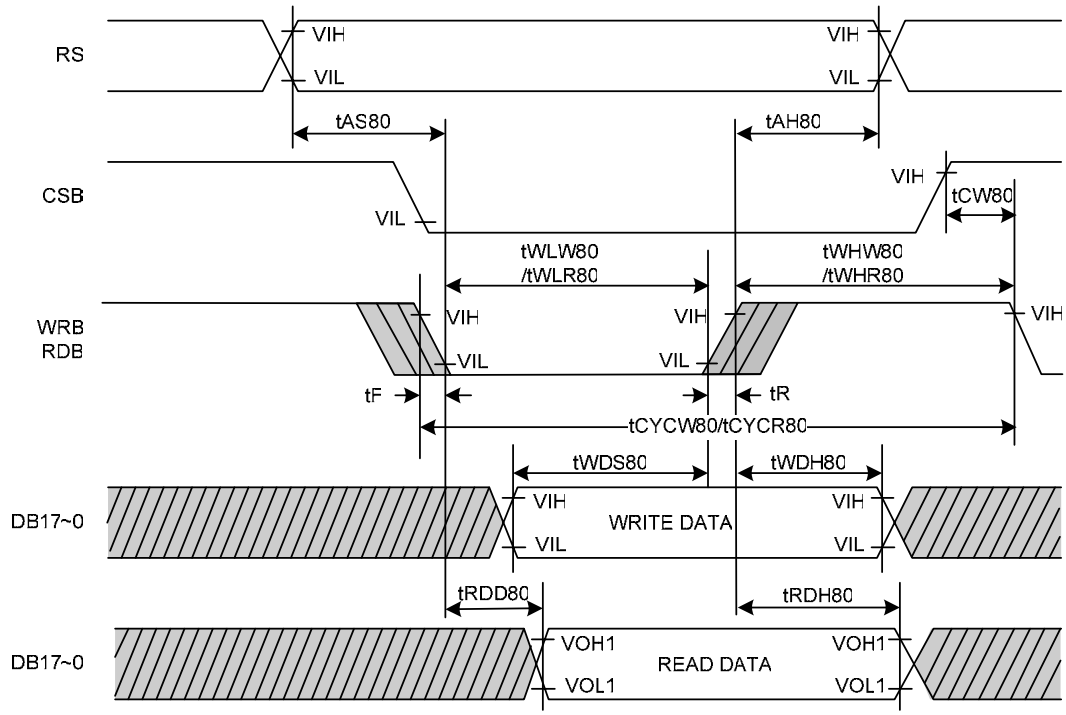


Figure 11-1 80-System Bus Interface

11.3.3. 68-System Bus Interface Timing Characteristics (18-/ 16- bit interface)

Table 11-5 Normal write operation (HWM=0 or 1), VDD3=1.65V~3.60V

Item	Symbol		Unit	Min.	Typ.	Max.
Bus cycle time	Write	tCYCW68	ns	100	-	-
	Read	tCYCR68	ns	500	-	-
Write low-level pulse width		tWLW68	ns	33	-	-
Read low-level pulse width		tWLR68	ns	250	-	-
Write high-level pulse width		tWHW68	ns	33	-	-
Read high-level pulse width		tWHR68	ns	250	-	-
Write/Read rise/ fall time		tR, tF	ns	-	-	15
Setup time Write (RS to CS*,WR*RD*)		tAS68	ns	10	-	-
Address Hold Time		tAH68	ns	2	-	-
CSB to WRB(RDB) time		tCW68	ns	15	-	-
Write data setup time		tWDS68	ns	20	-	-
Write data hold time		tWDH68	ns	10	-	-
Read data delay time		tRDD68	ns	-	-	200
Read data hold time		tRDH68	ns	10	-	-

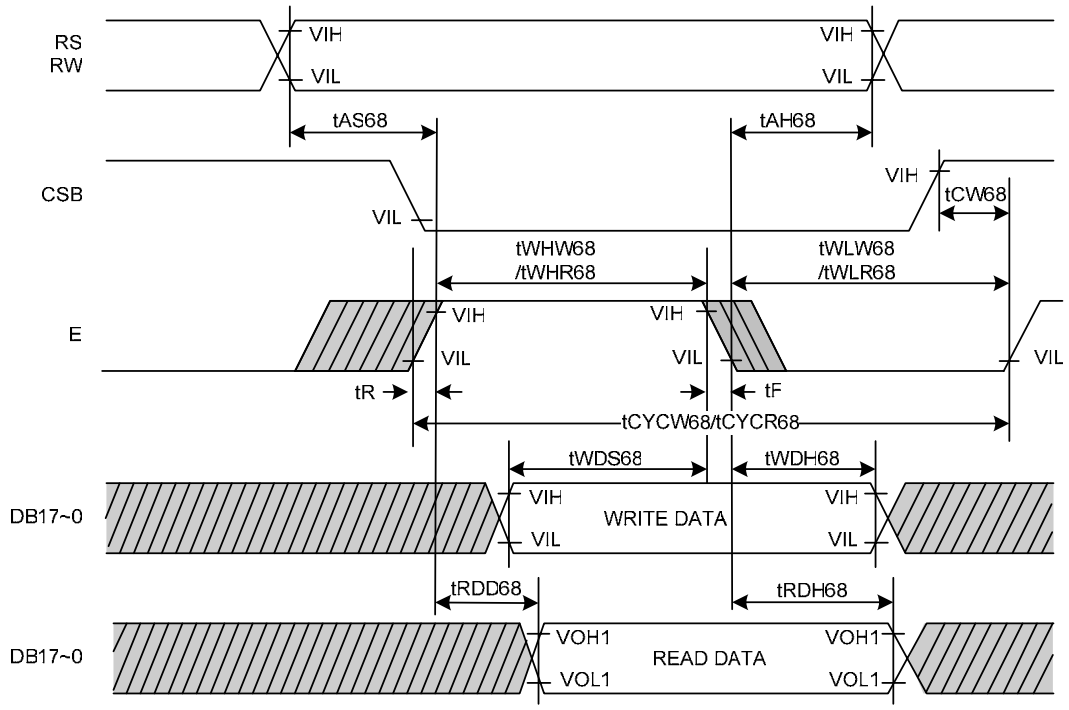


Figure 11-2 68-System Bus Interface

11.3.4. Clock-synchronized Serial Interface Timing Characteristics

VDD3=1.65~3.60V

Table 11-6

Item	Symbol		Unit	Min.	Typ.	Max.
Serial Time Clock Cycle	Write (received)	tSCYC	ns	130	-	-
	Read (transmitted)	tSCYC	ns	250	-	20.000
Serial Clock high-level width	Write (received)	tSCHW	ns	50	-	-
	Read (transmitted)	tSCHR	ns	110	-	-
Serial Clock low-level width	Write (received)	tSCLW	ns	50	-	-
	Read (transmitted)	tSCLR	ns	110	-	-
Serial clock rise/fall time		tR, tF	ns	-	-	15
Chip select setup time		tCSS	ns	20	-	-
Chip select hold time		tCSH	ns	60	-	-
Serial input data setup time		tSIDS	ns	30	-	-
Serial input data hold time		tSIDH	ns	30	-	-
Serial output data delay time		tSODD	ns	-	-	130
Serial output data hold time		tSODH	ns	5	-	-

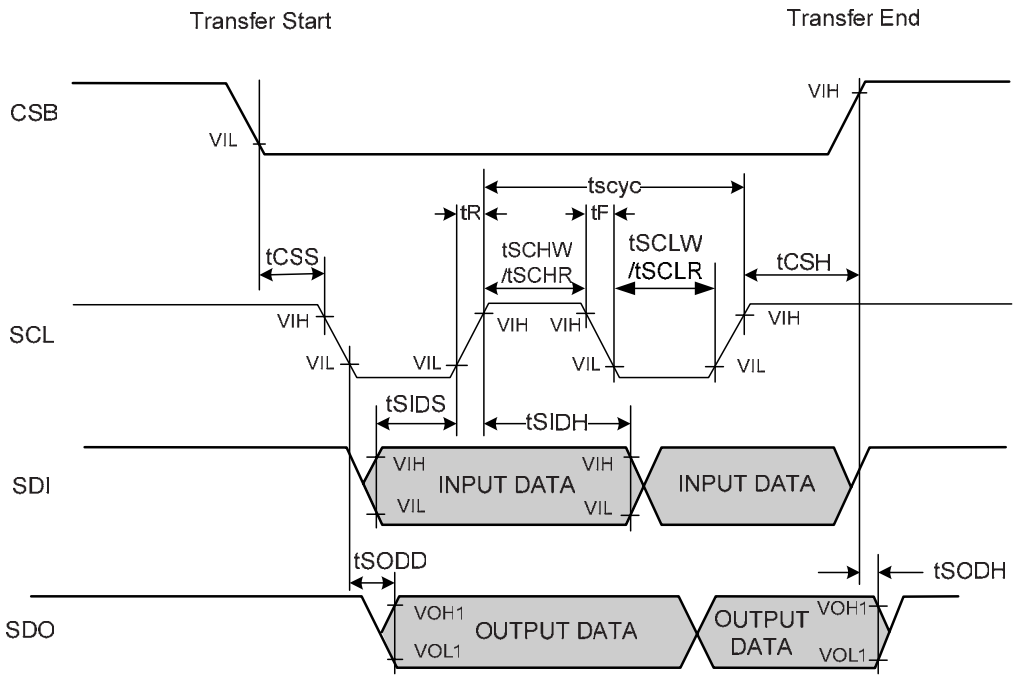


Figure 11-3 SPI mode

11.3.5. Reset Timing Characteristics (VDD3=1.65~3.60V)

Table 11-7

Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	ms	1	—	—

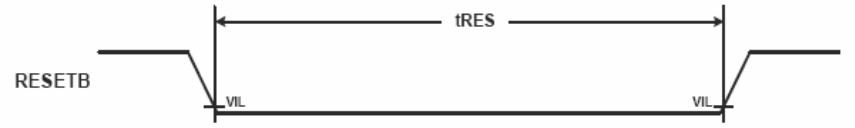


Figure 11-4 Reset Timing

11.3.6. RGB Interface Timing Characteristics

18-/ 16-/6- bit RGB interface, VDD3=1.65~3.60V

Table 11-8

Item	Symbol	Unit	Min.	Typ.	Max.
VSYNC/HSYNC Setup time	tvsys/thsys	ns	30	-	0
ENABLE Setup time	tENS	ns	30	-	-
ENABLE Hold time	tENH	ns	20	-	-
DOTCLK low-level pulse width	tDCLW	ns	40	-	-
DOTCLK high-level pulse width	tDCHW	ns	40	-	-
DOTCLK cycle time	tCYCD	ns	100	-	-
Data setup time	tPDS	ns	30	-	-
Data hold time	tPDH	ns	20	-	-
DOTCLK, VSYNC and HSYNC rise/fall time	tR, tF	ns	-	-	15

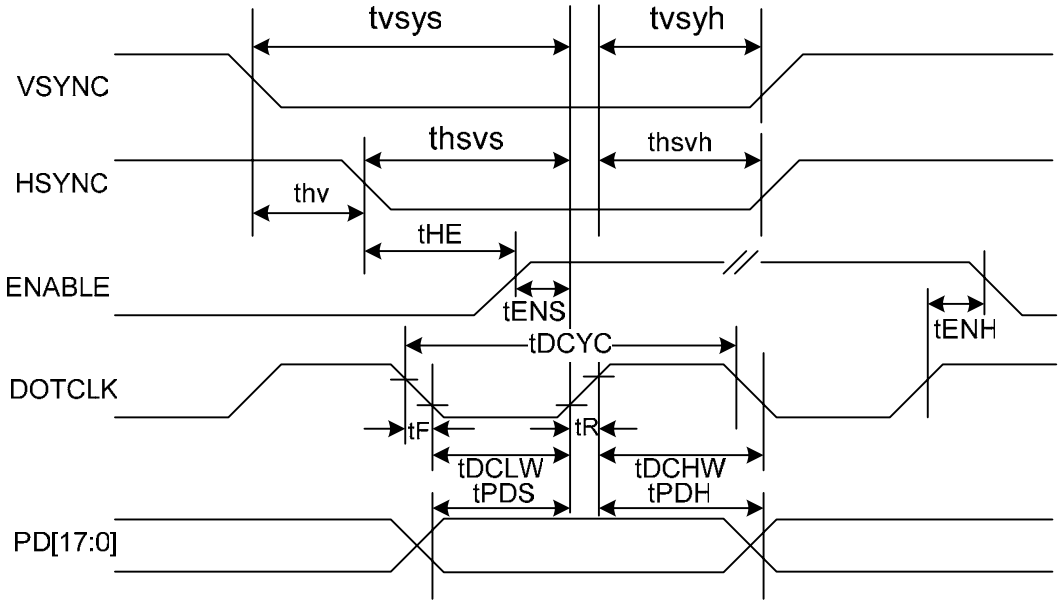
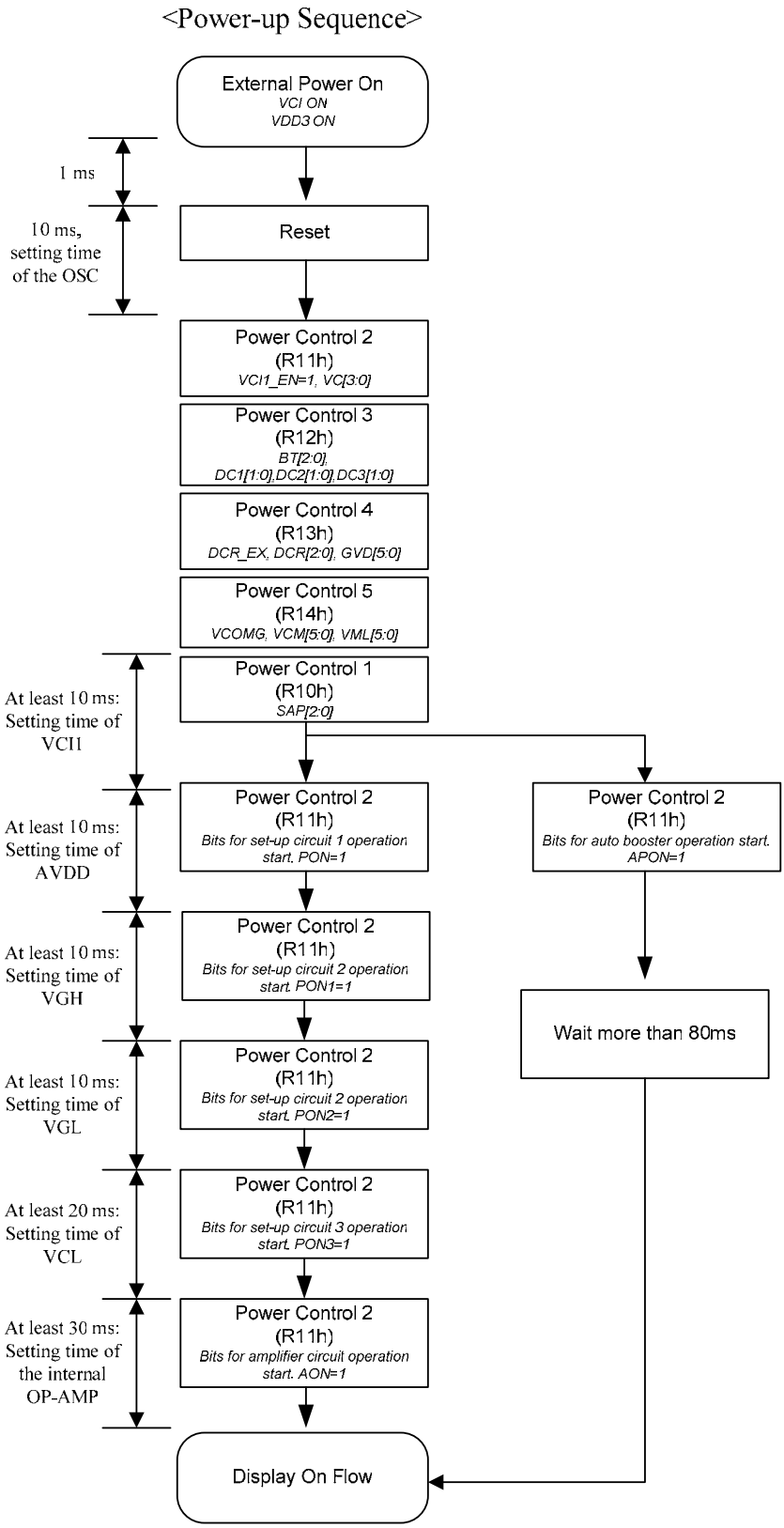


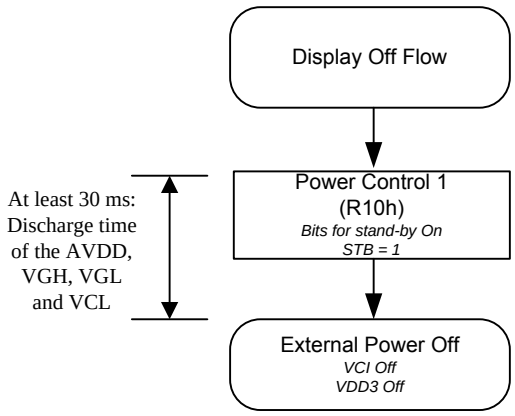
Figure 11-5 RGB Interface

12. Power on/off sequence

12.1. Power on / off sequence

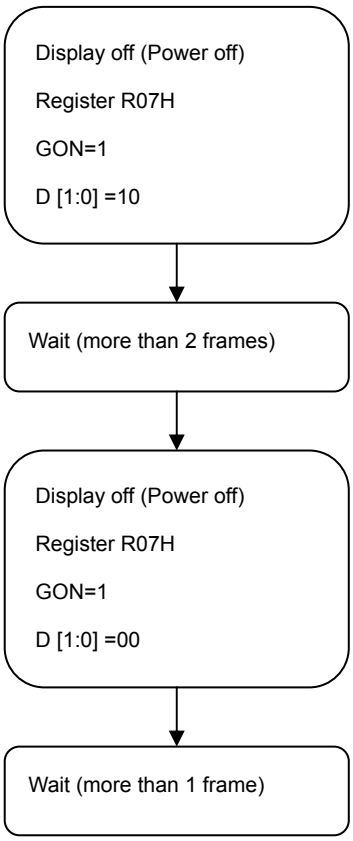


<Power-down Sequence>

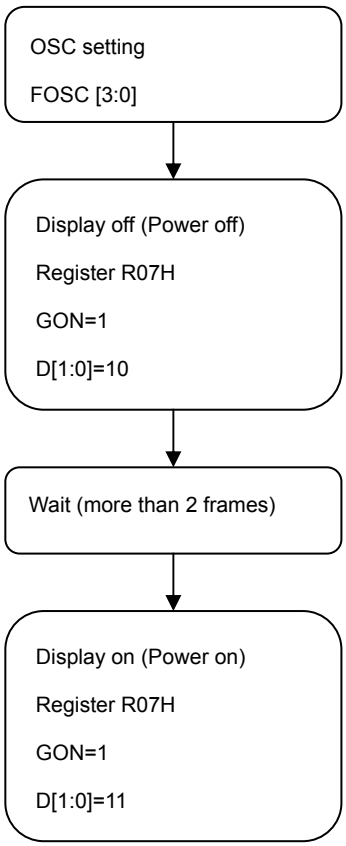


12.2. Display on / off sequence

Display off flow (Power off flow)

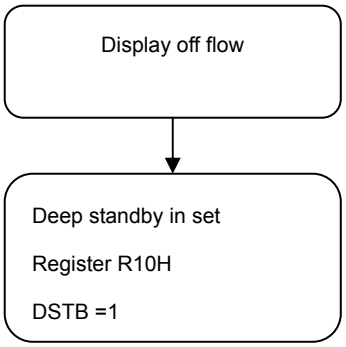


Display on flow (Power on flow)

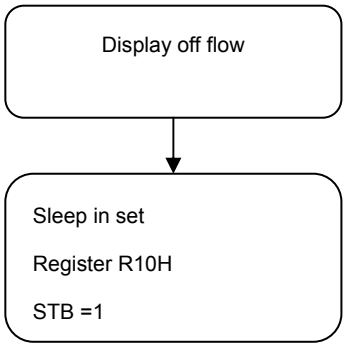


12.3. Deep standby and sleep mode in / out sequence

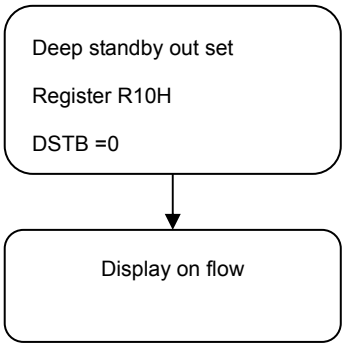
Deep standby in flow



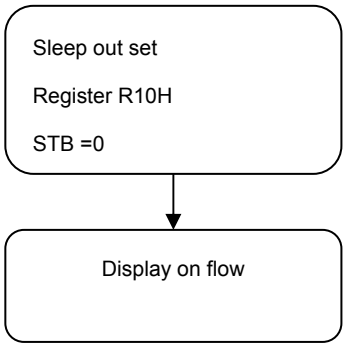
Sleep in flow



Deep standby out flow

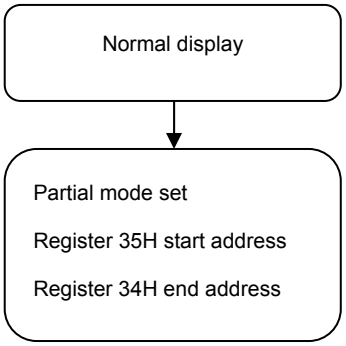


Sleep out flow

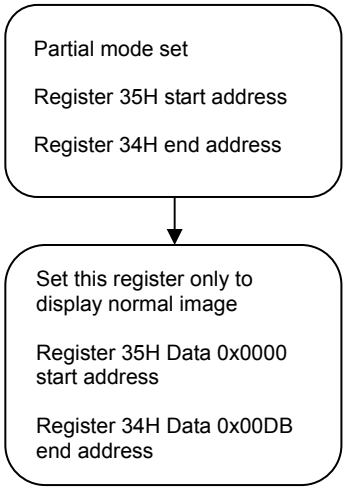


13.3. Partial mode on / off

Normal display => Partial mode

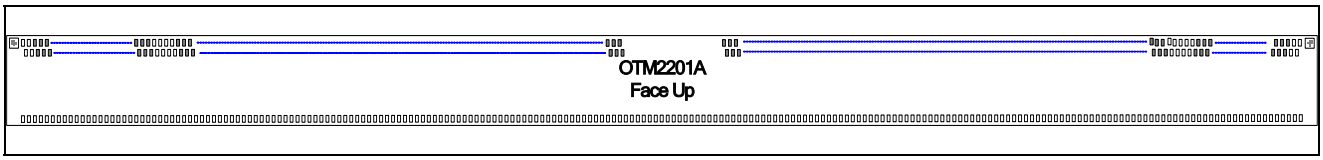


Partial mode => Normal display



13. CHIP INFORMATION

13.1. PAD Assignment



13.2. Pad Dimensions

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	13,880	670	μm
Chip thickness	-	400 ± 20		
Pad pitch	1-215	65/85	-	
	216-988	16	-	
Pad size	1-215	40	46	
	216-988	15	87	

Note1: Chip size included scribe line.

13.3. PAD Locations

PAD NO.	PAD Name	X	Y
1	DUMMY1	-6695	-265
2	DUMMY2	-6635	-265
3	VCOM	-6575	-265
4	VCOM	-6515	-265
5	VCOM	-6455	-265
6	VCOM	-6395	-265
7	DUMMY3	-6335	-265
8	VGH	-6275	-265
9	VGH	-6215	-265
10	VGH	-6155	-265
11	VGH	-6095	-265
12	VGH	-6035	-265
13	DUMMY4	-5975	-265
14	VGL	-5915	-265
15	VGL	-5855	-265
16	VGL	-5795	-265
17	VGL	-5735	-265
18	VGL	-5675	-265
19	DUMMY5	-5615	-265
20	C22P	-5555	-265
21	C22P	-5495	-265
22	C22P	-5435	-265
23	C22N	-5375	-265
24	C22N	-5315	-265
25	C22N	-5255	-265
26	C21P	-5195	-265
27	C21P	-5135	-265
28	C21P	-5075	-265
29	C21N	-5015	-265
30	C21N	-4955	-265
31	C21N	-4895	-265
32	DUMMY6	-4835	-265
33	DUMMY7	-4775	-265
34	VSS	-4715	-265
35	VSS	-4655	-265
36	VSS	-4595	-265
37	VSS	-4535	-265
38	VSS	-4475	-265
39	VSS	-4415	-265
40	VSS	-4355	-265
41	VSS	-4295	-265
42	VSS	-4235	-265
43	VSS	-4175	-265
44	VCI1	-4115	-265
45	VCI1	-4055	-265
46	VCI1	-3995	-265
47	VCI1	-3935	-265
48	VCI1	-3875	-265
49	VCI1	-3815	-265
50	C11P	-3755	-265
51	C11P	-3695	-265
52	C11P	-3635	-265
53	C11P	-3575	-265
54	C11P	-3515	-265
55	C11P	-3455	-265
56	C11P	-3395	-265
57	C11P	-3335	-265
58	C11N	-3275	-265
59	C11N	-3215	-265
60	C11N	-3155	-265
61	C11N	-3095	-265
62	C11N	-3035	-265
63	C11N	-2975	-265
64	C11N	-2915	-265
65	C11N	-2855	-265
66	C12P	-2795	-265
67	C12P	-2735	-265
68	C12P	-2675	-265
69	C12P	-2615	-265
70	C12P	-2555	-265
71	C12P	-2495	-265
72	C12N	-2435	-265
73	C12N	-2375	-265
74	C12N	-2315	-265
75	C12N	-2255	-265
76	C12N	-2195	-265
77	C12N	-2135	-265
78	C13P	-2075	-265
79	C13P	-2015	-265
80	C13P	-1955	-265
81	C13P	-1895	-265
82	C13P	-1835	-265
83	C13N	-1775	-265
84	C13N	-1715	-265
85	C13N	-1655	-265
86	C13N	-1595	-265
87	C13N	-1535	-265
88	AVDD	-1475	-265
89	AVDD	-1415	-265
90	AVDD	-1355	-265
91	AVDD	-1295	-265
92	AVDD	-1235	-265
93	AVDD	-1175	-265
94	AVDD	-1115	-265
95	AVDD	-1055	-265
96	VCI	-995	-265
97	VCI	-935	-265
98	VCI	-875	-265
99	VCI	-815	-265
100	VCI	-755	-265
101	VCI	-695	-265
102	VCI	-635	-265
103	VCI	-575	-265
104	VCI	-515	-265
105	VCI	-455	-265
106	VCL	-395	-265
107	VCL	-335	-265
108	VCL	-275	-265
109	VCL	-215	-265
110	VCL	-155	-265
111	DUMMY8	-95	-265
112	RS	-35	-265
113	CSB	25	-265
114	VSYNC	85	-265
115	HSYNC	145	-265
116	DOTCLK	205	-265
117	ENABLE	265	-265
118	RESETB	325	-265
119	SDI	385	-265
120	E_RDB	445	-265
121	RW_WRB	505	-265
122	DB17	565	-265
123	DB16	650	-265
124	DB15	735	-265
125	DB14	820	-265
126	DB13	905	-265
127	DB12	990	-265
128	DB11	1075	-265
129	DB10	1160	-265
130	DB9	1245	-265
131	DB8	1330	-265
132	DB7	1415	-265
133	DB6	1500	-265
134	DB5	1585	-265
135	DB4	1670	-265
136	DB3	1755	-265
137	DB2	1840	-265
138	DB1	1925	-265
139	DB0	2010	-265
140	IM3	2095	-265
141	IM2	2155	-265
142	IM1	2215	-265
143	IM0	2275	-265
144	SDO	2335	-265
145	TESTO1	2420	-265
146	FLM	2505	-265
147	TEST0	2590	-265
148	TEST1	2675	-265
149	TEST2	2735	-265
150	TEST3	2795	-265
151	TEST4	2855	-265
152	TEST5	2915	-265
153	TEST6	2975	-265
154	TEST7	3035	-265
155	EN_EXCLK	3095	-265
156	EXCLK	3155	-265

PAD NO.	PAD Name	X	Y
157	VSSA	3215	-265
158	VSSA	3275	-265
159	VSSA	3335	-265
160	VSSA	3395	-265
161	VSSA	3455	-265
162	VSSA	3515	-265
163	VSSA	3575	-265
164	VSSA	3635	-265
165	VSSA	3695	-265
166	VSS	3755	-265
167	VSS	3815	-265
168	VSS	3875	-265
169	VSS	3935	-265
170	VSS	3995	-265
171	VSS	4055	-265
172	VSS	4115	-265
173	VSS	4175	-265
174	VSS	4235	-265
175	VSS	4295	-265
176	VGS	4355	-265
177	VGS	4415	-265
178	VDD_18V	4475	-265
179	VDD_18V	4535	-265
180	VDD_18V	4595	-265
181	VDD_18V	4655	-265
182	VDD_18V	4715	-265
183	VDD_18V	4775	-265
184	VDD_18V	4835	-265
185	VDD_18V	4895	-265
186	VDD_18V	4955	-265
187	VDD_18V	5015	-265
188	VDD_18V	5075	-265
189	VDD_18V	5135	-265
190	VDD3	5195	-265
191	VDD3	5255	-265
192	VDD3	5315	-265
193	VDD3	5375	-265
194	VDD3	5435	-265
195	VDD3	5495	-265
196	DUMMY9	5555	-265
197	VREF	5615	-265
198	GVDD	5675	-265
199	GVDD	5735	-265
200	GVDD	5795	-265
201	GVDD	5855	-265
202	VCOMH	5915	-265
203	VCOMH	5975	-265
204	VCOML	6035	-265
205	VCOML	6095	-265
206	VCOMR	6155	-265
207	DUMMY10	6215	-265
208	DUMMY10	6275	-265
209	DUMMY10	6335	-265

PAD NO.	PAD Name	X	Y
210	VCOM	6395	-265
211	VCOM	6455	-265
212	VCOM	6515	-265
213	VCOM	6575	-265
214	DUMMY11	6635	-265
215	DUMMY12	6695	-265
216	DUMMY13	6772	237
217	DUMMY14	6756	84
218	DUMMY15	6740	237
219	DUMMY16	6724	84
220	G2	6708	237
221	G4	6692	84
222	G6	6676	237
223	G8	6660	84
224	G10	6644	237
225	G12	6628	84
226	G14	6612	237
227	G16	6596	84
228	G18	6580	237
229	G20	6564	84
230	G22	6548	237
231	G24	6532	84
232	G26	6516	237
233	G28	6500	84
234	G30	6484	237
235	G32	6468	84
236	G34	6452	237
237	G36	6436	84
238	G38	6420	237
239	G40	6404	84
240	G42	6388	237
241	G44	6372	84
242	G46	6356	237
243	G48	6340	84
244	G50	6324	237
245	G52	6308	84
246	G54	6292	237
247	G56	6276	84
248	G58	6260	237
249	G60	6244	84
250	G62	6228	237
251	G64	6212	84
252	G66	6196	237
253	G68	6180	84
254	G70	6164	237
255	G72	6148	84
256	G74	6132	237
257	G76	6116	84
258	G78	6100	237
259	G80	6084	84
260	G82	6068	237
261	G84	6052	84
262	G86	6036	237

PAD NO.	PAD Name	X	Y
263	G88	6020	84
264	G90	6004	237
265	G92	5988	84
266	G94	5972	237
267	G96	5956	84
268	G98	5940	237
269	G100	5924	84
270	G102	5908	237
271	G104	5892	84
272	G106	5876	237
273	G108	5860	84
274	G110	5844	237
275	G112	5828	84
276	G114	5812	237
277	G116	5796	84
278	G118	5780	237
279	G120	5764	84
280	G122	5748	237
281	G124	5732	84
282	G126	5716	237
283	G128	5700	84
284	G130	5684	237
285	G132	5668	84
286	G134	5652	237
287	G136	5636	84
288	G138	5620	237
289	G140	5604	84
290	G142	5588	237
291	G144	5572	84
292	G146	5556	237
293	G148	5540	84
294	G150	5524	237
295	G152	5508	84
296	G154	5492	237
297	G156	5476	84
298	G158	5460	237
299	G160	5444	84
300	G162	5428	237
301	G164	5412	84
302	G166	5396	237
303	G168	5380	84
304	G170	5364	237
305	G172	5348	84
306	G174	5332	237
307	G176	5316	84
308	G178	5300	237
309	G180	5284	84
310	G182	5268	237
311	G184	5252	84
312	G186	5236	237
313	G188	5220	84
314	G190	5204	237
315	G192	5188	84

PAD NO.	PAD Name	X	Y
316	G194	5172	237
317	G196	5156	84
318	G198	5140	237
319	G200	5124	84
320	G202	5108	237
321	G204	5092	84
322	G206	5076	237
323	G208	5060	84
324	G210	5044	237
325	G212	5028	84
326	G214	5012	237
327	G216	4996	84
328	G218	4980	237
329	G220	4964	84
330	DUMMY17	4948	237
331	DUMMY18	4932	84
332	DUMMY19	4916	237
333	DUMMY20	4900	84
334	DUMMY21	4884	237
335	DUMMY22	4868	84
336	DUMMY23	4852	237
337	DUMMY24	4836	84
338	DUMMY25	4820	237
339	S528	4804	84
340	S527	4788	237
341	S526	4772	84
342	S525	4756	237
343	S524	4740	84
344	S523	4724	237
345	S522	4708	84
346	S521	4692	237
347	S520	4676	84
348	S519	4660	237
349	S518	4644	84
350	S517	4628	237
351	S516	4612	84
352	S515	4596	237
353	S514	4580	84
354	S513	4564	237
355	S512	4548	84
356	S511	4532	237
357	S510	4516	84
358	S509	4500	237
359	S508	4484	84
360	S507	4468	237
361	S506	4452	84
362	S505	4436	237
363	S504	4420	84
364	S503	4404	237
365	S502	4388	84
366	S501	4372	237
367	S500	4356	84
368	S499	4340	237

PAD NO.	PAD Name	X	Y
369	S498	4324	84
370	S497	4308	237
371	S496	4292	84
372	S495	4276	237
373	S494	4260	84
374	S493	4244	237
375	S492	4228	84
376	S491	4212	237
377	S490	4196	84
378	S489	4180	237
379	S488	4164	84
380	S487	4148	237
381	S486	4132	84
382	S485	4116	237
383	S484	4100	84
384	S483	4084	237
385	S482	4068	84
386	S481	4052	237
387	S480	4036	84
388	S479	4020	237
389	S478	4004	84
390	S477	3988	237
391	S476	3972	84
392	S475	3956	237
393	S474	3940	84
394	S473	3924	237
395	S472	3908	84
396	S471	3892	237
397	S470	3876	84
398	S469	3860	237
399	S468	3844	84
400	S467	3828	237
401	S466	3812	84
402	S465	3796	237
403	S464	3780	84
404	S463	3764	237
405	S462	3748	84
406	S461	3732	237
407	S460	3716	84
408	S459	3700	237
409	S458	3684	84
410	S457	3668	237
411	S456	3652	84
412	S455	3636	237
413	S454	3620	84
414	S453	3604	237
415	S452	3588	84
416	S451	3572	237
417	S450	3556	84
418	S449	3540	237
419	S448	3524	84
420	S447	3508	237
421	S446	3492	84

PAD NO.	PAD Name	X	Y
422	S445	3476	237
423	S444	3460	84
424	S443	3444	237
425	S442	3428	84
426	S441	3412	237
427	S440	3396	84
428	S439	3380	237
429	S438	3364	84
430	S437	3348	237
431	S436	3332	84
432	S435	3316	237
433	S434	3300	84
434	S433	3284	237
435	S432	3268	84
436	S431	3252	237
437	S430	3236	84
438	S429	3220	237
439	S428	3204	84
440	S427	3188	237
441	S426	3172	84
442	S425	3156	237
443	S424	3140	84
444	S423	3124	237
445	S422	3108	84
446	S421	3092	237
447	S420	3076	84
448	S419	3060	237
449	S418	3044	84
450	S417	3028	237
451	S416	3012	84
452	S415	2996	237
453	S414	2980	84
454	S413	2964	237
455	S412	2948	84
456	S411	2932	237
457	S410	2916	84
458	S409	2900	237
459	S408	2884	84
460	S407	2868	237
461	S406	2852	84
462	S405	2836	237
463	S404	2820	84
464	S403	2804	237
465	S402	2788	84
466	S401	2772	237
467	S400	2756	84
468	S399	2740	237
469	S398	2724	84
470	S397	2708	237
471	S396	2642	84
472	S395	2626	237
473	S394	2610	84
474	S393	2594	237

PAD NO.	PAD Name	X	Y
475	S392	2578	84
476	S391	2562	237
477	S390	2546	84
478	S389	2530	237
479	S388	2514	84
480	S387	2498	237
481	S386	2482	84
482	S385	2466	237
483	S384	2450	84
484	S383	2434	237
485	S382	2418	84
486	S381	2402	237
487	S380	2386	84
488	S379	2370	237
489	S378	2354	84
490	S377	2338	237
491	S376	2322	84
492	S375	2306	237
493	S374	2290	84
494	S373	2274	237
495	S372	2258	84
496	S371	2242	237
497	S370	2226	84
498	S369	2210	237
499	S368	2194	84
500	S367	2178	237
501	S366	2162	84
502	S365	2146	237
503	S364	2130	84
504	S363	2114	237
505	S362	2098	84
506	S361	2082	237
507	S360	2066	84
508	S359	2050	237
509	S358	2034	84
510	S357	2018	237
511	S356	2002	84
512	S355	1986	237
513	S354	1970	84
514	S353	1954	237
515	S352	1938	84
516	S351	1922	237
517	S350	1906	84
518	S349	1890	237
519	S348	1874	84
520	S347	1858	237
521	S346	1842	84
522	S345	1826	237
523	S344	1810	84
524	S343	1794	237
525	S342	1778	84
526	S341	1762	237
527	S340	1746	84

PAD NO.	PAD Name	X	Y
528	S339	1730	237
529	S338	1714	84
530	S337	1698	237
531	S336	1682	84
532	S335	1666	237
533	S334	1650	84
534	S333	1634	237
535	S332	1618	84
536	S331	1602	237
537	S330	1586	84
538	S329	1570	237
539	S328	1554	84
540	S327	1538	237
541	S326	1522	84
542	S325	1506	237
543	S324	1490	84
544	S323	1474	237
545	S322	1458	84
546	S321	1442	237
547	S320	1426	84
548	S319	1410	237
549	S318	1394	84
550	S317	1378	237
551	S316	1362	84
552	S315	1346	237
553	S314	1330	84
554	S313	1314	237
555	S312	1298	84
556	S311	1282	237
557	S310	1266	84
558	S309	1250	237
559	S308	1234	84
560	S307	1218	237
561	S306	1202	84
562	S305	1186	237
563	S304	1170	84
564	S303	1154	237
565	S302	1138	84
566	S301	1122	237
567	S300	1106	84
568	S299	1090	237
569	S298	1074	84
570	S297	1058	237
571	S296	1042	84
572	S295	1026	237
573	S294	1010	84
574	S293	994	237
575	S292	978	84
576	S291	962	237
577	S290	946	84
578	S289	930	237
579	S288	914	84
580	S287	898	237

PAD NO.	PAD Name	X	Y
581	S286	882	84
582	S285	866	237
583	S284	850	84
584	S283	834	237
585	S282	818	84
586	S281	802	237
587	S280	786	84
588	S279	770	237
589	S278	754	84
590	S277	738	237
591	S276	722	84
592	S275	706	237
593	S274	690	84
594	S273	674	237
595	S272	658	84
596	S271	642	237
597	S270	626	84
598	S269	610	237
599	S268	594	84
600	S267	578	237
601	S266	562	84
602	S265	546	237
603	S264	-554	84
604	S263	-570	237
605	S262	-586	84
606	S261	-602	237
607	S260	-618	84
608	S259	-634	237
609	S258	-650	84
610	S257	-666	237
611	S256	-682	84
612	S255	-698	237
613	S254	-714	84
614	S253	-730	237
615	S252	-746	84
616	S251	-762	237
617	S250	-778	84
618	S249	-794	237
619	S248	-810	84
620	S247	-826	237
621	S246	-842	84
622	S245	-858	237
623	S244	-874	84
624	S243	-890	237
625	S242	-906	84
626	S241	-922	237
627	S240	-938	84
628	S239	-954	237
629	S238	-970	84
630	S237	-986	237
631	S236	-1002	84
632	S235	-1018	237
633	S234	-1034	84

PAD NO.	PAD Name	X	Y
634	S233	-1050	237
635	S232	-1066	84
636	S231	-1082	237
637	S230	-1098	84
638	S229	-1114	237
639	S228	-1130	84
640	S227	-1146	237
641	S226	-1162	84
642	S225	-1178	237
643	S224	-1194	84
644	S223	-1210	237
645	S222	-1226	84
646	S221	-1242	237
647	S220	-1258	84
648	S219	-1274	237
649	S218	-1290	84
650	S217	-1306	237
651	S216	-1322	84
652	S215	-1338	237
653	S214	-1354	84
654	S213	-1370	237
655	S212	-1386	84
656	S211	-1402	237
657	S210	-1418	84
658	S209	-1434	237
659	S208	-1450	84
660	S207	-1466	237
661	S206	-1482	84
662	S205	-1498	237
663	S204	-1514	84
664	S203	-1530	237
665	S202	-1546	84
666	S201	-1562	237
667	S200	-1578	84
668	S199	-1594	237
669	S198	-1610	84
670	S197	-1626	237
671	S196	-1642	84
672	S195	-1658	237
673	S194	-1674	84
674	S193	-1690	237
675	S192	-1706	84
676	S191	-1722	237
677	S190	-1738	84
678	S189	-1754	237
679	S188	-1770	84
680	S187	-1786	237
681	S186	-1802	84
682	S185	-1818	237
683	S184	-1834	84
684	S183	-1850	237
685	S182	-1866	84
686	S181	-1882	237

PAD NO.	PAD Name	X	Y
687	S180	-1898	84
688	S179	-1914	237
689	S178	-1930	84
690	S177	-1946	237
691	S176	-1962	84
692	S175	-1978	237
693	S174	-1994	84
694	S173	-2010	237
695	S172	-2026	84
696	S171	-2042	237
697	S170	-2058	84
698	S169	-2074	237
699	S168	-2090	84
700	S167	-2106	237
701	S166	-2122	84
702	S165	-2138	237
703	S164	-2154	84
704	S163	-2170	237
705	S162	-2186	84
706	S161	-2202	237
707	S160	-2218	84
708	S159	-2234	237
709	S158	-2250	84
710	S157	-2266	237
711	S156	-2282	84
712	S155	-2298	237
713	S154	-2314	84
714	S153	-2330	237
715	S152	-2346	84
716	S151	-2362	237
717	S150	-2378	84
718	S149	-2394	237
719	S148	-2410	84
720	S147	-2426	237
721	S146	-2442	84
722	S145	-2458	237
723	S144	-2474	84
724	S143	-2490	237
725	S142	-2506	84
726	S141	-2522	237
727	S140	-2538	84
728	S139	-2554	237
729	S138	-2570	84
730	S137	-2586	237
731	S136	-2602	84
732	S135	-2618	237
733	S134	-2634	84
734	S133	-2650	237
735	S132	-2716	84
736	S131	-2732	237
737	S130	-2748	84
738	S129	-2764	237
739	S128	-2780	84

PAD NO.	PAD Name	X	Y
740	S127	-2796	237
741	S126	-2812	84
742	S125	-2828	237
743	S124	-2844	84
744	S123	-2860	237
745	S122	-2876	84
746	S121	-2892	237
747	S120	-2908	84
748	S119	-2924	237
749	S118	-2940	84
750	S117	-2956	237
751	S116	-2972	84
752	S115	-2988	237
753	S114	-3004	84
754	S113	-3020	237
755	S112	-3036	84
756	S111	-3052	237
757	S110	-3068	84
758	S109	-3084	237
759	S108	-3100	84
760	S107	-3116	237
761	S106	-3132	84
762	S105	-3148	237
763	S104	-3164	84
764	S103	-3180	237
765	S102	-3196	84
766	S101	-3212	237
767	S100	-3228	84
768	S99	-3244	237
769	S98	-3260	84
770	S97	-3276	237
771	S96	-3292	84
772	S95	-3308	237
773	S94	-3324	84
774	S93	-3340	237
775	S92	-3356	84
776	S91	-3372	237
777	S90	-3388	84
778	S89	-3404	237
779	S88	-3420	84
780	S87	-3436	237
781	S86	-3452	84
782	S85	-3468	237
783	S84	-3484	84
784	S83	-3500	237
785	S82	-3516	84
786	S81	-3532	237
787	S80	-3548	84
788	S79	-3564	237
789	S78	-3580	84
790	S77	-3596	237
791	S76	-3612	84
792	S75	-3628	237

PAD NO.	PAD Name	X	Y
793	S74	-3644	84
794	S73	-3660	237
795	S72	-3676	84
796	S71	-3692	237
797	S70	-3708	84
798	S69	-3724	237
799	S68	-3740	84
800	S67	-3756	237
801	S66	-3772	84
802	S65	-3788	237
803	S64	-3804	84
804	S63	-3820	237
805	S62	-3836	84
806	S61	-3852	237
807	S60	-3868	84
808	S59	-3884	237
809	S58	-3900	84
810	S57	-3916	237
811	S56	-3932	84
812	S55	-3948	237
813	S54	-3964	84
814	S53	-3980	237
815	S52	-3996	84
816	S51	-4012	237
817	S50	-4028	84
818	S49	-4044	237
819	S48	-4060	84
820	S47	-4076	237
821	S46	-4092	84
822	S45	-4108	237
823	S44	-4124	84
824	S43	-4140	237
825	S42	-4156	84
826	S41	-4172	237
827	S40	-4188	84
828	S39	-4204	237
829	S38	-4220	84
830	S37	-4236	237
831	S36	-4252	84
832	S35	-4268	237
833	S34	-4284	84
834	S33	-4300	237
835	S32	-4316	84
836	S31	-4332	237
837	S30	-4348	84
838	S29	-4364	237
839	S28	-4380	84
840	S27	-4396	237
841	S26	-4412	84
842	S25	-4428	237
843	S24	-4444	84
844	S23	-4460	237
845	S22	-4476	84

PAD NO.	PAD Name	X	Y
846	S21	-4492	237
847	S20	-4508	84
848	S19	-4524	237
849	S18	-4540	84
850	S17	-4556	237
851	S16	-4572	84
852	S15	-4588	237
853	S14	-4604	84
854	S13	-4620	237
855	S12	-4636	84
856	S11	-4652	237
857	S10	-4668	84
858	S9	-4684	237
859	S8	-4700	84
860	S7	-4716	237
861	S6	-4732	84
862	S5	-4748	237
863	S4	-4764	84
864	S3	-4780	237
865	S2	-4796	84
866	S1	-4812	237
867	DUMMY26	-4828	84
868	DUMMY27	-4844	237
869	DUMMY28	-4860	84
870	DUMMY29	-4876	237
871	DUMMY30	-4892	84
872	DUMMY31	-4908	237
873	DUMMY32	-4924	84
874	DUMMY33	-4940	237
875	G219	-4956	84
876	G217	-4972	237
877	G215	-4988	84
878	G213	-5004	237
879	G211	-5020	84
880	G209	-5036	237
881	G207	-5052	84
882	G205	-5068	237
883	G203	-5084	84
884	G201	-5100	237
885	G199	-5116	84
886	G197	-5132	237
887	G195	-5148	84
888	G193	-5164	237
889	G191	-5180	84
890	G189	-5196	237
891	G187	-5212	84
892	G185	-5228	237
893	G183	-5244	84
894	G181	-5260	237
895	G179	-5276	84
896	G177	-5292	237
897	G175	-5308	84
898	G173	-5324	237

PAD NO.	PAD Name	X	Y
899	G171	-5340	84
900	G169	-5356	237
901	G167	-5372	84
902	G165	-5388	237
903	G163	-5404	84
904	G161	-5420	237
905	G159	-5436	84
906	G157	-5452	237
907	G155	-5468	84
908	G153	-5484	237
909	G151	-5500	84
910	G149	-5516	237
911	G147	-5532	84
912	G145	-5548	237
913	G143	-5564	84
914	G141	-5580	237
915	G139	-5596	84
916	G137	-5612	237
917	G135	-5628	84
918	G133	-5644	237
919	G131	-5660	84
920	G129	-5676	237
921	G127	-5692	84
922	G125	-5708	237
923	G123	-5724	84
924	G121	-5740	237
925	G119	-5756	84
926	G117	-5772	237
927	G115	-5788	84
928	G113	-5804	237
929	G111	-5820	84
930	G109	-5836	237
931	G107	-5852	84
932	G105	-5868	237
933	G103	-5884	84
934	G101	-5900	237
935	G99	-5916	84
936	G97	-5932	237
937	G95	-5948	84
938	G93	-5964	237
939	G91	-5980	84
940	G89	-5996	237
941	G87	-6012	84
942	G85	-6028	237
943	G83	-6044	84
944	G81	-6060	237
945	G79	-6076	84
946	G77	-6092	237
947	G75	-6108	84
948	G73	-6124	237
949	G71	-6140	84
950	G69	-6156	237
951	G67	-6172	84

PAD NO.	PAD Name	X	Y
952	G65	-6188	237
953	G63	-6204	84
954	G61	-6220	237
955	G59	-6236	84
956	G57	-6252	237
957	G55	-6268	84
958	G53	-6284	237
959	G51	-6300	84
960	G49	-6316	237
961	G47	-6332	84
962	G45	-6348	237
963	G43	-6364	84
964	G41	-6380	237

PAD NO.	PAD Name	X	Y
965	G39	-6396	84
966	G37	-6412	237
967	G35	-6428	84
968	G33	-6444	237
969	G31	-6460	84
970	G29	-6476	237
971	G27	-6492	84
972	G25	-6508	237
973	G23	-6524	84
974	G21	-6540	237
975	G19	-6556	84
976	G17	-6572	237
977	G15	-6588	84

PAD NO.	PAD Name	X	Y
978	G13	-6604	237
979	G11	-6620	84
980	G9	-6636	237
981	G7	-6652	84
982	G5	-6668	237
983	G3	-6684	84
984	G1	-6700	237
985	DUMMY34	-6716	84
986	DUMMY35	-6732	237
987	DUMMY36	-6748	84
988	DUMMY37	-6764	237

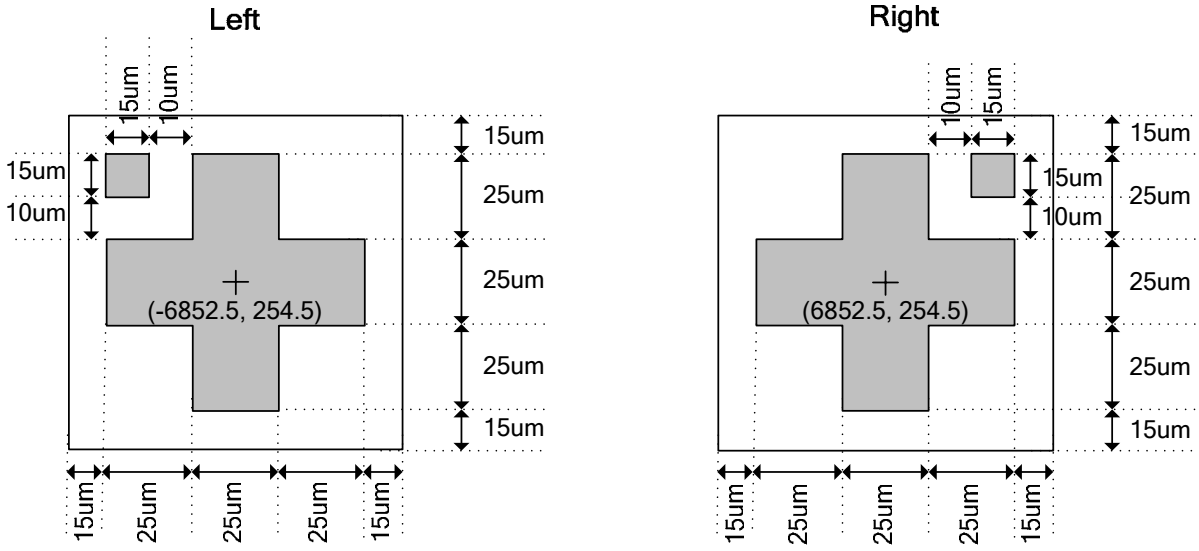
13.4. Alignment mark

--Alignment Mark coordinate

Left (-6852.5, 254.5)

Right (6852.5, 254.5)

--Alignment Mark size



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15. REVISION HISTORY

Date	Revision #	Description	Page
MAY. 05, 2009	0.2	1. Modify Block Diagram of Block function and description of R07h, R14h register. Revise AVSS to VSSA and VSSC to VSS. 2. Revise DVDD to VDD_18V, Modify Signal Description of TEST01, TEST2~7, VSS and VSSA 3. Modify description of R00h register 4. Modify description of R28h register 5. Add flow chart of Power ON/Off sequence. 6. Revise VDDA to AVDD, RW_WRB_SCL to RW_WRB,IM0_ID to IM0 7. Revise VDDIO to VDD3	5, 17, 25 10 13 42 50 53 54
JAN. 20, 2009	0.1	Original	61