PCF8576C
Universal LCD driver for low multiplex rates

Product specification
Supersedes data of 2001 Oct 02
Universal LCD driver for low multiplex rates

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1 FEATURES

• Single-chip LCD controller/driver
• Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
• Selectable display bias configuration: static, 1/2 or 1/3
• Internal LCD bias generation with voltage-follower buffers
• 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
• 40 × 4-bit RAM for display data storage
• Auto-incremented display data loading across device subaddress boundaries
• Display memory bank switching in static and duplex drive modes
• Versatile blinking modes
• LCD and logic supplies may be separated
• Wide power supply range: from 2 V for low-threshold LCDs and up to 6 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs. A 9 V version is also available on request.
• Low power consumption
• Power-saving mode for extremely low power consumption in battery-operated and telephone applications
• I²C-bus interface
• TTL/CMOS compatible
• Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers

• May be cascaded for large LCD applications (up to 2560 segments possible)
• Cascadable with 24-segment LCD driver PCF8566
• Optimized pinning for plane wiring in both and multiple PCF8576C applications
• Space-saving 56-lead plastic very small outline package (VSO56) or 64-lead low profile quad flat package (LQFP64)
• No external components
• Compatible with chip-on-glass technology
• Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCF8576C is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576C is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional I²C-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

3 ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TYPE NUMBER</th>
<th>NAME</th>
<th>PACKAGE NAME / DESCRIPTION</th>
<th>VERSION</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCF8576CT</td>
<td>VSO56</td>
<td>plastic very small outline package; 56 leads</td>
<td>SOT190-1</td>
</tr>
<tr>
<td>PCF8576CU</td>
<td>–</td>
<td>chip in tray</td>
<td>–</td>
</tr>
<tr>
<td>PCF8576CU/2</td>
<td>–</td>
<td>chip with bumps in tray</td>
<td>–</td>
</tr>
<tr>
<td>PCF8576CU/10</td>
<td>FFC</td>
<td>chip-on-film frame carrier</td>
<td>–</td>
</tr>
<tr>
<td>PCF8576CU/12</td>
<td>FFC</td>
<td>chip with bumps on film frame carrier</td>
<td>–</td>
</tr>
<tr>
<td>PCF8576CH</td>
<td>LQFP64</td>
<td>plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm</td>
<td>SOT314-2</td>
</tr>
</tbody>
</table>
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**Fig.1 Block diagram; VSO56.**
### 5 PINNING

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDA</td>
<td>1</td>
<td>10 I^2C-bus serial data input/output</td>
</tr>
<tr>
<td>SCL</td>
<td>2</td>
<td>11 I^2C-bus serial clock input</td>
</tr>
<tr>
<td>SYNC</td>
<td>3</td>
<td>12 cascade synchronization input/output</td>
</tr>
<tr>
<td>CLK</td>
<td>4</td>
<td>13 external clock input</td>
</tr>
<tr>
<td>V\text{DD}</td>
<td>5</td>
<td>14 supply voltage</td>
</tr>
<tr>
<td>OSC</td>
<td>6</td>
<td>15 oscillator input</td>
</tr>
<tr>
<td>A0 to A2</td>
<td>7 to 9</td>
<td>16 to 18 I^2C-bus subaddress inputs</td>
</tr>
<tr>
<td>SA0</td>
<td>10</td>
<td>19 I^2C-bus slave address input; bit 0</td>
</tr>
<tr>
<td>V\text{SS}</td>
<td>11</td>
<td>20 logic ground</td>
</tr>
<tr>
<td>V\text{LCD}</td>
<td>12</td>
<td>21 LCD supply voltage</td>
</tr>
<tr>
<td>BP0, BP2, BP1, BP3</td>
<td>13 to 16</td>
<td>25 to 28 LCD backplane outputs</td>
</tr>
<tr>
<td>S0 to S39</td>
<td>17 to 56</td>
<td>29 to 32, 34 to 47, 49 to 64, 2 to 7 LCD segment outputs</td>
</tr>
<tr>
<td>n.c.</td>
<td>–</td>
<td>1, 8, 9, 22 to 24, 33 and 48 not connected</td>
</tr>
</tbody>
</table>
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Fig.2 Pin configuration; VSO56.
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Fig.3 Pin configuration; LQFP64.
6 FUNCTIONAL DESCRIPTION

The PCF8576C is a versatile peripheral device designed to interface to any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576C depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig.4.

Table 1 Selection of display configurations

<table>
<thead>
<tr>
<th>BACKPLANES</th>
<th>SEGMENTS</th>
<th>SEGMENTS</th>
<th>DIGITS</th>
<th>DIGITS</th>
<th>SYMBOLS</th>
<th>SYMBOLS</th>
<th>DOT MATRIX</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>160</td>
<td>20</td>
<td>20</td>
<td>10</td>
<td>20</td>
<td>160 dots (4 × 40)</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>120</td>
<td>15</td>
<td>15</td>
<td>8</td>
<td>8</td>
<td>120 dots (3 × 40)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>80</td>
<td>10</td>
<td>10</td>
<td>5</td>
<td>10</td>
<td>80 dots (2 × 40)</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>40</td>
<td>5</td>
<td>5</td>
<td>2</td>
<td>12</td>
<td>40 dots (1 × 40)</td>
<td></td>
</tr>
</tbody>
</table>

The host microprocessor/microcontroller maintains the 2-line I²C-bus communication channel with the PCF8576C. The internal oscillator is selected by tying OSC (pin 6) to VSS (pin 11). The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (VDD, VSS and VLCD) and the LCD panel chosen for the application.

Fig.4 Typical system configuration.
6.1 Power-on reset

At power-on the PCF8576C resets to a starting condition as follows:
1. All backplane outputs are set to \( V_{DD} \).
2. All segment outputs are set to \( V_{DD} \).
3. The drive mode ‘1 : 4 multiplex with \( \frac{1}{3} \text{bias} \)’ is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I²C-bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I²C-bus should be avoided for 1 ms following power-on to allow completion of the reset action.

6.2 LCD bias generator

The full-scale LCD voltage (\( V_{op} \)) is obtained from \( V_{DD} - V_{LCD} \). The LCD voltage may be temperature compensated externally through the \( V_{LCD} \) supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of the three series resistors connected between \( V_{DD} \) and \( V_{LCD} \). The centre resistor can be switched out of the circuit to provide a \( \frac{1}{3} \text{bias} \) voltage level for the 1 : 2 multiplex configuration.

6.3 LCD voltage selector

The LCD voltage selector co-ordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of \( V_{op} = V_{DD} - V_{LCD} \) and the resulting discrimination ratios (D), are given in Table 2.

A practical value for \( V_{op} \) is determined by equating \( V_{off(rms)} \) with a defined LCD threshold voltage \( (V_{th}) \), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is \( V_{op} > 3V_{th} \) approximately.

Multiplex drive ratios of 1 : 3 and 1 : 4 with \( \frac{1}{2} \text{bias} \) are possible but the discrimination and hence the contrast ratios are smaller (\( \sqrt{3} = 1.732 \) for 1 : 3 multiplex or \( \sqrt{2} = 1.528 \) for 1 : 4 multiplex).

The advantage of these modes is a reduction of the LCD full-scale voltage \( V_{op} \) as follows:
- 1 : 3 multiplex (\( \frac{1}{2} \text{bias} \)):
  \[ V_{op} = \sqrt{3} \times V_{off(rms)} = 2.449 V_{off(rms)} \]
- 1 : 4 multiplex (\( \frac{1}{3} \text{bias} \)):
  \[ V_{op} = \left[ \frac{4 \times \sqrt{3}}{3} \right] = 2.309 V_{off(rms)} \]

These compare with \( V_{op} = 3 V_{off(rms)} \) when \( \frac{1}{3} \text{bias} \) is used.

### Table 2  Preferred LCD drive modes: summary of characteristics

<table>
<thead>
<tr>
<th>LCD DRIVE MODE</th>
<th>NUMBER OF BACKPLANES</th>
<th>NUMBER OF LEVELS</th>
<th>LCD BIAS CONFIGURATION</th>
<th>( V_{off(rms)} )</th>
<th>( \frac{V_{on(rms)}}{V_{op}} )</th>
<th>( \frac{V_{on(rms)}}{V_{op}} )</th>
<th>( D = \frac{V_{on(rms)}}{V_{off(rms)}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>static</td>
<td>1</td>
<td>2</td>
<td>static</td>
<td>0</td>
<td>1</td>
<td>( \infty )</td>
<td>2.236</td>
</tr>
<tr>
<td>1 : 2</td>
<td>2</td>
<td>3</td>
<td>( \frac{1}{2} )</td>
<td>0.354</td>
<td>0.791</td>
<td>2.236</td>
<td></td>
</tr>
<tr>
<td>1 : 2</td>
<td>2</td>
<td>4</td>
<td>( \frac{1}{3} )</td>
<td>0.333</td>
<td>0.745</td>
<td>2.236</td>
<td></td>
</tr>
<tr>
<td>1 : 3</td>
<td>3</td>
<td>4</td>
<td>( \frac{1}{3} )</td>
<td>0.333</td>
<td>0.638</td>
<td>1.915</td>
<td></td>
</tr>
<tr>
<td>1 : 4</td>
<td>4</td>
<td>4</td>
<td>( \frac{1}{3} )</td>
<td>0.333</td>
<td>0.577</td>
<td>1.732</td>
<td></td>
</tr>
</tbody>
</table>

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6.4 LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig.5.

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8576C allows use of \( \frac{1}{2} \) bias or \( \frac{1}{3} \) bias in this mode as shown in Figs 6 and 7.

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies, as shown in Fig.8.

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Fig.9.

Fig.5 Static drive mode waveforms (\( V_{op} = V_{DD} - V_{LCD} \)).
Fig. 6 Waveforms for the 1 : 2 multiplex drive mode with \( \frac{1}{2} \) bias (\( V_{\text{op}} = V_{\text{DD}} - V_{\text{LCD}} \)).

\[
V_{\text{state1}(t)} = V_{S_n(t)} - V_{BP0(t)} \\
V_{\text{on(rms)}} = 0.791V_{\text{op}} \\
V_{\text{state2}(t)} = V_{S_n(t)} - V_{BP1(t)} \\
V_{\text{off(rms)}} = 0.354V_{\text{op}}
\]
Fig. 7 Waveforms for the 1 : 2 multiplex drive mode with 1/3 bias (\(V_{\text{op}} = V_{\text{DD}} - V_{\text{LCD}}\)).
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Fig. 8 Waveforms for the 1:3 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).

\[ V_{state1}(t) = V_{op}(t) - V_{BR}(t) \]
\[ V_{on(rms)} = 0.638 V_{op} \]
\[ V_{state2}(t) = V_{op}(t) - V_{BR}(t) \]
\[ V_{off(rms)} = 0.333 V_{op} \]
Fig. 9 Waveforms for the 1 : 4 multiplex drive mode ($V_{op} = V_{DD} - V_{LCD}$).
6.5 Oscillator

6.5.1 INTERNAL CLOCK

The internal logic and the LCD drive signals of the PCF8576C are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, OSC (pin 6) should be connected to VSS (pin 11). In this event, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s or PCF8576Cs in the system.

Note that the PCF8576C is backwards compatible with the PCF8576. Where resistor Rosc to VSS is present, the internal oscillator is selected.

6.5.2 EXTERNAL CLOCK

The condition for external clock is made by tying OSC (pin 6) to VDD; CLK (pin 4) then becomes the external clock input.

The clock frequency (fclk) determines the LCD frame frequency and the maximum rate for data reception from the I2C-bus. To allow I2C-bus transmissions at their maximum data rate of 100 kHz, fclk should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

6.6 Timing

The timing of the PCF8576C organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal SYNC maintains the correct timing relationship between the PCF8576Cs in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (see Table 3). The frame frequency is set by the MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I2C-bus.

When a device is unable to digest a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I2C-bus but no data loss occurs.

6.7 Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

6.8 Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data is displayed.

6.9 Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open-circuit.

6.10 Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open-circuit. In the 1:3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.
6.11 Display RAM

The display RAM is a static 40 × 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (see Fig.10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

When display data is transmitted to the PCF8576C the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig.11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig.11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses.

In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Table 3 LCD frame frequencies

<table>
<thead>
<tr>
<th>PCF8576C MODE</th>
<th>FRAME FREQUENCY</th>
<th>NOMINAL FRAMES FREQUENCY (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal mode</td>
<td>$f_{clk}$ 2880</td>
<td>64</td>
</tr>
<tr>
<td>Power-saving mode</td>
<td>$f_{clk}$ 480</td>
<td>64</td>
</tr>
</tbody>
</table>

Fig.10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.
6.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig.11. The data pointer is automatically incremented in accordance with the chosen LCD configuration. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

6.13 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8576C occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

6.14 Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 and 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576C includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

6.15 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independent of the output bank selector.
6.16 Blinker

The display blinking capabilities of the PCF8576C are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads.

By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4  Blinking frequencies

<table>
<thead>
<tr>
<th>BLINKING MODE</th>
<th>NORMAL OPERATING MODE RATIO</th>
<th>POWER-SAVING MODE RATIO</th>
<th>NOMINAL BLINKING FREQUENCY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>−</td>
<td>−</td>
<td>blinking off</td>
</tr>
<tr>
<td>2 Hz</td>
<td>$\frac{f_{\text{clk}}}{92160}$</td>
<td>$\frac{f_{\text{clk}}}{15360}$</td>
<td>2 Hz</td>
</tr>
<tr>
<td>1 Hz</td>
<td>$\frac{f_{\text{clk}}}{184320}$</td>
<td>$\frac{f_{\text{clk}}}{30720}$</td>
<td>1 Hz</td>
</tr>
<tr>
<td>0.5 Hz</td>
<td>$\frac{f_{\text{clk}}}{368640}$</td>
<td>$\frac{f_{\text{clk}}}{61440}$</td>
<td>0.5 Hz</td>
</tr>
<tr>
<td>drive mode</td>
<td>LCD segments</td>
<td>LCD backplanes</td>
<td>display RAM filling order</td>
</tr>
<tr>
<td>------------</td>
<td>--------------</td>
<td>----------------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>static</td>
<td>$S_n$, $S_{n+1}$, $S_{n+2}$, $S_{n+3}$, $S_{n+5}$, $S_{n+7}$</td>
<td>BP0, BP1, BP2</td>
<td>n, n+1, n+2, n+3, n+4, n+5, n+6, n+7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit/0 BP 1 BP 2 BP 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1:2 multiplex</td>
<td>$S_n$, $S_{n+1}$, $S_{n+2}$</td>
<td>BP0, BP1</td>
<td>n, n+1, n+2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit/0 BP 1 BP 2 BP 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1:3 multiplex</td>
<td>$S_n$, $S_{n+1}$, $S_{n+2}$</td>
<td>BP0, BP1, BP2</td>
<td>n, n+1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit/0 BP 1 BP 2 BP 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1:4 multiplex</td>
<td>$S_n$, $S_{n+1}$</td>
<td>BP0, BP1, BP2, BP3</td>
<td>n</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>bit/0 BP 1 BP 2 BP 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

x = data bit unchanged.

Fig.11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus.
7 CHARACTERISTICS OF THE I2C-BUS

The I2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer (see Fig.12)
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

7.2 START and STOP conditions (see Fig.13)
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

7.3 System configuration (see Fig.14)
A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

7.4 Acknowledge (see Fig.15)
The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

7.5 PCF8576C I2C-bus controller
The PCF8576C acts as an I2C-bus slave receiver. It does not initiate I2C-bus transfers or transmit data to an I2C-bus master receiver. The only data output from the PCF8576C are the acknowledge signals of the selected devices. Device selection depends on the I2C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to VSS which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to VSS or VDD in accordance with a binary coding scheme such that no two devices with a common I2C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576C is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576C forces the SCL line LOW until its internal operations are completed. This is known as the ‘clock synchronization feature’ of the I2C-bus and serves to slow down fast transmitters. Data loss does not occur.

7.6 Input filters
To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.7 I2C-bus protocol
Two I2C-bus slave addresses (0111000 and 0111001) are reserved for the PCF8576C. The least significant bit of the slave address that a PCF8576C will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576C can be distinguished on the same I2C-bus which allows:
1. Up to 16 PCF8576Cs on the same I2C-bus for very large LCD applications.
2. The use of two types of LCD multiplex on the same I2C-bus.

The I2C-bus protocol is shown in Fig.16. The sequence is initiated with a START condition (S) from the I2C-bus master which is followed by one of the two PCF8675C slave addresses available. All PCF8576Cs with the corresponding SA0 level acknowledge in parallel with the slave address but all PCF8576Cs with the alternative SA0 level ignore the whole I2C-bus transfer.
After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576Cs.

The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576Cs on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8576C device. The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8576C. After the last display byte, the I2C-bus master issues a STOP condition (P).

7.8 Command decoder
The command decoder identifies command bytes that arrive on the I2C-bus. All available commands carry a continuation bit C in their most significant bit position (Fig.17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8576C are defined in Table 5.
Universal LCD driver for low multiplex rates  

**Fig. 14** System configuration.

**Fig. 15** Acknowledgement on the \( \text{I}^2\text{C} \)-bus.
Universal LCD driver for low multiplex rates

PCF8576C

Fig.16 I2C-bus protocol.

Fig.17 General format of command byte.

C = 0; last command.
C = 1; commands continue.
### Table 5: Definition of PCF8576C commands

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>OPCODE</th>
<th>OPTIONS</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODE SET</td>
<td>C 1 0</td>
<td>LP E B M1 M0</td>
<td>Table 6 Defines LCD drive mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Table 7 Defines LCD bias configuration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Table 8 Defines display status. The possibility to disable the display allows implementation of blinking under external control.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Table 9 Defines power dissipation mode.</td>
</tr>
<tr>
<td>LOAD DATA POINTER</td>
<td>C 0 P5 P4 P3 P2 P1 P0</td>
<td>Table 10 Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses.</td>
<td></td>
</tr>
<tr>
<td>DEVICE SELECT</td>
<td>C 1 1 0 0 A2 A1 A0</td>
<td>Table 11 Three bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of eight hardware subaddresses.</td>
<td></td>
</tr>
<tr>
<td>BANK SELECT</td>
<td>C 1 1 1 1 0 1 0</td>
<td>Table 12 Defines input bank selection (storage of arriving display data).</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Table 13 Defines output bank selection (retrieval of LCD display data).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes.</td>
</tr>
<tr>
<td>BLINK</td>
<td>C 1 1 1 0 A BF1 BF0</td>
<td>Table 14 Defines the blinking frequency.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Table 15 Selects the blinking mode; normal operation with frequency set by BF1, BF0 or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes.</td>
</tr>
</tbody>
</table>

### Table 6: Mode set option 1

<table>
<thead>
<tr>
<th>LCD DRIVE MODE</th>
<th>BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRIVE MODE</td>
<td>BACKPLANE</td>
</tr>
<tr>
<td>Static</td>
<td>1 BP</td>
</tr>
<tr>
<td>1 : 2</td>
<td>MUX (2 BP)</td>
</tr>
<tr>
<td>1 : 3</td>
<td>MUX (3 BP)</td>
</tr>
<tr>
<td>1 : 4</td>
<td>MUX (4 BP)</td>
</tr>
</tbody>
</table>

### Table 7: Mode set option 2

<table>
<thead>
<tr>
<th>LCD BIAS</th>
<th>BIT B</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2 bias</td>
<td>0</td>
</tr>
<tr>
<td>1/2 bias</td>
<td>1</td>
</tr>
</tbody>
</table>

### Table 8: Mode set option 3

<table>
<thead>
<tr>
<th>DISPLAY STATUS</th>
<th>BIT E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled (blank)</td>
<td>0</td>
</tr>
<tr>
<td>Enabled</td>
<td>1</td>
</tr>
</tbody>
</table>

### Table 9: Mode set option 4

<table>
<thead>
<tr>
<th>MODE</th>
<th>BIT LP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal mode</td>
<td>0</td>
</tr>
<tr>
<td>Power-saving mode</td>
<td>1</td>
</tr>
</tbody>
</table>

### Table 10: Load data pointer option 1

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 bit binary value of 0 to 39</td>
<td>P5 P4 P3 P2 P1 P0</td>
</tr>
</tbody>
</table>
The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576C and co-ordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

### 7.10 Cascaded operation

In large display configurations, up to 16 PCF8576Cs can be distinguished on the same I²C-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable I²C-bus slave address (SA0). When cascaded PCF8576Cs are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576Cs of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig.18).

The **SYNC** line is provided to maintain the correct synchronization between all cascaded PCF8576Cs. This synchronization is guaranteed after the power-on reset. The only time that **SYNC** is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576Cs with differing SA0 levels are cascaded). **SYNC** is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor.

A PCF8576C asserts the **SYNC** line at the onset of its last active backplane signal and monitors the **SYNC** line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8675C to assert **SYNC**. The timing relationship between the backplane waveforms and the **SYNC** signal for the various drive modes of the PCF8576C are shown in Fig.19.

For single plane wiring of packaged PCF8576Cs and chip-on-glass cascading, see Chapter “Application information”.
Universal LCD driver for low multiplex rates

**Fig. 18** Cascaded PCF8576C configuration.
Excessive capacitive coupling between SCL or CLK and \textit{SYNC} may cause erroneous synchronization. If this proves to be a problem, the capacitance of the \textit{SYNC} line should be increased (e.g. by an external capacitor between \textit{SYNC} and V_{DD}). Degradation of the positive edge of the \textit{SYNC} pulse may be countered by an external pull-up resistor.

(a) static drive mode.
(b) 1 : 2 multiplex drive mode.
(c) 1 : 3 multiplex drive mode.
(d) 1 : 4 multiplex drive mode.

\textbf{Fig.19} Synchronization of the cascade for the various PCF8576C drive modes.
8 LIMITING VALUES
In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_DD</td>
<td>supply voltage</td>
<td>−0.5</td>
<td>+8.0</td>
<td>V</td>
</tr>
<tr>
<td>V_LCD</td>
<td>LCD supply voltage</td>
<td>V_DD − 8.0</td>
<td>V_DD</td>
<td>V</td>
</tr>
<tr>
<td>V_{I1}</td>
<td>input voltage CLK, SYNC, SA0, OSC, A0 to A2</td>
<td>V_{SS} − 0.5</td>
<td>V_DD + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>V_{I2}</td>
<td>input voltage SDA, SCL</td>
<td>V_{SS} − 0.5</td>
<td>+8.0</td>
<td>V</td>
</tr>
<tr>
<td>V_O</td>
<td>output voltage S0 to S39, BP0 to BP3</td>
<td>V_LCD − 0.5</td>
<td>V_DD + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>I_I</td>
<td>DC input current</td>
<td>−20</td>
<td>+20</td>
<td>mA</td>
</tr>
<tr>
<td>I_O</td>
<td>DC output current</td>
<td>−25</td>
<td>+25</td>
<td>mA</td>
</tr>
<tr>
<td>I_{DD}, I_{SS}, I_{LCD}</td>
<td>V_DD, V_{SS} or V_LCD current</td>
<td>−50</td>
<td>+50</td>
<td>mA</td>
</tr>
<tr>
<td>P_tot</td>
<td>total power dissipation</td>
<td>−</td>
<td>400</td>
<td>mW</td>
</tr>
<tr>
<td>P_O</td>
<td>power dissipation per output</td>
<td>−</td>
<td>100</td>
<td>mW</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>storage temperature</td>
<td>−65</td>
<td>+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

9 HANDLING
Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS Devices”).
10 DC CHARACTERISTICS

$V_{DD} = 2 \text{ V to } 6 \text{ V}; V_{SS} = 0 \text{ V}; V_{LCD} = V_{DD} - 2 \text{ V to } V_{DD} - 6 \text{ V}; T_{amb} = -40 \degree \text{C to } +85 \degree \text{C};$ unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>supply voltage</td>
<td></td>
<td>2</td>
<td>–</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LCD}$</td>
<td>LCD supply voltage</td>
<td>note 1</td>
<td>$V_{DD} - 6$</td>
<td>–</td>
<td>$V_{DD} - 2$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>supply current</td>
<td></td>
<td>note 2</td>
<td>$f_{CLK} = 200 \text{ kHz}$</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td>normal mode</td>
<td></td>
<td></td>
<td>$f_{CLK} = 35 \text{ kHz}$; $V_{DD} = 3.5 \text{ V}; V_{LCD} = 0 \text{ V}$; A0, A1 and A2 tied to $V_{SS}$</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>LOW-level input voltage SDA, SCL, CLK, SYNC, SA0, OSC, A0 to A2</td>
<td>$V_{SS}$</td>
<td>–</td>
<td>–</td>
<td>0.3$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH1}$</td>
<td>HIGH-level input voltage CLK, SYNC, SA0, OSC, A0 to A2</td>
<td>$0.7V_{DD}$</td>
<td>–</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IH2}$</td>
<td>HIGH-level input voltage SDA, SCL</td>
<td>$0.7V_{DD}$</td>
<td>–</td>
<td>6.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$</td>
<td>LOW-level output voltage</td>
<td>$I_{OL} = 0 \text{ mA}$</td>
<td>–</td>
<td>–</td>
<td>0.05</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td>HIGH-level output voltage</td>
<td>$I_{OH} = 0 \text{ mA}$</td>
<td>$V_{DD} - 0.05$</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OL1}$</td>
<td>LOW-level output current CLK, SYNC</td>
<td>$V_{OL} = 1 \text{ V}; V_{DD} = 5 \text{ V}$</td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OH1}$</td>
<td>HIGH-level output current CLK</td>
<td>$V_{OH} = 4 \text{ V}; V_{DD} = 5 \text{ V}$</td>
<td>–1</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OL2}$</td>
<td>LOW-level output current SDA, SCL</td>
<td>$V_{OL} = 0.4 \text{ V}; V_{DD} = 5 \text{ V}$</td>
<td>3</td>
<td>–</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{L1}$</td>
<td>leakage current SA0, A0 to A2, CLK, SDA and SCL</td>
<td>$V = V_{DD}$ or $V_{SS}$</td>
<td>–1</td>
<td>–</td>
<td>+1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{L2}$</td>
<td>leakage current OSC</td>
<td>$V = V_{DD}$</td>
<td>–1</td>
<td>–</td>
<td>+1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{pd}$</td>
<td>A0, A1, A2 and OSC pull-down current</td>
<td>$V = 1 \text{ V}; V_{DD} = 5 \text{ V}$</td>
<td>15</td>
<td>50</td>
<td>150</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$R_{SYNC}$</td>
<td>pull-up resistor (SYNC)</td>
<td></td>
<td>20</td>
<td>50</td>
<td>150</td>
<td>k$\Omega$</td>
</tr>
<tr>
<td>$V_{POR}$</td>
<td>power-on reset voltage level</td>
<td>note 3</td>
<td>–</td>
<td>1.0</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td>$t_{SW}$</td>
<td>tolerable spike width on bus</td>
<td></td>
<td>–</td>
<td>–</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>$C_{i}$</td>
<td>input capacitance</td>
<td>note 4</td>
<td>–</td>
<td>–</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

**LCD outputs**

| SYMBOL | DC voltage component BP0 to BP3 | $C_{BP} = 35 \text{ nF}$ | –20 | – | +20 | mV |
| $V_{S}$ | DC voltage component S0 to S39 | $C_{S} = 5 \text{ nF}$ | –20 | – | +20 | mV |
| $R_{BP}$ | output resistance BP0 to BP3 | note 5; $V_{LCD} = V_{DD} - 5 \text{ V}$ | – | – | 5 | k$\Omega$ |
| $R_{S}$ | output resistance S0 to S39 | note 5; $V_{LCD} = V_{DD} - 5 \text{ V}$ | – | – | 7.5 | k$\Omega$ |

**Notes**

1. $V_{LCD} \leq V_{DD} - 3 \text{ V for } \frac{1}{2}\text{bias}$.  
2. LCD outputs are open-circuit; inputs at $V_{SS}$ or $V_{DD}$; external clock with 50 % duty factor; $I^{2}$C-bus inactive.
3. Resets all logic when $V_{DD} < V_{POR}$.  
4. Periodically sampled, not 100 % tested.  
5. Outputs measured one at a time.
11 AC CHARACTERISTICS

\( V_{DD} = 2 \, \text{V to 6 \, \text{V}} \); \( V_{SS} = 0 \, \text{V} \); \( V_{LCD} = V_{DD} - 2 \, \text{V to} \, V_{DD} - 6 \, \text{V} \); \( T_{amb} = -40 \, ^\circ \text{C} \) to +85 \, ^\circ \text{C}; unless otherwise specified.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{clk} )</td>
<td>oscillator frequency</td>
<td>( V_{DD} = 5 , \text{V}; ) note 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>normal mode</td>
<td>( V_{DD} = 5 , \text{V}; ) note 1</td>
<td>125</td>
<td>200</td>
<td>315</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>power-saving mode</td>
<td>( V_{DD} = 3.5 , \text{V} )</td>
<td>48</td>
<td>kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{clkH} )</td>
<td>CLK HIGH time</td>
<td></td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{clkL} )</td>
<td>CLK LOW time</td>
<td></td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{SYNC} )</td>
<td>SYNC propagation delay time</td>
<td></td>
<td>–</td>
<td>–</td>
<td>400</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{SYNC} )</td>
<td>SYNC LOW time</td>
<td></td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{PLCD} )</td>
<td>driver delays with test loads</td>
<td>( V_{LCD} = V_{DD} - 5 , \text{V} )</td>
<td>–</td>
<td>–</td>
<td>30</td>
<td>( \mu \text{s} )</td>
</tr>
</tbody>
</table>

Timing characteristics: \( \text{I}^2\text{C-bus}; \) note 2

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{BUF} )</td>
<td>bus free time</td>
<td></td>
<td>4.7</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{HD,STA} )</td>
<td>START condition hold time</td>
<td></td>
<td>4.0</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{SU,STA} )</td>
<td>set-up time for a repeated START condition</td>
<td></td>
<td>4.7</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{LOW} )</td>
<td>SCL LOW time</td>
<td></td>
<td>4.7</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t_{HIGH} )</td>
<td>SCL HIGH time</td>
<td></td>
<td>4.0</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t )</td>
<td>SCL and SDA rise time</td>
<td></td>
<td>–</td>
<td>–</td>
<td>1</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( t )</td>
<td>SCL and SDA fall time</td>
<td></td>
<td>–</td>
<td>–</td>
<td>0.3</td>
<td>( \mu \text{s} )</td>
</tr>
<tr>
<td>( C_{B} )</td>
<td>capacitive bus line load</td>
<td></td>
<td>–</td>
<td>–</td>
<td>400</td>
<td>pF</td>
</tr>
<tr>
<td>( t_{SU,DAT} )</td>
<td>data set-up time</td>
<td></td>
<td>250</td>
<td>–</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{HD,DAT} )</td>
<td>data hold time</td>
<td></td>
<td>0</td>
<td>–</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{SU,STO} )</td>
<td>set-up time for STOP condition</td>
<td></td>
<td>4.0</td>
<td>–</td>
<td>–</td>
<td>( \mu \text{s} )</td>
</tr>
</tbody>
</table>

Notes

1. At \( f_{clk} < 125 \, \text{kHz}, \) \( \text{I}^2\text{C-bus maximum transmission speed is derated.} \)
2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to \( V_{IL} \) and \( V_{IH} \) with an input voltage swing of \( V_{SS} \) to \( V_{DD} \).
Fig. 21  Driver timing waveforms.

Fig. 22  \( \text{I}^2\text{C}-\text{bus} \) timing waveforms.
11.1 Typical supply current characteristics

**Fig. 23** $I_{SS}$ as a function of $f_{\text{frame}}$.

\[
\begin{align*}
V_{DD} &= 5 \, \text{V} \quad V_{LCD} = 0 \, \text{V} \quad T_{\text{amb}} = 25 \, ^{\circ}\text{C}.
\end{align*}
\]

**Fig. 24** $I_{LCD}$ as a function of $f_{\text{frame}}$.

\[
\begin{align*}
V_{DD} &= 5 \, \text{V} \quad V_{LCD} = 0 \, \text{V} \quad T_{\text{amb}} = 25 \, ^{\circ}\text{C}.
\end{align*}
\]

**Fig. 25** $I_{SS}$ as a function of $V_{DD}$.

\[
\begin{align*}
V_{LCD} &= 0 \, \text{V} \quad \text{external clock} \quad T_{\text{amb}} = 25 \, ^{\circ}\text{C}.
\end{align*}
\]

**Fig. 26** $I_{LCD}$ as a function of $V_{DD}$.

\[
\begin{align*}
V_{LCD} &= 0 \, \text{V} \quad \text{external clock} \quad f_{\text{clk}} = \text{nominal frequency}.
\end{align*}
\]
11.2 Typical characteristics of LCD outputs

Fig. 27 $R_{O\text{max}}$ as a function of $V_{DD}$.

$V_{LCD} = 0\, V; T_{amb} = 25\, ^{\circ}C$.

Fig. 28 $R_{O\text{max}}$ as a function of $T_{amb}$.

$V_{DD} = 5\, V; V_{LCD} = 0\, V$. 

$R_{S}, R_{BP}$
Fig. 29  Single plane wiring of packaged PCF8576CTs.
12.1 Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576C bonding pad layout (Fig.30). Pads needing bus interconnection between all PCF8576Cs of the cascade are \( V_{DD} \), \( V_{SS} \), \( V_{LCD} \), CLK, SCL, SDA and SYNC. These lines may be led to the corresponding pads of the next PCF8576C through the wide opening between \( V_{LCD} \) pad and the backplane output pads. The only bus line that does not require a second opening to lead through to the next PCF8576C is \( V_{LCD} \), being the cascade centre. The placing of \( V_{LCD} \) adjacent to \( V_{SS} \) allows the two supplies to be tied together.

When an external clocking source is to be used, OSC of all devices should be tied to \( V_{DD} \). The pads OSC, A0, A1, A2 and SA0 have been placed between \( V_{SS} \) and \( V_{DD} \) to facilitate wiring of oscillator, hardware subaddress and slave address.

13 BONDING PAD INFORMATION

![Bonding pad locations](image)

Chip dimensions: approximately 2.92 mm \( \times \) 3.20 mm.
Pad area: 0.0121 mm\(^2\).
Table 16 Bonding pad locations (dimensions in µm)
All x and y coordinates are referenced to the centre of the chip (see Fig.30).

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PAD</th>
<th>COORDINATES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>SDA</td>
<td>1</td>
<td>−74</td>
</tr>
<tr>
<td>SCL</td>
<td>2</td>
<td>148</td>
</tr>
<tr>
<td>SYNC</td>
<td>3</td>
<td>355</td>
</tr>
<tr>
<td>CLK</td>
<td>4</td>
<td>534</td>
</tr>
<tr>
<td>V_DD</td>
<td>5</td>
<td>742</td>
</tr>
<tr>
<td>OSC</td>
<td>6</td>
<td>913</td>
</tr>
<tr>
<td>A0</td>
<td>7</td>
<td>1087</td>
</tr>
<tr>
<td>A1</td>
<td>8</td>
<td>1290</td>
</tr>
<tr>
<td>A2</td>
<td>9</td>
<td>1290</td>
</tr>
<tr>
<td>SA0</td>
<td>10</td>
<td>1290</td>
</tr>
<tr>
<td>V_SS</td>
<td>11</td>
<td>1290</td>
</tr>
<tr>
<td>V_LCD</td>
<td>12</td>
<td>1290</td>
</tr>
<tr>
<td>BP0</td>
<td>13</td>
<td>1290</td>
</tr>
<tr>
<td>BP2</td>
<td>14</td>
<td>1290</td>
</tr>
<tr>
<td>BP1</td>
<td>15</td>
<td>1290</td>
</tr>
<tr>
<td>BP3</td>
<td>16</td>
<td>1290</td>
</tr>
<tr>
<td>S0</td>
<td>17</td>
<td>1290</td>
</tr>
<tr>
<td>S1</td>
<td>18</td>
<td>1290</td>
</tr>
<tr>
<td>S2</td>
<td>19</td>
<td>1290</td>
</tr>
<tr>
<td>S3</td>
<td>20</td>
<td>1290</td>
</tr>
<tr>
<td>S4</td>
<td>21</td>
<td>1074</td>
</tr>
<tr>
<td>S5</td>
<td>22</td>
<td>914</td>
</tr>
<tr>
<td>S6</td>
<td>23</td>
<td>741</td>
</tr>
<tr>
<td>S7</td>
<td>24</td>
<td>581</td>
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<td>S8</td>
<td>25</td>
<td>408</td>
</tr>
<tr>
<td>S9</td>
<td>26</td>
<td>248</td>
</tr>
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<td>S10</td>
<td>27</td>
<td>75</td>
</tr>
<tr>
<td>S11</td>
<td>28</td>
<td>−85</td>
</tr>
<tr>
<td>S12</td>
<td>29</td>
<td>−258</td>
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<td>S13</td>
<td>30</td>
<td>−418</td>
</tr>
<tr>
<td>S14</td>
<td>31</td>
<td>−591</td>
</tr>
<tr>
<td>S15</td>
<td>32</td>
<td>−751</td>
</tr>
</tbody>
</table>

Table 17 Bonding pad dimensions

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>DIMENSIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pad pitch</td>
<td>160 µm</td>
</tr>
<tr>
<td>Pad size, aluminium</td>
<td>110 µm × 110 µm</td>
</tr>
<tr>
<td>Gold bump dimensions</td>
<td>94 µm × 94 µm × 17.5 µm</td>
</tr>
<tr>
<td>Gold bump tolerance</td>
<td>± 5 µm</td>
</tr>
</tbody>
</table>
14 TRAY INFORMATION: PCF8576CU and PCF8576CU/2

For dimensions see Table 18.

Fig.31 Tray details.

Table 18 Tray dimensions (see Fig.31)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>pocket pitch; x direction</td>
<td>5.59 mm</td>
</tr>
<tr>
<td>B</td>
<td>pocket pitch; y direction</td>
<td>6.35 mm</td>
</tr>
<tr>
<td>C</td>
<td>pocket width; x direction</td>
<td>3.22 mm</td>
</tr>
<tr>
<td>D</td>
<td>pocket width; y direction</td>
<td>3.50 mm</td>
</tr>
<tr>
<td>E</td>
<td>tray width; x direction</td>
<td>50.67 mm</td>
</tr>
<tr>
<td>F</td>
<td>tray width; y direction</td>
<td>50.67 mm</td>
</tr>
<tr>
<td>G</td>
<td>cut corner to pocket 1,1 centre</td>
<td>5.78 mm</td>
</tr>
<tr>
<td>H</td>
<td>cut corner to pocket 1,1 centre</td>
<td>6.29 mm</td>
</tr>
<tr>
<td>J</td>
<td>tray thickness</td>
<td>3.94 mm</td>
</tr>
<tr>
<td>K</td>
<td>tray cross section</td>
<td>1.76 mm</td>
</tr>
<tr>
<td>L</td>
<td>tray cross section</td>
<td>2.46 mm</td>
</tr>
<tr>
<td>M</td>
<td>pocket depth</td>
<td>0.89 mm</td>
</tr>
<tr>
<td>x</td>
<td>number of pockets; x direction</td>
<td>8</td>
</tr>
<tr>
<td>y</td>
<td>number of pockets; y direction</td>
<td>7</td>
</tr>
</tbody>
</table>

The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray.

Fig.32 Tray alignment.
15 PACKAGE OUTLINES

VSOS6: plastic very small outline package; 56 leads

SOT190-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A max.</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>b_p</th>
<th>c</th>
<th>D(1)</th>
<th>E(2)</th>
<th>e</th>
<th>H_E</th>
<th>L</th>
<th>L_p</th>
<th>Q</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>Z(1)</th>
<th>θ</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>3.3</td>
<td>0.3</td>
<td>3.0</td>
<td>0.25</td>
<td>0.42</td>
<td>0.30</td>
<td>0.22</td>
<td>0.14</td>
<td>21.65</td>
<td>11.1</td>
<td>11.0</td>
<td>0.75</td>
<td>15.8</td>
<td>15.2</td>
<td>2.25</td>
<td>1.6</td>
<td>1.4</td>
<td>1.45</td>
</tr>
<tr>
<td>inches</td>
<td>0.13</td>
<td>0.012</td>
<td>0.12</td>
<td>0.01</td>
<td>0.017</td>
<td>0.012</td>
<td>0.0055</td>
<td>0.0087</td>
<td>0.85</td>
<td>0.0295</td>
<td>0.0008</td>
<td>0.063</td>
<td>0.057</td>
<td>0.008</td>
<td>0.004</td>
<td>0.004</td>
<td>0.0035</td>
<td>0.01</td>
</tr>
</tbody>
</table>

Notes:
1. Plastic or metal protrusions of 0.3 mm (0.012 inch) maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm (0.01 inch) maximum per side are not included.
Universal LCD driver for low multiplex rates  

PCF8576C

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm  

SOT314-2

DIMENSIONS (mm are the original dimensions)

<table>
<thead>
<tr>
<th>UNIT</th>
<th>A max.</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>b p</th>
<th>c</th>
<th>D (1)</th>
<th>E (1)</th>
<th>e</th>
<th>H D</th>
<th>H E</th>
<th>L</th>
<th>L p</th>
<th>v</th>
<th>w</th>
<th>y</th>
<th>Z0 (1)</th>
<th>ZE (1)</th>
<th>α</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm</td>
<td>1.6</td>
<td>0.20</td>
<td>1.45</td>
<td>0.25</td>
<td>0.27</td>
<td>0.18</td>
<td>10.1</td>
<td>10.1</td>
<td>0.5</td>
<td>12.15</td>
<td>12.15</td>
<td>1</td>
<td>0.75</td>
<td>0.12</td>
<td>0.1</td>
<td>1.45</td>
<td>1.45</td>
<td>7°</td>
<td></td>
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Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION

<table>
<thead>
<tr>
<th>REFERENCES</th>
<th>EUROPEAN PROJECTION</th>
<th>ISSUE DATE</th>
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<td>06-01-19</td>
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<tr>
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<td>MS-026</td>
<td>03-02-25</td>
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16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our “Data Handbook IC: Integrated Circuit Packages” (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.
16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

<table>
<thead>
<tr>
<th>PACKAGE(1)</th>
<th>SOLENDER METHOD</th>
</tr>
</thead>
<tbody>
<tr>
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<td>WAVE</td>
</tr>
<tr>
<td>BGA, HTSSON..T(3), LBGA, LFBGA, SQFP, SSOP..T(3), TFBGA, VFBGA, XSON</td>
<td>not suitable</td>
</tr>
<tr>
<td>DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS</td>
<td>not suitable(4)</td>
</tr>
<tr>
<td>PLCC(5), SO, SOJ</td>
<td>suitable</td>
</tr>
<tr>
<td>LQFP, QFP, TQFP</td>
<td>not recommended(5)(6)</td>
</tr>
<tr>
<td>SSOP, TSSOP, VSO, VSSOP</td>
<td>not recommended(7)</td>
</tr>
<tr>
<td>CWQCCN..L(8), PMFP(9), WQCCN..L(8)</td>
<td>not suitable</td>
</tr>
</tbody>
</table>

1. For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.

2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.

3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

6. Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

9. Hot bar soldering or manual soldering is suitable for PMFP packages.
17 DATA SHEET STATUS

<table>
<thead>
<tr>
<th>LEVEL</th>
<th>DATA SHEET STATUS(^{(1)})</th>
<th>PRODUCT STATUS(^{(2)(3)})</th>
<th>DEFINITION</th>
</tr>
</thead>
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<td>I</td>
<td>Objective data</td>
<td>Development</td>
<td>This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.</td>
</tr>
<tr>
<td>II</td>
<td>Preliminary data</td>
<td>Qualification</td>
<td>This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.</td>
</tr>
<tr>
<td>III</td>
<td>Product data</td>
<td>Production</td>
<td>This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).</td>
</tr>
</tbody>
</table>

Notes
1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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