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Princeton Technology Corp.
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URL:http://www.princeton.com.tw

DESCRIPTION

PT6800 is an OLED Driver IC utilizing CMOS Technology specially designed to drive up to 80 segment output drivers. It provides 80-bit bidirectional shift register, 80-bit latch circuit, as well as serial/parallel converting function. Pin assignments and application circuits are optimized for easy PCB Layout and cost saving advantages.

FEATURES

- CMOS technology
- Up to 80 segment output driver
- 80-bit bidirectional shift register
- 80-bit latch circuit
- Internal logic circuit power supply: +5V ±10%
- OLED drive circuit power supply: 9.0V to 16.0V
- Available in C.O.B. or 100-pin QFP package

APPLICATIONS

- Cellular phone
- Data bank/Organizer
- Electronic dictionary/Translator
- Information appliance
- P.D.A.
- P.O.S.
- Car audio
- Electronic equipment with OLED display

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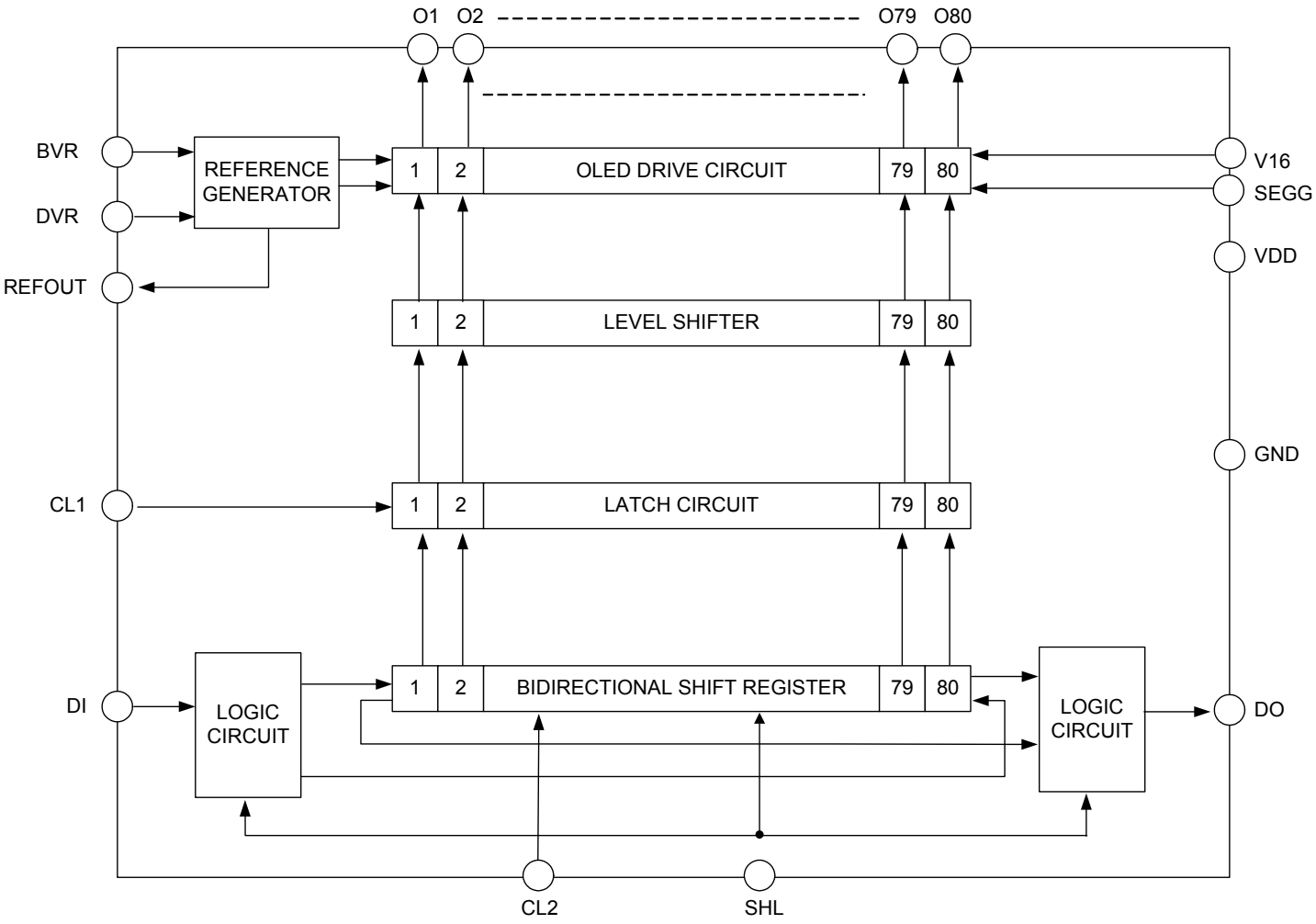
BLOCK DIAGRAM



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BLOCK DESCRIPTIONS

OLED DRIVE CIRCUITS

There are two voltage levels, namely V16 and SEGG that are used for driving the OLED. This block selects of these two voltage levels and transfers the selected one to the output terminals in accordance with the data in the latch circuit.

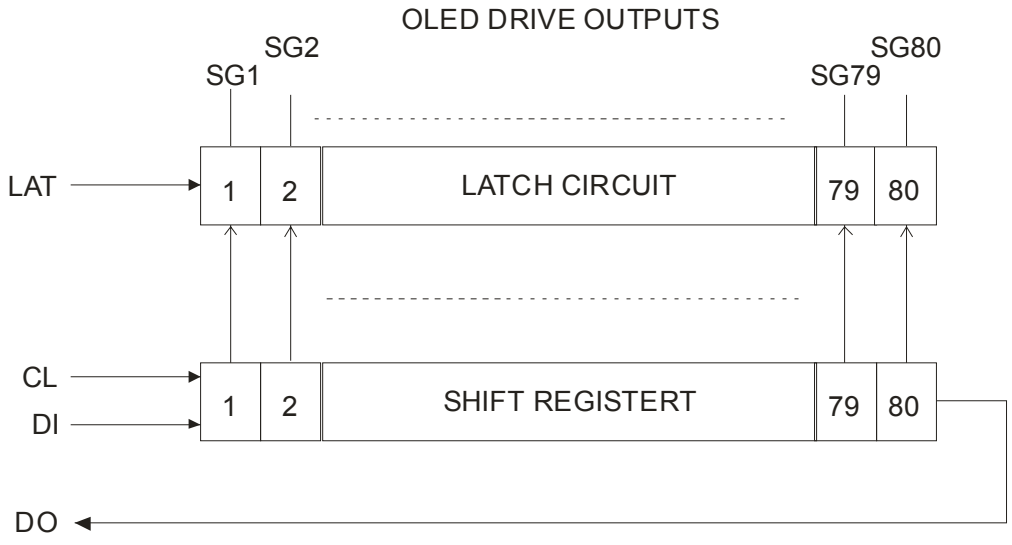
LATCH CIRCUIT BLOCK

This block latches the data inputted from the bidirectional shift register at the falling edge of the LAT signal and then transfer its output to the OLED Drive Circuits.

BIDIRECTIONAL SHIFT REGISTER BLOCK

This block shifts the serial data at the falling edge of the CL. The output of each register bits are then transferred to the Latch Circuit. When SHL is set to GND, the data input from the DI is shifted from bit 1 to bit 80 in the order of which they are entered. When SHL is set to VDD, the data is shifted from bit 80 to bit 1. In both conditions, the data of the last bit of the register is latched and outputted from DO pin at the rising edge of the CL signal. Please refer to the diagram below.

CONDITION 1: SHL=GND



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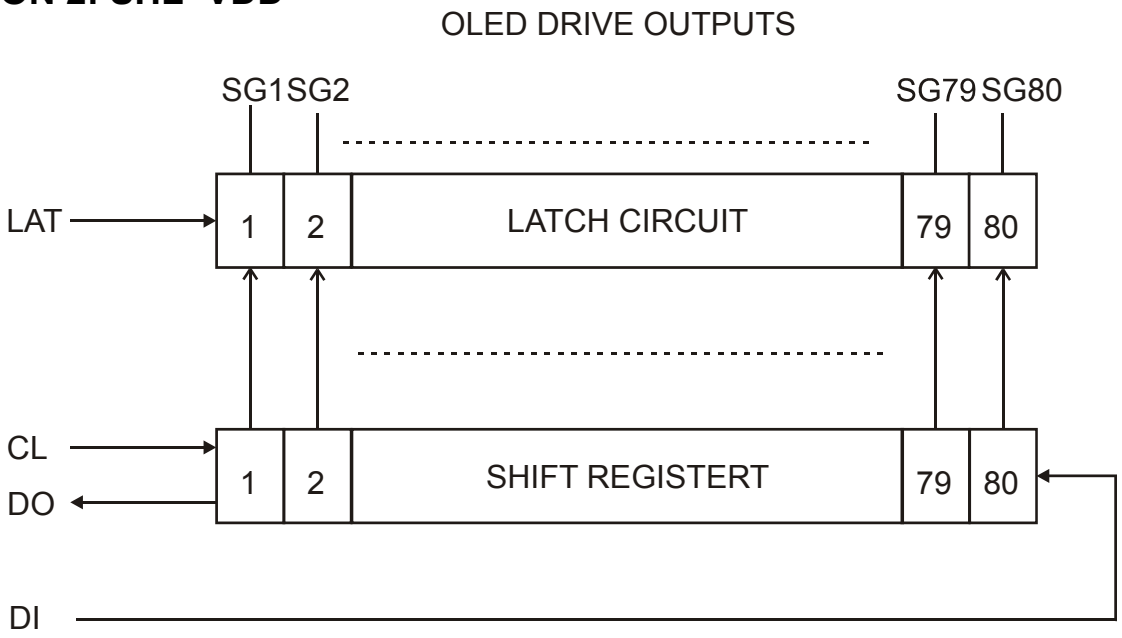
CONDITION 2: SHL=VDD



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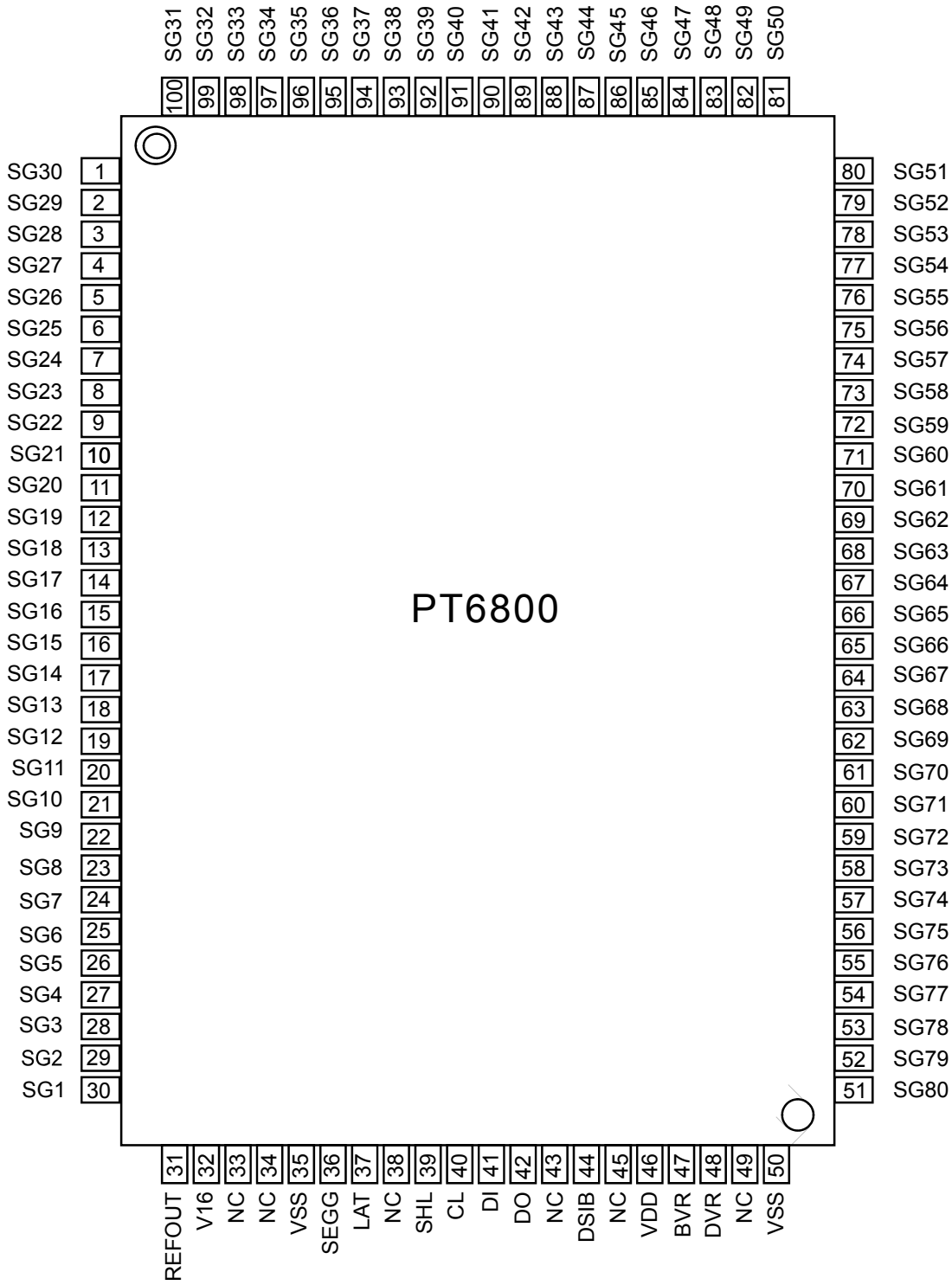
PIN CONFIGURATION

100 PINS, QFP



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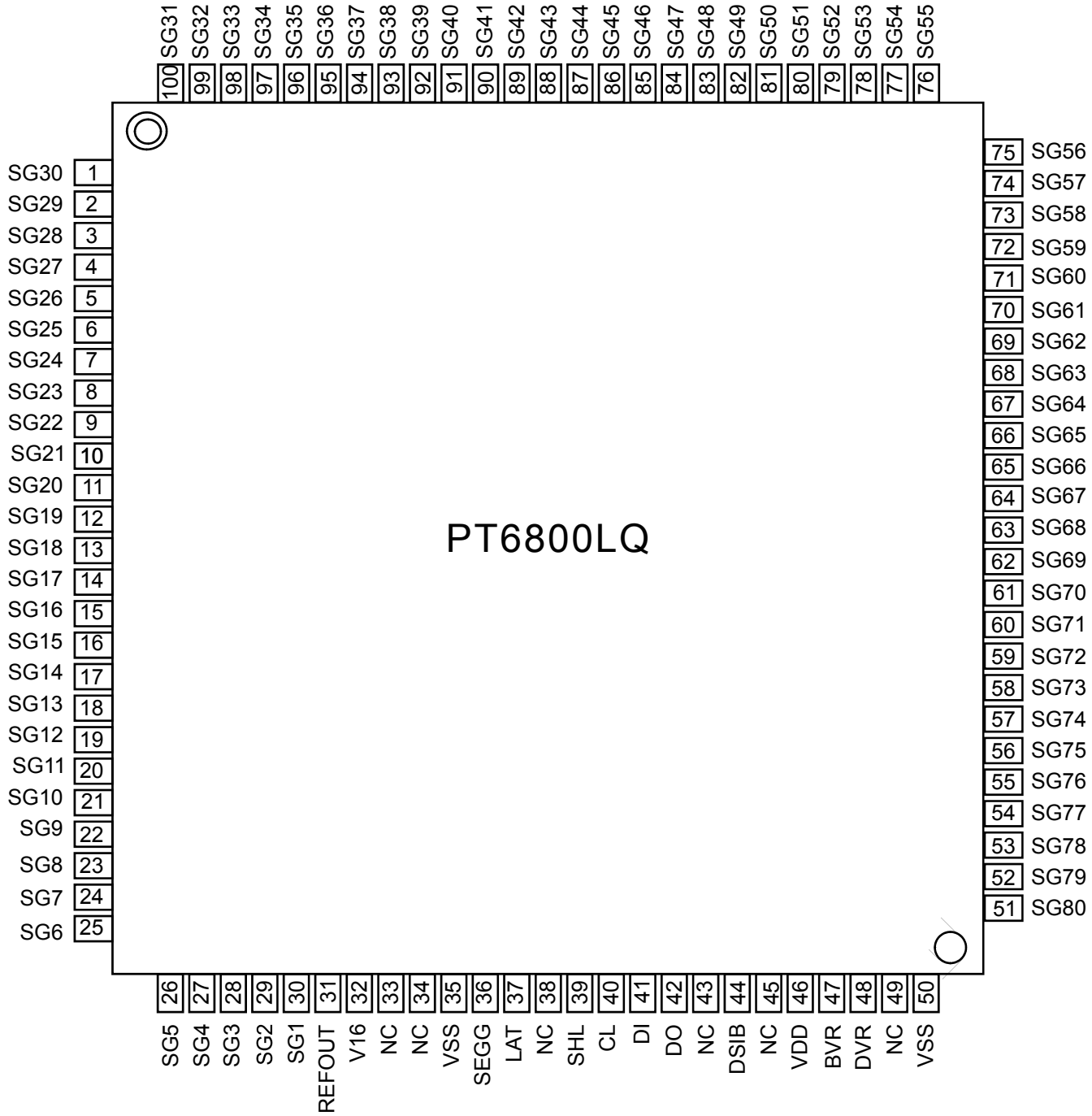
100 PINS, LQFP



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PIN/PAD DESCRIPTION

Pin Name	I/O	Description	Pad/Pin No.
SG30 ~ SG1 SG80 ~SG31	O	Segment driver output pins	1 ~ 30 51 ~ 100
VSS	-	Logic ground pin	35, 50
DVR	I	Precharge time control	48
BVR	I	Brightness control pin	47
VDD	-	Logic power supply	46
DISB	I	Reset signal	44
DO	O	Data output pin	42
DI	I	Data input pin	41
CL	I	Shift clock input pin	40
SHL	I	Data shift direction pin (see Note)	39
LAT	I	Latch clock input pin	37
SEGG	-	OLED drive power supply (0V)	36
V16	-	OLED drive power supply	32
DISB	O	Reset signal	31
NC	-	No connection	33, 34, 38, 43, 45, 49

Note: The SHL is used to select the shift direction of the serial data. When the serial data is inputted in the order of D1, D2, D3,…, D79, D80, the relationship between the data and the outputs -- SG1 to SG80 is shown in the table below.

SHL	SG1	SG2	SG3	……	SG78	SG79	SG80
VDD	D1	D2	D3	……	D78	D79	D80
VSS	D80	D79	D78	……	D3	D2	D1

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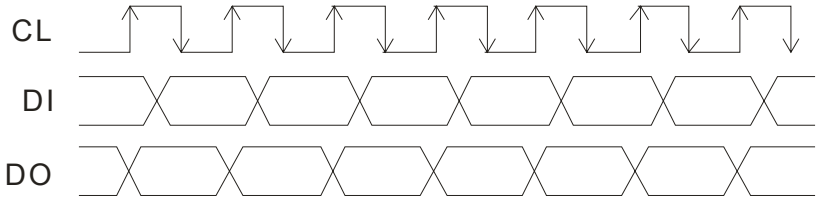
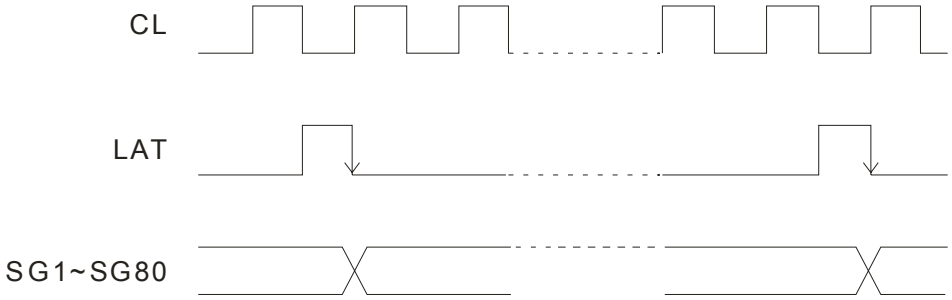
FUNCTION DESCRIPTION

The data is inputted to the shift register by the DI pin. The input data from DI is shifted at the falling edge of CL and is outputted from the DO pin after 80 bits. The output from the DO pin changes with each rising edge of the CL. The data shifting operation is independent of the latch clock -- LAT. Please refer to the diagram below.



The data of the shift register is latched at the falling edge of the latch clock LAT and the outputs SG1 to SG80 change with each falling edge of the LAT. Please refer to the diagram below.



If the SHL Pin is connected to the GND, then the data -- D80 that is located immediately before the falling edge of LAT is outputted from SG1. When the SHL is connected to VDD, then the data -- D80 is outputted from the SG80. Please refer to the diagram below.

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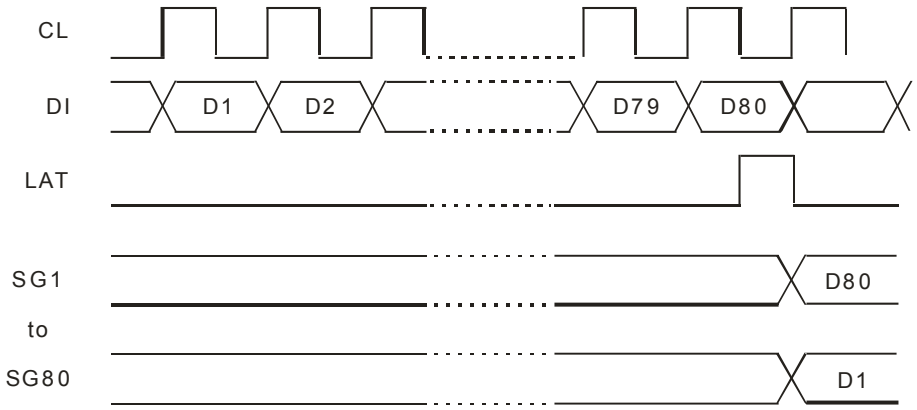
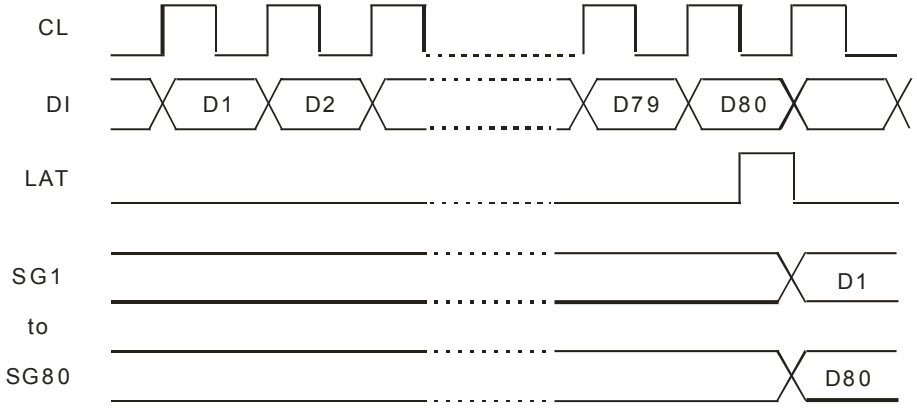
CONDITION 1: SHL=GND



CONDITION 2: SHL=VDD



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ABSOLUTE MAXIMUM RATING

(Unless otherwise specified, VDD=5V±10%, V16=9.0 to 16.0V, SEGG=0V, GND=0V, Ta=25℃)

Parameter	Symbol	Minimum	Maximum	Unit
Supply voltage (Ta=25℃)	V16	-0.3	18	V
	VDD	-0.3	5.5	V
I/O pin voltage(Ta=25 ℃)	VX	-0.3	VDD+0.3	V
Operating temperature	Topr	-40	+85	℃
Storage temperature	Tstg	-65	+150	℃

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, VDD=5V, V16=16.0V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Driver power supply	V16		7.0	-	16	V
Operating voltage	VDD		2.7	5.0	5.5	V
Operating current	ICC	VDD=5.0V, CL=270kHz	-	-	1	mA
Standby current	ISB	DISB=0V	-	-	1	μA
High level input voltage	VIH		0.8VDD	-	5.0	V
Low level input voltage	VIL		0.0	-	0.2VDD	V
High level segment output current	ISEGOH	VSEGOH=14V	-30	-	-300	μA
High level segment output current tolerance 1	ITOL1*	ISEGOH=300uA	-	-	±5	%
High level segment output current tolerance 2	ITOL2*	ISEGOH=300uA	-	-	±1	%
High level input leakage current	IIH	VDD=5V, Vo=0V VIN=5V, DISB=0V	-	-	2	μA
Low level input leakage current	IIL	VDD=5V, Vo=0V VIN=0V, DISB=0V	-	-	2	μA

Note:*=ITOL1 was measured using the 2 output pins -- one having the minimum current and the other having maximum current. ITOL2 was measured using two consecutive output pins

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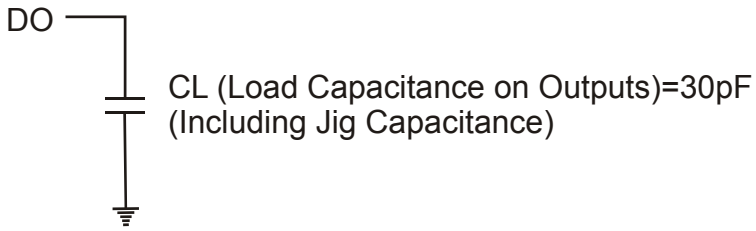
AC ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, V16=16.0V, Ta=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data shift frequency	fCL	CL	-	-	1	MHz
Clock high level width	tCWH	LAT, CL	500	-	-	ns
Clock low level width	tCWL	CL	500	-	-	ns
Data setup time	tSU	DI	100	-	-	ns
Clock setup time 1 (see Note 1)	tSL	CL	200	-	-	ns
Clock setup time 2 (see Note 2)	tLS	LAT	200	-	-	ns
Output delay time (see Note 3)	tpd	DO CL=30pF	-	-	250	ns
Data hold time	tDH	DI	100	-	-	ns

Notes:
1. Clock Setup Time 1 (tSL) is the setup time from the falling edge of CL to falling edge of LAT.
2. Clock Setup Time 2 (tLS) is the setup time from the falling edge of LAT to the falling edge of CL.
3. Please refer to the diagram below.



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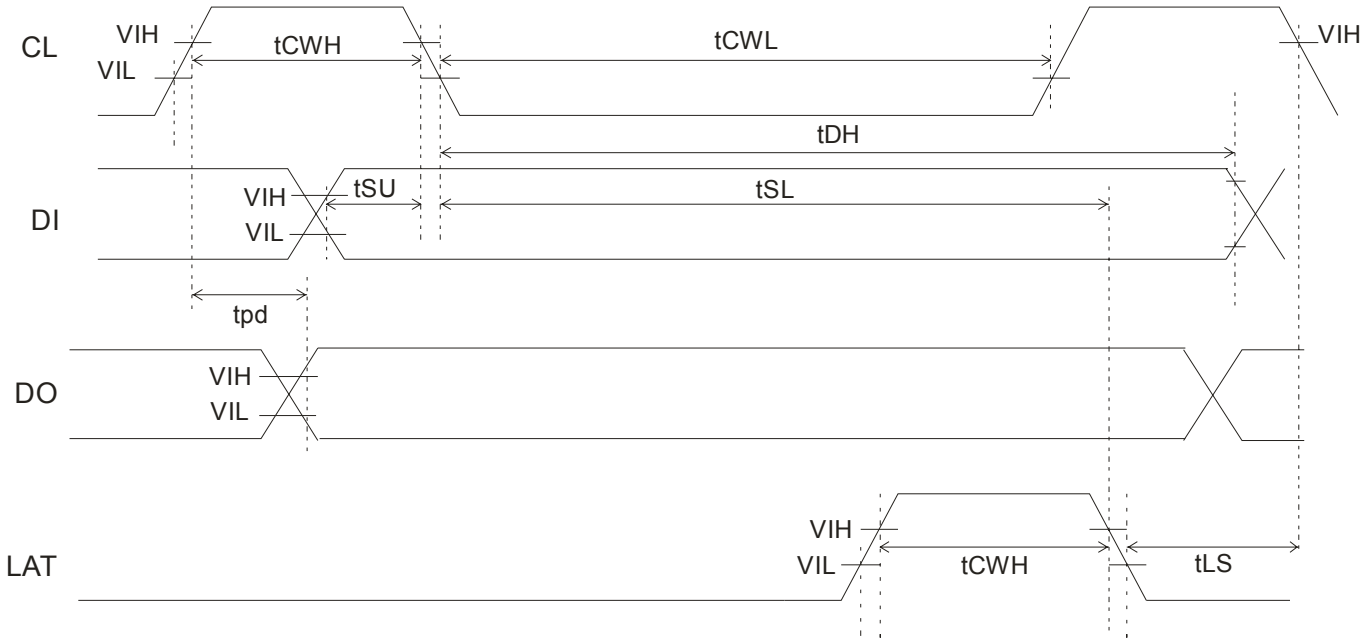
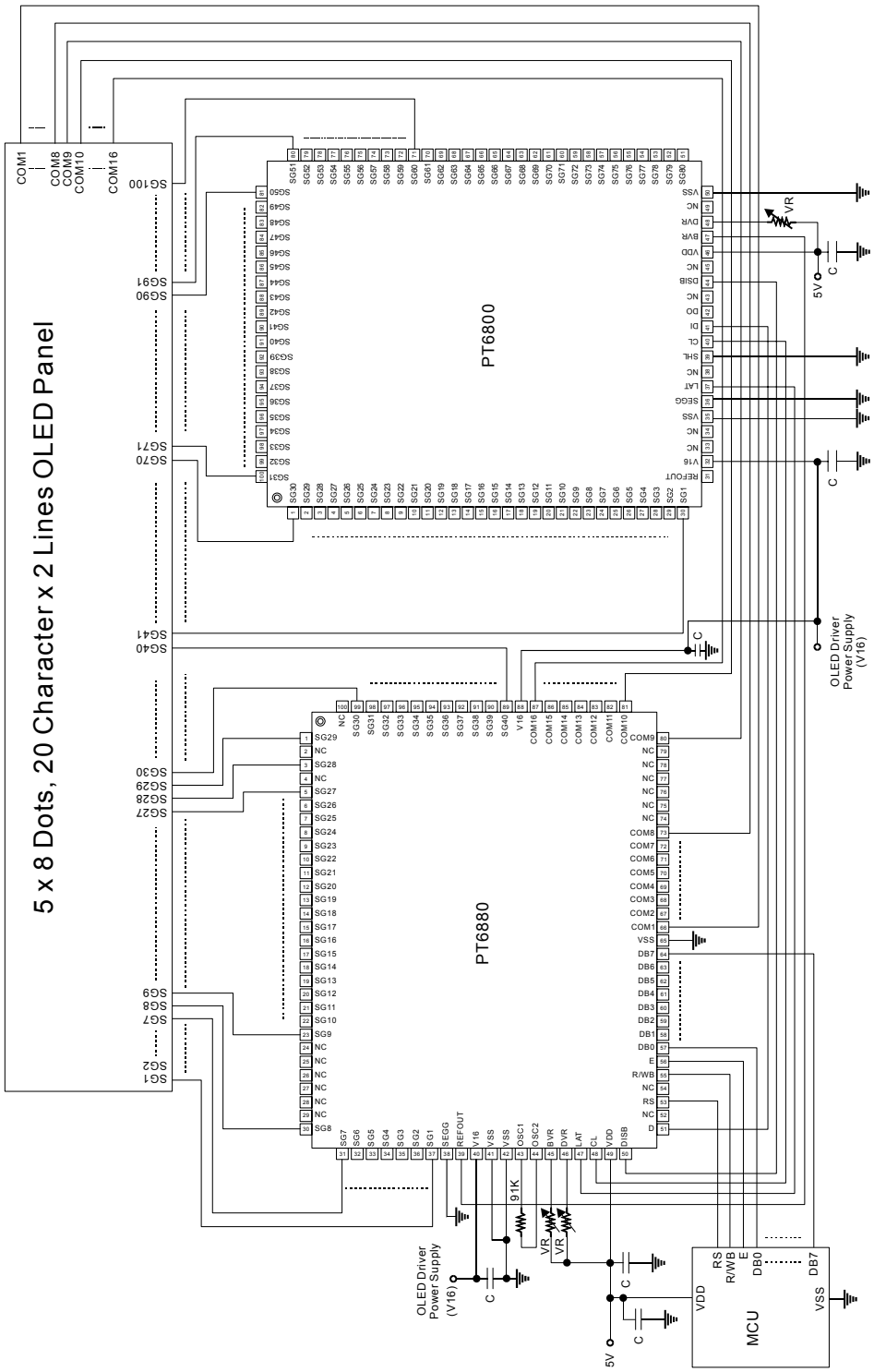
TIMING DIAGRAM



APPLICATION CIRCUIT



Note: VR=100KΩ, C=0.1μF

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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6800	100 Pins, QFP	PT6800
PT6800LQ	100 Pins, LQFP	PT6800LQ

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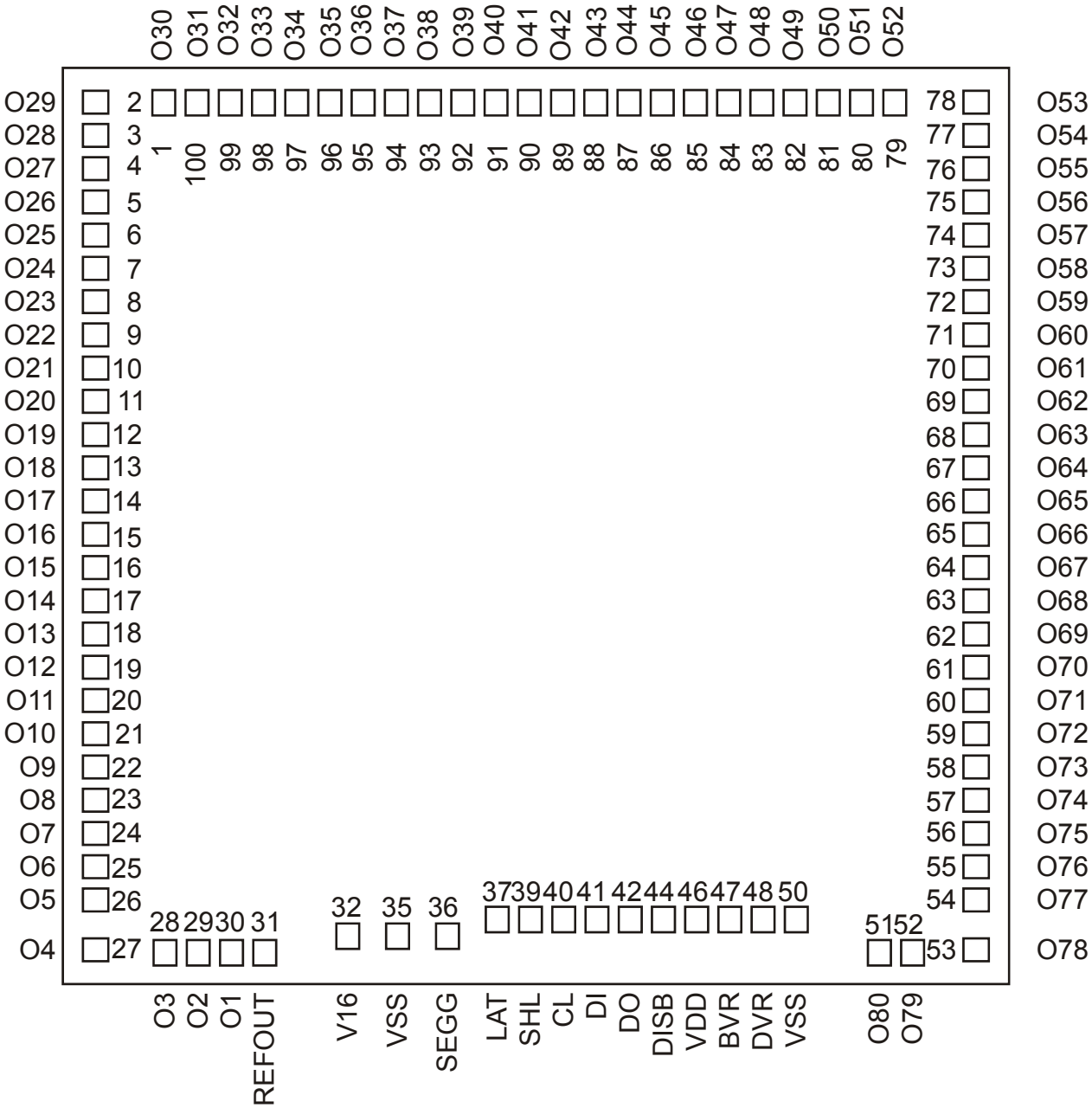
PAD CONFIGURATION



chip size: 3153 x 2793
pad size: 90 x 90
pitch size: 105
unit: μm
P-Substrate: VSS

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PAD LOCATION

Pad No.	Pad Name	Location
1	SG30	[220.200, 2714.500]
2	SG29	[50.000, 2702.300]
3	SG28	[50.000, 2597.300]
4	SG27	[50.000, 2492.300]
5	SG26	[50.000, 2387.300]
6	SG25	[50.000, 2282.300]
7	SG24	[50.000, 2177.300]
8	SG23	[50.000, 2072.300]
9	SG22	[50.000, 1967.300]
10	SG21	[50.000, 1862.300]
11	SG20	[50.000, 1757.300]
12	SG19	[50.000, 1652.300]
13	SG18	[50.000, 1547.300]
14	SG17	[50.000, 1442.300]
15	SG16	[50.000, 1337.300]
16	SG15	[50.000, 1232.300]
17	SG14	[50.000, 1127.300]
18	SG13	[50.000, 1022.300]
19	SG12	[50.000, 917.300]
20	SG11	[50.000, 812.300]
21	SG10	[50.000, 707.300]
22	SG9	[50.000, 602.300]
23	SG8	[50.000, 497.300]
24	SG7	[50.000, 392.300]
25	SG6	[50.000, 287.300]
26	SG5	[50.000, 182.300]
27	SG4	[50.000, 50.000]
28	SG3	[214.500, 50.000]
29	SG2	[319.500, 50.000]
30	SG1	[424.500, 50.000]
31	REFOUT	[529.500, 50.000]
32	V16	[1045.000, 94.700]
33	NC	
34	NC	
35	VSS	[1182.400, 86.300]
36	SEGG	[1340.400, 86.300]
37	LAT	[1509.200, 151.200]
38	NC	
39	SHL	[1619.200, 151.200]
40	CL	[1729.200, 151.200]
41	DI	[1839.200, 151.200]

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Pad No.	Pad Name	Location
42	DO	[1949.200, 151.200]
43	NC	
44	DISB	[2070.700, 151.200]
45	NC	
46	VDD	[2180.700, 151.200]
47	BVR	[2290.700, 151.200]
48	DVR	[2400.700, 151.200]
49	NC	
50	VSS	[2510.700, 151.200]
51	SG80	[2804.900, 50.000]
52	SG79	[2909.900, 50.000]
53	SG78	[3074.400, 50.000]
54	SG77	[3074.400, 182.300]
55	SG76	[3074.400, 287.300]
56	SG75	[3074.400, 392.300]
57	SG74	[3074.400, 497.300]
58	SG73	[3074.400, 602.300]
59	SG72	[3074.400, 707.300]
60	SG71	[3074.400, 812.300]
61	SG70	[3074.400, 917.300]
62	SG69	[3074.400, 1022.300]
63	SG68	[3074.400, 1127.300]
64	SG67	[3074.400, 1232.300]
65	SG66	[3074.400, 1337.300]
66	SG65	[3074.400, 1442.300]
67	SG64	[3074.400, 1547.300]
68	SG63	[3074.400, 1652.300]
69	SG62	[3074.400, 1757.300]
70	SG61	[3074.400, 1862.300]
71	SG60	[3074.400, 1967.300]
72	SG59	[3074.400, 2072.300]
73	SG58	[3074.400, 2177.300]
74	SG57	[3074.400, 2282.300]
75	SG56	[3074.400, 2387.300]
76	SG55	[3074.400, 2492.300]
77	SG54	[3074.400, 2597.300]
78	SG53	[3074.400, 2702.300]
79	SG52	[2904.200, 2714.500]
80	SG51	[2782.200, 2714.500]
81	SG50	[2660.200, 2714.500]
82	SG49	[2538.200, 2714.500]
83	SG48	[2416.200, 2714.500]
84	SG47	[2294.200, 2714.500]

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Pad No.	Pad Name	Location
85	SG46	[2172.200, 2714.500]
86	SG45	[2050.200, 2714.500]
87	SG44	[1928.200, 2714.500]
88	SG43	[1806.200, 2714.500]
89	SG42	[1684.200, 2714.500]
90	SG41	[1562.200, 2714.500]
91	SG40	[1440.200, 2714.500]
92	SG39	[1318.200, 2714.500]
93	SG38	[1196.200, 2714.500]
94	SG37	[1074.200, 2714.500]
95	SG36	[952.200, 2714.500]
96	SG35	[830.200, 2714.500]
97	SG34	[708.200, 2714.500]
98	SG33	[586.200, 2714.500]
99	SG32	[464.200, 2714.500]
100	SG31	[342.200, 2714.500]

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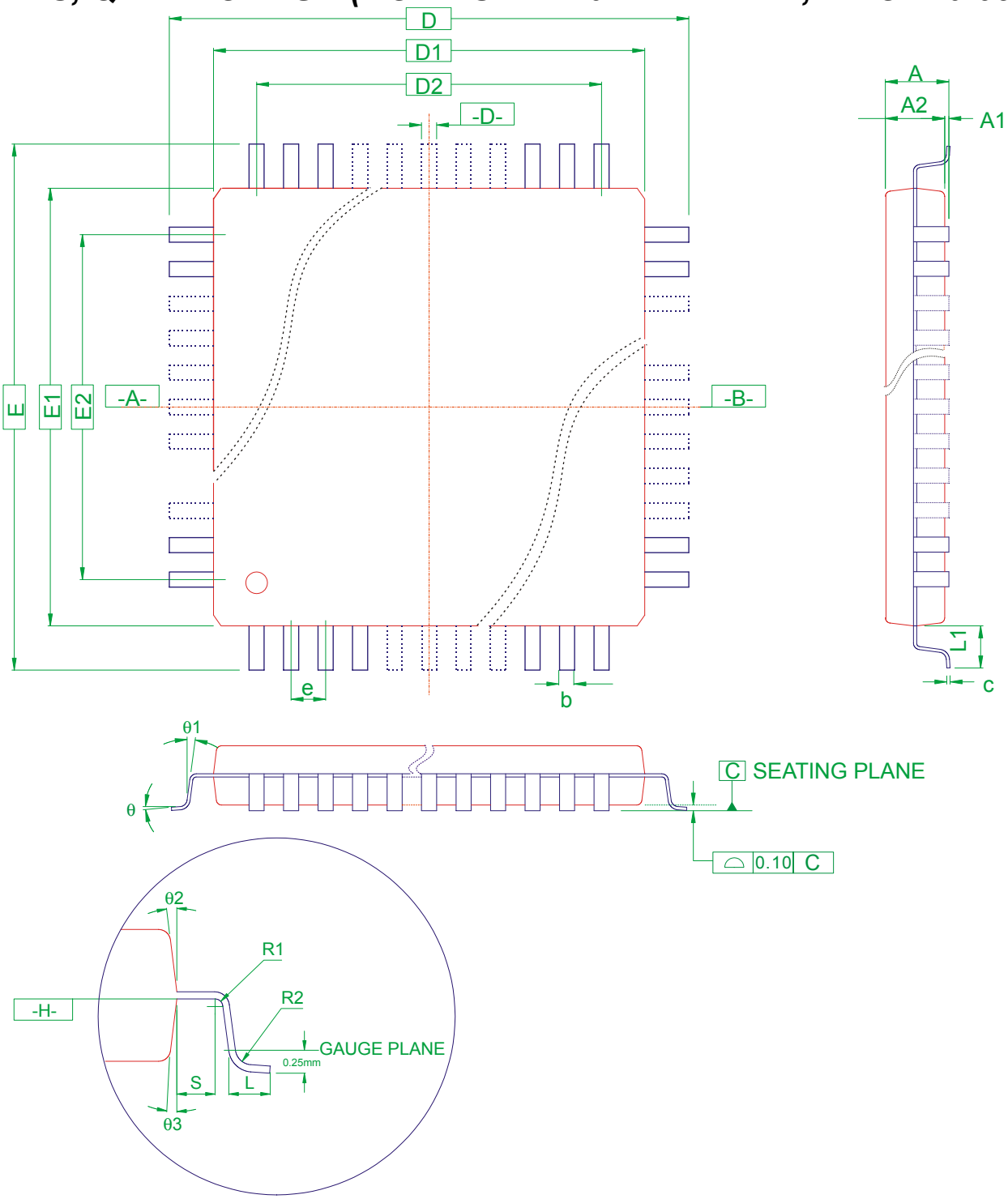
PACKAGE INFORMATION

100 PINS, QFP PACKAGE (BODY SIZE: 20MM X 14MM, PITCH: 0.65MM)



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Symbol	Min.	Nom.	Max
c	0.11		0.23
L	0.73	0.88	1.03
L1		1.60 BSC	
A			3.40
A1	0.25		0.50
A2	2.50	2.70	2.90
b	0.22		0.40
D	23.20 BSC.		
D1	20.00 BSC.		
D2	18.85 REF.		
E	17.20 BSC.		
E1	14.00 BSC.		
E2	12.35 REF.		
e	0.65 BSC.		
S	0.2	-	-
R1	0.13	-	-
R2	0.13	-	0.30
θ	0°	-	7°
θ1	0°	-	-
θ2	5°	-	16°
θ3	5°	-	16°

Notes:
1. All dimensioning and tolerancing dimension conform to ASME Y14.5M-19942.
2. Dimensions “D1” and “E1” do not include mold protrusion, allowable protrusion is 0.25 mm per side.
3. Regardless of the relative size of the upper and lower body sections, dimensions “D1” and “E1” are determined at the largest feature of the body exclusive of mold flash and gate burrs but including any mismatch between the upper and lower sections of the molded body.
4. Controlling Dimensions: Millimeters
5. Dimension “b” do not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed “B” maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
6. Refer to JEDEC MS-022 Variation GC-1.

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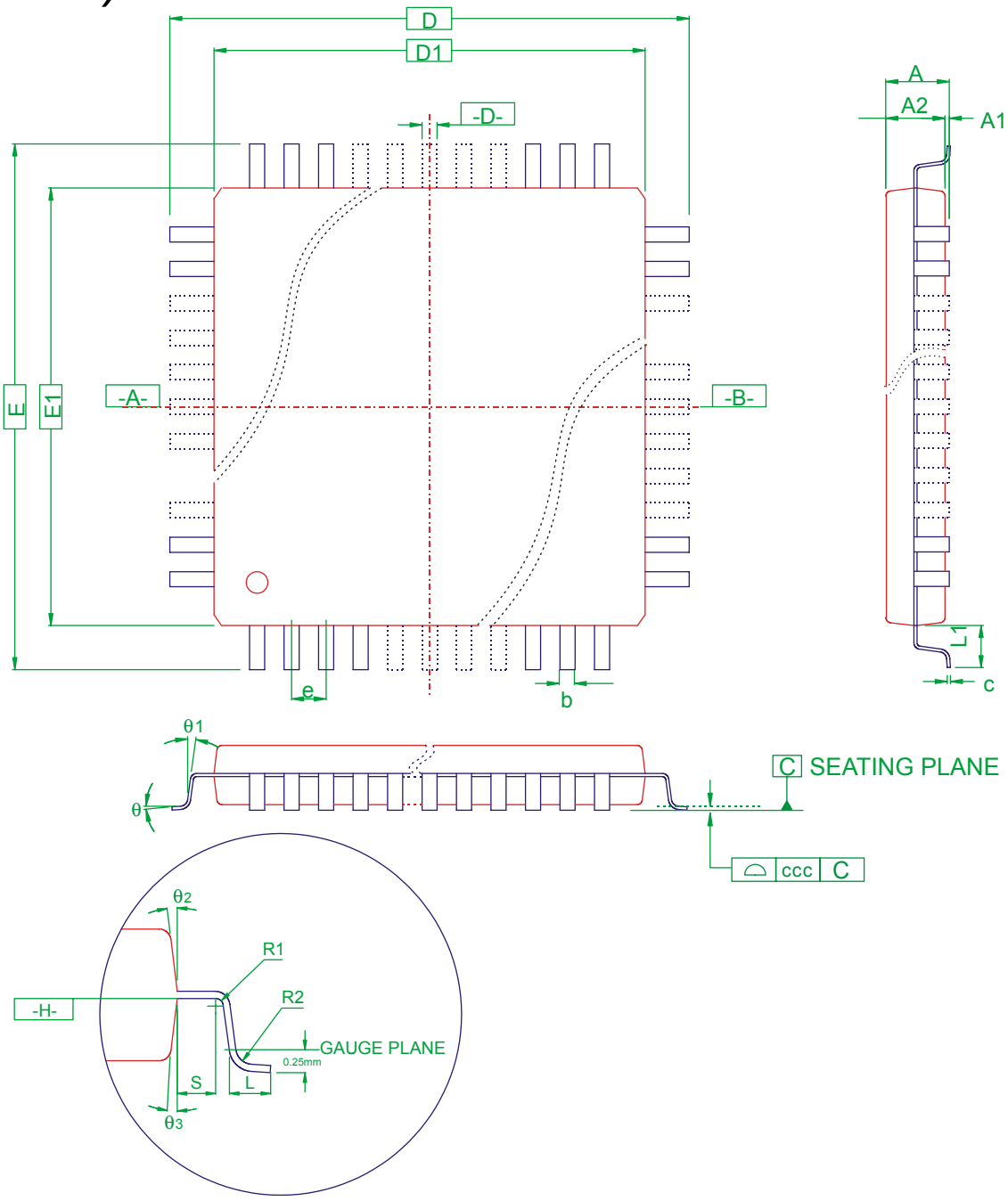
100 PINS, LQFP PACKAGE (BODY SIZE: 14MM X 14MM, PITCH: 0.50MM, THK: 1.40MM)



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Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	.027
D		16.00 BSC.	
D1		14.00 BSC.	
e		0.50 BSC.	
E		16.00 BSC.	
E1		14.00 BSC.	
θ	0^o	3.5^o	7^o
θ1	0^o	-	-
θ2	11^o	12^o	13^o
θ3	11^o	12^o	13^o
C	0.09	-	0.20
L	0.45	0.60	0.75
L1		1.00 REF.	
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
ccc		0.08	

Notes:
1. Dimensioning and tolerancing per ASMEY14.5-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusions is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mismatch.
5. Details of Pin1 identifier are optional but must be located within the zone indicated.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
7. Exact shape of each corner is optional.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Controlling Dimension: Millimeters
10. Refer to JEDEC MS-026 Variation BED

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