RAiO

RA8802/8820

Character/Graphic LCD Controller Specification

Version 1.3

February 2, 2005

RAiO Technology Inc.

Update History		
Version	**Date**	**Description**
1.2	April 26, 2004	First Release Version
1.3	February 2, 2005	Update Figure10-3

Chapter **Table of Contents** **Page**

1. General Description

The RA8802/8820 is a Character/Graphic dot-matrix liquid crystal display controller (LCD) with embedded 512K Byte Font ROM. The RA8802 supports up to 320x240 LCD panel size and RA8820 supports up to 240x160. In tradition, users need a graphic LCM to display Chinese characters. Now Chinese character's display of RA8802/8820 presents a revolution. The RA8802/8820, instead of a MCU, can directly deal with the access of Chinese/English fonts that consist of BIG5 or GB, and ASCII code.

The RA8802/8820 have some main functions as following. It's equipped with 8-bit ADC, supporting touch panel interface. DAC is 5-bit, providing the brightness control of the LCD panel. The RA8802/8820 built in PLL/OSC two circuits provides user choice to generate system clock. The interface of RA8802/8820 fits both of 8080/6800 series' MCU and 4/8-bit data bus. Besides that, the interface of LCD driver is compatible with many types of LCD drivers on the market.

2. Feature

- Dot matrix liquid crystal display controller supporting the display of Character/Graphic.
- Fast Character/Graphical Mode for ASCII & Chinese (Big5 Code and GB Code) support.
- Display Control Capacity →
  RA8802: 320×240 dots (Max), 20×15 full-size character or 40×15 half-size character
  RA8820: 240x160 dots (Max), 15x10 full-size character or 30x10 half-size character
- Display of 16x16 dot for full-size fonts consisting of Chinese, 8x16 dots for half-size fonts of alphanumeric characters and symbols in the same display.
- Clock source: RC Oscillator or 32K crystal for PLL (External 32KHz Crystal need).
- Built-in 9.6Kbyte/4.8Kbyte Display Data RAM
- High-speed 4/8-bit MCU interface allowing direct connection to both the 8080 and 6800.
- LCD interface: LCD driver compatible for data bus 4/8 bit supports.
- Built in 8-Bit ADC and 5-Bit DAC.
- Embedded 512KByte Font ROM and provide 512KByte Font ROM Interface.
  BIG5:
  --Includes standard font: 13094 Chinese words
  --Includes special font: 408 Chinese words
  --Includes two set ASCII codes
  GB:
  --Total font: 7602 Chinese words
- Various instruction functions
  --White black inversion, cursor on/off/blink/bold/cursor height and cursor-width.
  --Define the Work/ Display window address.
- Low Power Consumption
- Operating Voltage →
  _ RA8802: 2.7~4.0V
  _ RA8820: 2.7~5.0V
- Package: DIE, PQFP 100, LQFP 100

3. Block Diagram

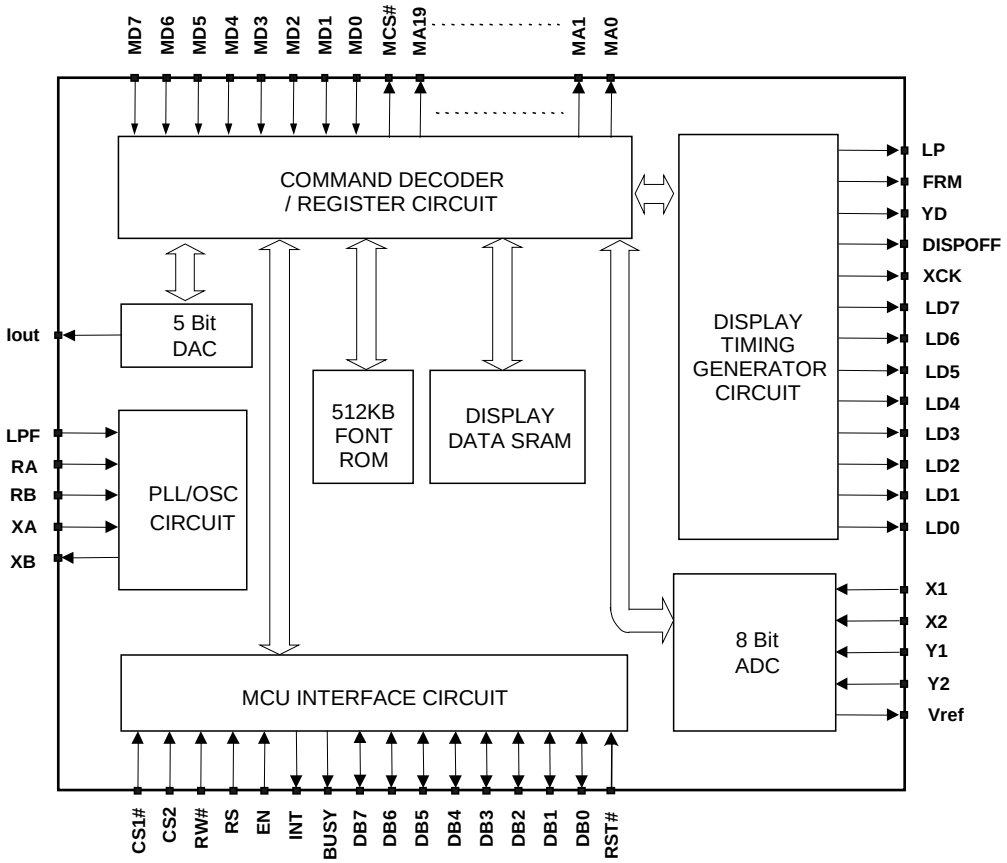

Figure 3-1 Function Block of RA8802/8820

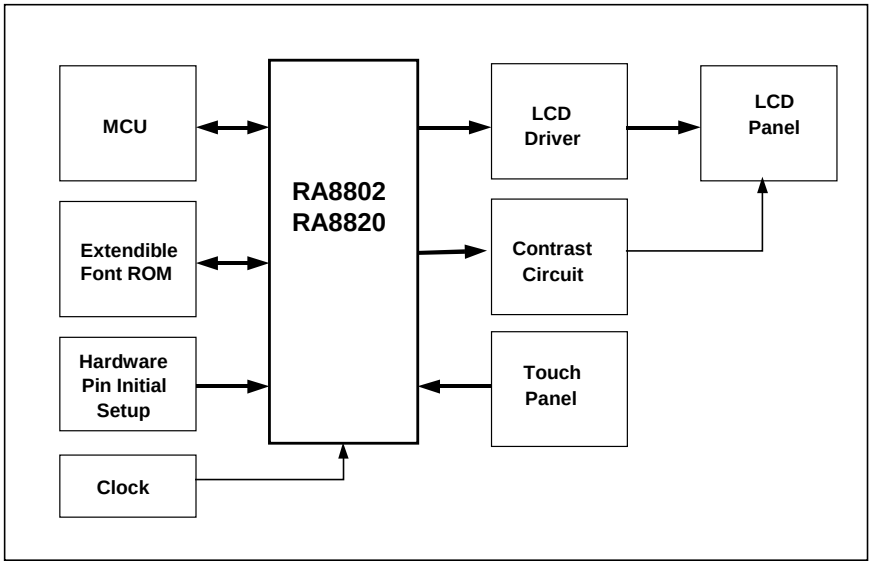

Figure 3-2 System Block

4. Pin Definition

4.1 MCU Interface

Pin name	I/O	Description
DB[7..0]	I/O	Bi-direction 8 bit data bus connected to MCU data bus. The high nibble DB[7..4] should be connected to GND when 4 bit data bus mode is used.
RD# (EN)	I	Active low RD# signal when 8080 MCU is used. Active high EN signal when 6800 series MCU are used.
WR# (R/W#)	I	Active low WR# signal when 8080 MCU is used. The data are latched at the rising edge of the WR# signal. Connected to 6800 series MCU R/W# pin when 6800 MCU is used. The MCU data will be read from RA8802/8820 when R/W# is high and will be written to RA8802/8820 when R/W# is low.
RS	I	Register/Data select pin. Usually connect to MCU address bus A0. The MCU will access Instruction Register when RS is high and access Data Register when RS is low.
CS1# CS2	I	Chip select pin. The RA8802/8820 is active when CS1# is low and CS2 is high
INT	O	Interrupt signal Active high or low Interrupt signal
BUSY	O	Active high or low busy signal. The RA8802/8820 can't be access when BUSY pin is high. It's should be connected to MCU I/O input. The MCU have to poll this pin before accessing RA8802/8820.

4.2 Driver Interface

Pin name	I/O	Description
YD	O	LCD Driver control signal YD will produce a pulse at the starting address of each Frame.
FRM	O	AC-converting signal input for LCD driver waveform. Normally inputs a frame inversion signal The LCD driver output pin's output voltage level can be set to the line latch output signal and the FR signal
LP	O	**For Column:** Latch pulse input pin for display data Data is latched on the falling edge of the clock pulse. **For Row:** Bi-directional shift register shift clock pulse input pin Data is shift on the falling edge of the clock pulse.
XCK	O	Shift clock signal for LCD driver IC. Data is shifted on the falling edge of the XCK.
DISPOFF	O	Display off control signal used to control LCD power supply or backlight. The pin is controlled by LCR bit 2. The status of this pin is the same as LCR bit 2.

LD7 SYS_MI	I/O	Alternative function pin LD7/SYS_MI. It's connected to LCD driver IC D7, when 8-bit LCD driver IC is used. SYS_MI is for MCU type selection. It's active on reset period. Non-Pull when 6800 MCU is used. Pull low when 8080 MCU series are used.
LD6 SYS_DB	I/O	Alternative function pin LD6/SYS_DB. It's connected to LCD driver IC D6, when 8-bit LCD driver IC is used. SYS_DB is for MCU data bit selection. Non-Pull when 8-bit MCU is used. Pull low when 4-bit MCU is used. The high nibble data bus DB[7..4] Should tied to GND When 4-bit MCU is used.
LD5 SYS_FQ	I/O	Alternative function pin LD5/SYS_FQ. It's connected to LCD driver IC D5, when 8-bit LCD driver IC is used. SYS_FQ is for RA8802/8820 clock source selection. Non-Pull will enable internal PLL circuit and X'tal will be the clock source of RA8802/8820. Pull low when RC oscillator is used and it will disable internal PLL.
LD4	I/O	LD4 It's connected to LCD driver IC D4. When 8 bit LCD driver IC is used.
LD3 SYS_LD	I/O	Alternative function pin LD3/SYS_LD. This pin is connected to D3 pin of LCD driver IC. SYS_LD is for LCD driver data bus selection. Non-Pull when 8-bit LCD driver is used. Pull low when 4-bit LCD driver is used.
LD2 SYS_PLR	I/O	It's connected to LCD driver IC D2. SYS_PLR is polarity select. It's connected to LCD driver IC D2. SYS_PLR is for RS polarity selection. When Non-Pull, then "RS" = 0 means Register Access Cycle, and "RS" = 1 means Data Access Cycle. When Pull Low, then "RS" = 1 means Register Access Cycle, and "RS" = 0 means Data Access Cycle.
LD1 OPM1	I/O	Alternative function pin LD1/OPM1. It's connected to LCD driver IC D1. OPM1 and OPM0 are used to choose the test model of RA8802/8820. Do not Pull-Low for this pin.
LD0 OPM0	I/O	Alternative function pin LD0/OPM0. It's connected to LCD driver IC D0. OPM1 and OPM0 are used to choose the test model of RA8802/8820. Do not Pull-Low for this pin.

4.3 Clock Interface

Pin name	I/O	Description
XA	I	Oscillator Input. This is the input signal of internal oscillator. Normally it connects to a 32768Hz X'tal. The XA, XB and LPF are used for X'tal and internal PLL. If in RC_OSC mode, then XA, XB and LPF should be Floating.
XB	O	Oscillator Output. This is the output signal of internal oscillator. Normally it connects to a 32768Hz X'tal.

LPF	I	LPF (Low Pass Filter) Input. This input is used for internal PLL circuit.
RA	I	Connect Resistance. The RA, RB are used for RC-Oscillator mode. If in X'tal/PLL mode then RA and RB should be Floating.
RB	I	Connect Resistance.

4.4 Power Signal

Pin name	I/O	Description
VDD	I	Power supply
GND	I	Power ground
AVDD	I	Analog power supply signal.
AGND	I	Analog ground.

4.5 Misc. Signal

Pin name	I/O	Description
RST#	I	Active low reset signal. (The reset pulse do not less than 100mS after MCU stable)
X1	I	Normally connected to touch panel Left pin XL.
X2	I	Normally connected to touch panel Right pin XR.
Y1	I	Normally connected to touch panel Top pin YU.
Y2	I	Normally connected to touch panel Bottom pin YD.
Iout	O	DAC current source output used to contrast voltage control.
Vref	O	ADC voltage reference signal.
MA[19..0]	O	20-bit Address Bus connected to the address bus of external character pattern ROM. **Note: MA0 need to be Pulled High (10K)** If do not use the external Font ROM, the MA[7:0] should tied to VDD to reduce the power consumption.
MCS#	O	Character pattern ROM chip select and output enable
MD[7..0]	I	8-bit Data Bus connected to the data bus of external character pattern ROM. Note: If do not use the external Font ROM, the MD[7:0] should tied to VDD to reduce the power consumption.
SEL0	I	Test pin must be tied to GND for normal use.
SEL1	I	Test pin must be tied to VDD for normal use.

5. Register Description

5.1 Register List Table

Table 5-1

Reg. No	Reg. Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	LCR	R/W	PW1	PW2	SR	RTM	CG	DP	DK	DV
08h	MIR	R/W	ABP	CKN	DISP	PLR	--	--	CKB1	CKB0
10h	CCR	R/W	ARI	ALG	WDI	WBC	AIX	CP	CK	CSD
18h	CSCR	R/W	CR3	CR2	CR1	CR0	DY3	DY2	DY1	DY0
20h	AWRR	R/W	--	--	X5	X4	X3	X2	X1	X0
28h	DWRR	R/W	--	--	A5	A4	A3	A2	A1	A0
30h	AWBR	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
38h	DWBR	R/W	B7	B6--	B5	B4	B3	B2	B1	B0
40h	AWLR	R/W	--	--	SS5	SS4	SS3	SS2	SS1	SS0
48h	DWLR	R/W	--	--	C5	C4	C3	C2	C1	C0
50h	AWTR	R/W	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
58h	DWTR	R/W	D7	D6	D5	D4	D3	D2	D1	D0
60h	CPXR	R/W	--	--	RS5	RS4	RS3	RS2	RS1	RS0
70h	CPYR	R/W	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
80h	BTR	R/W	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0
90h	SCCR	R/W	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0
A0h	INTR	R/W	BSY	INA	INX	INY	MSZ	MSA	MSX	MSY
B0h	INTX	R/W	--	--	IX5	IX4	IX3	IX2	IX1	IX0
B8h	INTY	R/W	IY7	IY6	IY5	IY4	IY3	IY2	IY1	IY0
C0h	TPCR	R/W	AZEN	AZOE	--	ADET	AS3	AS2	AS1	AS0
C8h	TPDR	R	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
D0h	LCCR	R/W	DZEN	DZWE	DRST	DAC4	DAC3	DAC2	DAC1	DAC0
E0h	PDR	R/W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
F0h	FCR	R/W	TNS	BNK	RM1	RM0	FDA	ASC	ABS1	ABS0

5.2 Register Description

REG [00h] LCD Controller Register (LCR)

Bit	Description	Text/Graph	Default	Access
7-6	Power Mode 11: Normal Mode 10: Standby Mode 01: Sleep Mode 00: Off Mode **Normal mode:** When RA8802/8820 is in normal mode it can execute full functions include RAM read/write, register read/write, LCD display valid signal.	--	11h	R/W

	Standby mode: When RA8802/8820 is in standby mode, except DDRAM/ROM access function is prohibited, others are working and so does LCD display function. **Sleeping mode:** When RA8802/8820 is in sleeping mode, the DDRAM/ROM access and LCD display are prohibited, but register access is permitted. **Off mode:** When RA8802/8820 is in off mode, all above functions enter power-off mode, except the wake-up trigger block. If wake-up event occurred, RA8802/8820 would wake-up and return to Normal mode.			
5	Software Reset: 1: Reset all registers except flushing RAM 0: Normal operation	--	0h	R/W
4	Set Auto_reset function When the bit is Enable, if RA8802/8820 doesn't get a full command or data within 2msec, then RA8802/8820 will ignore it. 1: Enable Auto_reset function 0: Disable Auto_reset function	--	0h	R/W
3	Display mode selection 1: Character mode The written data will be treated as a GB/BIG/ASCII code. 0: Graphical mode The written data will be treated as a bit-map pattern.	--	1h	R/W
2	Set Display on or off. The bit can control LCD Driver Interface signals DISP_OFF signal control 1: DISP_OFF pin output high 0: DISP_OFF pin output low.	Text/Graph	0h	R/W
1	Blink mode selection 0: Normal display 1: Blink full screen. The blink time is set by CBTR.	Text/Graph	0h	R/W
0	Inverse mode selection 1: Normal display 0: Inverse full screen. It will cause all data stored in DDRAM inversed.	Text/Graph	1h	R/W

REG [10h] Cursor Control Register (CCR)

Bit	Description	Text/Graph	Default	Access
7	Auto Increase Cursor Position in reading DDRAM operation. 1: Enable 0: Disable	Text/Graph	1h	R
6	Chinese/English character alignment 1: Enable 0: Disable The bit only valid in character mode, that can align full-size and half-size mixed font	Text	1h	R/W
5	Store Current Data to DDRAM 1: Store Current Data to DDRAM directly 0: Store Current Data to DDRAM Inversely	Text	1h	R/W
4	Set Bold font (character mode only) 1: Store Data shift 1 + origin data (Black Font) 0: Store Data Normality (origin Font)	Text/Graph	1h	R/W
3	Auto Increase Cursor Position in writing DDRAM operation. 1: Enable 0: Disable	Text/Graph	0h	R/W
2	Cursor display control 1: Set cursor on 0: Set cursor off	Text/Graph	0h	R/W
1	Cursor blink control 1: blink Cursor. The blink time is determined by register[80h] BTR 0: Normal	Text/Graph	0h	R/W
0	Set Cursor width 1: Cursor width is auto adjust by input data 0: Cursor is fixed at one byte width	Text	0h	R/W

REG [20h] Active Window Right Register (AWRR)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	Active window right position → Segment-Right	xxh	R/W

Note: REG [20h, 30h, 40h, 50h] are used for the function of change line and page. Users can use these four Registers to set a block as an active window. When data goes beyond the right boundary of active window (The value is set by REG [20h, 30h, 40h, 50h]), then the cursor will automatically change the line and write in data continuously. It means the cursor will move to the left boundary of active window, which is set by REG [40h]. When the data comes to the bottom line of the right side (set by REG [20h and 30h]), then the cursor

will be moved to the first line of the left side automatically and continue to put in data. (set by REG [40h, 50h]).

REG [30h] Active Window Left Register (AWBR)

Bit	Description	Default	Access
7-0	Active window bottom position → Common-Bottom	xxh	R/W

REG [40h] Active Window Bottom Register (AWLR)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	Active window left position → Segment-Left	0h	R/W

REG [50h] Active Window Top Register (AWTR)

Bit	Description	Default	Access
7-0	Active window top position → Common-Top	0h	R/W

REG [60h] Cursor Position X Register (CPXR)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	Set the cursor Segment address	0h	R/W

REG [70h] Cursor Position Y Register (CPYR)

Bit	Description	Default	Access
7-0	Set the cursor Common address	0h	R/W

REG [80h] Cursor Blink Time Register (BTR)

Bit	Description	Text/Graph	Default	Access
7-0	The Blink one unit time scale is the frame rate scale **Blinking time = BTR Bit [7..0] x (1/Frame_Rate)** Frame Rate setup depends on the LCD panel.	Text/Graph	23h	R/W

REG [90h] Shift Clock Control Register (SCCR)

Bit	Description	Default	Access
7-0	Setup the XCK signal cycle **SCCR = (SCLK*4)/(Column*Row*FRS)** SCLK: System Clock (Hz) DBW: 4(Bit)	--	R/W

	Column: Column of Display Screen (Pixel) Row: Row of Display Screen (Pixel) FRS: Frame Rate/Sec		

REG [A0h] Interrupt Setup & Status Register (INTR)

Bit	Description	Default	Access
7	Busy Status 1: RA8802/8820 is busy. The MCU have to wait until Busy Status is released 0: RA8802/8820 is idle ready for MCU access.	0h	R
6	Touch Panel detect 1: Touch Panel touched 0: Touch Panel untouched	0h	R
5	Cursor Column status 1: The Cursor Column is equal to INTX 0: The Cursor Column is not equal to INTX	0h	R
4	Cursor Row status 1: The Cursor Row is equal to INTY 0: The Cursor Row is not equal to INTY	0h	R
3	Busy interrupt mask 1: Enable Busy to generate Interrupt output 0: Disable Busy to generate Interrupt output	0h	R/W
2	Touch Panel interrupt mask 1: Generate interrupt output if touch panel was detected. 0: Don't generate interrupt output if touch panel was detected.	0h	R/W
1	INTX event occur INT or not 1: Enable INTX Interrupt 0: Disable INTX Interrupt	0h	R/W
0	Set INTY occur INT or not 1: Enable INTY Interrupt 0: Disable INTY Interrupt	0h	R/W

REG [B0h] Interrupt Column Setup Register (INTX)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	Setup Interrupt Column Address If Cursor Position X Register (CPXR)=INTX, a interrupt has occurred	27h	R/W

REG [B8h] Interrupt Row Setup Register (INTY)

Bit	Description	Default	Access
7-0	Setup Interrupt Row Address If Cursor Position Y Register (CPYR)=INTY, a interrupt has occurred	EFh	R/W

REG [C0h] Touch Panel Control Register (TPCR)

Bit	Description	Default	Access
7	Touch Panel function active 1: Disable 0: Enable	1h	R/W
6	Touch Panel Data Output 1: Disable the Touch Panel Data Output 0: Enable the Touch Panel Data Output	1h	R/W
5	Reserved	0h	R/W
4	Touch Event status. 1: No Touch Event. 0: Touch Event occur	1h	R
3-0	Touch Panel control bit The operation flowchart shown as Fig 6-6 Bit3 = 0 → Switch SW3 OFF, Bit3 = 1 → Switch SW3 ON Bit2 = 0 → Switch SW2 OFF, Bit2 = 1 → Switch SW2 ON Bit1 = 0 → Switch SW1 OFF, Bit1 = 1 → Switch SW1 ON Bit0 = 0 → Switch SW0 OFF, Bit0 = 1 → Switch SW0 ON	Fig 6-6	R/W

REG [C8h] Touch Panel Data Register (TPDR)

Bit	Description	Default	Access
7-0	This register keeps the touch panel active position (Column, Row)	0h	R

REG [D0] LCD Contrast Control Register (LCCR)

Bit	Description	Default	Access
7	LCD contrast control 1: Disable 0: Enable	1h	R/W
6	LCD contrast control DAC write enable 1: Don't allow MCU to write data to DAC Bit [4~0] 0: Allow MCU to write data to DAC Bit [4~0]	1h	R/W
5	Reset LCD contrast control function 1: Normal operation	1h	R/W

	0: DAC is reset. Set the Iout to 0 uA		
4-0	Set the LCD Brightness Control Iout Value (DAC Bit [4~0]) 00000b → 0μA (Min. Current) : : 11111b → 1mA (Max. Current)	0h	R/W

REG [E0h] Pattern Data Register (PDR)

Bit	Description	Text/Graph	Default	Access
7-0	Setup the Pattern Data When REG[F0h] bit3 is '1', it will read the data from Register [E0h] and fill the whole DDRAM. After the movement of filling the Active window, REG [F0h] bit3 will become "0".	Graph	0h	R/W

REG [F0h] Font Control Register (FCR)

Bit	Description	Text/Graph	Default	Access
7	External Character ROM control 1: Enable. 0: Disable.	--	1h	R/W
6	ROM BANK Selection 1: External Font ROM select 0: Internal Font ROM select	--	0h	R/W
5-4	Set Font ROM Translate 01: Support BIG5 font ROM 10: Support GB font ROM	--	00h	R/W
3	Fill Data to DDRAM 1: no action 0: Fill Data to DDRAM Enable	Graph	0h	R/W
2	Font ROM range select 1: Enable 0: Disable When the bit is '1', input data is ASCII code then output as symbol When the bit is '0', input data is GB/BIG5 code then output as character.	--	0h	R/W
1-0	ASCII Block Select bit 1~0 0 0: Map to ASCII block 0 0 1: Map to ASCII block 1	--	00h	R/W

	1 0: Map to ASCII block 2 1 1: Map to ASCII block 3			

REG [08h] Misc. Register (MIR)

Bit	Description	Default	Access
7	Reserved	1h	R
6	Enable CLK_OUT 1: Enable CLK_OUT 0: Disable CLK_OUT	1h	R/W
5	Window Mode Select 1: Active_ window 0: Display_ window	0h	R/W
4	Set INT and Busy Polarity 1: Set High_ Active mode 0: Set Low_ Active mode	0h	R/W
3-2	Reserved	0h	R
1-0	Clock speed selection 0 0：1MHz 0 1：2MHz 1 0：4MHz 1 1：8MHz		

REG [18h] Cursor Size Control Register (CSCR)

Bit	Description	Text/Graph	Default	Access
7-4	Setup the height of cursor (default value is 2)	Text	0010h	R/W
3-0	Setup the distance of row to row	Text	0010h	R/W

REG [28h] Display Window Right Register (DWRR)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-0	Set Display Window Right position → Segment-Right **Segment-Right = (Segment Number / 8) – 1** RA8802: If LCD panel size is 320x240, the value of the register is: (320 / 8) - 1 = 39 = 27h RA8820: If LCD panel size is 240x160, the value of the register is: (240 / 8) - 1 = 29 = 1Dh	xxh	R/W

Note: REG[28h, 38h, 48h, 58h] is used to set Display Window。 Users can set the viewing scope of Display RAM. For RA8802, the Column Address can be set between 0~39, and Row Address can be set between 0~239. For RA8820, the Column Address can be set between 0~29, and Row Address can be set between 0~159. Users can set start and end address first, and then by adding shift function to present the effect of rolling.

REG [38] Display Window Bottom Register (DWBR)

Bit	Description	Default	Access
7-0	Display Window Bottom position → Common-Bottom **Common_ Bottom = LCD Common Number –1** RA8802 : If LCD Panel is 320x240, the value of the register is: 240 – 1 = 239 = EFh RA8820 : If LCD Panel is 240x160, the value of the register is: 160 – 1 = 159 = 9Fh	xxh	R/W

REG [48] Display Window Left Register (DWLR)

Bit	Description	Default	Access
7-0	Display Window Left position → Segment-Left Usually set “00h”.	0h	R/W

REG [58] Display Window Top Register (DWTR)

Bit	Description	Default	Access
7-0	Display Window Top position → Common-Top Usually set “00h”.	0h	R/W

Note:

Please look at this example of how to set the default value of the Register.

1. AWRR≧CPXR≧AWBR, AWRR≧INTX≧AWBR
2. AWLR≧CPYR≧AWTR, AWLR≧INTY≧AWTR

6. Function Description

6.1 MCU Interface

The RA8802/8820's MCU interface support Intel (8080) or Motorola (6800) 4/8 bits data bus. Users could use SYS_MI to control. Non-Pull when 6800 MCU is used. Pull low when 8080 MCU series are used.

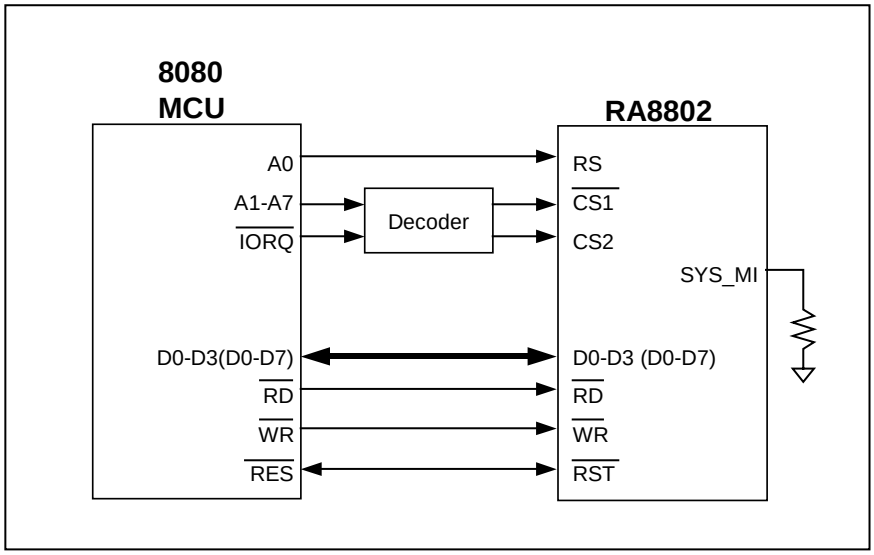

Figure 6-1：8080 (4/8-bit) MCU Interface Diagram

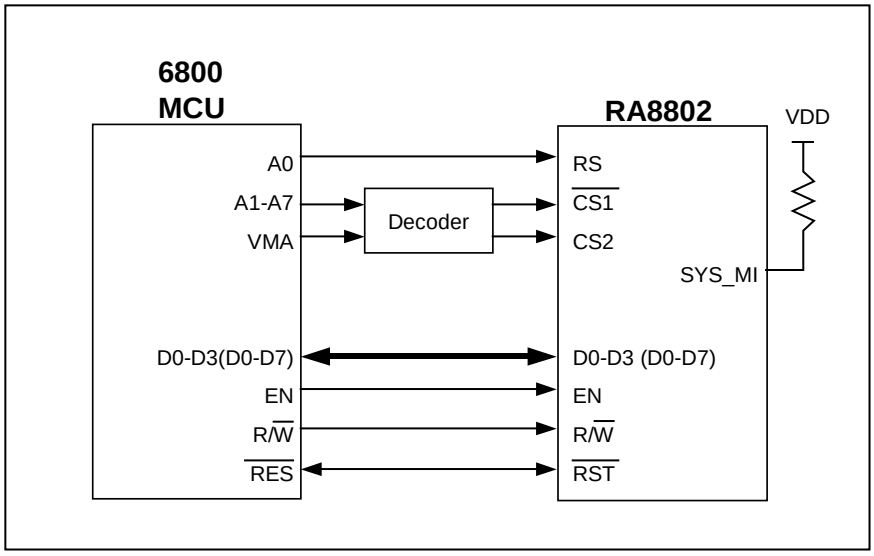

Figure 6-2：6800 (4/8-bit) MCU Interface Diagram

6.2 Command/Decoder register circuit

This circuit store and implement the command from MCU Interface. The Register [00h, 08h, 10h] treats the whole chip and cursor setup. The Register [20h, 30h, 40h, 50h] can setup the work range maximum

and minimum limit. When appreciate setup with Register [10h] bit3, [F0h] bit3 and [60h, 70h] the RA8802/8820 can offer powerful variety meet various application.

The Register [28h, 38h, 48h, 58h] of RA8802 can satisfy various LCD display from (0,0)~(320,240) pixels. The Register [28h, 38h, 48h, 58h] of RA8820 can satisfy various LCD display from (0,0)~(240,160) pixels. Powerful INT via Register [A0h, B0h, B8h] reduce MCU polling cycle to Interrupt interactive utility. Therefore we can use low end MCU to cost down and help the whole system reduce BOM cost.

6.3 Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores bit mapping pixel data and display attribute codes for displaying data. A full-size font is displayed using two bytes, and a half-size font is displayed using one byte. DDRAM displays only that data stored within the range corresponding to the DDRAM. Data stored outside the range is ignored. Refer to combined display of full-size and half-size characters for details on character codes stored in DDRAM.

The display data RAM stores pixel data for LCD. For RA8802, it is a 320 column by 240 row addressable array maximum. For RA8820, it is a 240 column by 160 rows. The time required to transfer data is very short. The microprocessor writes and reads data to/from the RAM through data bus. As the LCD controller operates independently, data can be written into the RAM at the same time as the data is being displayed, without the LCD to flicker. If apply to the character/graphical mix mode. RA8802/8820 can easy store and display the data/picture which user desired.

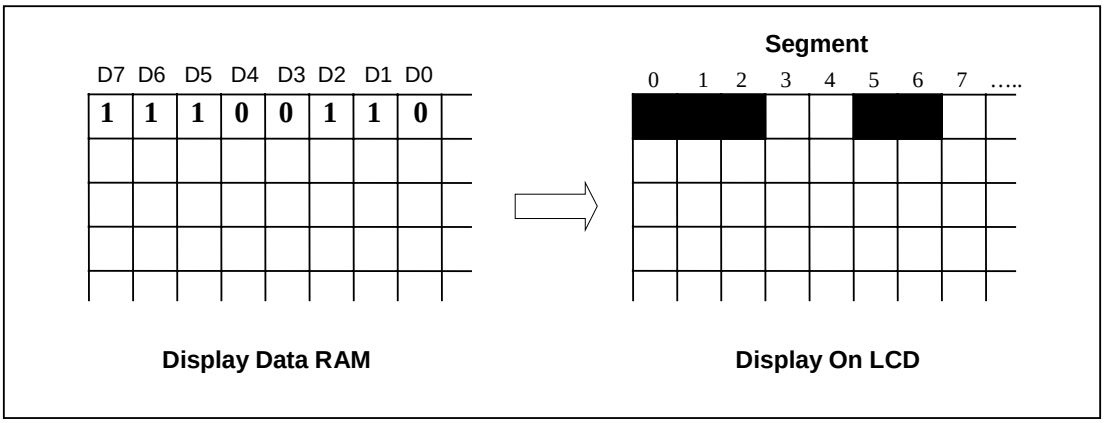

Figure 6-3 Display data to LCD map

6.4 Display Timing Generator

The main function is to generate Frame (FRM), Latch Pulse (LP), YD and Data Bus signals for external LCD driver IC. RA8802/8820 could both support 4-bit and 8-bit LCD driver interface. SYS_LD is for LCD driver data bus selection. Non-Pull when 8-bit LCD driver is used. Pull low when 4-bit LCD driver is used.

6.5 LCD Display

The RA8802 supports up to 320x240 LCD Panel, and RA8802 supports up to 240x160. Users could

setup the Register to change the size of the Display Panel.

6.6 ROM

RA8802/8820 embedded 512KByte Font ROM also provide external 512KByte Font ROM Interface can use put the standard and special fonts of BIG5, GB, and ASCII code. It can support the display 16x16 dot for full-size fonts consisting of Chinese, 8x16 dots for half-size fonts of alphanumeric characters and symbols in the same display. For example, when MCU sends Big5 code (2 Bytes), RA8802/8820 will read Font code (32 Bytes) from ROM, which is matching with Big5 code, and then deliver them to DDRAM.

6.7 PLL/OSC Circuit

The internal system clock of RA8802/8820 is generated from the following way:

- Use an external 32768Hz X'tal and internal PLL circuit
- Use an external Resistor for internal RC-Oscillator

The pin SYS_FQ is for RA8802/8820 clock source selection. Non-Pull will enable internal PLL circuit and X'tal will be the clock source of RA8802/8820. Pull low when RC oscillator is used and it will disable internal PLL.

The Figure 6-4 is the application circuit of clock. If select RC Oscillator mode, then pin XA, XB and LPF should be floating. If X'tal and PLL mode is selected, then RA and RB should be floating.

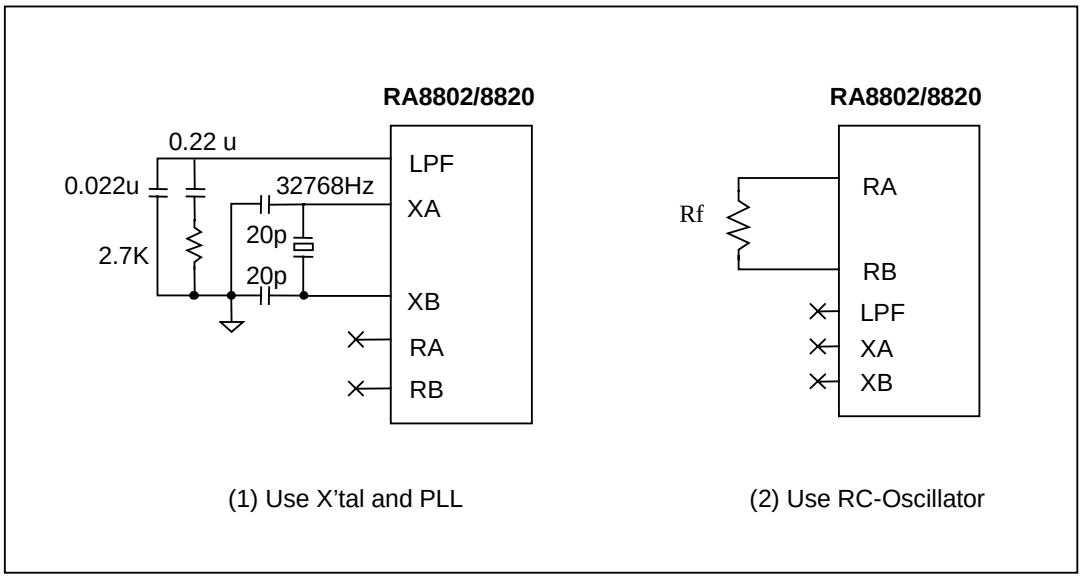

Figure 6-4 PLL & RC OSC Application Circuit

Note: The oscillator frequency can be adjusted by an oscillator resistor(Rf). If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases.

6.8 DAC

RA8802/8820 is built-in one 5-bit fixed current type Digital-to-Analog Converter (D/A). Because DAC will generate different current output, users can make use of it to control external boost circuit and let the voltage level which supply to LCD Panel will be changed by different setup of DAC. Then users can use program to control the brightness of LCD through MCU.

6.9 ADC

The RA8802/8820 built in 8 Bit ADC and control circuits to easily interface to 4-write analog resistive touch screens. The RA8802/8820 continually monitors the screen waiting for a touch. When the screen is touched, the RA8802/8820 performs analog to digital conversion to determine the location of the touch, stores the X and Y locations in the registers, and can issues an interrupt.

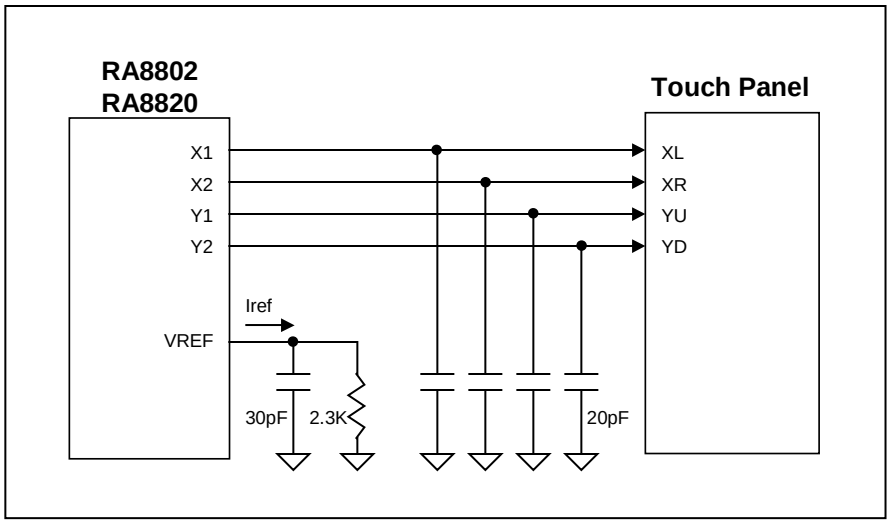

Figure 6-5: Application Circuit of Touch Panel

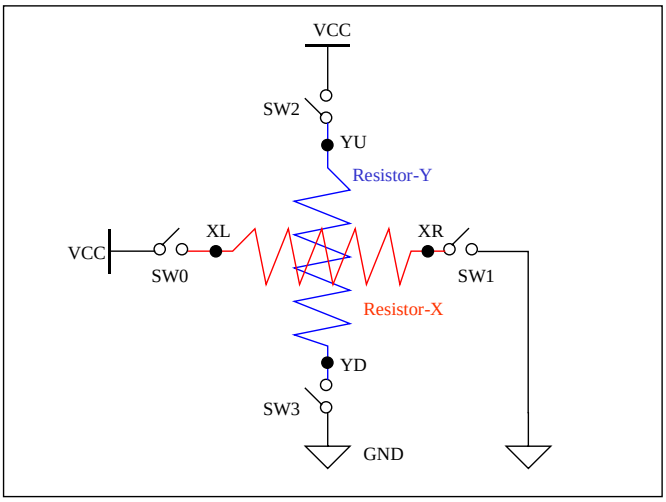

Figure 6-6: Touch Panel and detection switch

6.10 Interrupt and Busy Flag

RA8802/8820 provides an Interrupt signal (INT) to indicate three possible interrupts:

- If Cursor Position X Register (CPXR)=INTX, a interrupt has occurred
- If Cursor Position Y Register (CPYR)=INTY, a interrupt has occurred
- Interrupt occurs when Touch Panel is touched

These three interrupts can be enabled or disabled respectively. REG [A0h] INTR controls the setup of Interrupts. RA8802/8820 provides a Busy signal. When BUSY Flag is "1", which means RA8802/8820 is in busy status, so RA8802/8820 couldn't access data of DDRAM but still accept the commands from registers. This BUSY pin should be connected to MCU I/O input, and then MCU have to poll this pin before accessing RA8802/8820.

6.11 Power Saving Mode

The RA8802/8820 has four operation mode → Normal Mode, Standby Mode, Sleep Mode and Off Mode. Please refer to the register [00h] LCR of Chapter 5.2.

6.12 ASCII Block Selection

The RA8802/8820 built-in four blocks of ASCII Font. It including many special symbols that for users display. This feature is set by Bit[1:0] of Register [F0h]. If user want to create their special symbol or picture then it's possible to make new ROM Code.

7. Function Application

7.1 Character Mode

The Figure 7-1 shows the ability of RA8802/8820 to show Full-Size and Half-Size Characters

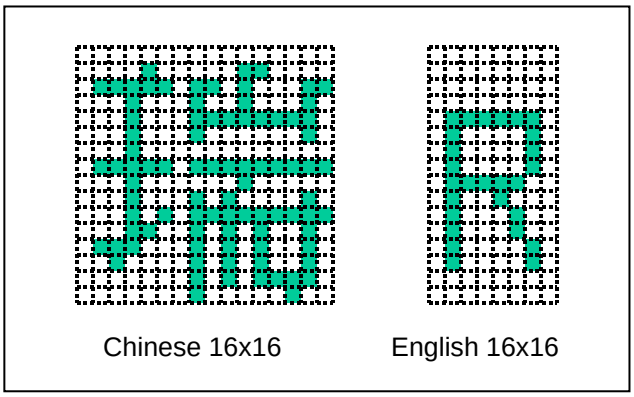

Figure 7-1：Full size and Half size character

Figure 7-2 Combined Display of Full-Size and Half-Size Characters

Table 7-1 is the character code of Full-Size and Half-Size showed in Figure 7-1.

Table 7-1 Character Code comparison table (BIG5)

Display Character	Character Code	Display Character	Character Code	Display Character	Character Code
瑞	B7E7	E	45	o	6F
佑	A6F6	C	43	c	63
科	ACEC	H	48	m	6D
技	A7DE	N	4E	t	74
股	AAD1	L	4C	電	20B7
份	A5F7	G	47	話	71B8
有	A6B3	Y	59	8	38
限	ADAD	.	2E	6	36

公	A4BD	網	BAF4	3	33
司	A571	頁	ADB6	5	35
R	52	:	3A	7	37
A	41	w	77	傳	20B6
I	49	r	72	真	C7AF
O	4F	a	61		
T	45	i	69		

7.2 Characteristic Bold Display Function

The Figure 7-3 is character bold display and Register setup.

1. Set REG [10h] bit4=1
2. Write in Big5 or GB code.

Figure 7-3 Character Bold Display

7.3 Graphics Display Function

Figure7-4 shows the function and the value that register need be set under graphics display.

1. Set the REG [00h] bit3=1
2. Using bit-map to fill in the data

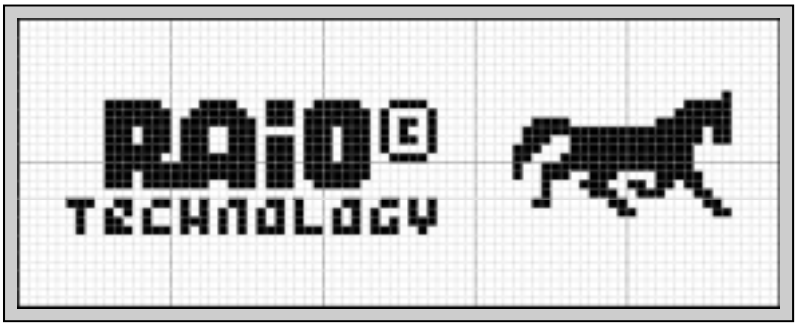

Figure 7-4 Graphics Display

7.4 Blinking Display

Figure7-5 shows the function and the value that register need to be set under blinking display.

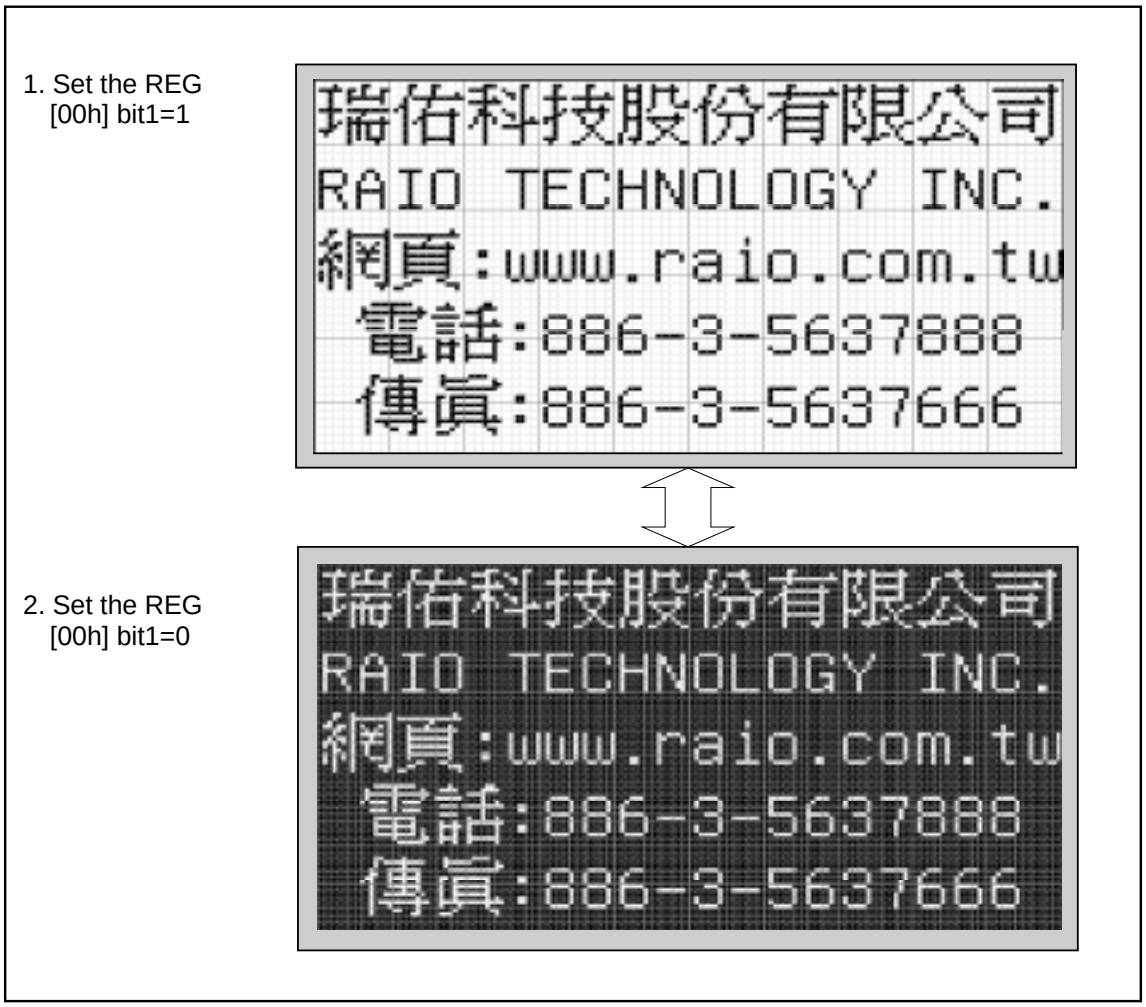

Figure 7-5 Blinking Display

7.5 Black-White Display

Figure7-6 shows the function and the value that register need to be set under black-white display.

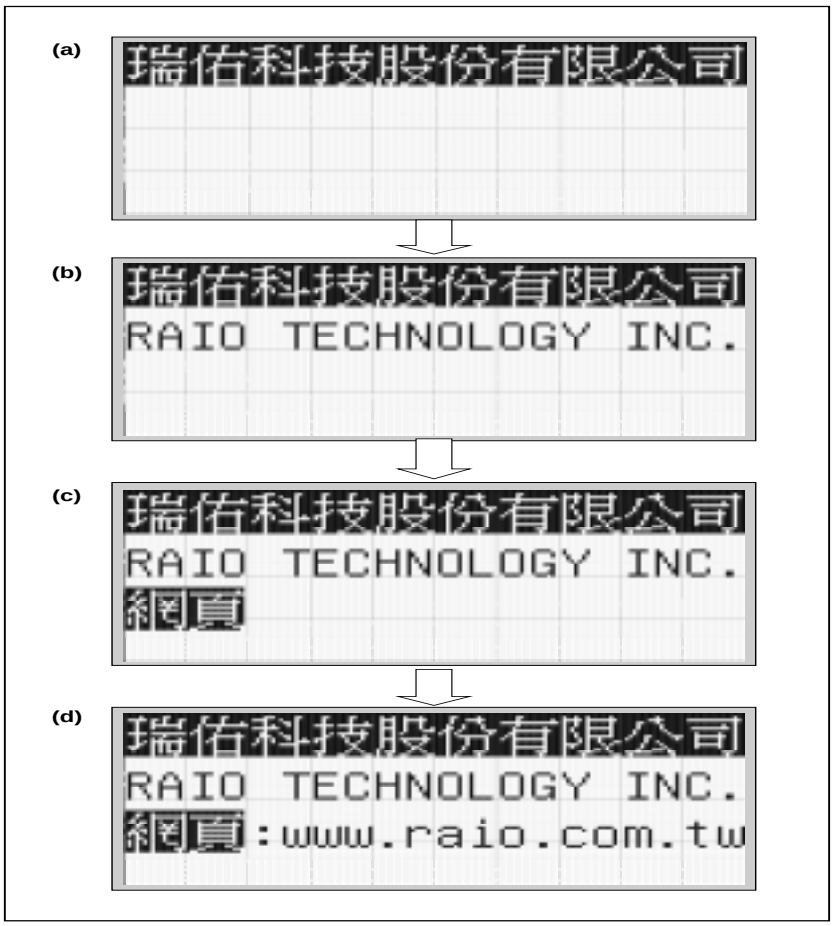

Figure 7-6 Blinking Display

(a)
1. Set REG [10h] bit5=0
2. Write in the Big5 code of "瑞佑科技股份有限公司" then it will show up "瑞佑科技股份有限公司"

(b)
3. Hold on (a)
4. Set REG [10h] bit5=1
5. Write in the Big5 code of "RAIO TECHNOLOGY INC." then it will show up " RAIO TECHNOLOGY INC."

(c)
6. Hold on (a), (b)
7. Set REG [10h] bit5=0
8. Write in the Big5 code of "網頁" then it will show up "網頁"

(d)
9. Hold on (a), (b) and (c)
10. Set REG [10h] bit5=1
11. Write in the Big5 code of ": www.raio.com.tw" then it will show up ": www.raio.com.tw"

7.6 Align the Chinese/English Font

Figure7-7 shows the function and the value that register need to be set under aligning the Chinese/English Font.

1. Set REG [10h] bit6=1

2. Write in the Big5 code of " 瑞佑科技股份有限公司 RAIO 中文 LCD 控制器" then it will show up " 瑞佑科技股份有限公司 RAIO 中文 LCD 控制器"

Figure 7-7 Align the Chinese/English Font

Figure 7-8 shows the function and the value that register need to be set under Non_Align the Chinese / English Font.

1. Set REG [10h] bit6=0

2. Write in the Big5 code of " 瑞佑科技股份有限公司 RAIO 中文 LCD 控制器" then it will show up " 瑞佑科技股份有限公司 RAIO 中文 LCD 控制器"

Figure 7-8 Non_Align the Chinese/English Font

7.7 Cursor

7.7.1 Cursor Position and Shift

The moving unit for segment of cursor is one byte(or one pixel). But the moving unit for common is pixel. For example, if user want to show "制" at third location of upper-left, then the Register value are CPXR = 04h, CPYR = 00h. If user want to show "器" at first position of second line, the register value are CPXR = 00h, CPYR = 10h. Please refer to Figure 7-9.

The cursor position is controlled by Register CPXR and CPYR for both text and graphics mode. You can also setup the Auto-Increase mode for write to DDRAM or read data DDRAM. The boundary depends on active window.

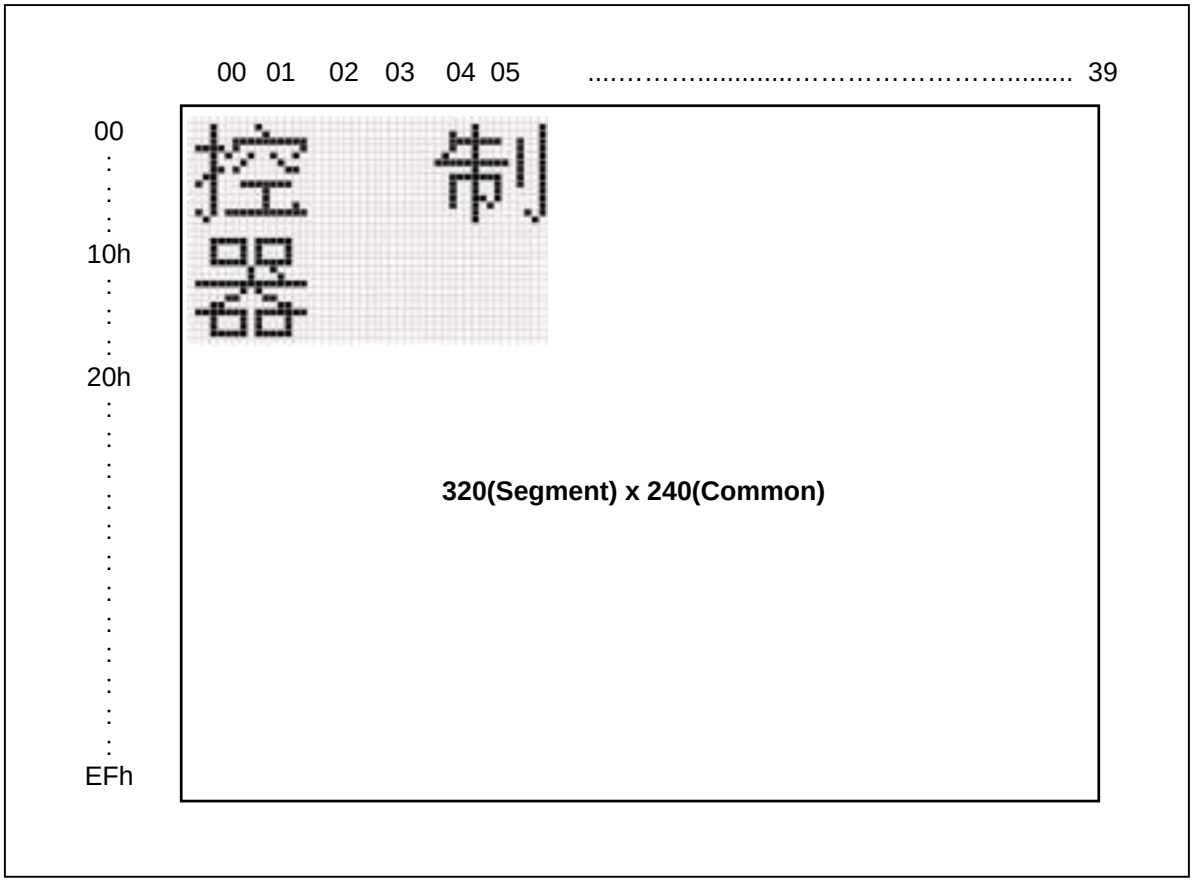

Figure 7-9 : Example of RA8802 Cursor Position

7.7.2 Cursor Display and Blinking

The user could control cursor On/Off or Blinking. The register [80h] BTR is used to set up the blinking time.

Blinking Time = BTR[80h] Bit[7..0] x (1/Frame_Rate)

7.7.3 Cursor Width and Height

The cursor height is controlled by register CSCR Bit[7..4] from 1~16pixel. It does depend on user's requirement.

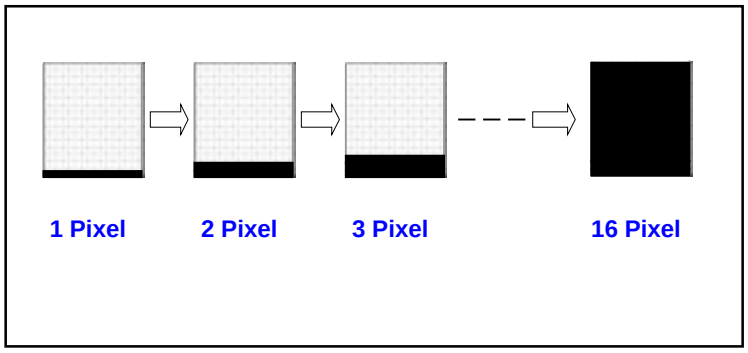

Figure 7-10 : Cursor Height

In text mode, RA8802/8820 provide two widths for selection. If Register CCR bit0 -- CSD = 0, the cursor width fixed to one byte(8 pixel). If CSD =1, the cursor width is depend on the character. If user sends a full size Chinese character, then the cursor width will become 2byte width(16 pixel). If user shows a half size character then the cursor width will change to one byte(8 pixel).

7.8 Display Window and Active Window

The RA8802/8820 provides two windows for real application -- Display Window and Active Window. The Display Window is the actual size of LCD panel. Active is a sub-window in Display Window. The boundary of cursor shift depends on the active window.

For RA8802, if LCD panel is 320x240 pixel then the display window size is 320x240. We can create an active window in the display window like Figure 7-11. This figure show the display size is 320x240, and a 160x160 active window is on the upper-middle.

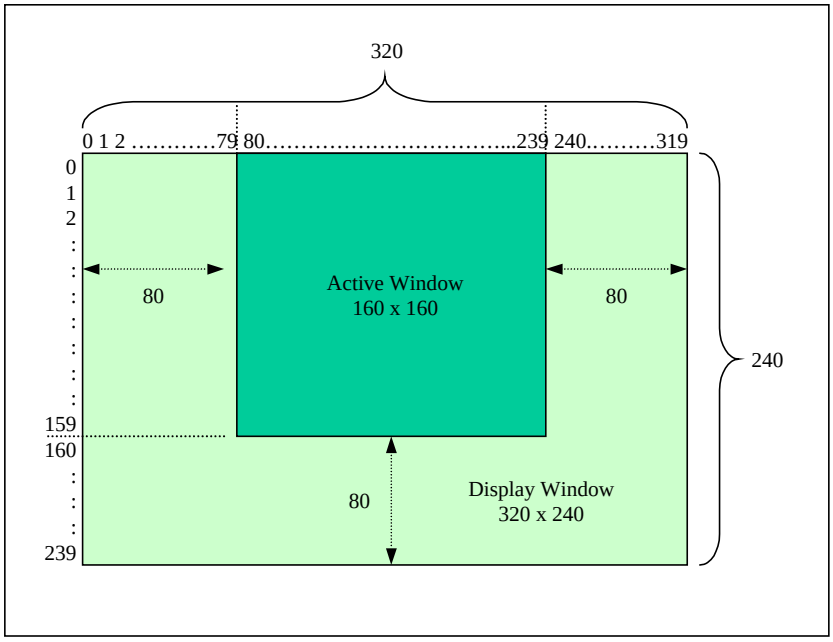

Figure 7-11 : RA8802 Display Window and Active Window

For RA8820, if LCD panel is 240x160 pixel then the display window size is 240x160. We can create an active window in the display window like Figure 7-12. This figure show the display size is 240x160, and a 120x120 active window is on the upper-left.

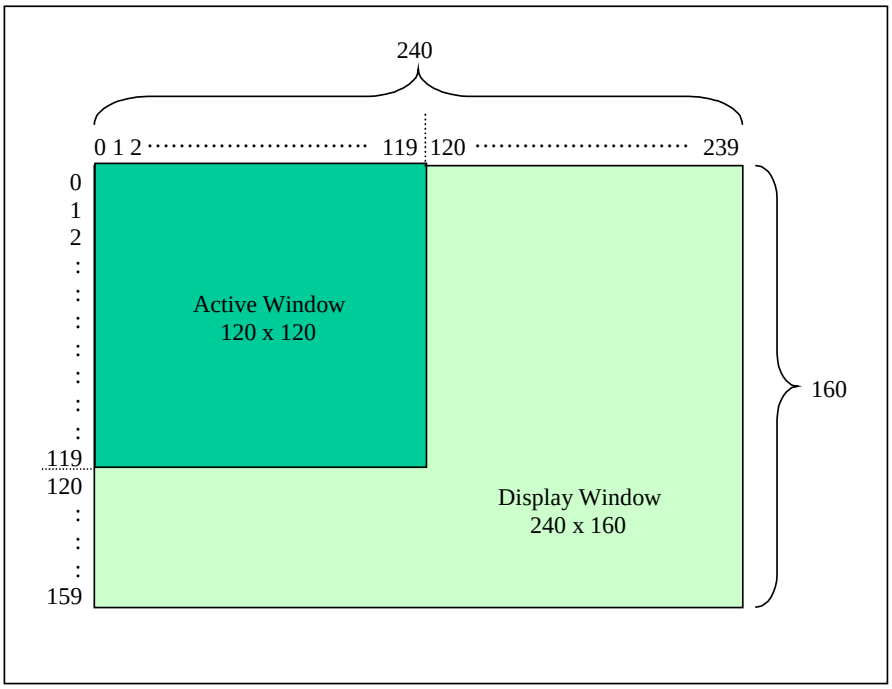

Figure 7-12 : RA8820 Display Window and Active window

8. Interfacing to the Driver

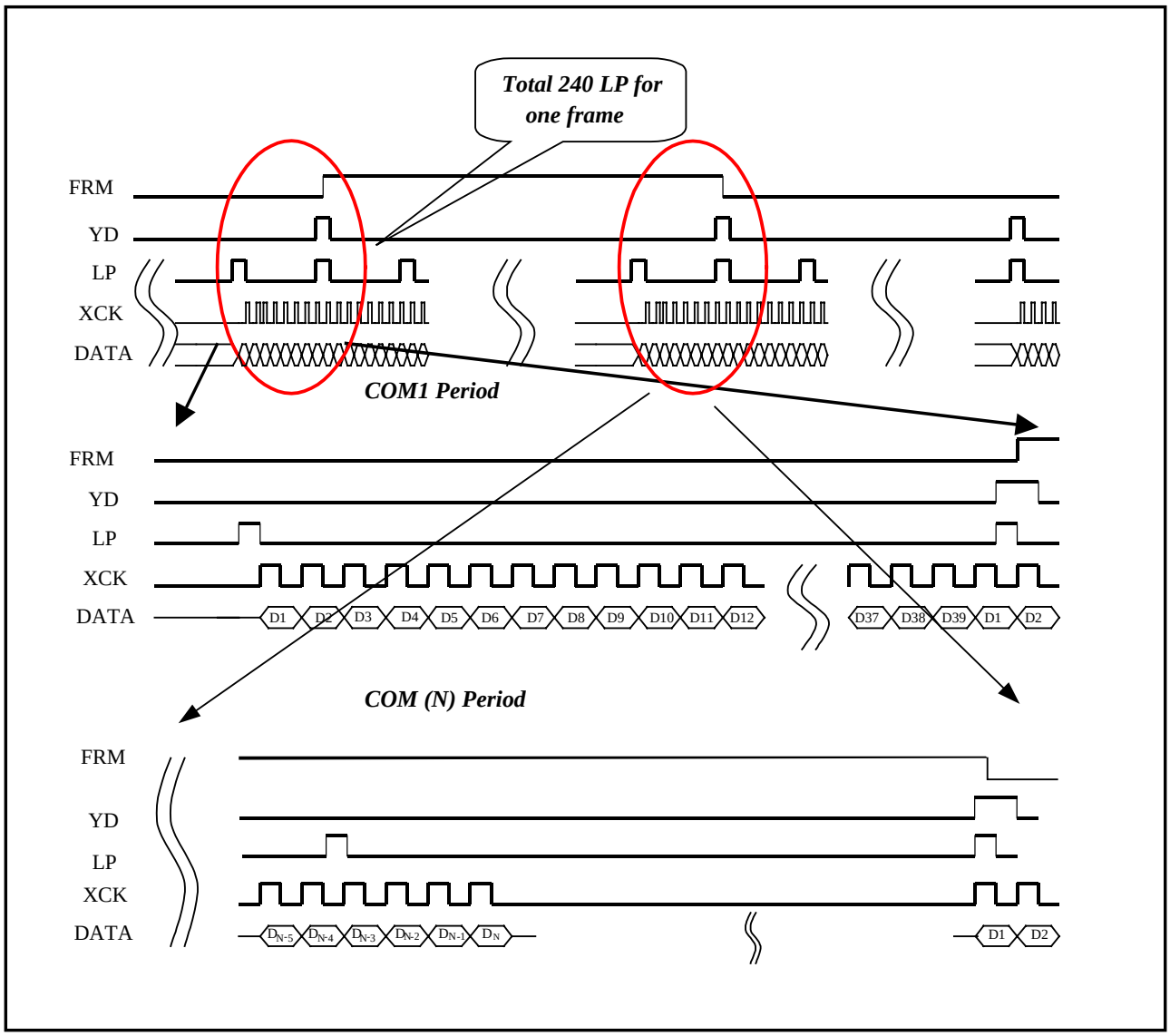

Figure 8-1 RA8802/8820 to Driver waveforms

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 9-1

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to 4.0	V
Input voltage range	V_{IN}	-0.3 to V_{DD}+0.3	V
Operation temperature range	T_{OPR}	-20 to 80	℃
Storage temperature	T_{ST}	-45 to 125	℃

9.2 DC Characteristic

Table 9-2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.7	3.3	4.0	V	
Input High Voltage	V_{IH}	0.8×V_{DD}	--	V_{DD}	V	
Input Low Voltage	V_{IL}	V_{SS}	--	0.2×V_{DD}	V	
Output High Voltage	V_{OH}	0.8×V_{DD}	--	V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}	--	0.2×V_{DD}	V	
Input leakage current 1	I_{IH}	--	--	+1	μA	
Input leakage current 2	I_{IL}	--	--	-1	μA	
Standby Mode current	I_{SB}	--	2.07	--	mA	**CLK_OUT: OFF** **LCD I/F: ON** **No MCU I/F Access** V_{DD}=3.3V, CLK=8MHz REG[90h] SCCR=08 Segment=320, Common=240 T_A=25℃
Normal Mode Current	I_{NORMAL}	--	2.07	--	mA	The same as above
Display Mode Current	$I_{DISPLAY}$	--	2.07	--	mA	The same as above
Off Mode	I_{OFF}	--	1	--	μA	The same as above

V_{DD}=2.7 to 4.0V, Vss=0V, Ta=-20 to 80℃

10. PAD Diagram

10.1 Bonding Pad

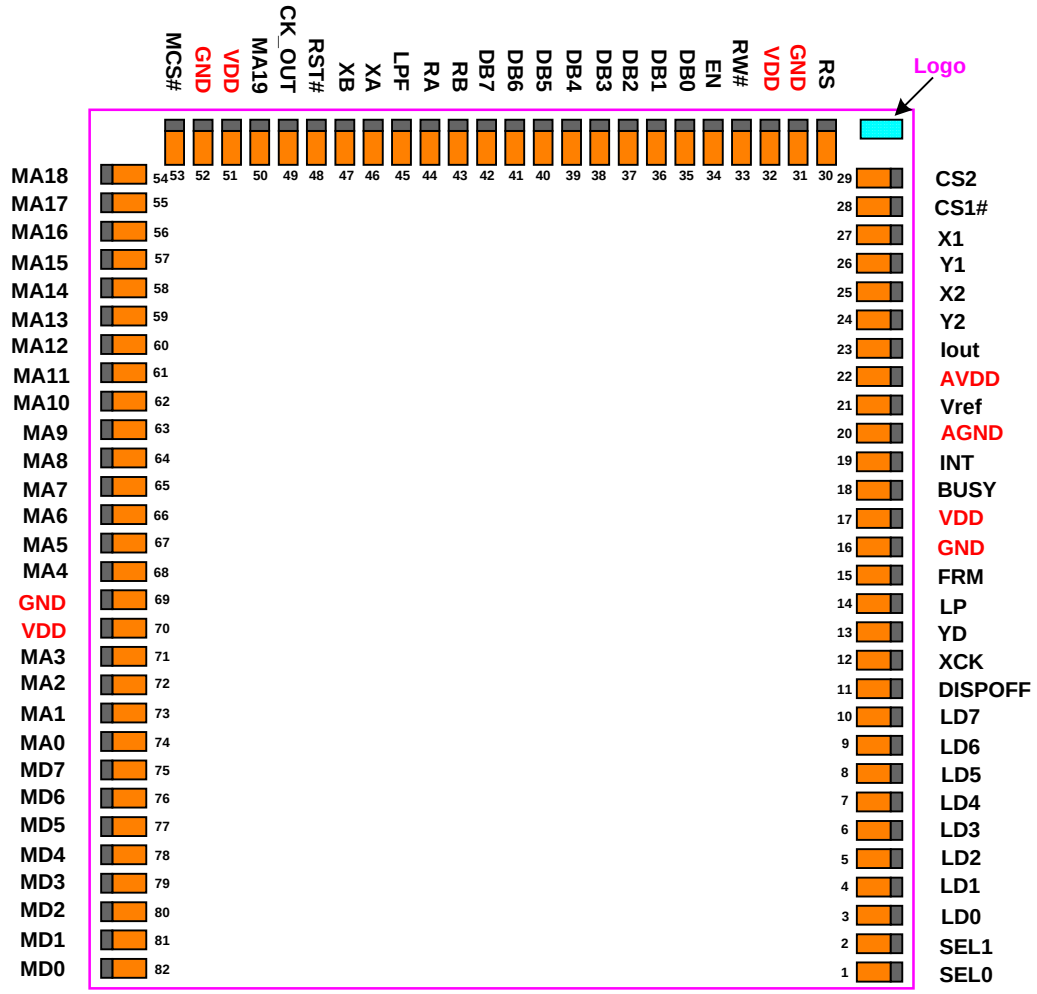

Figure 10-1：Bonding Pad

10.2 Pad X/Y Coordinate

Pad No.	Pad Name	X Coordinate	Y Coordinate
1	SEL0	1958.53	-1455.34
2	SEL1	1958.53	-1355.34
3	LD0	1958.53	-1255.34
4	LD1	1958.53	-1155.34
5	LD2	1958.53	-1055.34
6	LD3	1958.53	-955.34
7	LD4	1958.53	-855.34
8	LD5	1958.53	-755.34
9	LD6	1958.53	-655.34
10	LD7	1958.53	-555.34
11	DISPOFF	1958.53	-455.34
12	XCK	1958.53	-355.34
13	YD	1958.53	-255.34
14	LP	1958.53	-155.34
15	FRM	1958.53	-55.34
16	GND	1958.53	44.66
17	VDD	1958.53	144.66
18	BUSY	1958.53	244.66
19	INT	1958.53	344.66
20	AGND	1958.53	453.98
21	Vref	1958.53	564.54
22	AVDD	1958.53	675.04
23	Iout	1958.53	785.69
24	Y2	1958.53	890.69
25	X2	1958.53	995.69
26	Y1	1958.53	1100.69
27	X1	1958.53	1205.69
28	CS1#	1958.53	1305.69
29	CS2	1958.53	1405.69
30	RS	1423.48	1467.81
31	GND	1323.48	1467.81
32	VDD	1223.48	1467.81
33	RW#	1123.48	1467.81
34	EN	1023.48	1467.81
35	DB0	923.48	1467.81
36	DB1	823.48	1467.81
37	DB2	723.48	1467.81
38	DB3	623.48	1467.81
39	DB4	523.48	1467.81
40	DB5	423.48	1467.81
41	DB6	323.48	1467.81
42	DB7	223.48	1467.81
43	RB	-642.17	1467.81
44	RA	-742.17	1467.81
45	LPF	-842.17	1467.81
46	XA	-942.17	1467.81
47	XB	-1042.17	1467.81
48	RST#	-1142.17	1467.81
49	CK_OUT	-1242.17	1467.81
50	MA19	-1342.17	1467.81
51	VDD	-1442.17	1467.81
52	GND	-1542.17	1467.81
53	MCS#	-1642.17	1467.81
54	MA18	-1958.52	1344.66
55	MA17	-1958.52	1244.66
56	MA16	-1958.52	1144.66
57	MA15	-1958.52	1044.66
58	MA14	-1958.52	944.66
59	MA13	-1958.52	844.66
60	MA12	-1958.52	744.66
61	MA11	-1958.52	644.66
62	MA10	-1958.52	544.66
63	MA9	-1958.52	444.66
64	MA8	-1958.52	344.66
65	MA7	-1958.52	244.66
66	MA6	-1958.52	144.66
67	MA5	-1958.52	44.66
68	MA4	-1958.52	-55.34
69	GND	-1958.52	-155.34
70	VDD	-1958.52	-255.34
71	MA3	-1958.52	-355.34
72	MA2	-1958.52	-455.34
73	MA1	-1958.52	-555.34
74	MA0	-1958.52	-655.34
75	MD7	-1958.52	-755.34
76	MD6	-1958.52	-855.34
77	MD5	-1958.52	-955.34
78	MD4	-1958.52	-1055.34
79	MD3	-1958.52	-1155.34
80	MD2	-1958.52	-1255.34
81	MD1	-1958.52	-1355.34
82	MD0	-1958.52	-1455.34

10.3. Package Diagram

10.3.1 PQFP-100Pin

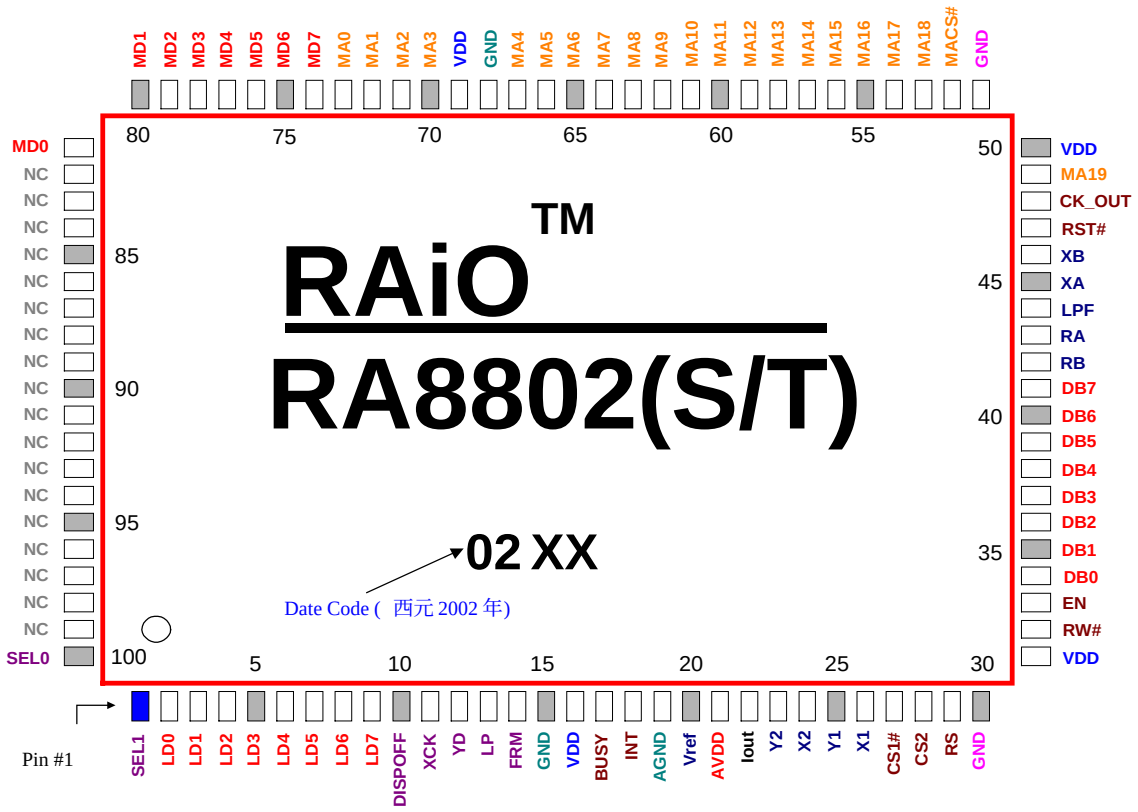

Figure 10-2：PQFP-100Pin Package Diagram

- RA8802/8820-S：Stands for Simplified Chinese Characters
- RA8802/8820-T：Stands for Traditional Chinese Characters
- The Package diagram of LQFP-100Pin(12x12) is same as PQFP-100Pin.

10.3.2 LQFP-100Pin(12x12)

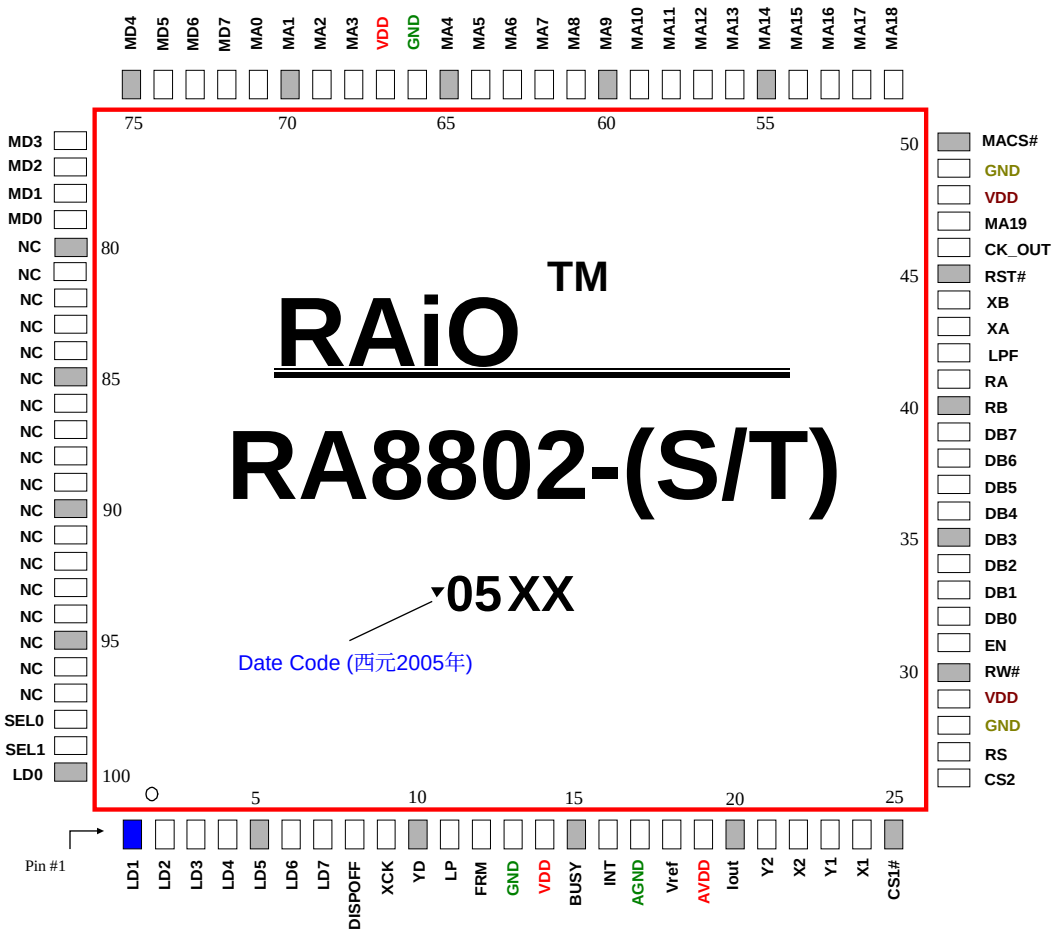

Figure 10-3：LQFP-100Pin(12x12) Package Diagram

10.4 RA8802/8820 Package Leap frame

10.4.1 PQFP-100 Pin

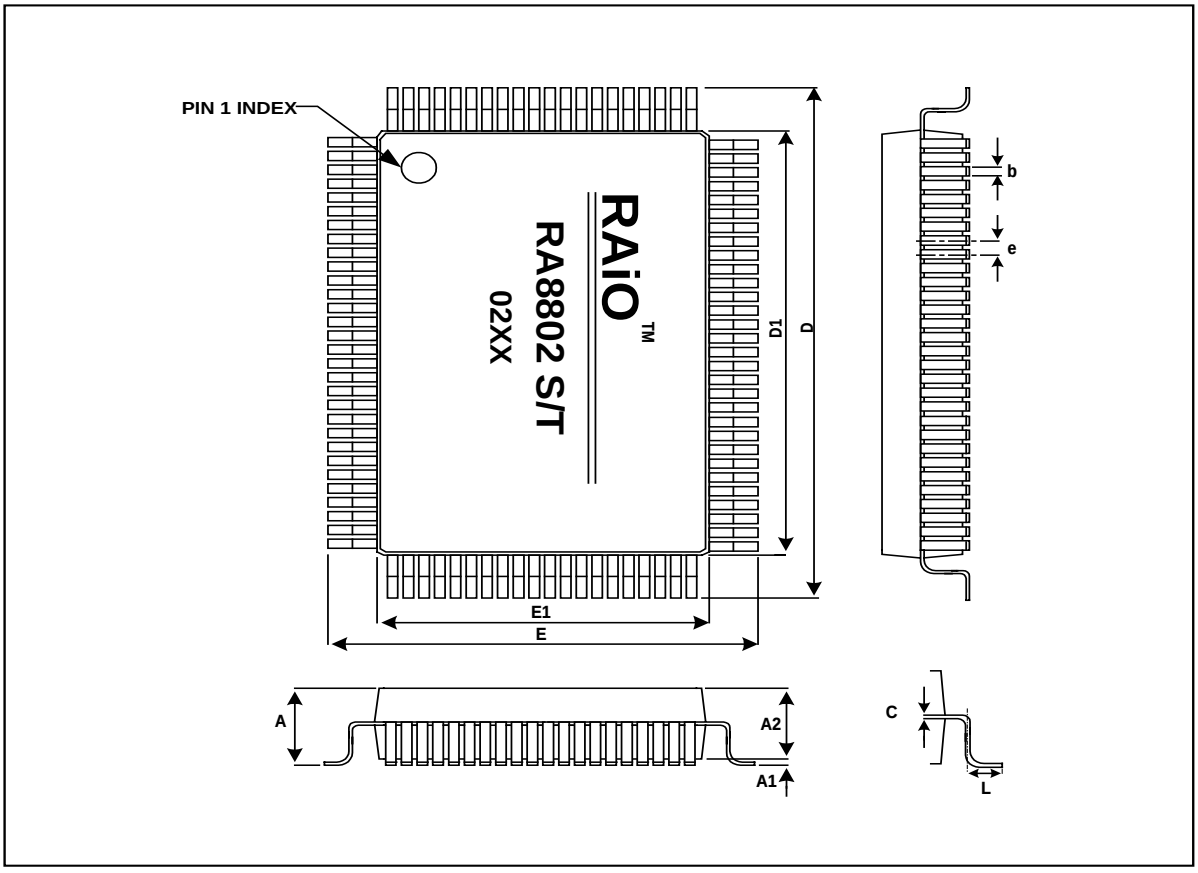

Figure 10-4：PQFP-100Pin Mechanical

Table 10-1

Symbols	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	--	--	3.40	--	--	0.134
A1	0.25	--	--	0.010	--	--
A2	2.54	2.79	3.05	0.100	0.110	0.120
b	0.23	--	0.38	0.009	--	0.015
C	0.13	0.15	0.20	0.005	0.006	0.008
E	16.94	17.20	17.45	0.667	0.667	0.687
E1	13.89	13.99	14.10	0.547	0.551	0.555
D	22.96	23.22	23.44	0.904	0.914	0.923
D1	19.89	19.99	20.09	0.783	0.787	0.791
e	--	0.65	--	--	0.0256	--
L	0.66	0.79	0.94	0.026	0.031	0.037

10.4.2 LQFP-100 Pin(Body Siz:14x20 mm)

Table 10-2

Symbols	Dimensions in Millimeters			Dimensions in Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	--	--	1.60	--	--	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09	--	0.20	0.004	--	0.008
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
D	21.90	22.00	22.10	0.862	0.866	0.870
D1	19.90	20.00	20.10	0.783	0.787	0.791
e	--	0.65	--	--	0.026	--
L	0.45	0.60	0.75	0.018	0.024	0.030

10.4.3 LQFP-100 Pin(Body Siz:12x12 mm)

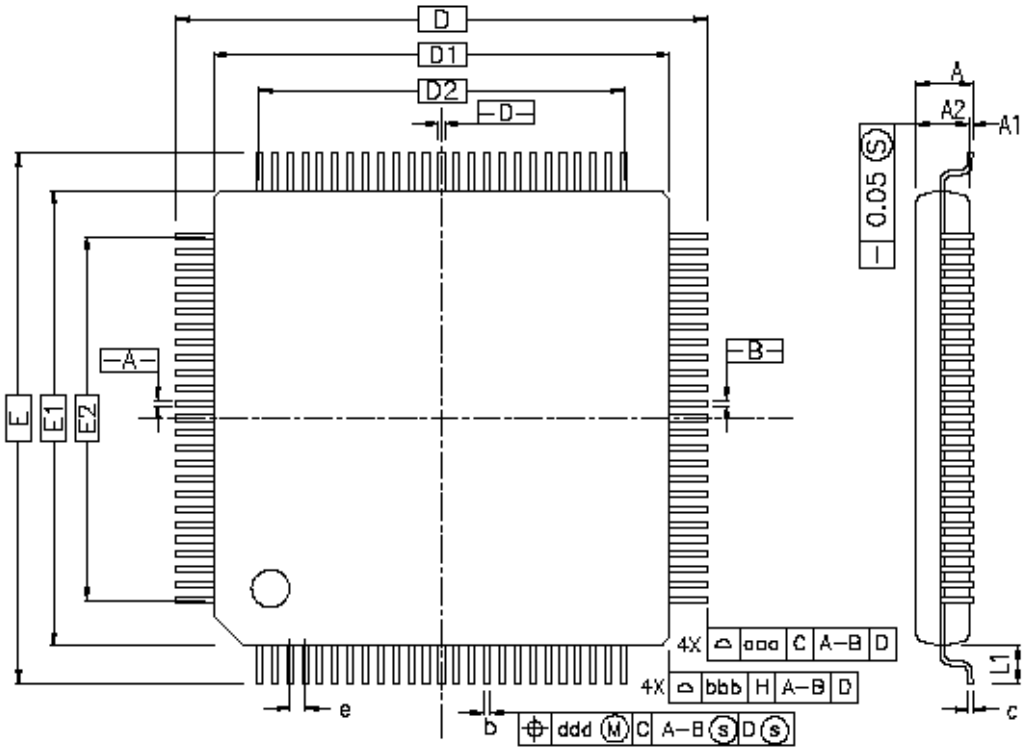

Figure 10-5：LQFP-100Pin(12x12 mm) Mechanical(1)

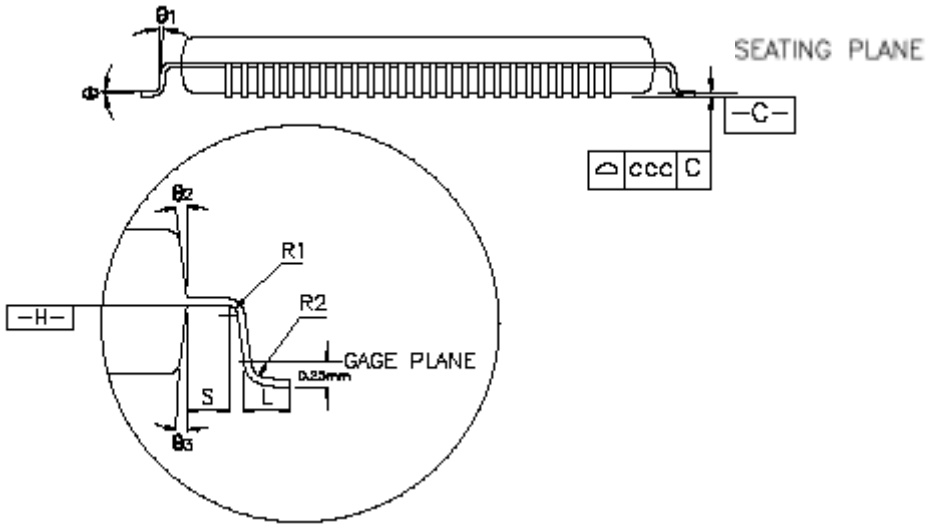

Figure 10-6：LQFP-100Pin(12x12 mm) Mechanical(2)

Table 10-3

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.15	0.002	--	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E1	12.00 BSC.			0.472 BSC.		
R2	0.08	--	0.20	0.003	--	0.008
R1	0.08	--	--	0.003	--	--
θ	0^o	3.5^o	7^o	0^o	3.5^o	7^o
θ1	0^o	--	--	0^o	--	--
θ2	11^o	12^o	13^o	11^o	12^o	13^o
θ3	11^o	12^o	13^o	11^o	12^o	13^o
c	0.09	--	0.20	0.004	--	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	--	--	0.008	--	--

Dimensions are in millimeters.

Table 10-4

SYMBOL	80L						100L					
	MILLIMEETR			INCH			MILLIMEETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011	0.13	0.16	0.23	0.005	0.006	0.009
e	0.50 BSC.			0.020 BSC.			0.40 BSC.			0.016 BSC.		
D2	9.50			0.374			9.60			0.378		
E2	9.50			0.374			9.60			0.378		
TOLERANCES OF FORM AND POSITION												
aaa	0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008		
ccc	0.08			0.003			0.08			0.003		
ddd	0.08			0.003			0.07			0.003		

Appendix A. Built-in ASCII Block

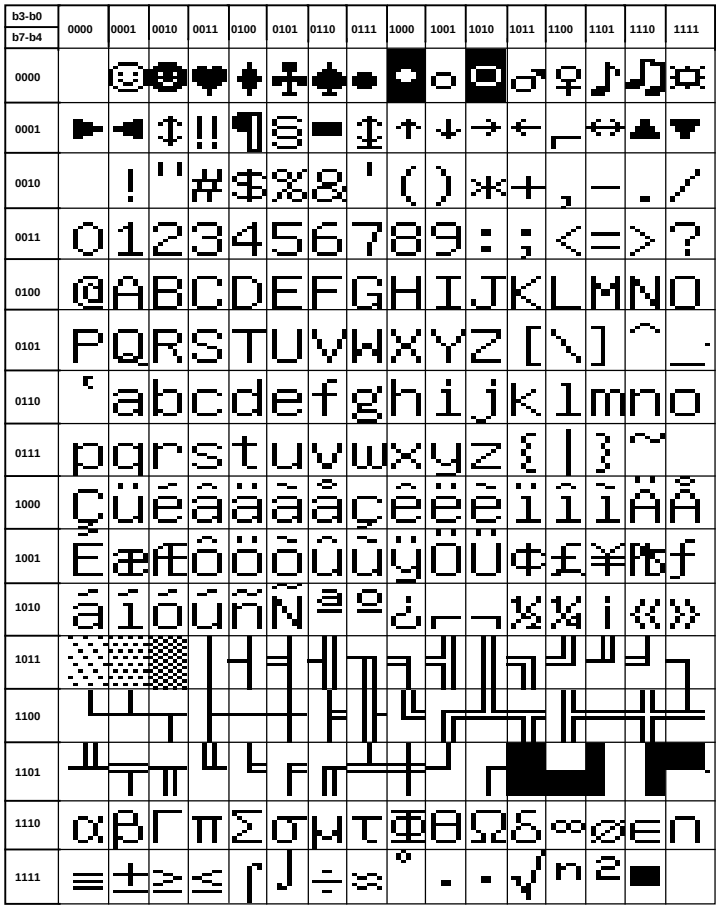

Figure A-1：ASCII Block 0

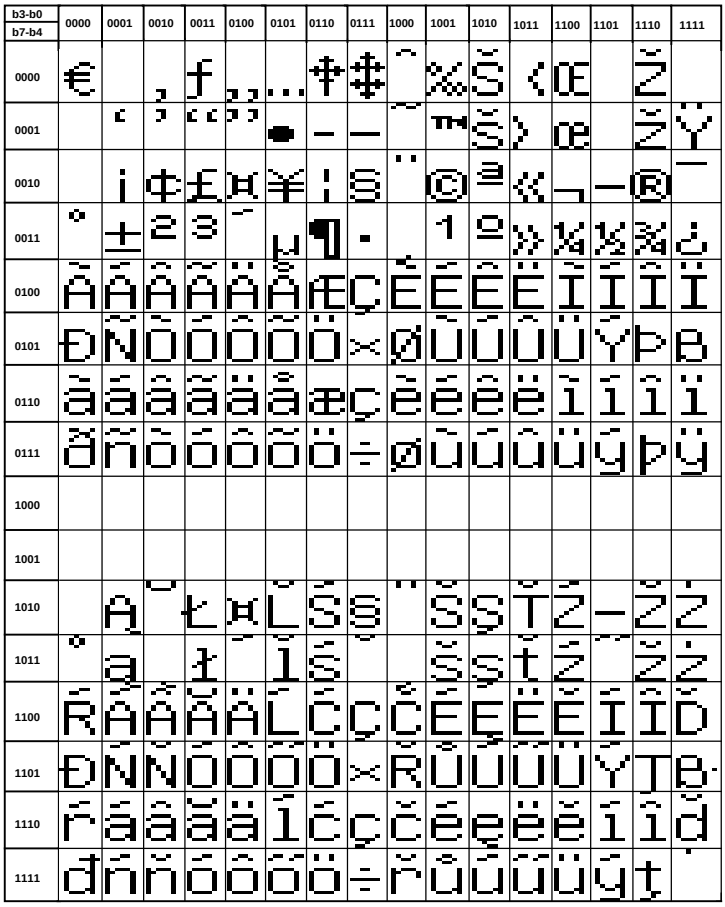

Figure A-2：ASCII Block 1

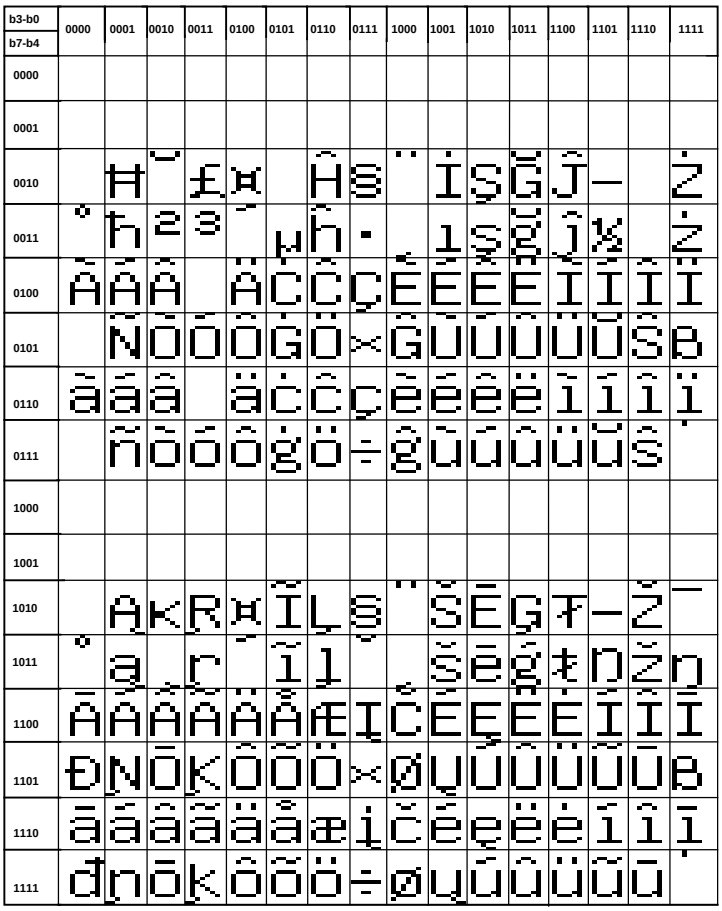

Figure A-3：ASCII Block 2

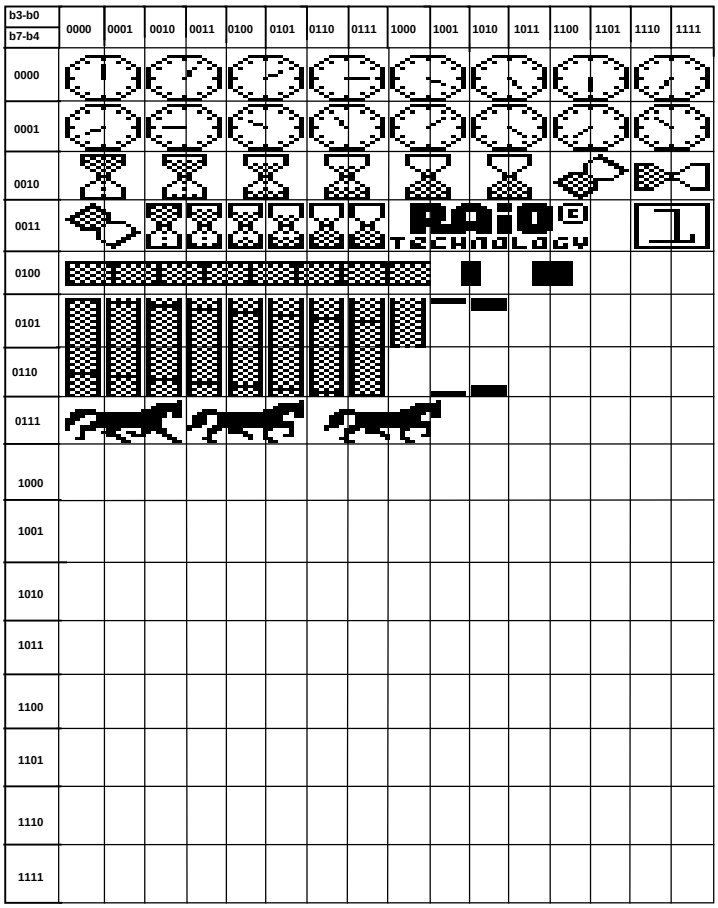

Figure A-4：ASCII Block 3