RAiO

RA8825

128x33 Dot Matrix

LCD Driver

Specification

Version 1.3
July 1, 2006

RAiO Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	October 13, 2005	First Release
1.1	January 3, 2006	Update section 6-4-2: Voltage Regulator Update Table 6-2: Power Circuit Setup Update Table 6-4: Select V_{REF}
1.2	March 2, 2006	Update section 4-4: The connection of TEST[2:0] for normal operation. Update Figure A-2, A-3, A-4 and A-5
1.3	July 1 2006	Update Table 8-1：Bump Size and Pitch

Chapter Contents Page

1. General Description

The RA8825 is a Dot-Matrix LCD Driver. The embedded 528Byte display RAM supports up to 128x33 dots LCD panel. The RA8825 also provides a scrolling buffer memory for scrolling functions. It supports up, down, left and right scrolling features, and all of the scrolling functions are execute by hardware.

The RA8825 integrates much powerful hardware that including Contrast adjustment, 4x5 Key-Scan, eight General Purpose I/O and EL Backlight signals for EL driver. The RA8825 is a high integration chip of LCD Controller. It reduce a lot of time for system develop, and save much cost for hardware system that due to it provides many features for related LCD display application.

2. Feature

- Support 8080/6800 8/4-bit Parallel Interface and 3-Wire/4-Wire Serial Interface
- Support Maximum 128Seg x 33Com LCD Panel.
- Built-in 528 Bytes Display RAM and 354Byte Scrolling Buffer
- Built-in 2X~3X(Voltage Booster), Voltage Regulator, Voltage Follower
- Support 1/33 Duty, 1/6~1/4 Bias Panel
- Eight General Purpose I/O
- Built-in 4x5 Key-scan Circuit
- Support Horizontal/Vertical Scrolling Functions
- Provide Signals for EL Driver
- Provide 32-Steps Contrast Adjust
- Build-in RC Oscillator
- Voltage Operation: 2.6~3.6V
- Package: Gold Bump Die

3. Block Diagram

The RA8825 is consist of Display RAM, 256Kbyte Font ROM, Command Registers, LCD Controller, LCD Driver, Voltage Booster, Voltage Regulator, MPU Interface and Key-Scan circuit.

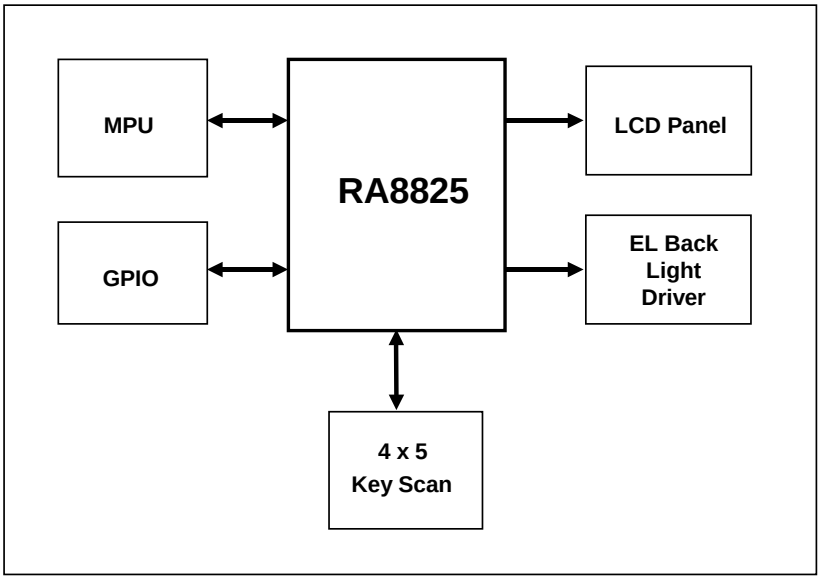


Figure 3-1: System Block

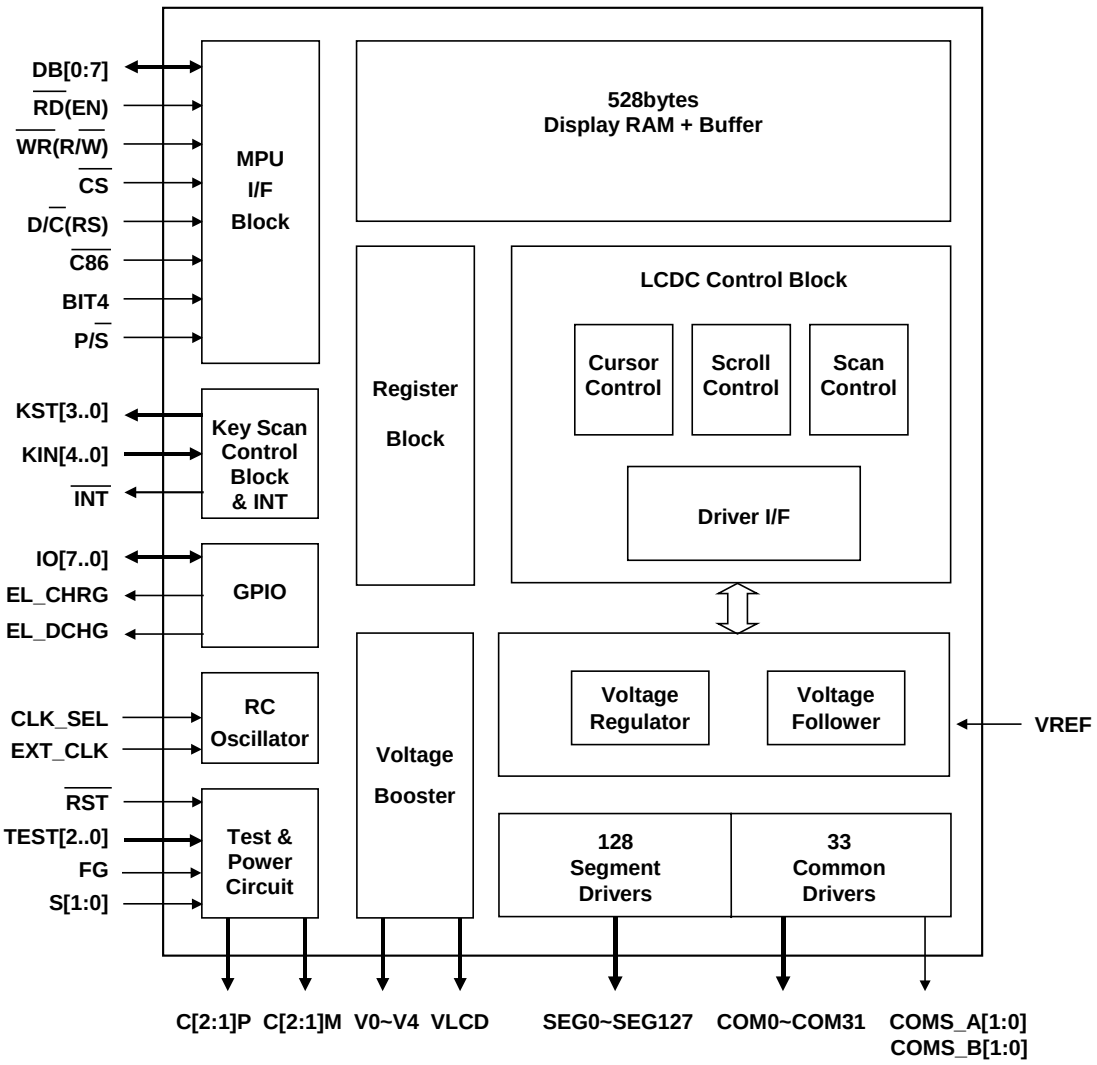


Figure 3-2: Internal Block

4. Pin Definition

4-1 MPU Interface

Pin Name	I/O	Description
DB[7..0] DB0: SCK DB1: SDA/SDO DB2: RS/SDI DB3: $\overline{CS}$ DB[7:6]: SMOD	I/O	**Data Bus** When the MPU uses parallel mode and 8-bit then all of the DB[7:0] are valid. When use 4-bit then only DB[3:0] are valid, and DB[7:4] have to keep floating. When P/$\overline{S}$ is "0", then the interface between MPU and RA8825 is Serial Mode. The pins DB[7:6](SMOD[1:0]) are used to select which serial mode: **SMOD: Serial Mode** ---------- 0 X : 3-Wire, SCK, SDA, $\overline{CS}$ are used. 1 0 : 4-Wire, SCK, SDA, RS, $\overline{CS}$ are used. 1 1 : 4-Wire, SCK, SDO, SDI, $\overline{CS}$ are used. In serial mode, all of the related signals are defined by DB[3:0]: SCK(DB0) : Serial Clock. SDA(DB1) : Bi-direction Mode Serial Data. SDO(DB1) : Data Out. RS(DB2) : Memory/Register Cycle Select. SDI(DB2) : Serial Data In. $\overline{CS}$(DB3) : Chip Select, active low. The unused pin must keep NC for serial mode.
$\overline{RD}$ EN	I	**Read Control or Enable** When use 8080 series interface, $\overline{RD}$ is the read signal and active low. When use 6800 series interface, EN is the Enable signal and active high. Connect this pin to VDD for serial mode.
$\overline{WR}$ R/$\overline{W}$	I	**Write Control or Read-Write Control** When use 8080 series interface, $\overline{WR}$ is the write signal and active low. When use 6800 series interface, this pin is R/$\overline{W}$, active high for read cycle and active low for write cycle. Connect this pin to VDD for serial mode.
D/$\overline{C}$ RS	I	**Data/Command Select or Register Select)** When use 8080 series interface, this is Data or Command signal. When D/$\overline{C}$ is "0", means Register Cycle(or Command Cycle). When D/$\overline{C}$ is "1", means Data Access Cycle(Data Cycle). When use 6800 series interface, this is the RS signal. When RS is "0", means Register Cycle and "1" means Data Access Cycle. Connect this pin to VDD for serial mode.
$\overline{CS}$	I	**Chip Select** This is a chip enable for RA8825. Connect this pin to VDD for serial mode.
$\overline{INT}$	O	**Interrupt Signal** This is an interrupt output for MPU. Active low。
$\overline{C86}$	I	**MPU Select** $\overline{C86}$ = 0 ➔ The MPU interface is 8080 series.

		$\overline{C86}$ = 1 ➔ The MPU interface is 6800 series(Default). Connect this pin to VDD for serial mode.
BIT4	I	**Data Bit Select** BIT4 = 0➔ The parallel mode is use 8-bit data bus. BIT4 = 1➔ The parallel mode is use 4-bit data bus(Default). Connect this pin to VDD for serial mode.
P/$\overline{S}$	I	**Parallel/Serial Select** P/$\overline{S}$ = 0 ➔ The MPU interface is serial mode(Default). See the setting of DB[7:6]. P/$\overline{S}$ = 1 ➔ The MPU interface is parallel mode.

4-2 LCD Panel Interface

Pin Name	I/O	Description
SEG0 ~ SEG127	O	**Segment Signals for Panel**
COM0 ~ COM31	O	**Common Signals for Panel**
COMS_A[1:0] COMS_B[1:0]	O	**Icon Common Signals for Panel**

4-3 Clock and Power

Pin Name	I/O	Description
V0~V4	O	**Voltage Source of LCD Driver** The relationship of the power is VLCD> V0≧V1≧V2≧V3≧V4≧VSS。 These pins have to add external 0.1uF~1uF capacitor to GND.
C1P, C1M	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
C2P, C2M	I	**Capacitor Input** These are used to connect a capacitor for internal Booster.
VLCD	O	**Booster Output**
VREF	I	**Reference Voltage Input** This is the refeence voltage input when use an external regulator. Normally keep this pin floating, if connect this signal to FPC then have to add a 0.1uF capacitor to GND.
CLK_SEL	I	**Clock Select** This pin is used to select the clock source. When CLK_SEL “1”, the clock is generated by internal RC oscillator. When CLK_SEL is “0”, the system clock is drive by external pin - EXT_CLK.
EXT_CLK	I	**External Clock** When CLK_SEL is “0”, this pin is the external clock input. When CLK_SEL is “1”, this pin do not used and has to connect VDD or GND.
VDD VDDP	P	**VDD Power**
GND GNDP	P	**Ground**

4-4 Misc.

Pin Name	I/O	Description
KST[3..0]	O	**Key Strobe Output**
KIN[4..0]	I	**Key Data Input** Connect these pins to VDD for unused.
IO[7..0]	I/O	**General Purpose I/O**
EL_CHRG	O	**EL Charge Signal**
EL_DCHG	O	**EL Discharge Signal**
$\overline{RST}$	I	**Reset** This is the Reset signal and active low.
TEST[2..0]	I	**Test Pins** These pins must contact to GND for normal mode.
S[1:0], FG	I	**Test Pins** These pins must keep NC for normal mode.

Table 4-1: Pin Definition of Parallel/Serial Mode of MPU

Pin Name	I/O	Parallel Mode				Serial Mode		
		8080		6800		3-Wire	4-Wire (A-Typ)	4-Wire (B-Typ)
		8Bit	4Bit	8Bit	4Bit			
DB7	I/O	DB7	--[*1]	DB7	--	0	1	1
DB6	I/O	DB6	--	DB6	--	0	0	1
DB5	I/O	DB5	--	DB5	--	--	--	--
DB4	I/O	DB4	--	DB4	--	--	--	--
DB3	I/O	DB3	DB3	DB3	DB3	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$
DB2	I/O	DB2	DB2	DB2	DB2	--	RS	SDI
DB1	I/O	DB1	DB1	DB1	DB1	SDA	SDA	SDO
DB0	I/O	DB0	DB0	DB0	DB0	SCK	SCK	SCK
$\overline{RD}$, EN	I	$\overline{RD}$	$\overline{RD}$	EN	EN	1[*2]	1	1
$\overline{WR}$, R/$\overline{W}$	I	$\overline{WR}$	$\overline{WR}$	R/$\overline{W}$	R/$\overline{W}$	1	1	1
D/$\overline{C}$, RS	I	D/$\overline{C}$	D/$\overline{C}$	RS	RS	1	1	1
$\overline{CS}$	I	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	1	1	1
$\overline{C86}$	I	0	0	1	1	1	1	1
BIT4	I	0	1	0	1	1	1	1
P/$\overline{S}$	I	1	1	1	1	0	0	0

Note1: "--" means not used and keep floating(NC).

Note2: In serial mode the unused parallel pins have to connect to 1(VDD).

5. Registers Description

5-1 Register Table

Table 5-1: Register Table

ID	Name	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	**DWFR**	B/C	--	NW5	NW4	NW3	NW2	NW1	NW0	Wave Form Select
1	**PWRR**	SRST	MCLR	--	--	KWK	IOWK	DOFF_Z	SLP	Power Control
2	**SYSR**	LS3	LS2	LS1	LS0	--	--	RS1	RS0	System Setting
3	**MWMR**	BMOD1	BMOD0	BIEN	--	--	--	--	--	Memory Mode
4	**CURCR**	--	H2	H1	H0	--	BLK	CR	CUR_EN	Cursor Control
5	**X-CUR**	--	--	X5	X4	X3	X2	X1	X0	Cursor X Position
6	**Y-CUR**	--	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Cursor Y Position
7	**KEYR**	KSB	KDB1	KDB0	KSTB_SEL	K_AUTO	IRE	KF1/ KSTB1	KF0/ KSTB0	Key-scan Control
	KSDR	SIRQ	KSTB1	KSTB0	KSD4	KSD3	KSD2	KSD1	KSD0	Key-scan Data
		SIRQ	AKD6	AKD5	AKD4	AKD3	AKD2	AKD1	AKD0	
8	**SWSXR**	--	--	--	SSX4	SSX3	SSX2	SSX1	SSX0	X-Scroll Start
9	**SWSYR**	--	--	SSY5	SSY4	SSY3	SSY2	SSY1	SSY0	Y-Scroll Start
A	**SWRXR**	--	--	--	SRX4	SRX3	SRX2	SRX1	SRX0	X-Scroll Range
B	**SWRYR**	--	--	SRY5	SRY4	SRY3	SRY2	SRY1	SRY0	Y-Scroll Range
C	**SCOR**	SL7	SL6	SL5/SR5	SL4/SR4	SL3/SR3	SL2/SR2	SL1/SR1	SL0/SR0	Scroll Unit
D	**ASCR**	SPD3	SPD2	SPD1	SPD0	STP3	STP2	STP1	STP0	Auto Scroll Control
E	**SCCR**	SCR_IMD1	SCR_IMD0	SCR_MD	SBUF	SCR_DIR1	SCR_DIR0	SCR_INTEN	AUTO_SCR	Scroll Control
F	**ISR**	--	--	--	--	--	SCR_I	KI	--	Interrupt Status
10	**CSTR**	BR2	BR1	BR0	CT4	CT3	CT2	CT1	CT0	Contrast
11	**DRCR_A**	BOFF	EN_R	EN_G	ROFF	IDIR	--	CDIR	SDIR	Driver Control
12	**DRCR_B**	CK_BS1	CK_BS0	RR2	RR1	RR0	HD2	HD1	HD0	Driver Control
13	**BLTR**	BLK_EN	PBK_EN	--	GINV	BLT3	BLT2	BLT1	BLT0	Blink Setting
14	**IODR**	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0	IO Port Direction
15	**IODAR**	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0	IO Port Data
16	**ELCR**	EL_EN	--	--	--	ELT3	ELT2	ELT1	ELT0	EL Control

5-2 Register Contents

The RA8825 accept two Command Cycle from MPU. One is Register Cycle(RS = 0) and the other is Memory Cycle(RS = 1). The MPU has to assign the register number of RA8825 that before access these registers. Therefore, the first byte that MPU pass to RA8825 will be store into Index Register. And RA8825 will assume the next byte is read from or write into the register which Index Register assigned.

IR (Index Register)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	ID4	ID3	ID2	ID1	ID0

ID[4:0]: These bits are used to store the register number that MPU want to access on next cycle.

The ID[[4:0] provide 32 register number(00h~1Fh). But currently the RA8825 only used 23 registers (00h~16h). All of these registers are be initially to “00h” after RESET.

Memory Data (RAMD)

RW	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0/1	1	D7	D6	D5	D4	D3	D2	D1	D0

If RS is “1”, It means MPU execute the Memory Cycle for RA8825. The memory include Display RAM and ICON RAM.

[00h] Driver Waveform Register (DWFR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	B/C	--	NW5	NW4	NW3	NW2	NW1	NW0

B/C: Select waveform of drive. 0 ➔ B-Type waveform. 1 ➔ C-Type waveform.

NW[5:0]: These bits are used to assign the Segment/Row number that when internal Frame signals can to it and want to change the state. This function support only when B/C is “1” (C-Type wave form).

[01h] Power Control Register (PWRR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SRST	MCLR	--	--	KWK	IOWK	DOFF_Z	SLP

SRST: S/W reset. 1 ➔ All of the register will be initialed again except the display memory. 0 ➔ No action.

After execute SRST command, please wait 2 times of system clock, and then execute other command.

MCLR: Clear memory. 1 ➔ Clear the Display RAM data to “00h”. 0 ➔ No action. If both MCLR and SRST set to ”1” then RA8825 will clear the display RAM and then Reset.

KWK: Key-scan wake up Setting. 0 ➔ Key-scan Wake up function off. 1 ➔ Key-scan wake up function on.

IOWK: I/O wake up Setting. 0 ➔ IO port wake up function off. 1 ➔ IO port wake up function on.

DOFF_Z: Display off. 0 ➔ LCD driver and display off. 1 ➔ LCD driver and display on.

SLP: Sleep mode setting. 1 ➔ Enter sleep mode, and turn off the clock. 0 ➔ RA8825 wake up. This bit was clear to “0” when wake up from I/O port or Key-scan. If SLP set to 1, the internal LCD Driver Circuit are not Closed. So before enter the sleep mode, you have to set the DB[7:4] of Register[11h] - **DRCR_A** to 0 for reduce the power consumption.

[02h] System Register (SYSR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	LS3	LS2	LS1	LS0	--	--	RS1	RS0

LS[3:0]: Setup the segment number. The maximum segment of RA8825 is 128.

LS3	LS2	LS1	LS0	Line No.
0	0	0	0	16
0	0	0	1	32
0	0	1	0	48
0	0	1	1	64
0	1	0	0	80
0	1	0	1	96
0	1	1	0	112
0	1	1	1	128
1	0	0	0	Reserved
:	:	:	:	Reserved
1	1	1	1	Reserved

RS[1:0]: Setup the common number. The maximum common of RA8825 is 32(Not including Icon).

RS1	RS0	Row No.
0	0	16
0	1	32
1	0	Reserved
1	1	Reserved

[03h] Memory Write Mode Register (MWMR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BMOD1	BMOD0	BIEN	--	--	--	--	--

BMOD[1:0]: Setup the range for memory written.

BMOD1	BMOD0	Memory Range of Write
0	0	Normal Display Range
0	1	Display Range + Scroll-Buffer
1	x	Scroll-Buffer

BIEN: Busy interrupt control. 1 ➔ Busy interrupt enable (After write data to memory). 0 ➔ Busy interrupt disable.

[04h] Cursor Control Register (CURCR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	--	H2	H1	H0	--	BLK	CR	CUR_EN

H[2:0]: Setup the cursor height.

H2	H1	H0	Height (Pixel)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

BLK: Cursor blink select. 0 ➔ No Blinking. 1 ➔ Cursor Blinking.
CR: Cursor return. 0 ➔ No action. 1 ➔ Cursor return. Cursor will return to the left of panel.
CUR_EN: Cursor display select. 0 ➔ Cursor hides. 1 ➔ Cursor Display.

[05h] Cursor Position Register of X (X-CUR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	--	--	X5	X4	X3	X2	X1	X0

X[5:0]: Setup the cursor position on segment. The unit is 8-pixels. Because maximum segment of RA8825 is 128-pixels, therefore the range of X[5:0] is 0~Fh. When the X[5:0] is 20h or 21h, then the cursor position is assign to horizontal Scroll-Buffer.

[06h] Cursor Position Register of Y (Y-CUR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	--	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Y[6:0]: Setup the cursor position on common. The unit is 1-pixels. Because maximum common of RA8825 is 32-pixels, therefore the range of Y[6:0] is 0~1Fh. When the Y[6:0] is 40h~4Fh, then the cursor position is assign to vertical Scroll-Buffer. When Y[6:0] is 50h then cursor is located at COMS(Icon).

[07h] Key-scan Control Register (KEYR) (Write Only)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	KSB	KDB1	KDB0	KSTB_SEL	K_AUTO	IRE	KF1/ KSTB1	KF0/ KSTB0

KSB: Key-scan control. 0 ➔ Key-scan disable. 1 ➔ Key-scan enable.
KDB[1:0]: Setup the de-bounce times of Key-scan in Auto-Mode. The one time means the time that Key-scan for one loop.

KDB1	KDB0	Times
0	0	8
0	1	16
1	0	32
1	1	64

KSTB_SEL: In non-Auto-mode, 0 ➔ the DB[1:0] are defined as KF[1:0]. 1 ➔ The DB[1:0] are defined as KSTB[1:0] ◦ In Auto-Mode, the DB[1:0] is also defined as KF[1:0].

K_AUTO: Setup the scan mode. 1 ➔ Auto-Mode. The RA8825 will auto detect the key and store the code into AKD[6:0] for MPU reading. 0 ➔ Non-Auto-Mode. The RA8825 will not store the code to AKD[6:0]. The MPU has to read data from KSTB[1:0] and KSD[4:0] to make sure which key was pressed. Of course, MPU could know if not only one key pressed at the same time In Non-Auto-Mode.

IRE: Setup the Interrupt of Key-scan. 0 ➔ Hardware Interrupt disable while key was pressed. 1 ➔ Generate hardware interrupt while key was pressed.

KF[1:0]: Setup the frequency of Key-scan.

KF1	KF0	Pulse Width	Key-scan Cycle Time (4x5)
0	0	256us	1.024ms
0	1	512us	2.048ms
1	0	1.024ms	4.096ms
1	1	2.048ms	9.182ms

KSTB[1:0]: In Non-Auto-Mode, These two bits are used to setup the strobe for the Row of key matrix. If any key pressed, the MPU can read data from KSTB[1:0] and KSD[4:0] to make sure which key was pressed. The strobe data are also readable from Bit[6:5] of register KSDR.

[07h] Key-scan Data Register (KSDR) (Read Only)

If K_AUTO = 0:

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	SIRQ	KSTB1	KSTB0	KSD4	KSD3	KSD2	KSD1	KSD0

SIRQ: Indicate the interrupt of Key-scan. This bit was clear when REG[0Fh] bit 1 write “0”.

KSTB[1:0]: These two bit show which pin of KST[3:0] active.

KSD[4:0]: KIN Return Data. These bits are used in Non-Auto-Mode. The MPU can read data from KSTB[1:0] and KSD[4:0] to make sure which key was pressed.

If K_AUTO = 1:

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	SIRQ	AKD6	AKD5	AKD4	AKD3	AKD2	AKD1	AKD0

SIRQ: Indicate the interrupt of Key-scan. This bit was clear when REG[0Fh] bit 1 write “0”.

AKD[6:0]: Scan Data(Code). In Auto–Mode, the MPU read data from this register to know the status of key matrix. The RA8825 supports 4x5 key matrix -- total 20Keys. The BCD number of 0~19h are mapping to these keys.

AKD[6:0]	Scan Data
0~19h	Key No. Input
20~39h	Long Key No. Input
42	Key Release
Other	Reserved

[08h] Scroll Window Start X Register (SWSXR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	--	--	--	SSX4	SSX3	SSX2	SSX1	SSX0

SSX[4:0]: Setup Segment (X) start point of scroll window. The unit is 8-Pixels width.

[09h] Scroll Window Start Y Register (SWSYR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	--	--	SSY5	SSY4	SSY3	SSY2	SSY1	SSY0

SSY[5:0]: Setup the Common (Y) start point of scroll window. The unit is pixel.

[0Ah] Scroll Window Rang X Register (SWRXR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	--	--	--	SRX4	SRX3	SRX2	SRX1	SRX0

SRX[4:0]: Setup Segment (X) offset of scroll window. The unit is 8-Pixels width.

Note:

1. SRX must large or equal than 1, that means the minimum scroll range of X is 16 pixels.

2. The “SSX+SRX” can not exceed the range of Segment (X) of LCD panel. For example, if the panel resolution is 96x32, then SSX+SRX must less than 96/8=12. That means the maximum of “SSX+SRX” is 11.

[0Bh] Scroll Window Rang Y Register (SWRYR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	--	--	SRY5	SRY4	SRY3	SRY2	SRY1	SRY0

SRY[5:0]: Setup the Common (Y) offset of scroll window. The unit is pixel.

Note:

1. SRY must large or equal than 1, that means the minimum scroll range of Y is 2 pixels.

2. The “SSY+SRY” can not exceed the range of Common (Y) of LCD panel. For example, if the panel resolution is 96x32, then SSY+SRY must less than 32. That means the maximum of “SSY+SRY” is 31.

[0Ch] Scroll Offset Register (SCOR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SL7	SL6	SL5/SR5	SL4/SR4	SL3/SR3	SL2/SR2	SL1/SR1	SL0/SR0

SL[7:0]: Setup the shift unit of horizontal scroll. The unit is pixel and active when register SCR_DIR1 (REG[0Eh]bit 3) is clear to “0”.

SR[5:0]: Setup the shift unit of vertical scroll. The unit is pixel and active when register SCR_DIR1 (REG[0Eh]bit 3) is set to “1”.

In auto scroll mode, this register is also used to setup the start position of scroll of Common or Segment.

[0Dh] Auto-Scroll Control Register (ASCR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SPD3	SPD2	SPD1	SPD0	STP3	STP2	STP1	STP0

SPD[3:0]: Setup the speed of auto scroll.

SPD3	SPD2	SPD1	SPD0	Scroll Time
0	0	0	0	1 Unit
0	0	0	1	3 Units
0	0	1	0	5 Units
0	0	1	1	7 Units
0	1	0	0	17 Units
0	1	0	1	19 Units
0	1	1	0	21 Units
0	1	1	1	23 Units
1	0	0	0	129 Units
1	0	0	1	131 Units
1	0	1	0	133 Units
1	0	1	1	135 Units
1	1	0	0	145 Units
1	1	0	1	147 Units
1	1	1	0	149 Units
1	1	1	1	151 Units

1 Unit = 1 Frame Times

STP[3:0]: Setup the shift unit on auto scroll mode.

SPD3	SPD2	SPD1	SPD0	Shift Pixel
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

[0Eh] Scroll Control Register (SCCR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SCR_IMD1	SCR_IMD0	SCR_MD	SBUF	SCR_DIR1	SCR_DIR0	SCR_INTEN	AUTO_SCR

SCR_IMD[1:0]: The definition is as following and they are available at Auto–Scroll-Mode.
0X: Setup 1-pixel shift to caused interrupt(SCR_INTEN must be 1).
10: Setup 8-pixel shift to caused interrupt(SCR_INTEN must be 1)
11: Setup 16-pixel shift to caused interrupt(SCR_INTEN must be 1)

SCR_MD: Scroll Mode Select. 0 ➔ Non-Auto-Scroll, the scroll offset clear to "0". 1➔ Auto-Scroll Mode.
SBUF: Scroll-Buffer Control. 0 ➔ Scroll-Buffer disable. The scroll will not including the Scroll-Buffer, only for display area. 1➔ Scroll-Buffer enable. The scroll area is including the display and Scroll-Buffer.
SCR_DIR[1:0]: Select the direction of scroll.

SCR_DIR1	SCR_DIR0	Direction of Scroll
0	0	Left to Right(Horizontal)
0	1	Right to Left(Horizontal)
1	0	Up to Down(Vertical)
1	1	Down to Up(Vertical)

SCR_INTEN: Setup the scroll interrupt. 0 ➔ Scroll interrupt disable. 1 ➔ In auto scroll mode, when scroll 1, 8 or 16-pixels generate an interrupt to MPU.
AUTO_SCR: Auto-Scroll control. 0 ➔ Stop the Auto-Scroll. 1 ➔ Auto-Scroll going.

[0Fh] Interrupt Status Register (ISR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	--	--	--	--	--	SCR_I	KI	--

SCR_I: Scroll interrupt. 1 ➔ Interrupt for scroll complete，0 ➔ No scroll Interrupt.
KI: Key-scan interrupt. 1 ➔ Interrupt for key pressed. 0 ➔ No Key pressed Interrupt.

[10h] Contrast Adjust Register (CSTR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BR2	BR1	BR0	CT4	CT3	CT2	CT1	CT0

BR[2:0]: Setup the LCD Bias(Base on 128x33).

BR2	BR1	BR0	Bias
0	0	0	1/4
0	0	1	1/4.5
0	1	0	1/5
0	1	1	1/5.5
1	0	0	1/6
1	0	1	1/6.5
1	1	X	1/7

CT[4:0]: Setup the Contrast(32 Level). Normally depend on the liquid, power and panel size to adjust the best display quality.

CT4	CT3	CT2	CT1	CT0	Contrast
0	0	0	0	0	Light
0	0	0	0	1	↓
		:			
1	1	1	1	1	Dark

[11h] Driver Control Register1 (DRCR_A)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BOFF	EN_R	EN_G	ROFF	IDIR	--	CDIR	SDIR

BOFF: Booster control. 1 ➔ Internal Booster enable. 0➔ Internal Booster disabled and used external voltage.
EN_R: Reference voltage control. 1 ➔ Internal reference voltage enable for Regulator. 0 ➔ Disable the internal reference voltage. The Regulator use external reference voltage.
EN_G: V0 control. 1 ➔ The V0 is generated by internal Regulator. 0 ➔ Use external V0, and the EN_R and BOFF have to clear "0"(Off) to reduce power consumption.
ROFF: Voltage Follower control. 1 ➔ Internal Voltage Follower enable for LCD Bias voltage. 0 ➔ Disable internal Voltage Follower, and use external voltage to generate LCD Bias voltage. If use external Voltage Follower, then EN_G, EN_R and BOFF have to clear "0"(Off) to reduce power consumption.
IDIR: Icon sequency select. 0 ➔ Icon sequence arrange fix. 1 ➔ Icon sequence arrange in SDIR.
CDIR: Common sequency select. 0 ➔ Pins COM0~31 are mapping to Common 0~31. 1➔ Pins COM0~31 are mapping to Common 31~0.
SDIR: Segment sequency select. 0 ➔ Pins SEG0~127 are mapping to Segment 0~127. 1➔ Pins SEG0~127 are mapping to Segment 127~0.
Note: The IDIR must set to 1 when both of CDIR and SDIR set to 1.

[12h] Driver Control Register (DRCR_B)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	CK_BS1	CK_BS0	RR2	RR1	RR0	HD2	HD1	HD0

CK_BS[1:0]: Select the clock of Booster. Assume the RC oscillator clock is 45KHz.

CK_BS1	CK_BS0	Clock of Booster
0	0	SYS_CLK/2 → 22.5KHz
0	1	SYS_CLK/4 → 11.25KHz
1	0	SYS_CLK/6 → 7.5KHz
1	1	SYS_CLK/8 → 5.625KHz

RR[2:0]: Setup the Resistor Ratio of Regulator. The ratio is V_{REF} : $V_{0.}$

RR2	RR1	RR0	Resistor Ratio
0	0	0	X2
0	0	1	X2.5
0	1	0	X3
0	1	1	X3.5
1	0	0	X4
1	0	1	X4.5
1	1	0	X5
1	1	1	--

Note: Refer to Section 6-4-2 for the description of V_{REF}.

HD[2:0]: Setup the LCD driving current. Normally big panel use bigger driving current to void bad display quality.

HD2	HD1	HD0	Driving Current
0	0	0	Min
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	Max

[13h] Blink Timer Register (BLTR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BLK_EN	PBK_EN	--	GINV	BLT3	BLT2	BLT1	BLT0

BLK_EN: Blinking. 0 ➔ Blinking off. 1 ➔ Blinking on.
PBK_EN: Blinking for assigned area. 0 ➔ Blinking off. 1 ➔ Blinking on. The blinking area is depending on the scroll window. If BLK_EN set to "1", then the whole display on blinking.
GINV: Setup display reverse. 0 ➔ Normal display. 1 ➔ Display reverse.
BLT[3:0]: Setup blinking time.

BLT3	BLT2	BLT1	BLT0	Blink Time (Unit: Frames)
0	0	0	0	8
0	0	0	1	16
0	0	1	0	24
0	0	1	1	32
0	1	0	0	40
0	1	0	1	48

0	1	1	0	56
0	1	1	1	64
1	0	0	0	72
1	0	0	1	80
1	0	1	0	88
1	0	1	1	96
1	1	0	0	104
1	1	0	1	112
1	1	1	0	120
1	1	1	1	128

[14h] IO Direction Control Register (IODR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0

OE[7:0]: Select the I/O port direction. 0 ➔ Input. 1 ➔ Output.

[15h] IO Data Register (IODAR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	IOD7	IOD6	IOD5	IOD4	IOD3	IOD2	IOD1	IOD0

IO[7:0]: This register stores the input data of I/O port when I/O port is input mode.

[16h] EL Control Register (ELCR)

RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	EL_EN	--	--	--	ELT3	ELT2	ELT1	ELT0

EL_EN: EL signals output . 0 ➔ Off. 1 ➔ On.
ELT[3:0]: Setup the output time of EL signals.

ELT3	ELT2	ELT1	ELT0	Output Time(Sec)
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
0	1	0	1	10
0	1	1	0	12
0	1	1	1	14
1	0	0	0	16
1	0	0	1	18.
1	0	1	0	20
1	0	1	1	22
1	1	0	0	24
1	1	0	1	26

1	1	1	0	28
1	1	1	1	30

6. Function Description

6-1 MPU Interface

6-1-1 Parallel Interface

The MPU interface of RA8825 supports both 8080 and 6800 series with in 4-Bit or 8-bit bus width. If the "$\overline{C86}$" connects to GND, then the MPU is defined as 8080 type interface. If pin "$\overline{C86}$" connects to VDD, then it's defined as 6800 type interface. Refer to the Figure 6-2.

If the pin "BIT4" connects to GND, then the bus width of MPU interface is 8-Bit. If the pin "BIT4" connects to VDD, then the bus width is 4-Bit. And only the DB[3:0] of data bus are available.

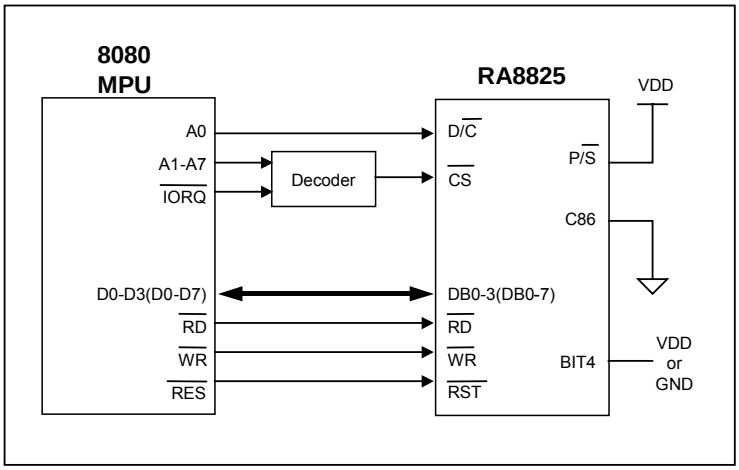


Figure 6-1: 8080 (4/8-Bit) MPU Interface

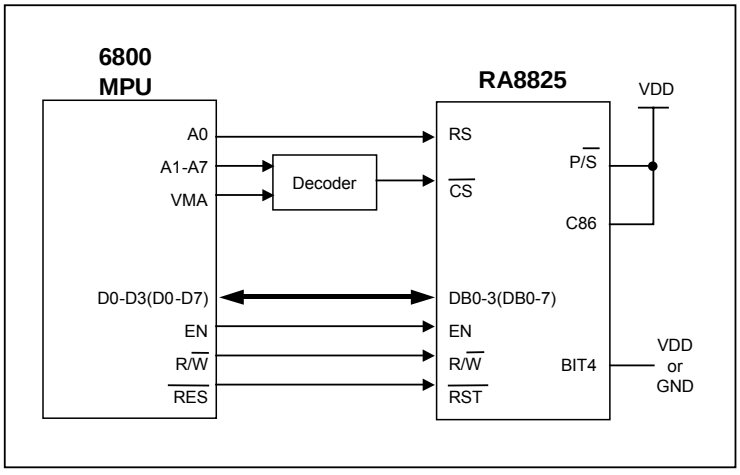


Figure 6-2: 6800 (4/8-Bit) MPU Interface

6-1-2 Serial Interface

The RA8825 aslo support three type serial interface. One is 3-Wires and the others are 4-Wires(A-Type, B-Type). This feature is control by the pin "P/$\overline{S}$" and DB[7:6]. Refer to Chapter 4-1. In serial mode the DB[7:6] are used as SMOD[1:0] to select the different serial mode. Please also refer to Table 6-1. The Figure 6-3 to 6-5 are the interface diagram of MPU and RA8825 which in serial mode. The 150pF capacitor is used to reduce the communication noise.

Table 6-1

SMOD	Serial Mode Interface
0 X	3-Wires. Use signals SCK, SDA and $\overline{CS}$.
1 0	4-Wires (A-Type). Use signals SCK, SDA, RS and $\overline{CS}$.
1 1	4-Wires (B-Type). Use signals SCK, SDO, SDI and $\overline{CS}$.

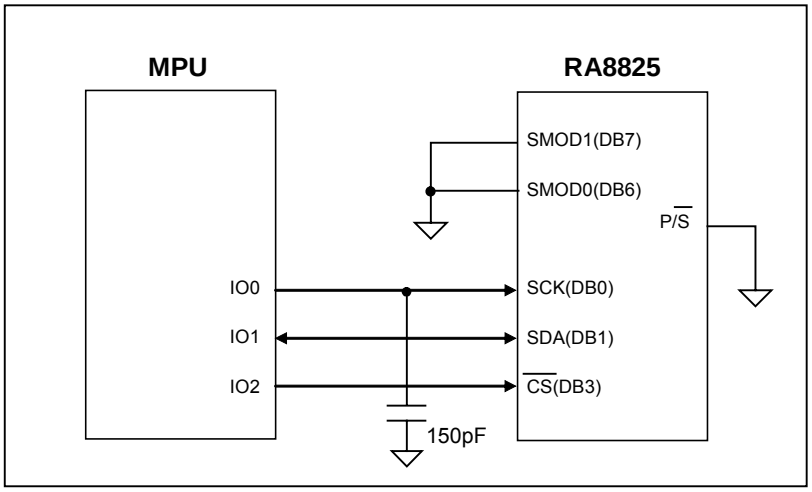


Figure 6-3: 3-Wires MPU interface

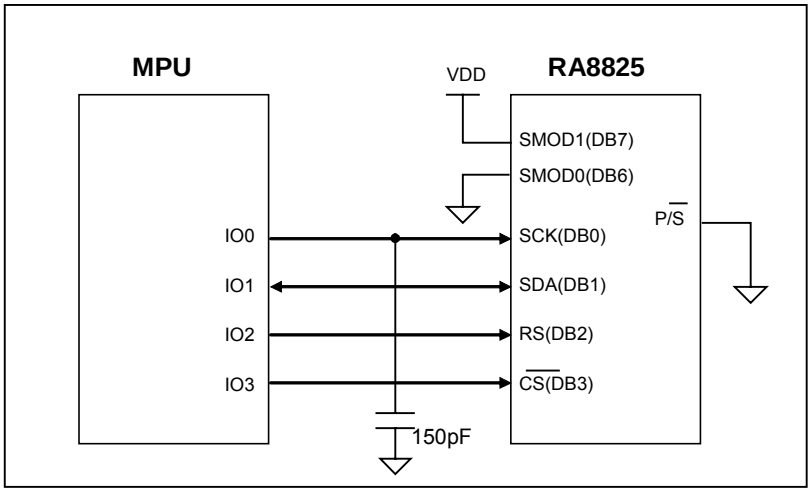


Figure 6-4: 4-Wires(A-Type) MPU interface

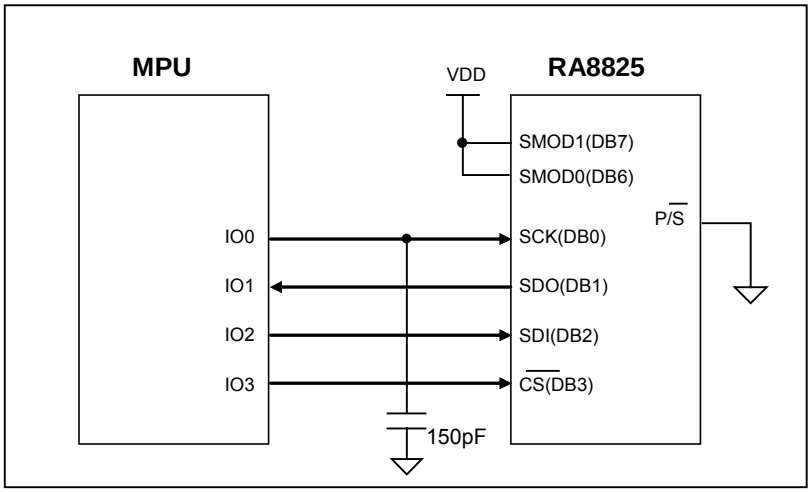


Figure 6-5: 4-Wires(B-Type) MPU interface

6-1-3 Register Read/Write

The RA8825 accepts two access cycles from MPU. One is read data from register or write data to register. Another is read data from memory or write data to memory. As description of Chapter 5-2, MPU must tell the RA8825 that which register will be access. Therefore the first data that write to RA8825 is to select the register number. And the second data is the exact data that writing into or reading from this register.

Because the features of RA8825 are controlled by the contents of internal registers, so if we write data to register is like to give a command to RA8825. Therefore we can say that the Register Access Cycle is same as Command Cycle.

The Figure 6-6 and 6-7 show the register access timing of 8080 MPU(8-Bit) with RA8825. Figure 6-8 and 6-9 show the register access timing of 6800MPU(8-Bit) interface. Figure 6-10 to 6-12 show the register access timing of serial interface.

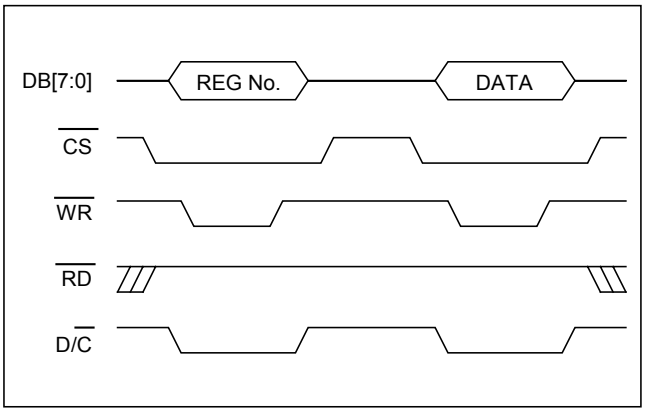


Figure 6-6: Register Wrie on 8080(8-Bit) I/F

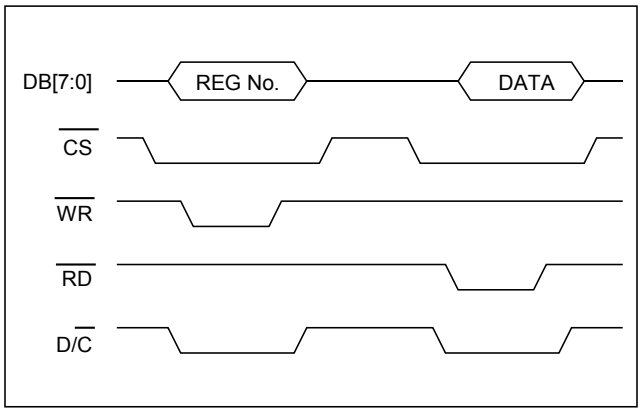


Figure 6-7: Register Read on 8080(8-Bit) I/F

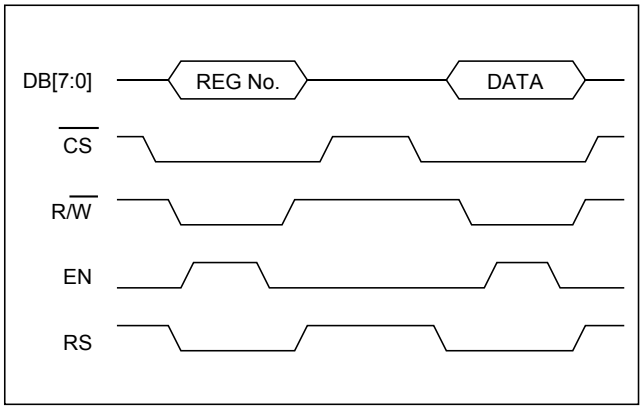


Figure 6-8: Register Write on 6800(8-Bit) I/F

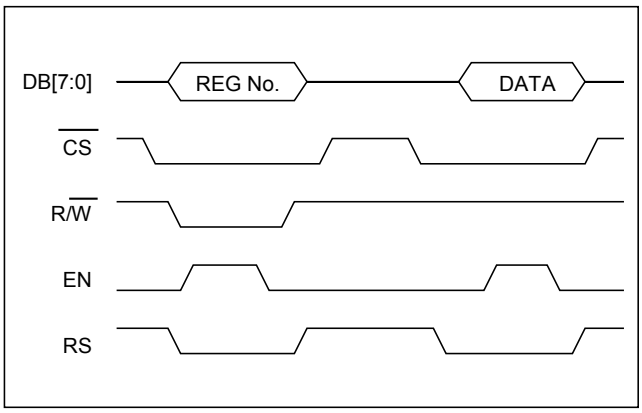


Figure 6-9: Register Read on 6800(8-Bit) I/F

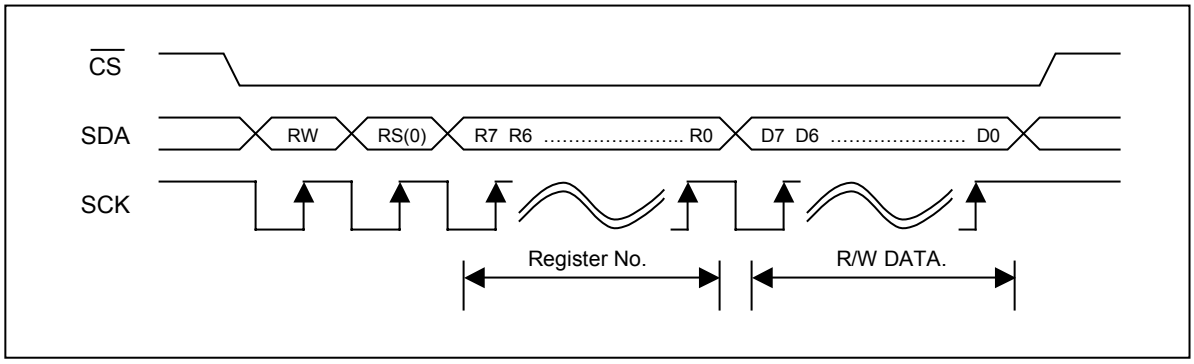


Figure 6-10: Register Read/Write Access on 3-Wires I/F

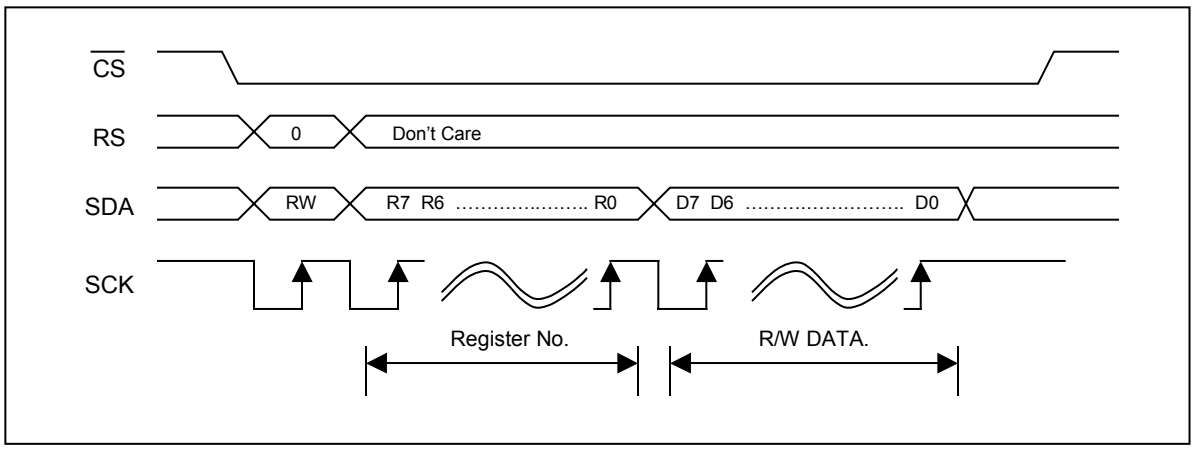


Figure 6-11: Register Read/Write Access on 4-Wires(A-Type) I/F

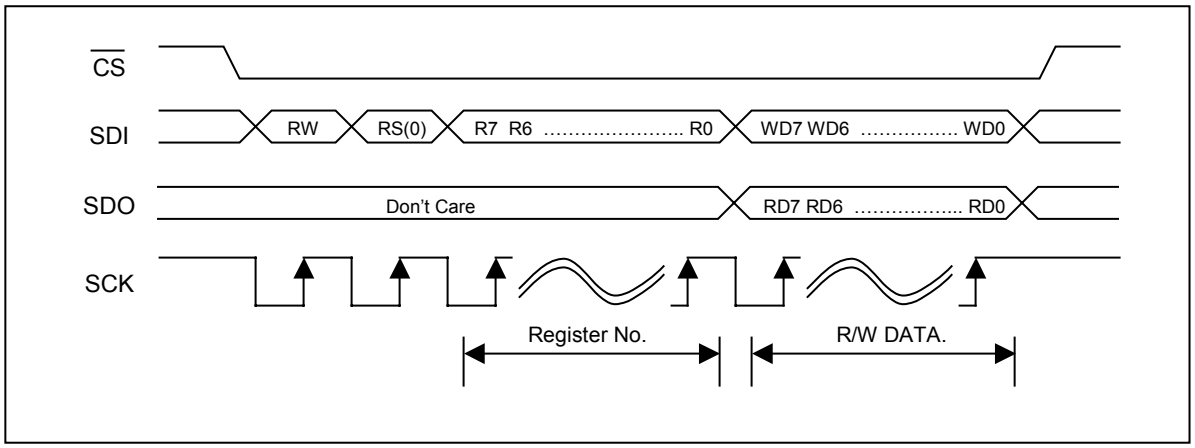


Figure 6-12: Register Read/Write Access on 4-Wires(B-Type) I/F

6-1-4 Memory Read/Write

Another cycle for MPU to RA8825 is memory Read/Write cycle. Normally it used to show information on the LCD screen. A memory writes means write a data into the mapping address that cursor located. After a memory write complete, the cursor will auto increase. And the data of next memory write will fill into the new memory address that new curser position located. Because all of the memory read/write cycles are transfer the display data, so we can abbreviate the name of Memory Access Cycle to Data Cycle.

The Figure 6-13 and 6-14 show the memory access timing of 8080 MPU(8-Bit) with RA8825. Figure 6-15 and 6-16 show the memory access timing of 6800MPU(8-Bit) interface. Figure 6-17 to 6-19 show the memory access timing of serial interface.

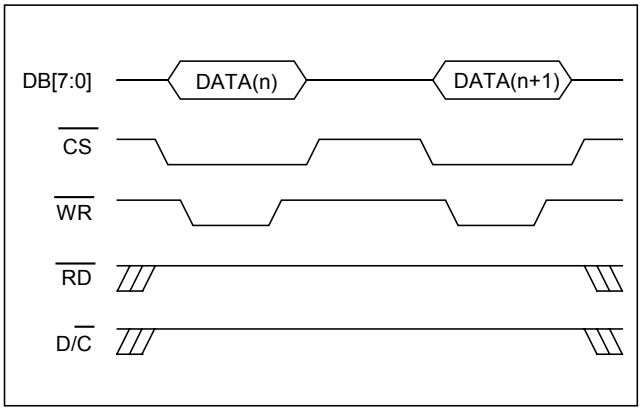


Figure 6-13: Memory Write on 8080(8-Bit) I/F

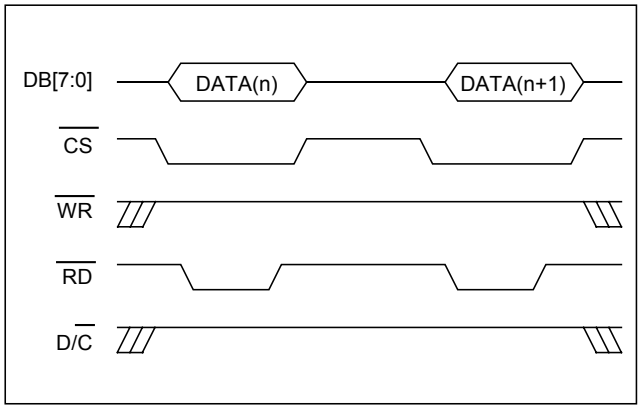


Figure 6-14: Memory Read on 8080(8-Bit) I/F

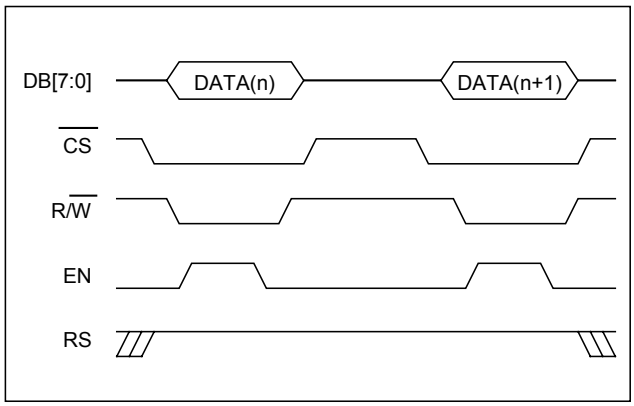


Figure 6-15: Memory Write on 6800(8-Bit) I/F

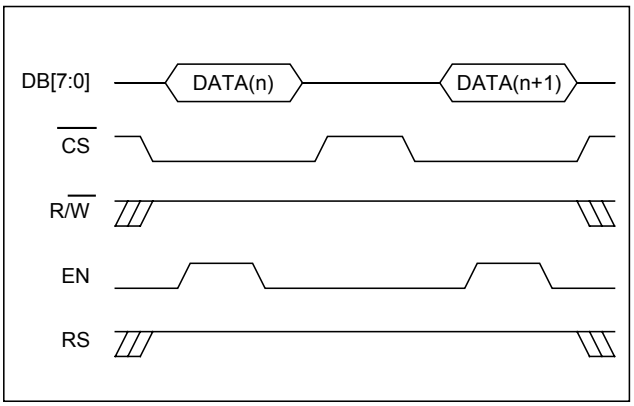


Figure 6-16: Memory Read on 6800(8-Bit) I/F

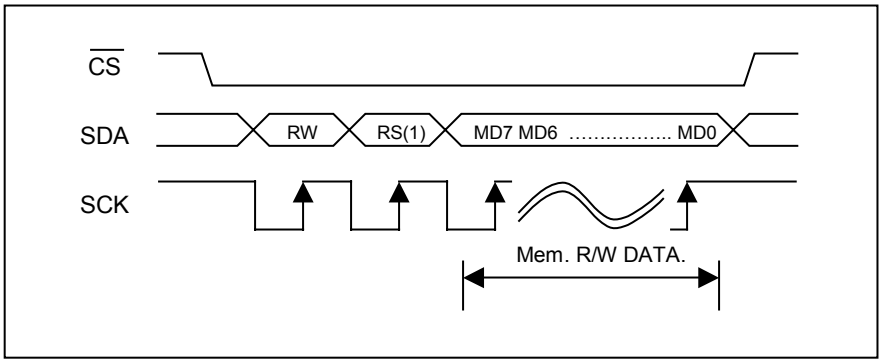


Figure 6-17: Memory Read/Write Access on 3-Wries I/F

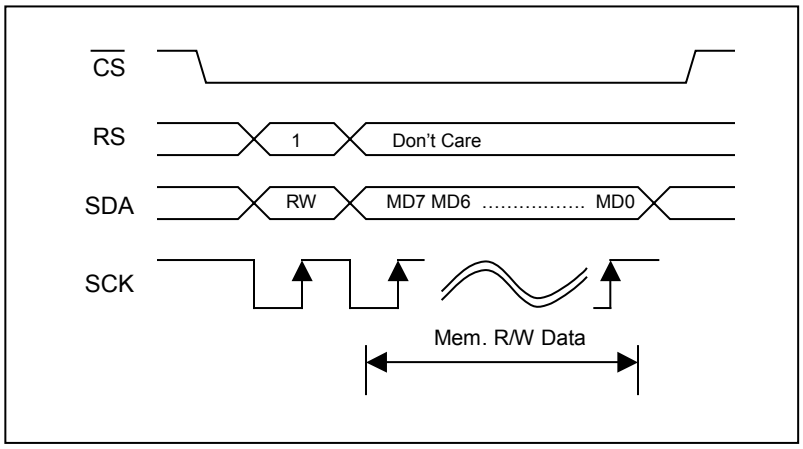


Figure 6-18: Memory Read/Write Access on 4-Wires(A-Type) I/F

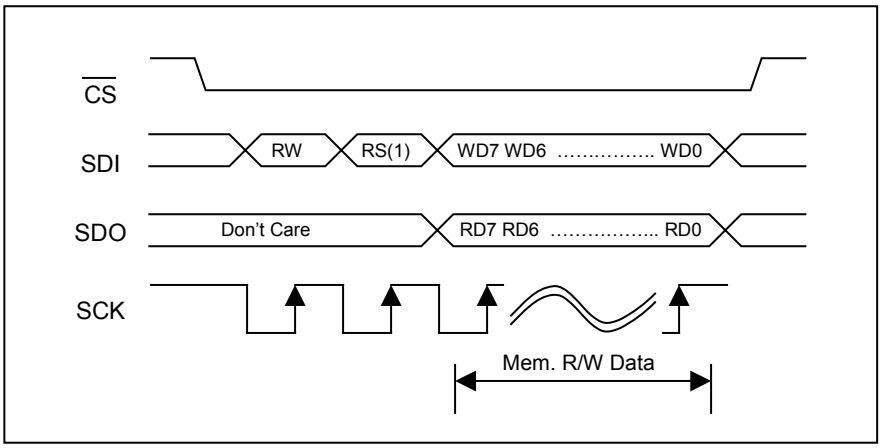


Figure 6-19: Memory Read/Write Access on 4-Wires(B-Type) I/F

6-2 Memory

The RA8825 built-in a 528Byte Display RAM. The display range of RA8825 is 128x33 dots. So it needs 528Byte(128*33/8) display RAM. In addition, RA8825 also built-in a scroll buffer to provide the scrlling and shiftting functions. The LCD control citcuit will read data of display RAM continuous and send to driver circuit.

6-3 System Clock

The clock of RA8825 is generated by the internal circuit and the clock frequency is around 55KHz. When the bit0(SLP) of register PWRR set to "1", then the clock will be stop.

Whe the input pin "CLK_SEL" set to "0", then system clock can also input from external clock through pin "EXT_CLK".

6-4 LCD Driver and Power Circuit

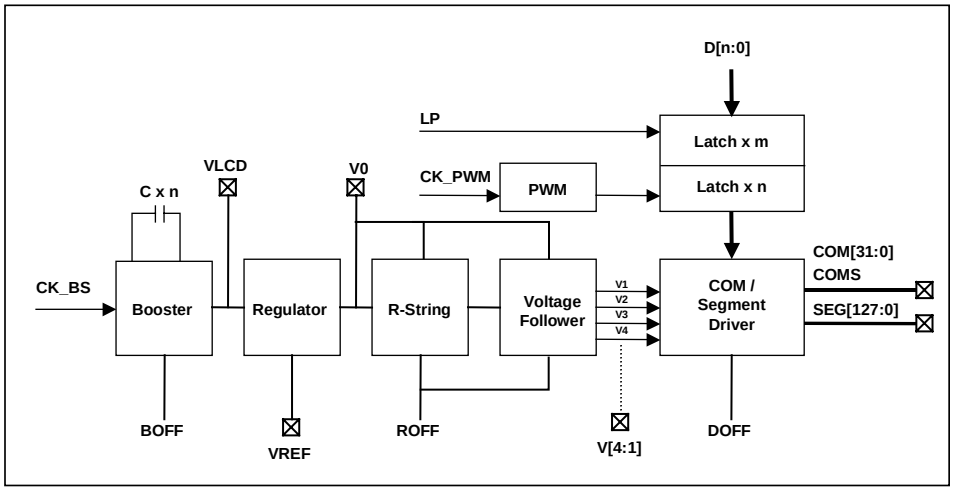


Figure 6-20: LCD Driver and Power Supply Circuit Block

The driver circuit of RA8825 is a low power design. The power supply circuit is consist of Booster, Voltage Regulator and Voltage Follower. For different requirement of power, the Driver Control Register(REG[11h]) is used to enable or disaable for related circuit.

The user could use the setting of register REG[11h] to select the internal or external power. Please refer to the following of Table 6-2 and Table 6-3.

Table 6-2: Power Circuit Setup

Driver Control Register (DRCR_A)	Functions	State '1' '0'
Bit7	Booster Circuit Control Bit	ON OFF
Bit6	Reference Voltage Circuit Control Bit	ON OFF
Bit5	Voltage Regulator Circuit Control Bit	ON OFF
Bit4	Voltage Follower Circuit Control Bit	ON OFF

Table 6-3: Setting Table of Power Circuit

Driver Control Register (DRCR_A) D7	D6	D5	D4	Booster	Voltage Regulator	Reference Voltage(VREF) of Voltage Regulator	Voltage Follower	External Power
1	1	1	1	ON	ON	Internal	ON	VDD
0	1	1	1	OFF	ON	Internal	ON	VLCD, VDD
1	0	1	1	ON	ON	External	ON	V_{REF}, VDD
0	0	1	1	OFF	ON	External	ON	VLCD, V_{REF}, VDD
0	0	0	1	OFF	OFF	Don't Need	ON	V0, VDD
0	0	0	0	OFF	OFF	Don't Need	OFF	V0~V4, VDD

6-4-1 Booster Circuit

The RA8825 built-in a Booster which create 3-times or 2-times of "V_{DD}-V_{SS}" that we called "VLCD". The VLCD is supply the power for next stage curcuit – Voltage Regulator and internal Driver cuicuit. If connect an 1uF capacitor on pin C1P and C1M, then the VLCD is eaual to 2*VDD. If the pin C2P and C2M also connect n 1uF capacitor then the VLCD is 3*VDD. Refer to the following description of Figure 6-21.

Because the RA8825 supports maximumn LCD panel is 128x33. Therefore sometimes you can get the good display quality that base on lower power such as 5V only. In that case, user only need to connect 5V to VDD, VLCD, C1P and C2P. And you do not need to add capacitor on C1P/C1M and C2P/C2M.

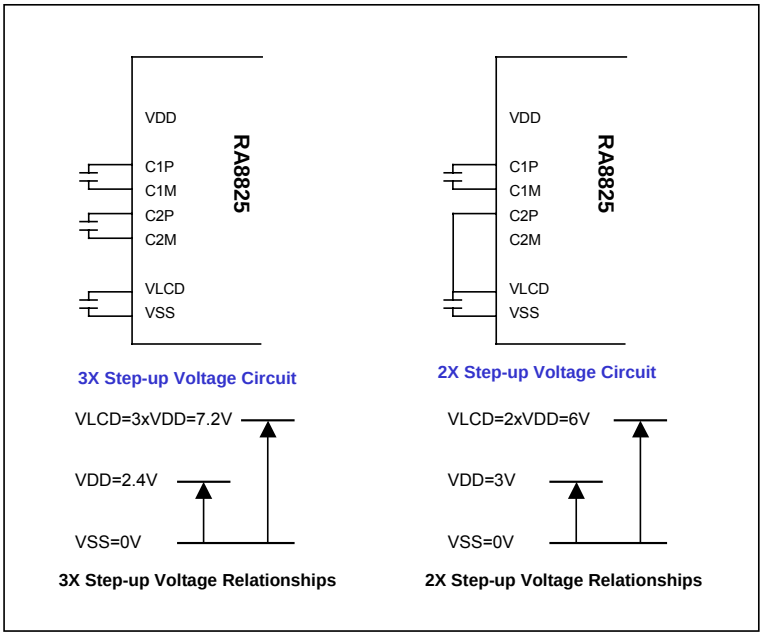


Figure 6-21: Application Circuit of Booster

The clock source of Booster is also control by register DRCR_B. Please refer to the description of REG[12h] in Chapter 5-2. Normally, if use the internal Driver Power, then the application circuit is follow Figure 6-22. If use external VLCD, that means do not use the internal Booster, then the connection is show as Figure 6-23. In Figure6-22 and 6-23, if use internal reference voltage then the VREF do not need to connect to FPC. But if connect VEF to FPC then have to add a external 0.1uF capacitor. To GND

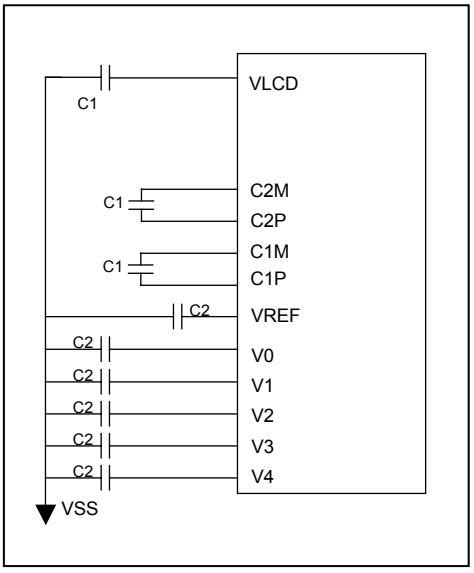


Figure 6-22: Internal VLCD(3*VDD)

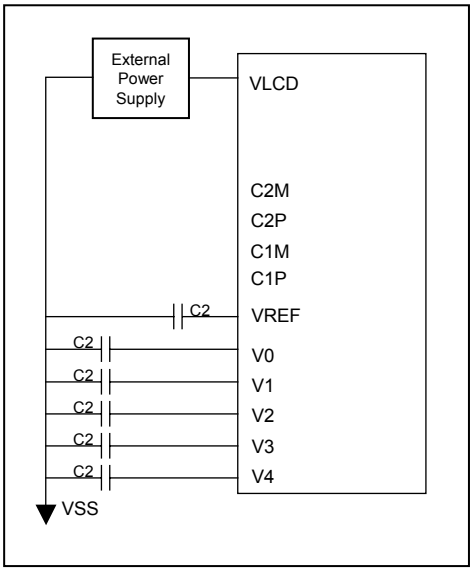


Figure 6-23: External VLCD

Note: The capacitor value of C1 is 1uF and C2 is 0.1uF.

6-4-2 Voltage Regulator

The Voltage Regulator is consists of Band-Gap and OP-Amp. The purpose is used to generated a stable power - V_0 for Voltage Follower. The RA8825 also built-in a 32-level adjust circuit and a fixed voltage – V_{IREF} to generate a reference voltage V_{REF}. This V_{REF} is for for Voltage Regulator to generated V_0. The basic formula is as following:

$$V_0 = (1+R1/R2) * V_{REF} = (1+R1/R2) * (0.096* (\alpha-31)+V_{IREF})$$

The α is the setting of CT[4:0] of Register CSTR. When CT[4:0]=1Fh then V_{REF}=V_{IREF}.

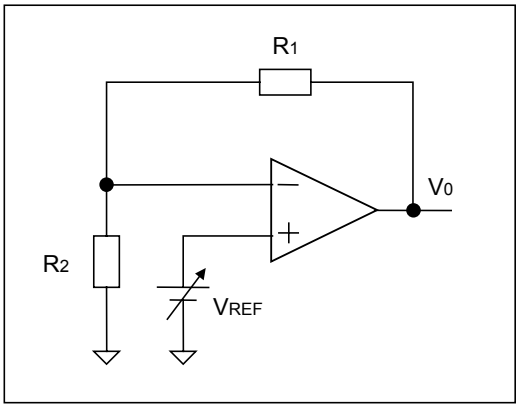


Figure 6-24: Voltage Regulator

The resistor ratio(V_{REF} and V_0) of Voltage Regulator is adjustable by register DRCR_B. There are total seven cases - 2/2.5/3/3.5/4/4.5/5X. Refer to the description of Bit[5:3] of register DRCR_B on Chapter 5-2. The Voltage Regulator also provide -0.05% auto adjust for temperature compensation.

The V_{REF} of RA8825 is supply from internal circuit or external V_{REF} Pin. Please refer to Table 6-4:

Table 6-4: Select V_{REF}

V_{REF} Type	DRCR-A Bit6 (EN_R)	DRCR-A Bit5 (EN_G)	Temperature Gradient	Unit	V_{REF}
Internal	1	1	-0.05	%/℃	$0.096* (\alpha-31)+V_{IREF}$
External	0	1	-	-	V_{REF} Pin
	X	0	-	-	

Normally the internal V_{IREF} value is 1.6V. When Voltage Regulator Circuit off(EN_G=0) then the Reference Voltage Circuit is be off too.

6-4-3 Voltage Follower

The internal Voltage Follower provides V0~V4 power for LCD Driver circuit. Of course, the user could select internal or external Voltage Follower. The relationship of V0~V4 and LVLCD is as following:

VLCD > V0 > V1 > V2 > V3 > V4 > GND

Figure 6-25A shows the circuit of using internal Voltage Follower. For external V0~V4, the connection is show as Figure 6-25B.

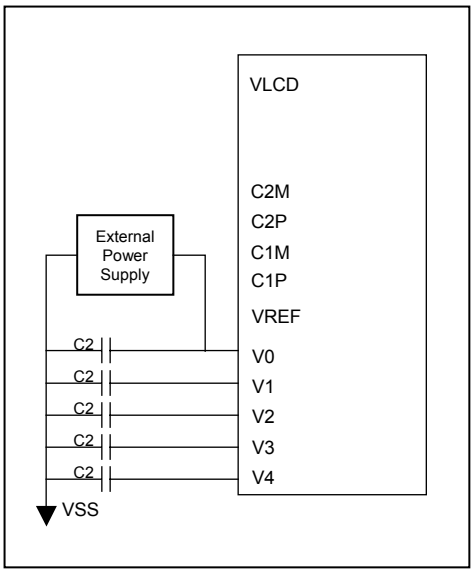


Figure 6-25A: Use Internal Voltage Follower

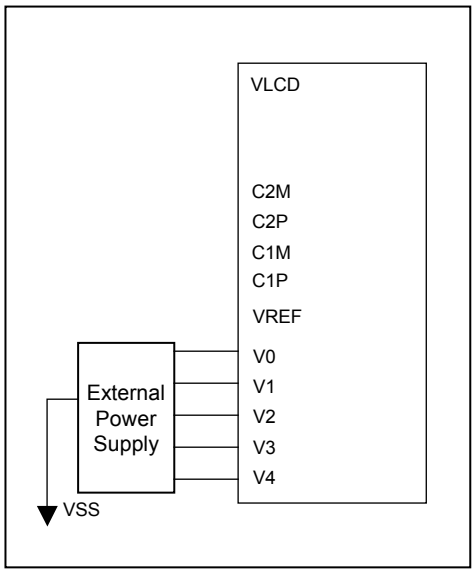


Figure 6-25B Use External Voltage Follower

6-4-4 LCD Driver

The Segment/Common Driver of RA8825 is used to latch the data of pre-stage, then send to Level Shifter for combination. The combined data will follow the Timing Generator to control the switchs then pass the V0~V4 to Common and Segment.

The LCD Bias of RA8825 is adjustable by register CSTR that from 1/4 to 1/7. The user can also adjust the display quality from this register. Meanwhile, the driving current is also adjustable by register DRCR_B that in order to meet different panel.

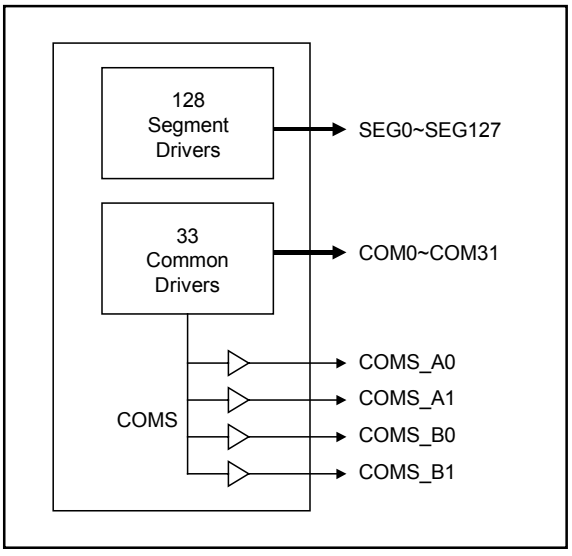


Figure 6-26：The Driver of Segment and Common

As Figure 6-26, the RA8825 provides 128 Segment and 33 Common signals. One of the Common signal – COMS is provide for the Icon of LCD Panel. The COMS_A[1:0] and COMS_B[1:0] are located on the both side of RA8825 that in order to easier layout for COG panel. The COMS_A[1:0] and COMS_B[1:0] have independent buffers, so if the area of Icon is bigger, then you can connect the COMS_A0 and COMS_A1 together. Or connect COMS_B0 and COMS_B1 together.

The DOFF_Z of register PWRR is used to cotrol the On/Off of LCD Panel, When DOFF_Z is set to "0" then LCD Driver was closed. At this state, the driver output signals COM0~COM31 and SEG0~SEG127 are connect to GND, and the screen of LCD Panel was Off.

6-5 Interrupt

The RA8825 provide a interrupt signal($\overline{INT}$) to response two possible interrupt:

- Scroll Interrupt - When the scroll window shifted 1, 8 or 16-pixels.
- Key-scan Interrupt - When a key was pressed.

The interrupt of above can be enabled or disable by register. The MPU can read the interrupt message form interrupt status register. The $\overline{INT}$ is active low, so when MPU detect the interrupt happen then must clear interrupt status for $\overline{INT}$ return to high. If user do not use the hardware interrupt($\overline{INT}$), then MPU can get the interrupt message by reading the status register.

6-6 Key-Scan

The RA8825 built-in 4x5 key-scan circuit for extra key board function to help user integrate a key matrix application. In auto-mode, MPU can read the key code from register to know the key was short-press, long-presee or key released. Use can also adjust the cycle time of key-scan. Figure 6-27 is the simple application curcuit. Table 6-5 is the mapping keyboard code of key matrix as Figure 6-27. So MPU knows which ket be pressed by reading register – KSDR. For Key-Scan application, you have to add the external pull-hi resistors on KIN[4:0].

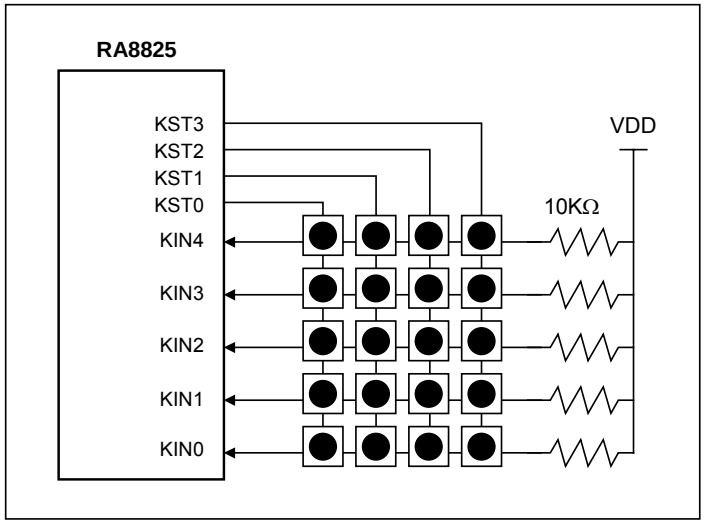


Figure 6-27: 4x5 Key Matrix Curcuit

Table 6-5: Keyboard Code of Auto-Mode

	Short-Press				Long-Press			
	KST3	KST2	KST1	KST0	KST3	KST2	KST1	KST0
KIN0	15h	10h	05h	00h	35h	30h	25h	20h
KIN1	16h	11h	06h	01h	36h	31h	26h	21h
KIN2	17h	12h	07h	02h	37h	32h	27h	22h
KIN3	18h	13h	08h	03h	38h	33h	28h	23h
KIN4	19h	14h	09h	04h	39h	34h	29h	24h

In Auto-Mode of Key-Scan function, if the key pressed over one second, then the RA8825 will cause interrupt and change the data of register – KSDR to a long-press code. Therefore MPU knows which key was pressed ove one second.

6-7 I/O Port

The RA8825 provide eight Igeneral purpose I/O pins. Each I/O pin is easy to setup as input or output. They can use to drive LED, wakeup the RA8825 or provide information for whole system.

6-8 EL Signals

The RA8825 provide two special signals for EL driver circuit. The signals active time can also setup by register ELCR. The waveform and application are show as Figure 6-28 and 6-29.

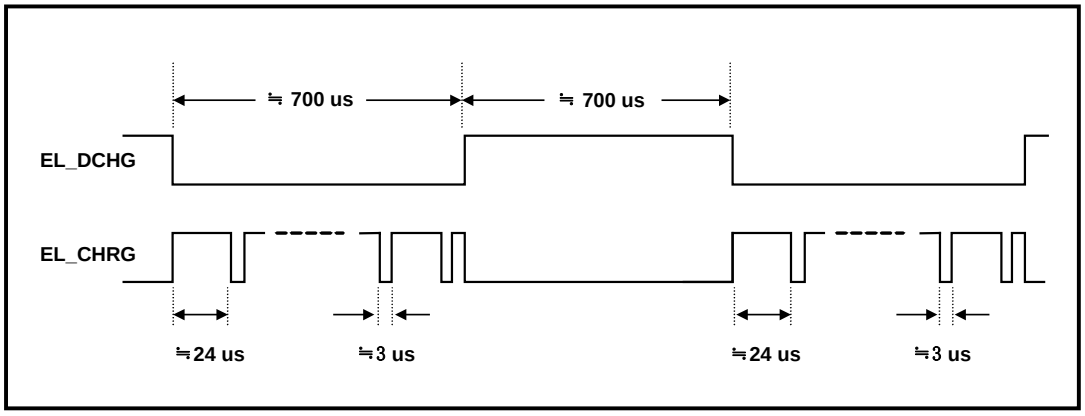


Figure 6-28: Control Signals for EL Driver

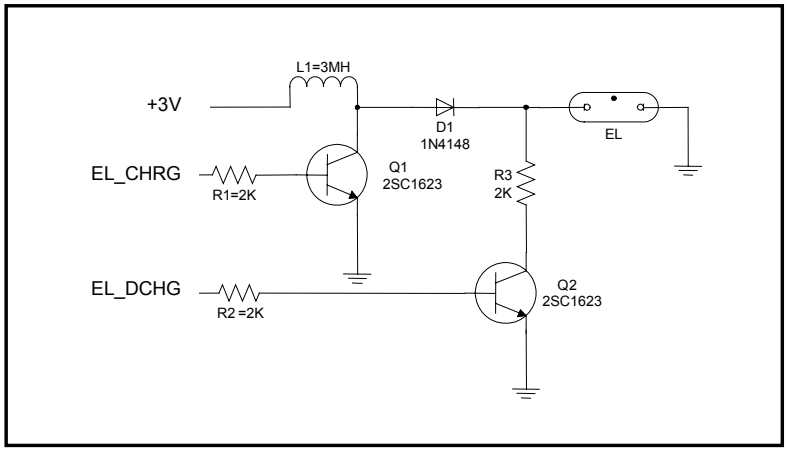


Figure 6-29: EL Driver Circuit

6-9 Power Control

The RA8825 supports Normal Mode and Sleep Mode for operation. If write “0” to bit0 of register PWRR, then RA8825 will enter sleep mode. The functions of LCD display and driver will stop. All of the signals of COM and SEG will keep low, Key Strobe signals will keep high, and I/O keep the original state. Because the RC clock was stop, so the power consumption is very samll.

The RA8825 provide three way to wake up the system:

1. Write ”1” to the bit0 of register PWRR.
2. Key-scan to wake up
3. I/O wake up

In wake up phase, the RA8825 will wake up the RC oscillator first, and it will take around 250ms. Then the RA8825 is enable to accept the command from MPU and LCD driver wake up for activity.

7. Display Functions

7-1 Data Write Mode

The RA8825 is fill the bit map data into display memory directly. And when write the data into memory, the data will show on the screen that cursor pointed.

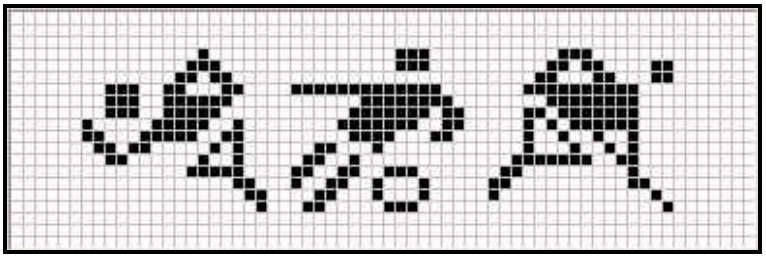


Figure 7-1: Graphics Mode Display

The display RAM size of RA8825 is 528Byte(128*33/8). Each memory bit is mapping to the LCD panel. If the data is “1” then the mapped dot is turn on. Please refer the Figure 7-3.

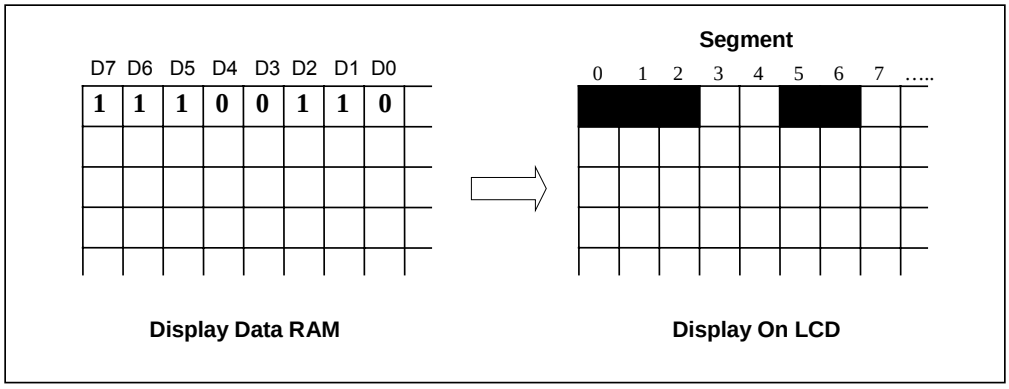


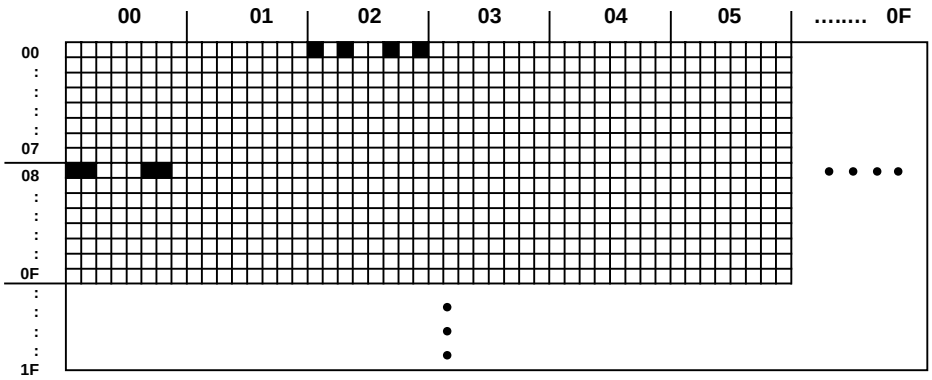
Figure 7-2: Display Data Mapping to the Screen

The RA8825 also provide a clean feature to clear all of the display RAM. If the “MCLR” of register PWRR is set to “1”, then all of contents of Display RAM will be clear to “0”. And the user could select the blinking or inverse through register BLTR. The blinking are is assigned by the size of Scroll Window.

7-2 Cursor Setting

7-2-1 Cursor Position and Shift

RA8825 panel size maximal can to support 128(Segment) x 33(Common), but the unit of Segment address is 8-Bits, so if we want to show the bitmap A5h in Left-Up corner of panel that the seventeen position, we have to set cursor position register(REG[05h] [06h]) X-CUR = 02h, Y-CUR = 00h, In the same way, we want to show C6h bitmap in the ninth row of panel, we need set cursor position register X-CUR = 00h, Y-CUR = 08h, Please refer the Figure 7-3.
RA8825 use Cursor Position Register X-CUR and Y-CUR to set cursor address, if fill data to display RAM, the cursor will auto increase, and the boundry is the display window.



128(Segment) x 32(Common)

Figure 7-3: An Example for Cursor Setting

7-2-2 Cursor Display and Blink

The RA8825 provide cursor On/Off and blinking features. These functions are control by register CURCR. The cycle time of blinking is depend on the setting of register BLTR. The range is from 8 to 128 frames.

7-3 Display Window

Normally, the Display Window size is same as LCD panel. It's setting by register SYSR. The maximumnis range is 128(Segment)x32(Common). The RA8825 provide a extran Common(Com-S) as the selection of Icon. Therefore the total 128 Icon for usage. Before access the Com-S, the register Y-CUR has set to 50h, then program the X-CUR to select Icon.

The RA8825 provides two positions for the panel layout of COM-S. It's convenient for user to deisgn the position of Icon fro their application. Refer to the Figure 7-6.

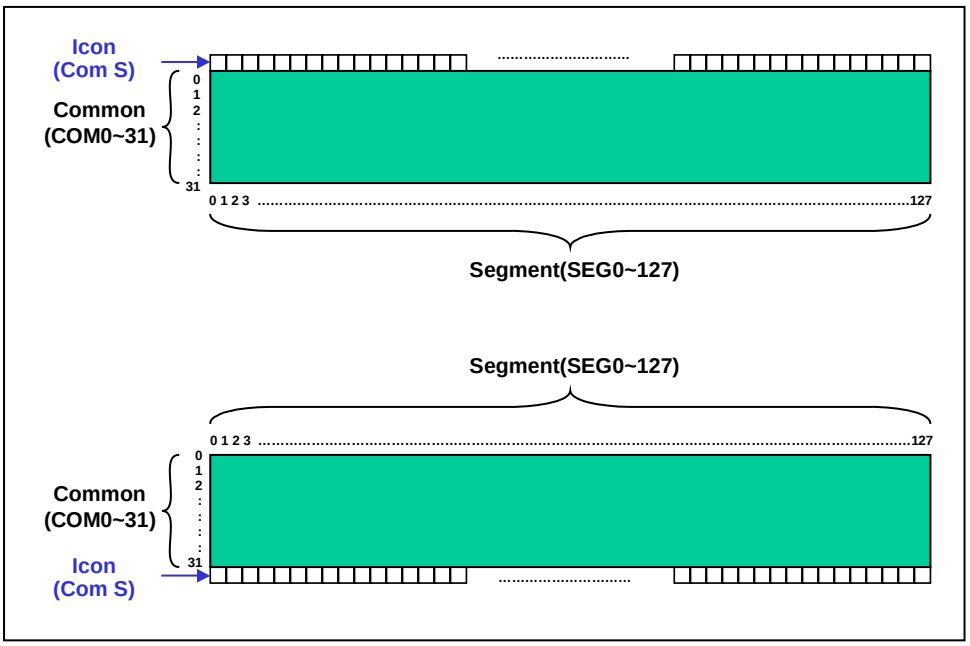


Figure 7-4: Display Window and Icon

7-4 Horizontal Scroll

The RA8825 provide Horizontal Scroll feature. User could assign the range of srolling, scroll unit and speed. Refer to the following example as Figure 7-7. The scroll unit is set to 2 pixels.

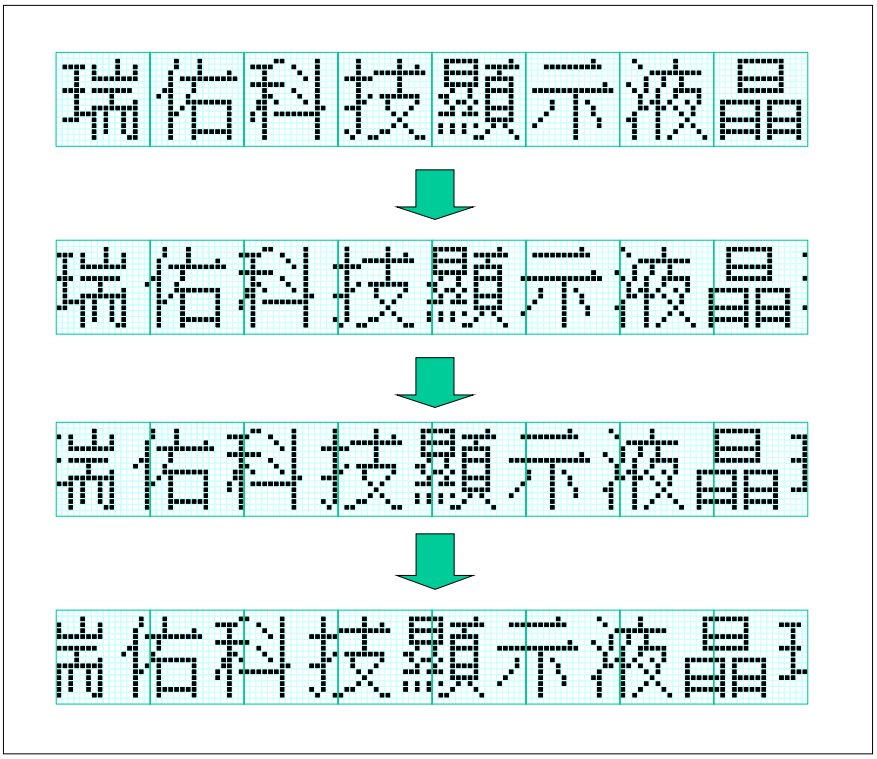


Figure 7-5: Horizontal Scroll

The RA8825 allows horizontal scroll for right or left way. The user could use the scrolling buffer to show the Shift funtion. For example, store the data on the Horizontal Scroll Buffer first, then fill the new data into the buffer that after the screen shift 16pixels. You can repeat these action and find the screen is shift like caption of advertisement. The Figure 7-8 is an example to show he Horizontal Shift. The shift unit is 8pixels and the gray area is the scroll buffer. The displat data will not show on the screen.

Please refer to application note for the related horizontal scroll feature.

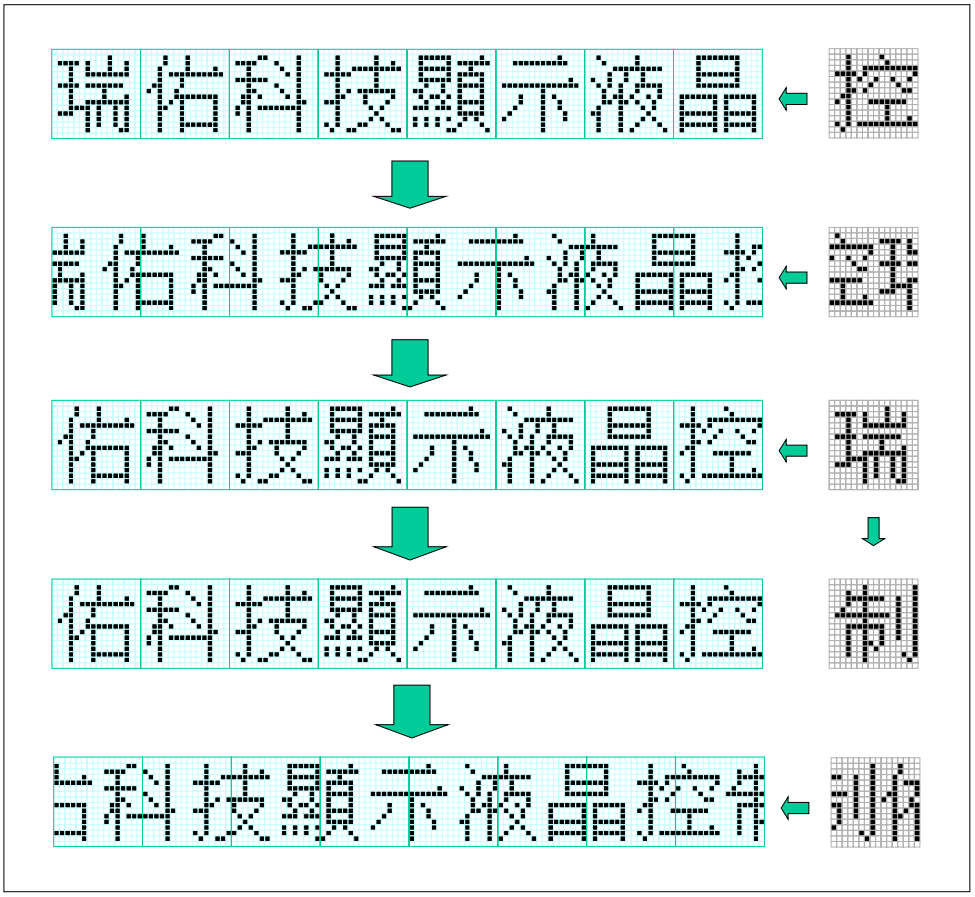


Figure 7-6: Horizontal Shift

7-5 Vertical Scroll

The RAS8825 alos provides the Vertical Scroll and Shift features that like horizontal function. User could assign the range of srolling, scroll unit and speed. Refer to the following example as Figure 7-9. The vertical scroll unit is set to 2 pixels.

The RA8825 allows vertical scroll for up or down way. The user could use the scrolling buffer to show the Shift funtion. For example, store the data on the Vertical Scroll Buffer first, then fill the new data into the buffer that after the screen shift 16pixels. Please refer to application note for the related vertical scroll features.

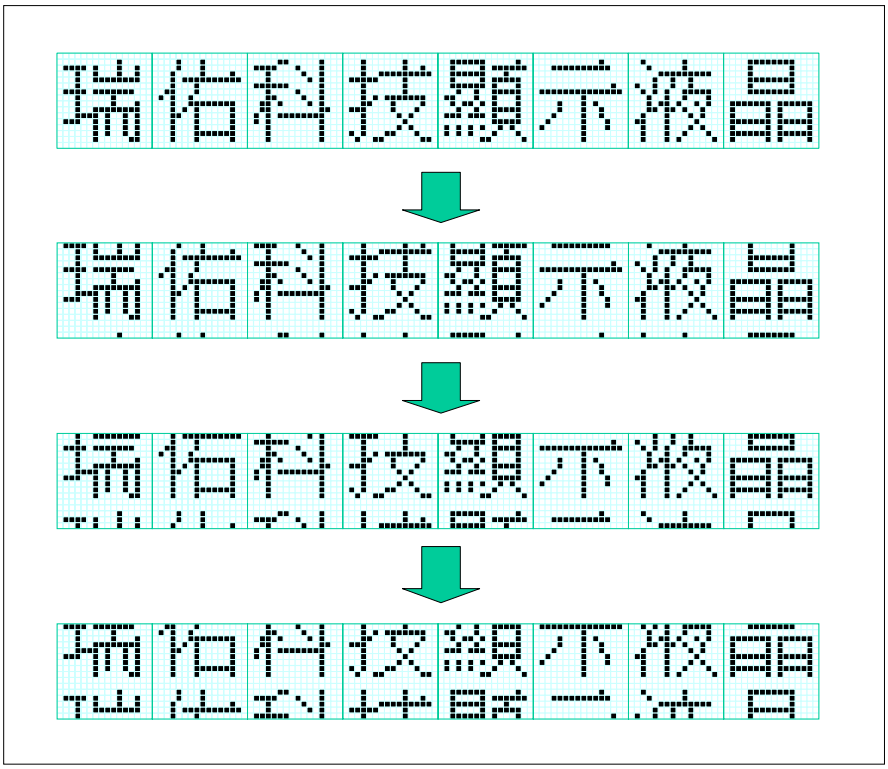


Figure 7-9: Vertical Scroll

8. Pin Diagram

8-1 COG Pad

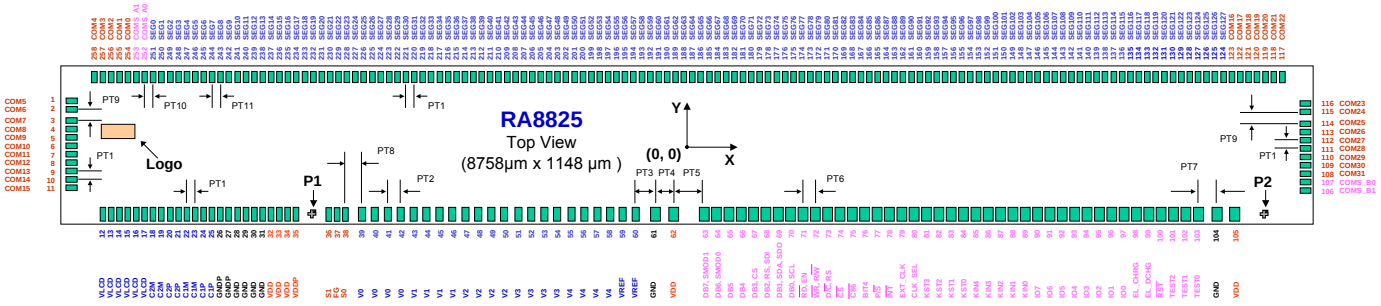
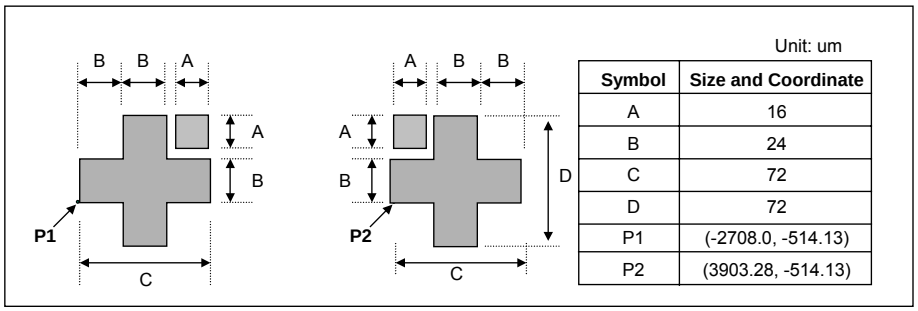


Figure 8-1：Pin Diagram

Table 8-1：Bump Size and Pitch

Chip Size	8758 μ m x 1148 μ m	
Bump Size	Pad 1~11, PAD 106~116 (COM Pads)	**74 μ m x 38 μ m**
	Pad 117~258 (SEG Pads, COM Pads), Pad 12~60 (Power Pads)	**38 μ m x 74 μ m**
	Pad 61~105 (MCU Pads)	67.4 μ m x 84 μ m
Bump Pitch	PT1: Pad 1~2, 3~11, 12~35, 36~38, 106~114, 115 to 116, 117~258	57 μ m
	PT2: Pad 39~60	100 μ m
	PT3: Pad 60 to 61	148.5 μ m
	PT4: Pad 61 to 62	100 μ m
	PT5: Pad 62 to 63	300 μ m
	PT6: Pad 63~103	80 μ m
	PT7: Pad 103 to 105	120 μ m
	PT8: Pad 38 to 39	78.5 μ m
	PT9: Pad 2 to 3, 114 to 115	80.6 μ m
	PT10: Pad 123 to 124, 251 to 252	74.1 μ m
	PT11: Pad 131 to 132, 147 to 148, 163 to 164, 179 to 180, 195 to 196, 211 to 212, 227 to 228, 243 to 244	74.6 μ m
Bump Height	15±3 μ m	



Unit: um

Symbol	Size and Coordinate
A	16
B	24
C	72
D	72
P1	(-2708.0, -514.13)
P2	(3903.28, -514.13)

Figure 8-2：Fixed Point Dimension

8-2 Pad X/Y Coordinate

Pad No.	Pad Name	X	Y
1	COM5	-4313	293.3
2	COM6	-4313	236.3
3	COM7	-4313	155.7
4	COM8	-4313	98.7
5	COM9	-4313	41.7
6	COM10	-4313	-15.3
7	COM11	-4313	-72.3
8	COM12	-4313	-129.3
9	COM13	-4313	-186.3
10	COM14	-4313	-243.3
11	COM15	-4313	-300.3
12	VLCD	-4088	-507.3
13	VLCD	-4031	-507.3
14	VLCD	-3974	-507.3
15	VLCD	-3917	-507.3
16	VLCD	-3860	-507.3
17	VLCD	-3803	-507.3
18	C2M	-3746	-507.3
19	C2M	-3689	-507.3
20	C2P	-3632	-507.3
21	C2P	-3575	-507.3
22	C1M	-3518	-507.3
23	C1M	-3461	-507.3
24	C1P	-3404	-507.3
25	C1P	-3347	-507.3
26	GNDP	-3283.7	-507.3
27	GNDP	-3226.7	-507.3
28	GND	-3169.7	-507.3
29	GND	-3112.7	-507.3
30	GND	-3055.7	-507.3
31	GND	-2998.7	-507.3
32	VDD	-2941.7	-507.3

Pad No.	Pad Name	X	Y
33	VDD	-2884.7	-507.3
34	VDD	-2827.7	-507.3
35	VDDP	-2770.7	-507.3
36	S1	-2575	-507.1
37	FG	-2520	-507.1
38	S0	-2465	-507.1
39	V0	-2386.5	-507.3
40	V0	-2286.5	-507.3
41	V0	-2186.5	-507.3
42	V0	-2086.5	-507.3
43	V1	-1986.5	-507.3
44	V1	-1886.5	-507.3
45	V1	-1786.5	-507.3
46	V1	-1686.5	-507.3
47	V2	-1586.5	-507.3
48	V2	-1486.5	-507.3
49	V2	-1386.5	-507.3
50	V2	-1286.5	-507.3
51	V3	-1186.5	-507.3
52	V3	-1086.5	-507.3
53	V3	-986.5	-507.3
54	V3	-886.5	-507.3
55	V4	-786.5	-507.3
56	V4	-686.5	-507.3
57	V4	-586.5	-507.3
58	V4	-486.5	-507.3
59	VREF	-386.5	-507.3
60	VREF	-286.5	-507.3
61	GND	-138	-507.3
62	VDD	-38	-507.3
63	DB7	262	-507.3
64	DB6	342	-507.3

Pad No.	Pad Name	X	Y
65	DB5	422	-507.3
66	DB4	502	-507.3
67	DB3	582	-507.3
68	DB2	662	-507.3
69	DB1	742	-507.3
70	DB0	822	-507.3
71	$\overline{RD}$	902	-507.3
72	$\overline{WR}$	982	-507.3
73	D/$\overline{C}$	1062	-507.3
74	$\overline{CS}$	1142	-507.3
75	$\overline{C86}$	1222	-507.3
76	BIT4	1302	-507.3
77	P/$\overline{S}$	1382	-507.3
78	$\overline{INT}$	1462	-507.3
79	EXT_CLK	1542	-507.3
80	CLK_SEL	1622	-507.3
81	KST3	1702	-507.3
82	KST2	1782	-507.3
83	KST1	1862	-507.3
84	KST0	1942	-507.3
85	KIN4	2022	-507.3
86	KIN3	2102	-507.3
87	KIN2	2182	-507.3
88	KIN1	2262	-507.3
89	KIN0	2342	-507.3
90	IO7	2422	-507.3
91	IO6	2502	-507.3
92	IO5	2582	-507.3
93	IO4	2662	-507.3
94	IO3	2742	-507.3
95	IO2	2822	-507.3
96	IO1	2902	-507.3
97	IO0	2982	-507.3
98	EL_CHRG	3062	-507.3

Pad No.	Pad Name	X	Y
99	EL_DCHG	3142	-507.3
100	$\overline{RST}$	3222	-507.3
101	TEST2	3302	-507.3
102	TEST1	3382	-507.3
103	TEST0	3462	-507.3
104	GND	3582	-507.3
105	VDD	3702	-507.3
106	COMS_B1	4313	-300.3
107	COMS_B0	4313	-243.3
108	COM31	4313	-186.3
109	COM30	4313	-129.3
110	COM29	4313	-72.3
111	COM28	4313	-15.3
112	COM27	4313	41.7
113	COM26	4313	98.7
114	COM25	4313	155.7
115	COM24	4313	236.3
116	COM23	4313	293.3
117	COM22	4106	507.3
118	COM21	4049	507.3
119	COM20	3992	507.3
120	COM19	3935	507.3
121	COM18	3878	507.3
122	COM17	3821	507.3
123	COM16	3764	507.3
124	SEG127	3689.9	507.3
125	SEG126	3632.9	507.3
126	SEG125	3575.9	507.3
127	SEG124	3518.9	507.3
128	SEG123	3461.9	507.3
129	SEG122	3404.9	507.3
130	SEG121	3347.9	507.3
131	SEG120	3290.9	507.3
132	SEG119	3216.3	507.3

Pad No.	Pad Name	X	Y
133	SEG118	3159.3	507.3
134	SEG117	3102.3	507.3
135	SEG116	3045.3	507.3
136	SEG115	2988.3	507.3
137	SEG114	2931.3	507.3
138	SEG113	2874.3	507.3
139	SEG112	2817.3	507.3
140	SEG111	2760.3	507.3
141	SEG110	2703.3	507.3
142	SEG109	2646.3	507.3
143	SEG108	2589.3	507.3
144	SEG107	2532.3	507.3
145	SEG106	2475.3	507.3
146	SEG105	2418.3	507.3
147	SEG104	2361.3	507.3
148	SEG103	2286.7	507.3
149	SEG102	2229.7	507.3
150	SEG101	2172.7	507.3
151	SEG100	2115.7	507.3
152	SEG99	2058.7	507.3
153	SEG98	2001.7	507.3
154	SEG97	1944.7	507.3
155	SEG96	1887.7	507.3
156	SEG95	1830.7	507.3
157	SEG94	1773.7	507.3
158	SEG93	1716.7	507.3
159	SEG92	1659.7	507.3
160	SEG91	1602.7	507.3
161	SEG90	1545.7	507.3
162	SEG89	1488.7	507.3
163	SEG88	1431.7	507.3
164	SEG87	1357.1	507.3
165	SEG86	1300.1	507.3
166	SEG85	1243.1	507.3

Pad No.	Pad Name	X	Y
167	SEG84	1186.1	507.3
168	SEG83	1129.1	507.3
169	SEG82	1072.1	507.3
170	SEG81	1015.1	507.3
171	SEG80	958.1	507.3
172	SEG79	901.1	507.3
173	SEG78	844.1	507.3
174	SEG77	787.1	507.3
175	SEG76	730.1	507.3
176	SEG75	673.1	507.3
177	SEG74	616.1	507.3
178	SEG73	559.1	507.3
179	SEG72	502.1	507.3
180	SEG71	427.5	507.3
181	SEG70	370.5	507.3
182	SEG69	313.5	507.3
183	SEG68	256.5	507.3
184	SEG67	199.5	507.3
185	SEG66	142.5	507.3
186	SEG65	85.5	507.3
187	SEG64	28.5	507.3
188	SEG63	-28.5	507.3
189	SEG62	-85.5	507.3
190	SEG61	-142.5	507.3
191	SEG60	-199.5	507.3
192	SEG59	-256.5	507.3
193	SEG58	-313.5	507.3
194	SEG57	-370.5	507.3
195	SEG56	-427.5	507.3
196	SEG55	-502.1	507.3
197	SEG54	-559.1	507.3
198	SEG53	-616.1	507.3
199	SEG52	-673.1	507.3
200	SEG51	-730.1	507.3

Pad No.	Pad Name	X	Y
201	SEG50	-787.1	507.3
202	SEG49	-844.1	507.3
203	SEG48	-901.1	507.3
204	SEG47	-958.1	507.3
205	SEG46	-1015.1	507.3
206	SEG45	-1072.1	507.3
207	SEG44	-1129.1	507.3
208	SEG43	-1186.1	507.3
209	SEG42	-1243.1	507.3
210	SEG41	-1300.1	507.3
211	SEG40	-1357.1	507.3
212	SEG39	-1431.7	507.3
213	SEG38	-1488.7	507.3
214	SEG37	-1545.7	507.3
215	SEG36	-1602.7	507.3
216	SEG35	-1659.7	507.3
217	SEG34	-1716.7	507.3
218	SEG33	-1773.7	507.3
219	SEG32	-1830.7	507.3
220	SEG31	-1887.7	507.3
221	SEG30	-1944.7	507.3
222	SEG29	-2001.7	507.3
223	SEG28	-2058.7	507.3
224	SEG27	-2115.7	507.3
225	SEG26	-2172.7	507.3
226	SEG25	-2229.7	507.3
227	SEG24	-2286.7	507.3
228	SEG23	-2361.3	507.3
229	SEG22	-2418.3	507.3
230	SEG21	-2475.3	507.3
231	SEG20	-2532.3	507.3
232	SEG19	-2589.3	507.3
233	SEG18	-2646.3	507.3
234	SEG17	-2703.3	507.3

Pad No.	Pad Name	X	Y
235	SEG16	-2760.3	507.3
236	SEG15	-2817.3	507.3
237	SEG14	-2874.3	507.3
238	SEG13	-2931.3	507.3
239	SEG12	-2988.3	507.3
240	SEG11	-3045.3	507.3
241	SEG10	-3102.3	507.3
242	SEG9	-3159.3	507.3
243	SEG8	-3216.3	507.3
244	SEG7	-3290.9	507.3
245	SEG6	-3347.9	507.3
246	SEG5	-3404.9	507.3
247	SEG4	-3461.9	507.3
248	SEG3	-3518.9	507.3
249	SEG2	-3575.9	507.3
250	SEG1	-3632.9	507.3
251	SEG0	-3689.9	507.3
252	COMS_A0	-3764	507.3
253	COMS_A1	-3821	507.3
254	COM0	-3878	507.3
255	COM1	-3935	507.3
256	COM2	-3992	507.3
257	COM3	-4049	507.3
258	COM4	-4106	507.3

9. Electrical Characteristic

9-1 Absolute Maximum Ratings

Table 9-1

Parameter	Symbol	Rating	Unit
Supply Voltage Range	V_{DD}	-0.3 to 6.5	V
Input Voltage Range	V_{IN}	-0.3 to V_{DD}+0.3	V
External VLCD Voltage Range	V_{LCD}	-0.3 to 8.0	V
Operation Temperature Range	T_{OPR}	-20 to 80	℃
Storage Temperature Range	T_{ST}	-45 to 125	℃

9-2 DC Characteristic

Table 9-2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.6	3.3	3.6	V	
VLCD Voltage	V_{LCD}	--	5~7	7.8	V	
Input High Voltage	V_{IH}	0.8×V_{DD}	--	V_{DD}	V	
Input Low Voltage	V_{IL}	Gnd	--	0.2×V_{DD}	V	
Output High Voltage	V_{OH}	0.8×V_{DD}	--	V_{DD}	V	
Output Low Voltage	V_{OL}	Gnd	--	0.2×V_{DD}	V	
Input Leakage Current	I_{IL}	-1	--	+1	μA	V_{IN} = V_{DD} to V_{SS}
Output Leakage Current	I_{OL}	-3	--	+2	μA	V_{IN} = V_{DD} to V_{SS}
Oscillator Frequency	F_{CL}	--	54	--	KHz	V_{DD}=3.3V
		--	45	--		V_{DD}=3.0V
		--	36	--		V_{DD}=2.6V
Standby Mode Current (Normal Mode Current)	I_{SB}	--	70	--	μA	**No MPU I/F Access** V_{DD}=3.3V, F_{CL} = 45KHz Segment=128, Common=32 FRM = 60Hz T_A=25℃
Display Off Current	$I_{DISPLAY}$	--	25	--	μA	The same as above
Sleep Mode Current	I_{SLEEP}	--	0.2	0.5	μA	The same as above

V_{DD} = 2.6 to 3.6V, Gnd = 0V, Ta = -20 to 80℃

9-3 Timing Characteristic

9-3-1 Parallel Interface

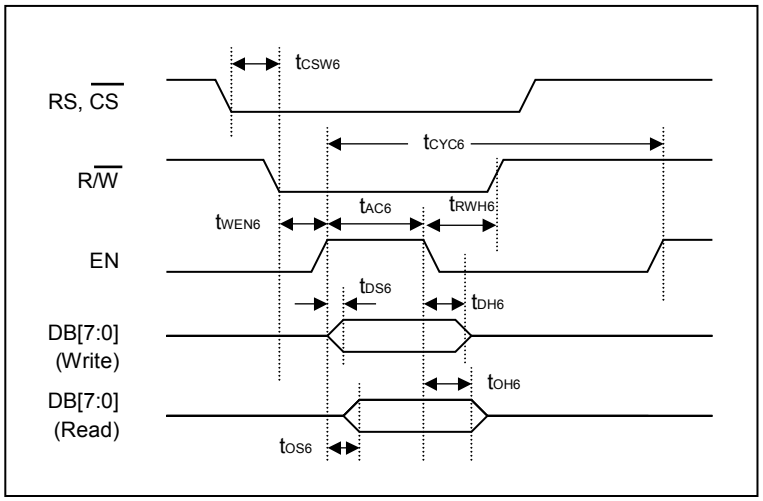


Figure 9-1：6800 MPU Timing

6800 MPU Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address Setup Time	RS, $\overline{CS}$	t_{CSW6}		0	--	ns
Read/Write Setup Time	R/$\overline{W}$	t_{WEN6}		10	--	
Read/Write Hold Time		t_{RWH6}		10	--	
Enable Access Time	EN	t_{AC6}		90	--	
Access Cycle Time		t_{CYC6}	Command Cycle	200	--	
			Data Cycle	400	--	
Write Data Setup Time	DB[7:0]	t_{DS6}		0	--	
Write Data Hold Time		t_{DH6}		10	--	
Read Data Access Time		t_{OS6}		30	50	
Read Data Hold Time		t_{OH6}		10	--	

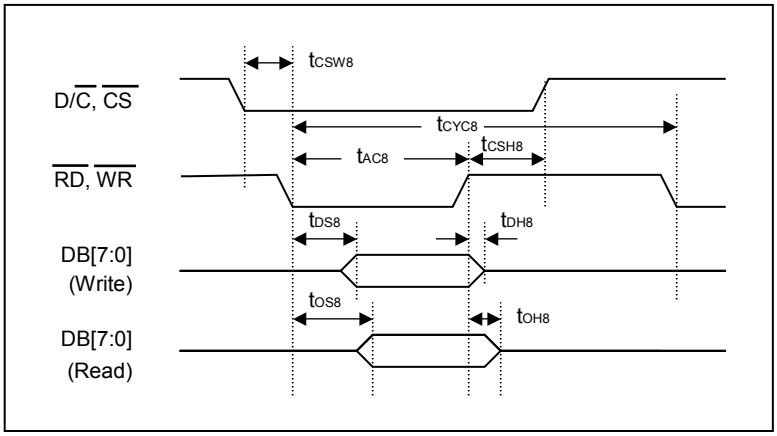


Figure 9-2：8080 MPU Timing

8080 MPU Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Address Setup Time	RS, $\overline{CS}$	T_{CSW8}		10	--	ns
Address Hold Time		T_{CSH8}		10	--	
Read/Write Access Time	$\overline{RD}$, $\overline{WR}$	t_{AC8}		90	--	
Access Cycle Time		T_{CYC8}	Command Cycle	200	--	
			Data Cycle	400	--	
Write Data Setup Time	DB[7:0]	t_{DS6}		0	--	
Write Data Hold Time		t_{DH6}		10	--	
Read Data Setup Time		t_{OS6}		30	50	
Read Data Setup Time		t_{OH6}		10	--	

9-3-2 Serial Interface

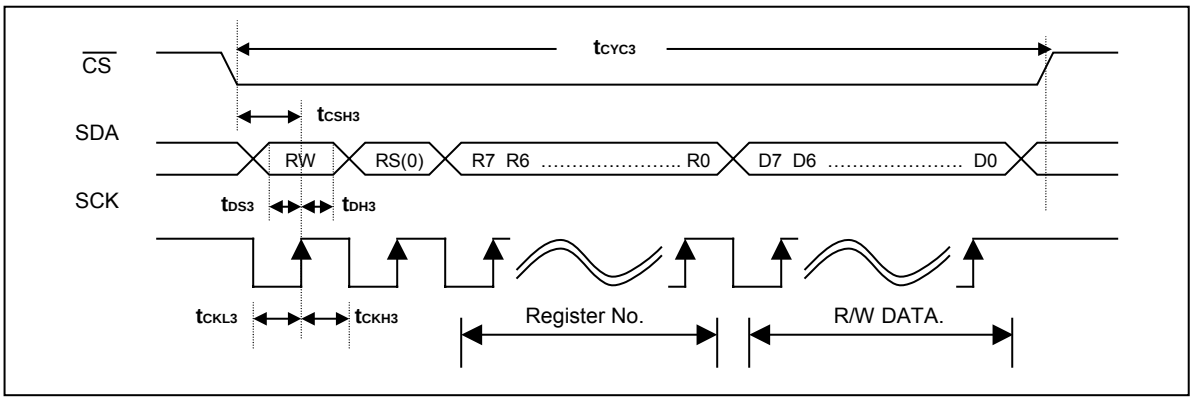


Figure 9-3：3-Wire Timing

3-Wire Serial Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Access Time	$\overline{CS}$	t_{CYC3}		3.6	--	ms
$\overline{CS}$ Setup Time		t_{CSH3}		20	--	ns
Clock Low Pulse Width	SCK	t_{CKL3}		100	--	
Clock High Pulse Width		t_{CKH3}		100	--	
Data Setup Time	SDA	t_{DS3}		20	--	
Data Hold Time		t_{DH3}		10	--	

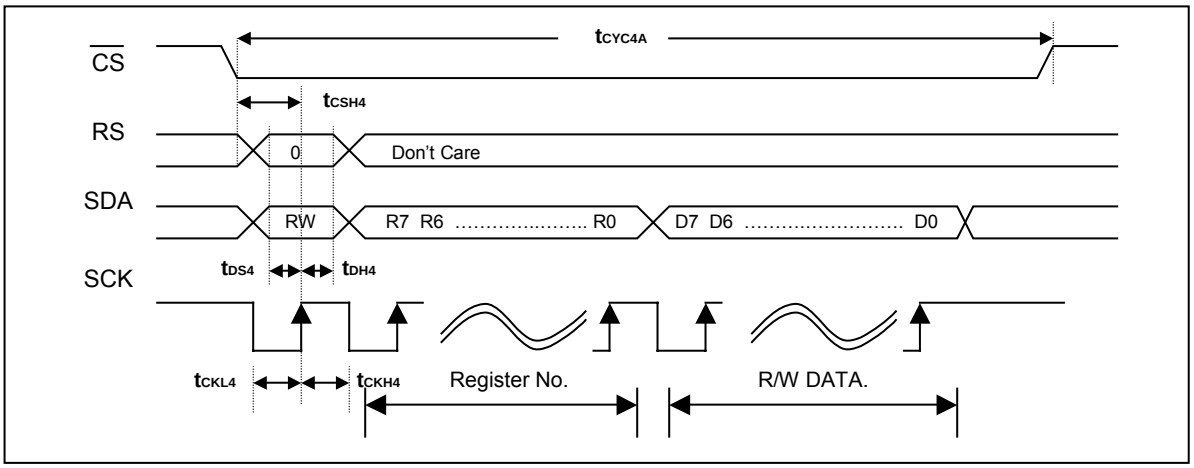


Figure 9-4：4-Wire(A-Type) Timing

4-Wire(A-Type) Serial Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Access Time	$\overline{CS}$	t_{CYC4A}		3.4	--	ms
$\overline{CS}$ Setup Time		t_{CSH4}		20	--	ns
Clock Low Pulse Width	SCK	t_{CKL4}		100	--	
Clock High Pulse Width		t_{CKH4}		100	--	
Data Setup Time	SDA, RS	t_{DS4}		20	--	
Data Hold Time		t_{DH4}		10	--	

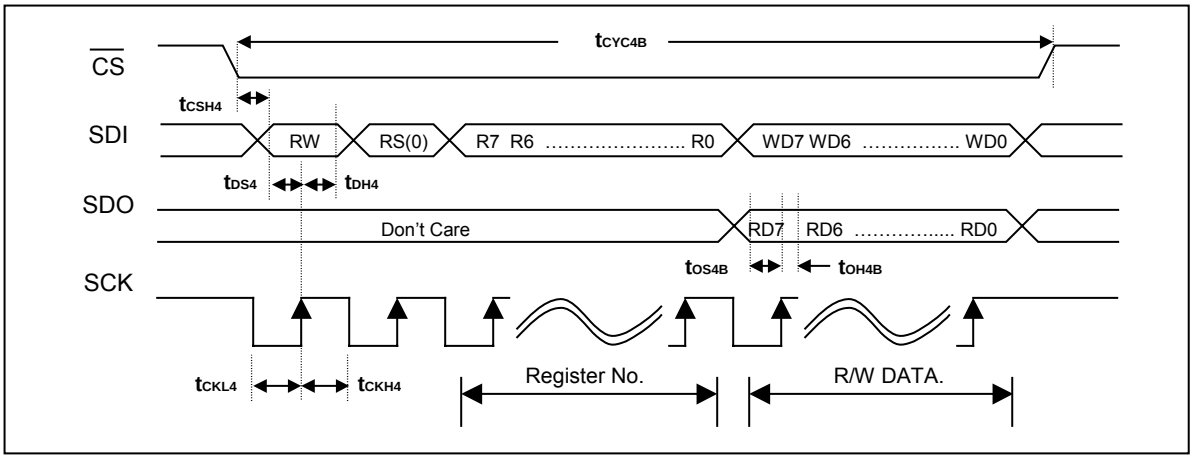


Figure 9-5：4-Wire(B Type) Timing

4-Wire(B-Type) Serial Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Access Time	$\overline{CS}$	t_{CYC4A}		3.6	--	ms
$\overline{CS}$ Setup Time		t_{CSH4}		20	--	ns
Clock Low Pulse Width	SCK	t_{CKL4}		100	--	
Clock High Pulse Width		t_{CKH4}		100	--	
Data Write Setup Time	SDI	t_{DS4}		20	--	
Data Write Hold Time		t_{DH4}		10	--	
Data Read Setup Time	SDO	t_{OS4B}		20	--	
Data Read Hold Time		t_{OH4B}		10	--	

9-3-3 Reset Interface

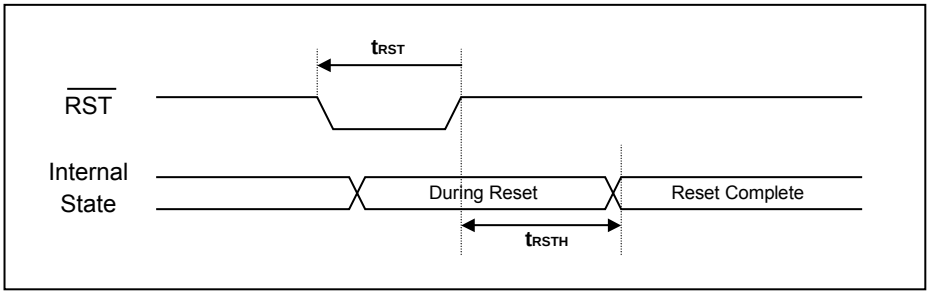


Figure 9-6: Reset Timing

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset Pulse Width	$\overline{RST}$	t_{RST}		100	--	ns
Reset Complete Hold Time	$\overline{RST}$	t_{RSTH}	F_{CL}= 55KHz	150	250	ms

Appendix A.

A-1 COG Application

A-1-1 Basic Connection of Serial I/F

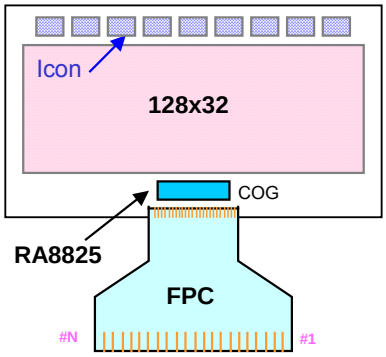


Figure A：COG Module

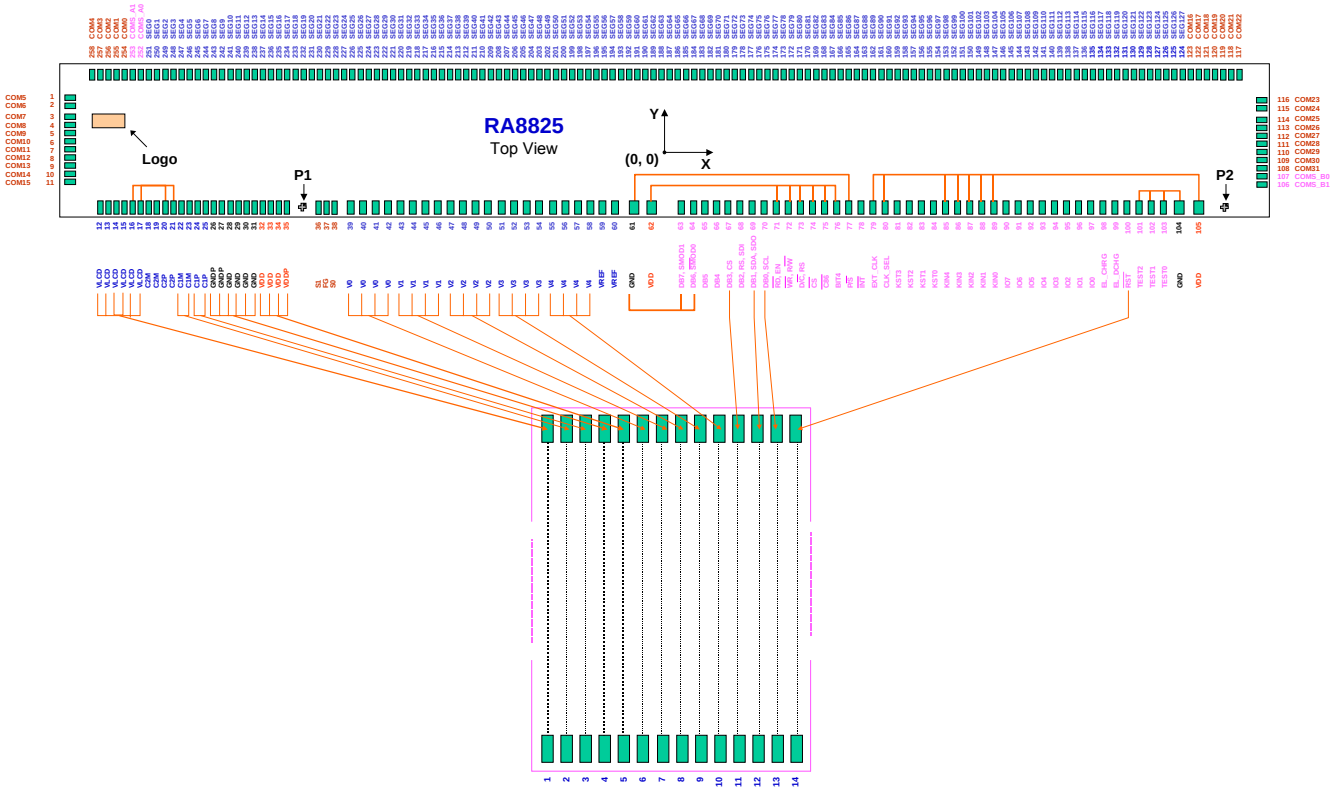


Figure A-2：Basic Connection of Serial I/F

The RA8825 provide many interfaces for MPU that including parallel, 3-Wire serial and 4-Wire serial, and some useful I/O interface like I/O and Key-scan. Therefore there are many options for user to connect the COG die to FPC. The Figure A-2 is the basic connection of serial mode in COG module. If the MPU interface is serial mode, then these signals are necessary for FPC. Note the unused parallel interface have to connect VDD.

A-1-2 Basic Connection of Parallel I/F

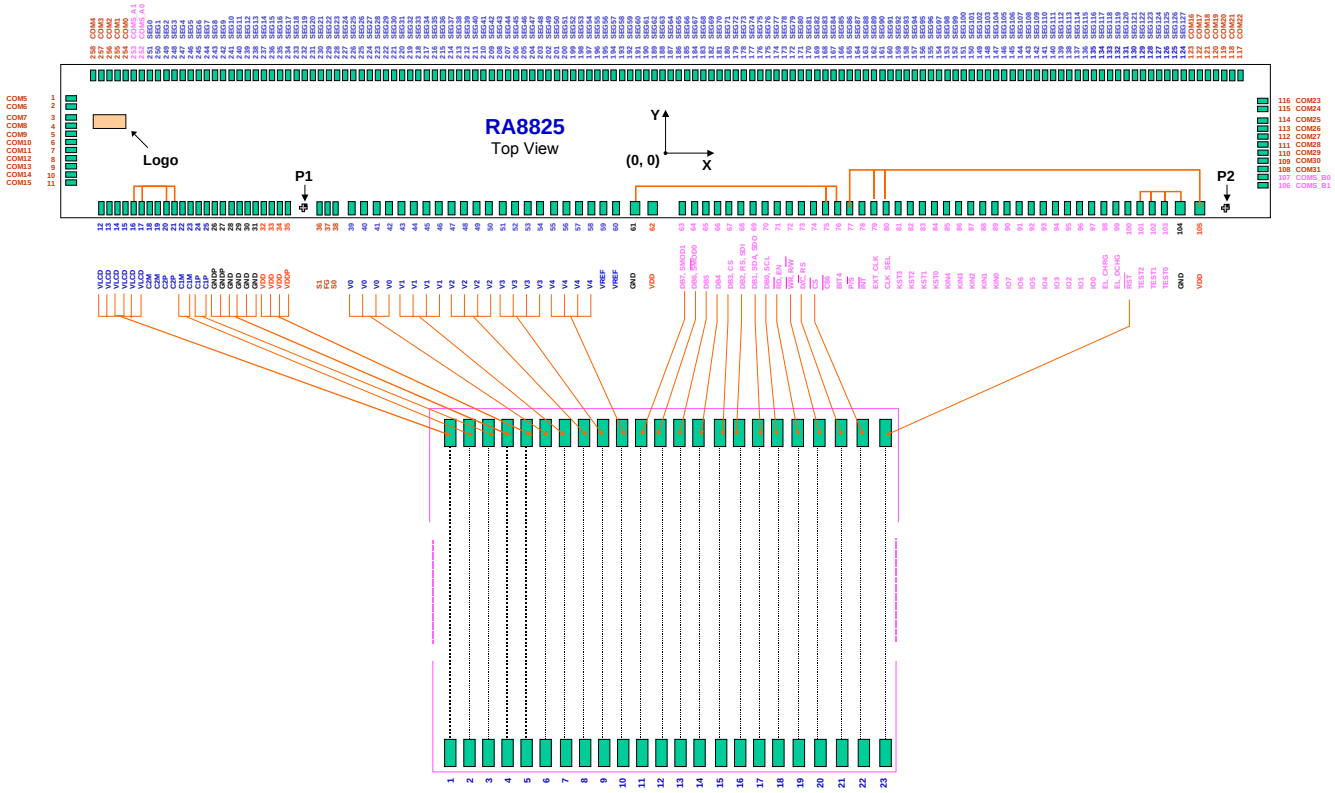


Figure A-3：Basic Connection of Parallel I/F

The figure A-3 is the basic connection of parallel mode in COG module. If the MPU interface is parallel mode, then these signals are necessary for FPC.

A-1-3 FPC Connection for Other Functions

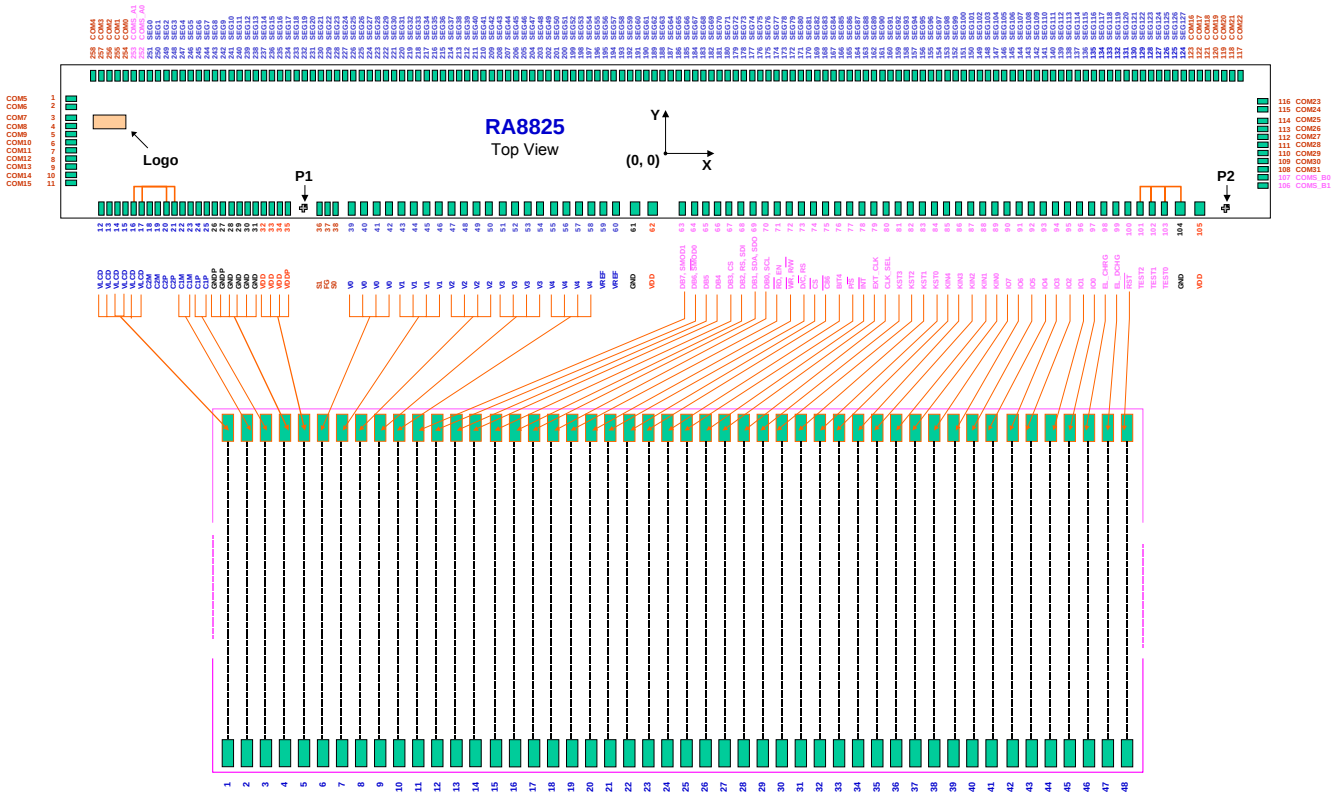


Figure A-4：Example(A) of FPC Connection

As previous mention, the RA8825 provides many interfaces for MPU that including parallel, 3-Wire serial and 4-Wire serial, and some useful I/O interface like I/O and Key-scan. The Figure A-4 is an example for RA8825 COG die that connect all of the signals to FPC.

The RA8825 also provides two common outputs for Icon that let the panel layout easier to meet their application.

The Figure A-5 is another example that uses 3-wire MPU interface, 2-times VDD, internal RC Oscillator, EL driver, 3x4 Key-scan, 2 I/O signal. In this case, the FPC only uses 23pins. Some configure pin are connect to VDD or GND through ITO resistance, such as P/$\overline{S}$, CLK_SEL and EXT_CLK. The unused parallel pins and KIN have to connect VDD.

The pad number 61, 62, 104, 105 are VDD or GND. Their purposes are used to pull-up or pull-down for some signals on panel. They do not need to connect to FPC.

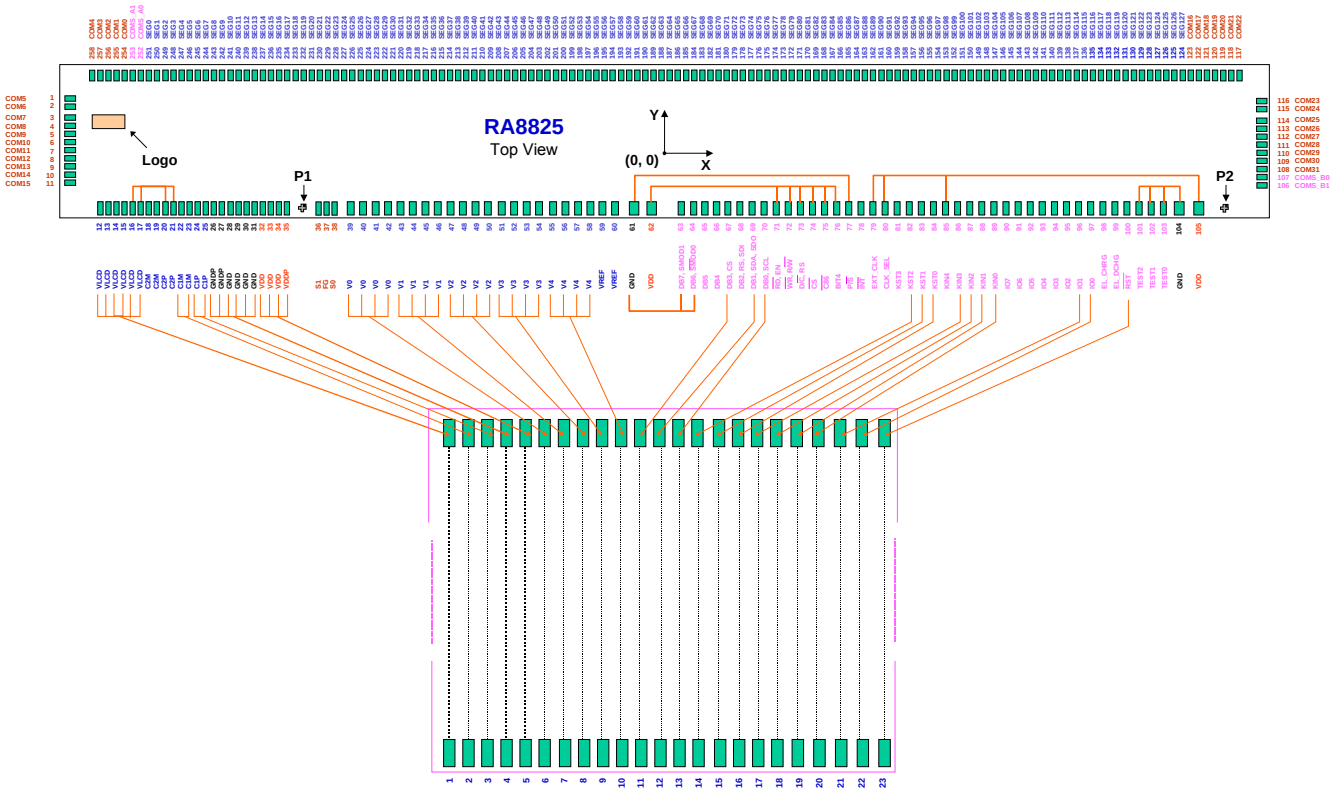


Figure A-5：Example(B) of COG Module

The Figure A-6 is an example for RA8825 to connect the driver signals(COM/SEG) to LCD panel. In this case, the panel size is 128x32. Please note the COG is reverse and stamp on the glass, so the point of COM0/SEG0 is on the right-bottom corner. Refer to Figure A-5.

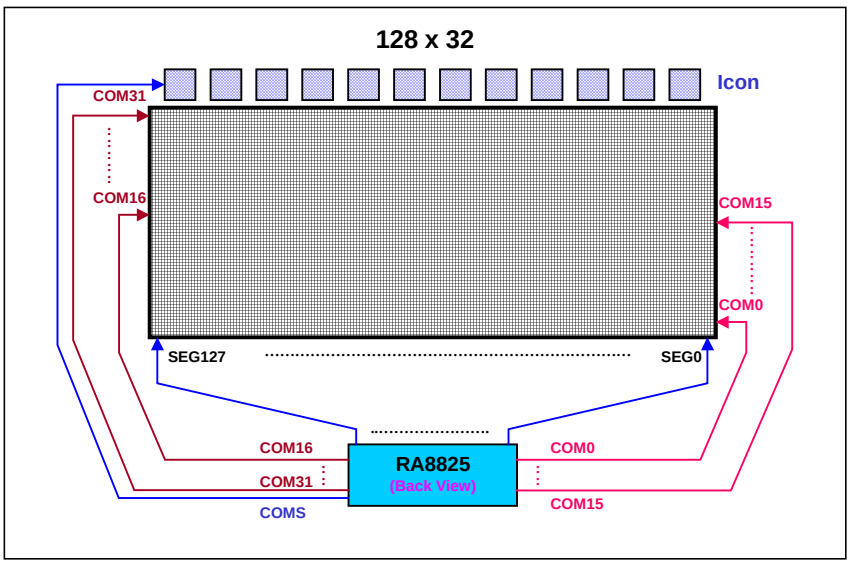


Figure A-6: The Connection of RA8825 with LCD Panel(128x32)

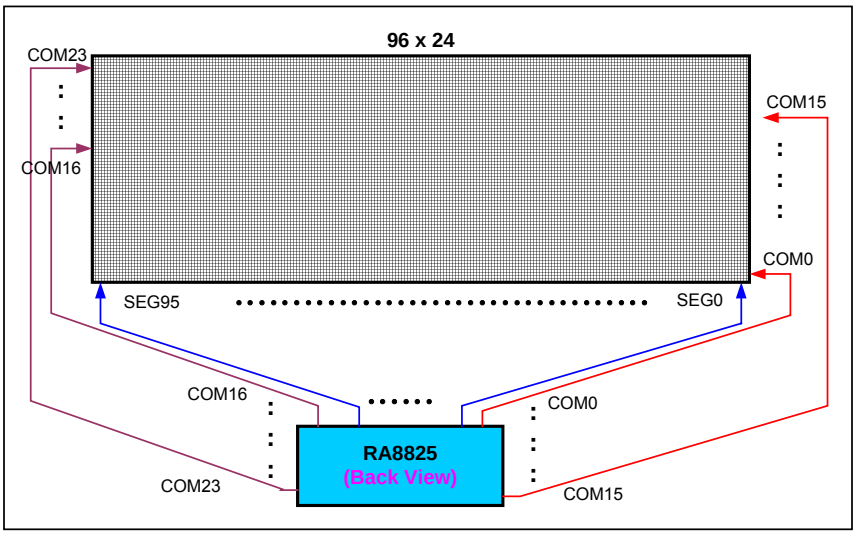


Figure A-7: The Connection of RA8825 with LCD Panel(96x24)

The Figure A-7 is an example of connection that use 96x24 panel. You can also separate the common signal for same number and each size is 13 common signals.

A-2 ITO

Table A-1: ITO Resistance of COG

PAD Name	ITO(Ohm)	PAD Name	ITO(Ohm)	PAD Name	ITO(Ohm)
VDD , VDDP	150	**C2P**	200	CLK_SEL	600
GND , GNDP	150	**C2M**	200	EXT_CLK	600
VREF	200	DB[7:0]	600	KST[3..0]	600
VLCD	200	$\overline{RD}$, EN	600	KIN[4..0]	600
V4	200	$\overline{WR}$, R/$\overline{W}$	600	IO[7:0]	600
V3	200	D/$\overline{C}$, RS	600	EL_CHRG	600
V2	200	$\overline{CS}$	600	EL_DCHG	600
V1	200	$\overline{INT}$	600	$\overline{RST}$	600
V0	200	$\overline{C86}$	600	TEST[2..0]	600
C1P	200	BIT4	600		
C1M	200	P/$\overline{S}$	600		

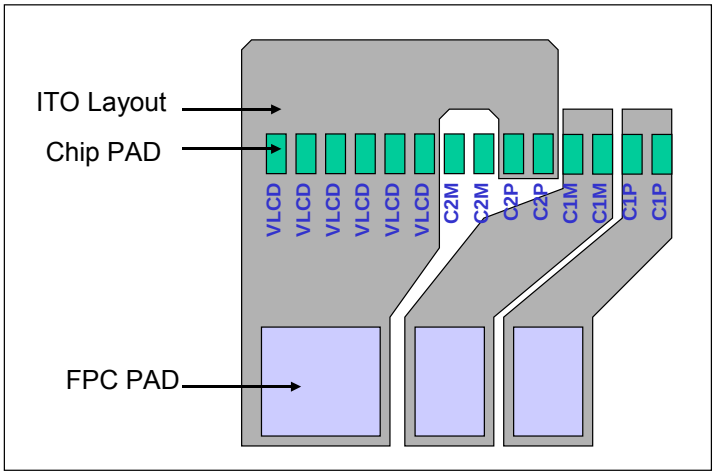


Figure A-8：ITO Layout Example - VLCD(2*VDD)

The RA8825 power signals (such as VDD, GND, VLCD, V[4:0], C1P, C1M) have to keep the smaller ITO resistance for panel layout. So the wires of layout need to keep as thick as possible to reduce the ITO resistance. The Figure A-8 is an example for VLCD layout of panel. Because the RA8825 provide six pads for VLCD, therefore the layout engineer has to connect all of these pads to FPC. In this case, the VLCD is two times of VDD, so the C2P have to connect to VLCD and do not forget keep the wire thicker.

The Figure A-9 is a layout example of RA8825 to FPC on COG module. The VDD and GND of RA8825 should as close as possible to FPC. The RA8825 provide six GND pad, user have to connect these six pad to FPC with a thick wire. For the design of FPC, the related power signals(VDD, GND, VLCD) of layout need to keep as thick as possible to reduce the wire resistance. And the VDD, GND pad of FPC keep double width than other signals.

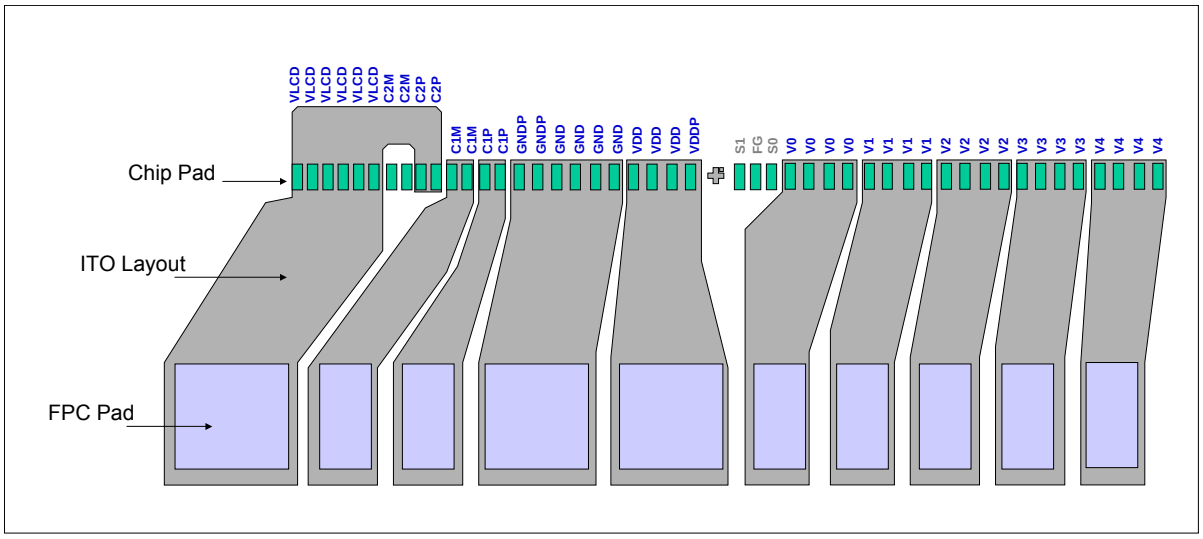


Figure A-9：ITO Layout Example