RAiO

RA8917

8-Bit Micro-Controller

Version 1.6

November 9, 2004
## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9</td>
<td>2003/5/13</td>
<td>Preliminary Specification Version</td>
</tr>
<tr>
<td>0.92</td>
<td>2003/7/15</td>
<td>Secondary Preliminary Specification Version</td>
</tr>
<tr>
<td>1.0</td>
<td>2003/10/28</td>
<td>First Release</td>
</tr>
<tr>
<td>1.1</td>
<td>2003/10/28</td>
<td>Update 8.3 section for Memory space, Erase/Program entry point(address).</td>
</tr>
<tr>
<td>1.2</td>
<td>2004/3/3</td>
<td>Update Figure 8-1.</td>
</tr>
<tr>
<td>1.3</td>
<td>2004/3/22</td>
<td>Update Chapter 4.1, 4.2.</td>
</tr>
<tr>
<td>1.4</td>
<td>2004/3/30</td>
<td>Update Appendix, Supported Flash Type</td>
</tr>
<tr>
<td>1.5</td>
<td>2004/5/10</td>
<td>Add Appendix A</td>
</tr>
<tr>
<td>1.6</td>
<td>2004/11/9</td>
<td>Pin Description of AIN[3:0]. Modify Operating Voltage.</td>
</tr>
</tbody>
</table>
# RA8917

## 8-Bit Micro-Controller

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Table of Contents</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>General Description</td>
<td>5</td>
</tr>
<tr>
<td>2.</td>
<td>Feature</td>
<td>5</td>
</tr>
<tr>
<td>3.</td>
<td>Block Diagram</td>
<td>6</td>
</tr>
<tr>
<td>4.</td>
<td>Die Form</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>4.1 PAD Diagram</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>4.2 Pin Assignment(PQFP-128Pin)</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>4.3 PAD X/Y Coordinate</td>
<td>8</td>
</tr>
<tr>
<td>5.</td>
<td>Pin Description</td>
<td>10</td>
</tr>
<tr>
<td>6.</td>
<td>Memory Organization</td>
<td>14</td>
</tr>
<tr>
<td>7.</td>
<td>Registers Description</td>
<td>15</td>
</tr>
<tr>
<td>8.</td>
<td>Function Description</td>
<td>48</td>
</tr>
<tr>
<td></td>
<td>8.1 System Clock</td>
<td>48</td>
</tr>
<tr>
<td></td>
<td>8.2 CPU Operation Mode</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td>8.2.1 Reset &amp; Idle &amp; Sleep &amp; Power Saving Mode</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td>8.2.2 Wakeup</td>
<td>52</td>
</tr>
<tr>
<td></td>
<td>8.3 External Flash ROM</td>
<td>52</td>
</tr>
<tr>
<td></td>
<td>8.3.1 Command Definitions</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td>8.3.2 Flash Sector Erase</td>
<td>56</td>
</tr>
<tr>
<td></td>
<td>8.3.3 Flash Programming</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td>8.4 I/O Ports</td>
<td>62</td>
</tr>
<tr>
<td></td>
<td>8.5 Timer</td>
<td>68</td>
</tr>
<tr>
<td></td>
<td>8.6 Watch Dog</td>
<td>72</td>
</tr>
<tr>
<td></td>
<td>8.7 Interrupt</td>
<td>74</td>
</tr>
<tr>
<td></td>
<td>8.8 Universal Synchronous Asynchronous Receiver Transmitter (UART)</td>
<td>81</td>
</tr>
<tr>
<td></td>
<td>8.9 IrDA Interface</td>
<td>84</td>
</tr>
<tr>
<td></td>
<td>8.10 Digital-to-Analog Converter (D/A) Module</td>
<td>84</td>
</tr>
<tr>
<td></td>
<td>8.11 LCD Interface</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td>8.12 PWM</td>
<td>88</td>
</tr>
<tr>
<td></td>
<td>8.13 Low Voltage Detect (LVD)</td>
<td>92</td>
</tr>
<tr>
<td></td>
<td>8.14 External SRAM</td>
<td>94</td>
</tr>
<tr>
<td></td>
<td>8.15 Analog-to-Digital Converter (ADC) Module</td>
<td>95</td>
</tr>
<tr>
<td></td>
<td>8.15.1 ADC Touch Panel Loop Control</td>
<td>97</td>
</tr>
<tr>
<td></td>
<td>8.15.2 ADC Touch Panel No Loop Control</td>
<td>98</td>
</tr>
<tr>
<td></td>
<td>8.16 1Hz, 2Hz and 1/60Hz Interrupt/Wakeup</td>
<td>99</td>
</tr>
<tr>
<td></td>
<td>8.17 Multiplier and Accumulator(MAC)</td>
<td>99</td>
</tr>
<tr>
<td></td>
<td>8.18 Extended Data Out (EDO) RAM Interface</td>
<td>103</td>
</tr>
<tr>
<td></td>
<td>8.18.1 Continue Read Cycle</td>
<td>104</td>
</tr>
<tr>
<td></td>
<td>8.18.2 Continue Write Cycle</td>
<td>104</td>
</tr>
</tbody>
</table>
8.18.3 Read/Write Interleave ........................................................................................................... 107
8.19 Analog Switch ......................................................................................................................... 107

9. Electrical Characteristic ....................................................................................................... 109
   9.1 DC Electrical Characteristics .......................................................................................... 109

10. Application .......................................................................................................................... 110

Appendix A. Package Dimension ............................................................................................... 111
Appendix B. Supports Flash ......................................................................................................... 112
1. General Description

RA8917 is an 8-bit downloadable micro-controller. Up to 22MHz system clock makes it a perfect choice for high-end device. It contains a 16x16 Multiplier and Accumulator (MAC), which not only greatly reduce programmer’s effort, but also shorten development time. RA8917 is embedded 4-channel 12-Bit ADC that can vary your application fields in analog detection, such as temperature, pressure, humidity, etc. Moreover, matched with LCM (LCD Module), 12-bit ADC can be perfectly used in Touch Panel function.

RA8917 is suitable for any downloadable device no matter used by end-users for voice/data download, or used by programmers for S/W program updated. The built-in 8K-byte ROM supports the on-chip RAiO ICE Monitor Program, ISP(In-System Programming) and ISD(In-System Debugging), which controls the UART and enables the RS232 connection between the RA8917 and a PC host. Besides that, IrDA application is also allowed to give the device multiple attractive characteristics.

In short, RA8917 supports embedded 4K-byte SRAM, three I/O ports, LCD interface, built in PLL / RC Oscillator, LVD, multiple timer/counter sources, versatile interrupt-handling architecture, built-in one DAC (Digital-to-Analog Converters), 16x16 Multiplier and Accumulator (MAC), 4-channel 12-Bit ADC and support three EDO DRAM (Extended Data Out) interface configuration: one 4Mx4bit chip, two 4Mx4 chips and one 8Mx8 chip.

2. Feature

- 8-bit Micro Processor for Maximum 22MHz
- Support 3 types EDO DRAM Interface configuration
  1. External one 4Mx4bit chip
  2. External two 4Mx4bit chips
  3. External one 8Mx8bit chip
- Internal 4K-Byte SRAM
- Support External ROM/RAM/Flash Interface
- Flexible External Flash Support, Up to 128MBYTE
- Flexible I/O Interrupt & Wake-Up Mode
- Support Wake-Up Reset Mode
- Support LVD(Low Voltage Detector)
- Support LCD Interface
- Support PWM Output with 50% or 100% Duty Select
- Four 8-Bits Programmable I/O Port
- Three 12-Bits Timer
- Six Time-Base Options
- Watch Dog Timer
- One 3-Level 10-bits Fixed Current Mode DAC
- Support 4-channel 12-bit ADC with Touch Panel Function
- One User’s UART with Baud Rate Generator, Up to 115200bps
- UART Provide Normal, IrDA/ASK IR Mode
- Support UART Wakeup
- Support Idle/Sleep/Power Saving Mode
- Support Timer Wake-Up Mode
- Support H/W 16x16 Multiplier with Adder Option
- 1Hz, 2Hz and 1/60Hz Interrupt/Wake up
- Support Interrupt Vector & Priority
- Built in two Independent Oscillator; Low Speed (32768Hz) and High Speed (From 1.84MHz to 22.1MHz)
- Low Power Consumption
- Operating Voltage: 2.4V ~ 3.6V
- Package: Die Form or PQFP-128Pin
3. Block Diagram

Figure 3.1
4. Die Form

4.1 PAD Diagram

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pad Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>94</td>
</tr>
<tr>
<td>IOUT</td>
<td>95</td>
</tr>
<tr>
<td>AVDD</td>
<td>96</td>
</tr>
<tr>
<td>VEXT</td>
<td>97</td>
</tr>
<tr>
<td>SW3</td>
<td>98</td>
</tr>
<tr>
<td>SW2</td>
<td>99</td>
</tr>
<tr>
<td>SW1</td>
<td>100</td>
</tr>
<tr>
<td>COM</td>
<td>101</td>
</tr>
<tr>
<td>PT1.0</td>
<td>102</td>
</tr>
<tr>
<td>PT1.1</td>
<td>103</td>
</tr>
<tr>
<td>BK7</td>
<td>104</td>
</tr>
<tr>
<td>BK6</td>
<td>105</td>
</tr>
<tr>
<td>BK5</td>
<td>106</td>
</tr>
<tr>
<td>BK4</td>
<td>107</td>
</tr>
<tr>
<td>BK3</td>
<td>108</td>
</tr>
<tr>
<td>BK2</td>
<td>109</td>
</tr>
<tr>
<td>BK1</td>
<td>110</td>
</tr>
<tr>
<td>BK0</td>
<td>111</td>
</tr>
<tr>
<td>ROM_OE#</td>
<td>112</td>
</tr>
<tr>
<td>ROM_CE#</td>
<td>113</td>
</tr>
<tr>
<td>VDD</td>
<td>114</td>
</tr>
<tr>
<td>VDDP</td>
<td>115</td>
</tr>
</tbody>
</table>

4.2 Pin Assignment(PQFP-128Pin)

Die Size: 3730 x 2850 (um²)
### 4.3 PAD X/Y Coordinate

<table>
<thead>
<tr>
<th>Pad Order</th>
<th>Pin Name</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GNDP</td>
<td>-1651.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>-1546.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>3</td>
<td>BK10</td>
<td>-1446.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>4</td>
<td>BK11</td>
<td>-1346.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>5</td>
<td>FL_OE#</td>
<td>-1246.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>6</td>
<td>FL_WE#</td>
<td>-1146.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>7</td>
<td>FL_CE#</td>
<td>-1046.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>8</td>
<td>PT3_4</td>
<td>-946.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>9</td>
<td>PT3_5</td>
<td>-846.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>10</td>
<td>PT3_6</td>
<td>-746.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>11</td>
<td>PT3_7</td>
<td>-646.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>12</td>
<td>PT4_4</td>
<td>-546.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>13</td>
<td>PT4_5</td>
<td>-446.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>14</td>
<td>PT4_6</td>
<td>-346.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>15</td>
<td>PT4_7</td>
<td>-246.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>16</td>
<td>D7</td>
<td>-146.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>17</td>
<td>D6</td>
<td>-46.65</td>
<td>-1330.4</td>
</tr>
<tr>
<td>18</td>
<td>D5</td>
<td>53.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>19</td>
<td>D4</td>
<td>153.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>20</td>
<td>D3</td>
<td>253.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>21</td>
<td>D2</td>
<td>353.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>22</td>
<td>D1</td>
<td>453.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>23</td>
<td>D0</td>
<td>553.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>24</td>
<td>GNDP</td>
<td>653.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>25</td>
<td>A0</td>
<td>753.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>26</td>
<td>A1</td>
<td>853.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>27</td>
<td>A2</td>
<td>953.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>28</td>
<td>A3</td>
<td>1053.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>29</td>
<td>A4</td>
<td>1153.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>30</td>
<td>A5</td>
<td>1253.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>31</td>
<td>A6</td>
<td>1353.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>32</td>
<td>A7</td>
<td>1453.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>33</td>
<td>A8</td>
<td>1553.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>34</td>
<td>GND</td>
<td>1653.35</td>
<td>-1330.4</td>
</tr>
<tr>
<td>35</td>
<td>A9</td>
<td>1769.7</td>
<td>-1214.05</td>
</tr>
<tr>
<td>36</td>
<td>A10</td>
<td>1769.7</td>
<td>-1114.05</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pad Order</th>
<th>Pin Name</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>37</td>
<td>A11</td>
<td>1769.7</td>
<td>-1014.05</td>
</tr>
<tr>
<td>38</td>
<td>A12</td>
<td>1769.7</td>
<td>-914.05</td>
</tr>
<tr>
<td>39</td>
<td>A13</td>
<td>1769.7</td>
<td>-814.05</td>
</tr>
<tr>
<td>40</td>
<td>VDD</td>
<td>1769.7</td>
<td>-585.85</td>
</tr>
<tr>
<td>41</td>
<td>PT3_0</td>
<td>1769.7</td>
<td>-485.85</td>
</tr>
<tr>
<td>42</td>
<td>PT3_1</td>
<td>1769.7</td>
<td>-385.85</td>
</tr>
<tr>
<td>43</td>
<td>PT3_2</td>
<td>1769.7</td>
<td>-285.85</td>
</tr>
<tr>
<td>44</td>
<td>PT3_3</td>
<td>1769.7</td>
<td>-185.85</td>
</tr>
<tr>
<td>45</td>
<td>PT2_0</td>
<td>1769.7</td>
<td>-85.85</td>
</tr>
<tr>
<td>46</td>
<td>PT2_1</td>
<td>1769.7</td>
<td>14.15</td>
</tr>
<tr>
<td>47</td>
<td>PT2_2</td>
<td>1769.7</td>
<td>114.15</td>
</tr>
<tr>
<td>48</td>
<td>PT2_3</td>
<td>1769.7</td>
<td>214.15</td>
</tr>
<tr>
<td>49</td>
<td>PT2_4</td>
<td>1769.7</td>
<td>314.15</td>
</tr>
<tr>
<td>50</td>
<td>PT2_5</td>
<td>1769.7</td>
<td>414.15</td>
</tr>
<tr>
<td>51</td>
<td>VDDP</td>
<td>1769.7</td>
<td>514.15</td>
</tr>
<tr>
<td>52</td>
<td>PT2_6</td>
<td>1769.7</td>
<td>614.15</td>
</tr>
<tr>
<td>53</td>
<td>PT2_6B</td>
<td>1769.7</td>
<td>714.15</td>
</tr>
<tr>
<td>54</td>
<td>PT2_7</td>
<td>1769.7</td>
<td>814.15</td>
</tr>
<tr>
<td>55</td>
<td>PT2_7B</td>
<td>1769.7</td>
<td>914.15</td>
</tr>
<tr>
<td>56</td>
<td>GNDP</td>
<td>1769.7</td>
<td>1014.15</td>
</tr>
<tr>
<td>57</td>
<td>VDDP</td>
<td>1769.7</td>
<td>1114.15</td>
</tr>
<tr>
<td>58</td>
<td>GNDP</td>
<td>1769.7</td>
<td>1215.55</td>
</tr>
<tr>
<td>59</td>
<td>OSC1_XA</td>
<td>1680.23</td>
<td>1330.5</td>
</tr>
<tr>
<td>60</td>
<td>OSC1_XB</td>
<td>1580.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>61</td>
<td>OSC2_XA</td>
<td>1480.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>62</td>
<td>OSC2_XB</td>
<td>1380.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>63</td>
<td>RESET#</td>
<td>1280.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>64</td>
<td>MONITOR#</td>
<td>1180.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>65</td>
<td>BREAK#</td>
<td>1080.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>66</td>
<td>CKS0</td>
<td>980.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>67</td>
<td>CKS1</td>
<td>880.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>68</td>
<td>CKS2</td>
<td>780.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>69</td>
<td>TYPE</td>
<td>680.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>70</td>
<td>TXD</td>
<td>580.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>71</td>
<td>RXD</td>
<td>480.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>72</td>
<td>PT4_3</td>
<td>380.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>Pad Order</td>
<td>Pin Name</td>
<td>X</td>
<td>Y</td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>73</td>
<td>PT4_2</td>
<td>280.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>74</td>
<td>PT4_1</td>
<td>180.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>75</td>
<td>PT4_0</td>
<td>80.22</td>
<td>1330.5</td>
</tr>
<tr>
<td>76</td>
<td>GNDP</td>
<td>-19.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>77</td>
<td>PT1_7</td>
<td>-119.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>78</td>
<td>PT1_6</td>
<td>-219.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>79</td>
<td>PT1_5</td>
<td>-319.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>80</td>
<td>PT1_4</td>
<td>-419.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>81</td>
<td>PT1_3</td>
<td>-519.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>82</td>
<td>PT1_2</td>
<td>-619.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>83</td>
<td>TEST2</td>
<td>-719.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>84</td>
<td>TEST1</td>
<td>-819.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>85</td>
<td>TEST0</td>
<td>-919.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>86</td>
<td>BK9</td>
<td>-1019.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>87</td>
<td>BK8</td>
<td>-1119.78</td>
<td>1330.5</td>
</tr>
<tr>
<td>88</td>
<td>AIN0</td>
<td>-1234.25</td>
<td>1330.5</td>
</tr>
<tr>
<td>89</td>
<td>AIN1</td>
<td>-1339.25</td>
<td>1330.5</td>
</tr>
<tr>
<td>90</td>
<td>AIN2</td>
<td>-1444.25</td>
<td>1330.5</td>
</tr>
<tr>
<td>91</td>
<td>AIN3</td>
<td>-1549.25</td>
<td>1330.5</td>
</tr>
<tr>
<td>92</td>
<td>AVDD</td>
<td>-1648.75</td>
<td>1330.5</td>
</tr>
<tr>
<td>93</td>
<td>AGND</td>
<td>-1748.75</td>
<td>1330.5</td>
</tr>
<tr>
<td>94</td>
<td>AGND</td>
<td>-1769.55</td>
<td>872.25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pad Order</th>
<th>Pin Name</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>95</td>
<td>IOUT</td>
<td>-1769.55</td>
<td>771.75</td>
</tr>
<tr>
<td>96</td>
<td>AVDD</td>
<td>-1769.55</td>
<td>672.25</td>
</tr>
<tr>
<td>97</td>
<td>VEXT</td>
<td>-1769.55</td>
<td>567.95</td>
</tr>
<tr>
<td>98</td>
<td>SW3</td>
<td>-1769.55</td>
<td>467.95</td>
</tr>
<tr>
<td>99</td>
<td>SW2</td>
<td>-1769.55</td>
<td>367.95</td>
</tr>
<tr>
<td>100</td>
<td>SW1</td>
<td>-1769.55</td>
<td>267.95</td>
</tr>
<tr>
<td>101</td>
<td>COM</td>
<td>-1769.55</td>
<td>167.95</td>
</tr>
<tr>
<td>102</td>
<td>PT1_1</td>
<td>-1769.55</td>
<td>67.95</td>
</tr>
<tr>
<td>103</td>
<td>PT1_0</td>
<td>-1769.55</td>
<td>-32.05</td>
</tr>
<tr>
<td>104</td>
<td>BK7</td>
<td>-1769.55</td>
<td>-132.05</td>
</tr>
<tr>
<td>105</td>
<td>BK6</td>
<td>-1769.55</td>
<td>-232.05</td>
</tr>
<tr>
<td>106</td>
<td>BK5</td>
<td>-1769.55</td>
<td>-332.05</td>
</tr>
<tr>
<td>107</td>
<td>BK4</td>
<td>-1769.55</td>
<td>-432.05</td>
</tr>
<tr>
<td>108</td>
<td>BK3</td>
<td>-1769.55</td>
<td>-532.05</td>
</tr>
<tr>
<td>109</td>
<td>BK2</td>
<td>-1769.55</td>
<td>-632.05</td>
</tr>
<tr>
<td>110</td>
<td>BK1</td>
<td>-1769.55</td>
<td>-732.05</td>
</tr>
<tr>
<td>111</td>
<td>BK0</td>
<td>-1769.55</td>
<td>-832.05</td>
</tr>
<tr>
<td>112</td>
<td>ROM_OE#</td>
<td>-1769.55</td>
<td>-932.05</td>
</tr>
<tr>
<td>113</td>
<td>ROM_CE#</td>
<td>-1769.55</td>
<td>-1032.05</td>
</tr>
<tr>
<td>114</td>
<td>VDD</td>
<td>-1769.55</td>
<td>-1132.05</td>
</tr>
<tr>
<td>115</td>
<td>VDDP</td>
<td>-1769.55</td>
<td>-1232.05</td>
</tr>
</tbody>
</table>
## 5. Pin Description

<table>
<thead>
<tr>
<th>Signal</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESET#</td>
<td>IN</td>
<td><strong>External Hardware Reset, active low.</strong> This pin is used to reset the system.</td>
</tr>
<tr>
<td>BREAK#</td>
<td>IN</td>
<td><strong>User Program Break, active low.</strong> This signal is used to break the user’s program from the ISD mode.</td>
</tr>
<tr>
<td>MONITOR#</td>
<td>IN</td>
<td><strong>Monitor Program Select, active low.</strong> This signal is used to select the system boot from monitor program (ROM) or user program (Flash). This signal has to pull low when the user wants to download the data from PC or enter the ISP/ISD mode. Note: Couldn’t be floating.</td>
</tr>
<tr>
<td>PT1_[7:0]</td>
<td>I/O</td>
<td><strong>Bit[7:0] of Port 1</strong> These are programmable pins for general-purpose I/O Port 1. The driving current and pull-high or pull-low can be selected by user register.</td>
</tr>
<tr>
<td>PT2_7</td>
<td>I/O</td>
<td><strong>Bit-7 of Port 2</strong> This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_7 is also as the output of PWM1. In PWM mode, the pin is always output and 72mA-driving current is selected.</td>
</tr>
<tr>
<td>PWM1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PT2_6</td>
<td>I/O</td>
<td><strong>Bit-6 of Port 2</strong> This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_6 is also as the output of PWM2. In PWM mode, the pin is always output and 72mA-driving current is selected.</td>
</tr>
<tr>
<td>PWM2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PT2_5</td>
<td>I/O</td>
<td><strong>Bit-5 of Port 2</strong> This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_5 is also as the write control of register $101E. If the write register $101F enabled, the pin is always output except the power saving mode.</td>
</tr>
<tr>
<td>EXP_WR#</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PT2_4</td>
<td>I/O</td>
<td><strong>Bit-4 of Port 2</strong> This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_4 is also as the secondary external flash chip select. If the secondary flash is enabled, the pin is always output except the power saving mode.</td>
</tr>
<tr>
<td>FL_CE2#</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PT2_3</td>
<td>I/O</td>
<td><strong>Bit-3 of Port 2</strong> This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_3 is also as the output of LVD. If the LVD enabled, the pin is always output except the power saving mode.</td>
</tr>
<tr>
<td>LVD_#</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PT2_2</td>
<td>I/O</td>
<td><strong>Bit-2 of Port 2</strong> This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register. The PT2_2 is also as the external memory write enable. If the external memory enabled, the pin is always output except the power saving mode. If REG[1032h] bit6 is set as 1, and then MEM_WE# and FL_WE# can be jointly used.</td>
</tr>
<tr>
<td>MEM_WE#</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
</tbody>
</table>
| PT2_1 | MEM_OE# | Bit-1 of Port 2  
This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.  
The PT2_1 is also as the external memory output enabling. If the external memory enabled, the pin is always output except the power saving mode. If REG[1032h] bit6 is set as 1, and then MEM_OE# and FL_OE# can be jointly used. |
| PT2_0 | MEM_CE# | Bit-0 of Port 2  
This is a programmable pin for general-purpose I/O Port 2. The driving current and pull-high or pull-low can be selected by user register.  
The PT2_0 is also as the external memory chip selecting. If the external memory enabled, the pin is always output except the power saving mode. |
| PT3_7 | EDO_OE# | Bit-7 of Port 3  
This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.  
The PT3_7 is also as the EDO RAM data output enable. |
| PT3_6 | EDO_WE# | Bit-6 of Port 3  
This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.  
The PT3_6 is also as the EDO RAM Read/Write input. |
| PT3_5 | CAS# | Bit-5 of Port 3  
This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.  
The PT3_5 is also as the EDO RAM Column Address Strobe. |
| PT3_4 | RAS# | Bit-4 of Port 3  
This is a programmable pin for general-purpose I/O Port 3. The driving current and pull-high or pull-low can be selected by user register.  
The PT3_4 is also as the EDO RAM Row Address Strobe. |
| PT3_3 | TX | Bit-3 of Port 3  
The PT3_3 is also as the transmission output of user’s UART. In UART mode, the pin is always output except the power saving mode. |
| PT3_2 | RX | Bit-2 of Port 3  
The PT3_2 is also as the receive input of user’s UART. In UART mode, the pin is always input. |
| PT3_1 | LCD_E | Bit-1 of Port 3  
The PT3_1 is also as the chip enable of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode. |
| PT3_0 | LCD_RW | Bit-0 of Port 3  
The PT3_0 is also as the read/write signal of external LCD controller. If the external LCD enabled, the pin is always output except the power saving mode. |
| PT4_[7:0] | OUT | Bit 7–0 of Port 4  
This is a programmable pin for general-purpose I/O Port 4. The driving current and pull-high or pull-low can be selected by user register.  
This pin is the current output of DAC. |
<table>
<thead>
<tr>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIN[3:0]</td>
<td>IN</td>
<td><strong>ADC Analog Input</strong>&lt;br&gt;These pins are the analog input of 12-bit ADC for 4-channel.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>ADC Mode</strong> &lt;br&gt;<strong>Touch Panel Mode</strong>&lt;br&gt;AIn0 X1&lt;br&gt;AIn1 Y1&lt;br&gt;AIn2 X2&lt;br&gt;AIn3 Y2</td>
</tr>
<tr>
<td>SW[3:1]</td>
<td>OUT</td>
<td><strong>Analog Switch [3~1]</strong>&lt;br&gt;Common input voltage of switch [3~1]</td>
</tr>
<tr>
<td>COM</td>
<td>IN</td>
<td><strong>14-bit Address Bus</strong>&lt;br&gt;These signal are used for external memory address bus.</td>
</tr>
<tr>
<td>A[13:0]</td>
<td>OUT</td>
<td><strong>8-bit Data Bus</strong>&lt;br&gt;These signal are used for external memory data bus.</td>
</tr>
<tr>
<td>D[7:0]</td>
<td>I/O</td>
<td><strong>Flash Chip Select, active low.</strong>&lt;br&gt;This signal is used for external flash.</td>
</tr>
<tr>
<td>FL_CE#</td>
<td>OUT</td>
<td><strong>Flash Write Enable, active low.</strong>&lt;br&gt;This signal is used for external flash. If REG[1032h] bit6 is set as 1, and then FL_WE# and MEM_WE can be jointly used.</td>
</tr>
<tr>
<td>FL_WE#</td>
<td>OUT</td>
<td><strong>Flash Output Enable, active low.</strong>&lt;br&gt;This signal is used for external flash. If REG[1032h] bit6 is set as 1, and then FL_OE# and MEM_OE# can be jointly used.</td>
</tr>
<tr>
<td>BK[11:0]</td>
<td>OUT</td>
<td><strong>Bank Bus.</strong>&lt;br&gt;Register FBANK[1030h], [105Ah] and Ext_SBANK [103Fh], [105Bh] jointly use Bank[11:0] Bus as the output of memory bank register. Normally, they are connected to the higher address of external Flash memory.</td>
</tr>
<tr>
<td>RXD</td>
<td>IN</td>
<td><strong>Receive Data</strong>&lt;br&gt;This is the received data input of system UART. Normally it's connected to the RS232's TX of PC.</td>
</tr>
<tr>
<td>TXD</td>
<td>OUT</td>
<td><strong>Transmit Data</strong>&lt;br&gt;This signal is the transmitted data output of system UART. Normally it's connected to the RS232’s RX of PC.</td>
</tr>
<tr>
<td>OSC1_XA</td>
<td>IN</td>
<td><strong>Oscillator1 Input.</strong>&lt;br&gt;This is the input signal of external X'tal(32768Hz).</td>
</tr>
<tr>
<td>OSC1_XB</td>
<td>OUT</td>
<td><strong>Oscillator1 Output.</strong>&lt;br&gt;This is the output signal of external X'tal(32768Hz).</td>
</tr>
<tr>
<td>OSC2_XA</td>
<td>IN</td>
<td><strong>Oscillator2 Input.</strong>&lt;br&gt;This is the input signal of external X'tal. (maximum up to 22.1184MHz)</td>
</tr>
<tr>
<td>OSC2_XB</td>
<td>OUT</td>
<td><strong>Oscillator2 Output.</strong>&lt;br&gt;This is the output signal of external X'tal. (maximum up to 22.1184MHz)</td>
</tr>
</tbody>
</table>
### CKS[2:0] IN

<table>
<thead>
<tr>
<th>CKS2</th>
<th>CKS1</th>
<th>CKS0</th>
<th>OSC2 Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1.8432MHz</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3.6864MHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>5.5296MHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>7.3728MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>11.0592MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>14.7456MHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>18.432MHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>22.1184MHz</td>
</tr>
</tbody>
</table>

Note: Couldn’t be floating.

### TYPE IN

**Clock Type Select for 32768Hz**
- 0: RC Oscillator
- 1: 32768 X’tal

Note: Couldn’t be floating.

### VEXT IN

**Low Voltage Detector Input**

### TEST[2:0]# IN

**Test Pins**
Test Pins are for RAIO’s internal testing purpose used in testing IC and ROM status. Normally, users will not use these pins. Therefore, please connect these three pins to VDD when making PCB board.

### Power Supply

- **VDD** PWR  | **Power Supply Voltage of Chip Core.**
- **VDDP** PWR | **Power Supply Voltage of Chip I/O.**
- **AVDD** PWR | **Analog Power Supply Voltage.**
- **GND** PWR  | **Ground of Chip Core.**
- **GNDP** PWR | **Ground of Chip I/O.**
- **AGND** PWR | **Analog Ground.**
## 6. Memory Organization

<table>
<thead>
<tr>
<th>C000~FFFF</th>
<th>Program Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFBA~FFBB</td>
<td>Timer Base INT Vector</td>
</tr>
<tr>
<td>FFBC~FFBD</td>
<td>ADC INT Vector</td>
</tr>
<tr>
<td>FFBE~FFBF</td>
<td>Low Speed Timer INT Vector</td>
</tr>
<tr>
<td>FFCC~FFC1</td>
<td>User UART INT Vector</td>
</tr>
<tr>
<td>FFCC~FFC3</td>
<td>Timer3 INT Vector</td>
</tr>
<tr>
<td>FFCC~FFC5</td>
<td>Port3 INT Vector</td>
</tr>
<tr>
<td>FFCE~FFC7</td>
<td>Timer2 INT Vector</td>
</tr>
<tr>
<td>FFCE~FFC9</td>
<td>Port2 INT Vector</td>
</tr>
<tr>
<td>FFCE~FFCB</td>
<td>Timer1 INT Vector</td>
</tr>
<tr>
<td>FFCE~FFCD</td>
<td>Port1 INT Vector</td>
</tr>
<tr>
<td>FFCE~FFCF</td>
<td>UART INT Vector</td>
</tr>
<tr>
<td>FFE0~FFE1</td>
<td>Low Speed Timer NMI Vector</td>
</tr>
<tr>
<td>FFE2~FFE3</td>
<td>Timer3 NMI Vector</td>
</tr>
<tr>
<td>FFE4~FFE5</td>
<td>Port3 NMI Vector</td>
</tr>
<tr>
<td>FFE6~FFE7</td>
<td>Timer2 NMI Vector</td>
</tr>
<tr>
<td>FFE8~FFE9</td>
<td>Port2 NMI Vector</td>
</tr>
<tr>
<td>FFEA~FFEB</td>
<td>Timer1 NMI Vector</td>
</tr>
<tr>
<td>FFEC~FFED</td>
<td>Port1 NMI Vector</td>
</tr>
<tr>
<td>FFEE~FFEF</td>
<td>Watch Dog Timer NMI Vector</td>
</tr>
<tr>
<td>FFFC~FFFD</td>
<td>NMI Vector</td>
</tr>
<tr>
<td>FFFC~FFFD</td>
<td>Reset Vector</td>
</tr>
<tr>
<td>FFFC~FFFD</td>
<td>IRQ_L, IRQ_H</td>
</tr>
</tbody>
</table>

*Note:* The User RAM is 4KByte mapped to address &0000h~0FFFh.
## 7. Registers Description

### Table 7-1

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000h</td>
<td>NMI MK(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>1001h</td>
<td>NMI MK(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>1002h</td>
<td>NMI ST(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>1003h</td>
<td>NMI ST(2)</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>REV</td>
</tr>
<tr>
<td>1004h</td>
<td>CLR NMI(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>1005h</td>
<td>CLR NMI(2)</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>REV</td>
</tr>
<tr>
<td>1006h</td>
<td>INT MK(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>1007h</td>
<td>INT MK(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>1008h</td>
<td>INT ST(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>1009h</td>
<td>INT ST(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>100Ah</td>
<td>CLR INT(1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>100Bh</td>
<td>CLR INT(2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>REV</td>
</tr>
<tr>
<td>100Ch</td>
<td>WDT_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>REV</td>
</tr>
<tr>
<td>100Dh</td>
<td>LCD_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>REV</td>
</tr>
<tr>
<td>100Eh</td>
<td>LCD(1)</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>100Fh</td>
<td>LCD(2)</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1010h</td>
<td>TM1_H</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>W/R</td>
</tr>
<tr>
<td>1011h</td>
<td>TM1_L</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1012h</td>
<td>TM1_CTL</td>
<td>ΓM1_EN</td>
<td>ΓM1_SLP_EN</td>
<td>ΓM1_WF_RST_EN</td>
<td>REV</td>
<td>ΓM1_LOOP</td>
<td>CKS2</td>
<td>CKS1</td>
<td>CKS0</td>
<td>W/R</td>
</tr>
<tr>
<td>1013h</td>
<td>TM2_H</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>W/R</td>
</tr>
<tr>
<td>1014h</td>
<td>TM2_L</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1015h</td>
<td>TM2_CTL</td>
<td>ΓM2_EN</td>
<td>ΓM2_SLP_EN</td>
<td>ΓM2_WF_RST_EN</td>
<td>REV</td>
<td>ΓM2_LOOP</td>
<td>CKS2</td>
<td>CKS1</td>
<td>CKS0</td>
<td>W/R</td>
</tr>
<tr>
<td>1016h</td>
<td>TM3_H</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>W/R</td>
</tr>
<tr>
<td>1017h</td>
<td>TM3_L</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1018h</td>
<td>TM3_CTL</td>
<td>ΓM3_EN</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>W/R</td>
</tr>
<tr>
<td>1019h</td>
<td>DAC_H</td>
<td>D9</td>
<td>D8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>W/R</td>
</tr>
<tr>
<td>101Ah</td>
<td>DAC_L</td>
<td>D1</td>
<td>D0</td>
<td>D9</td>
<td>D8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>W/R</td>
</tr>
<tr>
<td>101Bh</td>
<td>DAC_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>W/R</td>
</tr>
<tr>
<td>101Ch</td>
<td>PWM</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>101Dh</td>
<td>PWM_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>W/R</td>
</tr>
<tr>
<td>101Eh</td>
<td>EX IO</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>101Fh</td>
<td>EX_IO_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>W/R</td>
</tr>
<tr>
<td>1020h</td>
<td>PT1</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1021h</td>
<td>PT1_DIR</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1022h</td>
<td>PT1_INT</td>
<td>PT1_7</td>
<td>PT1_6</td>
<td>PT1_5</td>
<td>PT1_4</td>
<td>PT1_3</td>
<td>PT1_2</td>
<td>PT1_1</td>
<td>PT1_0</td>
<td>W/R</td>
</tr>
<tr>
<td>1023h</td>
<td>PT1_MOD</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1024h</td>
<td>PT2</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1025h</td>
<td>PT2_DIR</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W/R</td>
</tr>
<tr>
<td>1026h</td>
<td>PT2_INT</td>
<td>PT2_7</td>
<td>PT2_6</td>
<td>PT2_5</td>
<td>PT2_4</td>
<td>PT2_3</td>
<td>PT2_2</td>
<td>PT2_1</td>
<td>PT2_0</td>
<td>W/R</td>
</tr>
<tr>
<td>1027h</td>
<td>PT2_MOD</td>
<td>PT2_7</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
<tr>
<td>Address</td>
<td>Function</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3/TX</td>
<td>D2/RX</td>
<td>D1/LC</td>
<td>D0/LC</td>
<td>R/W</td>
</tr>
<tr>
<td>---------</td>
<td>----------</td>
<td>----</td>
<td>----</td>
<td>----</td>
<td>----</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-----</td>
</tr>
<tr>
<td>1028h</td>
<td>PT3</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>1029h</td>
<td>PT3_DIR</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>102Ah</td>
<td>PT3_INT</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>102Bh</td>
<td>I/O_R</td>
<td>R7</td>
<td>R6</td>
<td>R5</td>
<td>R4</td>
<td>R3</td>
<td>R2</td>
<td>R1</td>
<td>R0</td>
<td>R/W</td>
</tr>
<tr>
<td>102Ch</td>
<td>I/O_I</td>
<td>I7</td>
<td>I6</td>
<td>I5</td>
<td>I4</td>
<td>I3</td>
<td>I2</td>
<td>I1</td>
<td>I0</td>
<td>R/W</td>
</tr>
<tr>
<td>102Dh</td>
<td>I/O_INT</td>
<td>PT2_L_MD1</td>
<td>PT2_L_MD0</td>
<td>PT2_L_MD</td>
<td>PT2_L_MD</td>
<td>PT2_L_MD</td>
<td>PT2_L_MD</td>
<td>PT2_L_MD</td>
<td>PT2_L_MD</td>
<td>R/W</td>
</tr>
<tr>
<td>102Eh</td>
<td>I/O_WK_MD</td>
<td>PT3_H_EN</td>
<td>PT3_H_EN</td>
<td>PT3_H_MD</td>
<td>PT3_H_MD</td>
<td>PT3_H_MD</td>
<td>PT3_H_MD</td>
<td>PT3_H_MD</td>
<td>PT3_H_MD</td>
<td>R/W</td>
</tr>
<tr>
<td>102Fh</td>
<td>FBANK_L</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>1030h</td>
<td>TB_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1031h</td>
<td>LVD_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1032h</td>
<td>MEM_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1033h</td>
<td>LVD_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1034h</td>
<td>LVD_ST</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1035h</td>
<td>RXR</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>1036h</td>
<td>TXR</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>W</td>
</tr>
<tr>
<td>1037h</td>
<td>IR_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1038h</td>
<td>BAUD</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>D1</td>
</tr>
<tr>
<td>1039h</td>
<td>UR_ST</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>103Ah</td>
<td>ADC_H</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
<td>D8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>R</td>
</tr>
<tr>
<td>103Bh</td>
<td>ADC_L</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>R</td>
</tr>
<tr>
<td>103Ch</td>
<td>ADC_CTL(1)</td>
<td>INT_EN</td>
<td>ADET_WK_M</td>
<td>LOOP</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>R</td>
</tr>
<tr>
<td>103Dh</td>
<td>ADC_CTL(2)</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>103Eh</td>
<td>ADC_ST</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>103Fh</td>
<td>XT_SBANK_L</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>1040h</td>
<td>MTP_AL</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>1041h</td>
<td>MTP_AH</td>
<td>D15</td>
<td>D14</td>
<td>D13</td>
<td>D12</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
<td>D8</td>
<td>R/W</td>
</tr>
<tr>
<td>1042h</td>
<td>MTP_BL</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>1043h</td>
<td>MTP_BH</td>
<td>D15</td>
<td>D14</td>
<td>D13</td>
<td>D12</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
<td>D8</td>
<td>R/W</td>
</tr>
<tr>
<td>1044h</td>
<td>MTP_CL</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>R/W</td>
</tr>
<tr>
<td>1045h</td>
<td>MTP_CLH</td>
<td>D15</td>
<td>D14</td>
<td>D13</td>
<td>D12</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
<td>D8</td>
<td>R/W</td>
</tr>
<tr>
<td>1046h</td>
<td>MTP_MHL</td>
<td>D23</td>
<td>D22</td>
<td>D21</td>
<td>D20</td>
<td>D19</td>
<td>D18</td>
<td>D17</td>
<td>D16</td>
<td>R/W</td>
</tr>
<tr>
<td>1047h</td>
<td>MTP_CHH</td>
<td>D31</td>
<td>D30</td>
<td>D29</td>
<td>D28</td>
<td>D27</td>
<td>D26</td>
<td>D25</td>
<td>D24</td>
<td>R/W</td>
</tr>
<tr>
<td>1048h</td>
<td>MTP_CTL</td>
<td>OV3</td>
<td>OV2</td>
<td>OV1</td>
<td>OV0</td>
<td>CX_CL_R</td>
<td>ACC</td>
<td>AX</td>
<td>BX</td>
<td>R/W</td>
</tr>
<tr>
<td>1049h</td>
<td>LT_WK_CTL</td>
<td>REV.</td>
<td>1/60HZ_WK_MD</td>
<td>1HZ_WK_MD</td>
<td>2HZ_WK_MD</td>
<td>REV.</td>
<td>1/60HZ_WK_EN</td>
<td>1HZ_WK_EN</td>
<td>2HZ_WK_EN</td>
<td>R/W</td>
</tr>
<tr>
<td>104Ah</td>
<td>LT_WK_ST</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>104Bh</td>
<td>PWR_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>104Ch</td>
<td>CLK_CTL</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>Address</td>
<td>Description</td>
<td>Reset</td>
<td>Default</td>
<td>Access</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
<td>-------</td>
<td>---------</td>
<td>--------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0000h</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0001h</td>
<td>Timer 3 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0002h</td>
<td>Timer 2 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0003h</td>
<td>Timer 1 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0004h</td>
<td>Watch Dog NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0005h</td>
<td>Port 3 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0006h</td>
<td>Port 2 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0007h</td>
<td>Port 1 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Example:

LDA  #0Fh
STA  1000h ; Permit Port1, Port2, Port3 and WDT to produce NMI
          ; interrupt.

### [REG 1001h]: NMI Mask Register (2) [NMI_MK(2)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>1Min. NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>1HZ NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>2HZ NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

LDA  #02h
STA  1001h ; Permit 1Hz to produce NMI interrupt.

### [REG 1002h]: NMI Status Register (1) [NMI_ST(1)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>Timer 3 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>Timer 2 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>Timer 1 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>Watch Dog NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>Port 3 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Port 2 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Port 1 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example1:

LDA  1002h ; Can be used to diagnose which NMI occurs.

Example2:

LDA  1000h ; Can be used to diagnose which NMI occurs.

### [REG 1003h]: NMI Status Register (2) [NMI_ST(2)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>1Min. NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>1HZ NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>2HZ NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

LDA  1003h ; Can be used to diagnose which NMI occurs.
### [REG 1004h]: Clear NMI Status Register (1) [CLR_NMI(1)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>6</td>
<td>Clear Timer 3 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Clear Timer 2 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Clear Timer 1 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Clear Watch Dog NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Clear Port 3 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Clear Port 2 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Clear Port 1 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA  #7Fh
STA  1004h ; Clear Timer1~3, Port1~3, and WTD NMI Indicate.
```

### [REG 1005h]: Clear NMI Status Register (2) [CLR_NMI(2)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>2</td>
<td>Clear 1Min. NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Clear 1HZ NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Clear 2HZ NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA  #01h
STA  1005h ; Clear 2Hz NMI Indicate.
```

### [REG 1006h]: INT Mask Register (1) [INT_MK(1)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>Timer 3 INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Timer 2 INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Timer 1 INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

RAiO TECHNOLOGY INC.  19/118  www.raio.com.tw
### Port 3 INT Enable
0: Disable  
1: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Example:**
```
LDA #03h
STA 1006h ; Permit Port1 and Port2 produce INT interrupt.
```

### Port 2 INT Enable
0: Disable  
1: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Example:**
```
LDA #01h  
STA 1007h ; Permit 2Hz produce INT interrupt.
```

### Port 1 INT Enable
0: Disable  
1: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Example:**
```
LDA 1008h ; Can be used to diagnose which INT occurs.
```

### Bit Description

- **Bit Description**
  - 7: Reserved
  - 6: 2048HZ Time Base INT Enable
  - 5: 512HZ Time Base INT Enable
  - 4: 64HZ Time Base INT Enable
  - 3: Reserved
  - 2: 1Min. INT Enable
    - 0: Disable
    - 1: Enable
  - 1: 1HZ INT Enable
    - 0: Disable
    - 1: Enable
  - 0: 2HZ INT Enable
    - 0: Disable
    - 1: Enable

**Example:**
```
LDA #01h  
STA 1007h ; Permit 2Hz produce INT interrupt.
```

### Bit Description

- **Bit Description**
  - 7: Reserved
  - 6: Timer 3 INT Indicate
  - 5: Timer 2 INT Indicate
  - 4: Timer 1 INT Indicate
  - 3: Reserved
  - 2: Port 3 INT Indicate
  - 1: Port 2 INT Indicate
  - 0: Port 1 INT Indicate

**Example:**
```
LDA 1008h ; Can be used to diagnose which INT occurs.
```

### Bit Description

- **Bit Description**
  - 7: Reserved
<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>6</td>
<td>Clear Timer 3 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>5</td>
<td>Clear Timer 2 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>4</td>
<td>Clear Timer 1 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>2</td>
<td>Clear Port 3 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>1</td>
<td>Clear Port 2 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>0</td>
<td>Clear Port 1 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
</tbody>
</table>

Example:

LDA 1009h ; Can be used to diagnose which INT occurs.

[REG 100Ah]: Clear INT Status Register (1) [CLR_INT(1)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>6</td>
<td>Clear 2048HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>5</td>
<td>Clear 512HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>4</td>
<td>Clear 64HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>2</td>
<td>Clear 1Min. INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>1</td>
<td>Clear 1HZ INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>0</td>
<td>Clear 2HZ INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
</tbody>
</table>

Example:

LDA #77h
STA 100Ah ; Clear Timer1~3 and Port1~3 INT indicate.

[REG 100Bh]: Clear INT Status Register (2) [CLR_INT(2)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>6</td>
<td>Clear 2048HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>5</td>
<td>Clear 512HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>4</td>
<td>Clear 64HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>2</td>
<td>Clear 1Min. INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>1</td>
<td>Clear 1HZ INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>0</td>
<td>Clear 2HZ INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
</tbody>
</table>

Example:

LDA #01h
STA 100Bh ; Clear 2Hz INT indicate.
### [REG 100Ch]: Watch Dog Control Register [WDT_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Watch Dog Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Watch Dog Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Watch Dog Timer Clear</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Reset Watch Dog Timer, Write this bit high will cause Watch Dog Timer Reset. This bit will be clear automatically after clear.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Watch Dog Reset Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Example1:
```
LDA  #08h
STA  100Ch  ; Set Watch Dog Enable.
```

#### Example2:
```
LDA  #01h
STA  100Ch  ; Set Watch Dog Reset Enable.
```

### [REG 100Dh]: LCD Control Register [LCD_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2-1</td>
<td>Hi-Speed Control for External LCD Decoder</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>These two bits are used to add delay clock for LCD access time.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit2   Bit1   T1   T2   T3 (Unit: CPU Clock)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0    0   4.5   11  0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0    1   3.5   9   0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1    0   2.5   6   0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1    1   1.5   3   0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T1: Data Set-Up Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T2: Data Access Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T3: Data Hold Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>External LCD Driver Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is used to control the external LCD Driver interface enable or disable.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable, 1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>If set high, then the Port3 bit[1:0] are defined as LCD Driver interface signals.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PT3_1 → LCD_E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PT3_0 → LCD_RW</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Example:
```
LDA  #01h
STA  100Dh  ; Enable external LCD Driver interface and add delay
```
; clock.

[REG 100Eh]: LCD Command Register [LCD (1)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>This register is used for external LCD controller.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:
LDA #50h
STA 100Eh ; External LCD Driver Control Enable

[REG 100Fh]: LCD Data Register [LCD (2)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>This register is used for external LCD controller.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:
LDA #41h ; Data Write, write “A” into LCD screen.
STA 100Fh

[REG 1010h]: Timer 1 Count_H Register [TM1_H]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3-0</td>
<td>Timer 1 Down Count Data – High Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:
LDA #05h
STA 1010h ; Set Timer1 counter’s High-Byte(Bit11-8) at 05h
LDA #78h
STA 1011h ; Set Timer1 counter’s Low-Byte(Bit7-0) at 78h

[REG 1011h]: Timer 1 Count_L Register [TM1_L]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Timer 1 Down Count Data – Low Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:
LDA #1010h ; Set Timer1 counter at 578h
LDA #1011h
STA 1010h
LDA #05h
STA 1011h

[REG 1012h]: Timer 1 Control Register [TM1_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Timer 1 Enable or Timer 1 Start</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>Timer 1 wakeup enable from sleep mode.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>Timer 1 wakeup RESET enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>Timer 1 Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>Bit2</td>
<td>Bit1</td>
<td>Bit0</td>
<td>Clock Source</td>
<td>0h</td>
</tr>
<tr>
<td>------</td>
<td>------</td>
<td>------</td>
<td>-----------------------</td>
<td>------</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>External I/O Port (PT1_0)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK /2^16</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>USR_DIV_CLK /2^14</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>USR_DIV_CLK /2^10</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>USR_DIV_CLK /2^6</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK /2^2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>32768Hz</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>GND</td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA #C5h
STA 1012h ; Let Timer1 be Enable/Start ➔ Timer1 only count once and
; it with wakeup function.
; Timer1’s clock source set at USR_DIV_CLK /2^2.
```

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3-0</td>
<td>Timer 2 Down Count Data – High Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Timer 2 Down Count Data – Low Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

```
LDA #03h
STA 1013h ; Set Timer2 counter’s High-Byte(Bit11-8) at 03h
LDA #BBh
STA 1014h ; Set Timer2 counter’s Low-Byte(Bit7-0) at BBh
; Set Timer2 counter at 3BBh
```

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Timer 2 Enable or Timer 2 Start</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Disable/Stop</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable/Start</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Timer 2 wakeup enable from sleep mode.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Timer 2 wakeup RESET enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>Timer 2 Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Timer 2 Input Clock Source Select

<table>
<thead>
<tr>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Clock Source</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>External I/O Port (PT1_1)</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK /2^16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>USR_DIV_CLK /2^14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>USR_DIV_CLK /2^10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>USR_DIV_CLK /2^6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK /2^2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>32768Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>TIMER 1 Output</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA  #63h
STA  1015h  ; Let Timer2 Wakeup/Reset Enable.
            ; Timer2's clock source set at USR_DIV_CLK /2^10.
```

### [REG 1016h]: Timer 3 Count_H Register [TM3_H]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3-0</td>
<td>Timer 3 Down Count Data – High Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

```
LDA  #03h
STA  1016h  ; Set Timer3 counter’s High-Byte(Bit11-8) at 03h
LDA  #BBh
STA  1017h  ; Set Timer3 counter’s Low-Byte(Bit7-0) at BBh
            ; Set Timer3 counter at 3BBh
```

### [REG 1017h]: Timer 3 Count_L Register [TM3_L]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Timer 3 Down Count Data – Low Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1018h]: Timer 3 Control Register [TM3_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Timer 3 Enable or Timer 3 Start</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Timer 3 Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

```
0: Disable/Stop
1: Enable/Start
```

```
0: Disable
1: Enable
```

```
0h 0h R/W
```
**Timer 3 Input Clock Source Select**

<table>
<thead>
<tr>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Clock Source</th>
<th>0h</th>
<th>0h</th>
<th>R/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>USR_DIV_CLK/2^16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK/2^14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>USR_DIV_CLK/2^10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>USR_DIV_CLK/2^6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>USR_DIV_CLK/2^2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK/2^1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>USR_DIV_CLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>32768Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA #8Dh
STA 1018h ; Set Timer3 in loop mode before enable.
; Timer3’s clock source set at USR_DIV_CLK/2^1.
LDA #89h
STA 1018h ; Timer3 start count.
```

[REG 1019h]: DAC High Byte Data Register [DAC_H]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>10-Bit DAC Output Data[9:2]</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
</tbody>
</table>

Example:

```
LDA #01h
STA 101Bh ; Set DAC1 Enable, Iout Resolution is 0~2mA.
LDA #80h
STA 1019h ; Data 80h to DAC→Output middle current.
```

[REG 101Ah]: DAC Data Register [DAC_L]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6</td>
<td>10-Bit DAC Output Data[1:0]</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td>5-0</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>

[REG 101Bh]: DAC Control Register [DAC_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>2</td>
<td>Mode Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Audio Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: DTMF Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1-0</td>
<td>DAC Output Resolution Control</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA #00h
```
STA 101Bh ; Disable DAC.

[REG 101Ch]: PWM Data Register [PWM]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>8-bit PWM Data</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:
LDA #10h
STA 101Dh ; Set PWM1 Enable, produce 50% Duty cycle's PWM pulse.
; PWM Resolution is 8-Bit.
LDA #60h
STA 101Ch ; Data 60h to PWM output

[REG 101Dh]: PWM Control Register [PWM_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>PWM Enable</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>When PWM mode enable then the PT2_7 change to PWM1 output and PT2_6 change to PWM2 output.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PWM Mode Control</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Single Mode (PWM1 Enable)</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Differential Mode (PWM1 &amp; PWM2 Enable)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Single Mode</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Differential Mode</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Mode</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Mode</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>-----------------------------------------------------------------------------------</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PWM1 : 00<del>FFh 80</del>FFh</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>PWM2 : X 00~7Fh</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>PWM Duty Control</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 50 Duty Cycle for Differential Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 100 Duty Cycle for Differential Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1-0</td>
<td>PWM Resolution Control</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>00 8-Bit</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>01 7-Bit</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>10 6-Bit</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>11 5-Bit</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 101Eh]: External Register[EX_IO]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Data7-0</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
</tbody>
</table>

[REG 101Fh]: External REG-101Eh Control Register [EX_IO_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2</td>
<td>Reserved</td>
<td></td>
<td></td>
<td>--</td>
</tr>
</tbody>
</table>

RA8917
8-Bit Micro-Controller
**External REG-101Eh Write Signal Active Control**

This bit is used to control the active state of REG-101Eh write signal.

- 0: Active Low
- 1: Active High

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>External REG-101Eh Write Signal Active Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**External REG-101Eh Write Signal Control**

This bit is used to control the output of REG-101Eh write signal. If set high, then the Port2 bit5 is defined as the output of REG-101Eh write.

- 0: Disable
- 1: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>External REG-101Eh Write Signal Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1020h]: Port 1 Data Register [PT1]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2</td>
<td>Bit-[7:2] of Output Data to Port 1 or Input from Port 1</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Bit-1 of Output Data to Port 1 or Input from Port 1</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Bit-0 of Output Data to Port 1 or Input from Port 1</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: If the Port1 is output mode then the read access data is from the register 1020h. If the Port1 is input mode the read access is from Port1 I/O.

**Example:**

```
LDA #FFh
STA 1021h ; Set Port1 at output mode.
LDA #AAh
STA 1020h ; Output AAh to port1 Bit7~0.
```

**[REG 1021h]: Port 1 Direction Control Register [PT1_DIR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Select the Output or Input Mode of Port 1</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: If PT1[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.

**Example:**

```
LDA #F0h
STA 1021h ; Set Port1 Bit7~4 at output mode, Bit3~0 at input mode.
```

**[REG 1022h]: Port1 Interrupt Trigger Indicate Register [PT1_INT]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Port1 Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: After using "Interrupt Indicate", users have to write command cleaning it to “0”.

**Example:**

```
LDA 1022 ; Determine which bit of Port1 is Interrupt.
```
**RA8917**

**Version 1.6**

8-Bit Micro-Controller

[REG 1023h]: Port 1 Output Mode Select Register [PT1_MOD]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Select the Output Mode for CMOS or Open-Drain Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: CMOS Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Open-Drain Mode. In this mode, Port 1 Direction Control Register controls the Port1 output data.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:
```
LDA   #FFh
STA  1021h ; Set Port1 at output mode.
LDA   #F0h
STA  1023h ; Set Port1 Bit7~4 at Open-Drain output mode.
           ; Bit3~0 is CMOS mode output mode.
```

[REG 1024h]: Port 2 Data Register [PT2]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Bit-7 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the output of PWM2 when PWM enable(REG-101Dh bit4 = ‘1’).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Bit-6 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the output of PWM2 when PWM enable(REG-101Dh bit4 = ‘1’).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Bit-5 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the output of REG-101Eh write signal (EXP_WR#) when external REG-101Eh write enabled (REG-101Fh bit0= ‘1’).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Bit-4 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the secondary external Flash chip select output(FL_CE2#) when using two external flashes.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Bit-3 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the output of LVD indicated(LVD#) when external LVD enabled(REG-1033h bit2= ‘1’).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Bit-2 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the external memory write enable(MEM_WE#) when external memory decoder selected(REG-1032h bit0= ‘1’).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Bit-1 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the external memory output enable (MEM_OE#) when external memory decoder selected(REG-1032h bit0= ‘1’).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Bit-0 of Output Data to Port 2 or Input from Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is also as the external memory chip select output (MEM_CE#) when external memory decoder enabled (REG-1032h bit0= ‘1’). The external memory is decoded when CPU access from $4000 to $7FFF.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: If the Port2 is output mode then the read access date is from the register 1024h. If the Port2 is input mode then the read access is from Port2 I/O.

Example:
```
LDA   #FFh
STA  1025h ; Set Port2 at output mode.
LDA   #AAh
STA  1024h ; Output AAh to port2 Bit7~0.
```
### [REG 1025h]: Port 2 Direction Control Register [PT2_DIR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
| 7-0 | Select the Output or Input Mode of Port 2  
|     | 0: Input Mode  
|     | 1: Output Mode  
|     | Note: If PT2[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup. | 0h | 0h | R/W |

Example:
```
LDA   #F0h
STA   1025h  ; Set Port2 Bit7~4 at output mode, Bit3~0 at input mode.
```

### [REG 1026h]: Port2 Interrupt Trigger Indicate Register [PT2_INT]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
| 7-0 | Port2 Bit[7:0]  
|     | Note: After using “Interrupt Indicate”, users have to write command cleaning it to “0”. | 0h | 0h | R/W |

Example:
```
LDA   1026h  ; Determine which bit of Port2 in Interrupt.
```

### [REG 1027h]: Port 2 Output Mode Select Register [PT2_MOD]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
| 7-0 | Select the Output Mode for CMOS or Open-Drain Mode  
|     | 0: CMOS Mode  
|     | 1: Open-Drain Mode. In this mode, Port 2 Direction Control Register controls the Port2 output data. | 0h | 0h | R/W |

Example:
```
LDA   #FFh
STA   1025h  ; Set Port2 at output mode.
LDA   #F0h
STA   1027h  ; Set Port2 Bit7~4 at Open-Drain output mode.  
|     | Bit3~0 is CMOS mode output mode. |
```

### [REG 1028h]: Port 3 Data Register[PT3]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Bit-[7:4] of Output Data to Port 3 or Input from Port 3.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
| 3   | Bit-3 of Output Data to Port 3 or Input from Port 3.  
|     | This bit is also as the output of User UART TX when user UART enable( REG-1038h bit4 == '1'). | 0h | 0h | R/W |
| 2   | Bit-2 of Output Data to Port 3 or Input from Port 3.  
|     | This bit is also as the input of User UART RX when user UART enable( REG-1038h bit4 == '1'). | 0h | 0h | R/W |
| 1   | Bit-1 of Output Data to Port 3 or Input from Port 3.  
|     | This bit is also as the output of external LCD chip select(LCD_E) when external LCD enabled(REG-100Dh bit0= ’1’). The external LCD is decoded at REG-100Eh & REG-100Fh. | 0h | 0h | R/W |
0 Bit-0 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of external LCD R/W(LCD_RW) when external LCD enabled(REG-100Dh bit0= '1').

Note: If the Port3 is output mode then the read access date is from the register 1028h. If the Port3 is input mode then the read access is form Port3 I/O.

Example:

```
LDA   #FFh
STA  1029h  ; Set Port3 at output mode.
LDA   #AAh
STA  1028h  ; Output AAh to port3 Bit7~0.
```

[REG 1029h]: Port 3 Direction Control Register [PT3_DIR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Select the Output or Input Mode of Port 3 0: Input Mode 1: Output Mode  Note: If PT3[0..7] is set as Output mode, then it will not occur Interrupt or Wakeup.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

```
LDA   #F0h
STA  1029h  ; Set Port3 Bit7~4 at output mode, Bit3~0 at input mode.
```

[REG 102Ah]: Port3 Interrupt Trigger Indicate Register [PT3_INT]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Port3 Bit[7:0] Interrupt Indicate  Note: After using “Interrupt Indicate”, users have to write command cleaning it to “0”.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

```
LDA   102Ah  ; Determine which bit of Port3 is Interrupt.
```

[REG 102Bh]: I/O Resistor Control Register [I/O_R]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT4 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>PT4 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>PT3 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>PT3 Low Nibble Resistor Select 0: None 1: Pull Up: 50Kohm</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>PT2 High Nibble Resistor Select 0: None 1: Pull Up: 50Kohm</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
### RA8917

#### 8-Bit Micro-Controller

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>PT2 Low Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>PT1 High Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>PT1 Low Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:
```
LDA  #3Fh
STA  102Bh ; Set Port1~3 resister select is pull up 50K ohm.
```

#### [REG 102Ch]: I/O Driving Current Control Register [I/O_I]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT4 High Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PT4 Low Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PT3 High Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PT3 Low Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PT2 High Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA (24mA for PT2_6, PT2_7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA (36mA for PT2_6, PT2_7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>PT2 Low Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>PT1 High Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>PT1 Low Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:
```
LDA  #00h
STA  102Ch ; Set Port1~3 current select is 4mA.
```

#### [REG 102Dh]: I/O Interrupt Control Register [I/O_INT]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT2 High Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Value 1</td>
<td>Value 2</td>
<td>Access</td>
</tr>
<tr>
<td>---</td>
<td>-----------------------------------------------------------------------------</td>
<td>---------</td>
<td>---------</td>
<td>----------</td>
</tr>
<tr>
<td>6</td>
<td>PT2 Low Nibble Clock Select&lt;br&gt;0: Normal&lt;br&gt;1: Add Filter to De-bounce</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>PT1 High Nibble Clock Select&lt;br&gt;0: Normal&lt;br&gt;1: Add Filter to De-bounce</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>PT1 Low Nibble Clock Select&lt;br&gt;0: Normal&lt;br&gt;1: Add Filter to De-bounce</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>PT2 High Nibble Interrupt or Wakeup (default) / PT1_3 Bit Interrupt&lt;br&gt;0: Disable&lt;br&gt;1: Enable&lt;br&gt;When REG[1034h] bit7 set as “1”, which is Bit Interrupt Mode, and then PT1 bit3 could be used as Interrupt. Please refer to the following set-up:</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>PT2 Low Nibble Interrupt or Wakeup (default) / PT1_2 Bit Interrupt&lt;br&gt;0: Disable&lt;br&gt;1: Enable&lt;br&gt;When REG[1034h] bit7 set as “1”, which is Bit Interrupt Mode, and then PT1 bit2 could be used as Interrupt. Please refer to the following set-up:</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>PT1 High Nibble Interrupt or Wakeup (default) / PT1_1 Bit Interrupt&lt;br&gt;0: Disable&lt;br&gt;1: Enable&lt;br&gt;When REG[1034h] bit7 set as “1”, which is Bit Interrupt Mode, and then PT1 bit1 could be used as Interrupt. Please refer to the following set-up:</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>PT1 Low Nibble Interrupt or Wakeup (default) / PT1_0 Bit Interrupt&lt;br&gt;0: Disable&lt;br&gt;1: Enable&lt;br&gt;When REG[1034h] bit7 set as “1”, which is Bit Interrupt Mode, and then PT1 bit0 could be used as Interrupt. Please refer to the following set-up:</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

```
LDA  #0Ch
STA  102Dh ; It permitted I Interrupt or Wakeup occurs from Port2.
```
### [REG 102Eh]: I/O Interrupt/Wakeup Mode Select Register [I/O_INT&WK_MD]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6</td>
<td>PT2 High Nibble Mode Select</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit7  Bit6   Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Rising-Edge Trigger</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Falling-Edge Trigger</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Level Change Trigger (1)</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Level Change Trigger (2)</td>
<td>0h</td>
<td>0h</td>
</tr>
</tbody>
</table>

**Level Change Trigger (1):**

\[(1111) \rightarrow \text{Setup} \rightarrow (1111) \rightarrow (1110) \rightarrow (1010) \rightarrow (0000) \rightarrow (1111) \rightarrow \text{Return} \rightarrow (1011) \rightarrow \text{Trigger}\]

**Level Change Trigger (2):**

\[(1111) \rightarrow \text{Setup} \rightarrow (1111) \rightarrow (1110) \rightarrow (1010) \rightarrow (1011) \rightarrow (1111) \rightarrow \text{Triggere} \rightarrow (1010) \rightarrow (1011) \rightarrow (1111) \rightarrow \text{Trigger}\]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-4</td>
<td>PT2 Low Nibble Mode Select</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit5  Bit4   Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Rising-Edge Trigger</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Falling-Edge Trigger</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Level Change Trigger (1)</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Level Change Trigger (2)</td>
<td>0h</td>
<td>0h</td>
</tr>
</tbody>
</table>

### Example:

LDA #1Fh  ; Set PT2 High Nibble is Rising-Edge Trigger, Low-Nibble is Falling-Edge Trigger and PT1 is Level Change Trigger (2).

### [REG 102Fh]: I/O Wakeup Reset Control Register [I/O_WK_MD]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT3 High Nibble Interrupt or Wakeup</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Disable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: PT3[7:4] are Rising-Edge Trigger.
6  PT3 Low Nibble Interrupt or Wakeup
  0: Disable
  1: Enable
  Note: PT3[1:0] are Rising-Edge Trigger, PT3[3:2] are Falling-Edge Trigger.
  0h 0h R/W

5  PT3 High Nibble Wakeup Reset
  0: Wakeup CPU Only
  1: Wakeup & Cause Reset
  0h 0h R/W

4  PT3 Low Nibble Wakeup Reset
  0: Wakeup CPU Only
  1: Wakeup & Cause Reset
  0h 0h R/W

3  PT2 High Nibble Wakeup Reset
  0: Wakeup CPU Only
  1: Wakeup & Cause Reset
  0h 0h R/W

2  PT2 Low Nibble Wakeup Reset
  0: Wakeup CPU Only
  1: Wakeup & Cause Reset
  0h 0h R/W

1  PT1 High Nibble Wakeup Reset
  0: Wakeup CPU Only
  1: Wakeup & Cause Reset
  0h 0h R/W

0  PT1 Low Nibble Wakeup Reset
  0: Wakeup CPU Only
  1: Wakeup & Cause Reset
  0h 0h R/W

Example:
  LDA  #0Ch
  STA  102Fh ; Set PT2 Wakeup & Cause Reset Selected.

[REG 1030h]: Flash Bank Low Byte Register [FBANK_L]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Flash Bank Low Byte Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: Flash Bank High Byte Register is [105Ah]

Example:
  LDA  #01h
  STA  1030h ; Set BK1 equal to 01h.

[REG 1031h]: Timer / Clock Control Register [TB_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>
| 4   | Mac Control
  0: Disable
  1: Enable
 | 0h 0h R/W |
| 3   | Time Base 2048Hz Control
  0: Disable
  1: Enable
 | 0h 0h R/W |
| 2   | Time Base 512Hz/64Hz Control
  0: Disable
  1: Enable
 | 0h 0h R/W |
Time Base 1Hz/2Hz/1Min Control

<table>
<thead>
<tr>
<th>Bit1</th>
<th>Bit0</th>
<th>Delay Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Disable</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1Hz/2Hz Enable</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Not available</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1Min/1Hz/2Hz</td>
</tr>
</tbody>
</table>

Example1:
LDA #10h
STA 1031h ; Enable MAC Control.

Example2:
LDA #01h
STA 1031h ; Enable 1Hz/2Hz Control.

[REG 1032h]: Memory Control Register [MEM_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>6</td>
<td>External Memory (SRAM &amp; Flash) control pin share</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>External Flash &amp; SRAM share the FL_OE# and FL_WE# pins</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: The secondary Flash FL_CE# pin must be pulled high.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>EDO Speed Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>High Speed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Low Speed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EDO Re-fresh Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>32KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>64KHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>EDO RAM Enable Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-1</td>
<td>Hi-Speed Control for External Flash or Memory</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>Bit2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Bit1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Delay Cycle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0: add Three delay cycle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1: add Two delay cycle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0: add One delay cycle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1: add Zero delay cycle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>External Memory Control. This bit is used to control the external memory</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>interface enable or disable. If set high, then the Port2 bit[2-0] are</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>defined as memory interface signals.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PT2_0 → MEM_CE#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PT2_1 → MEM_OE#</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PT2_2 → MEM_WE#</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:
LDA #05h
STA 1032h ; External Memory Control Enable, add One delay cycle.
### [REG 1033h]: LVD Control Register [LVD_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>
| 3   | LVD Output Control  
   This bit is used to control the output of LVD. If set high, then the Port2 bit3 is defined as the output of LVD#.  
   0: Disable LVD output  
   1: Enable LVD Output | 0h  | 0h  | R/W |
| 2   | LVD Enable Control  
   0: Disable  
   1: Enable | 0h  | 0h  | R/W |
| 1-0 | LVD Voltage Select  
   Bit1 Bit0 Detected Voltage  
   | 0  0  3V  
   0  1  2.8V  
   1  0  2.6V  
   1  1  2.4V | 0h  | 0h  | R/W |

If the LVD enabled, the bit0 of register $1034h will indicate the status of LVD.

Example:

```
LDA  #0Ch
STA  1033h ; LVD Control Enable, LVD Detected Voltage Select 3V  
            ; LVD Output Enable.
```

### [REG 1034h]: LVD Status Register [LVD_ST]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
| 7   | I/O Interrupt mode for Nibble or Bit control  
   0: Nibble Interrupt Control  
   PT1 bit0~3, PT1 bit4~7, PT2 bit0~3 and PT2 bit4~7 are Nibble Interrupt.  
   1: Bit Interrupt Control  
   PT1 bit0~3 are Bit Interrupt | 0h  | 0h  | R/W |
| 6-1 | Not Used | --    | --      | --     |
| 0   | LVD Indicate.  
   0: Normal Voltage  
   1: Low Voltage Detected! | 0h  | 0h  | R |

Note: When REG[1034]bit7 is set as “1”, please also refer to the set up of REG[102Dh] bit0~3, the bit interrupt.

### [REG 1035h]: User UART Receive Register (Read Only) [RXR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>UART Receive Data</td>
<td>Xh</td>
<td>Xh</td>
<td>R</td>
</tr>
</tbody>
</table>

### [REG 1035h]: User UART Transmit Register (Write Only) [TXR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>UART Transmit Data</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
</tbody>
</table>

### [REG 1036h]: IR Mode Select [IR_CTL]
### UART IR Mode Select

<table>
<thead>
<tr>
<th>Bit1</th>
<th>Bit0</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>ASK IR</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>IrDA IR</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>IrDA IR</td>
</tr>
</tbody>
</table>

#### Example:
```
LDA  #03h
STA  1036h ; Set IrDA IR Mode.
```

### UART Baud Rate

<table>
<thead>
<tr>
<th>Bit1</th>
<th>Bit0</th>
<th>Baud Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>115200bps</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>57600bps</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>38400bps</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>28800bps</td>
</tr>
</tbody>
</table>

#### Example:
```
LDA  #00h
STA  1037h ; Set Baud Rate into 115200bps.
```

### UART Control Register [UR_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Transmit Empty Indicate INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>Received Data Available Indicate INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>User UART Enable Control</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>4</td>
<td>User UART Enable Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>UART Transmitter Inverter</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>UART Receiver Inverter</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>UART RX Wake Up Mode Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>UART RX Wake Up</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
Example:
```Assembly
LDA #10h
STA 1038h ; Enable UART function.
```

### [REG 1039h]: User UART Status Register [UR_ST]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Transmit Register Empty Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is set when transmit complete and be clear when write a data to UART Transmit Register (REG-1035h).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Received Data Available Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is set when UART received an available data but it will not be clear when the host read the data from UART Receive Register (REG-1035h).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-0</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 103Ah]: ADC High-Byte Register [ADC_H]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>ADC Output Data Bit[11:4]</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
</tbody>
</table>

### [REG 103Bh]: ADC Low-Byte Register [ADC_L]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>ADC Output Data Bit[3:0]</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td>3-0</td>
<td>Not Used</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
</tbody>
</table>

### [REG 103Ch]: ADC Control Register(1) [ADC_CTL(1)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td>6</td>
<td>ADC Interrupt Enable</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>ADC Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>ADC Mode Select</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: 4-Channels ADC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Touch Panel</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>ADC Enable</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ADC Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Low Frequency → 230Khz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: High Frequency → 460Khz</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ADC Channel Select

<table>
<thead>
<tr>
<th>Bit1</th>
<th>Bit0</th>
<th>Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>

Note: When RA8917 enters into Saving Mode, in order to avoid the leaking behavior, please do not let ADC Channel Floating or set ADC Type as Touch Panel function.

---

Example:

```assembly
LDA #08h
STA 103Ch ; Enable ADC and using ADC channel 0.
```

[REG 103Dh]: ADC Control Register(2) [ADC_CTL(2)]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ADET Wake Up</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>ADET Wake Up Mode Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: ADET Wake Up Only</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: ADET Wake Up &amp; Caused Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-4</td>
<td>Reserved</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Touch Panel Switch Y2 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Touch Panel Switch Y1 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Touch Panel Switch X2 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Touch Panel Switch X1 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```assembly
LDA #C0h
STA 103Dh ; Enable ADET Wakeup & Reset.
```

[REG 103Eh]: ADC Status Register [ADC_ST]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1</td>
<td>ADC Transfer Done</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td>0: Not Ready</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Ready</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: When ADC is under One Time Mode (No Loop) and data transfer is finished, then it will generate Ready Signal (Bit 1=1). At this time, users need to clean the Ready Signal and let it become Bit 1=0 before read the next data.
### Touch Panel Detector

<table>
<thead>
<tr>
<th>Touch Panel Detector</th>
<th>0: Normal</th>
<th>1: Touch Detected</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td></td>
</tr>
</tbody>
</table>

### [REG 103Fh]: External SRAM Bank Low Byte Register [Ext_SBANK_L]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>External SRAM Bank Low Byte Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: External SRAM Bank High Byte Register is [105Bh]

### [REG 1040h]: Multiplier A Low-Byte Register [MTP_AL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier A Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1041h]: Multiplier A High-Byte Register [MTP_AH]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier A Data Bit[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1042h]: Multiplier B Low-Byte Register [MTP_BL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier B Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1043h]: Multiplier B High-Byte Register [MTP_BH]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier B Data Bit[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1044h]: Multiplier C Low Word Low-Byte Register [MTP_CLL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1045h]: Multiplier C Low Word High-Byte Register [MTP_CLH]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1046h]: Multiplier C High Word Low-Byte Register [MTP_CHL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[23:16]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1047h]: Multiplier C High Word High-Byte Register [MTP_CHH]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[31:24]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1048h]: Multiplier Control Register [MTP_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Overflow Flag</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td>3</td>
<td>Clear CX</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Clear CX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Accumulate Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable, CX = AX x BX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable, CXn+1 = AX x BX + CXn</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### RA8917

#### Version 1.6

**RAiO TECHNOLOGY INC.**

**www.raio.com.tw**

---

**RA8917**

**8-Bit Micro-Controller**

1. **AX 8/16Bit Select**
   - 0: AX = 16Bit
   - 1: AX = 8Bit
   - Reset: 0h
   - Default: 0h
   - Access: R/W

2. **BX 8/16Bit Select**
   - 0: BX = 16Bit
   - 1: BX = 8Bit
   - Reset: 0h
   - Default: 0h
   - Access: R/W

---

**[REG 1049h]: Low Speed Timer Control Register [LT_WK_CTL]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>1Min. Wake Up Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Wake Up Only</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Wake Up and Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1Hz Wake Up Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Wake Up Only</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Wake Up and Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>2Hz Wake Up Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Wake Up Only</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Wake Up and Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>1Min. Wake Up</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1Hz Wake Up</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>2Hz Wake Up</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```asm
LDA  #22h
STA  1049h  ; Enable 1Hz Wakeup, Wakeup and Reset mode.
```

---

**[REG 104Ah]: Low Speed Timer Status Register [LT_WK_ST]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>1Min. Wake Up Indicate.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>1Hz Wake Up Indicate.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>2Hz Wake Up Indicate.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

```asm
LDA  104Ah  ; Low Speed Timer Indicate.
```

---

**[REG 104Bh]: Power Control Register [PWR_CTL]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>Bit</td>
<td>Description</td>
<td>Reset</td>
<td>Default</td>
<td>Access</td>
</tr>
<tr>
<td>-----</td>
<td>-------------------------------------------------</td>
<td>-------</td>
<td>---------</td>
<td>--------</td>
</tr>
<tr>
<td>3</td>
<td>Extra Sleep Mode (Only at RTC Mode)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Normal Sleep</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Extra Deep Sleep</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>In this mode, the Divisor is off and only 32768Hz X'tal, Low speed Timer circuit are active. But the Wakeup with Reset function is inhibited. This bit must used to go with bit-1 and bit-0. Only available when REG[104Bh] Bit[1:0] = 11b.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Software Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Disable.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Reset CPU, Write this bit high will cause CPU Reset. This bit will be clear automatically after reset.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Sleep Mode Select</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Normal Sleep</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Deep Sleep</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit must used to go with bit-0.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Wakeup mode operation please reference Table 8-3</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Sleep Mode Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Normal Operation Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Enter Sleep Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example1: (Sleep Mode)

```
LDA  #01h
STA  104Bh  ; Enter Sleep Mode
```

Example2: (Deep Sleep Mode)

```
LDA  #02h
STA  104Bh  ; Determine Deep Sleep Mode
LDA  104Bh
ORA  #01h
STA  104Bh  ; Enter Deep Sleep Mode
```

Example3: (Extra Sleep Mode--Only at RTC Mode)

```
LDA  #0Ah
STA  104Bh  ; Determine Deep Sleep Mode
LDA  104Bh
ORA  #0Bh
STA  104Bh  ; Enter Extra Sleep Mode
```

[REG 104Ch]: Clock Control Register [CLK_CTL]
**RA8917**

**Version 1.6**  
**8-Bit Micro-Controller**

<table>
<thead>
<tr>
<th></th>
<th>32768Hz X’tal-Oscillator On/Off Control</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>32768Hz X’tal-Oscillator On</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 32768Hz X’tal-Oscillator Off</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0h</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0h</td>
<td></td>
</tr>
<tr>
<td></td>
<td>R/W</td>
<td></td>
</tr>
</tbody>
</table>

Example:
```
LDA  #10h
STA  104Ch ; Set CPU Clock is OSC2_CLK/2.
```

**[REG 104Dh]: Reset Status Register [RST_ST]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Power On Reset Indicate</td>
<td>1h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>RESET (RST#) Pin Reset Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>Watch-Dog Reset Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>Software Reset Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>I/O Wake Up Reset Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>System UART RX Wake Up Reset Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>UART RX Wake Up Reset Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Not Used</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
</tbody>
</table>

**[REG 104Eh]: Port 4 Data Register [PT4]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Bit-[7:0] of Output Data to Port 4 or Input from Port 4.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: If the Port4 is output mode then the read access date is from the register 1028h.  
If the Port4 is input mode then the read access is from Port4 I/O.

**[REG 104Fh]: Port 4 Direction Control Register [PT4_DIR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Select the Output or Input Mode of Port 4</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Input Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Output Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**[REG 1050h]: Programming Flash Control Register [PFCR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>5</td>
<td>Erase Status</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Erase Error</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Erase Success</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Erase Type</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Chip Erase</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Sector Erase</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Programming Status</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Programming Error</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Programming Success</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Flash Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Flash Chip1 (FL_CE# active)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Flash Chip2 (FL_CE2# active)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>One or Two External Flash Option. This bit is used to indicate the external Flash number. This bit is read only.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: One External Flash</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Two External Flash</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**RA8917**

### 0: Flash Type

| 0 | Command 1 (Reference 8.3.1) |
| 1 | Command 2 (Reference 8.3.1) |

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0h 0h</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Example:

```
LDA #00h
STA 1050h ; Set One External Flash, Flash Type is Command 1
```

#### Registers:

**[REG 1051h]: Programming Flash FBANK High Byte Register [PFBHR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Bank Data [11:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1052h]: Programming Flash FBANK Low Byte Register [PFBLR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Bank Data [7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1053h]: Programming Flash Address High Byte Register [PFAHR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Programming Flash Address --&gt; A[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1054h]: Programming Flash Address Low Byte Register [PFALR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Programming Flash Address A[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1055h]: Programming Flash Data Register [PFDR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Programming Data</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1056h]: Flash Sector Address High Byte Register [FSAHR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Flash Sector High Byte Address</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1057h]: Flash Sector Address Middle Byte Register [FSAMR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Flash Sector Middle Byte Address</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1058h]: Flash Sector Address Low Byte Register [FSALR]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Flash Sector Low Byte Address</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 105Ah]: Flash Bank High Byte Register [FBANK_H]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-0</td>
<td>Flash Bank High Byte Data Bit [11:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Note: Flash Bank Low Byte Register is [1030h]

**[REG 105Bh]: External SRAM Bank High Byte Register [EXT_SBANK_H]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Not Used.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
3-0 External SRAM Bank High Byte Data Bit[11:8]  
Note: External SRAM Bank Low Byte Register is [103Fh]  

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-0</td>
<td>0h 0h R/W</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**[REG 105Fh]: Analog Switch Control Register [SW_CTL]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3</td>
<td>Reserved.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>Analog Switch 3 Enable.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Analog Switch 2 Enable.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Analog Switch 1 Enable.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1060h]: EDO RAM Control Register [EDO_CTL]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3</td>
<td>Reserved.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>EDO RAM MODE:</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Configuration type:</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1061h]: EDO RAM Address Lower-Byte Register [EDO_AL]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>EDO RAM Address Lower 8 bits. (A[7:0])</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1062h]: EDO RAM Address Middle -Byte Register [EDO_AM]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>EDO RAM Address Middle 8 bits. (A[15:8])</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1063h]: EDO RAM Address Upper -Byte Register [EDO_AH]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6-0</td>
<td>EDO RAM Address Upper 7 bits. (A[23:16])</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1064h]: EDO RAM Data Register [EDO_DA]**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>EDO RAM DATA.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1068h]: Vector Control Register [VEC_CTL]**
<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>NMI Vector Enable Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>INT Vector Enable Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-0</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1069h]: Non-Mask Interrupt Priority Register 1 [NMI_PRI1]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority NP[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 106Ah]: Non-Mask Interrupt Priority Register 2 [NMI_PRI2]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority NP[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 106Bh]: Interrupt Priority Register 1 [INT_PRI1]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority IP[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 106Ch]: Interrupt Priority Register 2 [INT_PRI2]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority IP[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
8. Function Description

8.1 System Clock

RA8917- built in two Oscillator (OSC1 & OSC2) circuit. One is for connecting an external 32.768KHz crystal to generate a low speed system clock, and the other one, matched with hardware set-up pin, is by users' need to connect different crystal (1.8432 / 3.6864 / 5.5296 / 7.3728 / 11.0592 / 14.7456 / 18.432 / 22.1841MHz) for different system clock. Please refer to Figure 8-1.

From Figure 8-1, you will know that system clock is controlled by [REG 104Ch]. The descriptions of this Register are listed underneath, and we also provide an example program to explain how to use them.
[REG 104Ch]: Clock Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4-2</td>
<td>CPU Clock Select</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bit4 Bit3 Bit2 CPU Clock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>x       x</td>
<td>OSC2_CLK</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0       0</td>
<td>OSC2_CLK /2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0       1</td>
<td>OSC2_CLK /4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1       x</td>
<td>OSC2_CLK /8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>System X'tal Clock (OSC2) On/Off Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>32768Hz X'tal-Oscillator On/Off Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

```
LDA #00000000b      ; System X'tal Clock ON
STA 104Ch           ; CPU Clock → OSC_CLK
LDA #00100010b      ; System X'tal Clock Disable, USR_DIV_CLK → 32768Hz
STA 104Ch
```

8.2 CPU Operation Mode

8.2.1 Reset & Idle & Sleep & Power Saving Mode

RESET can be produced by Power On, RESET# input Low, Software Reset, Watch Dog overflow, Timer overflow, 1Hz, 2Hz, 1Min. and I/O. At this time, the chip will remain RESET until a movement of OST(Oscillator Start-up Timer) or RESET# input High. When it is RESET, the statuses are as following:

- Continue to oscillate or being initialized (electric power raise or Wake Up from SLEEP)
- All I/O pins (PT1, PT2, PT3) enter into high impedance condition
- Set program counter as “FFFF~FFFF”
- Registers are set as initial value

Figure 8-2 below is RESET schema, and Figure 8-3 is RESET Block Diagram. The functions of other RESET will be explained in the relevant chapters.
Figure 8-2 RESET Schematic

Figure 8-3 RESET Block Diagram
**Figure 8-4 CPU Operation Diagram**

**Table 8-2 CPU Operation Mode Setting**

<table>
<thead>
<tr>
<th>POWER SAVING MODE</th>
<th>MASTER_CLK NORMAL MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>32768Hz OSC: stopped [REG 104Ch] Bit0 Xtal-Oscillator Off</td>
<td>32768Hz OSC: oscillating [REG 104Ch] Bit0 Xtal-Oscillator On</td>
</tr>
<tr>
<td>OSC2: turned on [REG 104Ch] Bit1 Disable</td>
<td>OSC2: turned on [REG 104Ch] Bit1 System Clock On</td>
</tr>
<tr>
<td>CPU: sleep mode [REG 104Bh] Bit0 CPU Enter Sleep</td>
<td>CPU: normal mode [REG 104Bh] Bit0 Normal Mode</td>
</tr>
<tr>
<td></td>
<td>CPU Clock Select [REG 104Ch] Bit4 ~2</td>
</tr>
<tr>
<td></td>
<td>Bit4</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SLEEP MODE</th>
<th>LOW SPEED MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>32768Hz OSC: oscillating [REG 104Ch] Bit0 Xtal-Oscillator On</td>
<td>32768Hz OSC: oscillating [REG 104Ch] Bit0 Xtal-Oscillator On</td>
</tr>
<tr>
<td>OSC2: turned on [REG 104Ch] Bit1 System Clock On</td>
<td>OSC2: turned on [REG 104Ch] Bit1 System Clock On</td>
</tr>
<tr>
<td>CPU: sleep mode [REG 104Bh] Bit0 CPU Enter Sleep</td>
<td>CPU: normal mode [REG 104Bh] Bit0 Normal Mode</td>
</tr>
<tr>
<td></td>
<td>CPU Clock Select [REG 104Ch] Bit4 ~2</td>
</tr>
<tr>
<td></td>
<td>Bit4</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Figure 8-4 is the diagram for CPU operation, and Table 8-2 is for CPU Operation Mode Setting. The flow path includes Sleep, Reset, Idle, Power Saving Mode, the flow of CPU Clock between normal and low speed, and setting Register [REG 104Bh, 104Ch]. When CPU Clock is set as low speed, the choice of speed could be made by setting [REG 104Ch] Bit4~2.

### 8.2.2 Wakeup

Table 8-3 shows the setting of Register [REG 104Bh and 104Ch] when CPU needs to be wakening up from the Sleeping, Deep Sleeping, and Power Saving Mode.

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>Sleep Mode</th>
<th>Deep-Sleep Mode</th>
<th>32KHz→ON OSC2→OFF</th>
<th>32KHz→OFF OSC2→OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wakeup &amp; Reset</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PT1 (Rising, Falling)</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PT1 (Level Change)</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>PT2 (Rising, Falling)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PT2 (Level Change)</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>PT3[1:0]~Rising</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PT3[7:4]~Rising</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PT3[3:2]~Falling</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Timer1</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Timer2</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Timer3</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>UART</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>1Min.</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>2Hz</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>1Hz</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Ext_Break</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Note: Yes → Can Wakeup CPU Clock or Reset  
No → Can't Wakeup CPU Clock or Reset

### 8.3 External Flash ROM

RA8917 can support 64K~64MByte external Flash. It can also be connected with two external memories, ranging from 64K~128MByte. Figure 8-5 and 8-6 are the circuits for external Flash ROM. RA8917 can support two Flash ROM at the same time. There are two Command type for Flash. Users can choose a suitable Command type for different brand by setting up [REG 1050h] bit0. [REG 1050~1058h] are the registers for Flash Programming address, Sector address, control indication, and status indication. The steps for Flash Programming and Sector Erase, please refer to the following description.
At the moment, RA8917 mainly supports MXIC Flash ROM series. Besides that, RA8917 provide flexibility for external Flash ROM. Users can use two Flash ROM in the same brand. Figure 8-6 is the circuit for two external 256K-Byte Flash ROM. Which Flash ROM acts depends on [REG 1050h] Bit 2. There are more information below related to relevant Register setting for Flash ROM.

Note: The secondary Flash CE# Pin must be pulled high
### [REG 1050h]: Programming Flash Control Register [PFCR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-6</td>
<td>Not Used.</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>5</td>
<td>Erase Status</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Erase Error</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Erase Success</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Erase Type</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Chip Erase</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Sector Erase</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Programming Status</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Programming Error</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Programming Success</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Flash Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Flash Chip1 (FL_CE# active)</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Flash Chip2 (FL_CE2# active)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>One or Two External Flash Option.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This bit is used to indicate the</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>external Flash number. This bit is</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>read only.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: One External Flash</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Two External Flash</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Flash Type</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Command 1 (Reference 8.3.1)</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>1: Command 2 (Reference 8.3.1)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### [REG 1051h]: Programming Flash FBANK High Byte Register [PFBHR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Bank Data [11:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1052h]: Programming Flash FBANK Low Byte Register [PFBLR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Bank Data [7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1053h]: Programming Flash Address High Byte Register [PFAHR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Programming Flash Address --&gt; A[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1054h]: Programming Flash Address Low Byte Register [PFALR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Programming Flash Address A[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1055h]: Programming Flash Data Register [PFDR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Programming Data</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1056h]: Flash Sector Address High Byte Register [FSAHR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Flash Sector High Byte Address</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1057h]: Flash Sector Address Middle Byte Register [FSAMR]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Flash Sector Middle Byte Address</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
8.3.1 Command Definitions

RA8917 supports two different types of Flash Command Definition, Command 1 and Command 2 as below. Please set Register PFCR[1050h]bit 0 as “0” when the Erase command define is in the format of Command 1. If the Erase command define is in the format of Command 2, please set Register PFCR[1050h]bit 0 as “1”.

### Command 1

<table>
<thead>
<tr>
<th>Command</th>
<th>First Bus Cycle</th>
<th>Second Bus Cycle</th>
<th>Third Bus Cycle</th>
<th>Fourth Bus Cycle</th>
<th>Fifth Bus Cycle</th>
<th>Sixth Bus Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Addr</td>
<td>Data</td>
<td>Addr</td>
<td>Data</td>
<td>Addr</td>
<td>Data</td>
</tr>
<tr>
<td>Erase Byte</td>
<td>5555H</td>
<td>A AH</td>
<td>2AAAH</td>
<td>55H</td>
<td>5555H</td>
<td>80H</td>
</tr>
<tr>
<td>Erase Byte</td>
<td>555H</td>
<td>A AH</td>
<td>AA AH</td>
<td>55H</td>
<td>555H</td>
<td>80H</td>
</tr>
<tr>
<td>Erase Byte</td>
<td>555H</td>
<td>A AH</td>
<td>2AA AH</td>
<td>55H</td>
<td>555H</td>
<td>80H</td>
</tr>
</tbody>
</table>

### Command 2

<table>
<thead>
<tr>
<th>Command</th>
<th>First Bus Cycle</th>
<th>Second Bus Cycle</th>
<th>Third Bus Cycle</th>
<th>Fourth Bus Cycle</th>
<th>Fifth Bus Cycle</th>
<th>Sixth Bus Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Addr</td>
<td>Data</td>
<td>Addr</td>
<td>Data</td>
<td>Addr</td>
<td>Data</td>
</tr>
<tr>
<td>Erase Byte</td>
<td>AAA AH</td>
<td>AAH</td>
<td>5555H</td>
<td>55H</td>
<td>AAA AH</td>
<td>80H</td>
</tr>
<tr>
<td>Erase Byte</td>
<td>AAAH</td>
<td>AAH</td>
<td>555H</td>
<td>55H</td>
<td>AAAH</td>
<td>80H</td>
</tr>
</tbody>
</table>

Let’s take MX29LV161T as an example, describing how to proceed Programming and Erase. The definition of Command is as following. Please refer to the Datasheet of MX29LV161 T/B if you need further information.

### MX29LV161T/B Command Definitions

<table>
<thead>
<tr>
<th>Command</th>
<th>First Bus Cycle</th>
<th>Second Bus Cycle</th>
<th>Third Bus Cycle</th>
<th>Fourth Bus Cycle</th>
<th>Fifth Bus Cycle</th>
<th>Sixth Bus Cycle</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Addr</td>
<td>Data</td>
<td>Addr</td>
<td>Data</td>
<td>Addr</td>
<td>Data</td>
</tr>
</tbody>
</table>

RA8917

8-Bit Micro-Controller

Program | Byte | AAAH | AAH | 55H | 55H | AAAH | A0H | PAH | PDH |
---|---|---|---|---|---|---|---|---|---|
Chip Erase | Byte | AAAH | AAH | 55H | 55H | AAAH | 80H | AAAH | AAH |
| | | 55H | AAAH | 55H | AAAH | 80H | AAAH | AAH |
| Sector Erase | Byte | AAAH | AAH | 55H | 55H | AAAH | 80H | AAAH | AAH |
| | | 55H | AAAH | 55H | AAAH | 80H | AAAH | AAH |

Note:
1. PA= Address of memory location to be programmed
   PD= Data to be programmed at location PA
   SA= Address of the sector to be erased

2. The system should generate the following address patterns: 555H or 2AAH to address A10~A0 in
   word mode /AAAH or 555H to address A10~A-1 in byte mode.
   Address bit A11~A19=X=Don’t care for all address commands except for Program Address(PA) and
   Sector Address(SA). Write sequence may be initiated with A11~A19 in either state.

3. For Sector Protect Verify operation: If read out data is 01H, it means the sector has been protected.
   If read out data is 00H, it means the sector is still not being protected.

8.3.2 Flash Sector Erase

There is an example telling you how to set Registers for Sector Erase to MX29LV161T.

Set [1050h] bit1=0, one external Flash

1. Set Flash Sector Address[1056h, 1057h, 1058h]. Let’s take Sector: SA0 as an example. Please
   refer to the following description and Table 8-4.

<table>
<thead>
<tr>
<th>Sector</th>
<th>Sector Address</th>
<th>Address Range(x16)</th>
<th>Fill Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>A19</td>
<td>A18</td>
<td>A17</td>
<td>A16</td>
</tr>
<tr>
<td>SA0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>SA1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>SA21</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

▲ Take Sector SA0 as an example. How to access data when Address Rang is 000000-00FFFF?
   ➔ Please choose the start Address “000000h” of SA0 Address Range.
   Then choose the left three numbers of “000000”, which is “000”. Because Flash Sector Address
   Register has two bytes (16bit), it must fill in one “0” because the high nibble of [1056h] is not used.
   Then it will become “0000h”, and it is the last fill-in data.

▲ Take Sector SA21 as an example. How to access data when Address Rang is 150000-15FFFF?
   ➔ Please choose the start Address “150000h” of SA21 Address Range.
   Then choose the left three numbers of “150000”, which is “150”. Because Flash Sector Address
   Register has two bytes (16bit), it must fill in one “0” because the high nibble of [1056h] is not used.
   Then it will become “000150h”, and it is the last fill-in data.
For Example: **MX29LV800T/B(x8)**

<table>
<thead>
<tr>
<th>Sector</th>
<th>Sector Address</th>
<th>Address Range(x8)</th>
<th>Fill Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A18 A17 A16 A15 A14 A13 A12</td>
<td>(in hexadecimal)</td>
<td></td>
</tr>
<tr>
<td>SA0</td>
<td>0 0 0 0 0 0 0 X</td>
<td>00000-03FFF</td>
<td>0000h</td>
</tr>
<tr>
<td>SA1</td>
<td>0 0 0 1 0 1 0 0</td>
<td>04000-05FFF</td>
<td>0004h</td>
</tr>
</tbody>
</table>

▲ Take Sector SA1 as an example. How to access data when Address Range is 04000-05FFF?

> Please choose the start Address “04000h” of SA1 Address Range.

Then choose the left two numbers of “04000”, which is “04”. Because Flash Sector Address Register has two bytes (16bit), it must fill in “00” because the high nibble and low nibble of [1056h] is not used. Then it will become “000004h”, and it is the last fill-in data.

Set [1050h] bit0 Flash Type is Command 2 format and [1050h] bit4 Erase Type is Sector Erase.

Call Erase Subroutine which provided by RAiO, Erase Address is 2F10h.

4. Erase Subroutine will set the result at [1050h] bit5 to see whether Erase is successful or not.

**Erase Flash Demo Program:**

```
LDA   #FFh
STA   PT1_DIR
STZ   PT1

LDA   #00001111b
STA   IO_R
LDA   #0000101b
STA   IO_I

LDA   #00h
STA   FSahr
LDA   #00h
STA   FSamr
LDA   #00h
STA   FSalr
LDA   #0010001b
STA   PFCR    ; Sector Erase

JSR   2 F10h
MBBS5 PFCR, EraseSuccess
LDA   #01h
STA   PT1
JMP   $   

EraseSuccess:

LDA   #55h
STA   PT1
JMP   $     
```
8.3.3 Flash Programming

There is an example telling you how to set Registers for Programming to MX29LV161T.
1. Choose to set [1050h] bit1, only one external Flash
2. Set [1050h] bit0 Flash Type is Command 2 format, and [1050h] bit4 Erase Type is Chip Erase
3. Set Flash Bank[1051h, 1052h]; we take Bank 7 as an example
4. Set Programming Flash Address(8000h~BFFFh)
5. Call Programming Flash Subroutine provided by RAiO, Programming Address is 2F00h
6. From [1050h] bit3, it can not only help us know whether Programming is successful or not, but also help us judge whether Programming Address is over BFFFh. If Programming Address writes to C000h, then jump to next Bank.

Programming Flash Demo Program:

Programming_Flash:

LDA   #FFh  
STA   PT1_DIR  
STZ   PT1  
LDA   #0000001b  
STA   PFCR  
LDA   #00  
STA   PFBHR  
LDA   #07  
STA   PFBLR  
LDA   #80h  
STA   PFAHR  
LDA   #00h  
STA   PFALR  
LDA   #66h  
STA   PFDR  

Programming_Loop:

JSR   2F00h  
MBBR3 PFCR, Programming_Error  
INC   PFALR  
BNE   Chk_AddrEnd  
INC   PFALR  

Chk_AddrEnd:

LDA   PFALR  
CMP   #00h  
BNE   Programming_Loop  
LDA   PFAHR  
CMP   #c0h  
BCC   Programming_Loop  
LDA   #55h  
STA   PT1  
JMP   $
Programming_Error:

LDA    #aah
STA    PT1
JMP    $
### Table 8-4: MX29LV161T Sector Architecture

<table>
<thead>
<tr>
<th>Sector</th>
<th>Sector Size</th>
<th>Address range</th>
<th>Sector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Byte Mode</td>
<td>Word Mode</td>
</tr>
<tr>
<td>SA0</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>000000-00FFFF</td>
</tr>
<tr>
<td>SA1</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>010000-01FFFF</td>
</tr>
<tr>
<td>SA2</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>020000-02FFFF</td>
</tr>
<tr>
<td>SA3</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>030000-03FFFF</td>
</tr>
<tr>
<td>SA4</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>040000-04FFFF</td>
</tr>
<tr>
<td>SA5</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>050000-05FFFF</td>
</tr>
<tr>
<td>SA6</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>060000-06FFFF</td>
</tr>
<tr>
<td>SA7</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>070000-07FFFF</td>
</tr>
<tr>
<td>SA8</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>080000-08FFFF</td>
</tr>
<tr>
<td>SA9</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>090000-09FFFF</td>
</tr>
<tr>
<td>SA10</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0A0000-0AFFFF</td>
</tr>
<tr>
<td>SA11</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0B0000-0BFFFF</td>
</tr>
<tr>
<td>SA12</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0C0000-CFFFFF</td>
</tr>
<tr>
<td>SA13</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0D0000-0DFFFF</td>
</tr>
<tr>
<td>SA14</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0E0000-0EFFFF</td>
</tr>
<tr>
<td>SA15</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0F0000-0FFFFF</td>
</tr>
<tr>
<td>SA16</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>100000-10FFFF</td>
</tr>
<tr>
<td>SA17</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>110000-11FFFF</td>
</tr>
<tr>
<td>SA18</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>120000-12FFFF</td>
</tr>
<tr>
<td>SA19</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>130000-13FFFF</td>
</tr>
<tr>
<td>SA20</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>140000-14FFFF</td>
</tr>
<tr>
<td>SA21</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>150000-15FFFF</td>
</tr>
<tr>
<td>SA22</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>160000-16FFFF</td>
</tr>
<tr>
<td>SA23</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>170000-17FFFF</td>
</tr>
<tr>
<td>SA24</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>180000-18FFFF</td>
</tr>
<tr>
<td>SA25</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>190000-19FFFF</td>
</tr>
<tr>
<td>SA26</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>1A0000-AFFFFF</td>
</tr>
<tr>
<td>SA27</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>1B0000-1BFFFFF</td>
</tr>
<tr>
<td>SA28</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>1C0000-1CFFFFF</td>
</tr>
<tr>
<td>SA29</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>1D0000-1DFFFFF</td>
</tr>
<tr>
<td>SA30</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>1E0000-1EFFFFF</td>
</tr>
<tr>
<td>SA31</td>
<td>32Kbytes</td>
<td>16Kwords</td>
<td>1F0000-1FFFFFF</td>
</tr>
<tr>
<td>SA32</td>
<td>8Kbytes</td>
<td>4Kwords</td>
<td>1F8000-1F8FFFFF</td>
</tr>
<tr>
<td>SA33</td>
<td>8Kbytes</td>
<td>4Kwords</td>
<td>1FA000-1FBFFFFF</td>
</tr>
<tr>
<td>SA34</td>
<td>16Kbytes</td>
<td>8Kwords</td>
<td>1FC000-1FFFFFFF</td>
</tr>
</tbody>
</table>
Table 8-5: MX29LV161B Sector Architecture

<table>
<thead>
<tr>
<th>Sector</th>
<th>Sector Size</th>
<th>Address range</th>
<th>Sector Address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Byte Mode</td>
<td>Word Mode</td>
<td></td>
</tr>
<tr>
<td>SA0</td>
<td>16Kbytes</td>
<td>8Kwords</td>
<td>000000-003FFF</td>
</tr>
<tr>
<td>SA1</td>
<td>8Kbytes</td>
<td>4Kwords</td>
<td>004000-005FFF</td>
</tr>
<tr>
<td>SA2</td>
<td>8Kbytes</td>
<td>4Kwords</td>
<td>006000-007FFF</td>
</tr>
<tr>
<td>SA3</td>
<td>32Kbytes</td>
<td>16Kwords</td>
<td>008000-00FFFF</td>
</tr>
<tr>
<td>SA4</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>010000-01FFFF</td>
</tr>
<tr>
<td>SA5</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>020000-02FFFF</td>
</tr>
<tr>
<td>SA6</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>030000-03FFFF</td>
</tr>
<tr>
<td>SA7</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>040000-04FFFF</td>
</tr>
<tr>
<td>SA8</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>050000-05FFFF</td>
</tr>
<tr>
<td>SA9</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>060000-06FFFF</td>
</tr>
<tr>
<td>SA10</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>070000-07FFFF</td>
</tr>
<tr>
<td>SA11</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>080000-08FFFF</td>
</tr>
<tr>
<td>SA12</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>090000-09FFFF</td>
</tr>
<tr>
<td>SA13</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0A0000-0AFFFF</td>
</tr>
<tr>
<td>SA14</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0B0000-0BFFFF</td>
</tr>
<tr>
<td>SA15</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0C0000-0CFFFF</td>
</tr>
<tr>
<td>SA16</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0D0000-0DFFFF</td>
</tr>
<tr>
<td>SA17</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0E0000-0EFFFF</td>
</tr>
<tr>
<td>SA18</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>0F0000-0FFFFF</td>
</tr>
<tr>
<td>SA19</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>100000-10FFFF</td>
</tr>
<tr>
<td>SA20</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>110000-11FFFF</td>
</tr>
<tr>
<td>SA21</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>120000-12FFFF</td>
</tr>
<tr>
<td>SA22</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>130000-13FFFF</td>
</tr>
<tr>
<td>SA23</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>140000-14FFFF</td>
</tr>
<tr>
<td>SA24</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>150000-15FFFF</td>
</tr>
<tr>
<td>SA25</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>160000-16FFFF</td>
</tr>
<tr>
<td>SA26</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>170000-17FFFF</td>
</tr>
<tr>
<td>SA27</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>180000-18FFFF</td>
</tr>
<tr>
<td>SA28</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>190000-19FFFF</td>
</tr>
<tr>
<td>SA29</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>1A0000-1AFFFF</td>
</tr>
<tr>
<td>SA30</td>
<td>64Kbytes</td>
<td>32Kwords</td>
<td>1B0000-1BFFFF</td>
</tr>
<tr>
<td>SA31</td>
<td>32Kbytes</td>
<td>16Kwords</td>
<td>1C0000-1CFFFF</td>
</tr>
<tr>
<td>SA32</td>
<td>8Kbytes</td>
<td>4Kwords</td>
<td>1D0000-1DFFFF</td>
</tr>
<tr>
<td>SA33</td>
<td>8Kbytes</td>
<td>4Kwords</td>
<td>1E0000-1EFFFF</td>
</tr>
<tr>
<td>SA34</td>
<td>16Kbytes</td>
<td>8Kwords</td>
<td>1F0000-1FFFFF</td>
</tr>
</tbody>
</table>
8.4 I/O Ports

The RA8917 has four 8-bit bi-direction I/O Port. The specialties of RA8917 are I/O resistor control register and I/O driving current control register, which provide the convenience for users to make a choice depend on the application. RA8917 also builds in De-bounce function, and could be set by [REG 102Dh] Bit7~Bit4.

### [REG 1020h]: Port 1 Data Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2</td>
<td>Bit-[7:2] of Output Data to Port 1 or Input from Port 1</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
| 1   | Bit-1 of Output Data to Port 1 or Input from Port 1  
This bit is also as the input of TM2 clock source when REG-1015h bit2-0 == '000' | 0h | 0h | R/W |
| 0   | Bit-0 of Output Data to Port 1 or Input from Port 1  
This bit is also as the input of TM1 clock source when REG-1012h bit2-0 == '000' | 0h | 0h | R/W |

Note: If the Port1 is output mode then the read access data is from the register 1020h. If the Port1 is input mode the read access is form Port1 I/O.

### [REG 1021h]: Port 1 Direction Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
| 7-0 | Select the Output or Input Mode of Port 1  
0: Input Mode  
1: Output Mode | 0h | 0h | R/W |

### [REG 1022h]: Port1 Interrupt Indicate Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Port1 Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1023h]: Port 1 Output Mode Select Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
| 7-0 | Select the Output Mode for CMOS or Open-Drain Mode  
0: CMOS Mode  
1: Open-Drain Mode. In this mode, Port 1 Direction Control Register controls the Port1 output data. | 0h | 0h | R/W |

### [REG 1024h]: Port 2 Data Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
| 7   | Bit-7 of Output Data to Port 2 or Input from Port 2  
This bit is also as the output of PWM1 when PWM enable (REG-101Dh bit4 = ‘1’). | 0h | 0h | R/W |
| 6   | Bit-6 of Output Data to Port 2 or Input from Port 2  
This bit is also as the output of PWM2 when PWM enable (REG-101Dh bit4 = ‘1’). | 0h | 0h | R/W |
| 5   | Bit-5 of Output Data to Port 2 or Input from Port 2  
This bit is also as the output of REG-101Eh write signal (EXP_WR#) when external REG-101Eh write enabled (REG-101Fh bit0= ‘1’). | 0h | 0h | R/W |
| 4   | Bit-4 of Output Data to Port 2 or Input from Port 2  
This bit is also as the secondary external Flash chip select output(FL_CE2#) when using two external flashes. | 0h | 0h | R/W |
| 3   | Bit-3 of Output Data to Port 2 or Input from Port 2  
This bit is also as the output of LVD indicated (LVD#) when external LVD enabled (REG-1033h bit2= ‘1’). | 0h | 0h | R/W |
Bit-2 of Output Data to Port 2 or Input from Port 2
This bit is also as the external memory write enable (MEM_WE#) when external memory decoder selected (REG-1032h bit0= ‘1’).

Bit-1 of Output Data to Port 2 or Input from Port 2
This bit is also as the external memory output enable (MEM_OE#) when external memory decoder selected (REG-1032h bit0= ‘1’).

Bit-0 of Output Data to Port 2 or Input from Port 2
This bit is also as the external memory chip select output (MEM_CE#) when external memory decoder enabled (REG-1032h bit0= ‘1’). The external memory is decoded when CPU access from $4000 to $7FFF.

Note: If the Port2 is output mode then the read access date is from the register 1024h. If the Port2 is input mode then the read access is form Port2 I/O.

[REG 1025h]: Port 2 Direction Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Select the Output or Input Mode of Port 2</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Input Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Output Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 1026h]: Port2 Interrupt Indicate Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Port2 Bit[7:0]</td>
</tr>
</tbody>
</table>

[REG 1027h]: Port 2 Output Mode Select Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Select the Output Mode for CMOS or Open-Drain Mode</td>
</tr>
<tr>
<td></td>
<td>0: CMOS Mode</td>
</tr>
<tr>
<td></td>
<td>1: Open-Drain Mode. In this mode, Port 2 Direction Control Register controls the Port1 output data.</td>
</tr>
</tbody>
</table>

[REG 1028h]: Port 3 Data Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Bit-[7:4] of Output Data to Port 3 or Input from Port 3.</td>
</tr>
<tr>
<td>3</td>
<td>Bit-3 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of User UART TX when user UART enable (REG-1038h bit4 == ‘1’).</td>
</tr>
<tr>
<td>2</td>
<td>Bit-2 of Output Data to Port 3 or Input from Port 3. This bit is also as the input of User UART RX when user UART enable (REG-1038h bit4 == ‘1’).</td>
</tr>
<tr>
<td>1</td>
<td>Bit-1 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of external LCD chip select(LCD_E) when external LCD enabled(REG-100Dh bit0= ‘1’). The external LCD is decoded at REG-100Eh &amp; REG-100Fh.</td>
</tr>
<tr>
<td>0</td>
<td>Bit-0 of Output Data to Port 3 or Input from Port 3. This bit is also as the output of external LCD R/W(LCD_RW) when external LCD enabled(REG-100Dh bit0= ‘1’).</td>
</tr>
</tbody>
</table>

Note: If the Port3 is output mode then the read access date is from the register 1028h. If the Port3 is input mode then the read access is form Port3 I/O.

[REG 1029h]: Port 3 Direction Control Register
### Bit Description

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Select the Output or Input Mode of Port 3</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Input Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Output Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**[REG 102Ah]: Port3 Interrupt Indicate Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Port3 Bit[7:0] Interrupt Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 102Bh]: I/O Resistor Control Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT4 High Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PT4 Low Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PT3 High Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PT3 Low Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PT2 High Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>PT2 Low Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>PT1 High Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>PT1 Low Nibble Resistor Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Pull Up: 50Kohm</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**[REG 102Ch]: I/O Driving Current Control Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT4 High Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PT4 Low Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PT3 High Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PT3 Low Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PT2 High Nibble Current Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 4mA (24mA for PT2_6, PT2_7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 8mA (36mA for PT2_6, PT2_7)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### PT2 Low Nibble Current Select
- 0: 4mA
- 1: 8mA

### PT1 High Nibble Current Select
- 0: 4mA
- 1: 8mA

### PT1 Low Nibble Current Select
- 0: 4mA
- 1: 8mA

---

**[REG 102Dh]: I/O Interrupt Control Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT2 High Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PT2 Low Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PT1 High Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PT1 Low Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PT2 High Nibble Interrupt or Wakeup</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>PT2 Low Nibble Interrupt or Wakeup</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>PT1 High Nibble Interrupt or Wakeup</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>PT1 Low Nibble Interrupt or Wakeup</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**[REG 102Eh]: I/O Interrupt/Wakeup Mode Select Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT2 High Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PT2 Low Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PT1 High Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PT1 Low Nibble Clock Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Add Filter to De-bounce</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**RA8917**

8-Bit Micro-Controller
### RA8917 8-Bit Micro-Controller

#### PT2 High Nibble Mode Select

<table>
<thead>
<tr>
<th>Bit7</th>
<th>Bit6</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Rising-Edge Trigger</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Falling-Edge Trigger</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Level Change Trigger (1)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Level Change Trigger (2)</td>
</tr>
</tbody>
</table>

**Level Change Trigger (1):**

(1111) → Setup
(1111) → (1111) → (1110) Trigger → (1010) → (0000) →
(1111) Return → (1011) Trigger

**Level Change Trigger (2):**

(1111) → Setup
(1111) → (1111) → (1110) Trigger → (1010) Trigger →
(1010) → (1011) Trigger → (1111) Trigger

#### PT2 Low Nibble Mode Select

<table>
<thead>
<tr>
<th>Bit5</th>
<th>Bit4</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Rising-Edge Trigger</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Falling-Edge Trigger</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Level Change Trigger (1)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Level Change Trigger (2)</td>
</tr>
</tbody>
</table>

#### PT1 High Nibble Mode Select

<table>
<thead>
<tr>
<th>Bit3</th>
<th>Bit2</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Rising-Edge Trigger</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Falling-Edge Trigger</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Level Change Trigger (1)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Level Change Trigger (2)</td>
</tr>
</tbody>
</table>

#### PT1 Low Nibble Mode Select

<table>
<thead>
<tr>
<th>Bit1</th>
<th>Bit0</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Rising-Edge Trigger</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Falling-Edge Trigger</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Level Change Trigger (1)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Level Change Trigger (2)</td>
</tr>
</tbody>
</table>

[REG 102Fh]: I/O Wakeup Reset Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PT3 High Nibble Interrupt or Wakeup</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Note: PT3[7:4] are Rising-Edge Trigger.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PT3 Low Nibble Interrupt or Wakeup</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Note: PT3[1:0] are Rising-Edge Trigger, PT3[3:2] are Falling-Edge Trigger.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PT3 High Nibble Wakeup Reset</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Wakeup CPU Only</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Wakeup &amp; Cause Reset</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PT3 Low Nibble Wakeup Reset</td>
<td>PT2 High Nibble Wakeup Reset</td>
<td>PT2 Low Nibble Wakeup Reset</td>
<td>PT1 High Nibble Wakeup Reset</td>
</tr>
<tr>
<td>---</td>
<td>----------------------------</td>
<td>----------------------------</td>
<td>----------------------------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>4</td>
<td>0: Wakeup CPU Only</td>
<td>0: Wakeup CPU Only</td>
<td>0: Wakeup CPU Only</td>
<td>0: Wakeup CPU Only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>0h</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**Example(1):** Each set-up while PT1 is in Output Mode.

```
LDA  #11111111b     ; PT1 Output Mode
STA  1021h
LDA  #00000000b     ; PT1 Resistor None
STA  102Bh
LDA  #00000000b     ; PT1 Driving Current = 4mA
STA  102Ch
LDA  #10101010b     ; PT1 Output Mode
STA  1020h
```

**Example(2):** Each set-up while PT1 is in Output and Input Mode.

```
LDA  #1110000b      ; PT2 Bit7~4 Output, Bit3~0 Input
STA  1025h
LDA  #0000100b      ; PT2 High Nibble Resistor: None
STA  102Bh
LDA  #01000000b     ; PT2 Low Nibble Resistor: Pull Up 5Kohm
STA  102Dh
LDA  #1100000b      ; PT2 Low Nibble Clock Select: Add Filter to De-bounce, High Nibble Normal.
STA  1024h
```

**Example(3):** Each set-up while PT1 is used for INT.

```
LDA  #00000000b     ; PT1 Input Mode
STA  1021h
LDA  #00110011b     ; PT1 add filter to de-bounce.
STA  102Dh
LDA  #00000101b     ; PT1 Interrupt or Wakeup Enable
STA  102Eh
LDA  #0000001b      ; PT1 INT Enable
STA  1006h
```

**Example(4):** Each set-up while PT1 is used for Wake-up Reset.

```
LDA  #00000000b     ; PT1 Input Mode
```
8.5 Timer

RA8917 provides three 12-Bit Timer/Counter. They are Timer1, Timer2, and Timer3, composed of two 8-bit Registers (THx, TLx). The functions of Timer1 and Timer2 are as following:

12 Bits counter auto re-load.
Down Counter type
Wake up from Sleep Mode
Wake up RESET
Overflow Interrupt Once or Loop

The functions of Timer3:

12 Bits counter auto re-load.
Down Counter type
Overflow Interrupt Once or Loop

Figures below are Block Diagrams illustrating operation principles and software control methods.

Figure 8-7 Timer1 Block Diagram
Figure 8-8 Timer2 Block Diagram

Figure 8-9 Timer3 Block Diagram
Figure 8-10 Timer Operation mode

[REG 1010h]: Timer 1 Count_H Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-0</td>
<td>Timer 1 Down Count Data – High Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1011h]: Timer 1 Count_L Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Timer 1 Down Count Data – Low Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1012h]: Timer 1 Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Timer 1 Enable or Timer 1 Start</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable/Stop</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable/Start</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Timer 1 wakeup enable from sleep mode.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Timer 1 wakeup RESET enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Timer 1 Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Timer 1 Input Clock Source Select

<table>
<thead>
<tr>
<th>Bit2</th>
<th>Bit1</th>
<th>Bit0</th>
<th>Clock Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>External I/O Port (PT1_0)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK /2^16</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>USR_DIV_CLK /2^14</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>USR_DIV_CLK /2^10</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>USR_DIV_CLK /2^6</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK /2^2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>32768Hz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>GND</td>
</tr>
</tbody>
</table>

**[REG 1013h]:** Timer 2 Count_H Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-0</td>
<td>Timer 2 Down Count Data – High Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1014h]:** Timer 2 Count_L Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Timer 2 Down Count Data – Low Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

**[REG 1015h]:** Timer 2 Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Timer 2 Enable or Timer 2 Start</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable/Stop</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable/Start</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Timer 2 wakeup enable from sleep mode.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Timer 2 wakeup RESET enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Timer 2 Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-0</td>
<td>Timer 2 Input Clock Source Select</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Timer 3 Count_H Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-0</td>
<td>Timer 3 Down Count Data – High Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### Timer 3 Count_L Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Timer 3 Down Count Data – Low Byte</td>
<td>Xh</td>
<td>Xh</td>
<td>R/W</td>
</tr>
</tbody>
</table>
### [REG 1018h]: Timer 3 Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Timer 3 Enable or Timer 3 Start</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable/Stop</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable/Start</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Timer 3 Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Bit 2-0: Timer 3 Input Clock Source Select

<table>
<thead>
<tr>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Clock Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>USR_DIV_CLK/2^16</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK/2^14</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>USR_DIV_CLK/2^10</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>USR_DIV_CLK/2^6</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>USR_DIV_CLK/2^2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>USR_DIV_CLK/2^1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>USR_DIV_CLK</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>32768Hz</td>
</tr>
</tbody>
</table>

#### Example:

Use Timer1 to produce interruption every 8KHz.

1/8KHz=125µs, USR_DIV_CLK=7.3728MHz, Timer1 Clock=USR_DIV_CLK/4=7.3728MHz/4

\[
\text{TH1}=00h, \text{TL1}=125\mu s \times \left( \frac{1}{\left( \frac{7.3728\text{MHz}}{4} \right)} \right) = 230, \text{TL1}=E6h
\]

- CLI ; Enable all Interrupt
- LDA #00000000b ; USR_DIV_CLK =7.3728MHz
- STA 104Ch
- LDA #00010000b ; Timer1 INT Enable
- STA 1006h
- LDA #00h
- STA 1010h
- LDA #e6h
- STA 1011h
- LDA #10001101b ; Timer1 start, Loop Enable, Clock=USR_DIV_CLK/4
- STA 1012h

### 8.6 Watch Dog

The counting period of Watch Dog timer is 2 second. Watch Dog will automatically RESET when it counts up to 2 second preventing the crash happens within the IC. If users need this function, then users need to clear Watch Dog with in 2 second. The Watch Dog could be used as general Timer, and has the function of NMI Interrupt. Figure 8-11 is the Block Diagram of the Watch Dog.
Figure 8-11 Watch Dog Block Diagram

[REG 104Bh]: Power Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Extra Sleep Mode (Only at RTC Mode)</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Normal Sleep</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Extra Deep Sleep</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>In this mode, the Divisor is off and only 32768Hz X'tal, Low speed Timer circuit are active. But the Wakeup with Reset function is inhibited. This bit must used to go with bit-1 and bit-0. Only available when REG[104Bh] Bit[1:0] = 11b.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 104Ch]: Clock Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-5</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4-2</td>
<td>CPU Clock Select</td>
<td>000h</td>
<td>000h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Bit4  Bit3  Bit2  CPU Clock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>x  x  OSC2_CLK</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0  0  OSC2_CLK /2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0  1  OSC2_CLK /4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1  x  OSC2_CLK /8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>System X'tal Clock (OSC2) On/Off Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: System X'tal Clock On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: System X'tal Clock Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>32768Hz X'tal-Oscillator On/Off Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: 32768Hz X'tal-Oscillator On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: 32768Hz X'tal-Oscillator Off</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 100Ch]: Watch Dog Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Watch Dog Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Watch Dog Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Watch Dog Timer Clear</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Reset Watch Dog Timer, Write this bit high will cause Watch Dog Timer Reset. This bit will be clear automatically after clear.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Watch Dog Reset Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA  #00111110b    ; USR_DIV_CLK=32768Hz
STA  104Ch

LDA  #00001001b    ; Watch Dog Enable, Reset Enable
STA  100Ch

LDA  100Ch
AND  #11110111bh
STA  100Ch
```

8.7 Interrupt

RA8917 provides 10 Non Mask Interrupt (NMI) and 14 INT. Figure 8-12 is NMI Block Diagram, and Figure 8-13 is INT Block Diagram. Below is relevant Register [REG 1000h~100Bh, 1022h, 1026h, 102A] of Interrupt. RA8917 supports many interrupt sources in INT/NMI. Please refer to Table 8-6. RA8917 also provide interrupt priority, which let users set by themselves. Please refer to the Table 8-6 for Interrupt vector address.
Figure 8-12 NMI Block Diagram
Figure 8-13 INT Block Diagram
### INT Priority

Table 8-6: INT / NMI Interrupt Priority

<table>
<thead>
<tr>
<th>Interrupt Priority</th>
<th>Interrupt Source</th>
<th>Interrupt Vector</th>
</tr>
</thead>
<tbody>
<tr>
<td>NP0 (NMI)</td>
<td>Watch Dog Timer</td>
<td>FFEE~FFEF</td>
</tr>
<tr>
<td>NP1 (NMI)</td>
<td>Port1</td>
<td>FFEC~FFED</td>
</tr>
<tr>
<td>NP2 (NMI)</td>
<td>Timer1</td>
<td>FFEA~FFEB</td>
</tr>
<tr>
<td>NP3 (NMI)</td>
<td>Port2</td>
<td>FFE8~FFE9</td>
</tr>
<tr>
<td>NP4 (NMI)</td>
<td>Timer2</td>
<td>FFE6~FFE7</td>
</tr>
<tr>
<td>NP5 (NMI)</td>
<td>Port3</td>
<td>FFE4~FFE5</td>
</tr>
<tr>
<td>NP6 (NMI)</td>
<td>Timer3</td>
<td>FFE2~FFE3</td>
</tr>
<tr>
<td>NP7 (NMI)</td>
<td>Low Speed Timer</td>
<td>FFE0~FFE1</td>
</tr>
<tr>
<td>IP0 (INT)</td>
<td>UART</td>
<td>FFCE~FFCF</td>
</tr>
<tr>
<td>IP1 (INT)</td>
<td>Port1</td>
<td>FFCC~FFCD</td>
</tr>
<tr>
<td>IP2 (INT)</td>
<td>Timer1</td>
<td>FFCA~FFCB</td>
</tr>
<tr>
<td>IP3 (INT)</td>
<td>Port2</td>
<td>FFC8~FFC9</td>
</tr>
<tr>
<td>IP4 (INT)</td>
<td>Timer2</td>
<td>FFC6~FFC7</td>
</tr>
<tr>
<td>IP5 (INT)</td>
<td>Port3</td>
<td>FFC4~FFC5</td>
</tr>
<tr>
<td>IP6 (INT)</td>
<td>Timer3</td>
<td>FFC2~FFC3</td>
</tr>
<tr>
<td>IP7 (INT)</td>
<td>User UART</td>
<td>FFC0~FFC1</td>
</tr>
<tr>
<td>IP8 (INT)</td>
<td>Low Speed Timer</td>
<td>FFBE~FFBF</td>
</tr>
<tr>
<td>IP9 (INT)</td>
<td>ADC</td>
<td>FFBC~FFBD</td>
</tr>
<tr>
<td>IP10 (INT)</td>
<td>Timer Base</td>
<td>FFBA~FFBB</td>
</tr>
</tbody>
</table>

Interrupt Priority:

NP0 > NP1 > NP2 > NP3 > NP4 > NP5 > NP6 > NP7 > IP0 > IP1 > IP2 > IP3 > IP4 > IP5 > IP6
> IP7 > IP8 > IP9 > IP10

[REG 1000h]: NMI Mask Register (1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Timer 3 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Timer 2 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Timer 1 NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Watch Dog NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### RA8917

#### 8-Bit Micro-Controller

**Version 1.6**

---

**Port 3 NMI Enable**
- 0: Disable
- 1: Enable
  - **Address:** 0h 0h
  - **Access:** R/W

**Port 2 NMI Enable**
- 0: Disable
- 1: Enable
  - **Address:** 0h 0h
  - **Access:** R/W

**Port 1 NMI Enable**
- 0: Disable
- 1: Enable
  - **Address:** 0h 0h
  - **Access:** R/W

---

**[REG 1001h]: NMI Mask Register (2)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1Min. NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1HZ NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>2HZ NMI Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**[REG 1002h]: NMI Status Register (1)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Timer 3 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>Timer 2 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>Timer 1 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>Watch Dog NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>Port 3 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Port 2 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>Port 1 NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

---

**[REG 1003h]: NMI Status Register (2)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1Min. NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>1HZ NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>2HZ NMI Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

---

**[REG 1004h]: Clear NMI Status Register (1)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Clear Timer 3 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Clear Timer 2 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Clear Timer 1 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Clear Watch Dog NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Clear Port 3 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Clear Port 2 NMI Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>1: Clear</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### [REG 1005h]: Clear NMI Status Register (2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Clear Port 1 NMI Indicate 1: Clear</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>1</td>
<td>Clear 1Min. NMI Indicate 1: Clear</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>2</td>
<td>Clear 1HZ NMI Indicate 1: Clear</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>3</td>
<td>Clear 2HZ NMI Indicate 1: Clear</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
</tbody>
</table>

### [REG 1006h]: INT Mask Register (1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Port 1 INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Port 2 INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>Port 3 INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>Timer 1 INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>Timer 2 INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>Timer 3 INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1007h]: INT Mask Register (2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2HZ INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>1HZ INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>1Min. INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>3</td>
<td>64HZ Time Base INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>512HZ Time Base INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>2048HZ Time Base INT Enable 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 1008h]: INT Status Register (1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Timer 1 INT Indicate 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>Timer 2 INT Indicate 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>Timer 3 INT Indicate 0: Disable 1: Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
### [REG 1009h]: INT Status Register (2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>2048HZ Time Base INT Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>5</td>
<td>512HZ Time Base INT Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>4</td>
<td>64HZ Time Base INT Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>1Min. INT Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>1</td>
<td>1HZ INT Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>2HZ INT Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 100Ah]: Clear INT Status Register (1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Clear Timer 3 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>5</td>
<td>Clear Timer 2 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>4</td>
<td>Clear Timer 1 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>2</td>
<td>Clear Port 3 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>1</td>
<td>Clear Port 2 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>0</td>
<td>Clear Port 1 INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
</tbody>
</table>

### [REG 100Bh]: Clear INT Status Register (2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>Clear 2048HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>5</td>
<td>Clear 512HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>4</td>
<td>Clear 64HZ Time Base INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>2</td>
<td>Clear 1Min. INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>1</td>
<td>Clear 1HZ INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
<tr>
<td>0</td>
<td>Clear 2HZ INT Indicate</td>
<td>--</td>
<td>--</td>
<td>W</td>
</tr>
</tbody>
</table>

### [REG 1038h]: User UART Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Transmit Empty Indicate INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>6</td>
<td>Received Data Available Indicate INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>
[REG 1068h]: Vector Control Register [VEC_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>NMI Vector Enable Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>INT Vector Enable Control</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5-0</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1069h]: Non-Mask Interrupt Priority Register 1 [NMI_PRI1]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority NP[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 106Ah]: Non-Mask Interrupt Priority Register 2 [NMI_PRI2]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority NP[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 106Bh]: Interrupt Priority Register 1 [INT_PRI1]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority IP[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[REG 106Ch]: Interrupt Priority Register 2 [INT_PRI2]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Non-Mask Interrupt Priority IP[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Note: Please reference the Table 8-6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8.8 Universal Synchronous Asynchronous Receiver Transmitter (UART)

RA8917 builds in one set UART. [REG 1035h] which includes Receive and Transmit can do read and write. Figure 8-14 is Baud Rate Clock Block Diagram. The transmission format of UART is as Figure 8-15. Besides that, UART provides three types of transmission models, such as Normal, ASK IR, IrDA IR. When CPU is during Sleep Mode, UART could be a source for Wake Up. The relevant Register [REG 1037h~1039h] for UART is as below.

![Figure 8-14 Baud Rate Clock Block Diagram](image)
### Figure 8-15 RX & TX Data Format

#### [REG 1035h]: User UART Receive Register (Read Only)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>UART Receive Data</td>
<td>Xh</td>
<td>Xh</td>
<td>R</td>
</tr>
</tbody>
</table>

#### [REG 1035h]: User UART Transmit Register (Write Only)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>UART Transmit Data</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
</tbody>
</table>

#### [REG 1036h]: IR Mode Select

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-0</td>
<td>UART IR Mode Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Bit1 Bit0 Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1 ASK IR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 0 IrDA IR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 IrDA IR</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### [REG 1037h]: User UART Baud Rate Select

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-0</td>
<td>UART Baud Rate</td>
<td>01h</td>
<td>01h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>Bit1 Bit0 Baud Rate</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 115200bps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1 57600bps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 0 38400bps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 28800bps</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### [REG 1038h]: User UART Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Transmit Empty Indicate INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Received Data Available Indicate INT Enable</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
User UART Enable Control
0: Disable, 1.843MHz Clock Stop
1: Enable
If set high, then the Port3 bit[3:2] are defined as Transmit and
Receive interface signals.
PT3_3 ➔ TX
PT3_2 ➔ RX

UART Transmitter Inverter
0: Disable
1: Enable

UART Receiver Inverter
0: Disable
1: Enable

UART RX Wake Up Mode Select
0: UART Wake Up only
1: UART Wake Up & caused Reset

UART RX Wake Up
0: Disable
1: Enable

[REG 1039h]: User UART Status Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Transmit Register Empty Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is set when transmit complete and be clear when write a data to</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>UART Transmit Register (REG-1035h).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Received Data Available Indicate</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>This bit is set when UART received an available data but it will not be</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>clear when the host read the data from UART Receive Register (REG-1035h).</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

LDA  #00h ; UART IR Mode ➔ Normal
STA  1036h

LDA  #00h ; Baud Rate=115200 bps
STA  1037h

LDA  #00010000b ; UART Enable
STA  1038h

LDA  #55h
STA  1035h ; Transmit 55h
LDA  1035h ; Receive
8.9 IrDA Interface

An IrDA interface, compatible with SIR(Serial Infrared) level IrDA, is built in RA8917. The IrDA encoder and decoder module is built on the fundamental of UART module. RA8917 and external IrDA module, connecting via RX(receiver, pin37) and TX(transmitter Pin38), complete the implementation of IrDA physical layer.

![Figure 8-16 RA8917 with IrDA module](image)

8.10 Digital-to-Analog Converter (D/A) Module

RA8917 Support one 4 level 10-bit fixed current types Digital-to-Analog Converter (D/A) Module. RA8917 current output IOUt is divided to two types and three current levels: Audio Mode (0~2mA, 0~2.5mA and 0~3mA) and DTMF Mode (0~200uA, 0~200uA and 0~200uA), which could be set by [REG 101Bh]. The maximum output current is 3mA as well as the data is “FF”. If the data is “00” then the output current is zero. Figure 8-17 is DAC application circuit.

![Figure 8-17 DAC Application](image)
8.11 LCD Interface

RA8917 supports a LCD Interface, including two LCD Registers, which are LCD Command register [REG 100Eh] and LCD Data register [REG 100Fh]. The external control signal saves the effort of some simulation actions. Figure 8-19 shows the interface of RA8917 and LCD/LCM. The relevant Register [REG 100Dh, 100Eh, 100Fh] for LCD Interface is one the following page. There is an example to illustrate how to control LCD.
Figure 8-20 Command Write Timing

<table>
<thead>
<tr>
<th>Addr</th>
<th>Data</th>
<th>R/W</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>100Eh</td>
<td>55H</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 8-21 Command Read Timing

<table>
<thead>
<tr>
<th>Addr</th>
<th>Data</th>
<th>R/W</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>100Fh</td>
<td>55H</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 8-22 Data Write Timing

<table>
<thead>
<tr>
<th>Addr</th>
<th>Data</th>
<th>R/W</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>100Fh</td>
<td>55H</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Figure 8-23 Data Read Timing

### [REG 100Dh]: LCD Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-1</td>
<td>Hi-Speed Control for External LCD Decoder&lt;br&gt;These two bits are used to add delay clock for LCD access time.</td>
<td></td>
<td></td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>Bit2 Bit1 T1 T2 T3 (Unit: CPU Clock)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0 0 : 4.5 11 0.5</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0</td>
<td>1 0 : 3.5 9 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0 1 : 2.5 6 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1 1 : 1.5 3 0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>T1: Data Set-Up Time&lt;br&gt;T2: Data Access Time&lt;br&gt;T3: Data Hold Time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>External LCD Driver Control. This bit is used to control the external LCD Driver interface enable or disable. &lt;br&gt;0: Disable&lt;br&gt;1: Enable&lt;br&gt;If set high, then the Port3 bit[1:0] are defined as LCD Driver interface signals. PT3_1 -&gt; LCD_E&lt;br&gt;PT3_0 -&gt; LCD_RW</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 100Eh]: LCD Command Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>This register is used for external LCD controller.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### [REG 100Fh]: LCD Data Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>This register is used for external LCD controller.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Example:

LDA #00000100b ; External LCD Driver Control Enable
STA 100Dh
LDA #01h ; Command Write, to clear LCD screen.
STA 100Eh
LDA 100Eh ; Command Read, to determine LCD busy flag.
LDA #41h ; Data Write, write “A” into LCD screen.
STA 100Fh
LDA 100Fh ; Data Read, read data into ACC from LCD module

8.12 PWM

When the bit4 of [REG 101Dh] is set to high, then the PWM mode is enable. The duty cycle of PWM output is controlled by [REG 101Ch] bit7~0. The Timer Base of PWM could be set by the Clock Source of Timer3 [REG 1018h] Bit2~0. The set-up of TM3_L is related to PWM Resolution. The optimized Value for TM3_L is as following table.

<table>
<thead>
<tr>
<th>PWM Resolution</th>
<th>TM3_L Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 bit</td>
<td>FFh</td>
</tr>
<tr>
<td>7 bit</td>
<td>7Fh</td>
</tr>
<tr>
<td>6 bit</td>
<td>3Fh</td>
</tr>
<tr>
<td>5 bit</td>
<td>1Fh</td>
</tr>
</tbody>
</table>

Example:

LDA #18h
STA 101Dh ; Set PWM Enable.
LDA #FFh
STA 101Ch ; producing 50% Duty Cycle’s PWM Pulse

; 8 bit resolution, PWM1&PWM2 Enable

![Figure 8-24 PWM Application](image-url)
The formula of PWM Clock and PWM Duty Cycle of Single Mode 50% or 100% Duty are as following:

1. PWM Clock (Unit: Time):

\[ T = \frac{1}{\text{PWM_CLK}} = \frac{(\text{TM3_H}+1) \times (\text{TM3_L}+1)}{\text{TM3_CLK\_Source}} \]

2. PWM Duty Cycle:

\[ \text{PWM\_Duty} = \frac{W}{T} = \frac{(\text{PWM\_Data}+1)}{(\text{TM3\_L}+1)} \]

\[ W = \frac{[(\text{TM3\_H}+1) \times (\text{PWM\_Data}+1)]}{\text{TM3\_CLK\_Source}} \]
The formula of PWM Clock and PWM Duty Cycle of Differential Mode 50% Duty are as following:

\[ T = \frac{1}{\text{PWM_CLK}} = \frac{(\text{TM3_H}+1) \times (\text{TM3_L}+1)}{\text{TM3_CLK}_{\text{Source}}} \]

\[
\text{PWM}_{\text{Data}} = 0 \sim 127 \rightarrow \text{PWM2} \\
\text{PWM}_{\text{Duty1}} = W_1 / T = \frac{128 - (\text{PWM}_{\text{Data}}+1)}{\text{TM3_L}+1}
\]

\[
\text{PWM}_{\text{Data}} = 128 \sim 255 \rightarrow \text{PWM1} \\
\text{PWM}_{\text{Duty2}} = W_2 / T = \frac{(\text{PWM}_{\text{Data}}+1) - 128}{\text{TM3_L}+1}
\]
The formula of PWM Clock and PWM Duty Cycle of Differential Mode 100% Duty are as following:

\[ T = \frac{1}{PWM_{\text{CLK}}} = \frac{(TM3_H+1) \times (TM3_L+1)}{TM3_{\text{CLK Source}}} \]

\[
\begin{align*}
\text{PWM}_{\text{Data}} &= 0 \sim 127 \Rightarrow \text{PWM}_2 \\
\text{PWM}_{\text{Duty1}} &= 2W_1/T = 2 \times \left[\frac{128-\text{PWM}_{\text{Data}}-1}{TM3_L+1}\right] \\
\text{PWM}_{\text{Data}} &= 128 \sim 255 \Rightarrow \text{PWM}_1 \\
\text{PWM}_{\text{Duty2}} &= 2W_2/T = 2 \times \left[\frac{\text{PWM}_{\text{Data}}+1-128}{TM3_L+1}\right]
\end{align*}
\]
8.13 Low Voltage Detect (LVD)

The RA8917 builds in an integrated low-voltage detector. The supply voltage is divided and compared to the band gap reference output. If the detect voltage (VEXT) falls below the set voltage value, the bit0 of [REG 1034h] will indicate the status of LVD. The nominal values of the low-voltage detector four points are below [REG 1033h].

When the voltage is lower than the default value, then [REG 1034h] Bit0 will be “1”. The signal could output through I/O, and then a warning could happen when users connect an external LED or buzzer. Figure 8-28 and 8-29 are the LVD application circuit. There is also an example following by that. RA8917 provides external voltage input detect pin VEXT, which could be used as system low voltage detection.

![Figure 8-28 LVD Application](image1)

![Figure 8-29 LVD Application](image2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>[REG 1033h]: LVD Control Register</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### LVD Output Control
This bit is used to control the output of LVD. If set high, then the Port2 bit3 is defined as the output of LVD#.

- **0**: Disable LVD output
- **1**: Enable LVD Output

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### LVD Enable Control

- **0**: Disable
- **1**: Enable

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

### LVD Voltage Select

<table>
<thead>
<tr>
<th>Bit1</th>
<th>Bit0</th>
<th>Detected Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>3V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>2.8V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2.6V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2.4V</td>
</tr>
</tbody>
</table>

If the LVD enabled, the bit0 of register $1034h will indicate the status of LVD.

### LVD Status Register [REG 1034h]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>LVD Indicate.</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td>0: Normal Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Low Voltage Detected!</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:

```
LDA  #00001110b  ; LVD Enable and Output Control Enable, LVD Voltage=2.6V
STA  1033h

Voltage_Detect:
LDA  1034h       ; Low Voltage Detected
AND  #01h
BEQ  Normal_Voltage
JSR  Low_Voltage

Normal_Voltage:
JMP  Voltage_Detect

Low_Voltage:
    :
    :
    RTS
```
8.14 External SRAM

RA8917 allows users to connect an external RAM or ROM. The decoding address is 4000H~7FFFH, and the size is 16K Byte. If share the BANK with Flash ROM, the size could reach $2^{12} \times 16K = 64$Mbyte. Figure 8-30 is the diagram for connecting external 32K-Byte RAM.

If REG[1032h] bit6 is set as 1, and then FL_OE# and MEM_OE# can be jointly used. Therefore, when users use external RAM, users could refer to the following figure to change MEM_OE# as FL_OE Pin.
8.15 Analog-to-Digital Converter (ADC) Module

RA8917 built in a high performance 4 channel 12-bit full range A/D converter. This ADC is designed by Successive Approximate Register structure (S.A.R.), and conversion rate is 100KHz for signal channel. 12-bit ADC can be perfectly used in Touch Panel function.

![ADC Converter Diagram]

**Figure 8-32 ADC Converter**

**[REG 103Ah]: ADC High-Byte Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>ADC Output Data Bit[11:4]</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
</tbody>
</table>

**[REG 103Bh]: ADC Low-Byte Register**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2</td>
<td>Not Used</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td>1-0</td>
<td>ADC Output Data Bit[3:0]</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
</tbody>
</table>

**[REG 103Ch]: ADC Control Register(1)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Reserved</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td>6</td>
<td>ADC Interrupt Enable</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>ADC Loop Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>ADC Mode Select</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: 4-Channels ADC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Touch Panel</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### [REG 103Dh]: ADC Control Register(2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Touch Panel Switch Y2 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Touch Panel Switch Y1 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Touch Panel Switch X2 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Touch Panel Switch X1 Control</td>
<td>0h</td>
<td>0h</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>0: Switch Off</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Switch On</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### [REG 103Eh]: ADC Status Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-2</td>
<td>Not Used</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>1</td>
<td>ADC Transfer Done</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td>0: Not Ready</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Ready</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Touch Panel Detector</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td></td>
<td>0: Normal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Touch Detected</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
8.15.1 ADC Touch Panel Loop Control

Example1: (ADC Touch Panel Loop Control)

LDA    #00111000b
STA    103Ch

LDA    #0Fh
STA    103Dh

ReDetect:
LDA    103Eh
AND    #01h
BEQ    ReDetect

LDA    #0Ch
STA    103Dh
JSR    Delay
LDA    103Bh
STA    80h
LDA    103Ah
STA    81h

LDA    #03h
STA    103Dh
JSR    Delay
LDA    103Bh
STA    82h
LDA    103Ah
STA    83h

JMP    ReDetect

Delay:
NOP
NOP
RTS

Figure 8-33 ADC Touch Panel Loop Control Flowchart
8.15.2 ADC Touch Panel No Loop Control

**Example2: (ADC Touch Panel without Loop Control)**

```
LDA #00010000b
STA 103Ch

LDA #0Fh
STA 103Dh

ReDetect:
LDA 103Eh
AND #01h
BEQ ReDetect

LDA #0Ch
STA 103Dh

LDA 103Ch
ORA #00001000b
STA 103Ch

Wait:
LDA 103eh
AND #00000010b
BEQ Wait

LDA 103Bh
STA 80h
LDA 103Ah
STA 81h

LDA #03h
STA 103Dh

LDA 103Ch
ORA #00001000b
STA 103Ch

Wait1:
LDA 103Eh
AND #00000010b
BEQ Wait1
LDA 103Bh
STA 82h
LDA 103Ah
STA 83h
JMP ReDetect
```

Figure 8-34 ADC Touch Panel No Loop Control Flowchart
RA8917 contains a 12-bit ADC, providing two modes selection: one is 4-channels ADC, and the other one is for Touch Panel function. When Touch Panel mode is selected, there are ADC Loop Control and No Loop Control while reading X and Y coordination from Touch Panel. The Touch Panel function of RA8917 is controlled by [RAG 103Ch and 103Dh]. When Touch Panel detection is executed, which is controlled by REG[103Eh]bit0, and then open the 4-wire resistor touch panel Switch X1, X2, Y1 and Y2 ON by [REG 103Dh] bit0~3. ADC will read the voltage value from resistor, and get data of touched coordination after transformation.

8.16 1Hz, 2Hz and 1/60Hz Interrupt/Wakeup

RA8917 provides 1Hz, 2Hz, and 1/60 Hz’s Interrupt/Wakeup source. If 1/60Hz is used as Source Clock, the RTC (Real Time Clock) function could be reached after some S/W effort. When RA8917 enters into Sleep mode, it could also be used as time counting function and wake-up the IC.

8.17 Multiplier and Accumulator (MAC)

RA8917 includes a 16x16 Hardware Multiplier and Accumulator. It provides four modes selection: 16×16, 16×8, 8×16, and 8×8. The function of MAC helps programmers shorten development time and save efforts of writing S/W instructions. Programmers only need to choose which mode they need, and then it will quickly provide answers after filling in multiplier and multiplicand.

RA8917 provides two set-up types for MAC, each separately includes four modes selection: The design structure of MAC provides three data Register for MAC (Multiplier A, B and C). Multiplier A and B could be divided to High Byte(8-bit) and Low Byte(8-bit), and Multiplier C is a combination of C0(LL), C1(LH), C2(HL), and C3(HH) with 8-bit each. MAC’s register is set and controlled by REG[1040h~1048h]. Please refer to the following description for the example of Read and Write.

1. Multiplier

When use Multiplier(AxB=C), programmers could follow the following steps:
Step:
1. Write REG[1031h] bit4 (MAC Control Enable)
2. Write REG[1048h](Select Multiplier Mode)
3. Write-in Low Byte data (AL) of multiplicand first, and then write High Byte data (AH) of multiplicand. (If users choose 8x8 or 8x16 MAC, then only need to write Low Byte data (AL) of multiplicand.)
4. Write-in Low Byte data (BL) of multiplier first, and then write High Byte data (BH) of multiplier. (If users choose 8x8 or 8x16 MAC, then only need to write Low Byte data (BL) of multiplier.)
5. Read out the result, C0=C1=C2=C3

Therefore, users could also refer to the following program writing procedure and example.

A. 16×16 Multiplier:

Calculation 16x16 (No ACC)
(AL→AH→BL→BH→C0→C1→C2→C3)

<table>
<thead>
<tr>
<th>AL</th>
<th>AH</th>
<th>BL</th>
<th>BH</th>
<th>--</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>W</td>
<td>W</td>
<td>W</td>
<td>-</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>

Example:
LDA #00010000b ; MAC Control Enable
STA 1031h
LDA  #00001000b  ; Select AX=16 Bit, BX=16 Bit
STA  1048h  ; Clear CX, Accumulate Disable

LDA  #73h  ; AL=73h
STA  1040h
LDA  #0bh  ; AH=0bh
STA  1041h
LDA  #71h  ; BL=71h
STA  1042h
LDA  #01h  ; BH=01h
STA  1043h

LDA  1044h  ; Store the value of C0 to memory address 80h
STA  80h
LDA  1045h  ; Store the value of C1 to memory address 81h
STA  81h
LDA  1046h  ; Store the value of C2 to memory address 82h
STA  82h
LDA  1047h  ; Store the value of C3 to memory address 83h
STA  83h

Note: C=A × B=0b73h×0171h⇒C=1080C3h
User RAM 80h=C3h
User RAM 81h=80h
User RAM 82h=10h
User RAM 83h=00h

B. 16×8 Multiplier:

Calculation 16x8 (No ACC)
(AL AH BL C0 C1 C2 C3)

<table>
<thead>
<tr>
<th>AL</th>
<th>AH</th>
<th>BL</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>W</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
</tr>
<tr>
<td>W</td>
<td>W</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>

C. 8×16 Multiplier:

Calculation 8x16 (No ACC)
(AL BL BH C0 C1 C2 C3)

<table>
<thead>
<tr>
<th>AL</th>
<th>BL</th>
<th>BH</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>W</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
</tr>
<tr>
<td>W</td>
<td>W</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>

D. 8×8 Multiplier:

Calculation 8x8 (No ACC)
(AL BL C0 C1 C2 C3)

<table>
<thead>
<tr>
<th>AL</th>
<th>BL</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
</tr>
<tr>
<td>W</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>
Note:
1. BH is not used in 16x8’s MAC; therefore, please do not fill in other value in BH register.
2. AH is not used in 8x16’s MAC; therefore, please do not fill in other value in AH register.
3. AH and BH are not used in 8x8’s MAC; therefore, please do not fill in other value in AH and BH registers.

2. Multiplier and Accumulator

When use Multiplier and Accumulator (A1xB1+A2xB2=C), programmers could follow the following steps.
Step:
1. Write REG [1031h] bit4 (MAC Control Enable)
2. Write REG [1048h](Select Multiplier Mode)
3. Write-in Low Byte data (AL) of multiplicand first, and then write High Byte data (AH) of multiplicand. (If users choose 8x8 or 8x16 MAC, then only need to write Low Byte data (AL) of multiplicand.)
4. Write-in Low Byte data (BL) of multiplier first, and then write High Byte data (BH) of multiplier. (If users choose 8x8 or 8x16 MAC, then only need to write Low Byte data (BL) of multiplier.)
5. Repeat step 3 and 4, and write in second multiplicand and multiplier.
6. Read out the result, C0 C1 C2 C3

A. 16×16 Multiplier and Accumulator:

Calculation 16x16 (ACC)
(AL AH BL BH C0 C1 C2 C3)

<table>
<thead>
<tr>
<th>AL</th>
<th>AH</th>
<th>BL</th>
<th>BH</th>
<th>--</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>W</td>
<td>W</td>
<td>W</td>
<td>--</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>

Example:

```
LDA  #00010000b  ; MAC Control Enable
STA  1031h
LDA  #00001100b  ; Select AX=16 Bit, BX=16 Bit
STA  1048h       ; Clear CX, Accumulate Enable

One: LDA  #73h     ; AL=73h
     STA  1040h
     LDA  #0bh      ; AH=0bh
     STA  1041h
     LDA  #71h      ; BL=71h
     STA  1042h
     LDA  #01h      ; BH=01h
     STA  1043h

Two:  LDA  #73h    ; AL=73h
      STA  1040h
      LDA  #0bh     ; AH=0bh
      STA  1041h
      LDA  #71h     ; BL=71h
      STA  1042h
      LDA  #01h     ; BH=01h
      STA  1043h

LDA  1044h       ; Store the value of C0 to memory address 80h
```
STA 80h
LDA 1045h ; Store the value of C1 to memory address 81h
STA 81h
LDA 1046h ; Store the value of C2 to memory address 82h
STA 82h
LDA 1047h ; Store the value of C3 to memory address 83h
STA 83h

Note: \( C = A1 \times B1 + A2 \times B2 = 0b73h \times 0171h + 0b73h \times 0171h \Rightarrow C = 210186h \)
User RAM Address 80h=86h
User RAM Address 81h=01h
User RAM Address 82h=21h
User RAM Address 83h=00h

B. 16×8 Multiplier and Accumulator:

Calculation 16x8 (ACC)

\((AL \Rightarrow AH \Rightarrow BL \Rightarrow C0 \Rightarrow C1 \Rightarrow C2 \Rightarrow C3)\)

<table>
<thead>
<tr>
<th>AL</th>
<th>AH</th>
<th>BL</th>
<th>--</th>
<th>--</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>W</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>

C. 8×16 Multiplier and Accumulator:

Calculation 8x16 (ACC)

\((AL \Rightarrow BL \Rightarrow BH \Rightarrow C0 \Rightarrow C1 \Rightarrow C2 \Rightarrow C3)\)

<table>
<thead>
<tr>
<th>AL</th>
<th>--</th>
<th>BL</th>
<th>BH</th>
<th>--</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>--</td>
<td>W</td>
<td>W</td>
<td>--</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>

D. 8×8 Multiplier and Accumulator:

Calculation 8x8 (ACC)

\((AL \Rightarrow BL \Rightarrow C0 \Rightarrow C1 \Rightarrow C2 \Rightarrow C3)\)

<table>
<thead>
<tr>
<th>AL</th>
<th>--</th>
<th>BL</th>
<th>--</th>
<th>--</th>
<th>C0</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
</tr>
</thead>
<tbody>
<tr>
<td>W</td>
<td>--</td>
<td>W</td>
<td>--</td>
<td>--</td>
<td>R</td>
<td>R</td>
<td>R</td>
<td>R</td>
</tr>
</tbody>
</table>

Note:
1. BH is not used in 16x8’s MAC; therefore, please do not fill in other value in BH register.
2. AH is not used in 8x16’s MAC; therefore, please do not fill in other value in AH register.
3. AH and BH are not used in 8x8’s MAC; therefore, please do not fill in other value in AH and BH registers.
4. If CPU is slow, IDLE cycle is optional.

[REG 1040h]: Multiplier A Low-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier A Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1041h]: Multiplier A High-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
</table>
7-0 Multiplier A Data Bit[15:8] 0h 0h R/W

[REG 1042h]: Multiplier B Low-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier B Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1043h]: Multiplier B High-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier B Data Bit[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1044h]: Multiplier C Low Word Low-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[7:0]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1045h]: Multiplier C Low Word High-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[15:8]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1046h]: Multiplier C High Word Low-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[23:16]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1047h]: Multiplier C High Word High-Byte Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-0</td>
<td>Multiplier C Data Bit[31:24]</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
</tbody>
</table>

[REG 1048h]: Multiplier Control Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-4</td>
<td>Overflow Flag</td>
<td>0h</td>
<td>0h</td>
<td>R</td>
</tr>
<tr>
<td>3</td>
<td>Clear CX</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0: Clear CX</td>
<td>1: No Action</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Accumulate Mode</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0: Disable, CX = AX x BX</td>
<td>1: Enable, CXn+1 = AX x BX + CXn</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>AX 8/16Bit Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0: AX = 16Bit</td>
<td>1: AX = 8Bit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>BX 8/16Bit Select</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>0: BX = 16Bit</td>
<td>1: BX = 8Bit</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8.18 Extended Data Out (EDO) RAM Interface

RA8917 Support 8M×8Bit, 4M×4Bit and (4M×4Bit)×2 Extended Data Out (EDO) RAM Interface. The RA8917 have CAS-before-RAS refresh capabilities for EDO RAM.
8.18.1 Continue Read Cycle

Step:
1. Write REG[1063h] (EDO RAM Address Upper-Byte)
2. Write REG[1062h] (EDO RAM Address Middle-Byte)
3. Write EDO RAM Address Lower-Byte[1061h]
4. Read Data register[1064h]

The define follow as:
- W: Write
- R: Read
- LA: EDO RAM Address Lower-Byte REG[1061h]
- MA: EDO RAM Address Middle-Byte REG[1062h]
- UA: EDO RAM Address Upper-Byte REG[1063h]
- DATA: Data Buffer REG[1064h]

8.18.2 Continue Write Cycle

Step:
1. Write REG[1063h] (EDO RAM Address Upper-Byte)
2. Write REG[1062h] (EDO RAM Address Middle-Byte)
3. Write EDO RAM Address Lower-Byte[1061h]
4. Write Data register[1064h]

Write:
- LDA  #00h
- STA  1063h ; Write Data to EDO RAM Address Upper-Byte REG[1063h]
- LDA  #00h
STA 1062h ; Write Data to EDO RAM Address Middle-Byte REG[1062h]
LDA #00h
STA 1061h ; Write Data to EDO RAM Address Lower-Byte REG[1061h]
LDA #01h
STA 1064h ; Read Data to REG[1064h]
LDA #02h
STA 1064h
LDA #03h
STA 1064h
LDA #04h
STA 1064h
END

Table 8-7 8Mx8 EDO RAM Map

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000</td>
<td>01h</td>
</tr>
<tr>
<td>000001</td>
<td>02h</td>
</tr>
<tr>
<td>000002</td>
<td>03h</td>
</tr>
<tr>
<td>000003</td>
<td>04h</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>7FFFFF</td>
<td></td>
</tr>
</tbody>
</table>

Note: Each data is one Byte unit

If choose 4M × 4bit EDO RAM mode, then please refer to the following Figure 8-36 and Table 8-8:
Figure 8-36 RA8917 with EDO RAM (4Mx4)

Table 8-8 (4Mx4)x2 EDO RAM Map

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000</td>
<td>000000</td>
</tr>
<tr>
<td>000001</td>
<td>000001</td>
</tr>
<tr>
<td>000002</td>
<td>000002</td>
</tr>
<tr>
<td>000003</td>
<td>000003</td>
</tr>
<tr>
<td>:</td>
<td>:</td>
</tr>
<tr>
<td>3FFFFF</td>
<td>3FFFFF</td>
</tr>
</tbody>
</table>
8.18.3 Read/Write Interleave

Example:

```
LDA  #00h
STA  1063h ; Write Data to EDO RAM Address Upper-Byte REG[1063h]
LDA  #00h
STA  1062h ; Write Data to RAM Address Middle-Byte REG[1062h]
LDA  #00h
STA  1061h ; Write Data to EDO RAM Address Lower-Byte REG[1061h]
LDA  #01h
STA  1064h ; Read Data to REG[1064h]
LDA  #02h
STA  1064h
LDA  #03h
STA  1064h
LDA  #04h
STA  1064h
END
```

Please refer to the above program example. After READ/WRITE, Register address reads the last data value is “4”, see Table 8-9.

<table>
<thead>
<tr>
<th>ADDRESS DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDRESS</td>
</tr>
<tr>
<td>000000</td>
</tr>
<tr>
<td>000001</td>
</tr>
<tr>
<td>000002</td>
</tr>
<tr>
<td>000003</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>7FFFFFF</td>
</tr>
</tbody>
</table>

8.19 Analog Switch

RA8917 Support three internal analog switch with one common input for user's application.
### [REG 105Fh]: Analog Switch Control Register [SW_CTL]

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Reset</th>
<th>Default</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-3</td>
<td>Reserved.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td>2</td>
<td>Analog Switch 3 Enable.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Analog Switch 2 Enable.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Analog Switch 1 Enable.</td>
<td>0h</td>
<td>0h</td>
<td>R/W</td>
</tr>
<tr>
<td></td>
<td>0: Disable</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1: Enable</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
9. Electrical Characteristic

Operating Temperature Range .............................................. -10°C to +75°C
Storage Temperature Range .................................................... -55°C to +140°C
Lead Temperature Range (soldering, 10 seconds)....................... +300°C
Positive Voltage on any pin, with respect to Ground .............. VIo + 0.3V
Negative Voltage on any pin, with respect to Ground ............. -0.3V
Maximum VIo ....................................................................... +5V
Maximum Vcc ....................................................................... +5.5V

* Stresses above those listed above could cause permanent damage to the device. This is stress rating only
and functional operation of the device at any other condition above those indicated in the operation sections
of this specification is not implied.

9.1 DC Electrical Characteristics
(TA = -10°C~75°C, Vcc = 2.4V ~ 3.6V)

Table 9-1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Buffer</td>
<td>VIL</td>
<td>2.0</td>
<td>0.8</td>
<td>V</td>
<td>V</td>
<td>TTL Levels</td>
</tr>
<tr>
<td>Low Input Level</td>
<td>VIL</td>
<td>2.0</td>
<td>0.8</td>
<td>V</td>
<td>V</td>
<td>TTL Levels</td>
</tr>
<tr>
<td>High Input Level</td>
<td>VIH</td>
<td>0.8</td>
<td>2.0</td>
<td>V</td>
<td>V</td>
<td>TTL Levels</td>
</tr>
<tr>
<td>Schmitt Input Buffer</td>
<td>VILS</td>
<td>2.2</td>
<td>250</td>
<td>0.8</td>
<td>V</td>
<td>Schmitt Trigger</td>
</tr>
<tr>
<td>Low Input Level</td>
<td>VILS</td>
<td>2.2</td>
<td>250</td>
<td>0.8</td>
<td>V</td>
<td>Schmitt Trigger</td>
</tr>
<tr>
<td>High Input Level</td>
<td>VIHIS</td>
<td>250</td>
<td>0.8</td>
<td>V</td>
<td>V</td>
<td>Schmitt Trigger</td>
</tr>
<tr>
<td>Schmitt Trigger Hysteresis</td>
<td>VHY</td>
<td>250</td>
<td>0.8</td>
<td>V</td>
<td>V</td>
<td>Schmitt Trigger</td>
</tr>
</tbody>
</table>
| Output Buffer | VOL | -10 | 0.5 | V | uA | IOL = 12mA (24mA)
| Low Output Level | IOL | -10 | 0.5 | V | uA | VIN = 0 to Vcc (Note 1) |
| High Output Level | VOL | -10 | 0.5 | V | uA | VIN = 0 to Vcc (Note 1) |
| Output Leakage | VOH | 10 | 0.5 | V | uA | VIN = 0 to Vcc (Note 1) |
| I/O Buffer | VOL | 2.4 | -10 | 0.5 | V | IOL = 8mA |
| Low Output Level | VOL | 2.4 | -10 | 0.5 | V | IOH = -4mA |
| High Output Level | VOL | 2.4 | -10 | 0.5 | V | VIN = 0 to Vcc (Note 1) |
| Output Leakage | VOH | -10 | 0.5 | V | uA | VIN = 0 to Vcc (Note 1) |
| I/O Buffer (PT2_[7:6]) | VOL | 2.4 | -10 | 0.5 | V | IOL = 36mA |
| Low Output Level | VOL | 2.4 | -10 | 0.5 | V | IOH = -18mA |
| High Output Level | VOL | 2.4 | -10 | 0.5 | V | VIN = 0 to Vcc (Note 1) |
| Output Leakage | VOH | -10 | 0.5 | V | uA | VIN = 0 to Vcc (Note 1) |
| I/O Buffer (FL_CE#, FL_OE#, FL_WE#, | VOL | 2.4 | -10 | 0.4 | V | IOL = 8mA |
| Low Output Level | VOL | 2.4 | -10 | 0.4 | V | IOH = -4mA |
| High Output Level | VOL | 2.4 | -10 | 0.4 | V | VIN = 0 to VIo (Note 1) |
| Output Leakage | VOH | -10 | 0.4 | V | uA | VIN = 0 to VIo (Note 1) |

Capacitance TA = 25°C; Vcc = 3.3V
10. Application

The following Block diagram is the basic application circuit of RA8917. We also give three examples on the user manual of RICE-2000 to let users have more understanding of RA8917 and the develop environment of RICE-2000, and then start to proceed program designing and product developing. The examples have one simple I/O control and speech samples. Please refer to the user manual of RICE-2000 if you needed.

<table>
<thead>
<tr>
<th>Application Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple I/O Controller</td>
</tr>
<tr>
<td>Speech Controller</td>
</tr>
<tr>
<td>Middle-Grade Product</td>
</tr>
<tr>
<td>High-Grade Product</td>
</tr>
</tbody>
</table>
Appendix A. Package Dimension

Note: Dimension are in millimeters.
Appendix B. Supports Flash

The following tables A-1 ~ A-8 are the Flash ROM list, which RA8917 supports.

<table>
<thead>
<tr>
<th>Table A-1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Manufacturer</strong></td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
<tr>
<td>MXIC</td>
</tr>
</tbody>
</table>
### Table A-2

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Device Number</th>
<th>Memory Size</th>
<th>Voltage</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSEL</td>
<td>V29C51000T</td>
<td>512K Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51000B</td>
<td>512K Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51001T</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51001B</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51002T</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51002B</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51004T</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51004B</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29LC51000</td>
<td>512K Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29LC51001</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29LC51002</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51400T</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C51400B</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C31004T</td>
<td>4M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>MOSEL</td>
<td>V29C31004B</td>
<td>4M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
</tbody>
</table>

### Table A-3

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Device Number</th>
<th>Memory Size</th>
<th>Voltage</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMIC</td>
<td>A29001TL-55</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29001UL-55</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29010L-55</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29002TL-55</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29002UL-55</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29040L-55</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29400TV-55</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29400UV-55</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29800TV-55</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMIC</td>
<td>A29800UV-55</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
</tbody>
</table>
### Table A-4

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Device Number</th>
<th>Memory Size</th>
<th>Voltage</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATMEL</td>
<td>AT49F512</td>
<td>512K Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F001(N)</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F001(N)T</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F002(N)</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F002(N)T</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F010</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F020</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F040</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F040T</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F080</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F080T</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F2048A</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F4096A</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F008A</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F008AT</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV8011</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV8011T</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F16X4</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49F16X4T</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV512</td>
<td>512K Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV001(N)</td>
<td>1M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV001(N)T</td>
<td>1M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV002(N)</td>
<td>2M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV002(N)T</td>
<td>2M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV010</td>
<td>1M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV020</td>
<td>2M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV040</td>
<td>4M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV008AT</td>
<td>8M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV008A</td>
<td>8M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV2048A</td>
<td>2M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV4096A</td>
<td>4M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV8011</td>
<td>8M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV8011T</td>
<td>8M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV16X</td>
<td>16M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV16XT</td>
<td>16M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>Device Number</td>
<td>Memory Size</td>
<td>Voltage</td>
<td>Bus</td>
</tr>
<tr>
<td>--------------</td>
<td>----------------</td>
<td>-------------</td>
<td>---------</td>
<td>------</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV16X4</td>
<td>16M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV16X4T</td>
<td>16M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV32X</td>
<td>32M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV/LV32XT</td>
<td>32M Bit</td>
<td>3.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ATMEL</td>
<td>AT49BV3214T</td>
<td>32M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
</tbody>
</table>

Table A-5

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Device Number</th>
<th>Memory Size</th>
<th>Voltage</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMD</td>
<td>AM29F002BT</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F002BB</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F004BT</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F004BB</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F200BT</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F200BB</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F400BT</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F400BB</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F800BT</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F800BB</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F160DT</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F160DB</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F010B</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F040B</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F080B</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F016D</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F017D</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29F032B</td>
<td>32M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV001BT</td>
<td>1M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV001BB</td>
<td>1M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV002BT</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV002BB</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV004BT</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV004BB</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV008BT</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV008BB</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV116DT</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV116DB</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>AMD</td>
<td>AM29LV200BT</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
</tbody>
</table>
### Table A-6

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Device Number</th>
<th>Memory Size</th>
<th>Voltage</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>SST</td>
<td>SST39SF512-70-4C-NH</td>
<td>512K Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39SF010-70-4C-NH</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39SF010A-70-4C-NH</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39SF020A-45-4C-NH</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39SF040-45-4C-NH</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39VF512-70-4C-NH</td>
<td>512K Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39VF010-70-4C-NH</td>
<td>1M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39VF020-70-4C-NH</td>
<td>2M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39VF040-70-4C-NH</td>
<td>4M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39VF080-70-4C-EI</td>
<td>8M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>SST</td>
<td>SST39VF016-70-4C-EI</td>
<td>16M Bit</td>
<td>3.0V</td>
<td>x8</td>
</tr>
<tr>
<td>Manufacturer</td>
<td>Device Number</td>
<td>Memory Size</td>
<td>Voltage</td>
<td>Bus</td>
</tr>
<tr>
<td>--------------</td>
<td>---------------</td>
<td>-------------</td>
<td>---------</td>
<td>-----</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F040C</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F080A</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F016A</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F200TC</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F400TC</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F400BC</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F800TA</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F800BA</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29F033C</td>
<td>32M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV002TC</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV002BC</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV004TC</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV004BC</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV008TA</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV008BA</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV200TC</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV200BC</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV400TC</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV400BC</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV800TA</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV800BA</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV160TE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV160BE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL161TE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL161BE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL162TE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL162BE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL163TE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL163BE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL164TE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29DL164BE</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV320TE</td>
<td>32M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>Fujistu</td>
<td>MBM29LV320BE</td>
<td>32M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
</tbody>
</table>
## Table A-8

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Device Number</th>
<th>Memory Size</th>
<th>Voltage</th>
<th>Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST</td>
<td>M29F512B</td>
<td>512K Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29F002T</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29F002B</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29F200T</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F200BB</td>
<td>2M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F400T</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F400B</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F800AT</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F800AB</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F160BT</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F160BB</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29F010B</td>
<td>1M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29F040</td>
<td>4M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29F080A</td>
<td>8M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29F016B</td>
<td>16M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29F032D</td>
<td>32M Bit</td>
<td>5.0V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W022BT</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W022BB</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W004T</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W004B</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W008AT</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W008AB</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W200BT</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W200BB</td>
<td>2M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W400T</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W400B</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W800AT</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W800AB</td>
<td>8M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W160BT</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W160BB</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W320DT</td>
<td>32M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W320DB</td>
<td>32M Bit</td>
<td>3.3V</td>
<td>x8/x16</td>
</tr>
<tr>
<td>ST</td>
<td>M29W512B</td>
<td>512K Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W010B</td>
<td>1M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W040</td>
<td>4M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
<tr>
<td>ST</td>
<td>M29W017D</td>
<td>16M Bit</td>
<td>3.3V</td>
<td>x8</td>
</tr>
</tbody>
</table>