Crystalfontz This controller datasheet was downloaded from **http://www.crystalfontz.com/controllers/**

RockWorks

RW1063-0B-002

16COM/40SEG DRIVER & CONTROLLER

◆ INTRODUCTION

RW1063 is a LCD driver & controller LSI which is fabricated by low power CMOS technology. It can display 2 lines x 8 (5 x 8 dot format) characters or 1 lines x 8 (5 x 8 or 5 x 11dot format) characters. It is ideal for multi-language application.
Standard code RW1063-0B-002 can support up to 240 fonts. Customized codes are available.

◆ FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal drivers: 16common and 40 segment for 2 line display, 1/16 duty (N=1, F=0).
  11common and 40 segment for 1 line display, 1/11 duty (N=0, F=1).
  8 common and 40 segment for 1 line display, 1/8 duty (N=0, F=0).

- Easy interface with 4-bit or 8-bit 68 series MPU or 4 lines SPI / IIC serial peripheral interface
- 5 x 8 dot matrix font or 5 x 11 dot matrix font
- Various instruction functions
- Automatic power on reset
- Double Frequency, half instruction time

◆ FEATURES

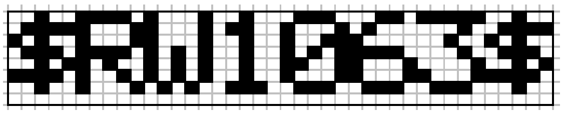
- Internal Memory
- Character Generator ROM (CGROM): 13200 bits (240 characters: 5 x 8 dot or 5 x 11 dots)
- Character Generator RAM (CGRAM): 64 x 8 bits (8 characters x 5 x 8 dot or 4 characters x 5 x 11)
- Display Data RAM (DDRAM): 80 x 8 bits (80 characters max.)
- Power supply voltage range: 2.7 ~ 5.5 V (VDD)
- LCD Drive voltage range: 3.0 ~ 7.0V (VDD – V5)
- CMOS process
- Programmable duty cycle: 1/16, 1/11, 1/8 (refer to Table1)
- Low power consumption
- Bare chip available

RW1063 Revision History		
Version	**Date**	**Description**
0.0	2011/8/4	First Edition
0.1	2011/11/9	Modify the AC Characteristics
0.2	2011/11/18	Make correction for number duty. P.4,P.9,P.25,P.32~P.33,P.40~P.43,P.47
0.3	2011/11/25	Make correction for number duty. P.1,P.7,P12,P.43,P.47 Modify initializing by instruction and DC characteristics(VIL)
0.3a	2012/4/13	Pad configuration add Substrate connects to VDD note
0.4	2013/1/15	Font table picture is changed
0.4a	2013/1/22	Modify page 47 circuit and interface setting
0.5	2013/11/26	Add 4-SPI and IIC timing

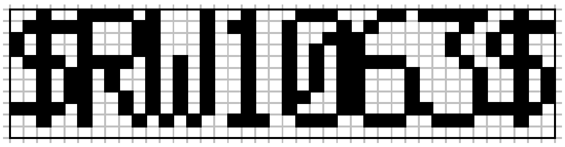
◆ Programmable duty cycles

Table 1

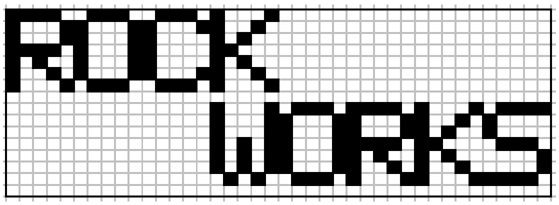
Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable characters	Possible icons
1	1/8	1 lines of 8 characters	0
	1/11		
2	1/16	2 lines of 8 characters	0



1 line x 8 (5 x 8 dot format)

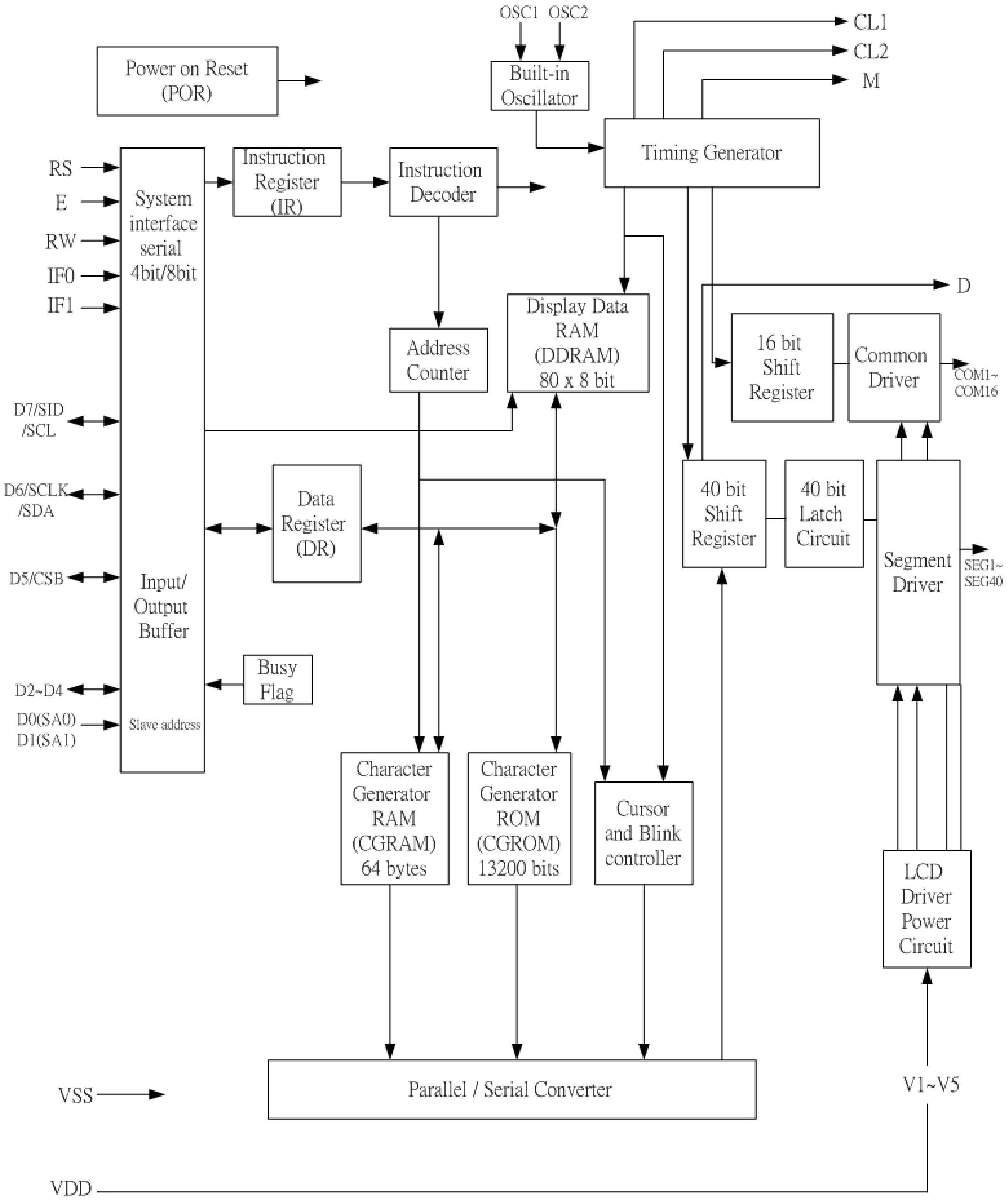


1 line x 8 (5 x 11 format)

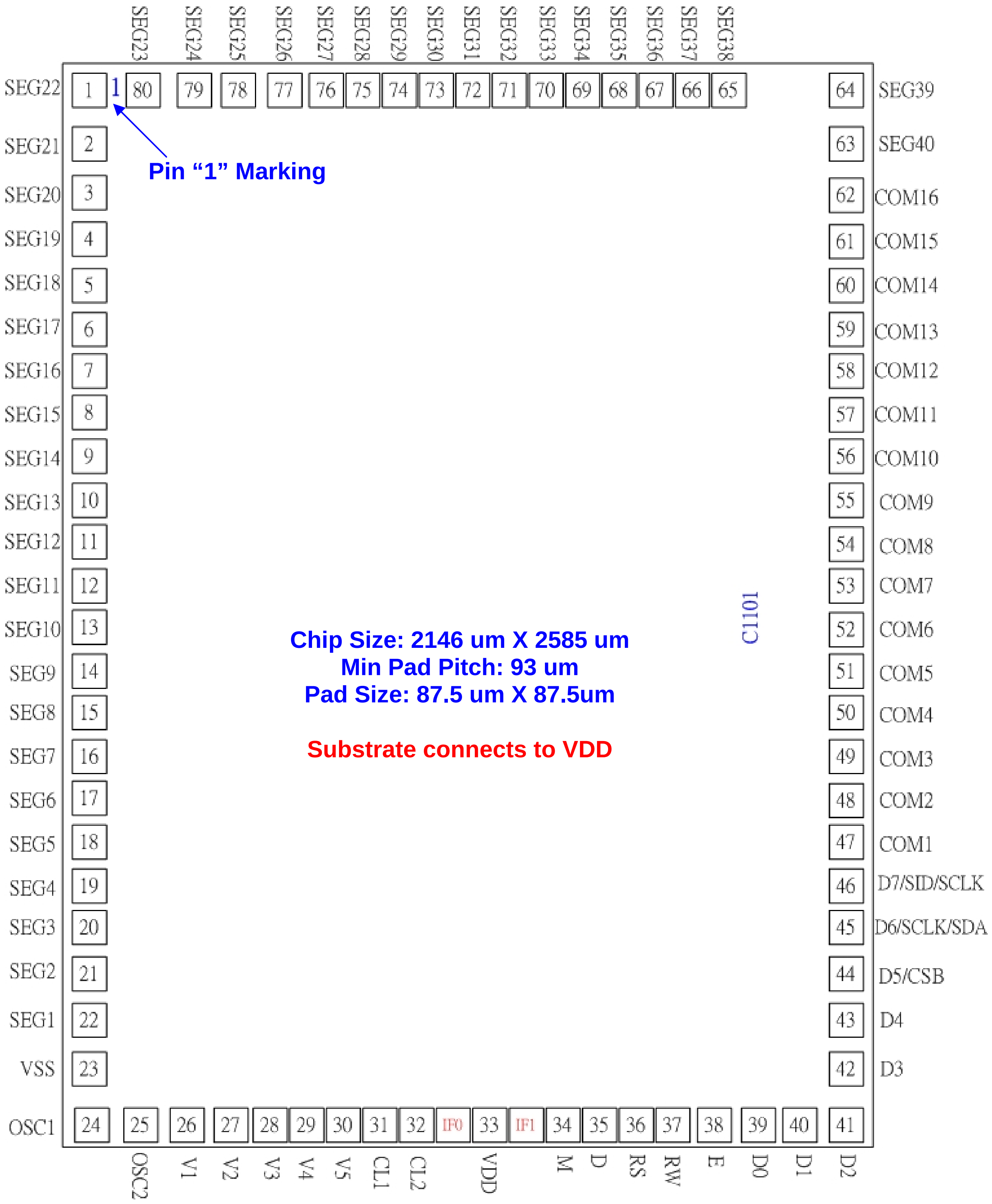


2 lines x 8 (5 x 8 dot format)

◆ BLOCK DIAGRAM


OSC1
OSC2
CL1
CL2
M
Power on Reset (POR)
Built-in Oscillator
Timing Generator
RS
E
RW
IF0
IF1
System interface serial 4bit/8bit
Instruction Register (IR)
Instruction Decoder
Display Data RAM (DDRAM) 80 x 8 bit
Address Counter
D
16 bit Shift Register
Common Driver
COM1~ COM16
D7/SID /SCL
D6/SCLK /SDA
D5/CSB
D2~D4
D0(SA0) D1(SA1)
Input/ Output Buffer
Slave address
Data Register (DR)
Busy Flag
40 bit Shift Register
40 bit Latch Circuit
Segment Driver
SEG1~ SEG40
Character Generator RAM (CGRAM) 64 bytes
Character Generator ROM (CGROM) 13200 bits
Cursor and Blink controller
LCD Driver Power Circuit
Parallel / Serial Converter
VSS
V1~V5
VDD

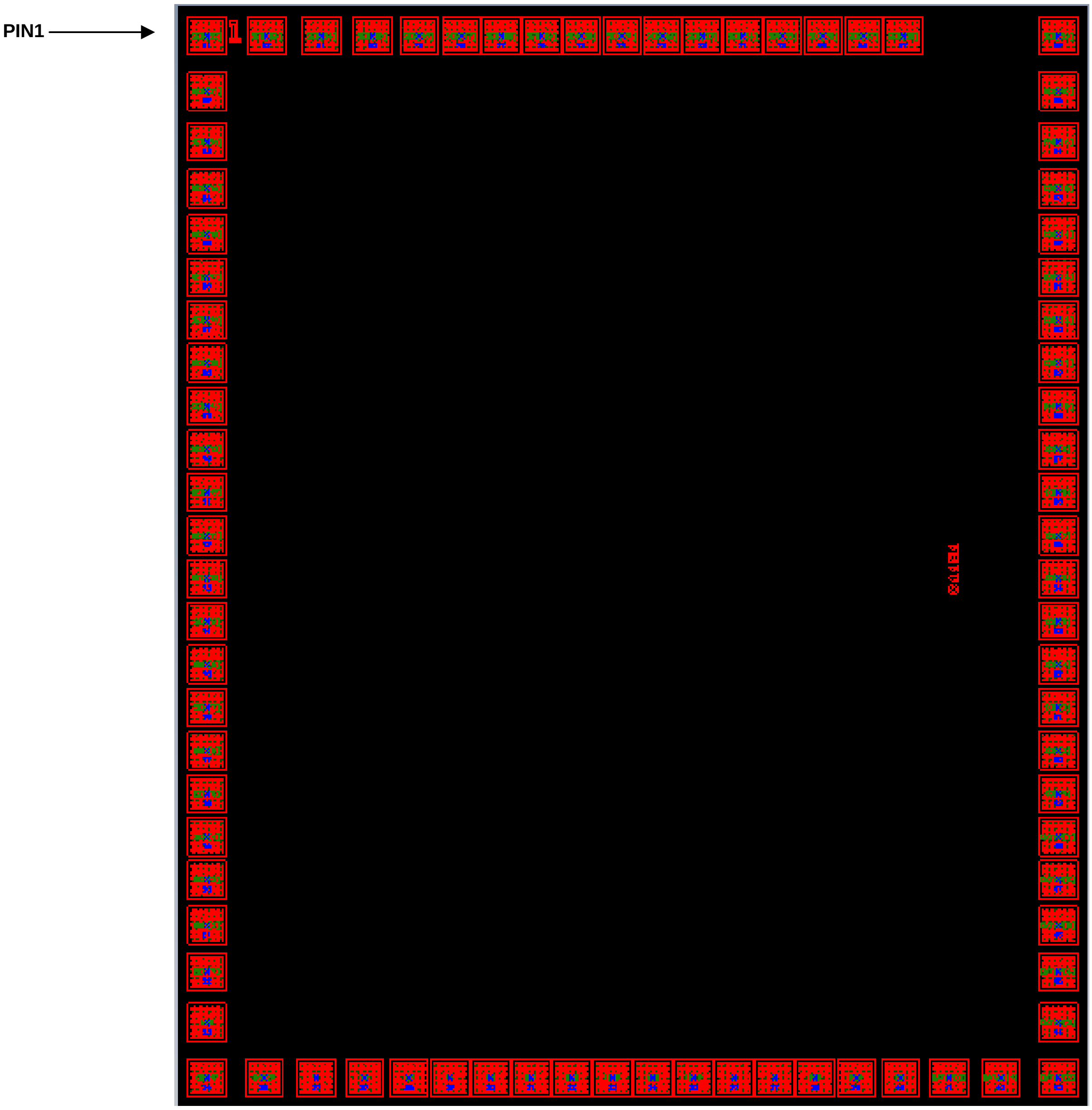
◆ **PAD CONFIGURATION**


SEG23
SEG24
SEG25
SEG26
SEG27
SEG28
SEG29
SEG30
SEG31
SEG32
SEG33
SEG34
SEG35
SEG36
SEG37
SEG38
SEG22 1
1
80
79
78
77
76
75
74
73
72
71
70
69
68
67
66
65
64 SEG39
SEG21 2
Pin “1” Marking
63 SEG40
SEG20 3
62 COM16
SEG19 4
61 COM15
SEG18 5
60 COM14
SEG17 6
59 COM13
SEG16 7
58 COM12
SEG15 8
57 COM11
SEG14 9
56 COM10
SEG13 10
55 COM9
SEG12 11
54 COM8
SEG11 12
53 COM7
C1101
SEG10 13
52 COM6
SEG9 14
51 COM5
SEG8 15
50 COM4
SEG7 16
49 COM3
SEG6 17
48 COM2
SEG5 18
47 COM1
SEG4 19
46 D7/SID/SCLK
SEG3 20
45 D6/SCLK/SDA
SEG2 21
44 D5/CSB
SEG1 22
43 D4
VSS 23
42 D3
OSC1 24
25 OSC2
26 V1
27 V2
28 V3
29 V4
30 V5
31 CL1
32 CL2
IF0
33 VDD
IF1
34 M
35 D
36 RS
37 RW
38 E
39 D0
40 D1
41 D2

Chip Size: 2146 um X 2585 um
Min Pad Pitch: 93 um
Pad Size: 87.5 um X 87.5um

Substrate connects to VDD

◆ CHIP LAYOUT



◆

PAD LOCATION

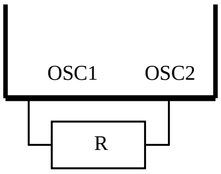
Unit: um

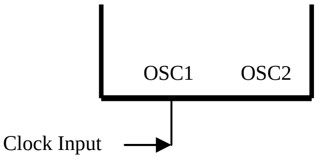
Pad No.	Pin Name	X	Y	Pad No.	Pin Name	X	Y
1	SEG[22]	-984.3	1203.8	40	D1(SA1)	851.8	-1203.8
2	SEG[21]	-984.3	1076.3	41	D2	984.3	-1203.8
3	SEG[20]	-984.3	958.8	42	D3	984.3	-1076.6
4	SEG[19]	-984.3	851.3	43	D4	984.3	-959.1
5	SEG[18]	-984.3	746.1	44	D5(CSB)	984.3	-851.6
6	SEG[17]	-984.3	646.6	45	D6/SCLK/SDA	984.3	-746.4
7	SEG[16]	-984.3	547.1	46	D7/SID/SCLK	984.3	-646.9
8	SEG[15]	-984.3	447.6	47	COM[1]	984.3	-547.4
9	SEG[14]	-984.3	348.1	48	COM[2]	984.3	-447.9
10	SEG[13]	-984.3	248.6	49	COM[3]	984.3	-348.4
11	SEG[12]	-984.3	149.1	50	COM[4]	984.3	-248.9
12	SEG[11]	-984.3	49.6	51	COM[5]	984.3	-149.4
13	SEG[10]	-984.3	-49.9	52	COM[6]	984.3	-49.9
14	SEG[9]	-984.3	-149.4	53	COM[7]	984.3	49.6
15	SEG[8]	-984.3	-248.9	54	COM[8]	984.3	149.1
16	SEG[7]	-984.3	-348.4	55	COM[9]	984.3	248.6
17	SEG[6]	-984.3	-447.9	56	COM[10]	984.3	348.1
18	SEG[5]	-984.3	-547.4	57	COM[11]	984.3	447.6
19	SEG[4]	-984.3	-646.9	58	COM[12]	984.3	547.1
20	SEG[3]	-984.3	-746.4	59	COM[13]	984.3	646.6
21	SEG[2]	-984.3	-851.6	60	COM[14]	984.3	746.1
22	SEG[1]	-984.3	-959.1	61	COM[15]	984.3	851.3
23	VSS	-984.3	-1076.6	62	COM[16]	984.3	958.8
24	OSC1	-984.3	-1203.8	63	SEG[40]	984.3	1076.3
25	OSC2	-851.8	-1203.8	64	SEG[39]	984.3	1203.8
26	V1	-731.9	-1203.8	65	SEG[38]	626.4	1203.8
27	V2	-619.4	-1203.8	66	SEG[37]	533.4	1203.8
28	V3	-516.9	-1203.8	67	SEG[36]	440.4	1203.8
29	V4	-422.6	-1203.8	68	SEG[35]	347.4	1203.8
30	V5	-328.7	-1203.8	69	SEG[34]	254.4	1203.8
31	CL1	-234.8	-1203.8	70	SEG[33]	161.4	1203.8
32	CL2	-140.9	-1203.8	71	SEG[32]	68.4	1203.8
	IF0	-47.0	-1203.8	72	SEG[31]	-24.6	1203.8
33	VDD	47.0	-1203.8	73	SEG[30]	-117.6	1203.8
	IF1	140.9	-1203.8	74	SEG[29]	-210.6	1203.8
34	M	234.8	-1203.8	75	SEG[28]	-303.6	1203.8
35	D	328.7	-1203.8	76	SEG[27]	-396.6	1203.8
36	RS	422.6	-1203.8	77	SEG[26]	-494.2	1203.8
37	RW	516.9	-1203.8	78	SEG[25]	-601.7	1203.8
38	E	619.4	-1203.8	79	SEG[24]	-719.2	1203.8
39	D0(SA0)	731.9	-1203.8	80	SEG[23]	-846.7	1203.8

◆ PAD DESCRIPTION

PAD	INPUT/ OUTPUT	DESCRIPTION		INTERFACE
VDD	-	Power supply	2.7V ~ 5.5V	Power supply
VSS			0V	
V1-V5			Bias voltage level for LCD driving	
SEG1-SEG40	O	Segment output	Segment signal output for LCD drive	LCD
COM1-COM16	O	Common output	Common signal output for LCD drive	LCD
OSC1	I	Oscillator	When oscillation is performed, a resistor must be connected externally. OSC1 also can be the external clock input pin when external clock mode used, OSC2 keep open while external clock input mode.	External Clock input pin (OSC1) Reference Note
OSC2	O	Oscillator		
RS	I	Register select	In bus mode, used as register selection input. When RS = “High”, Date register is selected. When RS = “Low”, Instruction register is selected.	MPU
E	I	Read. Write enable	In bus mode, used as read write enable signal.	MPU
RW	I	Read. Write	In bus mode, used as read / write selection input. When RW =”High”, read operation. When RW =”Low”, write operation.	MPU

Note:
1. VDD >=V1>=V2>=V3>=V4>=V5 must be maintained
2. Two clock input mode



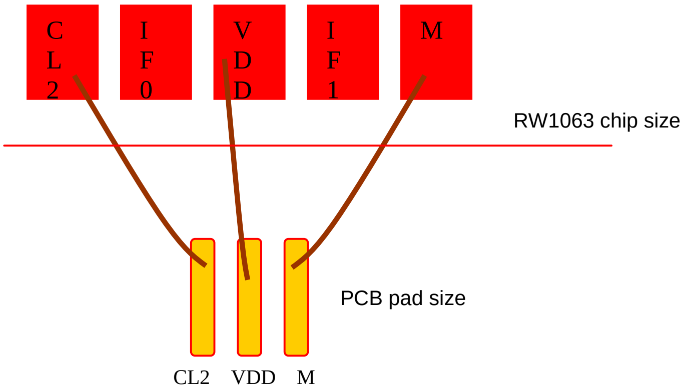


PAD	INPUT/ OUTPUT	DESCRIPTION		INTERFACE
DB0-DB3	I/O	Data bus 0~3/Slave address for IIC(DB1,DB0)	In 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode or serial mode, open these pins.	MPU
			In IIC interface ,DB1**(SA1)** and DB0**(SA0)** are used for Slave address, must be connect to VDD or VSS.	
DB4	I/O	Data bus 4	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order.	MPU
DB5/CSB	I/O	Data bus 5/ Chip select	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. In 4-SPI serial mode, used as chip selection input. In I2C serial mode, used as chip selection input. When CSB = “Low”, selected When CSB = “High”, not selected. (Low access enable)	MPU
DB6/SCLK /SDA	I/O	Data bus 6/ Serial clock input/Serial input data	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order.	MPU
			When the 4-Line serial interface selected: SCLK: serial clock input	
			When the IIC interface selected: SDA: serial input data	
DB7/SID /SCL	I/O	Data bus 7/ Serial data input/Serial clock input	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output.	MPU
			When the 4-Line serial interface selected: SID: serial data input	
			When the IIC interface selected: SCL: serial clock input	

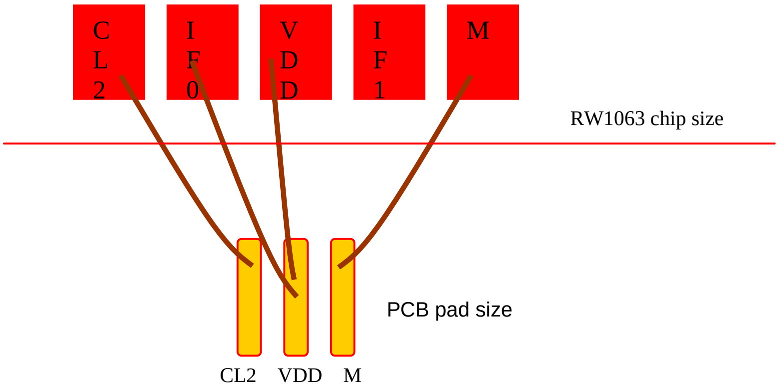
<table>
<tr><th>PAD</th><th>INPUT/ OUTPUT</th><th colspan="2">DESCRIPTION</th><th>INTERFACE</th></tr>
<tr><td>IF1,IF0</td><td>I</td><td>Interface select pins</td><td><table><tr><th>IF1</th><th>IF0</th><th>Interface</th></tr><tr><td>open</td><td>open</td><td>6800</td></tr><tr><td>open</td><td>Bonding to VDD</td><td>IIC</td></tr><tr><td>Bonding to VDD</td><td>open</td><td>4SPI</td></tr></table></td><td>MPU</td></tr>
<tr><td>M</td><td>O</td><td>Extension driver</td><td>Output the alternating signal to convert LCD driver waveform to A.C.</td><td></td></tr>
<tr><td>D</td><td>O</td><td>Extension driver</td><td>Outputs extension driver data (the 41st dot’s area)</td><td></td></tr>
<tr><td>CL1</td><td>O</td><td>Extension driver</td><td>Extension driver latch clock</td><td></td></tr>
<tr><td>CL2</td><td>O</td><td>Extension driver</td><td>Extension driver shift clock</td><td></td></tr>
</table>

◆ Interface select bonding Note for IF1,IF0

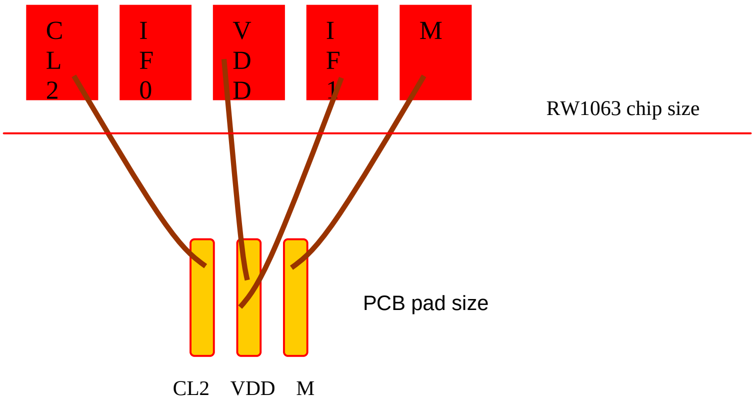
1. 6800 series MPU interface (IF0=open、IF1=open)


C L 2
I F 0
V D D
I F 1
M
RW1063 chip size
PCB pad size
CL2
VDD
M

2. IIC Interface Select (IF0=VDD、IF1=open)


C L 2
I F 0
V D D
I F 1
M
RW1063 chip size
PCB pad size
CL2
VDD
M

3. 4SPI Interface Select (IF0=open、IF1=VDD)


C L 2
I F 0
V D D
I F 1
M
RW1063 chip size
PCB pad size
CL2
VDD
M

◆ FUNCTION DESCRIPTION

● SYSTEM INTERFACE (Parallel 8-bit bus and 4-bit bus)

This chip has all four kinds interface type with MPU: IIC, 4SPI, 4-bit bus and 8-bit bus. Serial and parallel buses (4-bit/8-bit) are selected by IF1 and IF0 input pins, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.
During read or write operation, two 8-bit registers are used. One is data register (DR); the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.
IR: Instruction Register.
DR: Data Register.

RS	R/W	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR)

● BUSY FLAG (BF) (only support parallel 8-bit bus and 4-bit bus)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R / W = High (Read Instruction Operation); through DB7 before executing the next instruction, be sure that BF is not High.

● DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to Figure 1.)

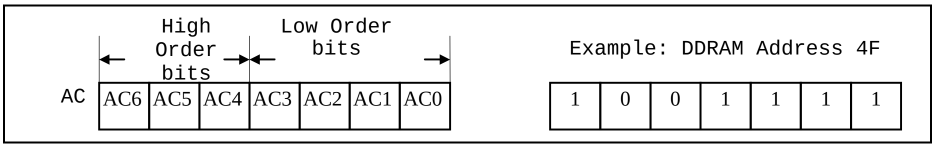


Figure 1 DDRAM Address

- **1-line display (N = 0) (Figure 2)**

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the RW1063, 8 characters are displayed. See Figure 3.
When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

Display Position (Digit)	1	2	3	4	5	6		78	79	80
DDRAM Address	00	01	02	03	04	05	………………..	4D	4E	4F

Figure 2 1-Line Display

Display Position	1	2	3	4	5	6	7	8
DDRAM Address	00	01	02	03	04	05	06	07
For Shift Left	01	02	03	04	05	06	07	08
For Shift Right	4F	00	01	02	03	04	05	06

Figure 3 1-Line by 8-Character Display Example

- **2-line display (N = 1) (Figure 4)**

Case 1: When the number of display characters is less than 40 x 2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the RW1063 is used, 8 characters x 2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

Display Position	1	2	3	4	5	6		38	39	40
DDRAM Address (hexadecimal)	00	01	02	03	04	05	………………..	25	26	27
	40	41	42	43	44	45	………………..	65	66	67

Figure 4 2-Lines Display

Display Position	1	2	3	4	5	6	7	8
DDRAM Address	00	01	02	03	04	05	06	07
	40	41	42	43	44	45	46	47
For Shift Left	01	02	03	04	05	06	07	08
	41	42	43	44	45	46	47	48
For Shift Right	27	00	01	02	03	04	05	06
	67	40	41	42	43	44	45	46

Figure 5 2-Lines by 8-Character Display Example

Case 2: For a 16-character x 2-line display, the RW1063 can be extended using one 40-output extension driver. See Figure 6.
When display shift operation is performed, the DDRAM address shifts. See Figure 6.

Figure 6 2-Lines by 16-Character Display Example

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
For Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

- **TIMING GENERATION CIRCUIT**

Timing generation circuit generates clock signals for the internal operations.

- **ADDRESS COUNTER (AC)**

Address Counter (AC) stores DDRAM/CGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0-DB6

- **CURSOR/BLINK CONTROL CIRCUIT**

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

- **LCD DRIVER CIRCUIT**

LCD Driver circuit has 16 common and 40 segment signals for 2-line display (N=1) or 8 common and 40 segments for 1-line display (N=0) for LCD driving.

Data from CGRAM/CGROM is transferred to 40 bit segment latches serially, and then it is stored to 40 bit shift latch.

- **CGROM (CHARACTER GENERATOR ROM)**

CGROM has 240 characters (5 x 8 dot)

- **CGRAM (CHARACTER GENERATOR RAM)**

CGRAM has up to 5 × 8 dots 8 characters. By writing font data to CGRAM, user defined character can be used (refer to Table 2).

- **5 x 8 dots Character Pattern**

Table 2. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	0	1	1	1	0	Pattern 1
-	-	-	-	-	0	0	0	-	-	-	0	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	0	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	0	1	1	-	-	-	1	1	1	1	1	
-	-	-	-	-	0	0	0	-	-	-	1	0	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	1	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	1	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	0	0	0	-	-	-	1	1	1	-	-	-	0	0	0	0	0	
				-					-			-						-				
				-					-			-						-				
0	0	0	0	0	1	1	1	1	1	1	0	0	0	X	X	X	1	0	0	0	1	Pattern 8
-	-	-	-	-	1	1	1	-	-	-	0	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	0	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	0	1	1	-	-	-	1	1	1	1	1	
-	-	-	-	-	1	1	1	-	-	-	1	0	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	1	0	1	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	1	1	0	-	-	-	1	0	0	0	1	
-	-	-	-	-	1	1	1	-	-	-	1	1	1	-	-	-	0	0	0	0	0	

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table 2, CGRAM character patterns are selected when character code bits 4 to 7 are all 0 and MW=0. However, since character code bit 3 has no effect, the H display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
   "-": Indicates no effect.

◆ INSTRUCTION DESCRIPTION

Instruction Table:

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Description Time (540KHz)
Read display data	1	1	Read data								Read data from DDRAM/CGRAM	18.5us
Write display data	1	0	Write data								Write data into DDRAM/CGRAM	18.5us
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM, and set DDRAM address to "00H" from AC	0.76ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	0.76ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and specify display shift. These operations are performed during data read and write. I/D="1": increment I/D="0": decrement	18.5us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Set Display /Cursor/Blink On/OFF D="1": display on D="0": display off C="1": cursor on C="0": cursor off B="1": blink on B="0": blink off	18.5us
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift S/C="1": display shift S/C="0": cursor shift R/L="1": shift to right R/L="0": shift to left	18.5us
Function Set	0	0	0	0	1	DL	N	F	X	X	Set Interface Data Length DL= 8-bit interface/ 4-bit interface N = 2-line/1-line display F= 5x8 Font Size / 5x11Font Size	18.5us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	18.5us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	18.5us
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can know internal operation is ready or not by reading BF. The contents of address counter can also be read. BF="1": busy state BF="0": ready state	0us

Note : 1. When an MPU program with Busy Flag(DB7) checking is made, 1/ 2 FOSC (is necessary) for executing the next instruction by the " E " signal after the Busy Flag (DB7) goes to " Low ".

2. "X" Don't care

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status; namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	x

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. A content of DDRAM does not change.

Entry Mode Set:

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

I/D: Increment/decrement of DDRAM address (cursor or blink)
I/D = 1: cursor/blink moves to right and DDRAM address is increased by 1.
I/D = 0: cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read/write from or to CGRAM

S: Shift of entire display
When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed.
If S= "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1": shift left, I/D = "0": shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

Display ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: **Display ON/OFF control bit.**
D = 1: entire display is turned on.
D = 0: display is turned off, but display data is remained in DDRAM.

C: **Cursor ON/OFF control bit.**
C = 1: cursor is turned on.
C = 0: cursor is disappeared in current display, but I/D register remains its data.

B: **Cursor Blink ON/OFF control bit.**
B = 1: cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 540 kHz frequency, blinking has 185 ms interval.
B = 0: blink is off.

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to Table 4). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
Note that display shift is performed simultaneously by the shift enable instruction. When displayed data is shifted repeatedly, all display lines shifted simultaneously. When display shift is performed, the contents of address counter are not changed.

Table 4. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	X	X

DL: Interface data length control bit

When DL = "High", it means 8-bit bus mode with MPU.

When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data by two times.

IF using IIC and 4-SPI interface、DL bit must be setting to “1”

N: Display line number control bit

When N = "Low", it means 1-line display mode.

When N = "High", 2-line display mode is set.

F: Display font type control bit

When F = "Low", it means 5 x 8 dots format display mode

When F = "High", 5 x11 dots format display mode.

N	F	No. of Display Lines	Character Font	Duty Factor
L	L	1	5x8	1/8
L	H	1	5x11	1/11
H	x	2	5x8	1/16

Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.
When 1-line display mode (N=0), DDRAM address is from “00H” to “4FH”
In 2-line display mode (NW = 0), DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H".

- **Read Busy Flag and Address** (only support parallel 8-bit bus and 4 bit bus)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether RW1063 is in internal operation or not. If the resultant BF is “high”, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

- **Write Data to RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction:
DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

- **Read Data from RAM** (only support parallel 8-bit bus and 4 bit bus)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined.
If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction: it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

● OUTLINE

To overcome the speed difference between internal clock of RW1063 and MPU clock, RW1063 performs internal operation by storing control information to IR (Instruction Register) or DR (data Register).
The internal operation is determined according to the signal from MPU, composed of read/write and data bus.

Instruction can be divided largely four kinds;

- RW1063 function set instructions (set display methods, set data length, etc.)
- Address set instructions to internal RAM
- Data transfer instructions with internal RAM
- Others

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read high. Busy Flag check must be preceded the next instruction.
Busy flag check must be proceeded the next instruction.
When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc (is necessary) for executing the next instruction by the falling edge of the "E" signal after the Busy Flag (DB7) goes to "Low".

◆ INTERFACE WITH MPU

RW1063 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU.
In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.

- When interfacing data lengths are 4-bit, only 4 ports, from DB4 - DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4- bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended.

- When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 - DB7.

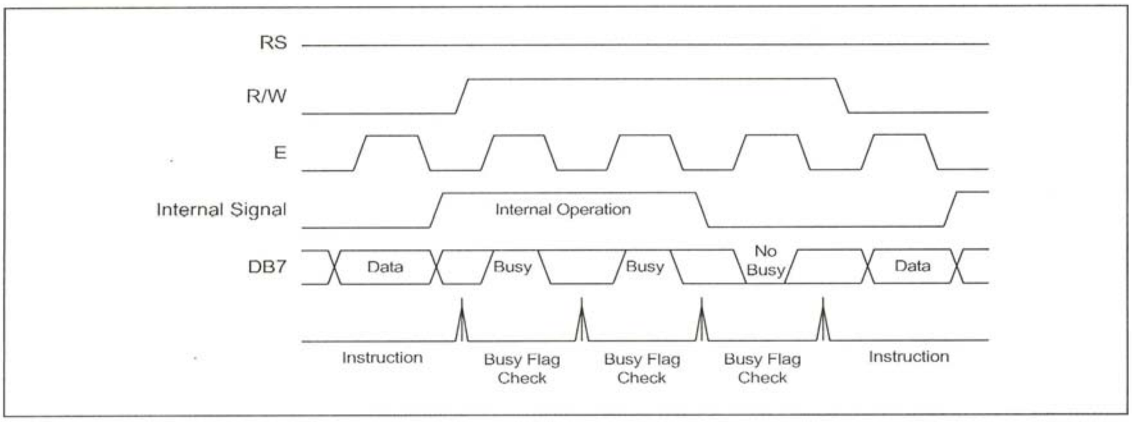
- Interface is selected by IF1,IF0 pins (refer to **Bonding Note for IF1, IF0** on Page 10)

IF1	IF0	Interface select
open	open	6800 8/4 bit
open	Bonding to VDD	IIC
Bonding to VDD	open	4-line SPI

◆ INTERFACE WITH MPU IN BUS MODE

● Interface with 8-bit MPU

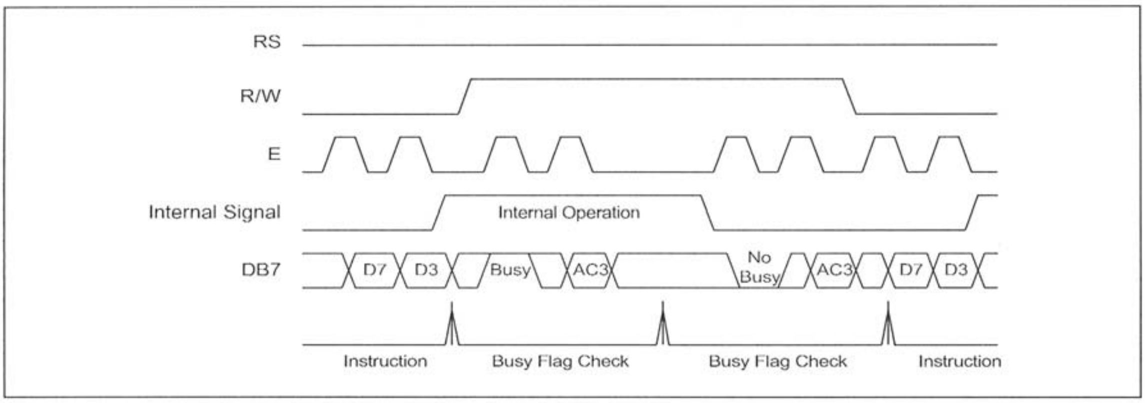
If 8-bits MPU is used, RW1063 can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.


RS
R/W
E
Internal Signal
Internal Operation
DB7
Data
Busy
Busy
No Busy
Data
Instruction
Busy Flag Check
Busy Flag Check
Busy Flag Check
Instruction

Example of 8-bit Bus Mode Timing Sequence

● Interface with 4-bit MPU

If 4-bit MPU is used, RW1063 can connect directly with this. In this case, port E, RS, R/W and DB4 - DB7 need to interface each other. The transfer is performed by two times. Example of timing sequence is shown below.

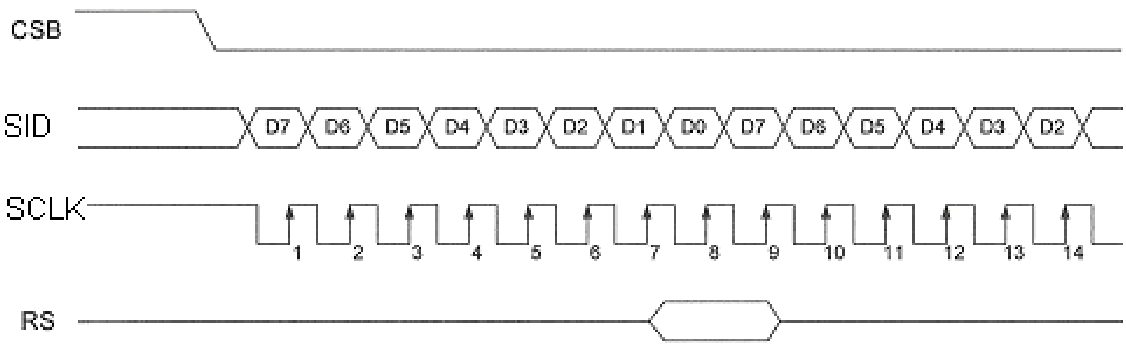

RS
R/W
E
Internal Signal
Internal Operation
DB7
D7
D3
Busy
AC3
No Busy
AC3
D7
D3
Instruction
Busy Flag Check
Busy Flag Check
Instruction

Example of 4-bit Bus Mode Timing Sequence

For serial interface data, bus lines (DB5 to DB7) are used. 4-Line SPI

If 4-Pin SPI mode is used, CSB (DB5), SID (DB7), SCLK (DB6), and RS are used. They are chip selection; serial input data, serial clock input, and data/instruction section, relatively. The example of timing sequence is shown below.

➢ Example of timing sequence


CSB
SID
D7
D6
D5
D4
D3
D2
D1
D0
D7
D6
D5
D4
D3
D2
SCLK
1
2
3
4
5
6
7
8
9
10
11
12
13
14
RS

Note: Following is the master SPI clock mode of MPU.
Idle state for clock is a high level，data transmitted on rising edge of SCLK, and data is hold during low level.

■ For serial interface data, bus lines (DB5(CSB)、DB6(SDA) and DB7(SCL)) are used. IIC interface

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules. Serial data line SDA (DB6) and a Serial clock line SCL (DB7) must be connected to a positive supply via a pull-up resistor.
Data transfer may be initiated only when the bus is not busy.
*The CSB (DB5) Pin must be setting to “VSS”.
* When IIC interface is selected, the DL register must be set to “1”.

➢ BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.9.1

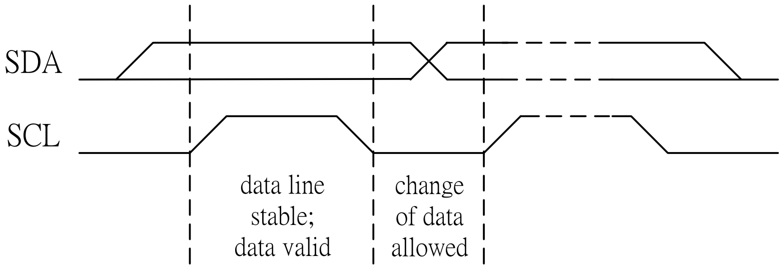


Fig .9.1 Bit transfer

➢ START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.9.2

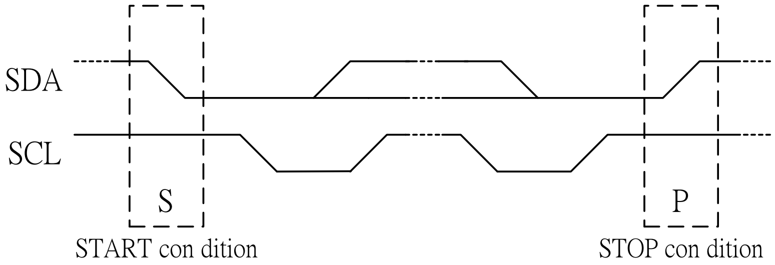


Fig .9.2 Definition of START and STOP conditions

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.9.3
· Transmitter: the device, which sends the data to the bus
· Receiver: the device, which receives the data from the bus
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer
· Slave: the device addressed by a master
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
· Synchronization: procedure to synchronize the clock signals of two or more devices.

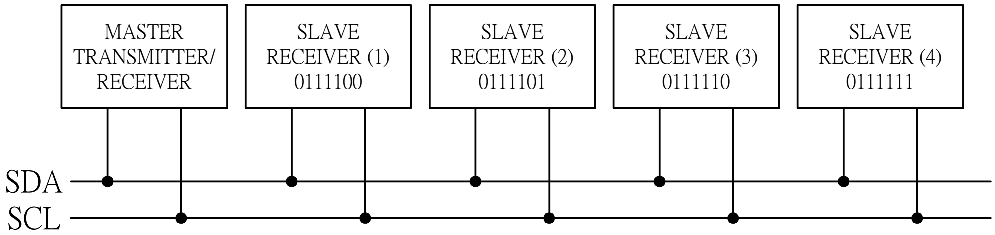

MASTER TRANSMITTER/ RECEIVER
SLAVE RECEIVER (1) 0111100
SLAVE RECEIVER (2) 0111101
SLAVE RECEIVER (3) 0111110
SLAVE RECEIVER (4) 0111111
SDA
SCL

Fig .9.3 System configuration

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge after the reception of each byte. A master receiver must also generate an Acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the Acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an Acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Fig.9.4

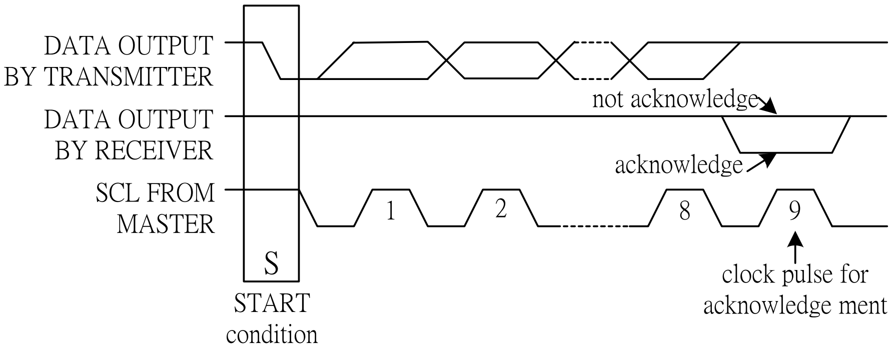

DATA OUTPUT BY TRANSMITTER
DATA OUTPUT BY RECEIVER
SCL FROM MASTER
not acknowledge
acknowledge
1
2
8
9
S
START condition
clock pulse for acknowledge ment

Fig .9.4 Acknowledgement on the 2-line Interface

➢ IIC Interface protocol

The RW1063 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first.
Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the RW1063. The least significant bit of the slave address is set by connecting the input SA0 (DB0) and SA1 (DB1) to either logic 0 (VSS) or logic 1 (VDD).
The IIC Interface protocol is illustrated in Figure.9.5
The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1063 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC interface-bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

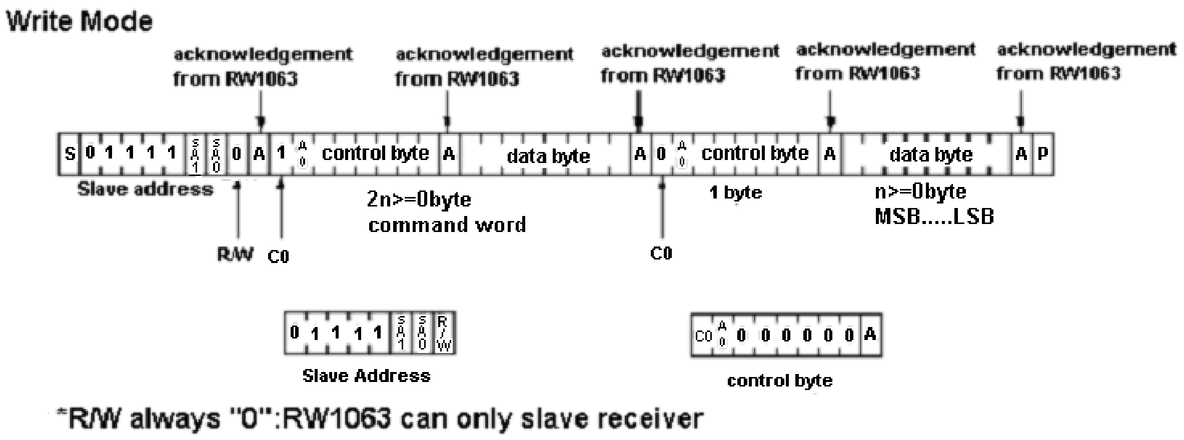

Write Mode
acknowledgement from RW1063
acknowledgement from RW1063
acknowledgement from RW1063
acknowledgement from RW1063
acknowledgement from RW1063
S 0 1 1 1 1 SA1 SA0 0 A 1 A0 control byte A data byte A 0 A0 control byte A data byte A P
Slave address
2n>=0byte
command word
1 byte
n>=0byte
MSB.....LSB
R/W C0
C0
0 1 1 1 1 SA1 SA0 R/W
Slave Address
C0 A0 0 0 0 0 0 0 A
control byte
*R/W always "0":RW1063 can only slave receiver

Fig .9.5 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

◆ INITIALIZING

● INITIALIZING BY INTERNAL RESET CIRCUIT

When the power is turned on, RW1063 is initialized automatically by power on reset circuit.
During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High"(busy state) to the end of initialization.

● Clear Display Instruction

Write "20H" to all DDRAM

● Set Functions Instruction

DL = 1: 8-bit bus mode
N = 0: 1-line display
F = 0: 5 x 8 dot character font

● Display ON/OFF Instruction

D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Blink OFF

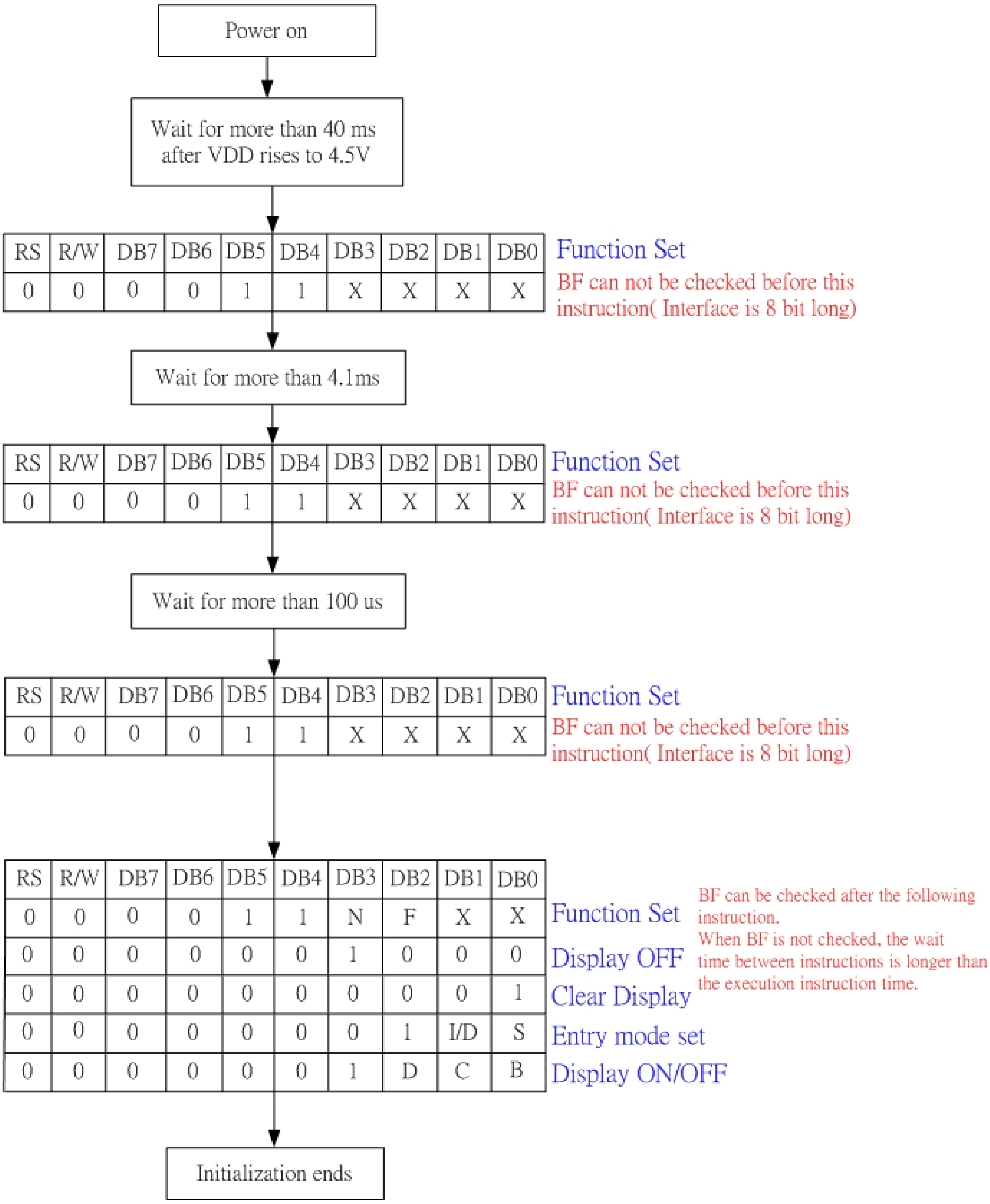
● Set Entry Mode Instruction

I/D = 1: Increment by 1
S = 0: No entire display shift

Note:
If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the RW1063. For such a case, initialization must be performed by the MPU as explain by the following figure.

◆ INITIALIZING BY INSTRUCTION

- **8 bit interface (Fosc=540KHz)**


Power on
Wait for more than 40 ms after VDD rises to 4.5V
Wait for more than 4.1ms
Wait for more than 100 us
Initialization ends

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X

Function Set
BF can not be checked before this instruction(Interface is 8 bit long)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X

Function Set
BF can not be checked before this instruction(Interface is 8 bit long)

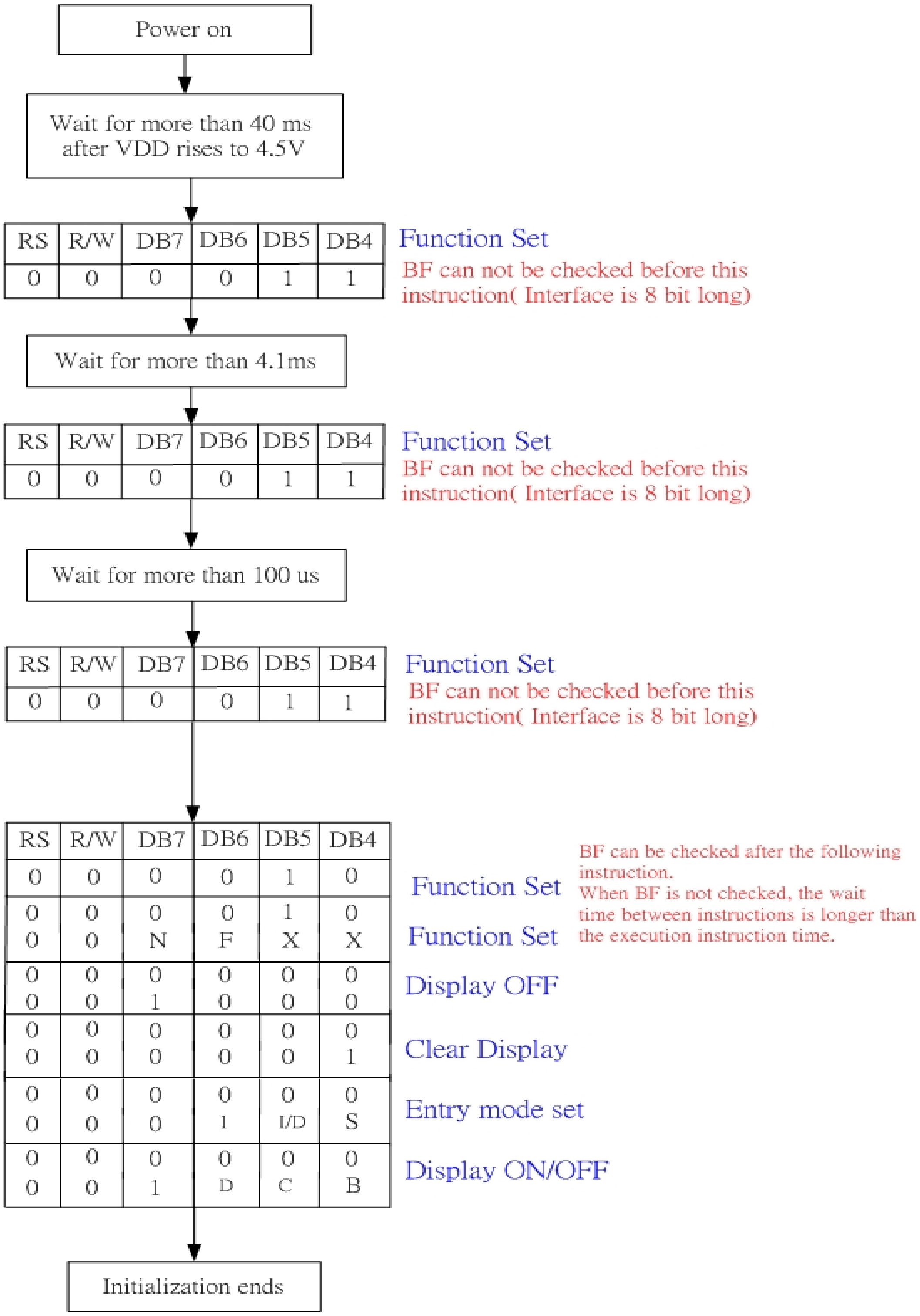
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X

Function Set
BF can not be checked before this instruction(Interface is 8 bit long)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	1	1	N	F	X	X	Function Set
0	0	0	0	0	0	1	0	0	0	Display OFF
0	0	0	0	0	0	0	0	0	1	Clear Display
0	0	0	0	0	0	0	1	I/D	S	Entry mode set
0	0	0	0	0	0	1	D	C	B	Display ON/OFF

BF can be checked after the following instruction.
When BF is not checked, the wait time between instructions is longer than the execution instruction time.

- **4 bit interface (Fosc=540KHz)**



Power on

Wait for more than 40 ms after VDD rises to 4.5V

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

Function Set
BF can not be checked before this instruction(Interface is 8 bit long)

Wait for more than 4.1ms

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

Function Set
BF can not be checked before this instruction(Interface is 8 bit long)

Wait for more than 100 us

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

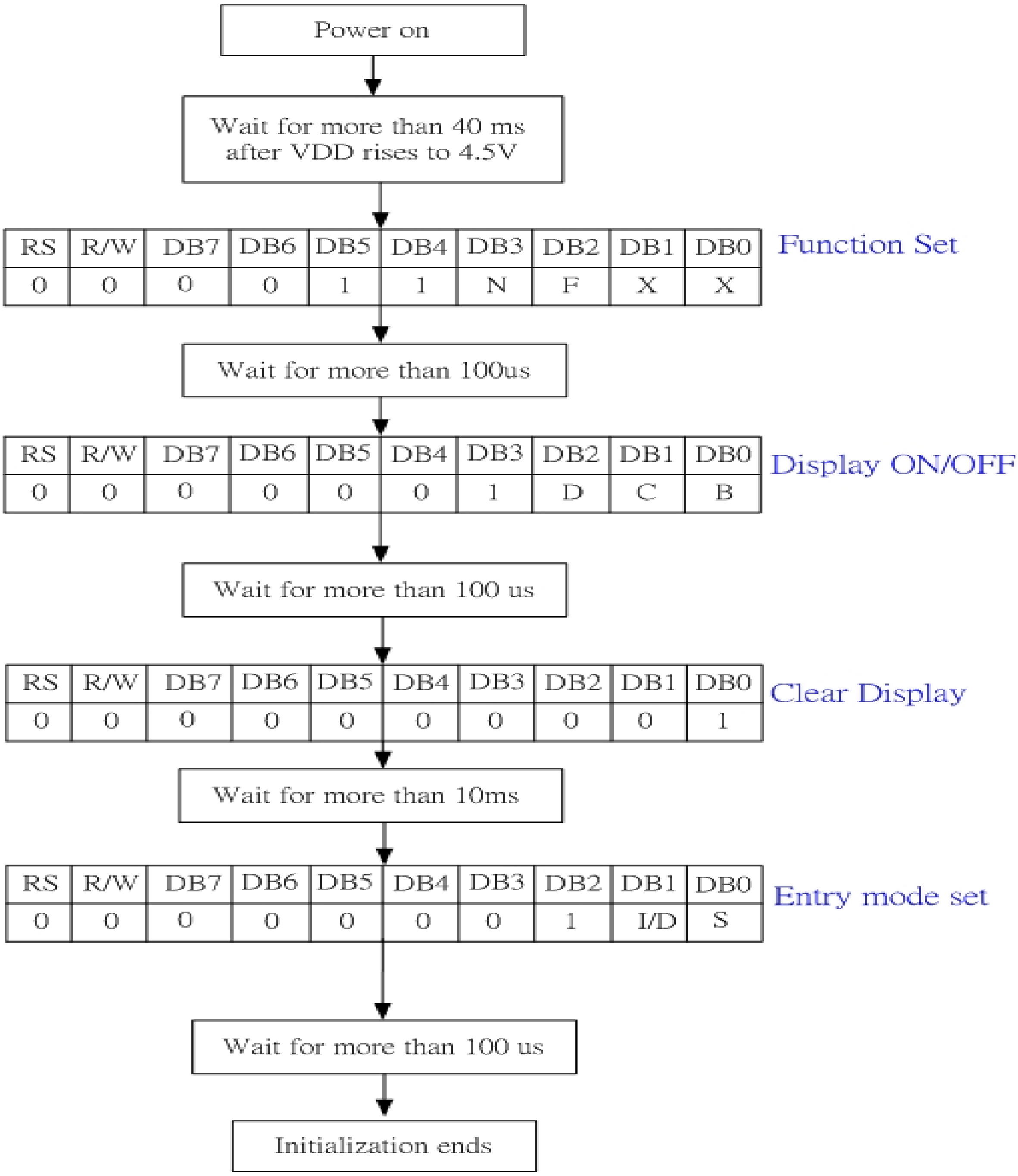
Function Set
BF can not be checked before this instruction(Interface is 8 bit long)

RS	R/W	DB7	DB6	DB5	DB4	
0	0	0	0	1	0	Function Set
0 0	0 0	0 N	0 F	1 X	0 X	Function Set
0 0	0 0	0 1	0 0	0 0	0 0	Display OFF
0 0	0 0	0 0	0 0	0 0	0 1	Clear Display
0 0	0 0	0 0	0 1	0 I/D	0 S	Entry mode set
0 0	0 0	0 1	0 D	0 C	0 B	Display ON/OFF

BF can be checked after the following instruction.
When BF is not checked, the wait time between instructions is longer than the execution instruction time.

Initialization ends

- **Serial Interfaceode(Fosc=540KHz)**


Power on
Wait for more than 40 ms after VDD rises to 4.5V

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	X	X

Wait for more than 100us

Display ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Wait for more than 100 us

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Wait for more than 10ms

Entry mode set

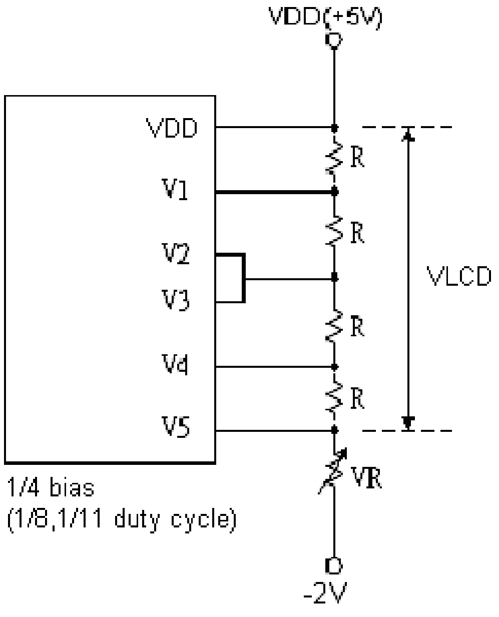
RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

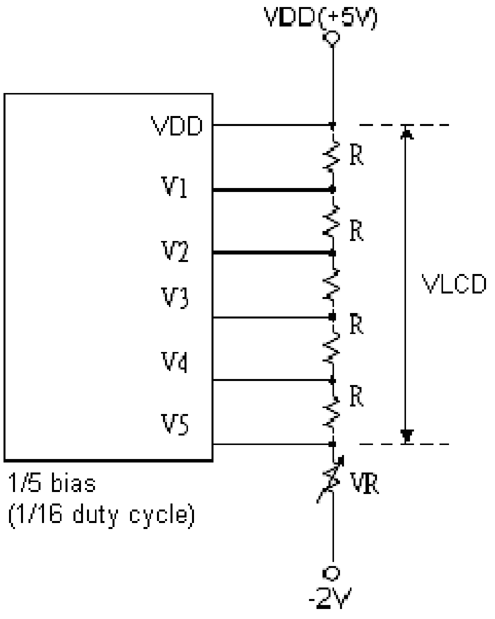
Wait for more than 100 us
Initialization ends

◆ Supply Voltage for LCD Drive

There are different voltages that supply to RW1063's pin (V1 - V5) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as below:

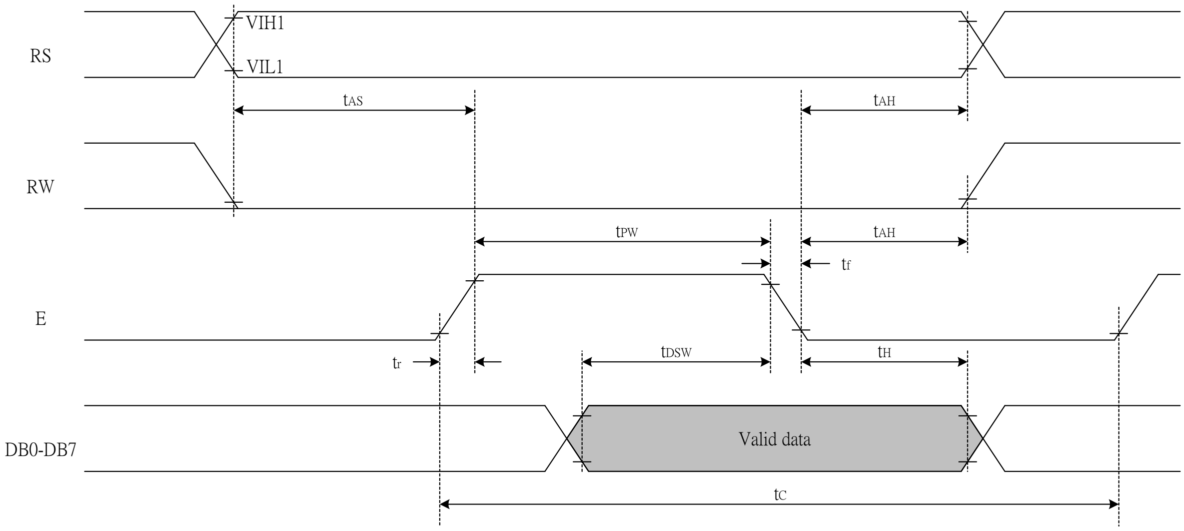
	Duty Factor	
	1/8, 1/11	1/16
	Bias	
Supply Voltage	1/4	1/5
V1	VDD - 1/4VLCD	VDD - 1/5VLCD
V2	VDD - 1/2VLCD	VDD - 2/5VLCD
V3	VDD - 1/2VLCD	VDD - 3/5VLCD
V4	VDD - 3/4VLCD	VDD - 4/5VLCD
V5	VDD - VLCD	VDD - VLCD


VDD(+5V)
VDD
V1
V2
V3
V4
V5
R
R
R
R
VLCD
VR
-2V
1/4 bias
(1/8,1/11 duty cycle)

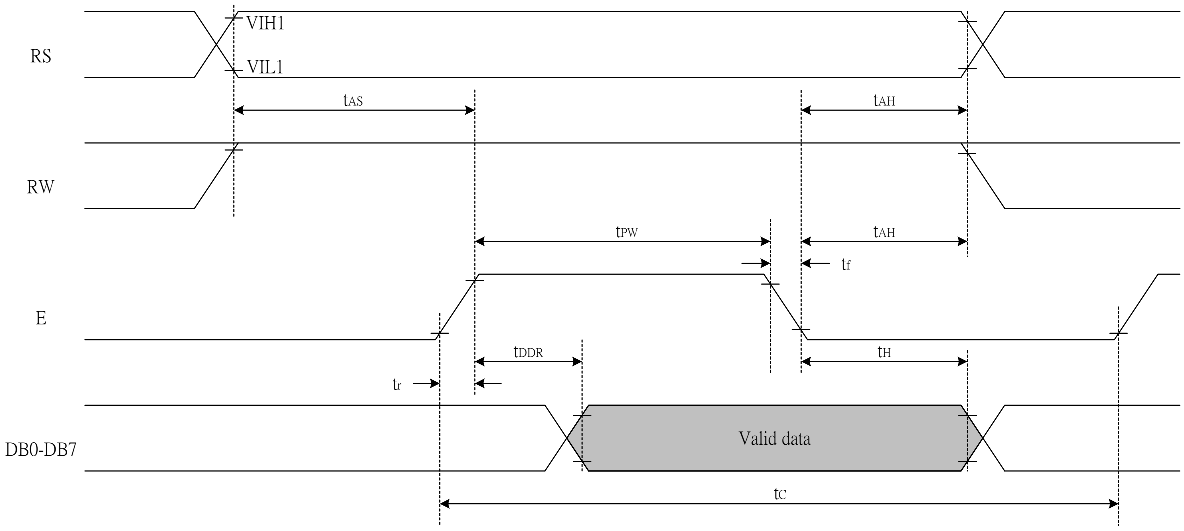

VDD(+5V)
VDD
V1
V2
V3
V4
V5
R
R
R
R
VLCD
VR
-2V
1/5 bias
(1/16 duty cycle)

◆ Timing Characteristics

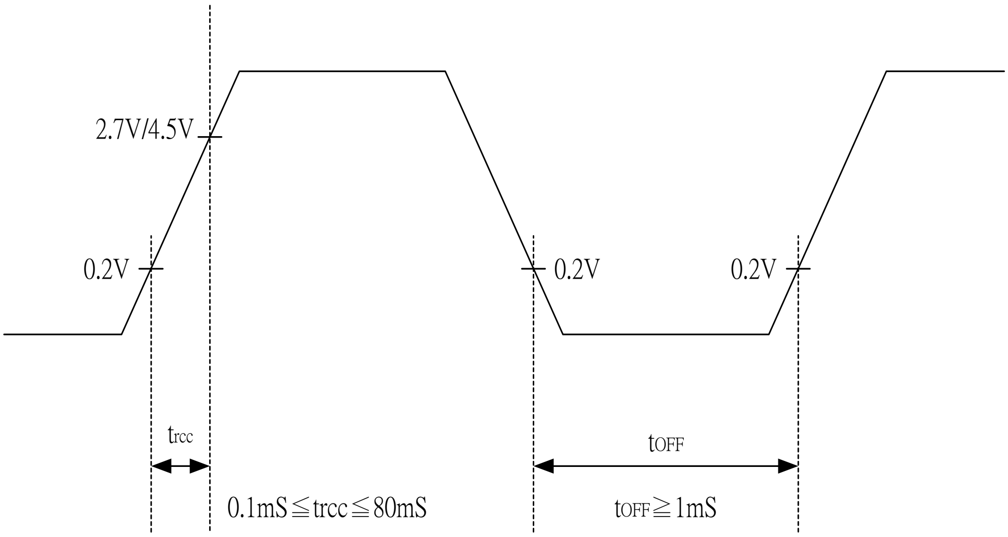
- **Writing data from MPU to RW1063 (Parallel 8-bit bus and 4-bit bus)**


RS
VIH1
VIL1
tAS
tAH
RW
tPW
tAH
tf
E
tr
tDSW
tH
DB0-DB7
Valid data
tC

- **Reading data from RW1063 to MPU(Parallel 8-bit bus and 4-bit bus)**


RS
VIH1
VIL1
tAS
tAH
RW
tPW
tAH
tf
E
tDDR
tH
tr
DB0-DB7
Valid data
tC

- **Internal Power Supply Reset**


2.7V/4.5V
0.2V
0.2V
0.2V
trcc
tOFF
0.1mS≦trcc≦80mS
tOFF≧1mS

Notes:

- ■ tOFF compensates for the power oscillation period caused by momentary power supply oscillations.
- ■ Specified at 4.5V for 5V operation,and at 2.7V for 3V operation.
- ■ For if 4.5V is not reached during 5V operation,teh internal reset circuit will not operate normally.

◆ AC Characteristics

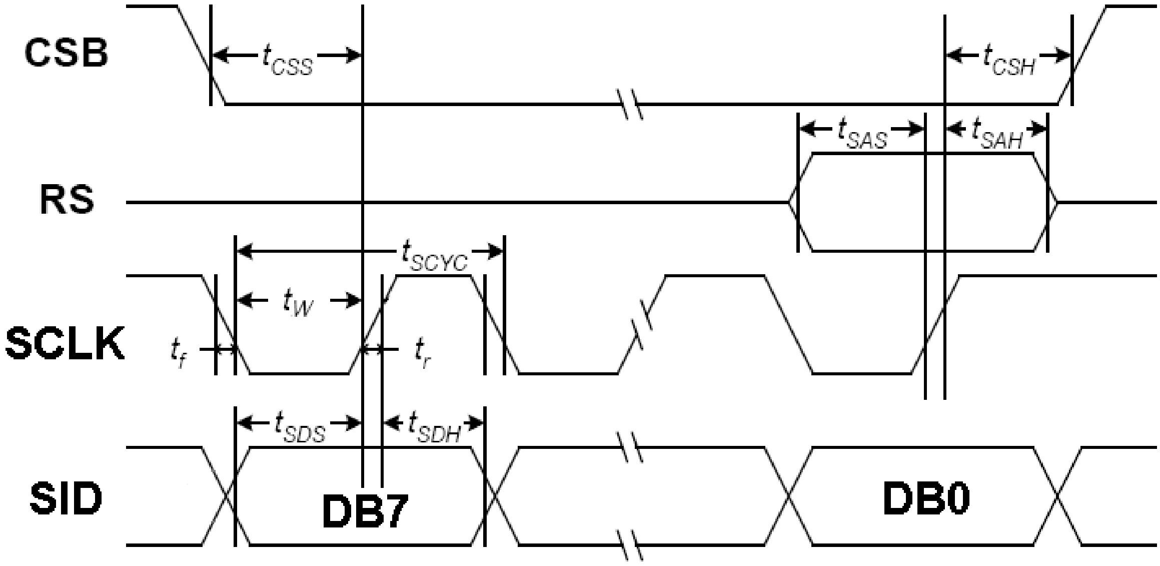
In 6800 interface (TA = 25℃, VDD = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	RF=75K	380	540	700	KHz
External Clock Operation						
f_{EX}	External Frequency	-	380	540	700	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	µs
Write Mode (Writing data from MPU to RW1063)						
T_C	Enable Cycle Time	Pin E (except clear display)	1000	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	450	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	60	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	195	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from RW1063 to MPU)						
T_C	Enable Cycle Time	Pin E	1000	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	450	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	25	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	60	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	360	ns
T_H	Data Hold Time	Pins: DB0 - DB7	5	-	-	ns

In 6800 interface (TA = 25℃, VDD = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Internal Clock Operation						
f_{OSC}	OSC Frequency	RF=91K	380	540	700	KHz
External Clock Operation						
f_{EX}	External Frequency	-	380	540	700	KHz
	Duty Cycle	-	45	50	55	%
T_R,T_F	Rise/Fall Time	-	-	-	0.2	µs
Write Mode (Writing data from MPU to RW1063)						
T_C	Enable Cycle Time	Pin E (except clear display)	500	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	230	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	20	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	40	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DSW}	Data Setup Time	Pins: DB0 - DB7	80	-	-	ns
T_H	Data Hold Time	Pins: DB0 - DB7	10	-	-	ns
Read Mode (Reading Data from RW1063 to MPU)						
T_C	Enable Cycle Time	Pin E	500	-	-	ns
T_{PW}	Enable Pulse Width	Pin E	230	-	-	ns
T_R,T_F	Enable Rise/Fall Time	Pin E	-	-	20	ns
T_{AS}	Address Setup Time	Pins: RS,RW,E	40	-	-	ns
T_{AH}	Address Hold Time	Pins: RS,RW,E	10	-	-	ns
T_{DDR}	Data Setup Time	Pins: DB0 - DB7	-	-	120	ns
T_H	Data Hold Time	Pins: DB0 - DB7	5	-	-	ns

- **Serial interface timing (4-SPI)**


CSB
RS
SCLK
SID
t_{CSS}
t_{CSH}
t_{SAS}
t_{SAH}
t_{SCYC}
t_W
t_f
t_r
t_{SDS}
t_{SDH}
DB7
DB0

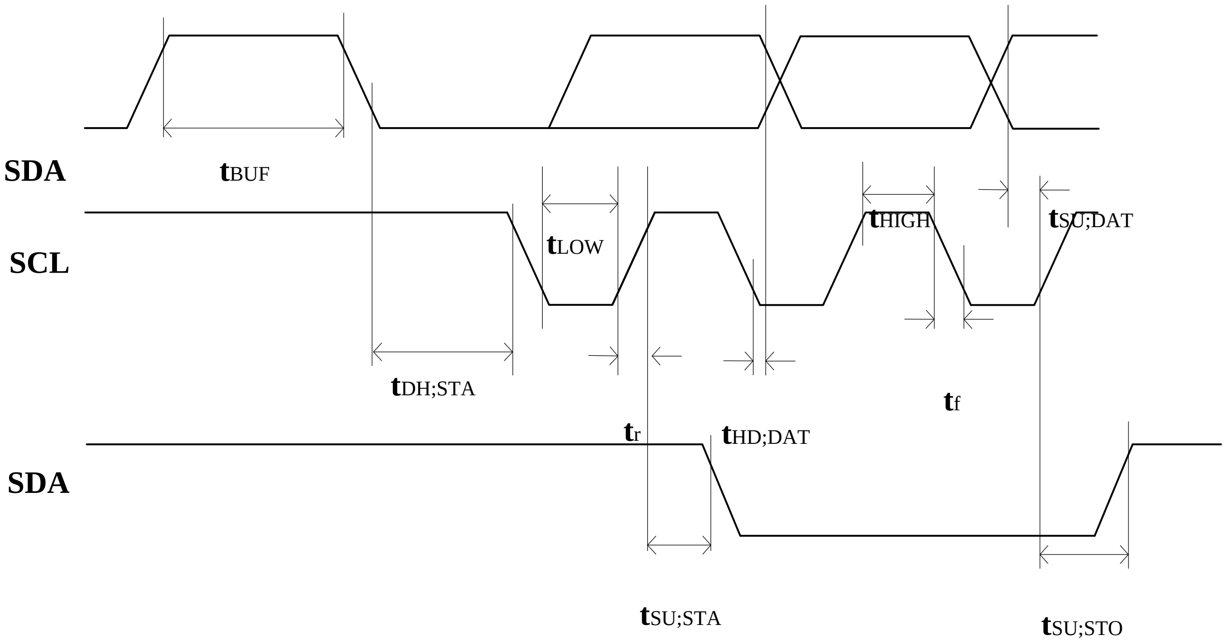
In 4-SPI Serial Interface (TA = 25℃, VCC = 2.7V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Write Mode (Writing data from MPU to RW1063)						
t_{SCYC}	SCLK Cycle Time	SCLK	640	-	-	ns
t_w	SCLK pulse width	SCLK	320	-	-	ns
t_R,t_F	SCLK Rise/Fall time	SCLK	-	-	25	ns
t_{SAS}	Address Setup time	RS	120	-	-	ns
t_{SAH}	Address Hold time	RS	80	-	-	ns
t_{SDS}	Data setup time	SID	160	--	-	ns
t_{SDH}	Data hold time	SID	80	-	-	ns
t_{CSS}	CSB Setup Time	CSB	160			ns
t_{CSH}	CSB Hold Time	CSB	240			ns

In 4-SPI Serial Interface (TA = 25℃, VCC = 5V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Write Mode (Writing data from MPU to RW1063)						
t_{SCYC}	SCLK Cycle Time	SCLK	480	-	-	ns
t_w	SCLK pulse width	SCLK	240	-	-	ns
t_R,t_F	SCLK Rise/Fall time	SCLK	-	-	25	ns
t_{SAS}	Address Setup time	RS	80	-	-	ns
t_{SAH}	Address Hold time	RS	40	-	-	ns
t_{SDS}	Data setup time	SID	40	--	-	ns
t_{SDH}	Data hold time	SID	40	-	-	ns
t_{CSS}	CSB Setup Time	CSB	20			ns
t_{CSH}	CSB Hold Time	CSB	160			ns

◆ IIC interface timing



(Ta = 25°C)

Item	Signal	Symbol	Condition	VDD=2.7V		VDD=5V		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SDA	$t_{SU;DAT}$	—	180	–	80	–	ns
Data hold time		$t_{HD:DAT}$		0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	$20+0.1C_b$	300	$20+0.1C_b$	300	ns
SCL,SDA fall time		t_f		$20+0.1C_b$	300	$20+0.1C_b$	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	us

◆ Absolute Maximum Ratings

Characteristics	Symbol	Value
Power Supply Voltage	V_{DD}	-0.3 to +5.5
LCD Driver Voltage	V_{LCD}	Vss+7.0 to Vss-0.3
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3
Operating Temperature	T_A	-40°C to + 90°C
Storage Temperature	T_{STO}	-55°C to + 125°C

◆ DC Characteristics

(TA = 25℃ , VDD = 2.7 V – 4.5 V)

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	2.7	-	4.5	V
V_{LCD}	LCD Voltage	V_{DD} – V5	3.0	-	7.0	V
I_{DD}	Power Supply Current	f_{OSC} =540KHz V_{DD}=3.0V,RF=75K	-	0.25	0.45	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	0.7V_{DD}	-	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	- 0.3	-	0.6	V
V_{IH2}	Input High Voltage (OSC1)	-	0.7V_{DD}	-	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2V_{DD}	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	0.75 V_{DD}	-	-	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.2V_{DD}	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.8V_{DD}	-	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.2V_{DD}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-1	-	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 3V	10	60	120	µA

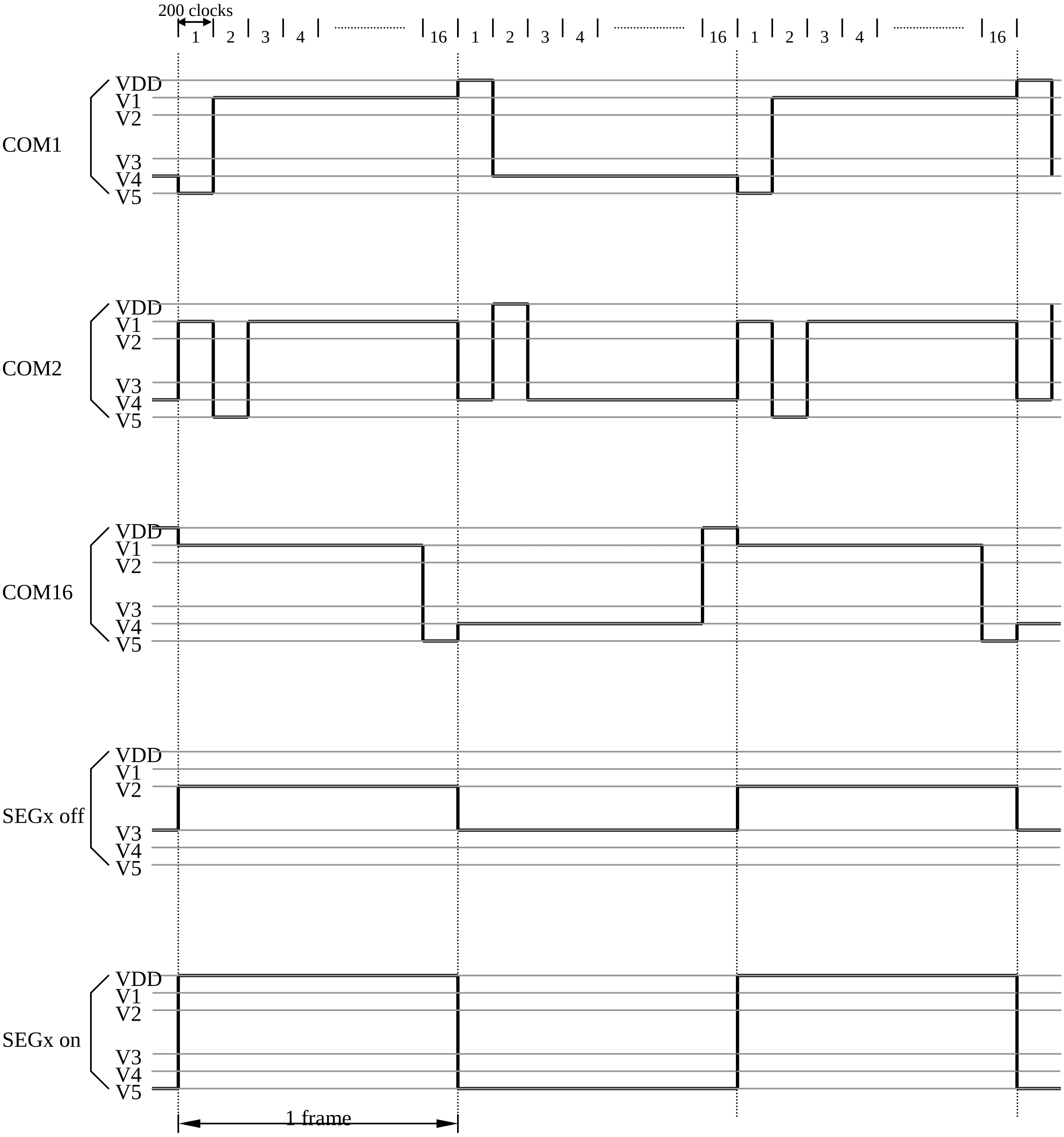
◆ DC Characteristics

(TA = 25℃, V_{DD}= 4.5 V - 5.5 V)

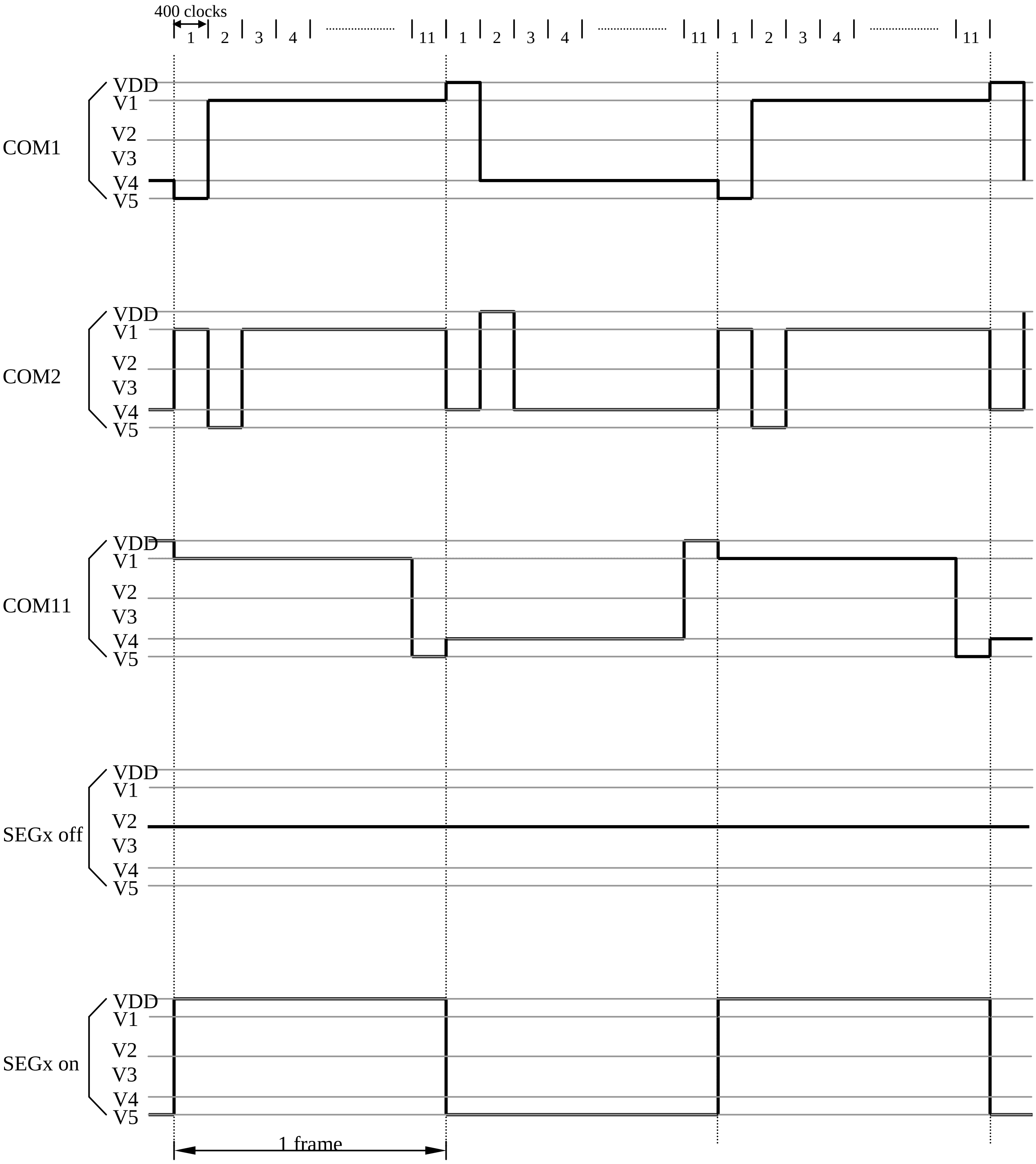
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	-	4.5	-	5.5	V
V_{LCD}	LCD Voltage	V_{DD} – V5	3.0	-	7.0	V
I_{DD}	Power Supply Current	f_{OSC} = 540KHz V_{DD}=5.0V,RF=91K	-	0.35	0.55	mA
V_{IH1}	Input High Voltage (Except OSC1)	-	2.5	-	V_{DD}	V
V_{IL1}	Input Low Voltage (Except OSC1)	-	-0.3	-	0.55	V
V_{IH2}	Input High Voltage (OSC1)	-	V_{DD}-1	-	V_{DD}	V
V_{IL2}	Input Low Voltage (OSC1)	-	-	-	0.2 V_{DD}	V
V_{OH1}	Output High Voltage (DB0 - DB7)	I_{OH} = -0.1mA	3.9	-	V_{DD}	V
V_{OL1}	Output Low Voltage (DB0 - DB7)	I_{OL} = 0.1mA	-	-	0.4	V
V_{OH2}	Output High Voltage (Except DB0 - DB7)	I_{OH} = -0.04mA	0.9V_{DD}	-	V_{DD}	V
V_{OL2}	Output Low Voltage (Except DB0 - DB7)	I_{OL} = 0.04mA	-	-	0.1V_{DD}	V
R_{COM}	Common Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	20	KΩ
R_{SEG}	Segment Resistance	V_{LCD} = 4V, I_d = 0.05mA	-	2	30	KΩ
I_{LEAK}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-1	-	1	µA
I_{PUP}	Pull Up MOS Current	V_{DD} = 5V	90	200	330	µA

◆ LCD Frame Frequency

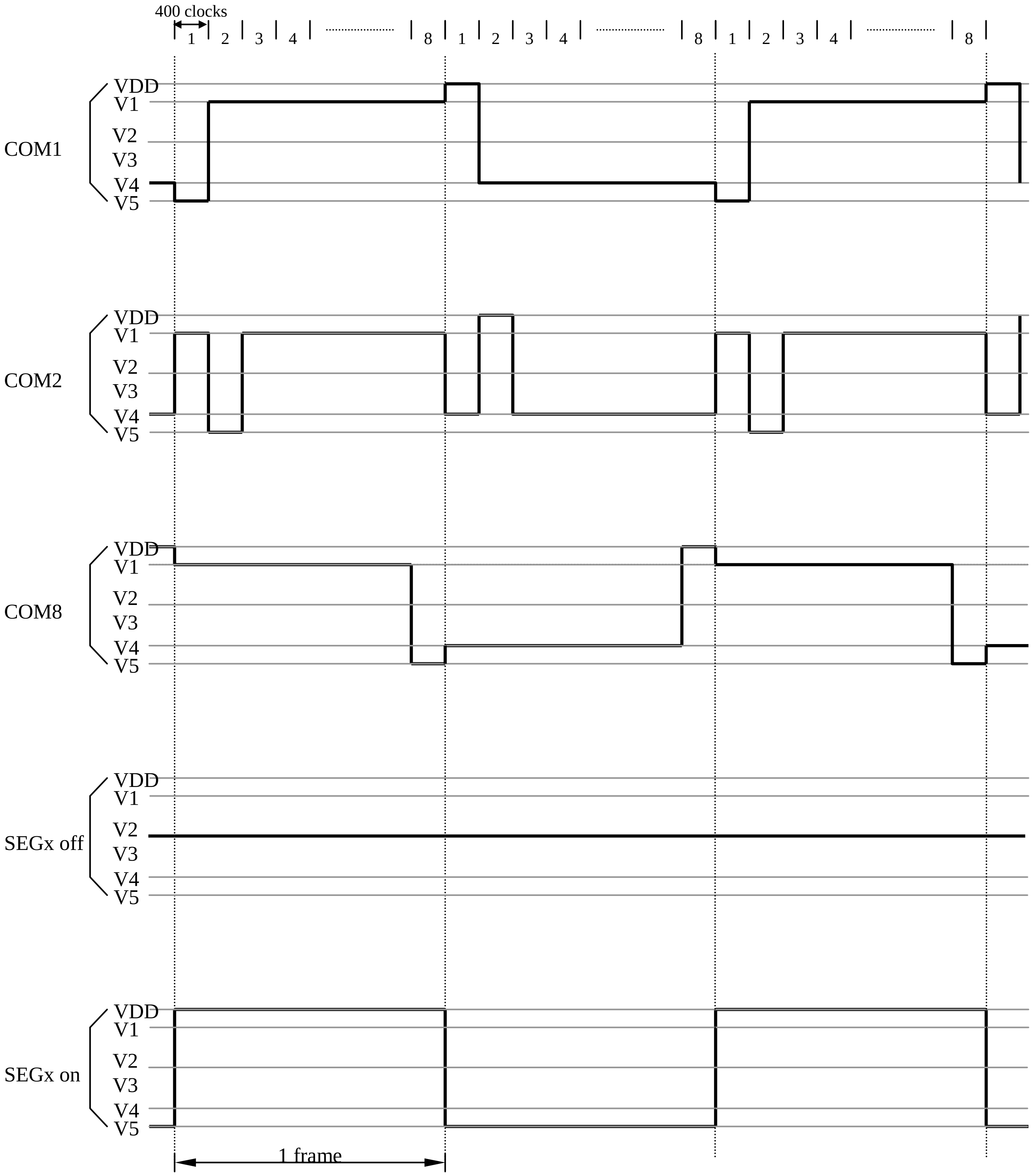
- **Assume the oscillation frequency is 540KHz, 1 clock cycle time = 1.85us, 1/16 duty; 1/5 bias, 1 frame = 1.85us x 200 x 16 = 5920us=5.92ms (168.9Hz)**


200 clocks
1
2
3
4
16
1
2
3
4
16
1
2
3
4
16
COM1
COM2
COM16
SEGx off
SEGx on
VDD
V1
V2
V3
V4
V5
1 frame

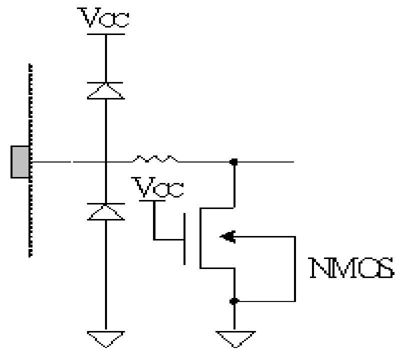
- **Assume the oscillation frequency is 540KHz, 1 clock cycle time = 1.85us, 1/11 duty; 1/4 bias, 1 frame = 1.85us x 400 x 11 = 8140us=8.14ms (122.8Hz)**


400 clocks
1
2
3
4
11
COM1
COM2
COM11
SEGx off
SEGx on
VDD
V1
V2
V3
V4
V5
1 frame

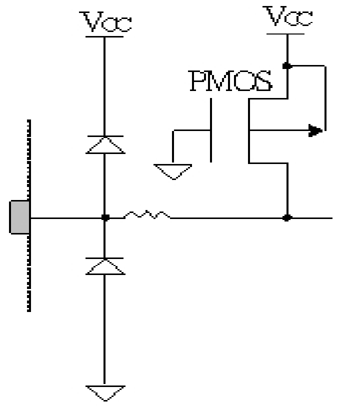
- **Assume the oscillation frequency is 540KHz, 1 clock cycle time = 1.85us, 1/8 duty; 1/4 bias, 1 frame = 1.85us x 400 x 8 = 5920us=5.92ms (168.9Hz)**


400 clocks
1
2
3
4
8
1
2
3
4
8
1
2
3
4
8
COM1
VDD
V1
V2
V3
V4
V5
COM2
VDD
V1
V2
V3
V4
V5
COM8
VDD
V1
V2
V3
V4
V5
SEGx off
VDD
V1
V2
V3
V4
V5
SEGx on
VDD
V1
V2
V3
V4
V5
1 frame

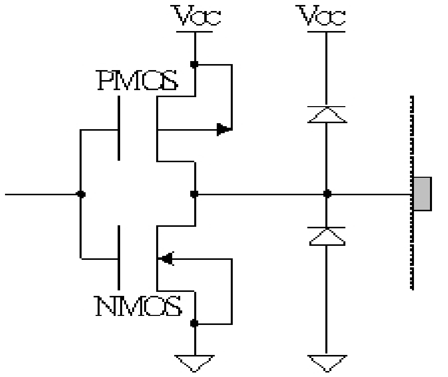
◆ I/O Pad Configuration


Vcc
Vcc
NMOS

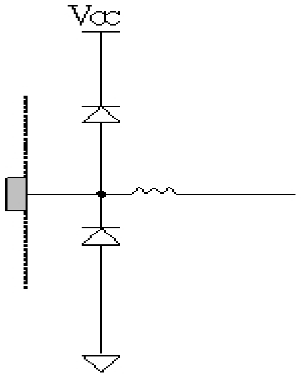
Input PAD:E
(with Pull-down in Serial interface)


Vcc
Vcc
PMOS

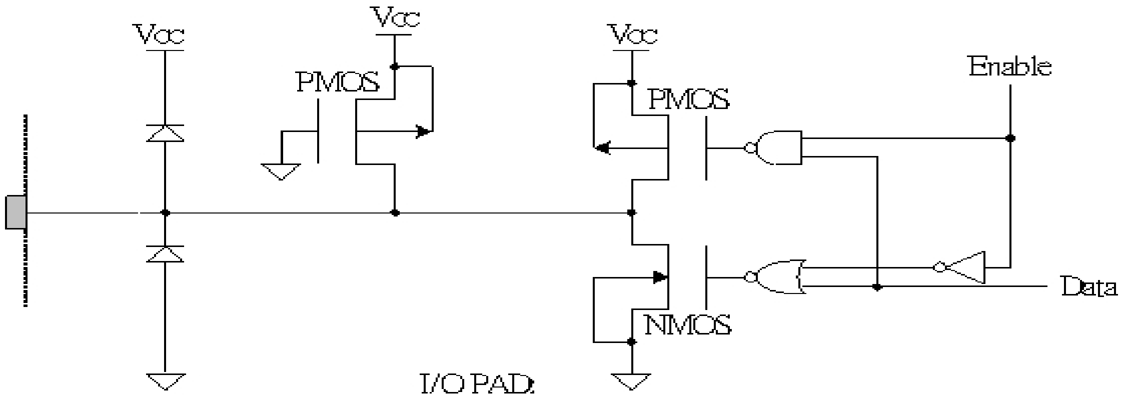
Input PAD:RW(with Pull-up)
RS(with Pull-up in parallel and IIC interface)


Vcc
Vcc
PMOS
NMOS

Output PAD:CL1,CL2,M,D



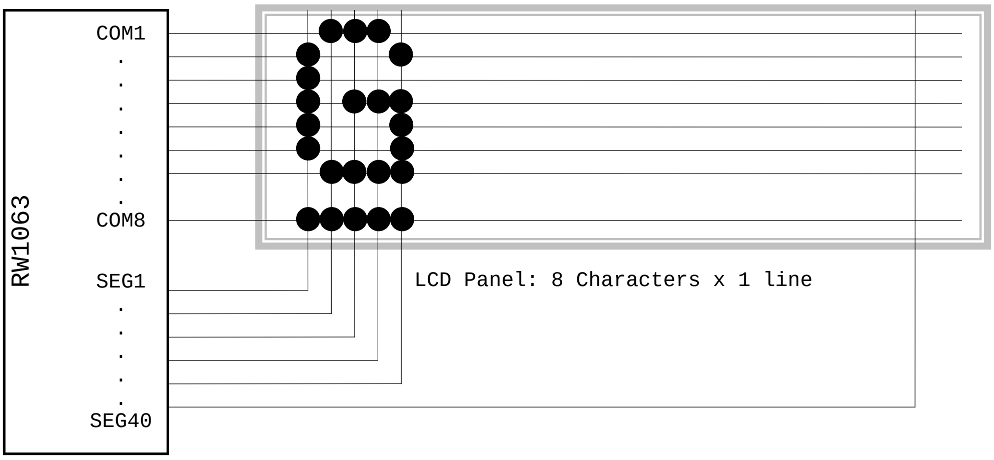
Input PAD:IF0,IF1


Vcc
Vcc
PMOS
Vcc
PMOS
Enable
NMOS
Data

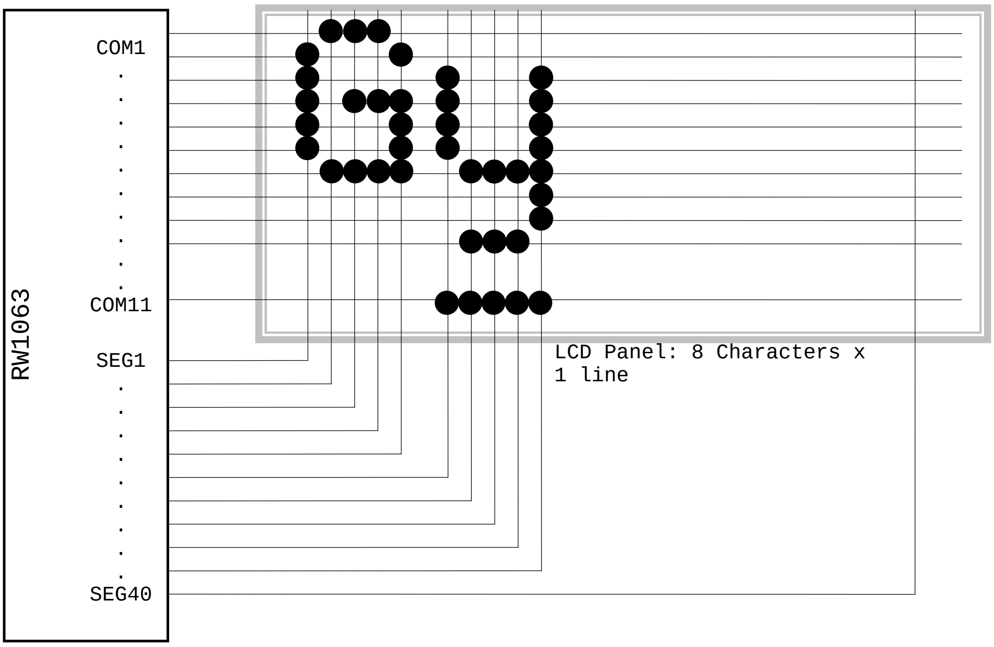
I/O PAD:
DB0-DB7 with Pull-up in parallel interface
D2,D3,D4,D5 with Pull-up in IIC interface
D0~D4 with Pull-up in 4SPI interface

◆ **LCD and RW1063 Connection**

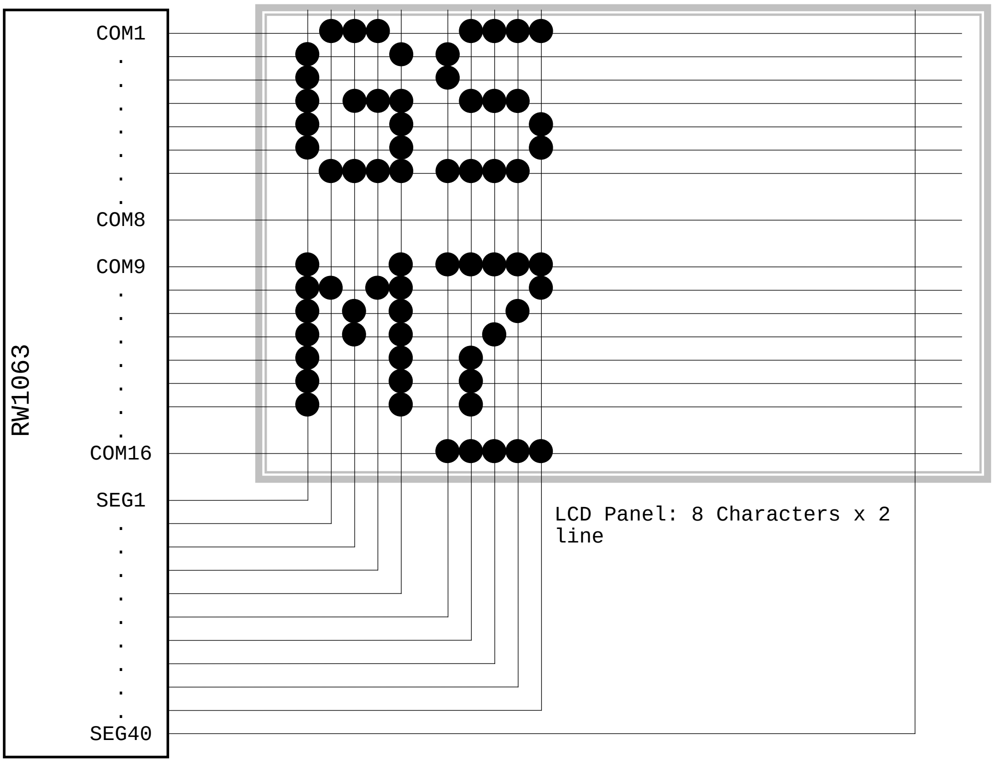
A. 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)


RW1063
COM1
COM8
SEG1
SEG40
LCD Panel: 8 Characters x 1 line

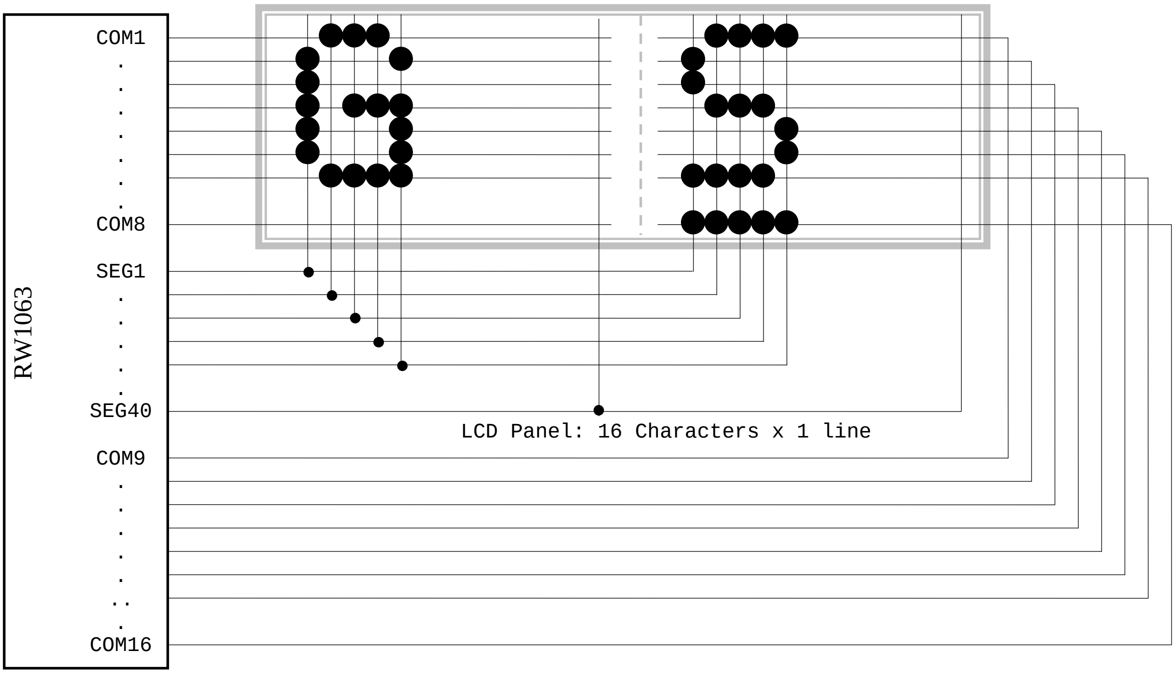
B. 5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)


RW1063
COM1
COM11
SEG1
SEG40
LCD Panel: 8 Characters x 1 line

C. 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)


RW1063
COM1
COM8
COM9
COM16
SEG1
SEG40
LCD Panel: 8 Characters x 2 line

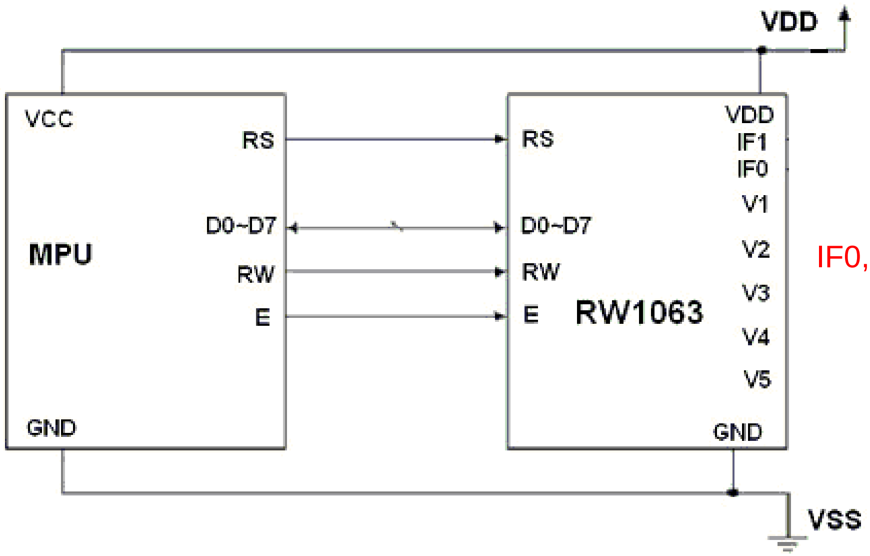
D. 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)


RW1063
COM1
COM8
SEG1
SEG40
COM9
COM16
LCD Panel: 16 Characters x 1 line

◆ THE MPU INTERFACE CIRCUIT

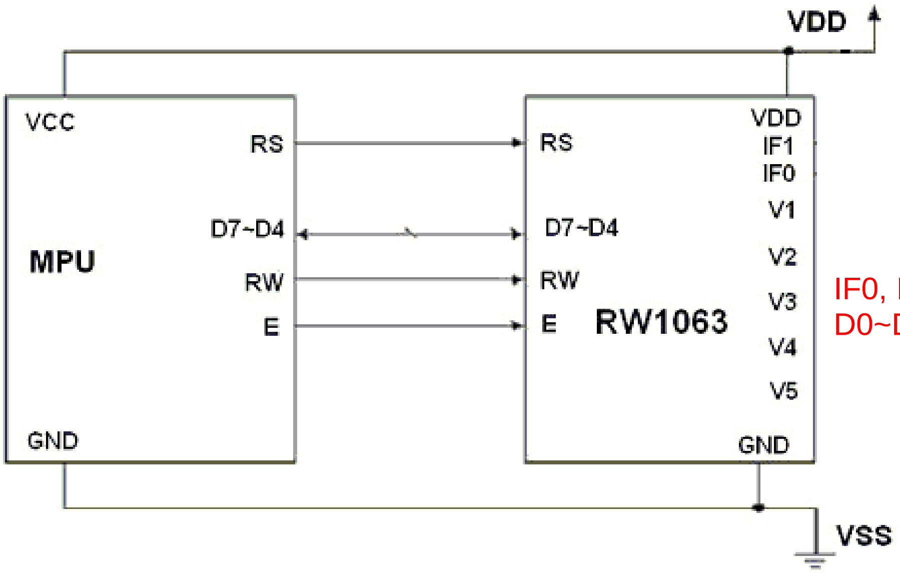
The RW1063 Series can be connected to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the RW1063 series chips with fewer signal lines.
The display area can be enlarged by using multiple RW1063 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

(1) 6800 8 bits Series MPUs


VDD
VCC
RS
D0~D7
MPU
RW
E
GND
RS
D0~D7
RW
E
RW1063
VDD
IF1
IF0
V1
V2
V3
V4
V5
GND
VSS

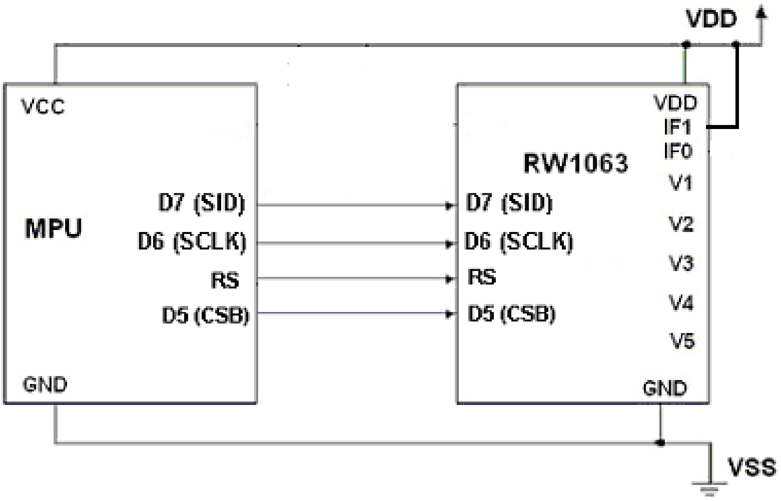
IF0, IF1: opened

(2) 6800 4 bits Series MPUs


VDD
VCC
RS
D7~D4
MPU
RW
E
GND
RS
D7~D4
RW
E
RW1063
VDD
IF1
IF0
V1
V2
V3
V4
V5
GND
VSS

IF0, IF1: opened
D0~D3: opened

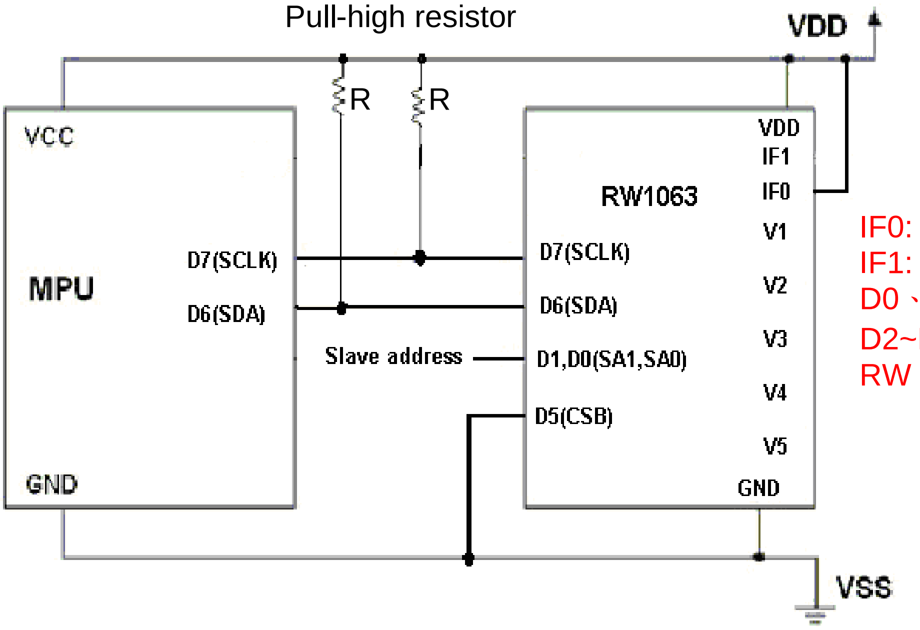
(3) Using the Serial Interface—For 4 SPI


VDD
VCC
MPU
D7 (SID)
D6 (SCLK)
RS
D5 (CSB)
GND
RW1063
VDD
IF1
IF0
V1
D7 (SID)
V2
D6 (SCLK)
V3
RS
V4
D5 (CSB)
V5
GND
VSS

IF0: opened
IF1: bonding to VDD
D0~D4: opened
RW、E: opened

(4) Using the Serial Interface—For IIC Interface

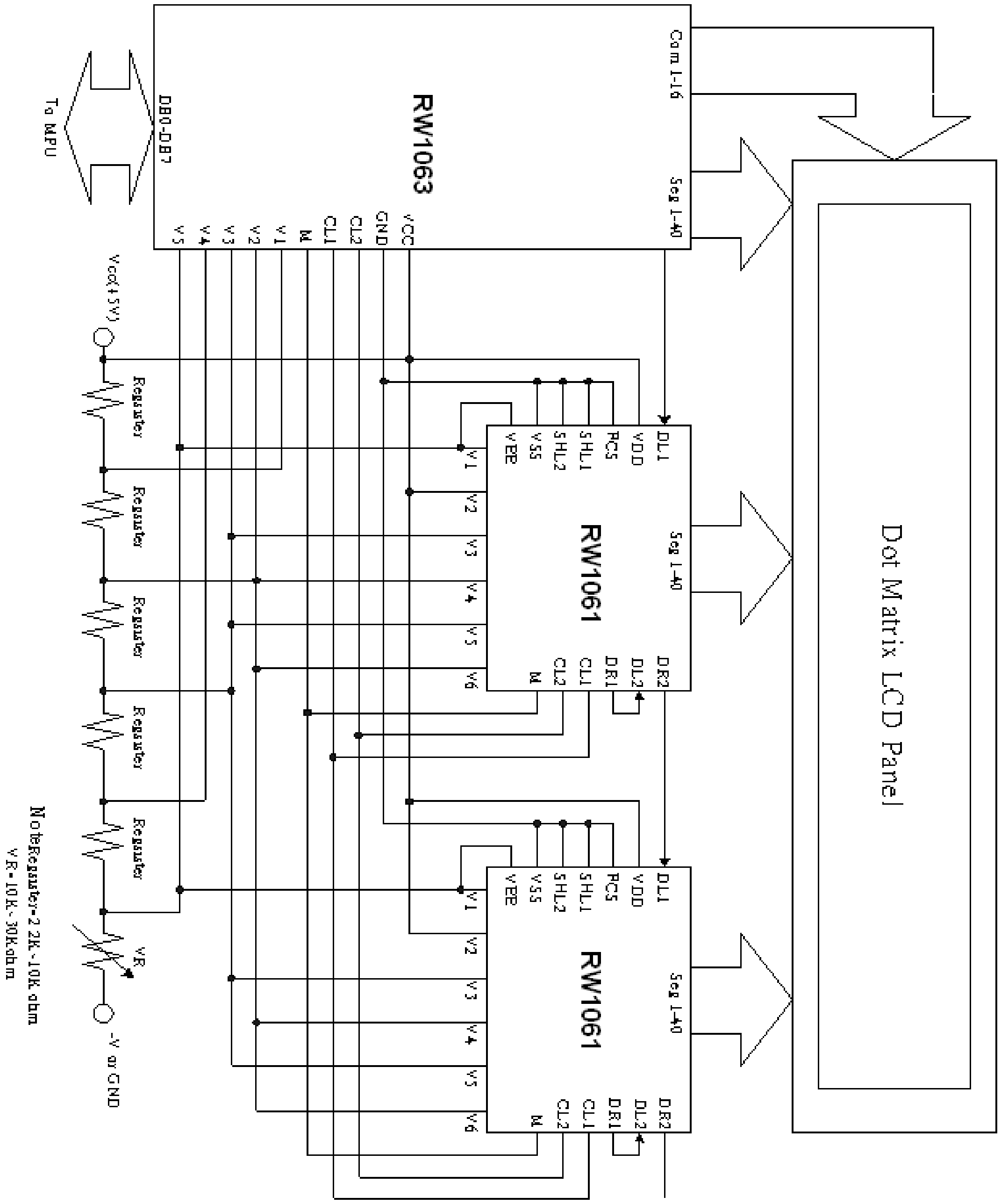
R=2.2K
Pull-high resistor


VDD
R
R
VCC
MPU
D7(SCLK)
D6(SDA)
GND
Slave address
RW1063
VDD
IF1
IF0
V1
D7(SCLK)
V2
D6(SDA)
V3
D1,D0(SA1,SA0)
V4
D5(CSB)
V5
GND
VSS

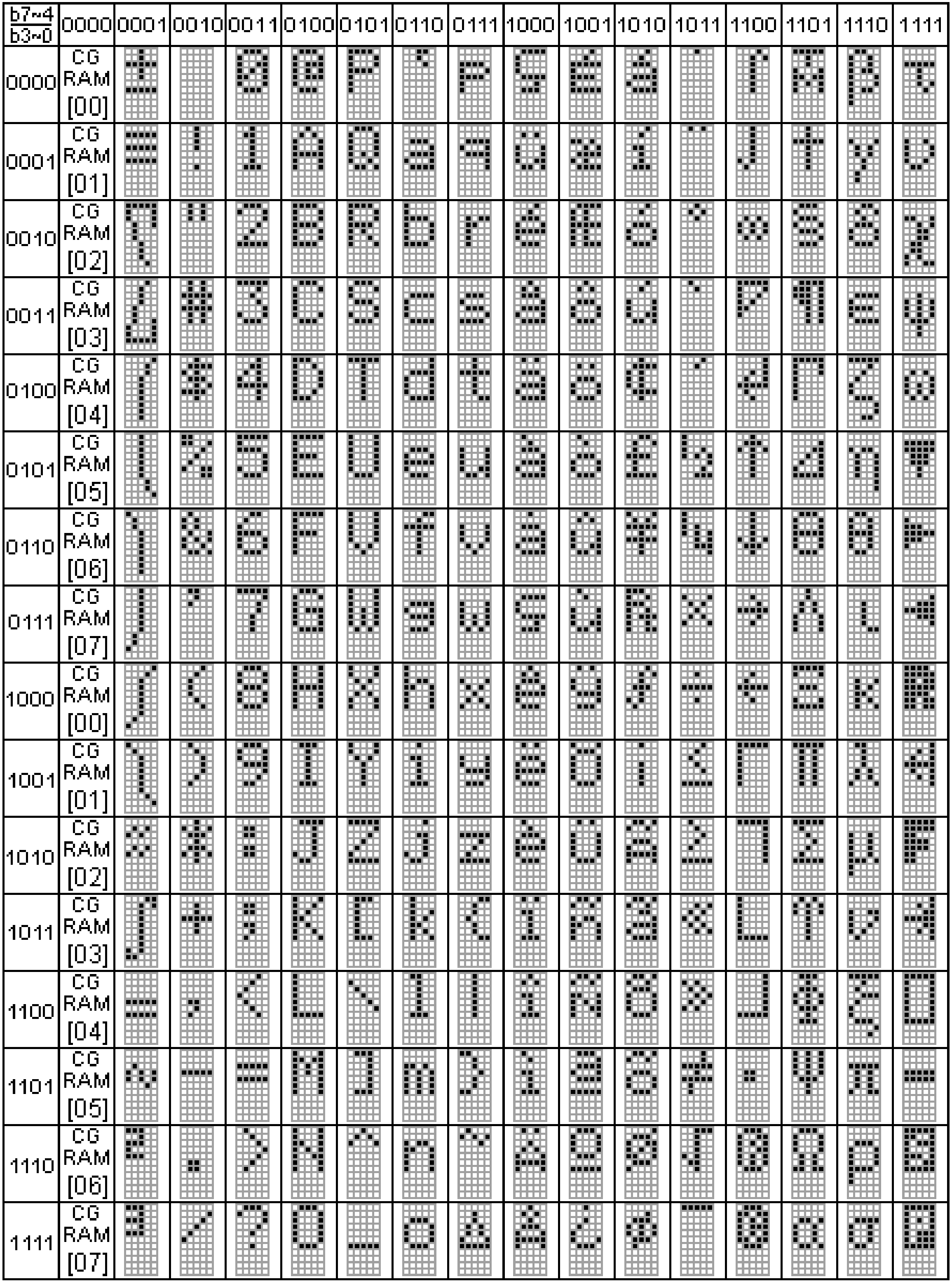
IF0: bonding to VDD
IF1: opened
D0、D1:Slave address
D2~D4: opened
RW、E: opened

◆ Application Circuit

(2 Line x 24 Characters)


RW1063
Com 1-16
Seg 1-40
DB0-DB7
To MPU
V5
V4
V3
V2
V1
M
CL1
CL2
GND
VCC
Vcc(+5V)
Register
Register
Register
Register
Register
VR
-V or GND
NoteRegister=2.2K-10K ohm
VR=10K-30K ohm
RW1061
DL1
VDD
RCS
SHL1
SHL2
VSS
VEE
V1
V2
V3
V4
V5
V6
Seg 1-40
DR2
DL2
DR1
CL1
CL2
M
RW1061
DL1
VDD
RCS
SHL1
SHL2
VSS
VEE
V1
V2
V3
V4
V5
V6
Seg 1-40
DR2
DL2
DR1
CL1
CL2
M
Dot Matrix LCD Panel

RW1063 Font table (0B-002)


b7~4
b3~0
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
CG RAM [00]
CG RAM [01]
CG RAM [02]
CG RAM [03]
CG RAM [04]
CG RAM [05]
CG RAM [06]
CG RAM [07]