Crystalfontz This controller datasheet was downloaded from **http://www.crystalfontz.com/controllers/**

RockWorks **(Preliminary)** **RW1068**

26COM/84SEG DRIVER & CONTROLLER FOR DOT MATRIX LCD

INTRODUCTION

RW1068 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology.
It can display 2 lines x 14 (6 x 12 dot format)
When using the 2 lines x 14 (6 x 12 dot format), it can display 2 lines of 7 Chinese character, Japanese kan-ji or Korean character. Therefore maximum 504 characters can be included. Customized codes are available.

FUNCTIONS

_ Character type dot matrix LCD driver & controller
_ Internal drivers: 26 common and 84 segment output
_ Easy interface with 4-bit or 8-bit MPU or standard 4 lines / 3 lines serial port interface (SPI)
_ 6 x 12 dot matrix possible
_ Bi-directional shift function
_ All character reverse display
_ Display shift per line
_ Voltage converter for LCD drive voltage : 10 V max (2 times / 3 times)
_ Various instruction functions
_ Automatic power on reset

FEATURES

_ Internal Memory
- Character Generator ROM (CGROM): 17,280 bits +18,432 bits x 3 (240 + 256 x 3 characters x 6 x 12 dot)
- Character Generator RAM (CGRAM) : 64 x 8 bits (4 characters x 6 x12 dot)
- Icon RAM (SEGRAM) : 16 x 8 bits (84 icons max.)
- Display Data RAM (DDRAM) : 80 x 8 bits (80 characters max.)

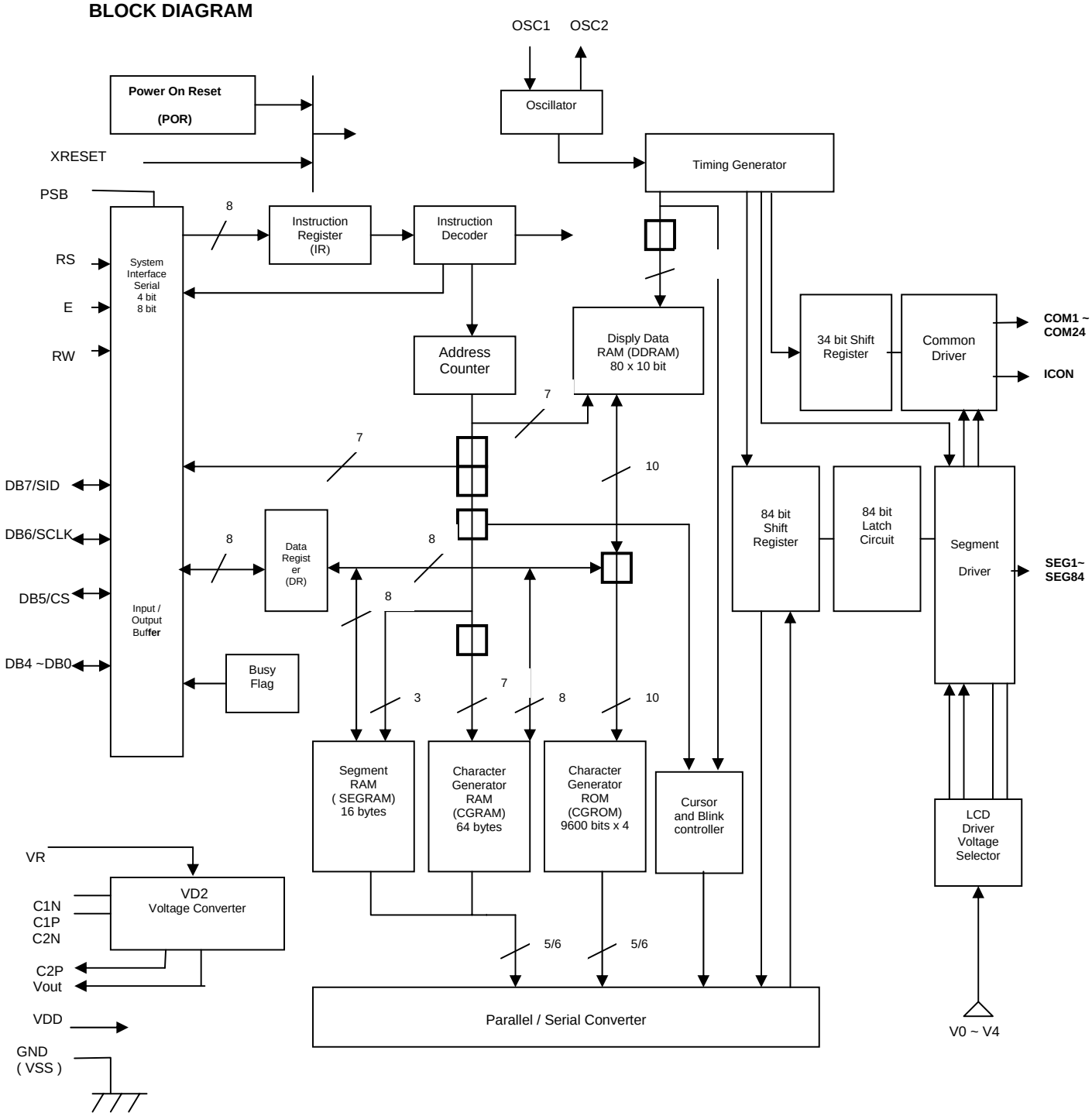
_ Low power operation
- Power supply voltage range : 2.7 ~ 5.5 V (VDD)
- LCD Drive voltage range : 3.0 ~ 10 V (Vss – V0)

_ CMOS process
_ duty cycles: 1/25 (refer to Table 1.)
_ Internal oscillator with an external resistor
_ Low power consumption
_ Bare chip available

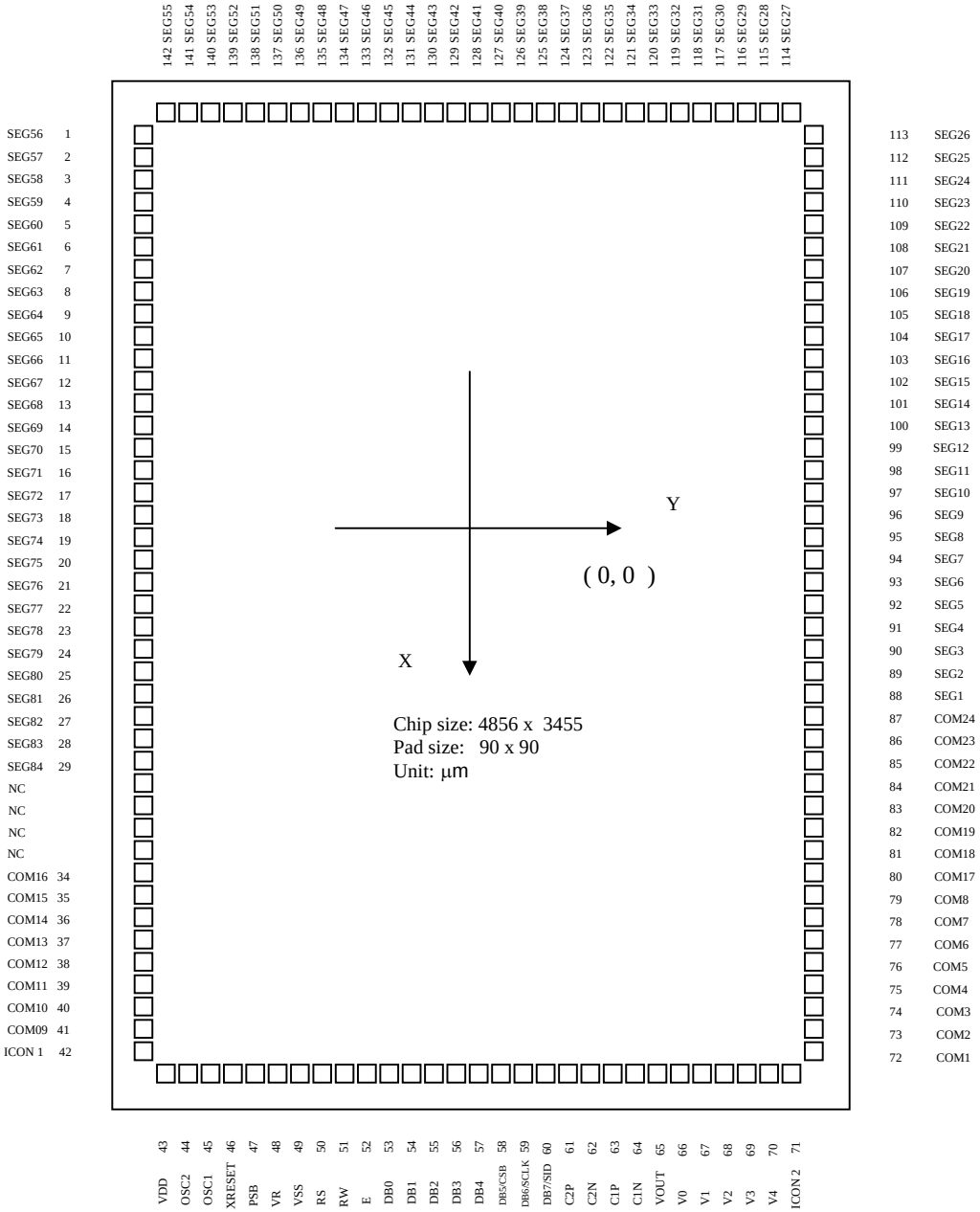
Programmable duty cycles
(Table 1)

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable characters	Possible icons
2	1/25	2 lines of 14 characters (6 x 12 dots)	84

BLOCK DIAGRAM



PAD CONFIGURATION



PAD LOCATION

UNIT: (μm)

PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE		PAD NUMBER	PAD NAME	COORDINATE	
		X	Y			X	Y			X	Y
1	SEG56	-2203	-1623	49	VSS	2323	-831	97	SEG10	-474	1623
2	SEG57	-2073	-1623	50	RS	2323	-727	98	SEG11	-580	1623
3	SEG58	-1953	-1623	51	RW	2323	-623	99	SEG12	-685	1623
4	SEG59	-1843	-1623	52	E	2323	-519	100	SEG13	-790	1623
5	SEG60	-1738	-1623	53	DB0	2323	-415	101	SEG14	-895	1623
6	SEG61	-1632	-1623	54	DB1	2323	-312	102	SEG15	-1000	1623
7	SEG62	-1527	-1623	55	DB2	2323	-208	103	SEG16	-1106	1623
8	SEG63	-1422	-1623	56	DB3	2323	-104	104	SEG17	-1211	1623
9	SEG64	-1316	-1623	57	DB4	2323	0	105	SEG18	-1316	1623
10	SEG65	-1211	-1623	58	DB5 / CSB	2323	104	106	SEG19	-1422	1623
11	SEG66	-1106	-1623	59	DB6 / SCLK	2323	208	107	SEG20	-1527	1623
12	SEG67	-1000	-1623	60	DB7 / SID	2323	312	108	SEG21	-1632	1623
13	SEG68	-895	-1623	61	C2P	2323	416	109	SEG22	-1738	1623
14	SEG69	-790	-1623	62	C2N	2323	519	110	SEG23	-1843	1623
15	SEG70	-685	-1623	63	C1P	2323	623	111	SEG24	-1953	1623
16	SEG71	-579	-1623	64	C1N	2323	727	112	SEG25	-2073	1623
17	SEG72	-474	-1623	65	VOUT	2323	831	113	SEG26	-2203	1623
18	SEG73	-369	-1623	66	V0	2323	935	114	SEG27	-2323	1503
19	SEG74	-263	-1623	67	V1	2323	1039	115	SEG28	-2323	1373
20	SEG75	-158	-1623	68	V2	2323	1143	116	SEG29	-2323	1253
21	SEG76	-53	-1623	69	V3	2323	1253	117	SEG30	-2323	1143
22	SEG77	53	-1623	70	V4	2323	1373	118	SEG31	-2323	1039
23	SEG78	158	-1623	71	ICON2	2323	1503	119	SEG32	-2323	935
24	SEG79	263	-1623	72	COM1	2203	1623	120	SEG33	-2323	831
25	SEG80	369	-1623	73	COM2	2073	1623	121	SEG34	-2323	727
26	SEG81	474	-1623	74	COM3	1953	1623	122	SEG35	-2323	623
27	SEG82	579	-1623	75	COM4	1843	1623	123	SEG36	-2323	519
28	SEG83	684	-1623	76	COM5	1738	1623	124	SEG37	-2323	416
29	SEG84	790	-1623	77	COM6	1632	1623	125	SEG38	-2323	312
30	NC	895	-1623	78	COM7	1527	1623	126	SEG39	-2323	208
31	NC	1000	-1623	79	COM8	1422	1623	127	SEG40	-2323	104
32	NC	1106	-1623	80	COM17	1316	1623	128	SEG41	-2323	0
33	NC	1211	-1623	81	COM18	1211	1623	129	SEG42	-2323	-104
34	COM16	1316	-1623	82	COM19	1106	1623	130	SEG43	-2323	-208
35	COM15	1422	-1623	83	COM20	1000	1623	131	SEG44	-2323	-312
36	COM14	1527	-1623	84	COM21	895	1623	132	SEG45	-2323	-415
37	COM13	1632	-1623	85	COM22	790	1623	133	SEG46	-2323	-519
38	COM12	1738	-1623	86	COM23	684	1623	134	SEG47	-2323	-623
39	COM11	1843	-1623	87	COM24	579	1623	135	SEG48	-2323	-727
40	COM10	1953	-1623	88	SEG1	474	1623	136	SEG49	-2323	-831
41	COM9	2073	-1623	89	SEG2	369	1623	137	SEG50	-2323	-935
42	ICON1	2203	-1623	90	SEG3	263	1623	138	SEG51	-2323	-1039
43	VDD	2323	-1503	91	SEG4	158	1623	139	SEG52	-2323	-1143
44	OSC2	2323	-1373	92	SEG5	53	1623	140	SEG53	-2323	-1253
45	OSC1	2323	-1253	93	SEG6	-53	1623	141	SEG54	-2323	-1373
46	XRESET	2323	-1143	94	SEG7	-158	1623	142	SEG55	-2323	-1503
47	PSB	2323	-1039	95	SEG8	-263	1623				
48	VR	2323	-935	96	SEG9	-369	1623				

*** "RW1068" Marking: easy to find the PAD No: 1**

PAD DESCRIPTION

PAD(NO)	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE
VDD (43)	-	Power supply	For logical circuit(+3V,+5V)	Power supply
VSS (49)			0V (GND)	
V 0-V4 (66-70)			Bias voltage level for LCD driving	
VR (48)	Input	Reference input voltage	Reference voltage input to generate V0	-
SEG1-SEG84 (88-142,1-25)	Output	Segment output	Segment signal output for LCD drive	LCD
ICON1 (42)	Output	Common output	Common signal output for LCD drive	LCD
ICON2 (71)	Output	Common output	Common signal output for LCD drive	
COM1-COM24 (72-87)	Output	Common output	Common signal output for LCD drive	LCD
OSC1,OSC2 (45,44)	Input (OSC1), Output (OSC2)	Oscillator	When use internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External resistor/oscillator (OSC1)
C1N,C1P,C2N, C2P (64,63,62,61)	Input	External Capacitance input	To use the voltage converter (2 times/ 3 times), these pins must be connected to the external capacitance.	External Capacitance
XRESET (46)	Input	Reset pin	Initialized to Low	-
VOUT (65)	Output	Two / Three times converter output	Voltage converter output voltage	-

PAD DESCRIPTION (continued)

PAD(NO)	INPUT/OUTPUT	NAME	DESCRIPTION	INTERFACE
PSB (47)	Input	Interface mode selection	Select Interface mode with the MPU. When PSB = “Low” : Serial mode, When PSB = “High”: 4 -bit / 8 -bit bus mode.	MPU
RS (50)	Input	Register select	In bus mode, used as register selection input. When RS = “High”, Date register is selected. When RS = “Low”, Instruction register is selected.	MPU
E (52)	Input	Read. Write enable	In bus mode, used as read write enable signal.	MPU
RW (51)	Input	Read. Write	In bus mode, used as read / write selection input. When RW =”High”, read operation. When RW =”Low”, write operation.	MPU
DB4 (57)	Input. Output	Data bus 4	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order.	MPU
DB5/CSB (58)	Input. Output	Data bus 5 / Chip select	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. In serial mode, used as chip selection input. When CSB = “Low”, selected When CSB = “High”, not selected. (Low access enable)	MPU
DB6/SCLK (59)	Input. Output	Data bus 6 / Serial clock	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. In serial mode, used as serial clock input pin.	MPU
DB7/SID (60)	Input. Output	Data bus 7 / Serial input data	In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. In serial mode, used for data input pin.	MPU
DB0-DB3 (53~56)	Input. Output	Data bus 0~3	In 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode or serial mode, open these pins.	MPU

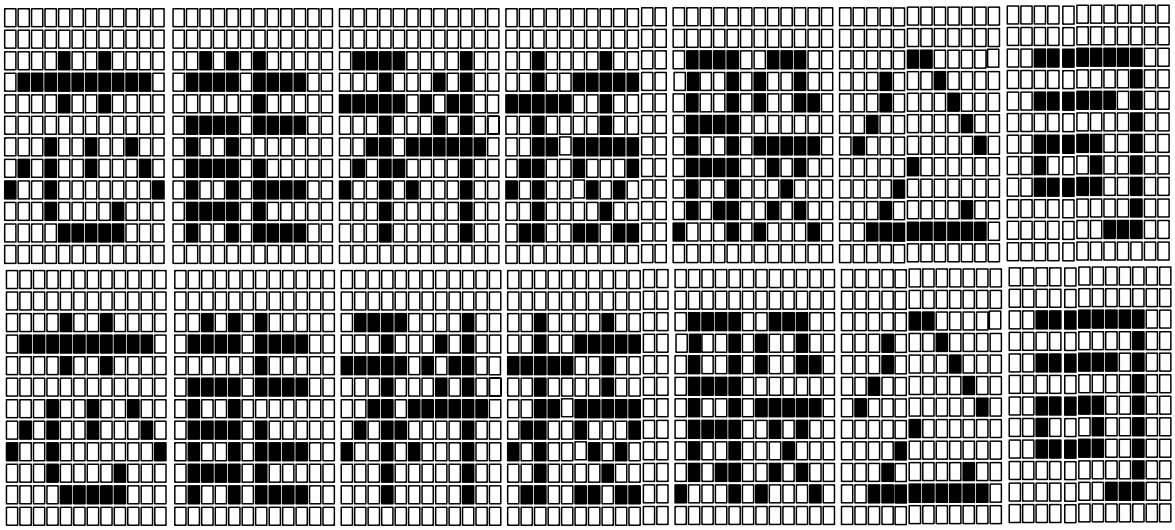
INSTRUCTION DESCRIPTION

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	x	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM. and set DDRAM address to “00H” from AC.	1.53ms
Return Home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Power Down Mode	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. PD = “1” : power down mode set, PD = “0”: power down mode disable.	37μs
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = “1”: increment I/D = “0”: decrement And display shift enable bit. S = “1”: make display shift of the enabled lines by the DS2 - DS1 bits in the Shift Enable instruction. S = “0”: display shift disable	37μs
	1	0	0	0	0	0	0	0	1	1	BID	Segment bi-direction function. BID = “1”: Seg84 →Seg1, BID = “0”: Seg1→Seg84.	
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display / cursor / blink on/off D = “1”: display on, D = “0”: display off, C = “1”: cursor on, C = “0”: cursor off, B = “1”: blink on, B = “0: blink off.	37μs
Extended Function set	1	0	0	0	0	0	0	1	1	B/W	0	Assign black/white inverting of cursor, B/W = “1”: black/white inverting of cursor enable, B/W = “0”: black/white inverting of cursor disable	37μs

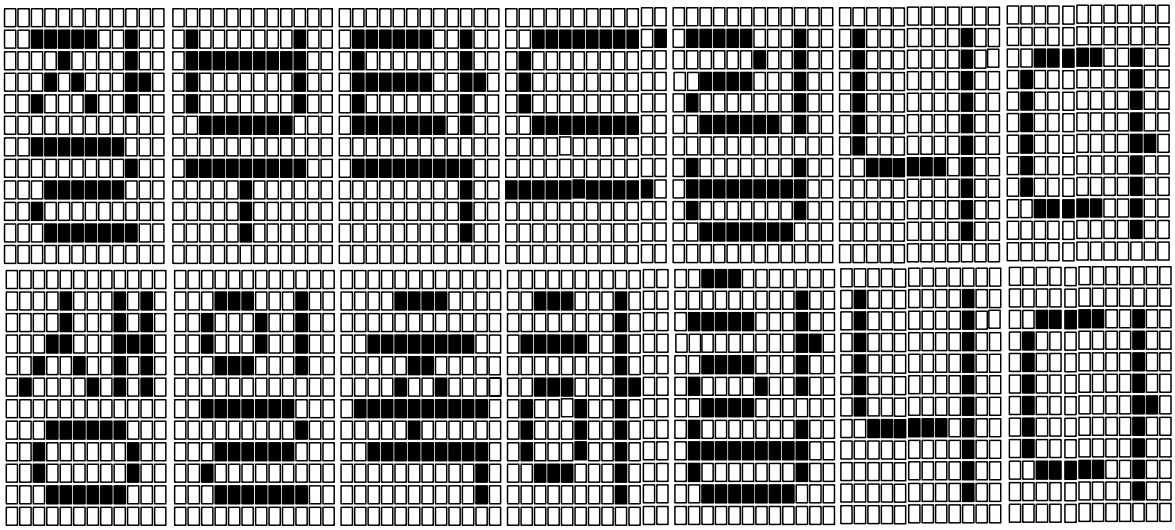
Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Cursor or Display shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift. S/C = “1” : display shift, S/C = “0” : cursor shift, R/L = “1” : shift to right, R/L = “0” : shift to left.	37μs
Shift Enable	1	0	0	0	0	0	1	0	0	DS2	DS1	(when DC = “1“) Determine the line for display shift. DS1 = “1/0”: 1st line display shift enable/disable DS2 = “1/0”: 2nd line display shift enable/disable	37μs
Code Bank Selection	1	0	0	0	0	0	1	X	X	CB1	CB0	(when DC = “0“) (CB1, CB0) = (0, 0) ROM code Bank 0 selected (0, 1) ROM code Bank 1 selected (1, 0) ROM code Bank 2 selected (1, 1) ROM code Bank 3 selected	37μs
Function Set	0	0	0	0	0	1	IF	X	RE(0)	DC	REV	Set interface data length (IF =”1”: 8-bit, IF =”0”: 4-bit), extension register, RE(“0”), shift enable. DC=”1”: enable display shift per line. DC=”0”: enable the selection of code bank. Reverse bit REV =”1”: reverse display, REV =”0”: normal display.	37μs
	1	0	0	0	0	1	IF	X	RE(1)	BE	0	Set IF, RE(“1”) and CGRAM/SEGRAM blink enable (BE) BE = “1/0”: CGRAM/SEGRAM blink enable/disable.	37μs

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set CGRAM Address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	37μs
Set SEGRAM Address	1	0	0	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter.	37μs
Set DDRAM Address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	37μs
Set Data Length	1	0	0	1	SD6	SD5	SD4	SD3	SD2	SD1	SD0	Set data length for 3 line SPI	37μs
Read Busy flag and Address	X	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can know internal operation is ready or not by reading BF. The contents of address counter can also be read. BF = “1” : busy state, BF = "0" : ready state.	0μs
Write Data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM. (DDRAM / CGRAM / SEGRAM).	43μs
Read Data	X	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM. (DDRAM / CGRAM / SEGRAM).	43μs

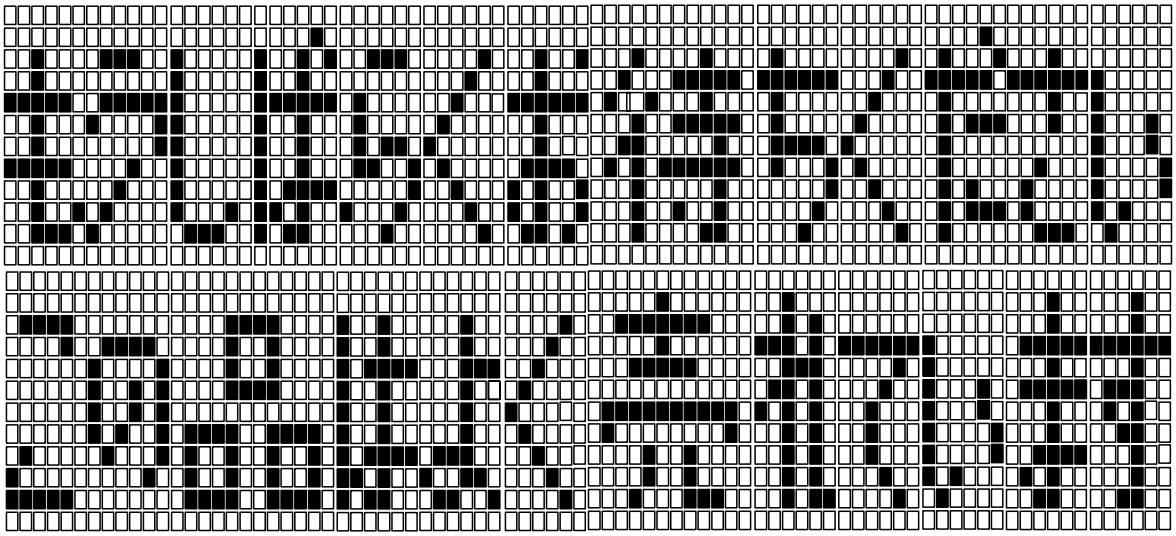
- Note : 1. When an MPU program with Busy Flag(DB7) checking is made, 1/ 2 Fosc (is necessary) for executing the next instruction by the “ E “ signal after the Busy Flag (DB7) goes to “ Low ”.
  2. “ X ” Don’t care



2 lines x 14 (6 x 12 dot format) – Chinese character



2 lines x 14 (6 x 12 dot format) – Korean Character



2 lines x 14 (6 x 12 dot format) –Japanese kan-ji Character

FUNCTION DESCRIPTION

SYSTEM INTERFACE

This chip has all three kinds interface type with MPU : serial, 4-bit bus and 8-bit bus. Serial and bus (4-bit/8-bit) is selected by PSB input, and 4-bit bus and 8-bit bus is selected by IF bit in the instruction register. During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR). The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.

So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/SEGRAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS input pin in 4-bit/8-bit bus mode (PSB = "High") or RS bit in serial mode (PSB= "Low").

RS	R/W	Operation
0	0	Instruction write operation (MPU writes Instruction code into IR)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	Data write operation (MPU writes data into DR)
1	1	Data read operation (MPU reads data from DR)

BUSY FLAG (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R / W = High (Read Instruction Operation), through DB7 Before executing the next instruction, be sure that BF is not High.

DISPLAY DATA RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure 1.)

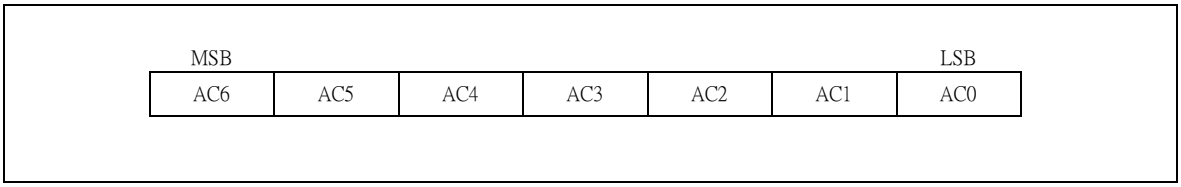
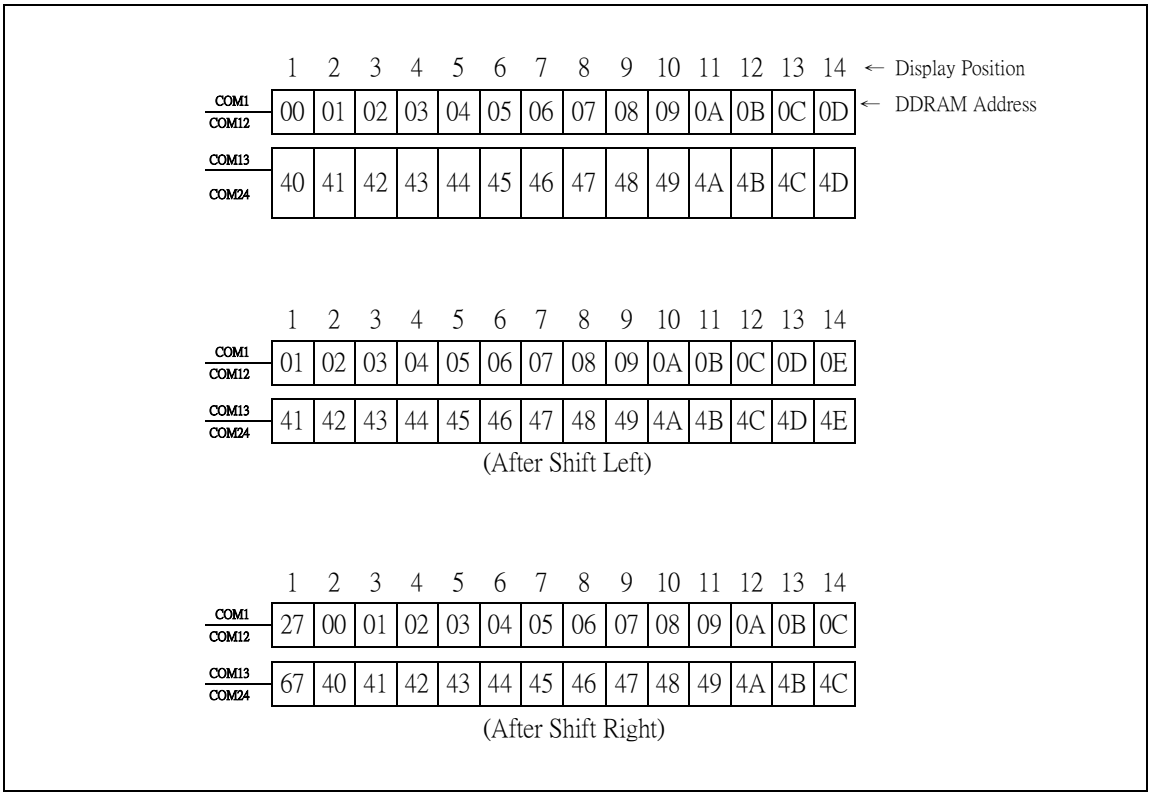


Figure 1. DDRAM Address

6-dot 2-line Display

In case of 2-line display with 6-dot font, the address range of DDRAM is 00H-27H, 40H-67H (refer to Figure 2).



(Figure 2.) 2 - line X 24ch. Display (6-dot Font Width)

TIMING GENERATION CIRCUIT

Timing generation circuit generates clock signals for the internal operations.

ADDRESS COUNTER (AC)

Address Counter (AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR.

After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0-DB6

CURSOR/BLINK CONTROL CIRCUIT

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

LCD DRIVER CIRCUIT

LCD Driver circuit has 26 common and 84 segment signals for LCD driving.
Data from SEGRAM/CGRAM/CGROM is transferred to 84 bit segment latch serially,
and then it is stored to 84 bit shift latch. When each COM is selected by 26 bit common register, segment data also output through segment driver from 84 bit segment latch.
In case of 2 line (6 dots width) display mode, COM0-COM25 have 1/25 duty.

CGROM (CHARACTER GENERATOR ROM)

CGROM has 17,280 bits +18,432 bits x 3 (240 + 256 x 3 characters x 6 x 12 dot)

CGRAM (CHARACTER GENERATOR RAM)

CGRAM has up to 6 x 12 dots 4 characters. By writing font data to CGRAM, user defined character can be used (refer to Table 2).

6 x 12 dots Character Pattern

Table 2.

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern Number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	0	0	0	X	0	0	0	0	0	0	B1	B0	0	0	1	1	1	0	Pattern 1
											0	0	1			0	1	0	0	0	1	
				.					.		0	1	0		.	0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	0	0	0	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0			0	1	1	1	1	1	
											1	1	1			0	1	0	0	0	1	
0	0	0	0	0	0	0	X	0	0	1	0	0	0	B1	B0	0	1	0	0	0	1	
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	0	0	0	1	
				.					.		1	0	0		.	0	0	0	0	0	0	
				.					.		1	0	1		.	0	0	0	0	0	0	
				.					.		1	1	0		.	0	0	0	0	0	0	
											1	1	1			0	0	0	0	0	0	
0	0	0	0	0	1	1	X	1	1	0	0	0	0	B1	B0	0	0	1	1	1	0	Pattern 4
											0	0	1			0	1	0	0	0	1	
				.					.		0	1	0		.	0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	0	0	0	1	
				.					.		1	0	0		.	0	1	0	0	0	1	
				.					.		1	0	1		.	0	1	0	0	0	1	
											1	1	0			0	1	1	1	1	1	
											1	1	1			0	1	0	0	0	1	
0	0	0	0	0	1	1	X	1	1	1	0	0	0	B1	B0	0	1	0	0	0	1	
											0	0	1			0	1	0	0	0	1	
											0	1	0			0	1	0	0	0	1	
				.					.		0	1	1		.	0	1	0	0	0	1	
				.					.		1	0	0		.	0	0	0	0	0	0	
				.					.		1	0	1		.	0	0	0	0	0	0	
				.					.		1	1	0		.	0	0	0	0	0	0	
											1	1	1			0	0	0	0	0	0	

1. When BE (Blink Enable bit) = "High", blink is controlled by B1 and B0 bit.
In case of 6-dot font width, when B1 = "1", enabled dots of P0-P5 will blink, and when B1 = "0" and B0 = "1", enabled dots of P5 will blink, when B1 = "0" and B0 = "0", blink will not happen.

2. "X": Don't care

SEGRAM (SEGMENT ICON RAM)

SEGRAM has segment control data and segment pattern data. There are 2 ICON pins act as the COM line to display the icon SEGRAM data. The outputs of these 2 ICON pins are exactly the same. The higher 2-bits of SEGRAM data are blinking control data, and lower 6-bits are pattern data (refer to Table 3 and Figure 3).

Table 3. Relationship between SEGRAM Address and Display Pattern

SEGRAM Address				SEGRAM Data Display Pattern							
				6-dot Font Width							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	1	B1	B0	S55	S56	S57	S58	S59	S60
1	0	1	0	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	S79	S80	S81	S82	S83	S84
1	1	1	0	-	-	-	-	-	-	-	-
1	1	1	1	-	-	-	-	-	-	-	-

1. B1, B0: Blinking control bit

Control Bit			Binking Port
BE	B1	B0	6- dot font width
0	X	X	No blink
1	0	0	No blink
1	0	1	D5
1	1	X	D5 - D0

2. S1 – S84: Icon pattern ON/OFF in 6- dot font width

3. " X " : Don't care

6 Dot Font Width

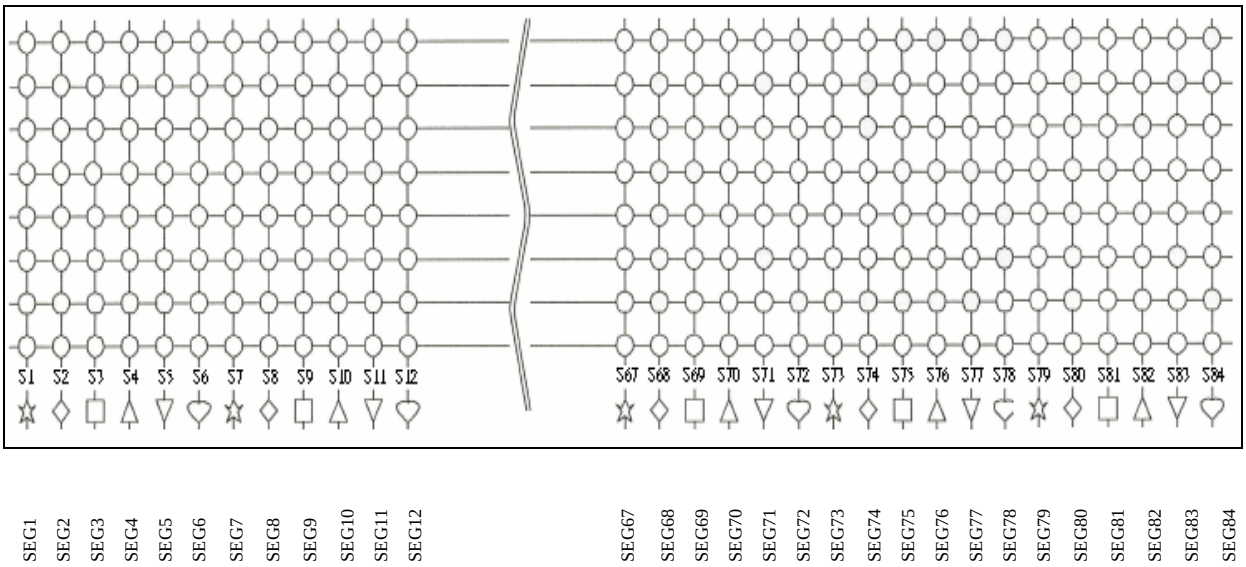


Figure 3. Relationship between SEGRAM and Segment Display

INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of RW1068 and MPU clock, RW1068 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus.

Instruction can be divided largely four kinds;

- RW1068 function set instructions (set display methods, set data length, etc.)
- Address set instructions to internal RAM
- Data transfer instructions with internal RAM
- Others

The address of internal RAM is automatically increased or decreased by 1.

NOTE: During internal operation, Busy Flag (DB7) is read high. Busy Flag check must be proceeded the next instruction.
Busy flag check must be proceeded the next instruction.
When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home: (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Power Down Mode Set: (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction.
PD = “High”, it makes RW1068 suppress current consumption except the current needed for data storage by executing next three functions.
1. Makes the output value of all the COM / SEG ports VSS.
2. Disable voltage converter to remove the current through the divide resistor of power supply.
   This instruction can be used as power sleep mode.
   When PD = “Low”, power down mode becomes disabled.

Entry Mode Set: (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.
I/D: Increment/decrement of DDRAM address (cursor or blink)
   When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
   When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the display of enabled line by DS1 – DS2 bits in the shift enable instruction is shifted to the right (I/D = "0") or to the left (I/D = "1"). But it will seem as if the cursor does not move. When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display like this function is not performed.

Entry Mode Set: (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	BID

Set the data shift direction of segment in the application set.

BID: Data Shift Direction of Segment
When BID = "Low", segment data shift direction is set to normal order from SEG1 to SEG80.
When BID = "High", segment data shift direction is set to reverse from SEG80 to SEG1.
By using this instruction, the efficiency of application board area can be raised.
- The BID setting instruction is recommended to be set at the same time level of function set instruction.
- DB1 bit must be set to “1”.

Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.
C: Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
B: Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270kHz frequency, blinking has 370 ms interval.
When B = "Low", blink is off.

Extended Function Set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	B/W	0

FW: Font width control
When FW = "High", display character font width is assigned to 6-dot
The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the leftmost space bit of CGRAM.(refer to Fig-4)
B/W: Black/ white inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270kHz, inversion has 70 ms intervals.

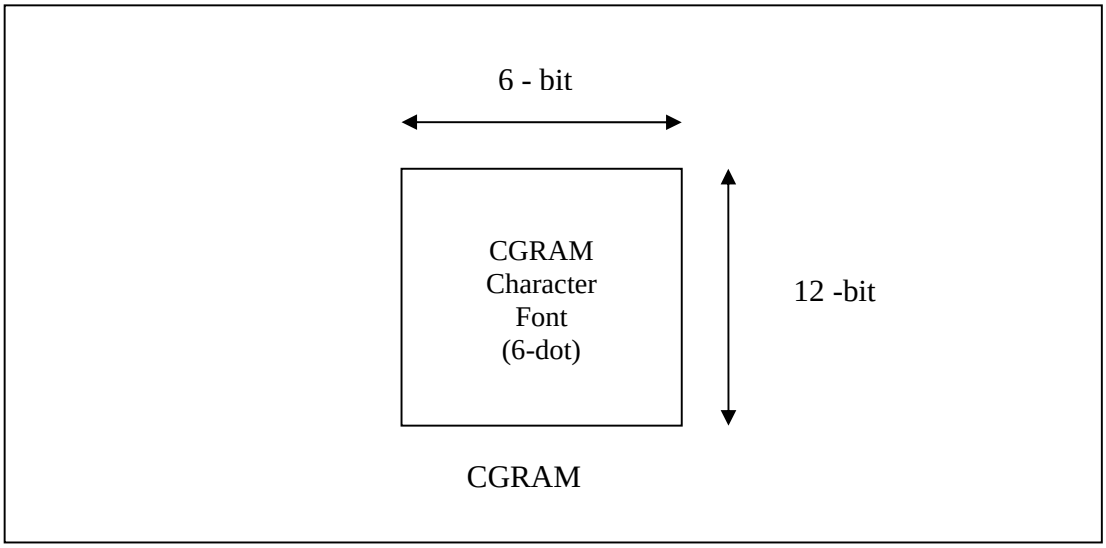


Figure 4. 6-dot Font Width CGROM/CGRAM

Cursor or Display Shift (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to Table 4). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
Note that display shift is performed simultaneously in all the line enabled by DS1 – DS2 in the shift enable instruction. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.
During low power consumption mode, display shift may not be performed normally.

Table 4. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, address counter is decreased by 1
0	1	Shift cursor to the right, address counter is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Code Bank Selection

(DC=0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	x	x	CB1	CB0

There's 4 different code bank with each 256 fonts of 6 x 12 bits

CB1	CB0	
0	0	code bank 1
0	1	code bank 2
1	0	code bank 3
1	1	code bank 4

When writing to DDRAM for each displaying character the code bank must be properly set.

(DC=1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	DS2	DS1

DS: Display Shift per Line Enable
This instruction selects shifted to be according to each line mode in display shift right/left instruction.
DS1, DS2 indicate each line to be shifted, and each shift is performed individually in each line.

Table 5. Relationship between DS and COM Signal (2 lines)

Enable Bit	Enabled Common Signals during Shift	Operation
DS1	COM1 ~ COM12	The parts of display line the Corresponds to enabled Common signal can be shifted.
DS2	COM13 ~ COM24	

Function Set

(RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	IF	X	RE(0)	DC	REV

IF : Interface data length control bit
When IF = "High", it means 8-bit bus mode with MPU.
When IF = "Low", it means 4-bit bus mode with MPU. So to speak ,IF is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

RE : Extended function registers enable bit
At this instruction, RE must be "Low".

DC : Display shift enable selection bit
When DC = ”High”, enable display shift per line.
When DC =”Low”, enable the selection of code bank.

REV: Reverse enable bit
When REV = “High”, all the display data are reversed. i.e., all the white dots become black and black dots become white.
When REV =”Low”, the display mode set normal display.

(RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	IF	X	RE(1)	BE	0

IF : Interface data length control bit
When IF = "High", it means 8-bit bus mode with MPU.
When IF = "Low", it means 4-bit bus mode with MPU. So to speak, IF is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it needs to transfer 4-bit data by two times.

RE: Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, BID bit, DC bits of shift enable instruction and BE bits of function set register can be accessed.

BE: CGRAM/SEGRAM data blink enable bit If BE is "High", It makes user font of CGRAM and segment of SEGRAM blink. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

Set SEGRAM Address (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	x	x	AC3	AC2	AC1	AC0

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.
In 2-line display mode , DDRAM address in the 1st line is from "00H" - "27H", and DDRAM address in the 2nd line is from "40H" - "67H".

Set data length for 3 line SPI

Table 6. Set data length according to SD Bits

SD6	SD5	SD4	SD3	SD2	SD1	SD0	Function
0	0	0	0	0	0	0	Followed by 1 data write
0	0	0	0	0	0	1	Followed by 2 data write
0	0	0	0	0	1	0	Followed by 3 data write
0	0	0	0	0	1	1	Followed by 4 data write
:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	Followed by 80 data write

Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether RW1068 is in internal operation or not. If the resultant BF is High, it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

Write Data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.

The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction:
DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determines the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read Data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM. The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

- In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

INTERFACE WITH MPU

RW1068 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU. So you can use any type 4 or 8- bit MPU.

In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.

- When interfacing data length are 4-bit, only 4 ports, from DB4 - DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4- bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended.

- When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 - DB7.

- If PSB is set to "Low", serial transfer mode is set.

INTERFACE WITH MPU IN BUS MODE

Interface with 8-bit MPU

If 8-bits MPU is used, RW1068 can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.

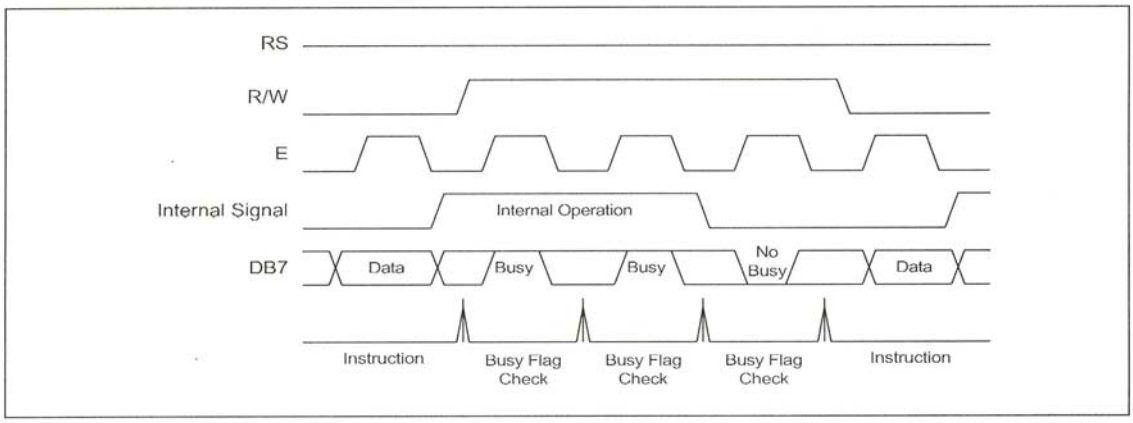


Figure 5. Example of 8-bit Bus Mode Timing Sequence

Interface with 4-bit MPU

If 4-bit MPU is used, RW1068 can connect directly with this. In this case, port E, RS, R/W and DB4 - DB7 need to interface each other. The transfer is performed by two times. Example of timing sequence is shown below.

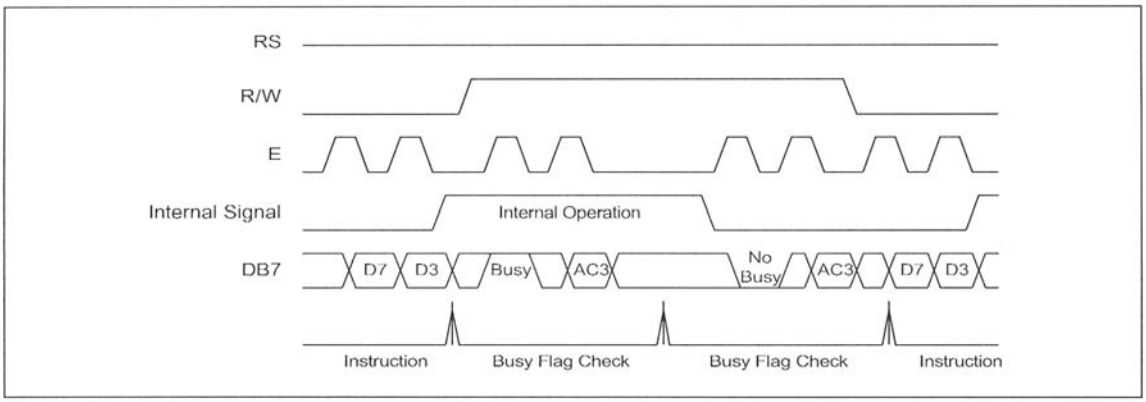
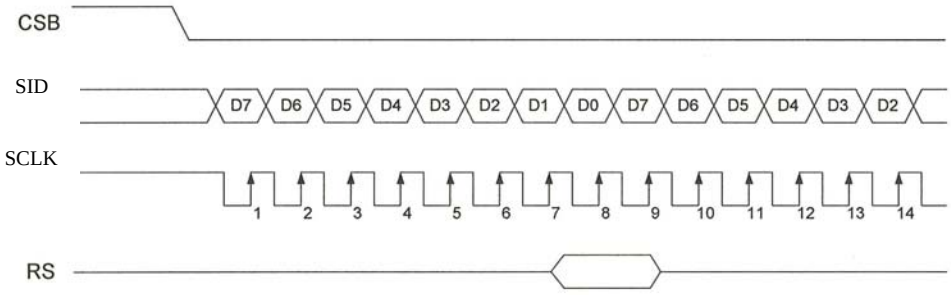


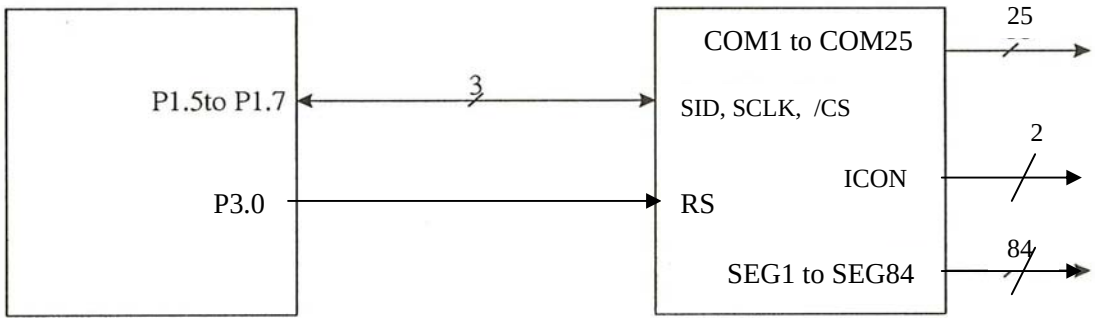
Figure 6. Example of 4-bit Bus Mode Timing Sequence

For serial interface data, bus lines (DB5 to DB7) are used. 4-Pin SPI

Example of timing sequence



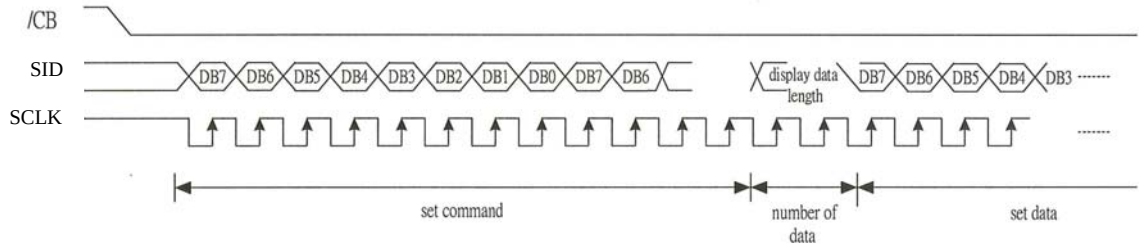
Intel 8051 interface (Serial)



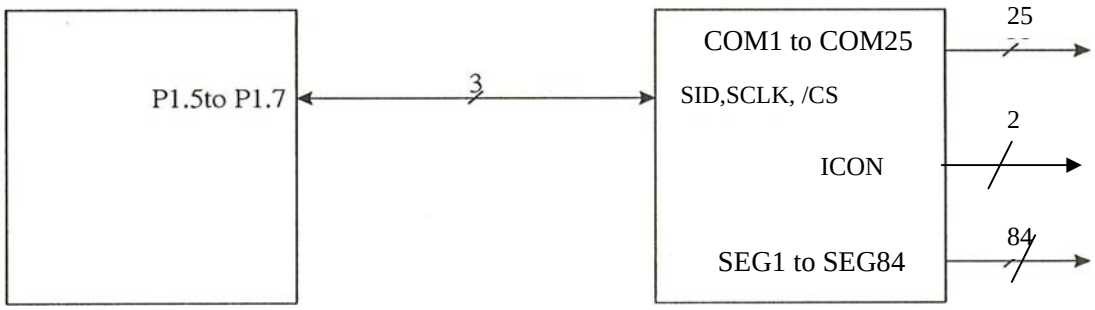
Intel 8051 Serial RW1068

For serial interface data, bus lines (DB5 to DB7) are used. 3 – Pin SPI

Example of timing sequence



Intel 8051 interface (Serial)



Intel 8051 Serial **RW1068**

INITIALIZING

INITIALIZING BY INTERNAL RESET CIRCUIT
When the power is turned on, RW1068 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF (Busy Flag) is kept "High"(busy state) to the end of initialization.

Display Clear Instruction
Write "20H" to all DDRAM

Set Functions Instruction
IF = 1: 8-bit bus mode
RE = 0: Extension register disable
BE = 0: CGRAM/SEGRAM blink OFF
DC = 0: Code bank selection enable
REV = 0: Normal display (Not reversed display)

Control Display ON/OFF Instruction
D = 0: Display OFF
C = 0: Cursor OFF
B = 0: Blink OFF

Set Entry Mode Instruction
I/D = 1: Increment by 1
S = 0: No entire display shift
BID = 0: Normal direction segment port

Set Extension Function Instruction
B/W = 0: Normal cursor (11th line)

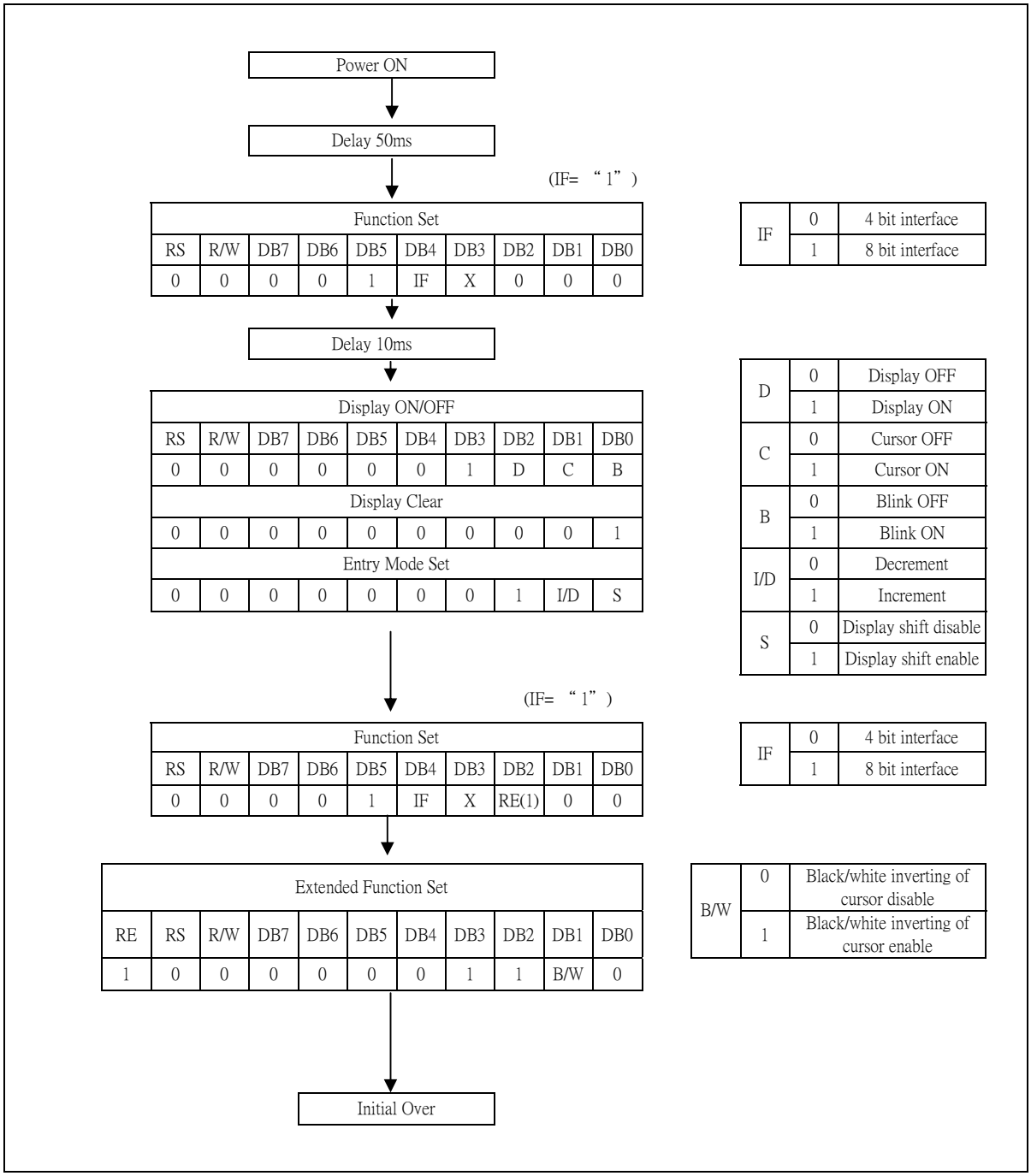
Enable Shift Instruction
DS=00

Set data length Instruction
SD = 000000

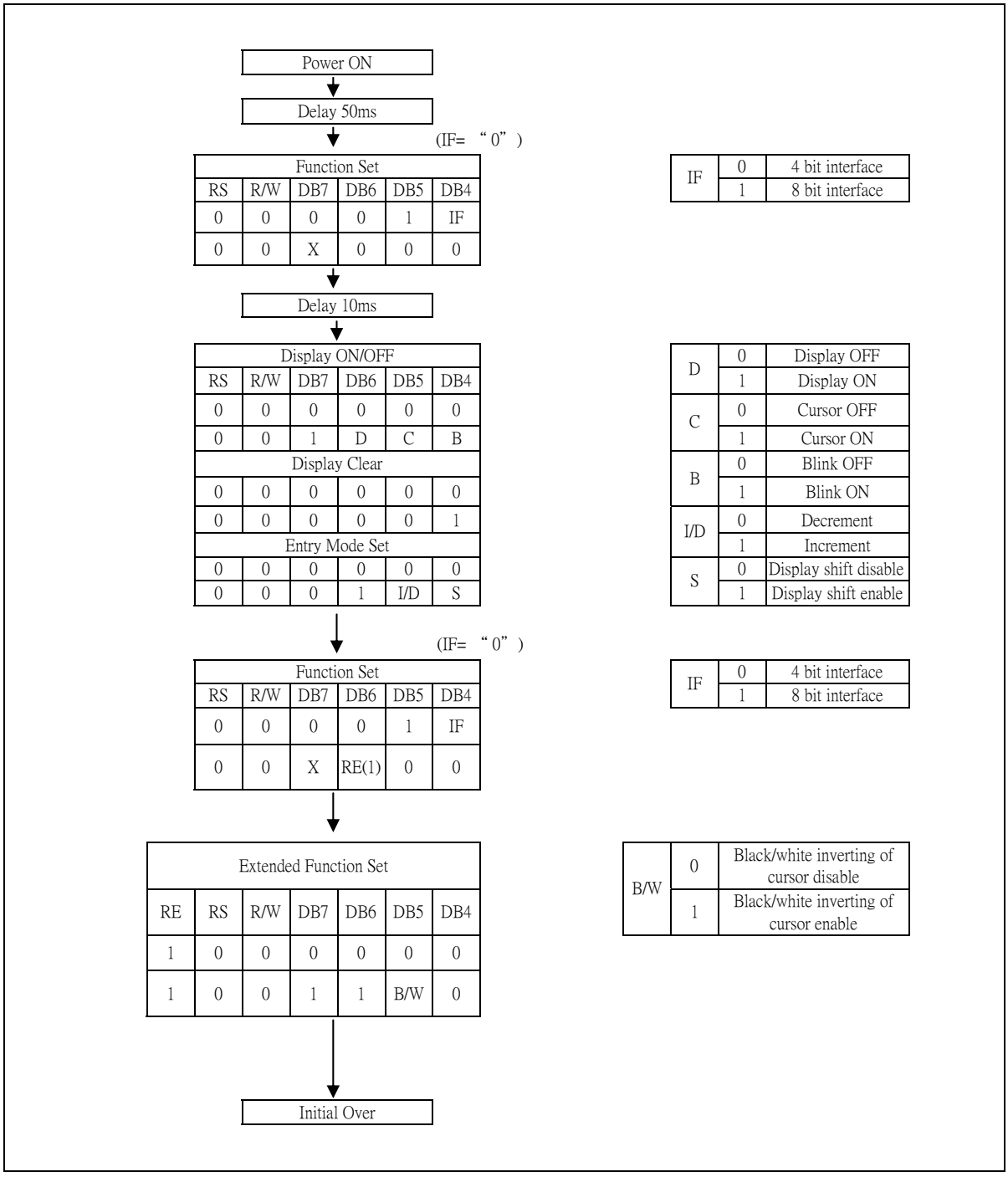
INITIALIZING BY HARDWARE RESET INPUT
When XRESET pin = "Low", RW1068 can be initialized like the case of power on reset. During the power on reset operation, this pin is ignored.

INITIALIZING BY INSTRUCTION

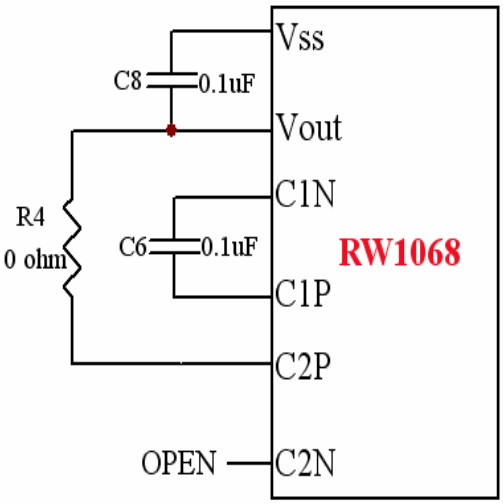
8-BIT INTERFACE MODE



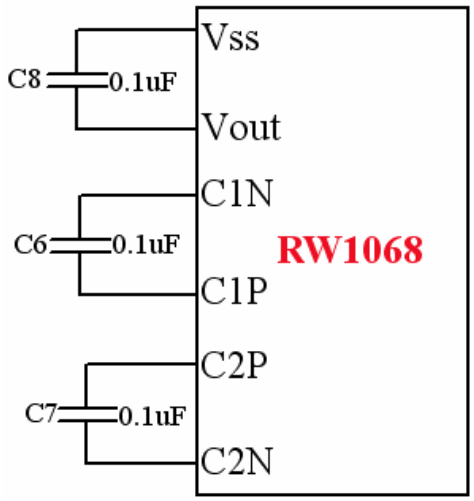
4 – BIT INTERFACE MODE



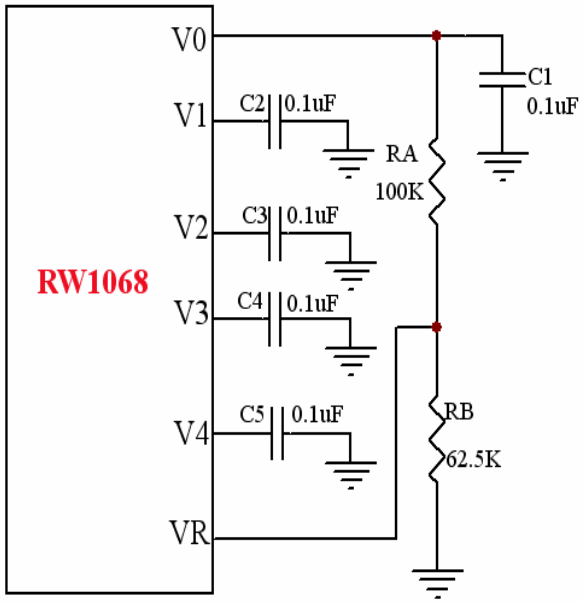
2x Step-up voltage circuit



3x Step-up voltage circuit



External connection



$$V0 = \frac{\frac{VDD}{2}}{RB} * (RA + RB)$$

Table 7. Duty Ratio and Power Supply for LCD Driving

Item	Data
Number of lines	2
Duty ratio	1/25
Bias	1/5

MAXIMUM ABSOLUTE RATE

Characteristic	Symbol	Value	Unit
Power supply voltage (1)	V_{DD}	-0.3 to +7.0	V
Power supply voltage (2)	V_{LCD}	V_{DD} -15.0 to V_{DD} + 0.3	V
Input voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Operation temperature	T_{OPR}	-30 to +85	°C
Storage temperature	T_{STG}	-55 to +125	°C

Voltage greater than above may damage to the circuit (VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (VDD = 2.7V to 5.5V, Ta = -30 to +85°C)

Characheristic	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-		2.7	-	5.5	V
Supply Current	I_{DD}	Internal oscillation or external clock (V_{DD} = 3.0V, fosc = 270kHz)		-	TBD	TBD	mA
Input voltage (1) (Except OSC1)	V_{IH1}	-		TBD	-	TBD	-
	V_{IL1}	V_{DD} = 2.7 - 3.0		TBD	-	TBD	
		V_{DD} = 3.0 - 5.5		TBD	-	TBD	
Input voltage (2) (OSC1)	V_{IH2}	-		TBD	-	TBD	V
	V_{IL2}	-		-	-	TBD	
Output voltage (1) (DB0 – DB7)	V_{OH1}	I_{OH} = -0.1 mA		TBD	-	-	V
	V_{OL1}	I_{OL} = 0.1 mA		-	-	TBD	
Output voltage (2) (Except DB0-DB7)	V_{OH2}	I_O = -40μA		TBD	-	-	V
	V_{OL1}	I_O= 40μA		-	-	TBD	
Voltage drop	Vd_{COM}	I_O = ±0.1mA		-	-	TBD	V
	Vd_{SEG}			-	-	TBD	
Input leakage current	I_{LKG}	V_{IN} = 0V - V_{DD}		TBD	-	TBD	μA
Low input current	I_{IL}	V_{IN} = 0V, V_{DD} = 3V (pull up)		TBD	TBD	TBD	
Internal clock (external Rf)	f_{OSC}	Rf = 91kΩ ± 2% (V_{DD} = 5V)		TBD	TBD	TBD	kHz
External clock	f_{EC}	-		TBD	TBD	TBD	kHz
	duty			TBD	TBD	TBD	%
	t_R, t_F			-	-	TBD	μs
Voltage converter out2 (Vci = 4.5V)	V_{OUT2}	Ta = 25°C, C = 0.1μF, I_{OUT} = 0.25mA, f_{OSC} = 270kHz		TBD	TBD	-	V
Voltage converter out3 (Vci = 2.7V)	V_{OUT3}			TBD	TBD	-	
Voltage converter input	Vci	-		TBD	-	TBD	V
LCD driving voltage	V_{LCD}	V_0-Vss	1/5 Bias	TBD	-	TBD	
			1/6.7 Bias	TBD	-	TBD	

AC Characteristics (Continued) (VDD = 2.7 to 4.5V, Ta = -30 to +85°C)

Table 8. AC Characteristics

Mode	Item	Symbol	Min	Typ	Max	Unit
(1) Write mode (refer to Figure 7)	E cycle time	tc	TBD	-	-	ns
	E rise/fall time	tr, tf	-	-	TBD	
	E pulse width (high, low)	tw	TBD	-	-	
	R/W and RS setup time	tsu1	TBD	-	-	
	R/W and RS hold time	th1	TBD	-	-	
	Data setup time	tsu2	TBD	-	-	
	Data hold time	th2	TBD	-	-	
(2) Read mode (refer to Figure 8)	E cycle time	tc	TBD	-	-	ns
	E rise/fall time	tr, tf	-	-	TBD	
	E pulse width (high, low)	tw	TBD	-	-	
	R/W and RS setup time	tsu	TBD	-	-	
	R/W and RS hold time	th	TBD	-	-	
	Data output delay time	t_D	-	-	TBD	
	Data hold time	t_{DH}	TBD	-	-	μs
(3) Serial interface Mode	Serial clock cycle time	t_C	TBD	-	TBD	ns
	Serial clock rise/fall time	tr, tf	-	-	TBD	
	Serial clock width (high, low)	tw	TBD	-	-	
	Chip select setup time	tsu1	TBD	-	-	
	Chip select hold time	th1	TBD	-	-	
	Serial input data setup time	tsu2	TBD	-	-	
	Serial input data hold time	th2	TBD	-	-	
	Serial output data delay time	t_D	-	-	TBD	
	Serial output data hold time	t_{DH}	TBD	-	-	

Table 9. AC Characteristics (Continued) (VDD = 2.7 to 4.5V, Ta = -30 to +85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(4) Write mode (refer to Figure 7)	E cycle time	tc	TBD	-	-	ns
	E rise/fall time	tr, tf	-	-	TBD	
	E pulse width (high, low)	tw	TBD	-	-	
	R/W and RS setup time	tsu1	TBD	-	-	
	R/W and RS hold time	th1	TBD	-	-	
	Data setup time	tsu2	TBD	-	-	
	Data hold time	th2	TBD	-	-	
(5) Read mode (refer to Figure 8)	E cycle time	tc,	TBD	-	-	ns
	E rise/fall time	tr, tf	-	-	TBD	
	E pulse width (high, low)	tw	TBD	-	-	
	R/W and RS setup time	tsu	TBD	-	-	
	R/W and RS hold time	th	TBD	-	-	
	Data output delay time	tD	-	-	TBD	
	Data hold time	tDH	TBD	-	-	μS
(6) Serial interface Mode	Serial clock cycle time	tC	TBD	-	TBD	ns
	Serial clock rise/fall time	tr, tf	-	-	TBD	
	Serial clock width (high, low)	tw	TBD	-	-	
	Chip select setup time	tsu1	TBD	-	-	
	Chip select hold time	th1	TBD	-	-	
	Serial input data setup time	tsu2	TBD	-	-	
	Serial input data hold time	th2	TBD	-	-	
	Serial output data delay time	tD	-	-	TBD	
	Serial output data hold time	tDH	TBD	-	-	

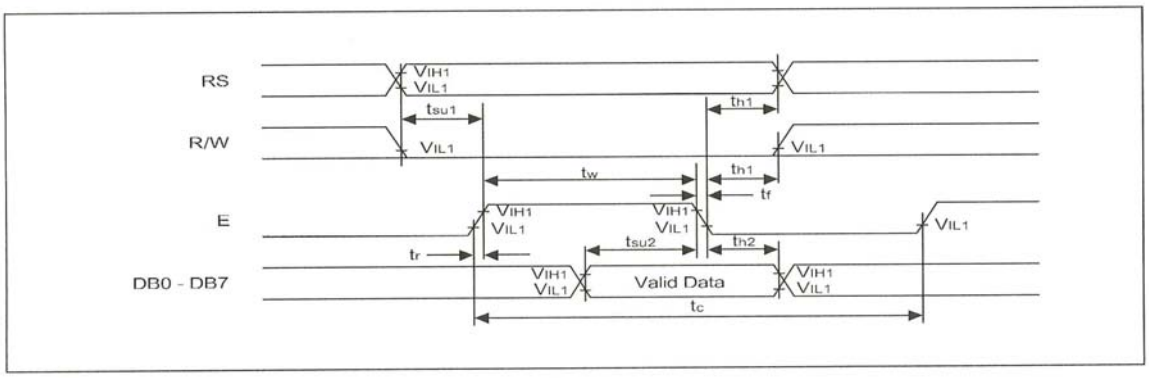


Figure 7 Write Mode

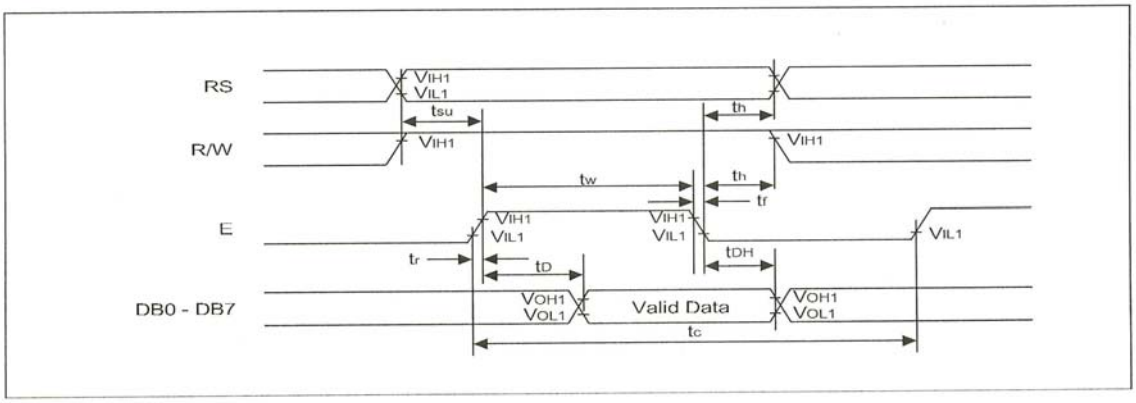


Figure 8 Read Mode

RESET TIMING (VDD = 2.7 to 5.5V, Ta = -30 to +85°C)

Item	Symbol	Min	Typ	Max	Unit
Reset low level width (refer to Figure 9)	t_{RES}	10	-	-	ms

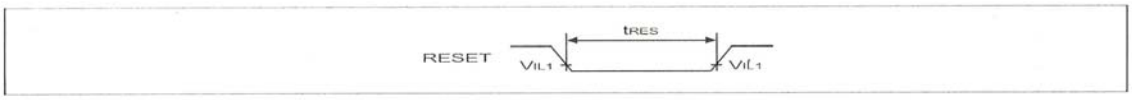


Figure 9. Reset Timing Diagram

Code Bank0

b7-b4 / b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	(2)															
0010	(3)															
0011	(4)															
0100	(5)															
0101	(6)															
0110	(7)															
0111	(8)															
1000	(1)															
1001	(2)															
1010	(3)															
1011	(4)															
1100	(5)															
1101	(6)															
1110	(7)															
1111	(8)															

Code Bank1

B7-B4 / B3-B0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	正	送	姓	者	下	打	尺	期	级	确	控	错	果	添	志	次
0001																
0010	在	第	待	按	情	印	寸	间	电	认	收	误	调	加	列	每
0011																
0100	拨	页	重	快	况	较	音	个	话	方	密	修	没	删	表	要
0101																
0110	号	传	秒	速	时	浅	铃	人	线	法	特	不	有	除	选	求
0111																
1000	已	真	输	钮	应	深	声	化	尝	适	色	响	低	改	择	最
1001																
1010	连	完	入	出	答	空	编	报	试	合	前	之	中	您	频	毫
1011																
1100	接	毕	码	现	质	白	辑	告	隔	面	扫	后	上	的	脉	米
1101																
1110	发	等	或	以	量	纸	日	高	转	遥	描	如	午	名	冲	处
1111																

Code Bank2

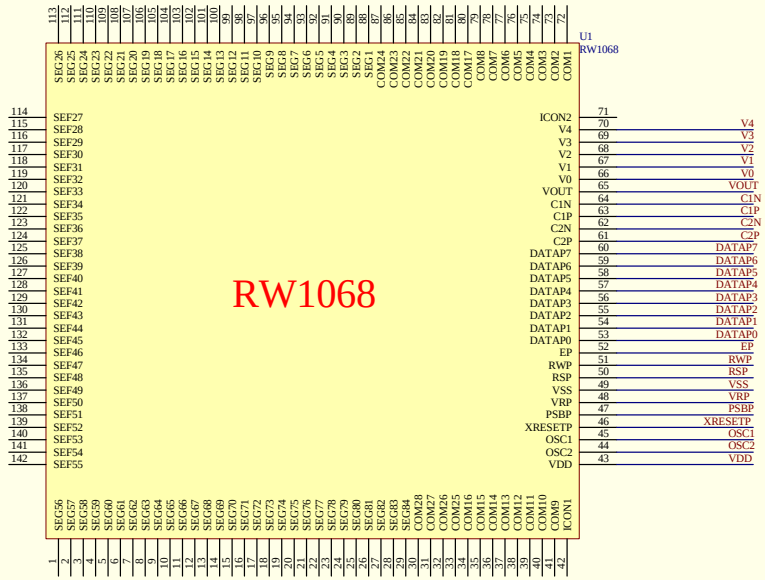
B7-B4 / B3-B0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	裁	被	使	别	准	图	份	小	半	彩	节	检	透	立	牙	波
0001																
0010	数	张	消	功	好	像	复	放	卡	原	约	测	明	刻	意	俄
0011																
0100	和	未	稍	能	佳	缀	制	大	至	始	设	普	胶	厂	利	档
0101																
0110	无	指	候	失	模	自	海	实	从	容	置	通	条	当	荷	到
0111																
1000	记	定	存	败	式	动	镜	双	计	逐	默	涂	画	英	兰	剩
1001																
1010	住	断	满	路	纯	交	常	倍	算	黑	值	层	水	德	巴	余
1011																
1100	请	开	用	忙	文	换	保	义	类	墨	语	照	更	西	葡	校
1101																
1110	内	取	识	标	字	机	缩	一	型	盒	言	片	洗	班	萄	成
1111																

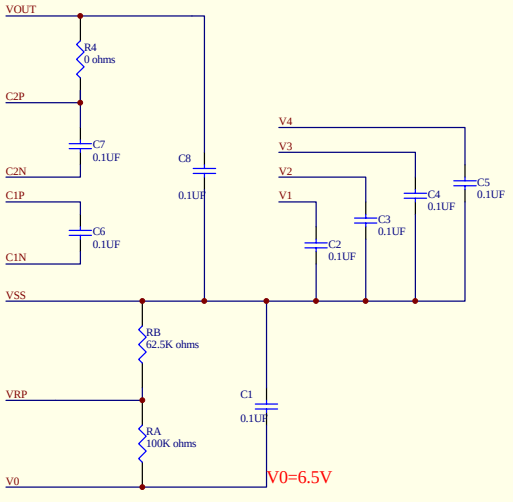
Code Bank3

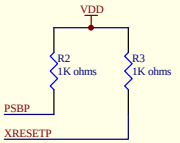
B7-B4 / B3-B0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	左	建	际	题	操	将	体	稿	版	关	装	C	S	i	y	>
0001												D	T	j	z	?
0010	右	偏	软	帮	作	多	简	光	剪	闭	然	E	U	k	0	!
0011												F	V	l	1	"
0100	盖	解	程	助	继	变	假	学	贴	并	清	G	W	m	2	#
0101												H	X	n	3	$
0110	旧	仪	序	信	项	露	演	符	板	全	架	I	Y	o	4	%
0111												J	Z	p	5	&
1000	新	锁	侧	息	再	撕	示	讯	续	部	固	K	a	q	6	’
1001												L	b	r	7	(
1010	产	硬	参	停	进	掉	器	簿	地	源	议	M	c	s	8	)
1011												N	d	t	9	*
1100	品	件	阅	止	行	封	理	管	分	预	繁	O	e	u	:	+
1101												P	f	v	;	,
1110	创	子	问	此	为	支	网	桌	钟	热	A	Q	g	w	<	–
1111																

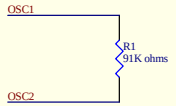
3X step-up voltage: Put C7 between C2P and C2N,NO R4

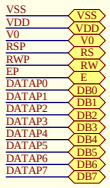
2X step-up voltage: Put R4 between Vout and C2P,NO C7











PIN1	VSS
PIN2	VDD
PIN3	V0
PIN4	RS
PIN5	RW
PIN6	E
PIN7	DB0
PIN8	DB1
PIN9	DB2
PIN10	DB3
PIN11	DB4
PIN12	DB5
PIN13	DB6
PIN14	DB7

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