## INTRODUCTION

The S6A0070 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It is capable of displaying 1 or 2 lines with the 5 × 7 format or 1 line with the 5 × 10 dots format.

The mirror type of S6A0070: S6A1070

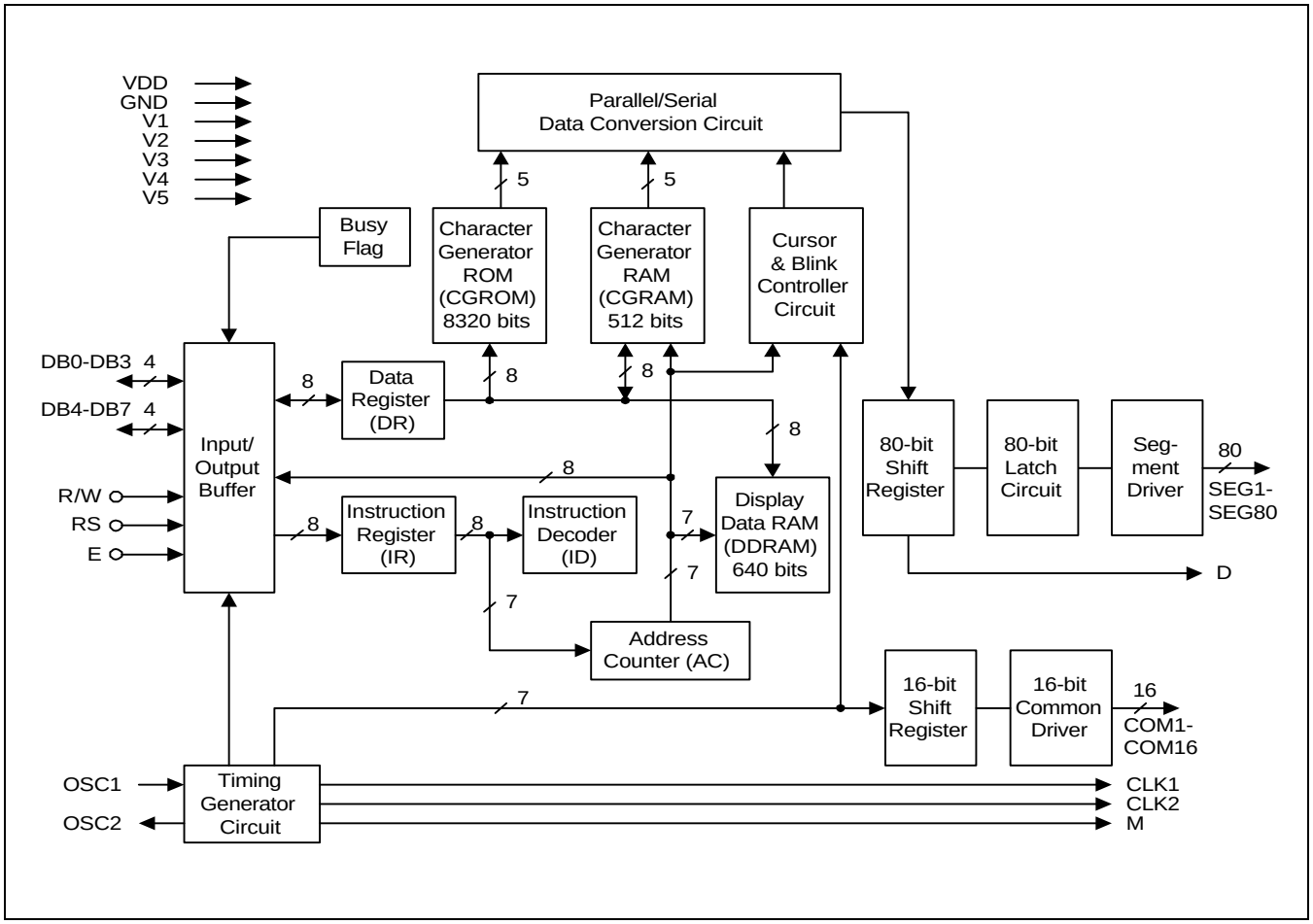
## FUNCTION

- Character type dot matrix LCD driver & controller
- Internal driver: 16 common and 80 segment signal output
- Easy Interface with a 4-bit or 8-bit MPU
- Display character pattern: 5 × 7 dots format (192 kinds), 5 × 10 dots format (32 kinds)
- The special character pattern is directly programmable by the Character Generator RAM.
- A customer character pattern is programmable by mask option.
- It can drive a maximum 80 characters by using the S6A0065 or S6A2067 externally.
- Various instruction functions
- Built-in automatic power on reset
- Driving method is A-type (line inversion)

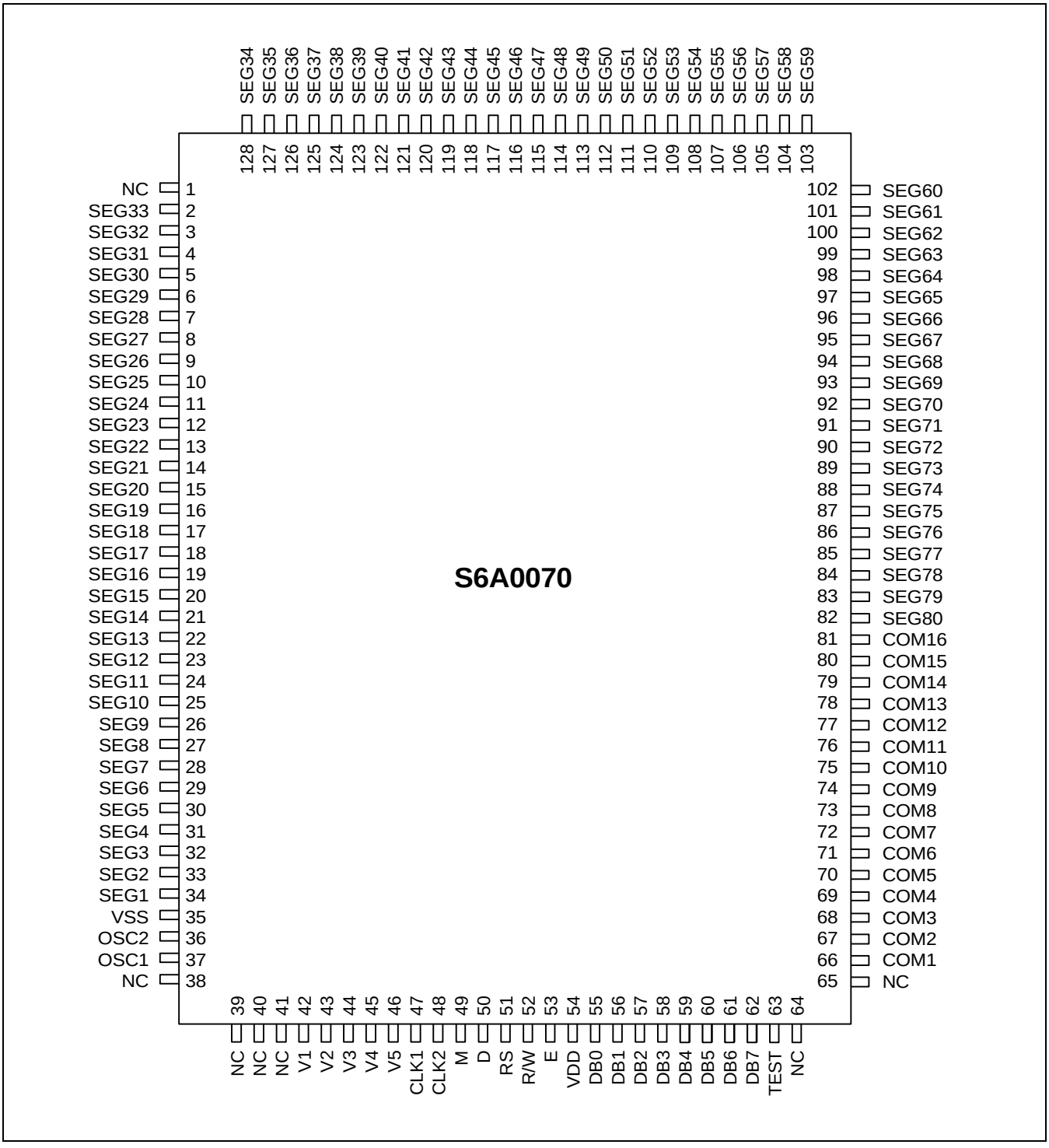
## FEATURES

- Internal Memory
  - Character Generator ROM: 8320bits (192 cha. X 5 x 7 dots) & (32 cha. X 5 x 10 dots)
  - Character Generator RAM: 64 x 8 bits (8 cha. X 5 x 7 dots)
  - Display Data RAM: 80 × 8 bits for 80 digits (80 characters max.)
- Power Supply Voltage: 2.7 to 5.5 V (VDD)
- LCD Driving Voltage: 3.0 to 10.0 V (VDD - V5)
- Supply Voltage for display: 0 to -5V (V5)
- Programmable duty cycle: 1/8 duty, 1/11 duty or 1/16
- Internal oscillator with an external resistor
- Bare die or bumped chip available

## BLOCK DIAGRAM

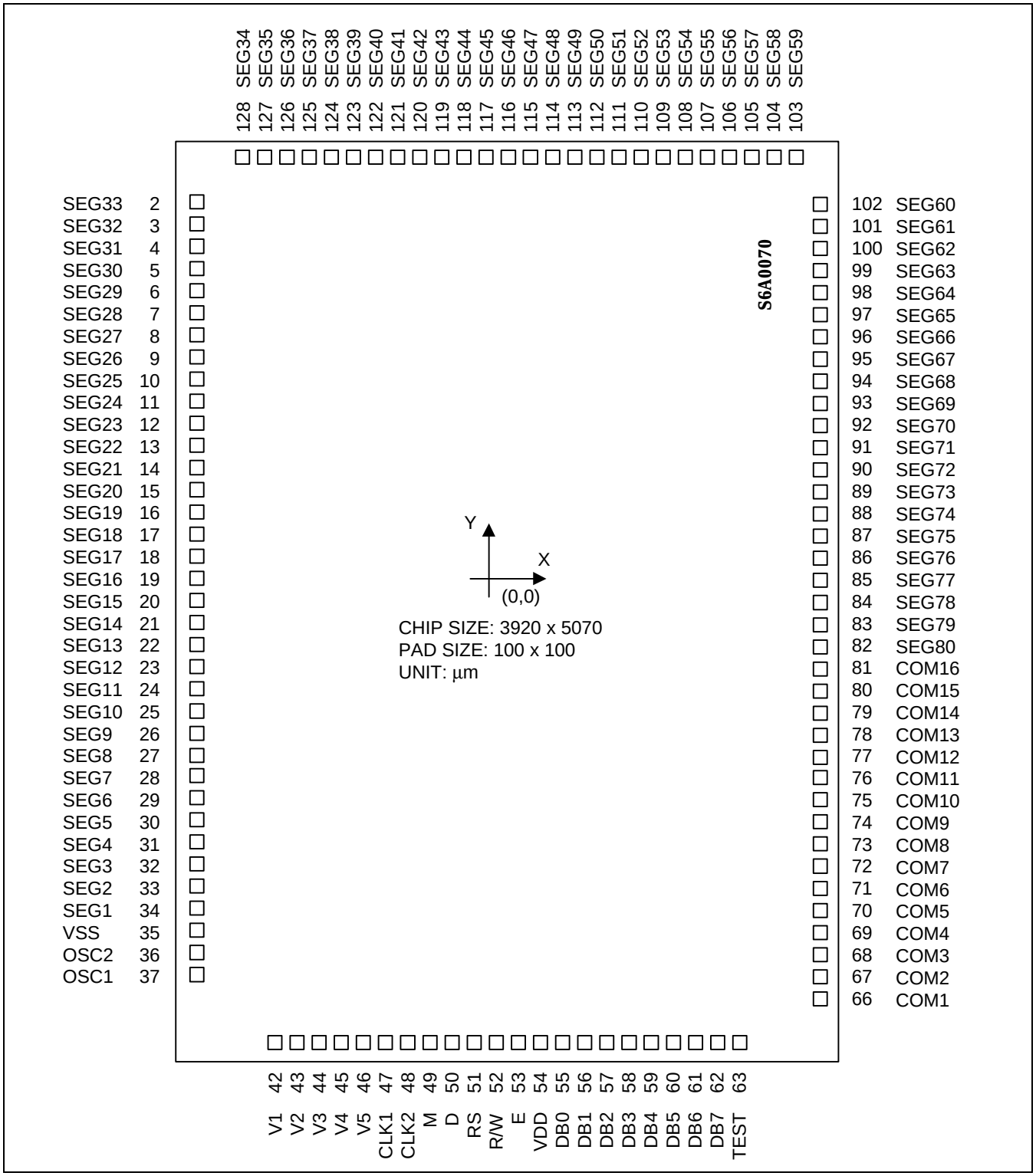


## PIN CONFIGURATION

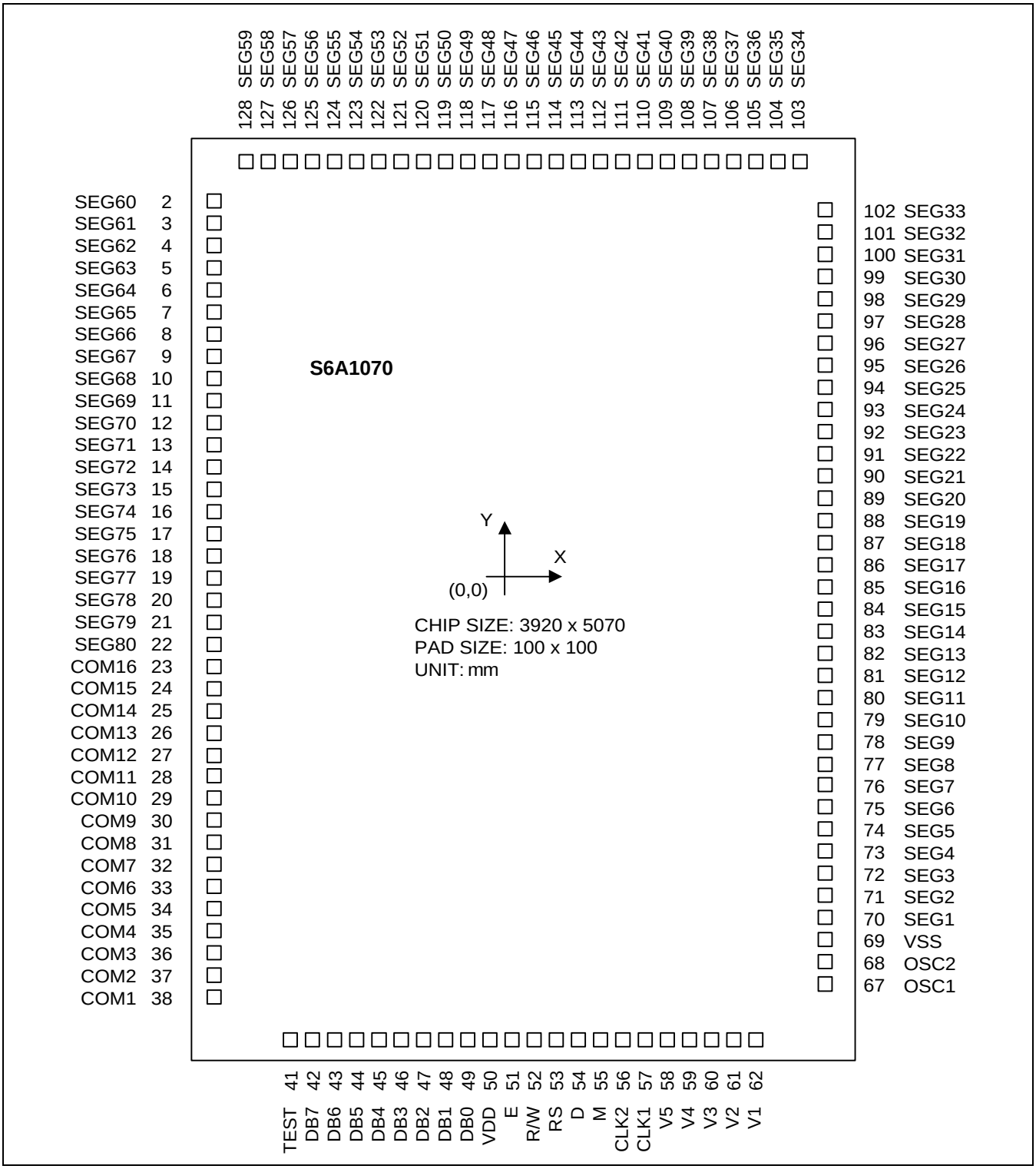


## PAD CONFIGURATION

### 1) Normal Type PAD Configuration



## 2) Mirror Type PAD Configuration



## PAD CENTER COORDINATES

### 1) Normal Type PAD Coordinate (S6A0070)

| PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | NC | | | 44 | V3 | -905 | -2369 | 87 | SEG75 | 1794 | 294 |
| 2 | SEG33 | -1794 | 2169 | 45 | V4 | -780 | -2369 | 88 | SEG74 | 1794 | 419 |
| 3 | SEG32 | -1794 | 2044 | 46 | V5 | -655 | -2369 | 89 | SEG73 | 1794 | 544 |
| 4 | SEG31 | -1794 | 1919 | 47 | CLK1 | -530 | -2369 | 90 | SEG72 | 1794 | 669 |
| 5 | SEG30 | -1794 | 1794 | 48 | CLK2 | -405 | -2369 | 91 | SEG71 | 1794 | 794 |
| 6 | SEG29 | -1794 | 1669 | 49 | M | -280 | -2369 | 92 | SEG70 | 1794 | 919 |
| 7 | SEG28 | -1794 | 1544 | 50 | D | -155 | -2369 | 93 | SEG69 | 1794 | 1044 |
| 8 | SEG27 | -1794 | 1419 | 51 | RS | -30 | -2369 | 94 | SEG68 | 1794 | 1169 |
| 9 | SEG26 | -1794 | 1294 | 52 | R/W | 95 | -2369 | 95 | SEG67 | 1794 | 1294 |
| 10 | SEG25 | -1794 | 1169 | 53 | E | 220 | -2369 | 96 | SEG66 | 1794 | 1419 |
| 11 | SEG24 | -1794 | 1044 | 54 | VDD | 345 | -2369 | 97 | SEG65 | 1794 | 1544 |
| 12 | SEG23 | -1794 | 919 | 55 | DB0 | 470 | -2369 | 98 | SEG64 | 1794 | 1669 |
| 13 | SEG22 | -1794 | 794 | 56 | DB1 | 595 | -2369 | 99 | SEG63 | 1794 | 1794 |
| 14 | SEG21 | -1794 | 669 | 57 | DB2 | 720 | -2369 | 100 | SEG62 | 1794 | 1919 |
| 15 | SEG20 | -1794 | 544 | 58 | DB3 | 845 | -2369 | 101 | SEG61 | 1794 | 2044 |
| 16 | SEG19 | -1794 | 419 | 59 | DB4 | 970 | -2369 | 102 | SEG60 | 1794 | 2169 |
| 17 | SEG18 | -1794 | 294 | 60 | DB5 | 1095 | -2369 | 103 | SEG59 | 1563 | 2369 |
| 18 | SEG17 | -1794 | 169 | 61 | DB6 | 1220 | -2369 | 104 | SEG58 | 1438 | 2369 |
| 19 | SEG16 | -1794 | 44 | 62 | DB7 | 1345 | -2369 | 105 | SEG57 | 1313 | 2369 |
| 20 | SEG15 | -1794 | -81 | 63 | TEST | 1470 | -2369 | 106 | SEG56 | 1188 | 2369 |
| 21 | SEG14 | -1794 | -206 | 64 | NC | | | 107 | SEG55 | 1063 | 2369 |
| 22 | SEG13 | -1794 | -331 | 65 | NC | | | 108 | SEG54 | 938 | 2369 |
| 23 | SEG12 | -1794 | -456 | 66 | COM1 | 1794 | -2331 | 109 | SEG53 | 813 | 2369 |
| 24 | SEG11 | -1794 | -581 | 67 | COM2 | 1794 | -2206 | 110 | SEG52 | 688 | 2369 |
| 25 | SEG10 | -1794 | -706 | 68 | COM3 | 1794 | -2081 | 111 | SEG51 | 563 | 2369 |
| 26 | SEG9 | -1794 | -831 | 69 | COM4 | 1794 | -1956 | 112 | SEG50 | 438 | 2369 |
| 27 | SEG8 | -1794 | -956 | 70 | COM5 | 1794 | -1831 | 113 | SEG49 | 313 | 2369 |
| 28 | SEG7 | -1794 | -1081 | 71 | COM6 | 1794 | -1706 | 114 | SEG48 | 188 | 2369 |
| 29 | SEG6 | -1794 | -1206 | 72 | COM7 | 1794 | -1581 | 115 | SEG47 | 63 | 2369 |
| 30 | SEG5 | -1794 | -1331 | 73 | COM8 | 1794 | -1456 | 116 | SEG46 | -62 | 2369 |

**Normal Type Pad Coordinate (Continued)**

| PAD | PAD | COORDINATE | | PAD | PAD | COORDINATE | | PAD | PAD | COORDINATE | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| NUM. | NAME | X | Y | NUM. | NAME | X | Y | NUM. | NAME | X | Y |
| 31 | SEG4 | -1794 | -1456 | 74 | COM9 | 1794 | -1331 | 117 | SEG45 | -187 | 2369 |
| 32 | SEG3 | -1794 | -1581 | 75 | COM10 | 1794 | -1206 | 118 | SEG44 | -312 | 2369 |
| 33 | SEG2 | -1794 | -1706 | 76 | COM11 | 1794 | -1081 | 119 | SEG43 | -437 | 2369 |
| 34 | SEG1 | -1794 | -1831 | 77 | COM12 | 1794 | -956 | 120 | SEG42 | -562 | 2369 |
| 35 | VSS | -1794 | -1956 | 78 | COM13 | 1794 | -831 | 121 | SEG41 | -687 | 2369 |
| 36 | OSC2 | -1794 | -2106 | 79 | COM14 | 1794 | -706 | 122 | SEG40 | -812 | 2369 |
| 37 | OSC1 | -1794 | -2231 | 80 | COM15 | 1794 | -581 | 123 | SEG39 | -937 | 2369 |
| 38 | NC | | | 81 | COM16 | 1794 | -456 | 124 | SEG38 | -1062 | 2369 |
| 39 | NC | | | 82 | SEG80 | 1794 | -331 | 125 | SEG37 | -1187 | 2369 |
| 40 | NC | | | 83 | SEG79 | 1794 | -206 | 126 | SEG36 | -1312 | 2369 |
| 41 | NC | | | 84 | SEG78 | 1794 | -81 | 127 | SEG35 | -1437 | 2369 |
| 42 | V1 | -1155 | -2369 | 85 | SEG77 | 1794 | 44 | 128 | SEG34 | -1562 | 2369 |
| 43 | V2 | -1030 | -2369 | 86 | SEG76 | 1794 | 169 | | | | |

* “S6A0070” Marking: easy to find the PAD No. 98.

### 2) Mirror Type PAD Coordinate (S6A1070)

| PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | NC | | | 44 | DB5 | -1095 | -2369 | 87 | SEG18 | 1794 | 294 |
| 2 | SEG60 | -1794 | 2169 | 45 | DB4 | -970 | -2369 | 88 | SEG19 | 1794 | 419 |
| 3 | SEG61 | -1794 | 2044 | 46 | DB3 | -845 | -2369 | 89 | SEG20 | 1794 | 544 |
| 4 | SEG62 | -1794 | 1919 | 47 | DB2 | -720 | -2369 | 90 | SEG21 | 1794 | 669 |
| 5 | SEG63 | -1794 | 1794 | 48 | DB1 | -595 | -2369 | 91 | SEG22 | 1794 | 794 |
| 6 | SEG64 | -1794 | 1669 | 49 | DB0 | -470 | -2369 | 92 | SEG23 | 1794 | 919 |
| 7 | SEG65 | -1794 | 1544 | 50 | VDD | -345 | -2369 | 93 | SEG24 | 1794 | 1044 |
| 8 | SEG66 | -1794 | 1419 | 51 | E | -220 | -2369 | 94 | SEG25 | 1794 | 1169 |
| 9 | SEG67 | -1794 | 1294 | 52 | RW | -95 | -2369 | 95 | SEG26 | 1794 | 1294 |
| 10 | SEG68 | -1794 | 1169 | 53 | RS | 30 | -2369 | 96 | SEG27 | 1794 | 1419 |
| 11 | SEG69 | -1794 | 1044 | 54 | D | 155 | -2369 | 97 | SEG28 | 1794 | 1544 |
| 12 | SEG70 | -1794 | 919 | 55 | M | 280 | -2369 | 98 | SEG29 | 1794 | 1669 |
| 13 | SEG71 | -1794 | 794 | 56 | CLK2 | 405 | -2369 | 99 | SEG30 | 1794 | 1794 |
| 14 | SEG72 | -1794 | 669 | 57 | CLK1 | 530 | -2369 | 100 | SEG31 | 1794 | 1919 |
| 15 | SEG73 | -1794 | 544 | 58 | V5 | 655 | -2369 | 101 | SEG32 | 1794 | 2044 |
| 16 | SEG74 | -1794 | 419 | 59 | V4 | 780 | -2369 | 102 | SEG33 | 1794 | 2169 |
| 17 | SEG75 | -1794 | 294 | 60 | V3 | 905 | -2369 | 103 | SEG34 | 1562 | 2369 |
| 18 | SEG76 | -1794 | 169 | 61 | V2 | 1030 | -2369 | 104 | SEG35 | 1437 | 2369 |
| 19 | SEG77 | -1794 | 44 | 62 | V1 | 1155 | -2369 | 105 | SEG36 | 1312 | 2369 |
| 20 | SEG78 | -1794 | -81 | 63 | NC | | | 106 | SEG37 | 1187 | 2369 |
| 21 | SEG79 | -1794 | -206 | 64 | NC | | | 107 | SEG38 | 1062 | 2369 |
| 22 | SEG80 | -1794 | -331 | 65 | NC | | | 108 | SEG39 | 937 | 2369 |
| 23 | C16 | -1794 | -456 | 66 | NC | | | 109 | SEG40 | 812 | 2369 |
| 24 | C15 | -1794 | -581 | 67 | OSC1 | 1794 | -2231 | 110 | SEG41 | 687 | 2369 |
| 25 | C14 | -1794 | -706 | 68 | PSC2 | 1794 | -2106 | 111 | SEG42 | 562 | 2369 |
| 26 | C13 | -1794 | -831 | 69 | VSS | 1794 | -1956 | 112 | SEG43 | 437 | 2369 |
| 27 | C12 | -1794 | -956 | 70 | SEG1 | 1794 | -1831 | 113 | SEG44 | 312 | 2369 |
| 28 | C11 | -1794 | -1081 | 71 | SEG2 | 1794 | -1706 | 114 | SEG45 | 187 | 2369 |
| 29 | C10 | -1794 | -1206 | 72 | SEG3 | 1794 | -1581 | 115 | SEG46 | 62 | 2369 |
| 30 | C9 | -1794 | -1331 | 73 | SEG4 | 1794 | -1456 | 116 | SEG47 | -63 | 2369 |
| 31 | C8 | -1794 | -1456 | 74 | SEG5 | 1794 | -1331 | 117 | SEG48 | -188 | 2369 |
| 32 | C7 | -1794 | -1581 | 75 | SEG6 | 1794 | -1206 | 118 | SEG49 | -313 | 2369 |
| 33 | C6 | -1794 | -1706 | 76 | SEG7 | 1794 | -1081 | 119 | SEG50 | -438 | 2369 |

**Mirror Type Pad Coordinate (Continued)**

| PAD | PAD | COORDINATE | | PAD | PAD | COORDINATE | | PAD | PAD | COORDINATE | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| NUM. | NAME | X | Y | NUM. | NAME | X | Y | NUM. | NAME | X | Y |
| 34 | COM5 | -1794 | -1831 | 77 | SEG8 | 1794 | -956 | 120 | SEG51 | -563 | 2369 |
| 35 | COM4 | -1794 | -1956 | 78 | SEG9 | 1794 | -831 | 121 | SEG52 | -688 | 2369 |
| 36 | COM3 | -1794 | -2081 | 79 | SEG10 | 1794 | -706 | 122 | SEG53 | -813 | 2369 |
| 37 | COM2 | -1794 | -2206 | 80 | SEG11 | 1794 | -581 | 123 | SEG54 | -938 | 2369 |
| 38 | COM1 | -1794 | -2331 | 81 | SEG12 | 1794 | -456 | 124 | SEG55 | -1063 | 2369 |
| 39 | NC | | | 82 | SEG13 | 1794 | -331 | 125 | SEG56 | -1188 | 2369 |
| 40 | NC | | | 83 | SEG14 | 1794 | -206 | 126 | SEG57 | -1313 | 2369 |
| 41 | TEST | -1470 | -2369 | 84 | SEG15 | 1794 | -81 | 127 | SEG58 | -1438 | 2369 |
| 42 | DB7 | -1345 | -2369 | 85 | SEG16 | 1794 | 44 | 128 | SEG59 | -1563 | 2369 |
| 43 | DB6 | -1220 | -2369 | 86 | SEG17 | 1794 | 169 | | | | |

* “S6A1070” Marking: easy to find the PAD No. 12.

## PIN DESCRIPTION

| Pad (No) (normal/mirror) | I/O | Name | Description | Interface |
|---|---|---|---|---|
| $V_{DD}$(54/50) | - | Power supply | for logical circuit (+3V, +5V) | Power supply |
| $V_{SS}$(35, 69) | | | 0V (GND) | |
| V1-V5 (42-46/62-58) | | Power supply | Bias voltage level for LCD driving | |
| SEG1-SEG80 (34-2, 128-82/ 70-128, 2-28 | Output | Segment output | Segment signal output for LCD driving | LCD |
| COM1-COM16 (66-81/38-23) | Output | Common output | Common signal output for LCD driving | LCD |
| OSC1, OSC2 (37, 36/67, 68) | Input (OSC1) Output (OSC2) | Oscillator | When using internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1. | Extension register/ oscillator (OSC1) |
| CLK1, CLK2 (47, 48/57, 56) | Output | Extension driver latch (CLK1)/Shift (CLK2) clock | Each outputs extension driver latch clock and extension driver shift clock | Extension driver |
| M (49/55) | Output | Alternated signal for LCD driver output | Outputs the alternating signal to convert LCD driver waveform to AC. | Extension driver |
| D (50/54) | Output | Display data interface | Output extension driver data (the 41st dot's data) | Extension driver |
| RS (51/53) | Input | Register select | Used s register selection input. When RS = 1, Data register is selected. When RS = 0, Instruction register is selected | MPU |
| RW (52/52) | Input | Read/Write | Used as read/write selection input. When RW = 1, read operation. When RW = 0, write operation. | MPU |
| E (53/51) | Input | Read/Write Enable | Used as read. Write enable signal. | MPU |
| DB0-DB3 (55-58/49-46) | Input/ Output | Data bus 0-3 | When 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode open these pins. | MPU |
| DB4-DB7 (59-62/45-42) | Input/ Output | Data bus 4-7 | When 8-bit bus mode, used as high order bidirectional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. | MPU |
| TEST(63/41) | Input | Test pin | This pin must be fixed to VDD or open. | - |

# FUNCTION DESCRIPTION

### System Interface

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bits bus. 4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DRAM/CGRAM . Target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. After MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The instruction register (IR) is used only to store instruction codes transferred from MPU. MPU cannot use it to read instruction data.

To select a register, use RS input pin in 4-bit/8-bit bus mode.

Table 1. Various Kinds of Operations to RS and R/W bits.

| RS | R/W | Operation |
|---|---|---|
| 0 | 0 | Instruction Write operation (MPU writes instruction code into IR) |
| 0 | 1 | Read Busy flag (DB7) and address counter (DB0 - DB7) |
| 1 | 0 | Data Write operation (MPU writes data into DR) |
| 1 | 1 | Data Read operation (MPU reads data into DR) |

### Busy Flag (BF)

When BF = 1, it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = 0, and R/W = 1. (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not 1.

### Address Counter (AC)

The Address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR. After writing into (reading from) DDRAM/CGRAM. AC is automatically increased (decreased) by 1. When RS = 0 and R/W = 1, AC can be read through ports DB0 - DB6.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characteristics). DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to fig-1).

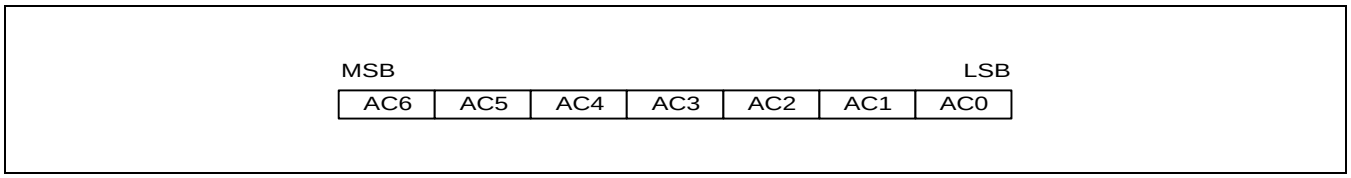



**Figure 1. DDRAM Address**

1) 1-line Display

In the case of a 1-line display, the address range of DDRAM is 00H - 04H. An Extension driver will be used. Figure 2 shows the example when a 40-segment extension driver is added.

2) 2-line Display

In the case of a 2-line display, the address range of DDRAM is 00H - 27H and 40H - 67H. An Extension driver will be used. Figure 3 shows the example a 40 segment extension driver is added.

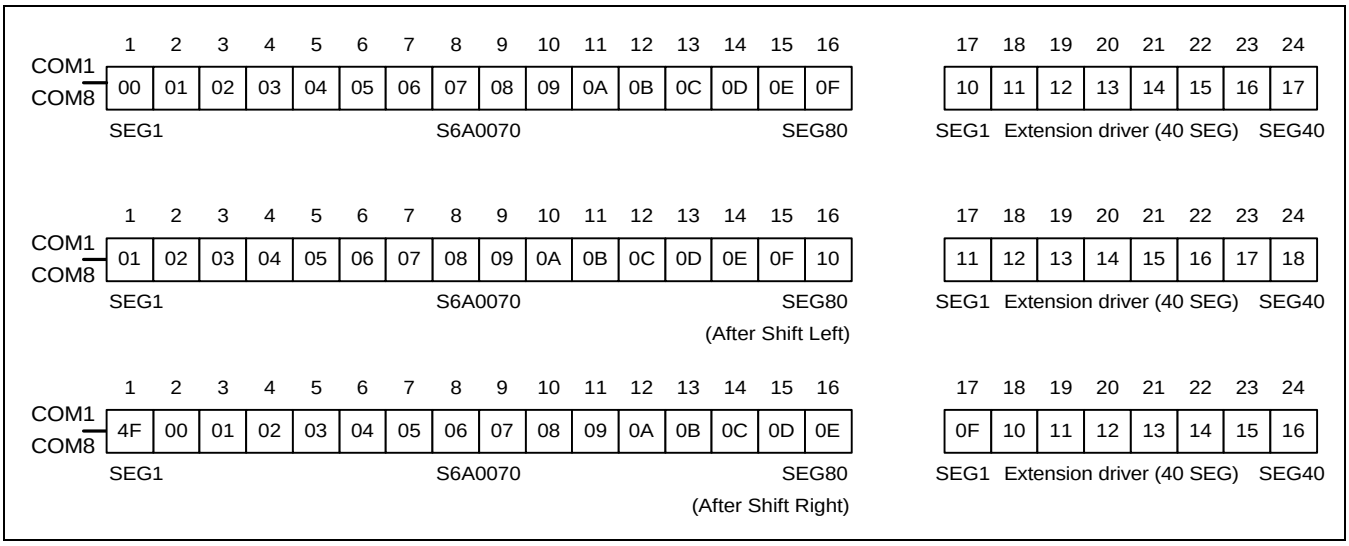



**Figure 2. 1-line x 24ch. Display with 40 SEG. Extension Driver**

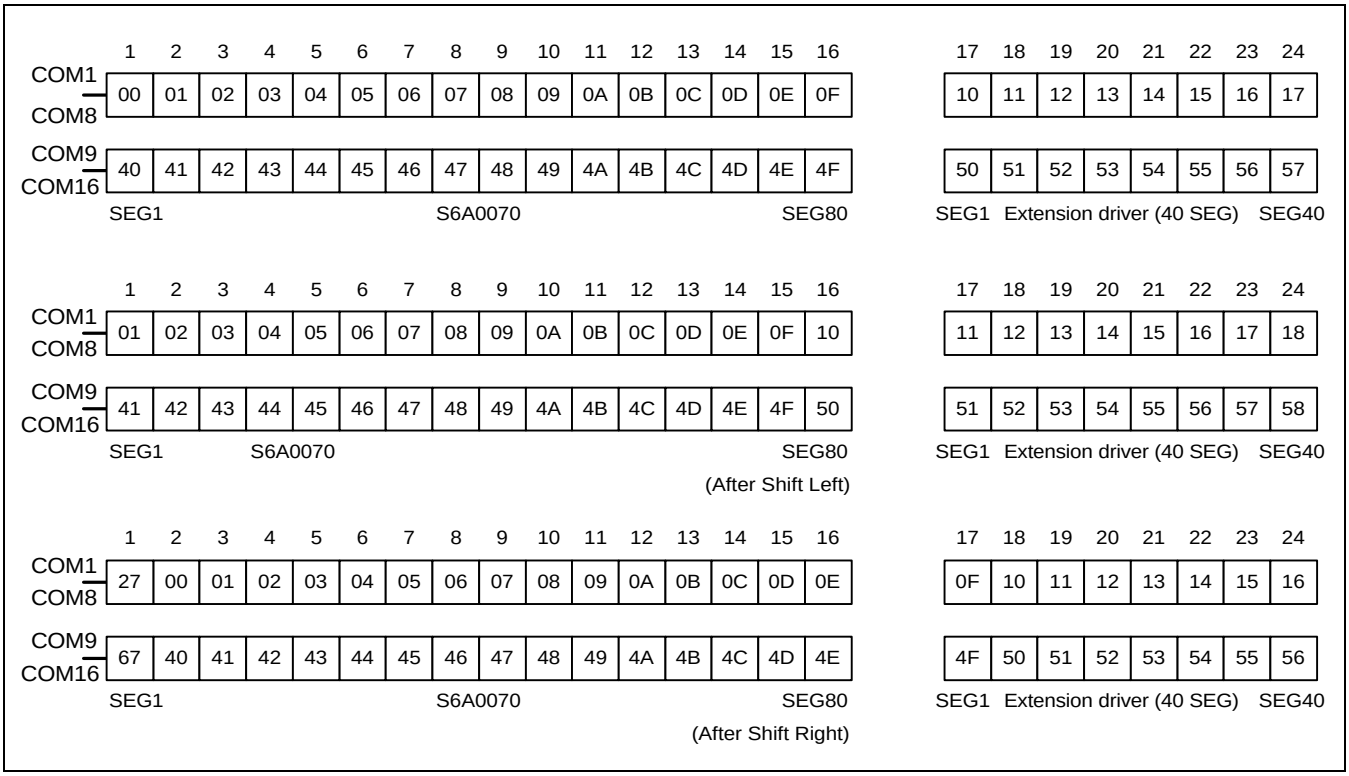



**Figure 3. 2-line x 24ch. Display with 40 SEG. Extension Driver**

### CGROM (Characteristic Generator ROM)

CGROM has a 5 x 7 dots 192 character pattern, and a 5 x 7 10 dots 32 character pattern

### CGRAM (Character Generator RAM)

CDRAM has up to 5 x 8 dots 8 characters. By writing font data to CGRAM, user defined characters can be used (Refer to table 3).

### Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

### LCD Driver Circuit

LCD Driver circuit has 16 common and 80 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to an 80-bit segment latch serially, and then stored to an 80-bit shift latch. When each com is selected by a 16-bit common register, segment data is also output through the segment driver from and 80-bit segment latch. In case of a 1-line display mode, COM - COM8 have 1/8 duty or COM1-COM11 have a 1/11 duty. In a 2-line display mode, COM1 - COM16 have a 1/16 duty ratio.

### Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at cursor position.

**Table 3. Relationship Between Character Code (DDRAM) and Character Pattern (CGROM)**

| Character Code (DDRAM data) | | | | | | | | CGRAM Address | | | | | | CGRAM Data | | | | | | | | Pattern number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | |
| 0 | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | 0 | 1 | 1 | 1 | 0 | Pattern 1 |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | 1 | 0 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |
| | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | x | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | x | x | x | 1 | 0 | 0 | 0 | 1 | Pattern 8 |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 1 | 1 | 1 | 1 | 1 | |
| | | | | | | | | | | | 1 | 0 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |

"x": Don't care.

# INSTRUCTION DESCRIPTION

## OUTLINE

To overcome the speed difference between internal clock of S6A0070 and MPU clock, S6A0070 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 5) Instruction can be divided largely four kinds,

(1) S6A0070 function set instructions (set display methods, set data length, etc.)

(2) Address set instructions to internal RAM

(3) Data transfer instructions with internal RAM

(4) Others

The address of internal RAM is automatically increased or decreased by 1.

**NOTE:** During internal operation, Busy Flag (DB7) is read "1". Busy Flag check must be precede by the next instruction. When you make an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by falling E signal after the Busy Flag (DB7) goes to "0".

### Contents

### 1) Clear Display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" in the AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

### 2) Return Home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x |

Return Home is cursor return home instruction. Set DDRAM address to "00H" in the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

### 3) Entry Mode Set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH |

Set the moving direction of cursor and display.
I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = "1", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "0", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when reading from or writing to CGRAM.

**SH: Shift of Entire Display**
When DDRAM read (CGRAM read/write) operation or SH = "0", shift of entire display is not performed. If SH = "1" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

### 4) Display ON / OFF Control

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

**D : Display ON/OFF Control Bit**
When D = "1", entire display is turned on.
When D = "0", display is turned off, but display data remained in DDRAM.

**C : Cursor ON/OFF Control Bit**
When C = "1", cursor is turned on.
When C = "0", cursor is disappeared in current display, but I/D register remains its data.

**B : Cursor Blink ON/OFF Control Bit**
When B = "1", cursor blink is on, which performs alternate between all the "1" data and display character at the cursor position. When B = "0", blink is off.

### 5) Cursor or Display Shift

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | x | x |

Without waiting or reading the display data, shift right/left cursor position or display. This instruction is used to correct or search display data. (Refer to table 4) During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously in all the lines. When displayed data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

**Table 4. Shift Patterns According to S/C and R/L Bits**

| S/C | R/L | Operation |
|---|---|---|
| 0 | 0 | Shift cursor to the left, AC is decreased by 1 |
| 0 | 1 | Shift cursor to the right, AC is increased by 1 |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display |

### 6) Function Set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | DL | N | F | x | x |

**DL : Interface data length control bit**
When DL = "1", it means 8-bit bus mode with MPU.
When DL = "0", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data in two times.

**N : Display line number control bit**
When N = "0", it means 1-line display mode.
When N = "1", 2-line display mode is set.

**F : Display font type control bit**
When F = "0", $5 \times 7$ dots format display mode
When F = "1", $5 \times 10$ dots format display mode.

### 7) Set CGRAM Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

### 8) Set DDRAM Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

### 9) Read Busy Flag & Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether S6A0070 is in internal operation or not. If the resultant BF is "1", it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

### 10) Write Data to RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

### 11) Read Data from RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that is read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction; it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

**NOTE:** In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

**Table 5. Instruction Table**

| Instruction | Instruction Code | | | | | | | | | | Description Instruction Code | Execution Time (fsoc=270kHz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM. and set DDRAM address to "00H" from AC. | 1.53ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. | 1.53ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | SH | Assign cursor moving direction and enable the shift of entire display | 39µs |
| Display ON/OFF Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display(D), cursor(C), and blinking of cursor(B) on/off control bit. | 39µs |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 39µs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | X | X | Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type(F :0 ..) | 39µs |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. | 39µs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. | 39µs |
| Read Busy Flag and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0µs |
| Write Data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM/CGRAM). | 43µs |
| Read Data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM/CGRAM). | 43µs |

**NOTE:** When an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "0".

## INTERFACE WITH MPU

### 1) Interface with 8-bit MPU

When interfacing data length are 8-bit, transfer is performed all at once through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.

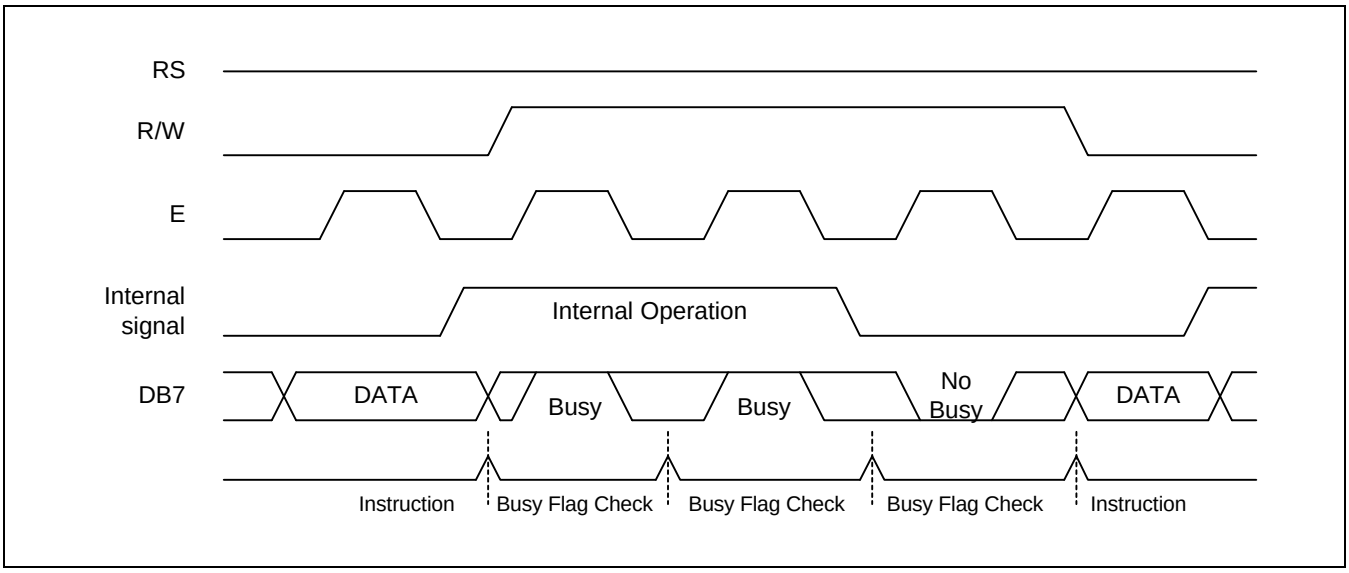



**Figure 4. Example of 8-bit Bus Mode Timing Diagram**

### 2) Interface with 4-bit MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two parts. Busy Flag outputs "1" after the second transfer are ended. Example of timing sequence is shown below.

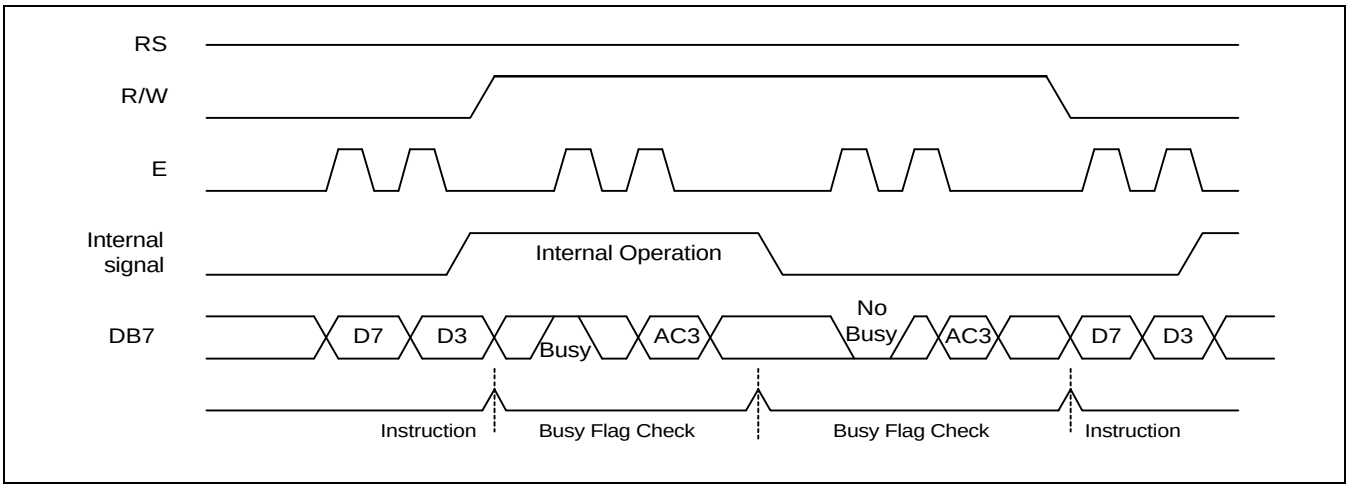
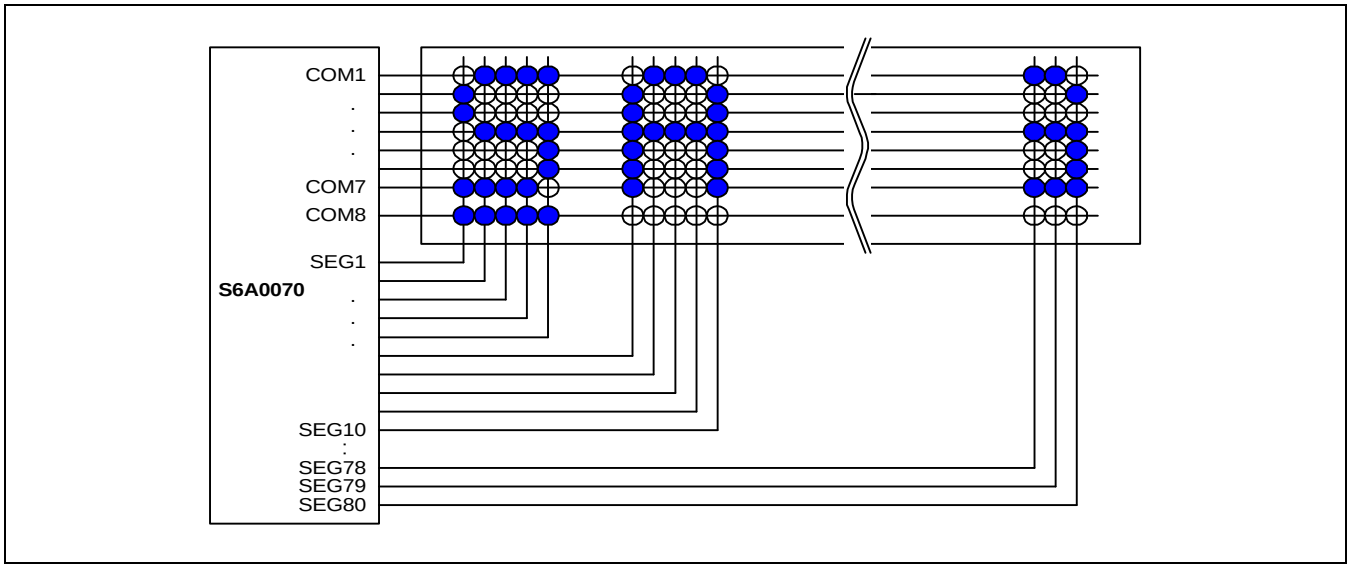


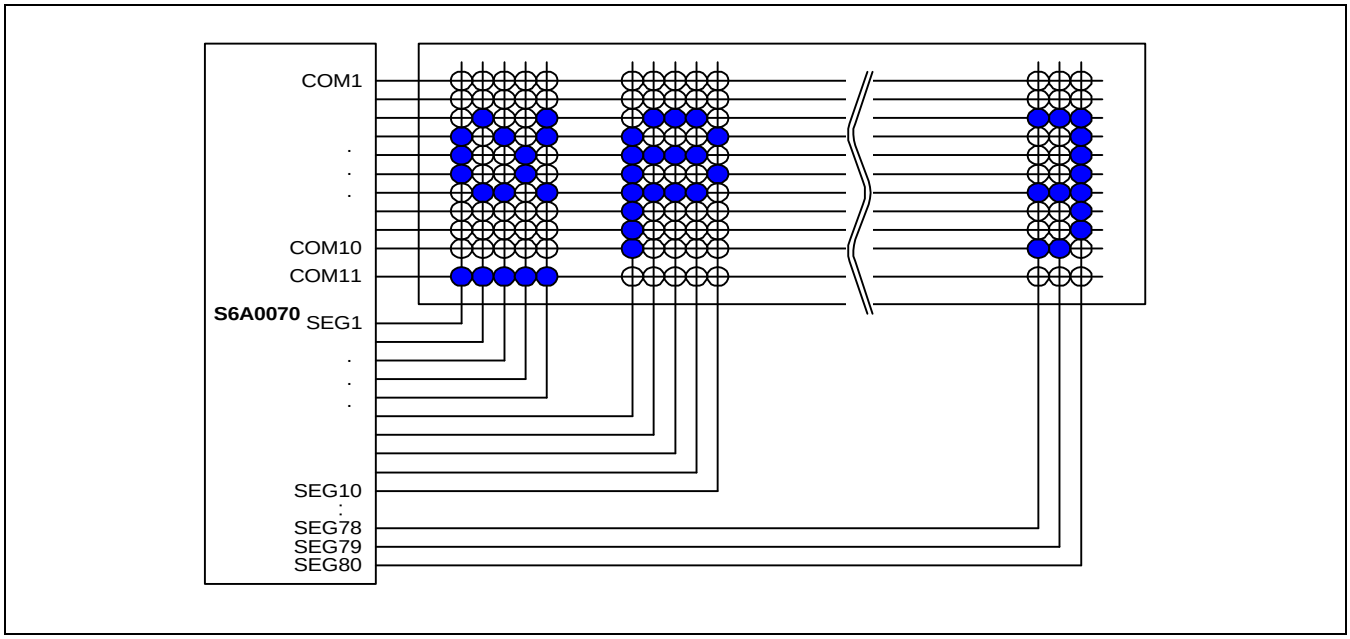

**Figure 5. Example of 4-bit Bus Mode Timing Diagram**

## APPLICATION INFORMATION ACCORDING TO LCD PANEL

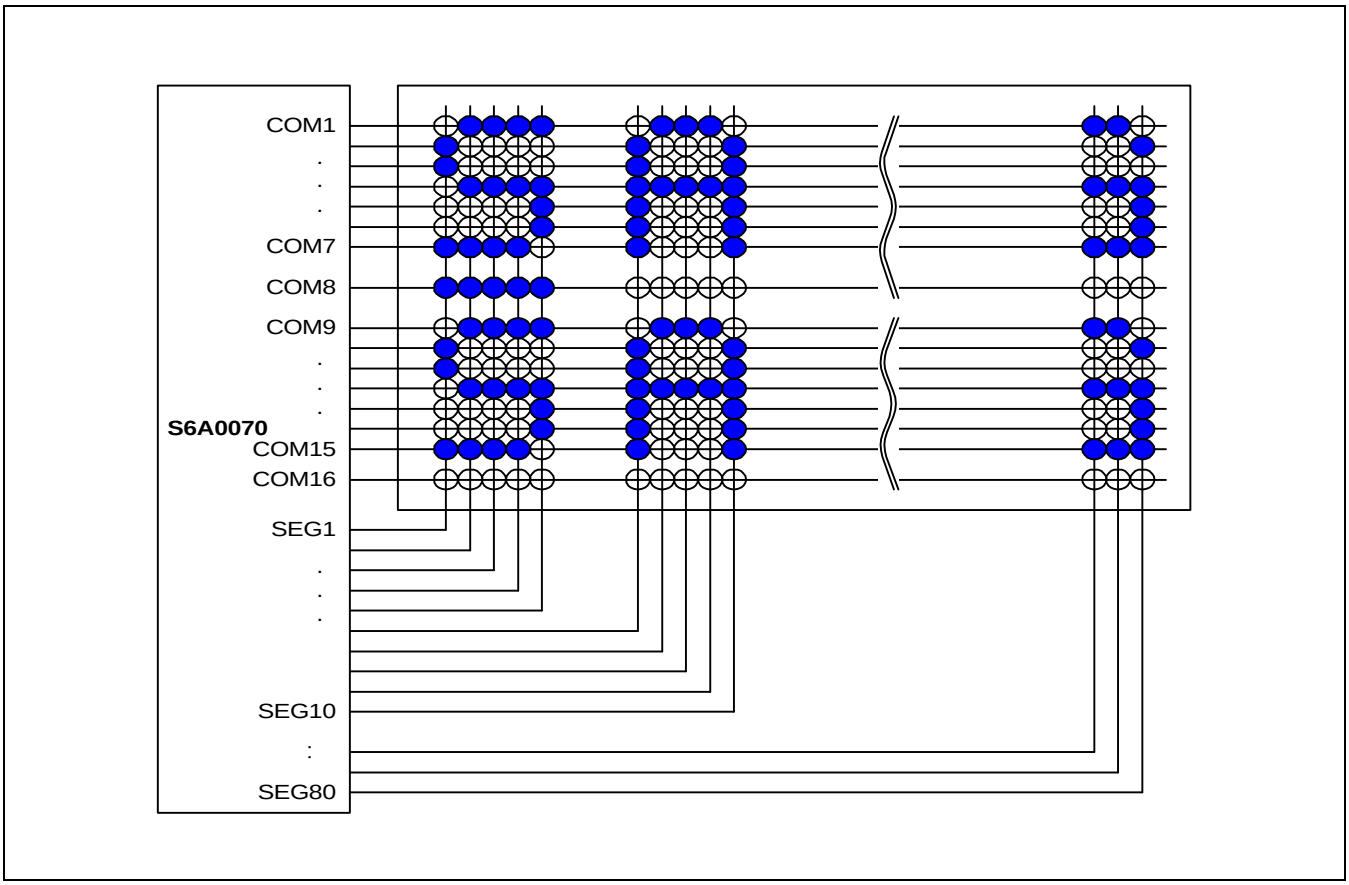
### 1) LCD Panel: 16 character ´ 1-line character format: 5 ´ 7 dots + 1 cursor line (1/4 bias, 1/8 duty)



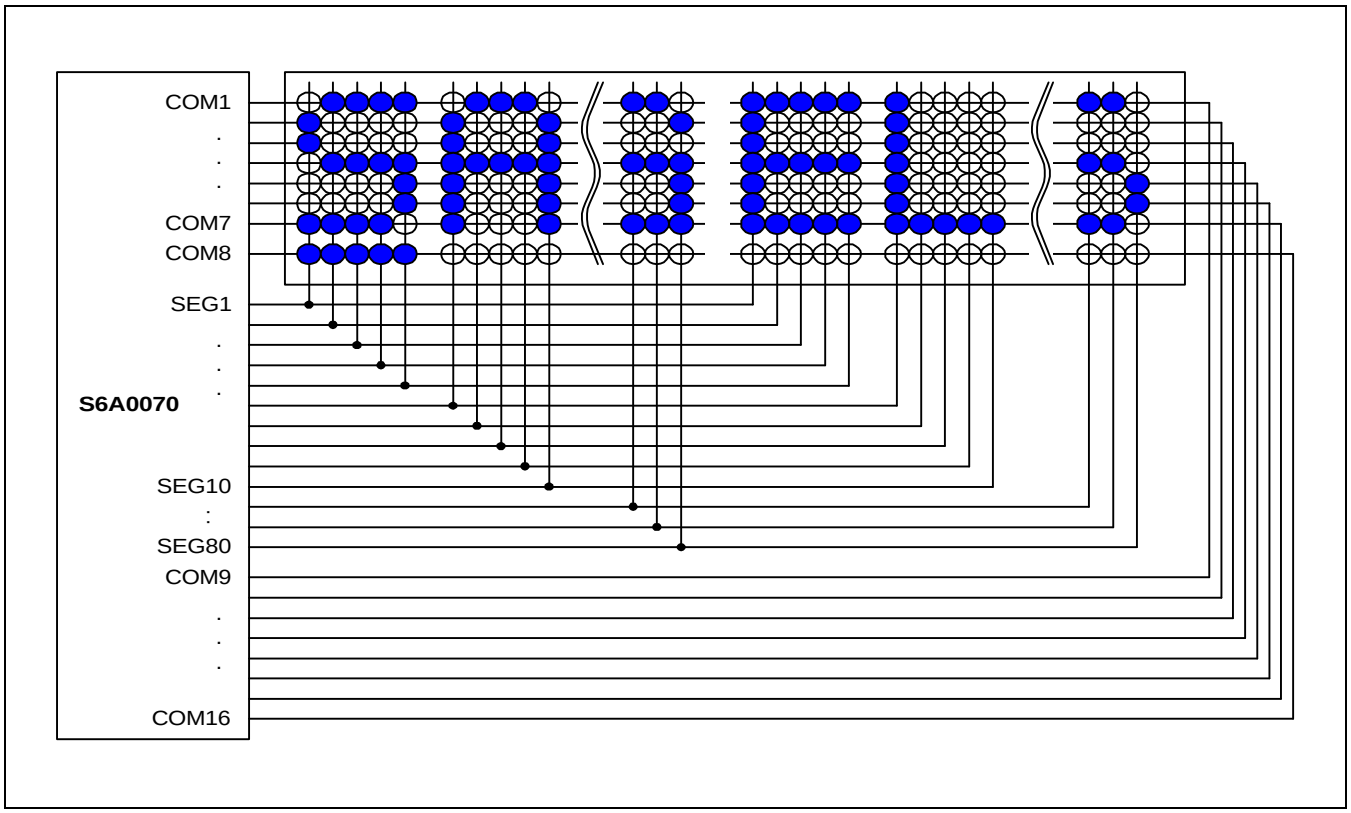

### 2) LCD Panel: 16 character ´ 1-line character format; 5 ´ 10 dots + 1 cursor line (1/4 bias, 1/11 duty)



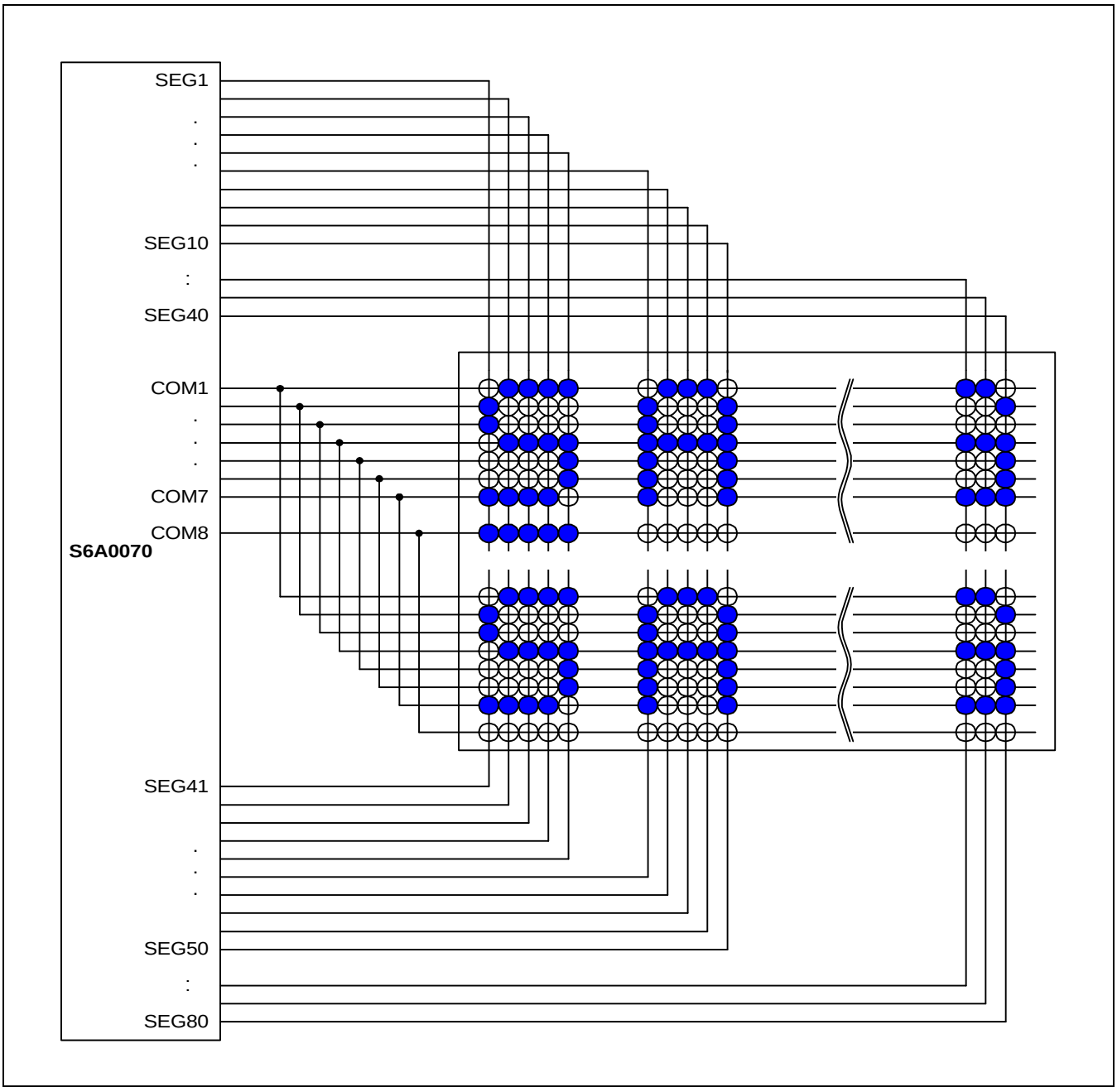
**3) LCD Panel: 16 character ´ 2-line character format; 5 ´ 7 dots + 1 cursor line (1/5 bias, 1/16 duty)**



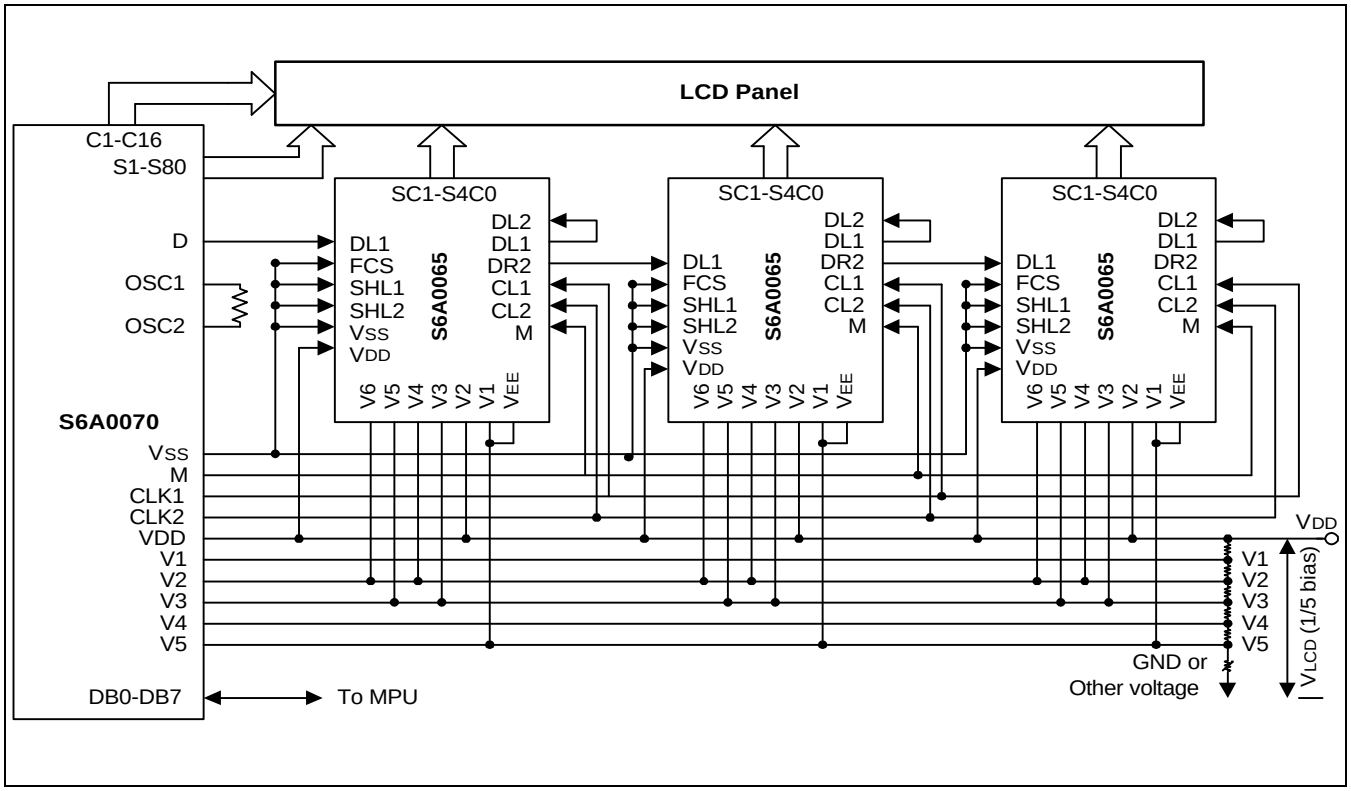
**4) LCD Panel: 32 character ´ 1-line Character format; 5 ´ 7 dots + 1 cursor line (1/5 bias, 1/16 duty)**



**5) LCD Panel: 4 character ´ 2-line character format: 5 ´ 7 dots + 1 cursor line (1/4 bias, 1/8 duty)**



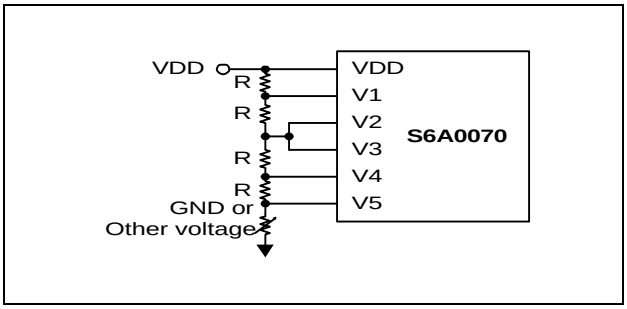
## APPLICATION CIRCUIT



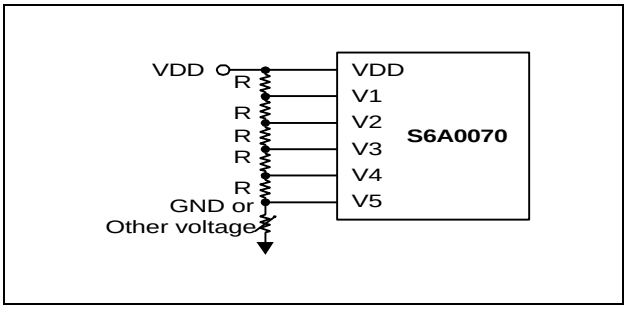

**NOTE:** When S6A0065 is externally connected to the S6A0070, you can increase the number of display digits up to 80 characteristics.

## BIAS VOLTAGE DIVIDE CIRCUIT

1) 1/4 bias, 1/8 or 1/11 duty




2) 1/5 bias, 1/16 duty




## INITIALIZING

When the power is turned on, S6A0070 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

(1) Display Clear instruction: Write "20H" to all DDRAM

(2) Set Functions instruction
- DL = 1 : 8-bit bus mode
- N = 0 : 1-line display mode
- F = 0 : 5 X 7 font type

(3) Control Display ON/OFF instruction
- D = 0 : Display OFF
- C = 0 : Cursor OFF
- B = 0 : Blink OFF

(4) Set Entry Mode instruction
- I/D = 1 : Increment by 1
- SH = 0 : No entire display shift

## FRAME FREQUENCY

1) 1/8 Duty Cycle

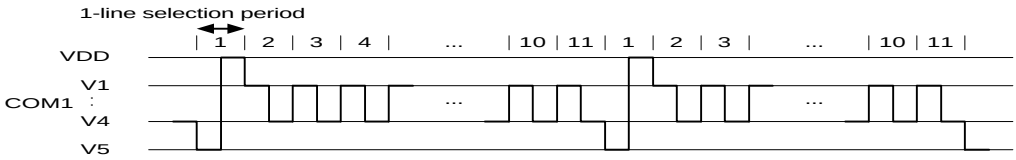
A) A-Type Waveform


| Item | Clock/Frequency |
|---|---|
| Line Selection Period | 400 clocks |
| Frame Frequency | 84.4Hz |

* $f_{OSC}$ = 270kHz (1 clock = 3.7µs)

2) 1/11 Duty Cycle

A) A-type Waveform

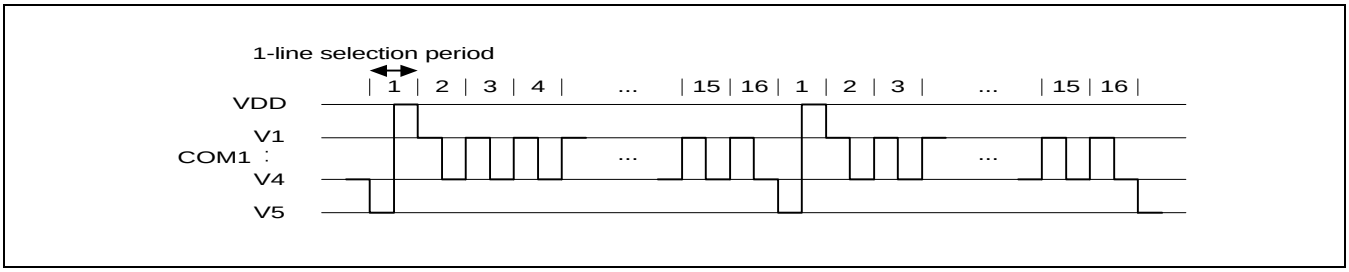



| Item | Clock/Frequency |
|---|---|
| Line Selection Period | 400 clocks |
| Frame Frequency | 61.4Hz |

* $f_{OSC}$ = 270kHz (1 clock = 3.7µs)

3) 1/16 Duty Cycle

A) A-type Waveform

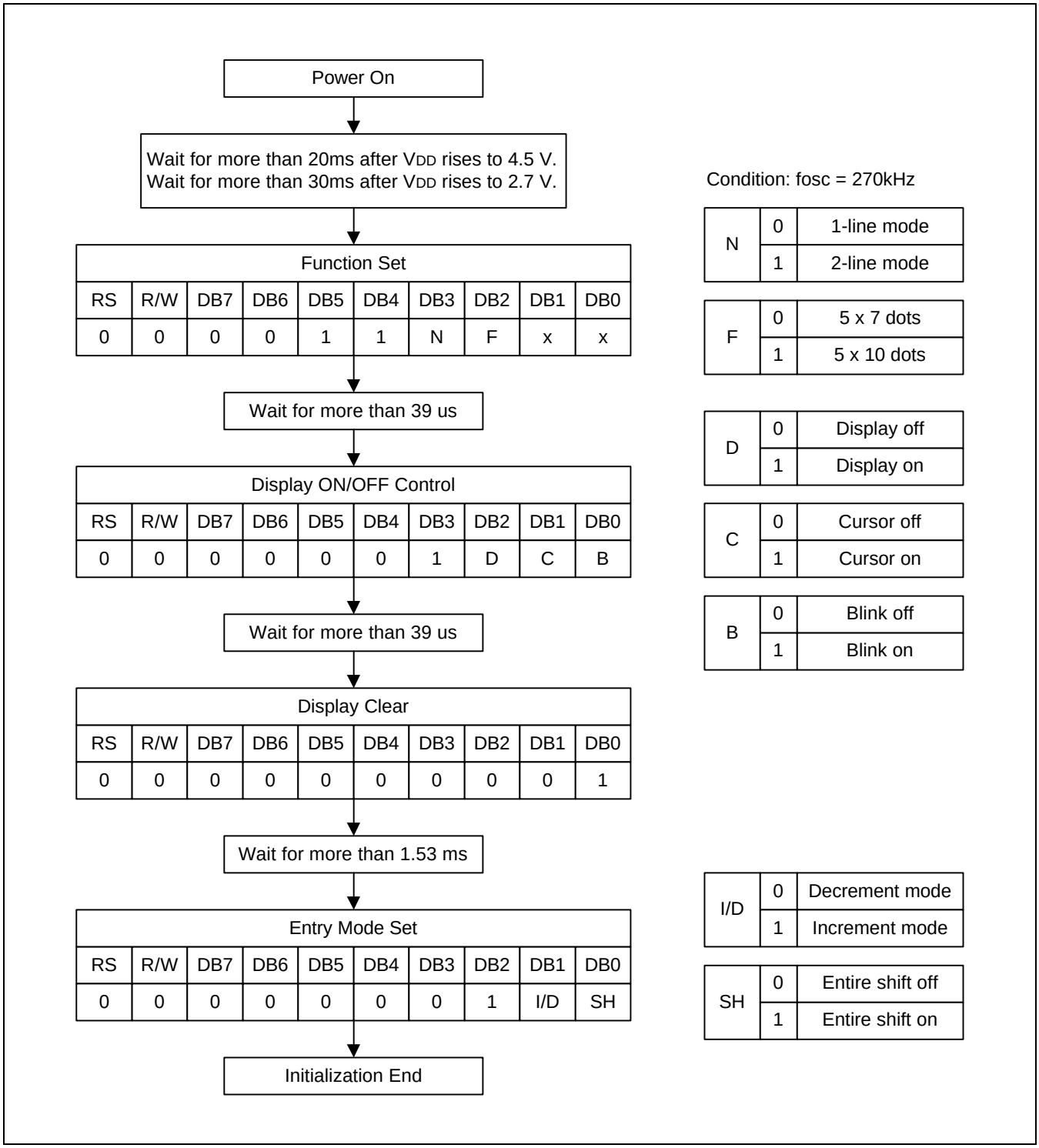



| Item | Clock/Frequency |
|---|---|
| Line Selection Period | 200 clocks |
| Frame Frequency | 84.4Hz |

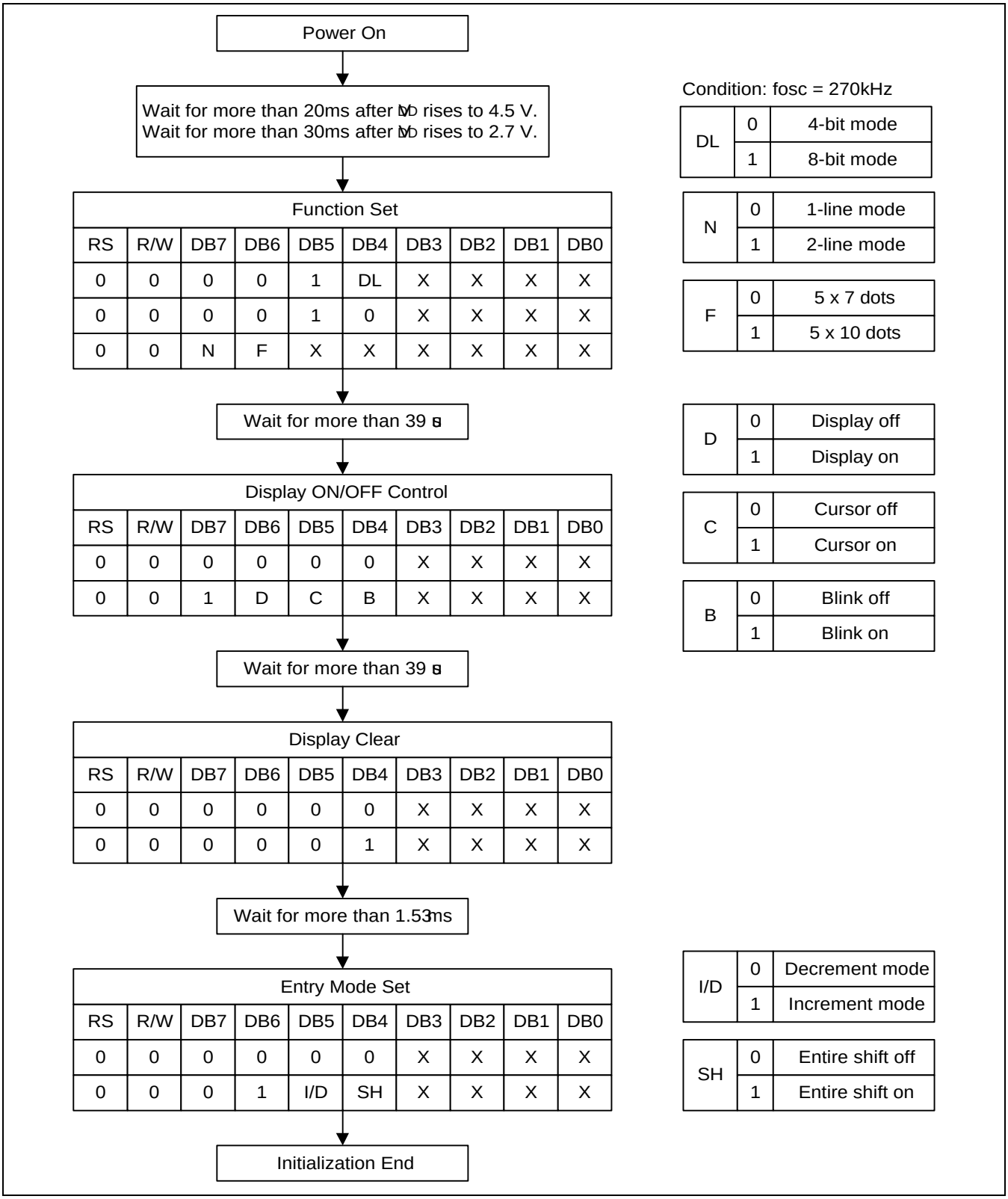
* $f_{OSC}$ = 270kHz (1 clock = 3.7μs)

## INITIALIZING BY INSTRUCTION

1) 8-bit Interface Mode



2) 4-bit Interface Mode



## EXAMPLE OF INSTRUCTION AND DISPLAY CORRESPONDENCE

1. Power supply on: Initialized by the internal power on reset circuit

LCD DISPLAY

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | |

2. Function Set: 8-bit, 2-line, 5 x 7 dot

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | X | X |

3. Display ON/OFF Control: Display/Cursor on/blink off

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

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4. Entry Mode Set: Increment

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

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5. Write Data to DDRAM: Write S

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

**S**_

6. Write Data to DDRAM: Write A

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

**SA**_

7. Write Data to DDRAM: Write M

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |

**SAM**_

8. Write Data to DDRAM: Write S

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

**SAMS**_

9. Write Data to DDRAM: Write U

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

LCD DISPLAY

**SAMSU_**

10. Write Data to DDRAM: Write N

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |

**SAMSUN_**

11. Write Data to DDRAM: Write G

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

**SAMSUNG_**

12. Set DDRAM Address: 40H

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

**SAMSUNG**
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13. Write Data to DDRAM: Write K

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

**SAMSUNG**
**K_**

14. Write Data to DDRAM: Write S

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |

**SAMSUNG**
**KS_**

15. Write Data to DDRAM: Write 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**SAMSUNG**
**KS0_**

16. Write Data to DDRAM: Write 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**SAMSUNG**
**KS00_**

17. Write Data to DDRAM: Write 7

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |

LCD DISPLAY

**SAMSUNG**
**KS007_**

18. Write Data to DDRAM: Write 2

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

**SAMSUNG**
**KS0072_**

19. Cursor or Display Shift: Cursor shift left

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | x | x |

**SAMSUNG**
**KS0072**

20. Write Data to DDRAM: Write 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

**SAMSUNG**
**KS0070_**

21. Entry Mode Set: Entire shift Enable

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**SAMSUNG**
**KS0070_**

22. Write Data to DDRAM: Write B

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

**SAMSUNG**
**KS0070B_**

23. Return Hone

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x |

**SAMSUNG**
**KS0070B**

24. Clear Display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

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## MAXIMUM ABSOLUTE LIMIT

| Item | Symbol | Unit | Value |
|---|---|---|---|
| Power Supply Voltage | $V_{DD}$ | V | -0.3 to +7.0 |
| LCD Drive Voltage | $V_{LCD}$ | V | $V_{DD}$-15 to $V_{DD}$+0.3 |
| Input Voltage | $V_{IN}$ | V | -0.3 to $V_{DD}$+0.3 |

**NOTE:** Voltage greater than above may damage the circuit ($V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$)

### Temperature Characteristics

| Item | Symbol | Unit | Value |
|---|---|---|---|
| Operating Temperature | $T_{OPR}$ | °C | - 30 to +85 |
| Storage Temperature | $T_{STG}$ | °C | - 55 to +125 |

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{DD}$ = 4.5V to 5.5V, Ta = - 30 to + 85°C)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 4.5 | - | 5.5 | V |
| Supply Current | $I_{DD1}$ | ceramic resonator $f_{OSC}$ = 250kHz | - | 0.7 | 1.0 | mA |
| | $I_{DD2}$ | Resister oscillation external clock operation $f_{OSC}$ = 270kHz | - | 0.4 | 0.6 | mA |
| Input Voltage (1) (except OSC1) | $V_{IH1}$ | - | 2.2 | - | $V_{DD}$ | V |
| | $V_{IL1}$ | - | -0.3 | - | 0.6 | V |
| Input Voltage (2) (except OSC1) | $V_{IH2}$ | - | $V_{DD}$-1.0 | - | $V_{DD}$ | V |
| | $V_{IL2}$ | - | -0.2 | - | 1.0 | V |
| Output Voltage (1) (DB0 to DB7) | $V_{OH1}$ | $I_{OH}$ = -0.205mA | 2.4 | - | - | V |
| | $V_{OL1}$ | $I_{OL}$ = 1.2mA | - | - | 0.4 | V |
| Output Voltage (2) (except DB0 to DB7) | $V_{OH2}$ | $I_O$ = -40µA | $0.9V_{DD}$ | - | - | V |
| | $V_{OL2}$ | $I_O$ = 40µA | - | - | $0.1V_{DD}$ | V |
| Voltage Drop | $Vd_{COM}$ | $I_O$ = ± 0.1mA | - | - | 1 | V |
| | $Vd_{SEG}$ | $I_O$ = ± 0.1mA | - | - | 1 | V |
| Input Leakage Current | $I_{IL}$ | $V_{IN}$ = 0V to $V_{DD}$ | -1 | - | 1 | µA |
| Low Input Current | $I_{IN}$ | $V_{IN}$ = 0V, $V_{DD}$ = 5V (pull-up) | -50 | -125 | -250 | µA |
| Internal Clock (external Rf) | $f_{IC}$ | Rf = 91kΩ ± 2% ($V_{DD}$ = 5V) | 190 | 270 | 350 | KHz |
| External Clock | $f_{EC}$ | - | 150 | 250 | 350 | KHz |
| | duty | | 45 | 50 | 55 | % |
| | $f_R$, $t_F$ | | - | - | 0.2 | µs |
| LCD Driving Voltage | $V_{LCD}$ | $V_{DD}$-5V (1/5, 1/4 bias) | 4.6 | - | 10.0 | V |

($V_{DD}$ = 2.7V to 4.5V, Ta = - 30 to + 85°C)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | 2.7 | - | 4.5 | V |
| Supply Current | $I_{DD1}$ | ceramic resonator $f_{OSC}$ = 250kHz | - | 0.3 | 0.5 | mA |
| | $I_{DD2}$ | Resister oscillation external clock operation $f_{OSC}$ = 270kHz | - | 0.17 | 0.3 | mA |
| Input Voltage (1) | $V_{IH1}$ | - | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| (except OSC1) | $V_{IL1}$ | - | -0.3 | - | 0.4 | V |
| Input Voltage (2) | $V_{IH2}$ | - | 0.7$V_{DD}$ | - | $V_{DD}$ | V |
| (except OSC1) | $V_{IL2}$ | - | - | - | 0.2$V_{DD}$ | V |
| Output Voltage (1) | $V_{OH1}$ | $I_{OH}$ = -0.1mA | 2.0 | - | - | V |
| (DB0 to DB7) | $V_{OL1}$ | $I_{OL}$ = 0.1mA | - | - | 0.4 | V |
| Output Voltage (2) | $V_{OH2}$ | $I_O$ = -40µA | 0.8$V_{DD}$ | - | - | V |
| (except DB0 to DB7) | $V_{OL2}$ | $I_O$ = 40µA | - | - | 0.2$V_{DD}$ | V |
| Voltage Drop | $Vd_{COM}$ | $I_O$ = ± 0.1mA | - | | 1 | V |
| | $Vd_{SEG}$ | $I_O$ = ± 0.1mA | - | - | 1.5 | V |
| Input Leakage Current | $I_{IL}$ | $V_{IN}$ = 0V to $V_{DD}$ | -1 | - | 1 | µA |
| Low Input Current | $I_{IN}$ | $V_{IN}$ = 0V, $V_{DD}$ = 5V (pull-up) | -10 | -50 | -120 | µA |
| Internal Clock (external Rf) | $f_{IC}$ | Rf = 75kΩ ± 2% ($V_{DD}$ = 3V) | 190 | 250 | 350 | KHz |
| External Clock | $f_{EC}$ | - | 125 | 270 | 350 | KHz |
| | duty | | 45 | 50 | 55 | % |
| | $f_R$, $t_F$ | | - | - | 0.2 | µs |
| *LCD Driving Voltage | $V_{LCD}$ | $V_{DD}$-$V_5$ (1/5, 1/4 bias) | 3.0 | - | 10.0 | V |

**NOTE:** LCD Driving Voltage

LCD Driving Voltage

| Power | DUTY | 1/8, 1/11 DUTY | 1/16 DUTY |
|---|---|---|---|
| | BIAS | 1/4 BIAS | 1/5 BIAS |
| $V_{DD}$ | | $V_{DD}$ | $V_{DD}$ |
| $V_1$ | | $V_{DD}$ - $V_{LCD}$/4 | $V_{DD}$ - $V_{LCD}$/5 |
| $V_2$ | | $V_{DD}$ - $V_{LCD}$/2 | $V_{DD}$ - 2$V_{LCD}$/5 |
| $V_3$ | | $V_{DD}$ - $V_{LCD}$/2 | $V_{DD}$ - 3$V_{LCD}$/5 |
| $V_4$ | | $V_{DD}$ - 3$V_{LCD}$/4 | $V_{DD}$ - 4$V_{LCD}$/5 |
| $V_5$ | | $V_{DD}$ - $V_{LCD}$ | $V_{DD}$ - $V_{LCD}$ |

## AC Characteristics

($V_{DD}$ = 4.5 to 5.5V, Ta = - 30 to + 85°C)

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Write Mode (Refer to Figure 6) | E Cycle Time | tc | 500 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 25 | ns |
| | E Pulse Width (High, Low) | tw | 220 | - | - | ns |
| | R/W and RS Setup Time | tsu1 | 40 | - | - | ns |
| | R/W and RS Hold Time | th1 | 10 | - | - | ns |
| | Data Setup Time | tsu2 | 60 | - | - | ns |
| | Data Hold Time | th2 | 10 | - | - | ns |
| Read mode (refer to figure 7) | E Cycle Time | tc | 500 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 25 | ns |
| | E Pulse Width (High, Low) | tw | 220 | - | - | ns |
| | R/W and RS Setup Time | tsu | 40 | - | - | ns |
| | R/W and RS Hold Time | th | 10 | - | - | ns |
| | Data Output Delay Time | $t_D$ | - | - | 120 | ns |
| | Data Hold Time | $t_{DH}$ | 20 | - | - | ns |

($V_{DD}$ = 2.7 to 4.5V, Ta = - 30 to + 85°C)

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Write Mode (Refer to Figure 6) | E Cycle Time | tc | 1400 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 25 | ns |
| | E Pulse Width (High, Low) | tw | 400 | - | - | ns |
| | R/W and RS Setup Time | tsu1 | 60 | - | - | ns |
| | R/W and RS Hold Time | th1 | 20 | - | - | ns |
| | Data Setup Time | tsu2 | 140 | - | - | ns |
| | Data Hold Time | th2 | 10 | - | - | ns |
| Read mode (refer to figure 7) | E Cycle Time | tc | 1400 | - | - | ns |
| | E Rise / Fall Time | tr, tf | - | - | 25 | ns |
| | E Pulse Width (High, Low) | tw | 400 | - | - | ns |
| | R/W and RS Setup Time | tsu | 60 | - | - | ns |
| | R/W and RS Hold Time | th | 20 | - | - | ns |
| | Data Output Delay Time | $t_D$ | - | - | 360 | ns |
| | Data Hold Time | $t_{DH}$ | 5 | - | - | ns |

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Interface Mode with Extension Driver (refer to figure 8) | Clock Pulse Width (High, Low) | tw | 800 | - | - | ns |
| | Clock Rise/Fall Time | tr, tf | - | - | 100 | ns |
| | Clock Setup Time | tsu1 | 500 | - | - | ns |
| | Data Setup Time | tsu2 | 300 | - | - | ns |
| | Data Hold Time | $t_{DH}$ | 300 | - | - | ns |
| | M Delay Time | $t_{DW}$ | -1000 | - | 1000 | ns |

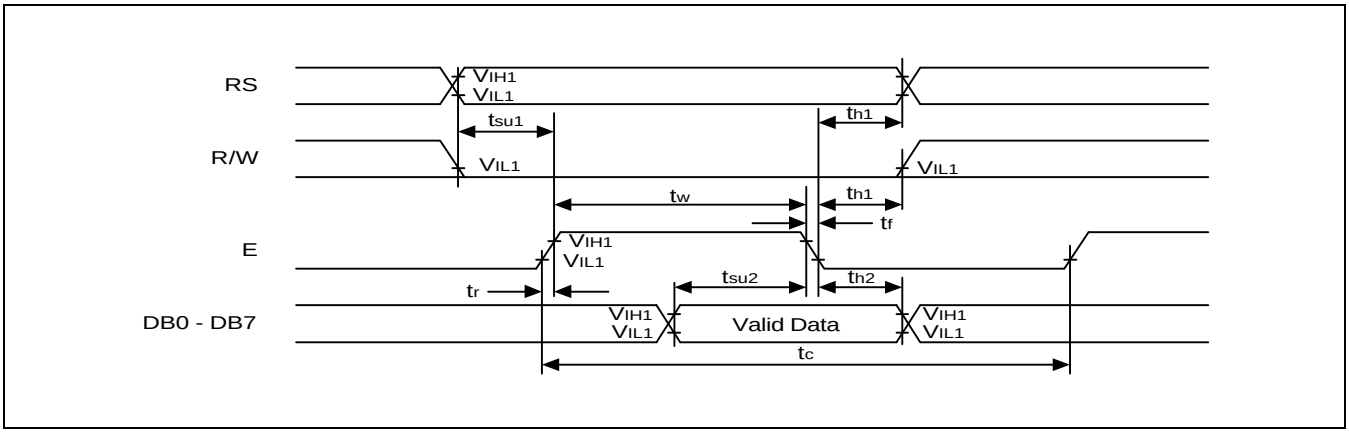


**Figure 6. Write Mode Timing Diagram**

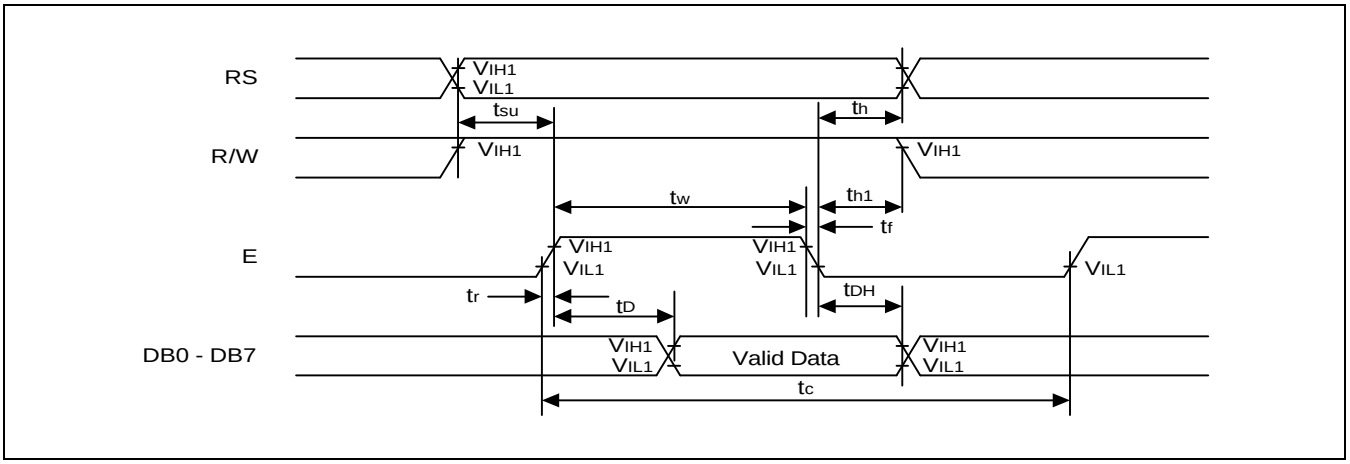


**Figure 7. Read Mode Timing Diagram**

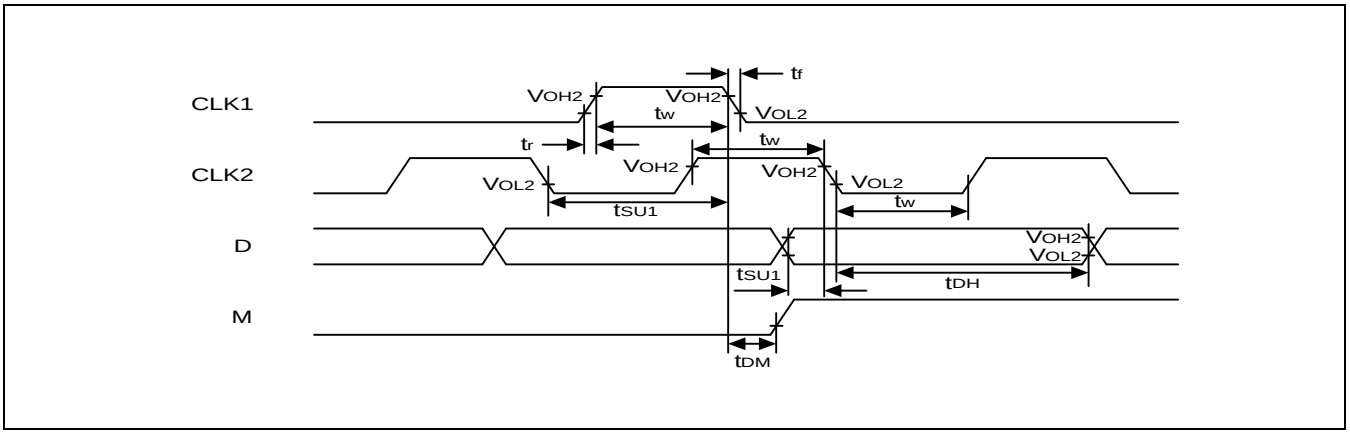


**Figure 8. Interface Mode with Extension Driver Timing Diagram**