S6B1713

65 COM / 132 SEG DRIVER & CONTROLLER FOR STN LCD

March .2002

Ver. 4.2

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

S6B1713 Specification Revision History		
Version	**Content**	**Date**
2.0	Neglect the more past version than version 2.0	Nov. 1998
2.1	f_{OSC} = 16kHz (Typ.) → 22kHz (Typ.): For removing flicker phenomenon Temperature coefficient (when TEMPS = L): -0.0%/°C → -0.05%/°C	Nov. 1998
3.0	Modified some syntax errors Voltage regulator reference voltage [V_{REF}]: TBD → 2.0 Modified voltage regulator block of "Functional Description"	Nov. 1998
3.1	V_{LCD} absolute maximum rating: 15.0V → 17.0V Power consumption: 100μA → 80μA	
3.2	Oscillator frequency (1): 19 (Min.) →17 (Min.), 25 (Max.) →27 (Max.) Oscillator frequency (2): 22 (Min.) →20 (Min.), 28 (Max.) →30 (Max.)	
3.3	Modified Y-axis values of "Pad Center Coordinates" Modified the contents of "Referential Instruction Setup Flow"	
3.4	Word-processor version change	Apr.1999
3.5	Modified error: pad No.113 (COMS) Y Coordinate: -1210 → -1140 (after)	Oct.1999
4.0	Change VDD Range : 2.4V to 5.5V → 2.4V to 3.6V	Jan.2000
4.1	Added detail information for several items	Mar.2001
4.2	Change VDD Range : 2.4V to 3.6V → 2.4V to 5.5V	Mar.2002

CONTENTS

INTRODUCTION **1**
FEATURES **1**
BLOCK DIAGRAM **3**
PAD CONFIGURATION **4**
PAD CENTER COORDINATES **5**
PIN DESCRIPTION **8**
POWER SUPPLY 8
LCD DRIVER SUPPLY 8
SYSTEM CONTROL 9
MICROPROCESSOR INTERFACE 11
LCD DRIVER OUTPUTS 13
FUNCTIONAL DESCRIPTION **14**
MICROPROCESSOR INTERFACE 14
DISPLAY DATA RAM (DDRAM) 18
LCD DISPLAY CIRCUITS 21
LCD DRIVER CIRCUIT 23
POWER SUPPLY CIRCUITS 24
REFERECE CIRCUIT EXAMPLES 31
RESET CIRCUIT 33
INSTRUCTION DESCRIPTION **34**
SPECIFICATIONS **48**
ABSOLUTE MAXIMUM RATINGS 48
DC CHARACTERISTICS 49
REFERENCE DATA 52
AC CHARACTERISTICS 54
REFERENCE APPLICATIONS **60**
MICROPROCESSOR INTERFACE 60
CONNECTIONS BETWEEN S6B1713 AND LCD PANEL 61
TCP PIN LAYOUT (SAMPLE) 66

INTRODUCTION

The S6B1713 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 65 commons and 132 segments driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip Display Data RAM of 65 x 132 bits. It provides a high-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

– 65 common outputs / 132 segment outputs

On-chip Display Data RAM

– Capacity: 65 x 132 = 8,580 bits

Applicable Duty Ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/65	1/7 or 1/9	65 × 132
1/49	1/6 or 1/8	49 × 132
1/33	1/5 or 1/6	33 × 132

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

Function Set

– Various instructions sets
– H/W, S/W reset capable

Built-in Analog Circuit

– On-chip oscillator circuit
– Voltage converter (x2, x3, x4, x5)
– Voltage regulator (temperature coefficient: -0.05%/°C, -0.2%/°C)
– Voltage follower
– Electronic contrast control function (64 steps)

Operating Voltage Range

– Supply voltage2 (V_{DD}): 2.4 to 5.5 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low Power Consumption

– 70 µA Typ. (V_{DD} = 3V, x4 boosting, V0 = 11V, internal power supply ON)
– 10 µA Max. (during power save [standby] mode)

Package Type

– Gold bumped chip or TCP

Series Specifications

Product code	TEMPS pin	Temperature coefficient	Package type	Chip thickness
S6B1713A05-B0CZ	0 (V_{SS} connected)	-0.05%/°C	COG	670 µm
S6B1713A05-B0CY				470 µm
S6B1713A15-B0CZ	1 (V_{DD} connected)	-0.2%/°C		670 µm
S6B1713A15-B0CY				470 µm
S6B1713A05-xxX0	0 (V_{SS} connected)	-0.05%/°C	TCP	670 µm
S6B1713A05-xxXN				470 µm
S6B1713A15-xxX0	1 (V_{DD} connected)	-0.2%/°C		670 µm
S6B1713A15-xxXN				470 µm

* xx: TCP ordering number

BLOCK DIAGRAM

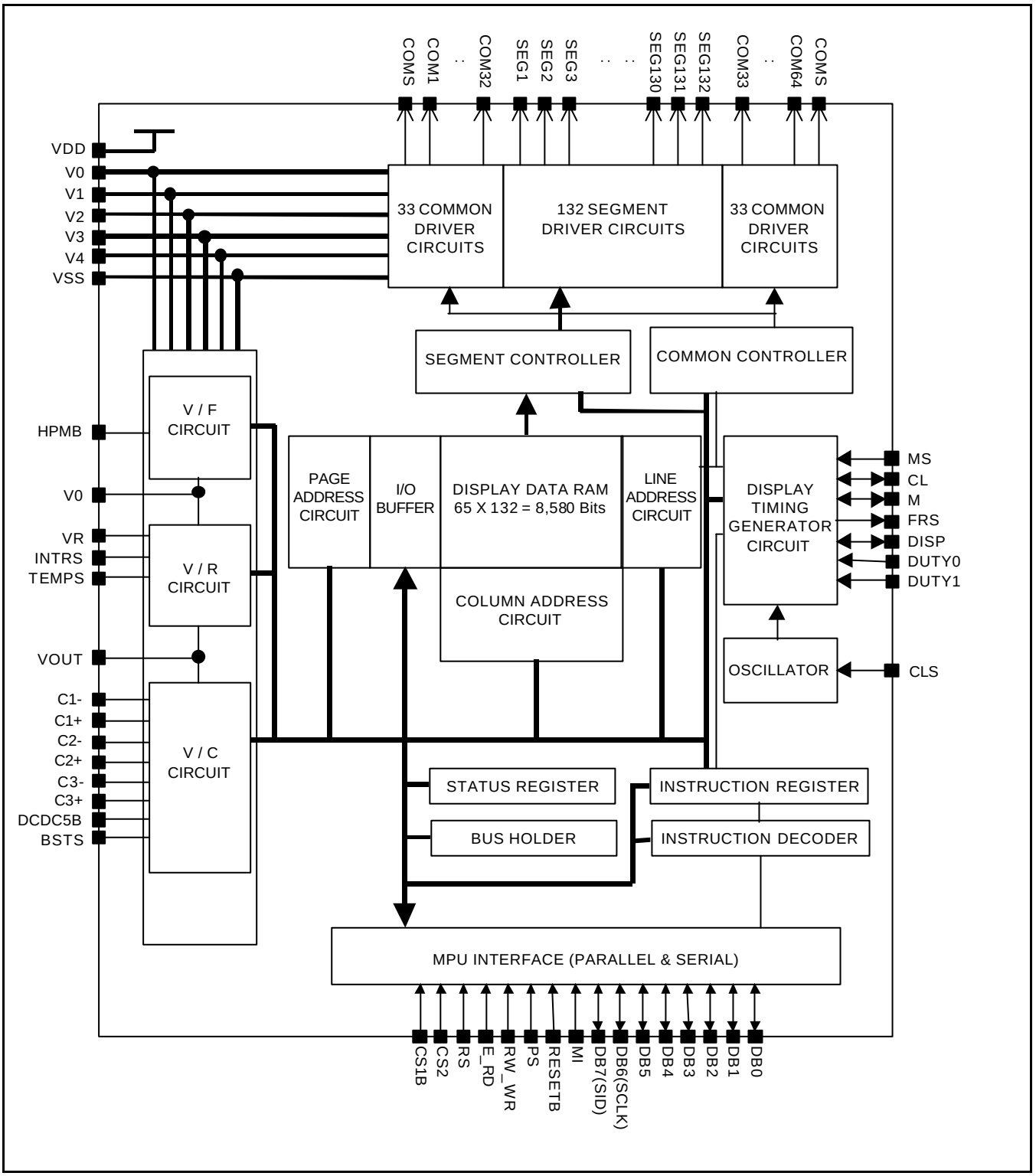


Figure 1. Block Diagram

PAD CONFIGURATION

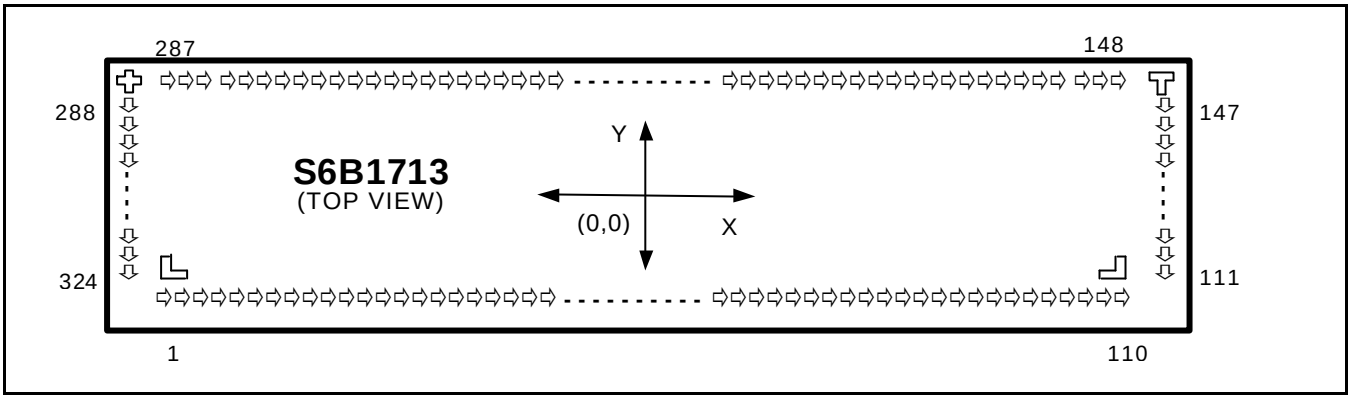


Figure 2. S6B1713 Chip Configuration

Table 1. S6B1713 Pad Dimensions

Items	Pad No.	Size		Unit
		X	Y	
Chip size	-	10860	2920	μm
Pad pitch	1 to 110	90		
	111 to 324	70		
Bumped pad size	1 to 110	56	114	
	111 to 147	108	50	
	148 to 287	50	108	
	288 to 324	108	50	
Bumped pad height	1 to 324	17 (Typ.)		

Figure 3. COG Align Key Coordinate

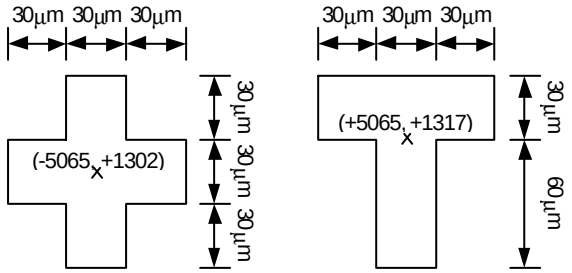
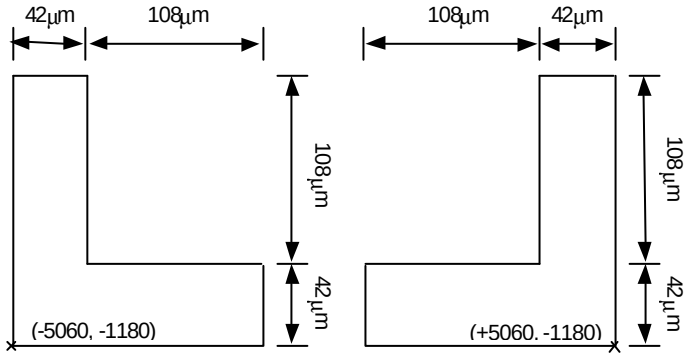


Figure 4. ILB Align Key Coordinate(with Gold Bump *)



* When designing electrode pattern must be prohibited on this area (ILB Align Key). If electrode pattern is used for routing over this area, it can be happened pattern-short through gold bump pattern on ILB Align Key.

PAD Center Coordinates

Table 2. Pad Center Coordinates

[Unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-4905	-1336	51	VDD	-405	-1336	101	BSTS	4095	-1336
2	DUMMY	-4815	-1336	52	VDD	-315	-1336	102	DCDC5B	4185	-1336
3	FRS	-4725	-1336	53	VDD	-225	-1336	103	VDD	4275	-1336
4	M	-4635	-1336	54	VDD	-135	-1336	104	HPM	4365	-1336
5	CL	-4545	-1336	55	VDD	-45	-1336	105	INTRS	4455	-1336
6	DISP	-4455	-1336	56	VDD	45	-1336	106	VSS	4545	-1336
7	VSS	-4365	-1336	57	VOUT	135	-1336	107	TEMPS	4635	-1336
8	CS1B	-4275	-1336	58	VOUT	225	-1336	108	VDD	4725	-1336
9	CS2	-4185	-1336	59	VOUT	315	-1336	109	DUMMY	4815	-1336
10	VDD	-4095	-1336	60	VOUT	405	-1336	110	DUMMY	4905	-1336
11	RESETB	-4005	-1336	61	C3+	495	-1336	111	DUMMY	5271	-1280
12	RS	-3915	-1336	62	C3+	585	-1336	112	DUMMY	5271	-1210
13	VSS	-3825	-1336	63	C3+	675	-1336	113	COMS	5271	-1140
14	RW_WR	-3735	-1336	64	C3+	765	-1336	114	COM1	5271	-1070
15	E_RD	-3645	-1336	65	C3-	855	-1336	115	COM2	5271	-1000
16	VDD	-3555	-1336	66	C3-	945	-1336	116	COM3	5271	-930
17	DB0	-3465	-1336	67	C3-	1035	-1336	117	COM4	5271	-860
18	DB1	-3375	-1336	68	C3-	1125	-1336	118	COM5	5271	-790
19	DB2	-3285	-1336	69	C1+	1215	-1336	119	COM6	5271	-720
20	DB3	-3195	-1336	70	C1+	1305	-1336	120	COM7	5271	-650
21	DB4	-3105	-1336	71	C1+	1395	-1336	121	COM8	5271	-580
22	DB5	-3015	-1336	72	C1+	1485	-1336	122	COM9	5271	-510
23	DB6	-2925	-1336	73	C1-	1575	-1336	123	COM10	5271	-440
24	DB7	-2835	-1336	74	C1-	1665	-1336	124	COM11	5271	-370
25	VSS	-2745	-1336	75	C1-	1755	-1336	125	COM12	5271	-300
26	VDD	-2655	-1336	76	C1-	1845	-1336	126	COM13	5271	-230
27	VDD	-2565	-1336	77	C2+	1935	-1336	127	COM14	5271	-160
28	VDD	-2475	-1336	78	C2+	2025	-1336	128	COM15	5271	-90
29	DUTY0	-2385	-1336	79	C2+	2115	-1336	129	COM16	5271	-20
30	DUTY1	-2295	-1336	80	C2+	2205	-1336	130	COM17	5271	50
31	VSS	-2205	-1336	81	C2-	2295	-1336	131	COM18	5271	120
32	MS	-2115	-1336	82	C2-	2385	-1336	132	COM19	5271	190
33	CLS	-2025	-1336	83	C2-	2475	-1336	133	COM20	5271	260
34	VDD	-1935	-1336	84	C2-	2565	-1336	134	COM21	5271	330
35	MI	-1845	-1336	85	VSS	2655	-1336	135	COM22	5271	400
36	PS	-1755	-1336	86	VSS	2745	-1336	136	COM23	5271	470
37	VSS	-1665	-1336	87	VR	2835	-1336	137	COM24	5271	540
38	VSS	-1575	-1336	88	VR	2925	-1336	138	COM25	5271	610
39	VSS	-1485	-1336	89	V0	3015	-1336	139	COM26	5271	680
40	VSS	-1395	-1336	90	V0	3105	-1336	140	COM27	5271	750
41	VSS	-1305	-1336	91	V1	3195	-1336	141	COM28	5271	820
42	VSS	-1215	-1336	92	V1	3285	-1336	142	COM29	5271	890
43	VSS	-1125	-1336	93	V2	3375	-1336	143	COM30	5271	960
44	VSS	-1035	-1336	94	V2	3465	-1336	144	COM31	5271	1030
45	VSS	-945	-1336	95	V3	3555	-1336	145	COM32	5271	1100
46	VSS	-855	-1336	96	V3	3645	-1336	146	DUMMY	5271	1170
47	VDD	-765	-1336	97	V4	3735	-1336	147	DUMMY	5271	1240
48	VDD	-675	-1336	98	V4	3825	-1336	148	DUMMY	4865	1301
49	VDD	-585	-1336	99	VSS	3915	-1336	149	DUMMY	4795	1301
50	VDD	-495	-1336	100	VSS	4005	-1336	150	DUMMY	4725	1301

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
151	DUMMY	4655	1301	201	SEG50	1155	1301	251	SEG100	-2345	1301
152	SEG1	4585	1301	202	SEG51	1085	1301	252	SEG101	-2415	1301
153	SEG2	4515	1301	203	SEG52	1015	1301	253	SEG102	-2485	1301
154	SEG3	4445	1301	204	SEG53	945	1301	254	SEG103	-2555	1301
155	SEG4	4375	1301	205	SEG54	875	1301	255	SEG104	-2625	1301
156	SEG5	4305	1301	206	SEG55	805	1301	256	SEG105	-2695	1301
157	SEG6	4235	1301	207	SEG56	735	1301	257	SEG106	-2765	1301
158	SEG7	4165	1301	208	SEG57	665	1301	258	SEG107	-2835	1301
159	SEG8	4095	1301	209	SEG58	595	1301	259	SEG108	-2905	1301
160	SEG9	4025	1301	210	SEG59	525	1301	260	SEG109	-2975	1301
161	SEG10	3955	1301	211	SEG60	455	1301	261	SEG110	-3045	1301
162	SEG11	3885	1301	212	SEG61	385	1301	262	SEG111	-3115	1301
163	SEG12	3815	1301	213	SEG62	315	1301	263	SEG112	-3185	1301
164	SEG13	3745	1301	214	SEG63	245	1301	264	SEG113	-3255	1301
165	SEG14	3675	1301	215	SEG64	175	1301	265	SEG114	-3325	1301
166	SEG15	3605	1301	216	SEG65	105	1301	266	SEG115	-3395	1301
167	SEG16	3535	1301	217	SEG66	35	1301	267	SEG116	-3465	1301
168	SEG17	3465	1301	218	SEG67	-35	1301	268	SEG117	-3535	1301
169	SEG18	3395	1301	219	SEG68	-105	1301	269	SEG118	-3605	1301
170	SEG19	3325	1301	220	SEG69	-175	1301	270	SEG119	-3675	1301
171	SEG20	3255	1301	221	SEG70	-245	1301	271	SEG120	-3745	1301
172	SEG21	3185	1301	222	SEG71	-315	1301	272	SEG121	-3815	1301
173	SEG22	3115	1301	223	SEG72	-385	1301	273	SEG122	-3885	1301
174	SEG23	3045	1301	224	SEG73	-455	1301	274	SEG123	-3955	1301
175	SEG24	2975	1301	225	SEG74	-525	1301	275	SEG124	-4025	1301
176	SEG25	2905	1301	226	SEG75	-595	1301	276	SEG125	-4095	1301
177	SEG26	2835	1301	227	SEG76	-665	1301	277	SEG126	-4165	1301
178	SEG27	2765	1301	228	SEG77	-735	1301	278	SEG127	-4235	1301
179	SEG28	2695	1301	229	SEG78	-805	1301	279	SEG128	-4305	1301
180	SEG29	2625	1301	230	SEG79	-875	1301	280	SEG129	-4375	1301
181	SEG30	2555	1301	231	SEG80	-945	1301	281	SEG130	-4445	1301
182	SEG31	2485	1301	232	SEG81	-1015	1301	282	SEG131	-4515	1301
183	SEG32	2415	1301	233	SEG82	-1085	1301	283	SEG132	-4585	1301
184	SEG33	2345	1301	234	SEG83	-1155	1301	284	DUMMY	-4655	1301
185	SEG34	2275	1301	235	SEG84	-1225	1301	285	DUMMY	-4725	1301
186	SEG35	2205	1301	236	SEG85	-1295	1301	286	DUMMY	-4795	1301
187	SEG36	2135	1301	237	SEG86	-1365	1301	287	DUMMY	-4865	1301
188	SEG37	2065	1301	238	SEG87	-1435	1301	288	DUMMY	-5271	1240
189	SEG38	1995	1301	239	SEG88	-1505	1301	289	DUMMY	-5271	1170
190	SEG39	1925	1301	240	SEG89	-1575	1301	290	COMS	-5271	1100
191	SEG40	1855	1301	241	SEG90	-1645	1301	291	COM64	-5271	1030
192	SEG41	1785	1301	242	SEG91	-1715	1301	292	COM63	-5271	960
193	SEG42	1715	1301	243	SEG92	-1785	1301	293	COM62	-5271	890
194	SEG43	1645	1301	244	SEG93	-1855	1301	294	COM61	-5271	820
195	SEG44	1575	1301	245	SEG94	-1925	1301	295	COM60	-5271	750
196	SEG45	1505	1301	246	SEG95	-1995	1301	296	COM59	-5271	680
197	SEG46	1435	1301	247	SEG96	-2065	1301	297	COM58	-5271	610
198	SEG47	1365	1301	248	SEG97	-2135	1301	298	COM57	-5271	540
199	SEG48	1295	1301	249	SEG98	-2205	1301	299	COM56	-5271	470
200	SEG49	1225	1301	250	SEG99	-2275	1301	300	COM55	-5271	400

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
301	COM54	-5271	330								
302	COM53	-5271	260								
303	COM52	-5271	190								
304	COM51	-5271	120								
305	COM50	-5271	50								
306	COM49	-5271	-20								
307	COM48	-5271	-90								
308	COM47	-5271	-160								
309	COM46	-5271	-230								
310	COM45	-5271	-300								
311	COM44	-5271	-370								
312	COM43	-5271	-440								
313	COM42	-5271	-510								
314	COM41	-5271	-580								
315	COM40	-5271	-650								
316	COM39	-5271	-720								
317	COM38	-5271	-790								
318	COM37	-5271	-860								
319	COM36	-5271	-930								
320	COM35	-5271	-1000								
321	COM34	-5271	-1070								
322	COM33	-5271	-1140								
323	DUMMY	-5271	-1210								
324	DUMMY	-5271	-1280								

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td>Power supply</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>LCD driver supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship;
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD Bias.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/9 bias</td><td>(8/9) x V0</td><td>(7/9) x V0</td><td>(2/9) x V0</td><td>(1/9) x V0</td></tr>
<tr><td>1/8 bias</td><td>(7/8) x V0</td><td>(6/8) x V0</td><td>(2/8) x V0</td><td>(1/8) x V0</td></tr>
<tr><td>1/7 bias</td><td>(6/7) x V0</td><td>(5/7) x V0</td><td>(2/7) x V0</td><td>(1/7) x V0</td></tr>
<tr><td>1/6 bias</td><td>(5/6) x V0</td><td>(4/6) x V0</td><td>(2/6) x V0</td><td>(1/6) x V0</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table>
</td></tr>
</table>

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pin Description

Name	I/O	Description
C1-	O	Capacitor 1 negative connection pin for voltage converter
C1+	O	Capacitor 1 positive connection pin for voltage converter
C2-	O	Capacitor 2 negative connection pin for voltage converter
C2+	O	Capacitor 2 positive connection pin for voltage converter
C3-	O	Capacitor 3 negative connection pin for voltage converter
C3+	O	Capacitor 3 positive connection pin for voltage converter
VOUT	I/O	Voltage converter input / output pin
DCDC5B	I	5 times boosting circuit enable input pin When this pin is low in 4 times boosting circuit, the 5-times boosting voltage appears at VOUT.
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used (INTRS = “L”).

SYSTEM CONTROL

Table 5. System Control Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="6">MS</td><td rowspan="6">I</td><td>Master / Slave operation select pin
– MS = "H": master operation
– MS = "L": slave operation
The following table depends on the MS status.</td></tr>
<tr><td>
<table>
<tr><th>MS</th><th>CLS</th><th>OSC circuit</th><th>Power supply circuit</th><th>CL</th><th>M</th><th>FRS</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Enabled</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>H or L</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table>
</td></tr>
<tr><td>When slave mode, the CLS pin must be fixed ‘ H’ or ‘ L’</td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enable / disable select pin
– CLS = “ H” : enable
– CLS = “ L” : disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the S6B1713 is used in master/slave mode (multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input / output pin
When the S6B1713 is used in master/slave mode (multi-chip), the M pins must be connected each other.
– MS = “ H” : output
– MS = “ L” : input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the M pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input / output
When S6B1713 is used in master/slave mode (multi-chip), the DISP pins must be connected each other.
– MS = “ H” : output
– MS = “ L” : input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistors select pin
This pin selects the resistors for adjusting V0 voltage level.
– INTRS = "H": use the internal resistors.
– INTRS = "L": use the external resistors.
V0 voltage is controlled with VR pin and external resistive divider.</td></tr>
<tr><td>HPM</td><td>I</td><td>Power control pin of the power supply circuit for LCD driver
– HPM = "H": high power mode
– HPM = "L": normal mode
This pin is valid in master operation.</td></tr>
<tr><td>TEMPS</td><td>I</td><td>Selects temperature coefficient of the reference voltage
– TEMPS = "L": -0.05%/°C
– TEMPS = "H": -0.2%/°C</td></tr>
</table>

Table 5. System Control Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="3">Description</th></tr>
<tr><td rowspan="5">BSTS</td><td rowspan="5">I</td><td colspan="3">Selects input voltages of the built-in voltage converter</td></tr>
<tr><td>BSTS</td><td>Voltage converter input voltage</td><td>Remarks</td></tr>
<tr><td>L</td><td>4V</td><td>V_{DD} > 4V</td></tr>
<tr><td>H</td><td>V_{DD}</td><td>2.4V ≤ V_{DD} ≤ 5.5V</td></tr>
<tr><td colspan="3">NOTE: Because the maximum voltage of V_{DD} has been changed to 5.5V, we strongly recommend that BSTS pin should be fixed to “H”.</td></tr>
<tr><td rowspan="6">DUTY0
DUTY1</td><td rowspan="6">I</td><td colspan="3">The LCD driver duty ratio depends on the following table</td></tr>
<tr><td>DUTY1</td><td>DUTY0</td><td>Duty ratio</td></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L/H</td><td>1/65</td></tr>
<tr><td colspan="3"></td></tr>
</table>

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS</td><td>Interface mode</td><td>Chip select</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>CS1B, CS2</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>CS1B, CS2</td><td>RS</td><td>SID(DB7)</td><td>Write only</td><td>SCLK(DB6)</td></tr>
</table>
</td></tr>
<tr><td>*NOTE: In serial mode, it is impossible to read data from the on-chip RAM. And DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>MI</td><td>I</td><td>Microprocessor interface selects input pin
– MI = "H": 6800-series MPU interface
– MI = "L": 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”.
When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="4">RW_WR</td><td rowspan="4">I</td><td>Read / Write execution control pin
<table>
<tr><td>MI</td><td>MPU type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
– RW = “H”: read
– RW = “L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data ON DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table>
</td></tr>
<tr><td></td></tr>
</table>

Table 6. Microprocessor Interface Pin Description (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>MI</td><td>MPU type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

LCD DRIVER OUTPUTS

Table 7. LCD Driver Outputs Pin Description

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG1
to
SEG132</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM1
to
COM64</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">VSS</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>COMS</td><td>O</td><td colspan="4">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.
In multi-chip (master / slave) mode, all COMS pins on both master and slave units are the same signal.</td></tr>
</table>

NOTE: **DUMMY - These pins should be opened (floated).**

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for Chip Selection. The S6B1713 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

S6B1713 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8.

Table 8. Parallel / Serial Interface Mode

PS	Type	CS1B	CS2	MI	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*	Serial-mode

* : Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by MI as shown in table 9. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in table10.

Table 9. Microprocessor Selection for Parallel Interface

MI	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

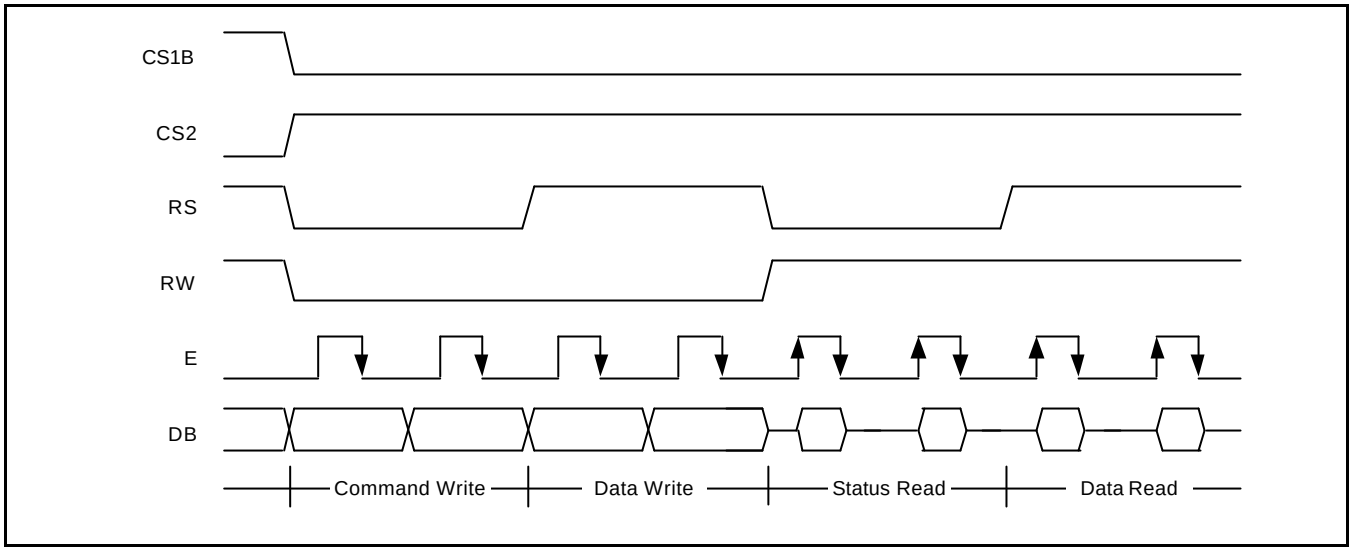


Figure 5. 6800-Series MPU Interface protocol (PS="H", MI="H")

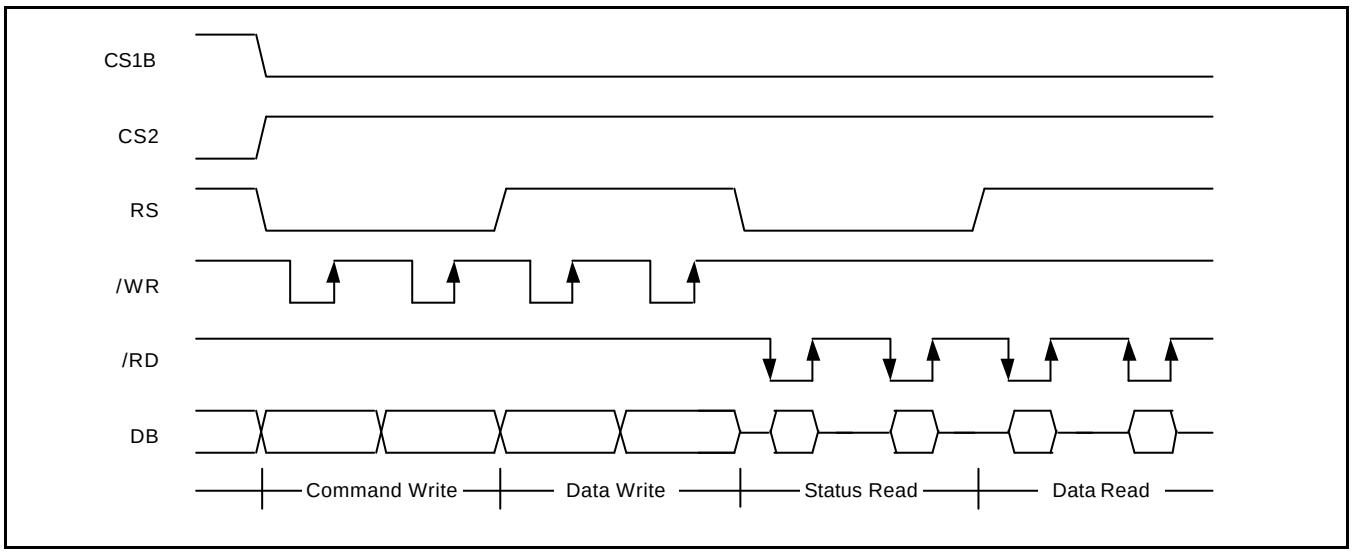


Figure 6. 8080-Series MPU Interface Protocol (PS="H", MI="L")

Serial Interface (PS = "L", MI="H" or "L")

When the S6B1713 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

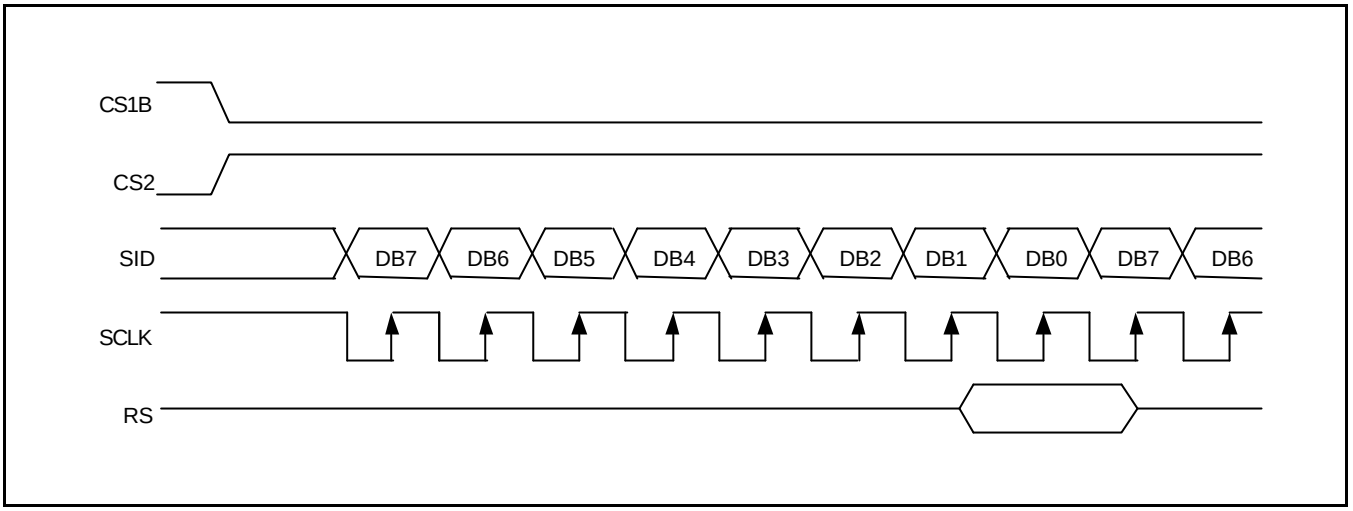


Figure 7. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the S6B1713 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B1713 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 8. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 9. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

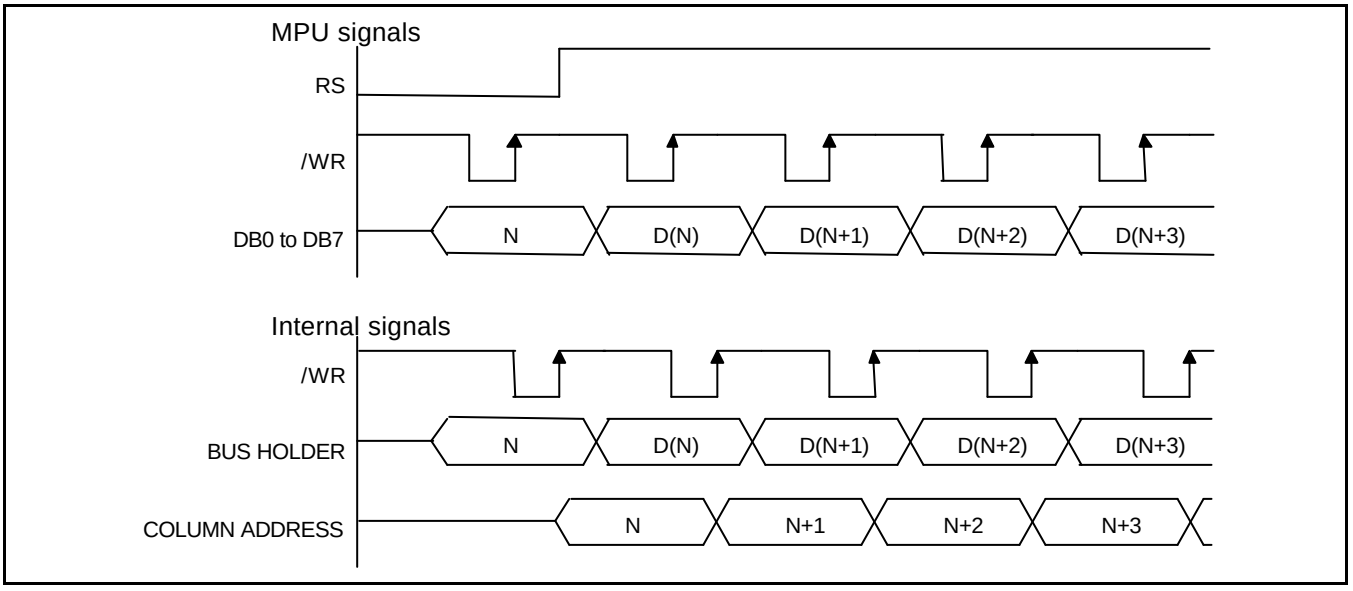


Figure 8. Write Timing

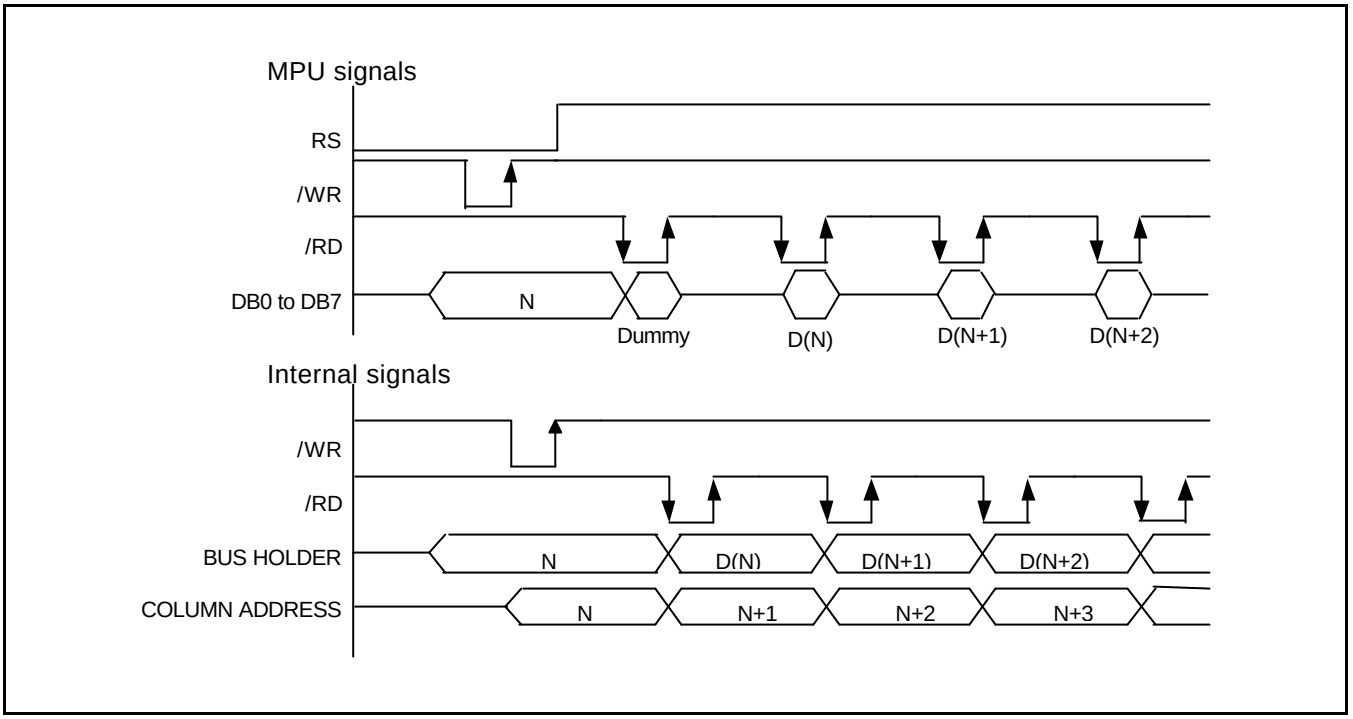


Figure 9. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 65-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in Figure 10. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

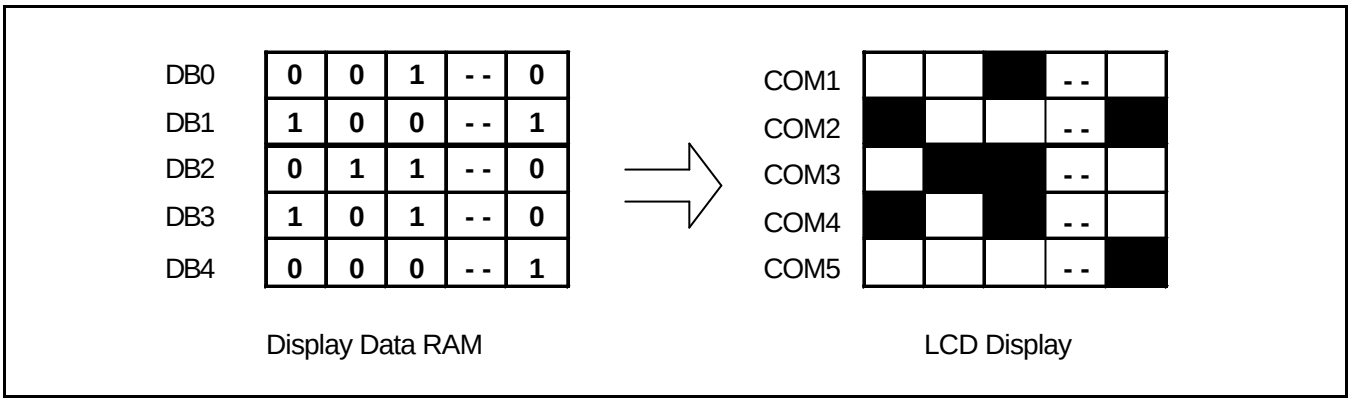


Figure 10. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in Figure 12. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 8 (DB3 is "H", but DB2, DB1 and DB0 are "L") is a special RAM area for the icons and display data DB0 is only valid. When Page Address is above 8, it is impossible to access to on-chip RAM.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM1) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 12. It incorporates 6-bit line address register changed by only the initial display line instruction and 6-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column address circuit has a 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 12. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a Read or Write Data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 11.

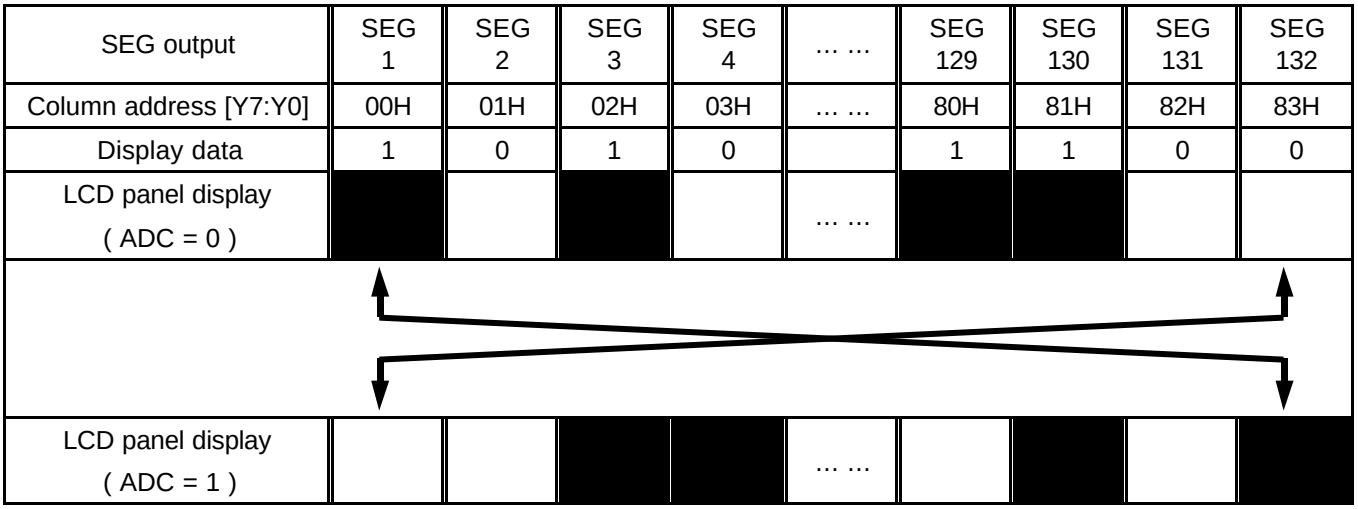


Figure 11. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the Display ON / OFF, Reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

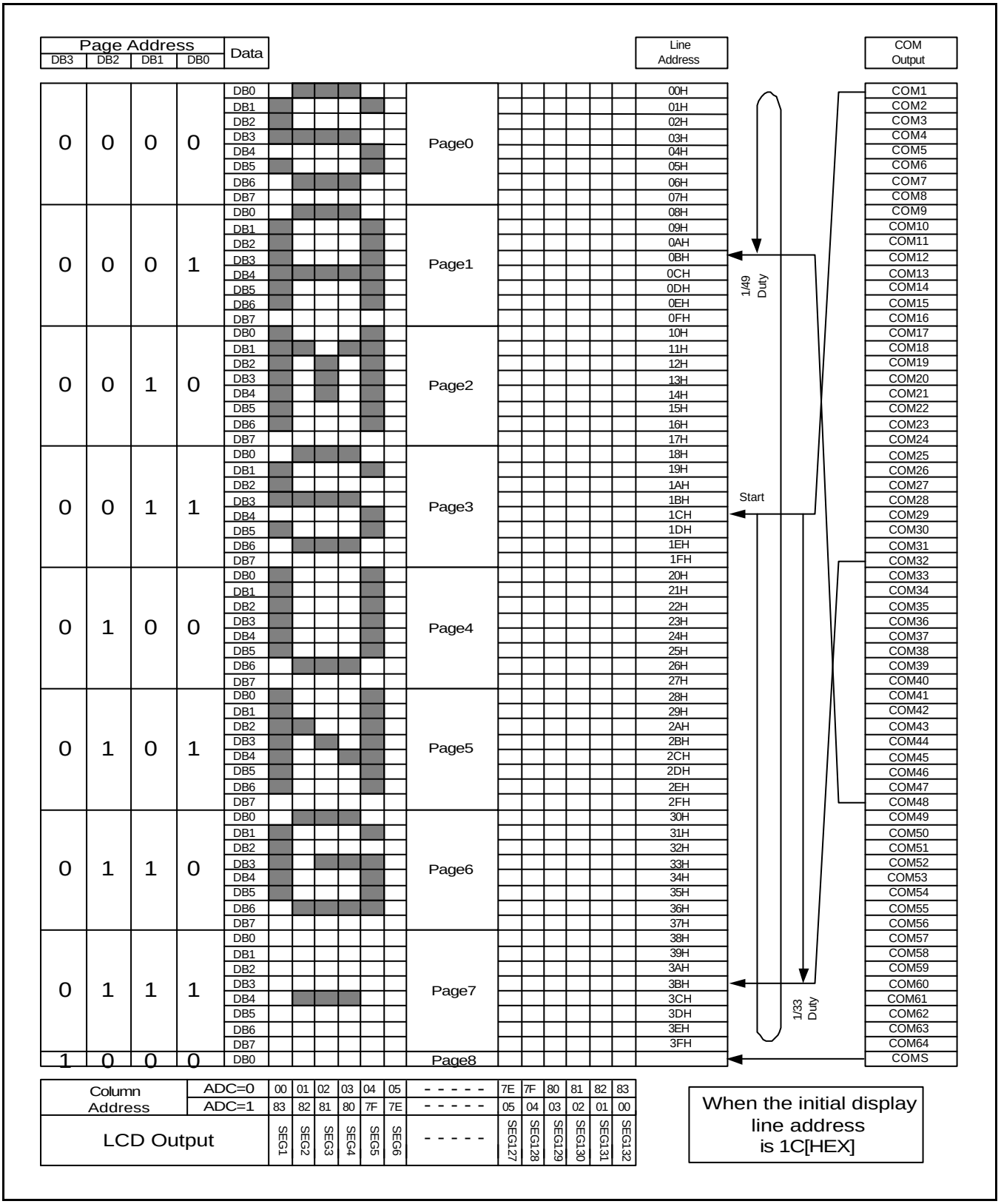


Figure 12. Display Data RAM Map

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of VDD. This oscillator signal is used in the voltage converter and display timing generation circuit.

* Test condition: Temperature: 25°C & 85°C, TEMPS=" L" , No load

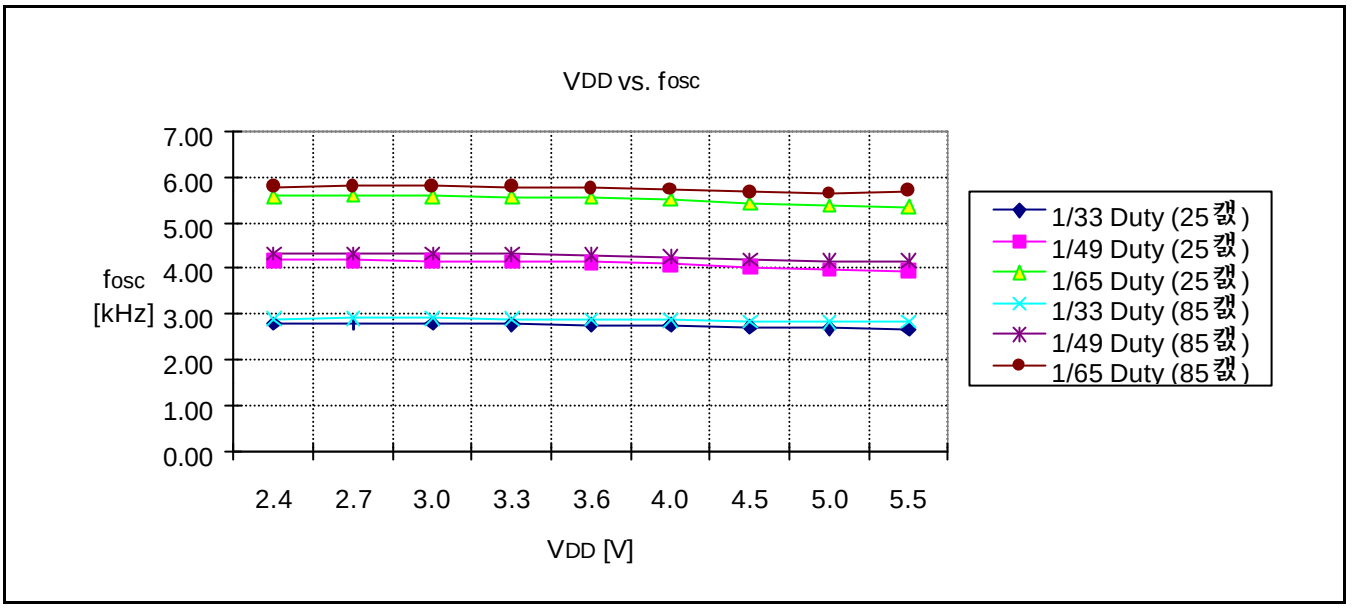


Figure 13. VDD vs. fOSC

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 132-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal(M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in figure 14.

In a multiple-chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 11 shows the M, CL, and DISP status.

Table 11. Master and Slave Timing Signal Status

Operation mode	Oscillator	M	CL	DISP
Master	ON (internal clock used)	Output	Output	Output
	OFF (external clock used)	Output	Input	Output
Slave	-	Input	Input	Input

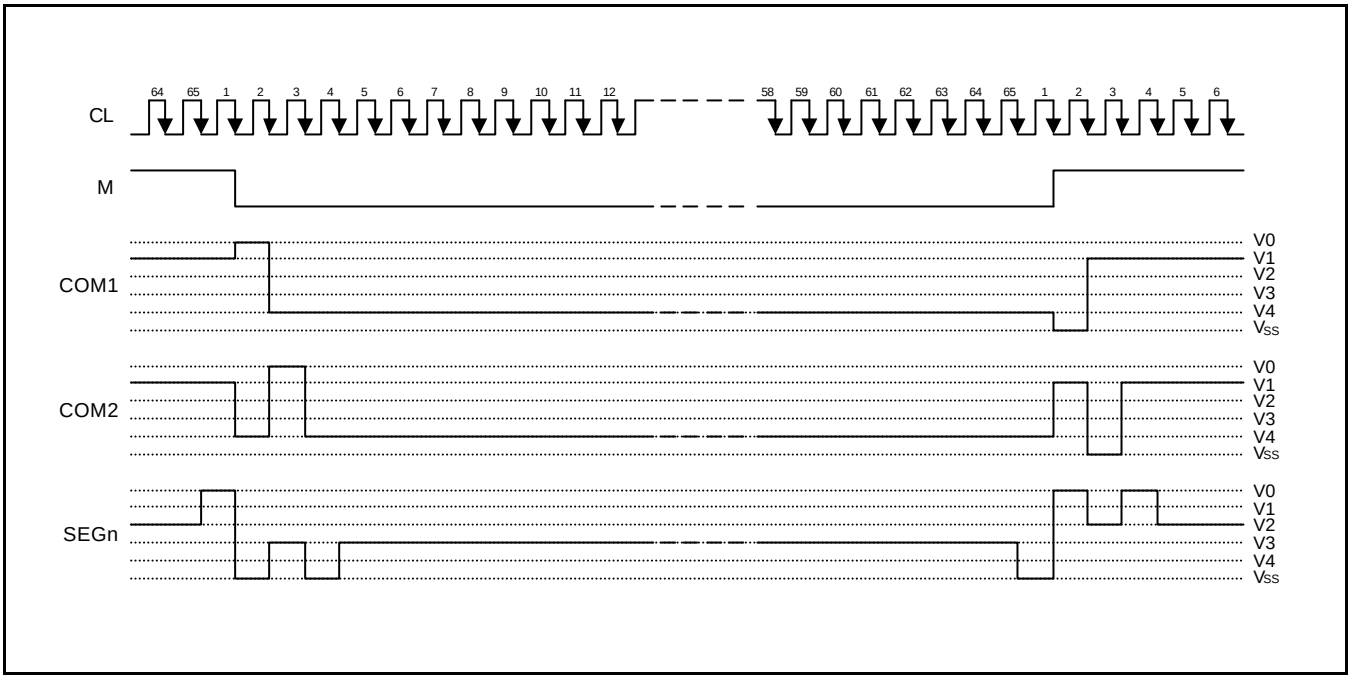


Figure 14. 2-frame AC Driving Waveform (Duty ratio = 1/65)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select Instruction specifies the scanning direction of the common output pins.

Table 12. The Relationship between Duty Ratio and Common Output

Duty	SHL	Common output pins					
		COM[1:16]	COM[17:24]	COM[25:40]	COM[41:48]	COM[49:64]	COMS
1/33	0	COM[1:16]	*NC			COM[17:32]	COMS
	1	COM[32:17]	*NC			COM[16:1]	
1/49	0	COM[1:24]		*NC	COM[25:48]		COMS
	1	COM[48:25]		*NC	COM[24:1]		
1/65	0	COM[1:64]					COMS
	1	COM[64:1]					

*NC: No Connection

LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel common drivers (including 2 COMS channels) and 132-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.

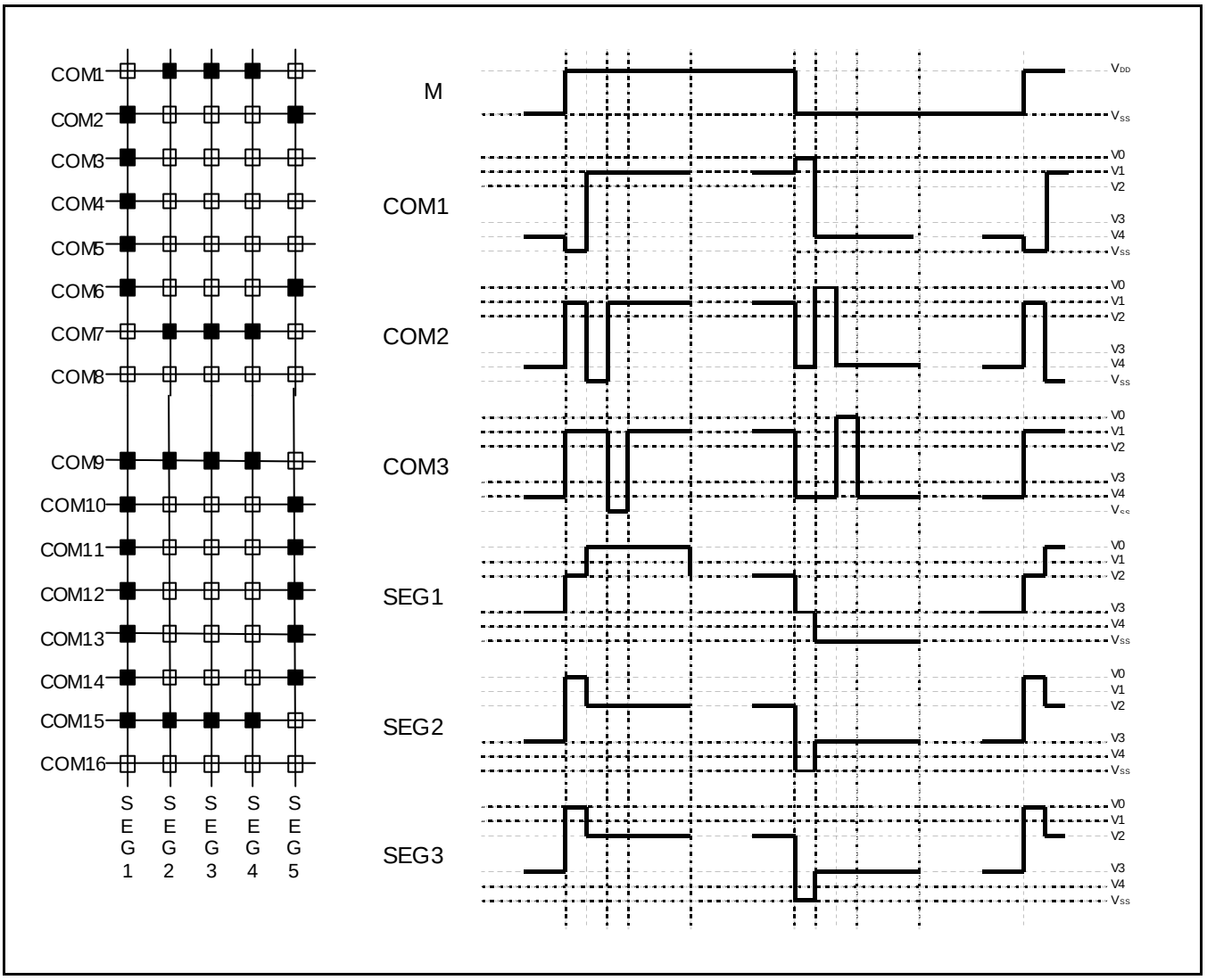


Figure 15. Segment and Common Timing

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 13 shows the referenced combinations in using power supply circuits.

Table 13. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	Open	External input	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VDD and VSS to 2, 3, 4 or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 μF]

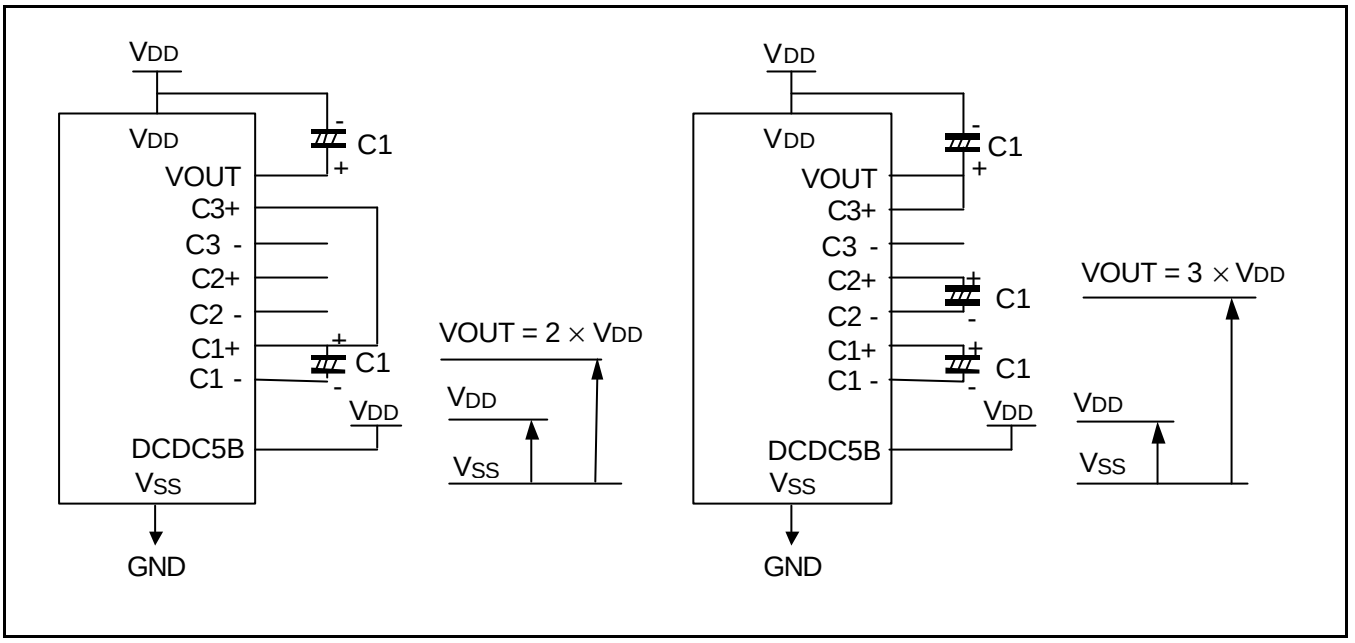


Figure 16. Two Times Boosting Circuit **Figure 17. Three Times Boosting Circuit**

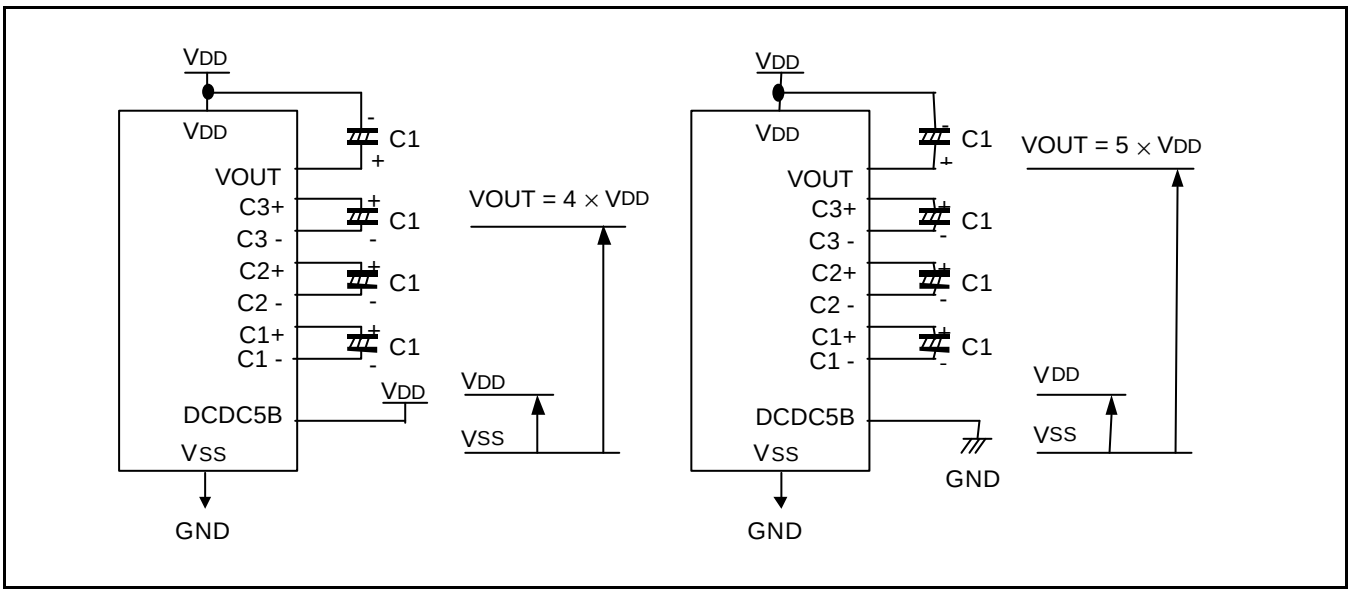


Figure 18. Four Times Boosting Circuit **Figure 19. Five Times Boosting Circuit**

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 20, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in table 14-1.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 1)}$$

$$V_{EV} = \left(1 - \frac{(63 - \alpha)}{300}\right) \times V_{REF} \quad [V] \text{ ------ (Eq. 2)}$$

Table 14-1. V_{REF} Voltage at Ta = 25 °C

TEMPS	Temp. coefficient	V_{REF} [V]
L	-0.05% / °C	2.0
H	-0.2% / °C	2.0

Table 14-2. Reference Voltage Parameters (a)

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

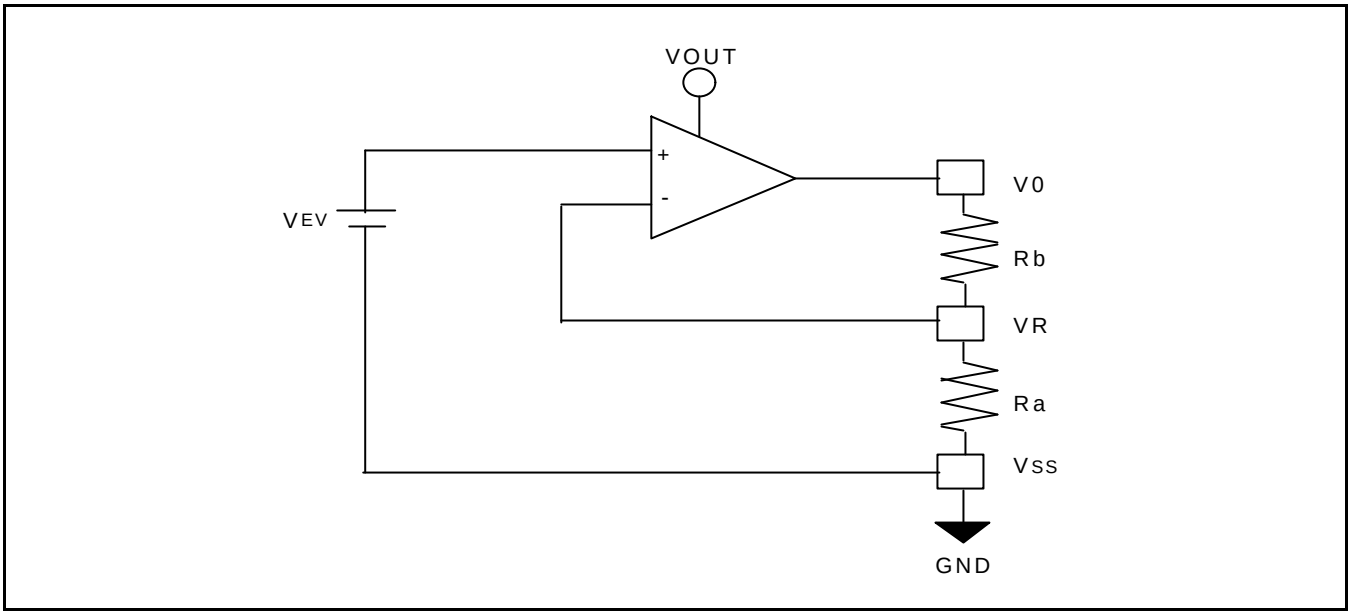


Figure 20. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

Table 15. Internal Rb / Ra Ratio depending on 3-bit Data (R2 R1 R0)

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1+(Rb / Ra)	1.90	2.19	2.55	3.02	3.61	4.35	5.29	6.48

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

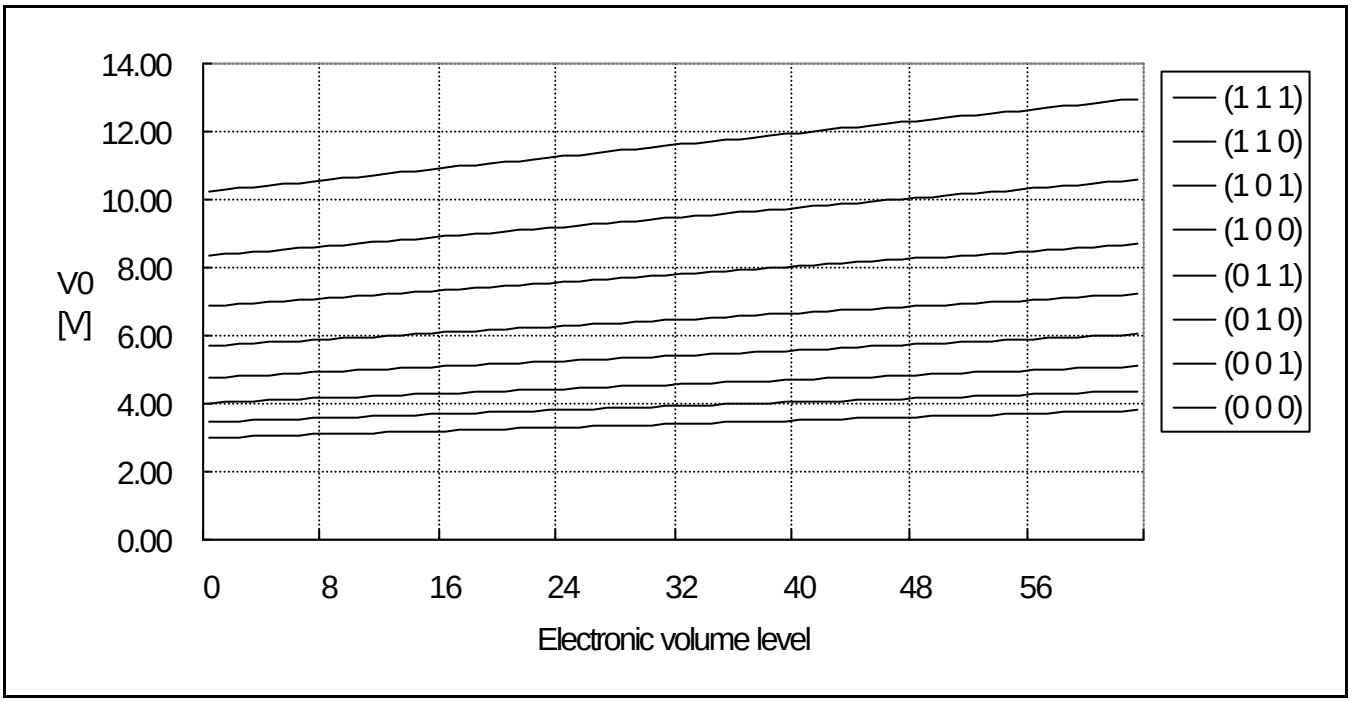


Figure 21. Electronic Volume Level

In Case of Using External Resistors, Ra and Rb. (INTRS = "L")

When INTRS pin is "L", it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \text{ ------ (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(63 - 32)}{300}\right) \times 2.0 = 1.79 \quad [V] \text{ ------ (Eq. 4)}$$

From requirement 3.

$$\frac{10}{Ra + Rb} = 1 \text{ [uA]} \quad \text{------ (Eq. 5)}$$

From equations Eq. 3, 4 and 5
Ra = 1.79 [MΩ]
Rb = 8.21 [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 16. V0 Depending on Electronic Volume Level

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.83	.....	10.00	.....	11.17

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the Voltage Follower for increasing drive capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 17. The Relationship between V1 to V4 level and Duty Ratio

Duty Ratio	DUTY1	DUTY0	LCD Bias	V1	V2	V3	V4
1/33	L	L	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
			1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/49	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/65	H	L/H	1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
			1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0

REFERECE CIRCUIT EXAMPLES

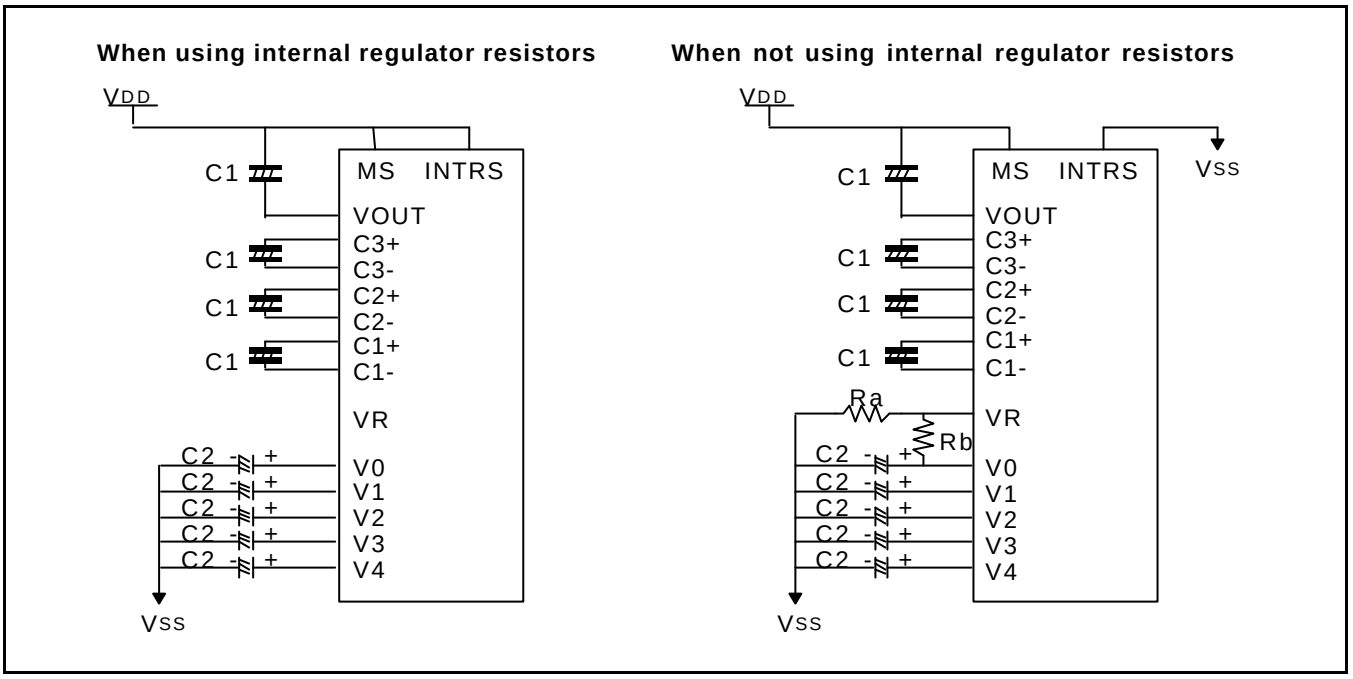


Figure 22. When Using all LCD Power Circuits (4-Time V/C: ON, V/R: ON, V/F: ON)

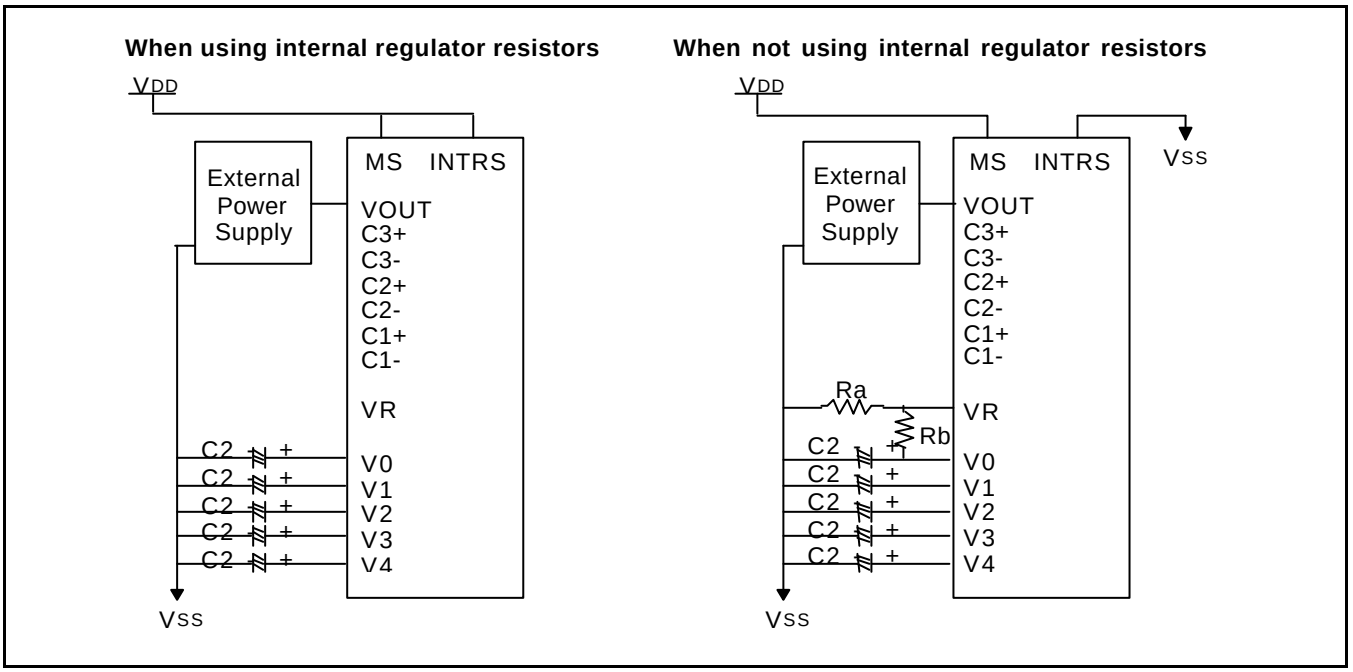


Figure 23. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

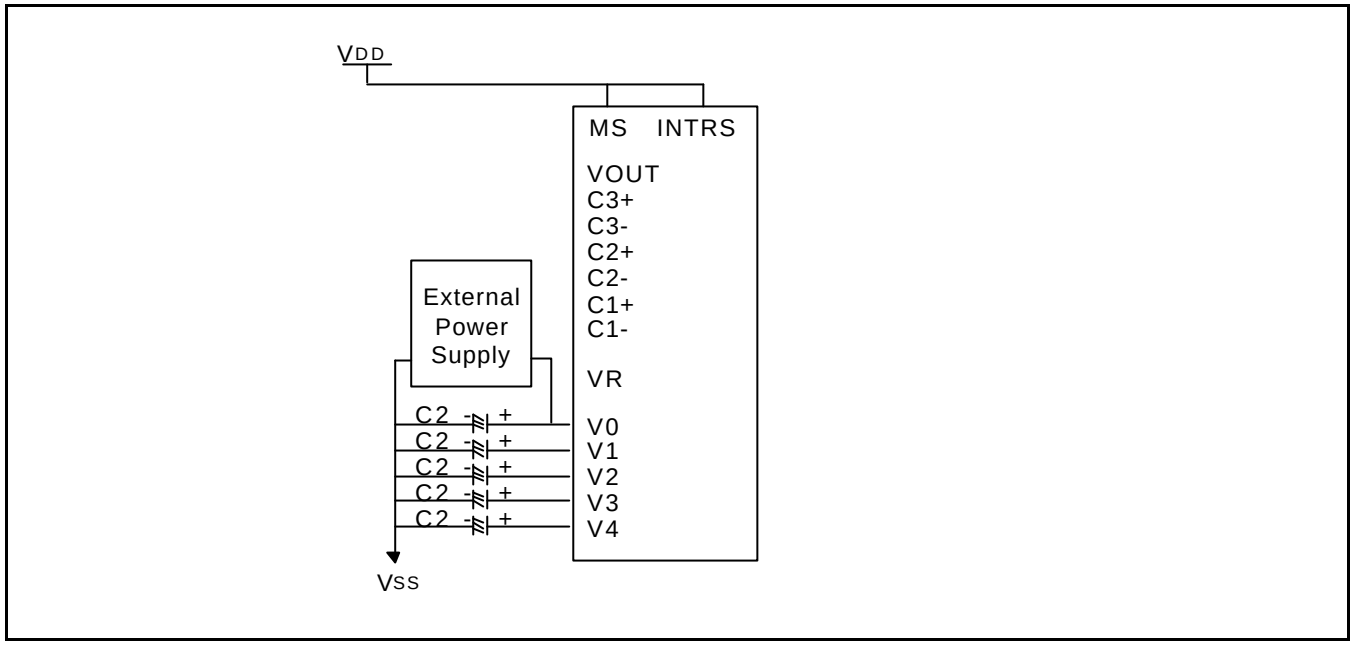
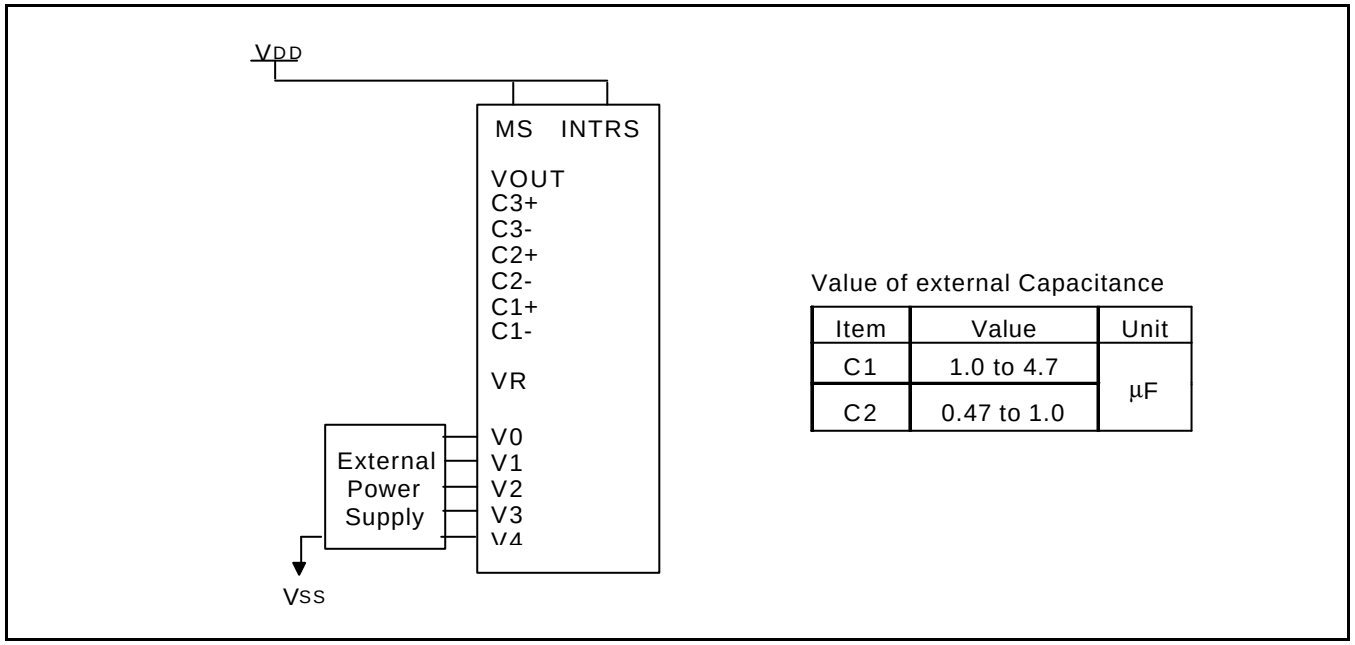


Figure 24. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)



Value of external Capacitance

Item	Value	Unit
C1	1.0 to 4.7	µF
C2	0.47 to 1.0	

Figure 25. When Not Using any Internal LCD Power Supply Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

Display ON / OFF: OFF
Entire display ON / OFF: OFF (normal)
ADC select: OFF (normal)
Reverse display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
LCD bias ratio: 1/7 (1/65 duty), 1/6 (1/49 duty), 1/5 (1/33 duty)
Read-modify-write: OFF
SHL select: OFF (normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure is occurred.

Read-modify-write: OFF
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
SHL select: 0
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)

While RESETB is "L" or Reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 18. Instruction Table

× : Don' t care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0	Read the internal status
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn on/off LCD panel When DON = 0: display OFF When DON = 1: display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM1
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage Mode
Set reference voltage register	0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction When ADC = 0: normal direction (SEG1→SEG132) When ADC = 1: reverse direction (SEG132→SEG1)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal / entire display ON When EON = 0: normal display. When EON = 1: entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
SHL select	0	0	1	1	0	0	SHL	×	×	×	Select COM output direction When SHL = 0: normal direction (COM1→COM64) When SHL = 1: reverse direction (COM64→COM1)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON
Test instruction	0	0	1	1	1	1	×	×	×	×	***Don't use this instruction.***

" x" : don' t care

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display Data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

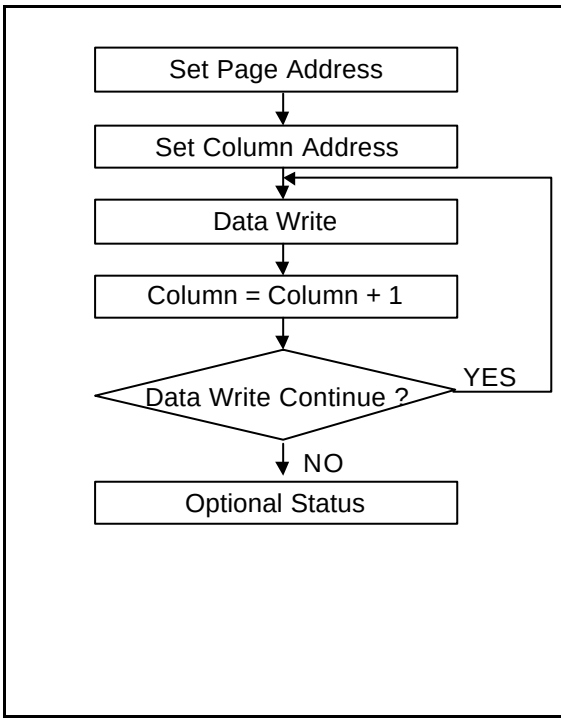


Figure 26. Sequence for Writing Display Data

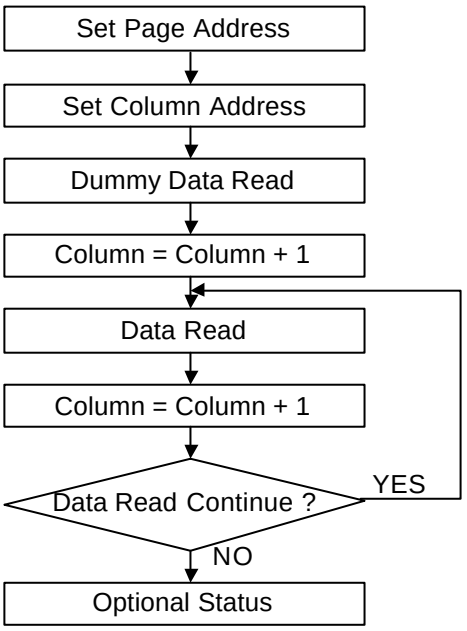


Figure 27. Sequence for Reading Display Data

Read Status

Indicates the internal status of the S6B1713.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON / OFF	RESETB	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG132 → SEG1), 1: normal direction (SEG1 → SEG132)
ON / OFF	Indicates display ON / OFF status 0: display ON, 1: display OFF
RESETB	Indicates the initialization is in progress by RESETB signal. 0: chip is active, 1: chip is being reset.

Display ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

Initial Display Line

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM1 when SHL = L, COM64 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Reference Voltage Select

Consists of 2-byte instruction
The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction: Set Reference Voltage Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

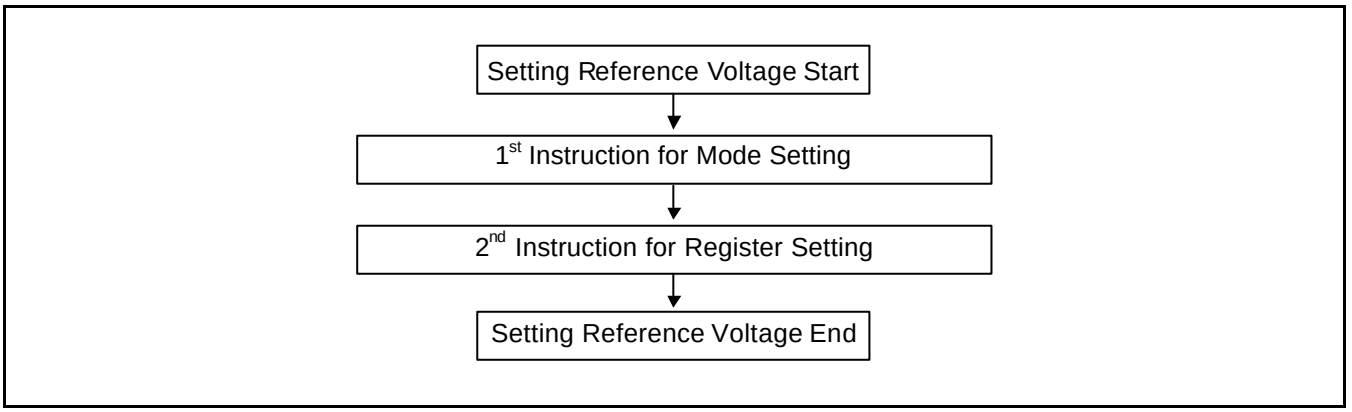


Figure 28. Sequence for Setting the Reference Voltage

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, column addresses are automatically increased.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG1 → SEG132)
ADC = 1: reverse direction (SEG132 → SEG1)

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DUTY1	DUTY0	LCD bias	
			Bias = 0	Bias = 1
1/33	0	0	1/5	1/6
1/49	0	1	1/6	1/8
1/65	1	0/1	1/7	1/9

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

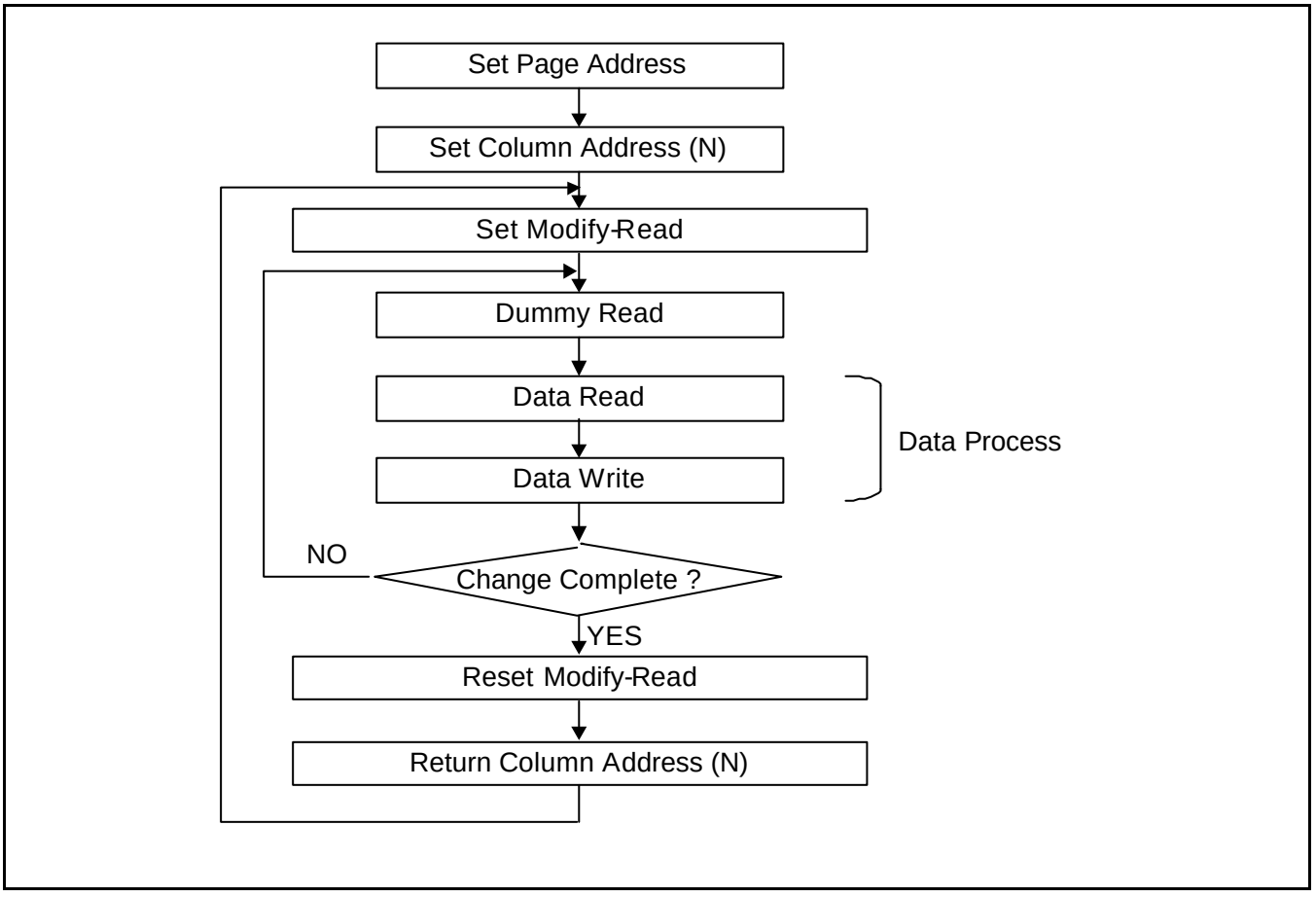


Figure 29. Sequence for Cursor Display

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply which is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

×: Don't care

SHL = 0: normal direction (COM1 → COM64)
SHL = 1: reverse direction (COM64 → COM1)

Power control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0 1			Internal voltage converter circuit is OFF Internal voltage converter circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1 + (Rb / Ra)
0	0	0	1.90
0	0	1	2.19
0	1	0	2.55
0	1	1	3.02
1	0	0	3.61
1	0	1	4.35
1	1	0	5.29
1	1	1	6.48

Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator mode) enables the second byte instruction (set Static Indicator register) to be valid. The first byte sets the static indicator ON / OFF. When it is on, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

The 1st Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The 2nd Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, S6B1713 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode). When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the display ON and entire display OFF instruction.

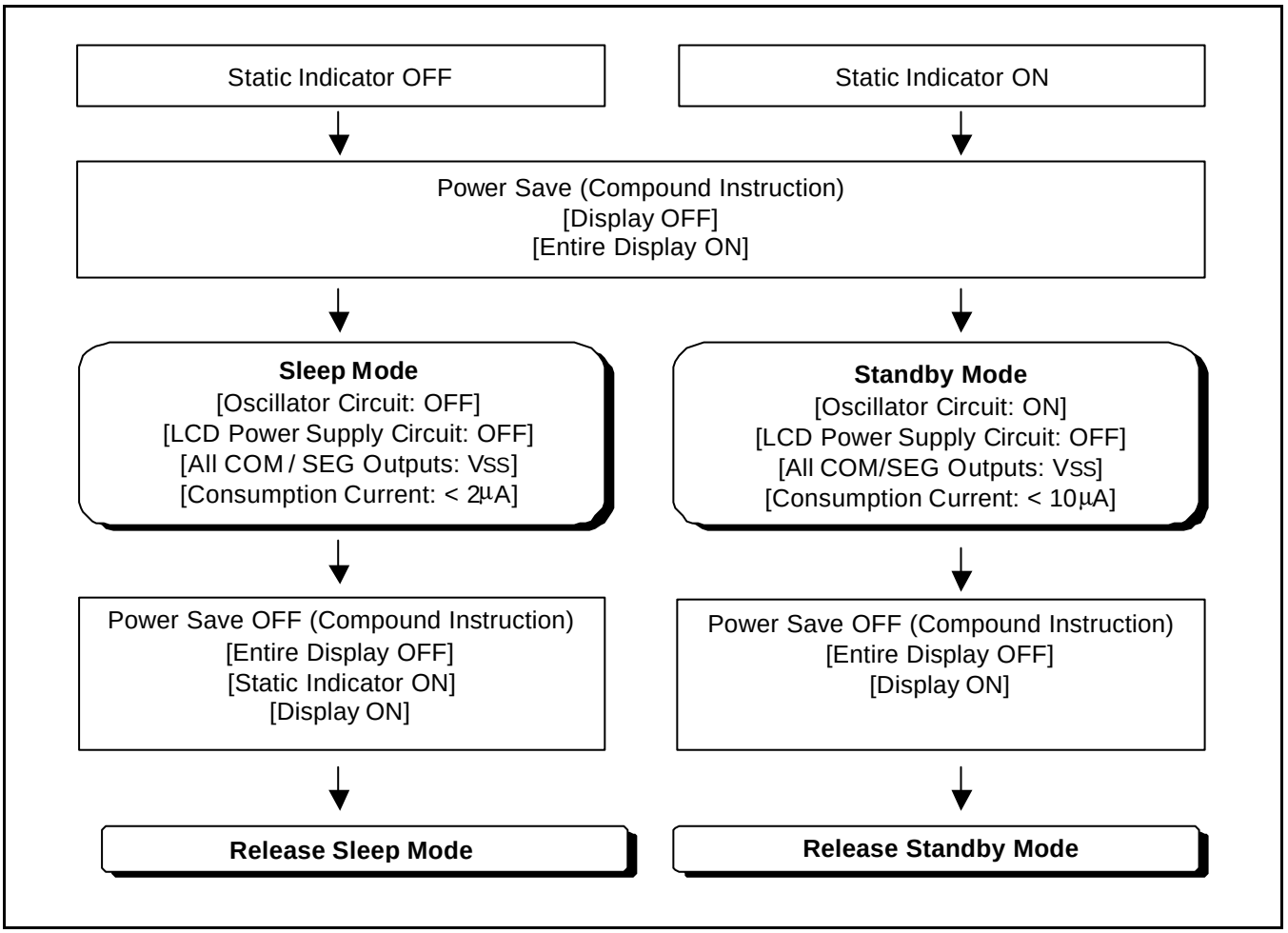


Figure 30. Power Save Routine

Referential Instruction Setup Flow (1)

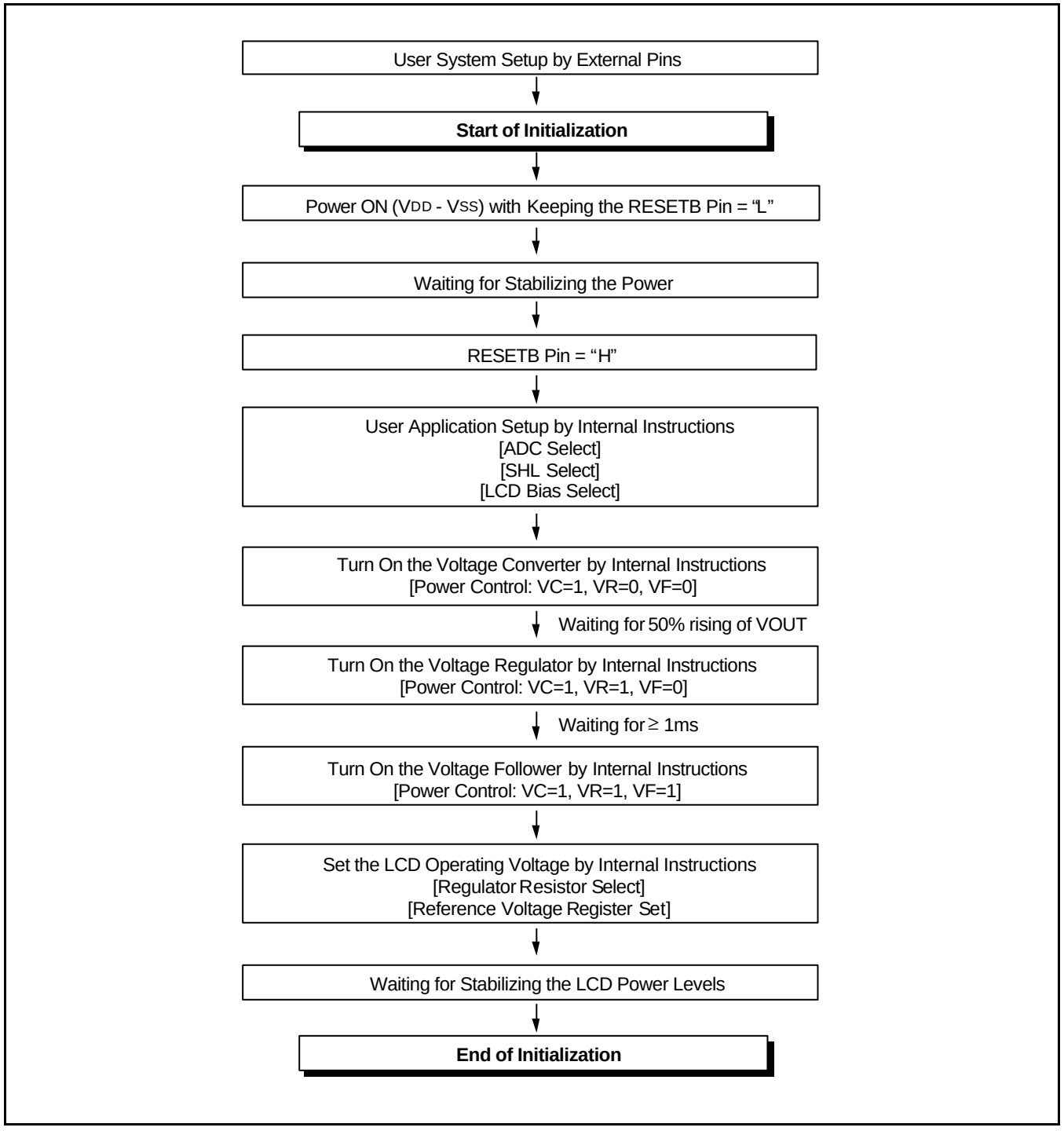


Figure 31. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow (2)

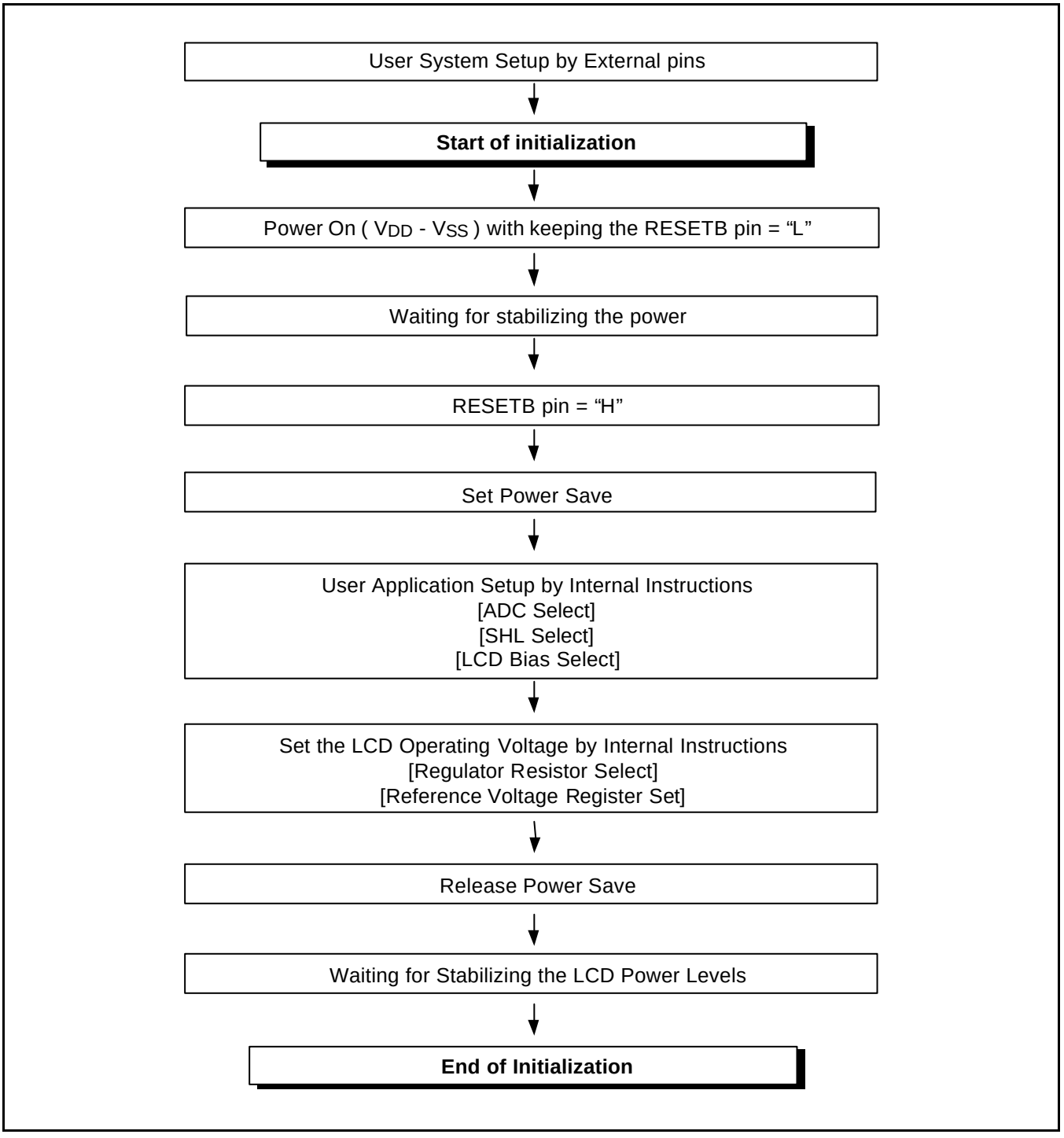


Figure 32. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow (3)

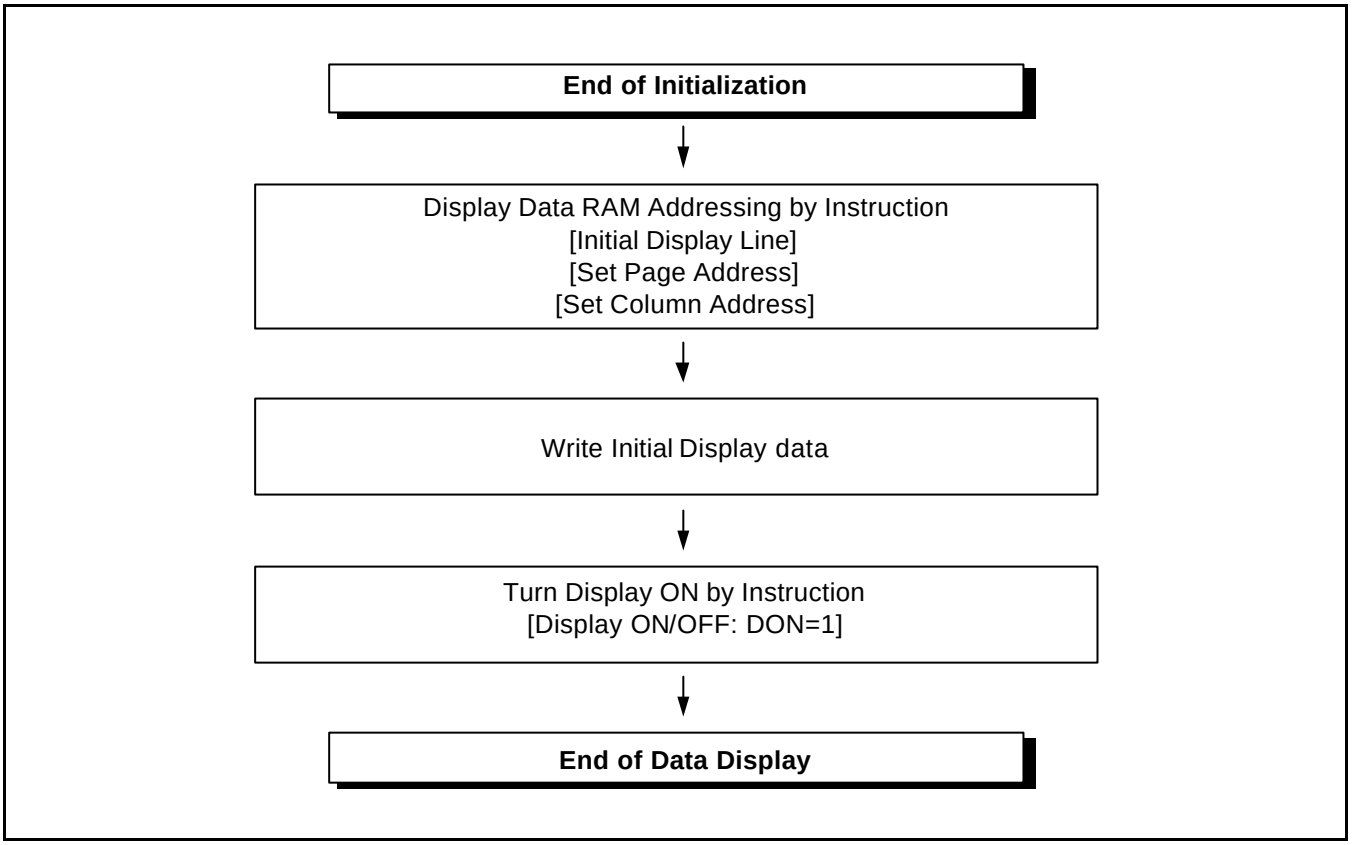


Figure 33. Data Displaying

Referential Instruction Setup Flow (4)

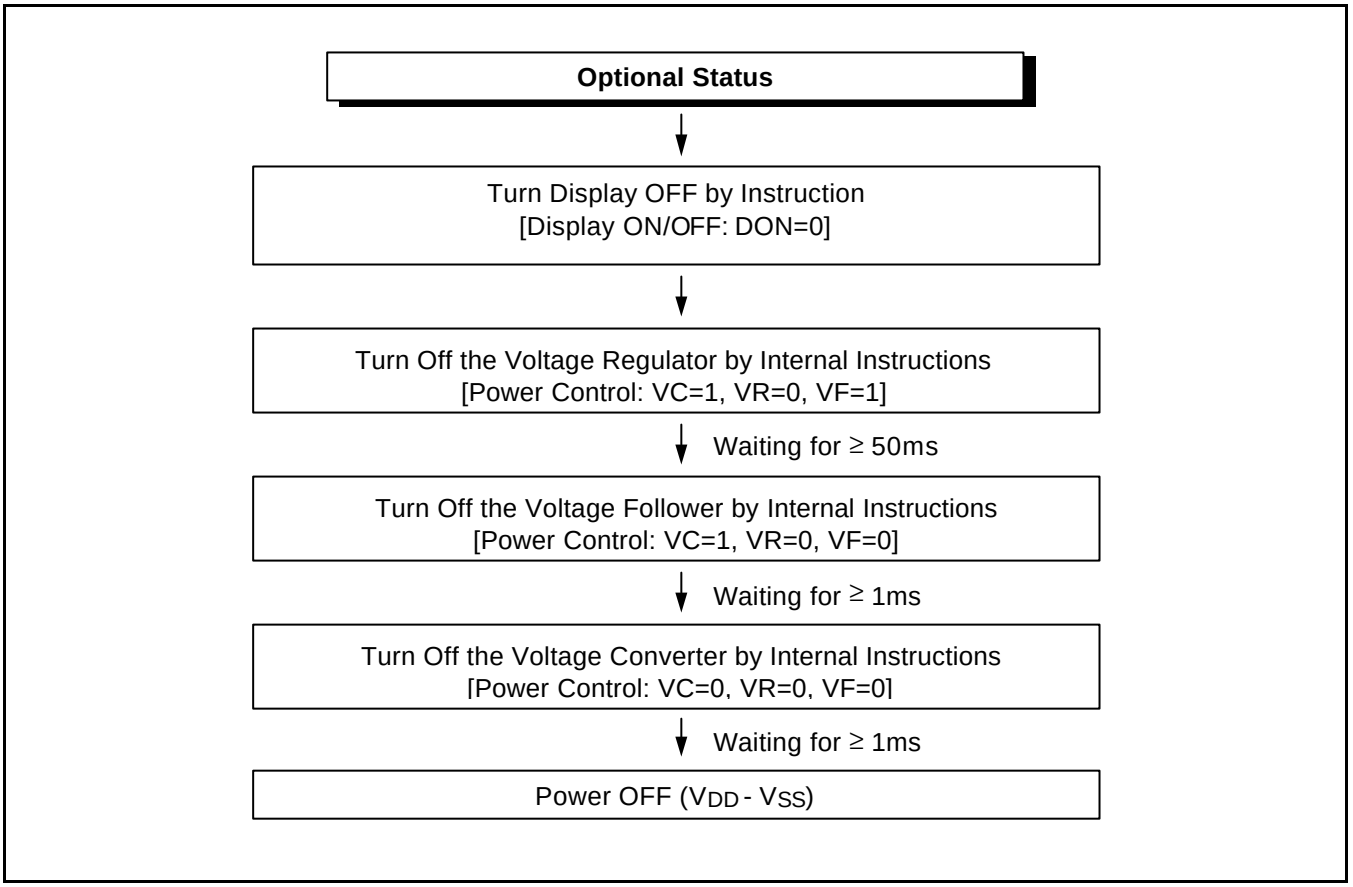


Figure 34. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to +7.0	V
	V_{LCD}	-0.3 to +17.0	V
Input voltage range	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating temperature range	T_{OPR}	-40 to +85	°C
Storage temperature range	T_{STR}	-55 to +125	°C

NOTES:

1. VDD and VLCD are based on VSS = 0V.
2. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied. (VLCD = V0 – VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 20. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 5.5V, Ta = -40 to 85°C)

Item		Symbol	Condition	Min.	Typ.	Max	Unit	Pin used
Operating voltage (1)		V_{DD}	Select by product code	2.4	-	5.5	V	V_{DD} *1
Operating voltage (2)		V0		4.0	-	15.0	V	V0 *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{DD} = 3.0V V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*5
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*6
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	KΩ	SEGn COMn *7
Oscillator frequency (1)	Internal	f_{OSC}	V_{DD} = 3.0V Ta = 25°C Duty ratio = 1/65, 1/33	17	22	27	kHz	CL *8
	External	f_{CL}		4.25	5.50	6.75		
Oscillator frequency (2)	Internal	f_{OSC}	V_{DD} = 3.0V Ta = 25°C Duty ratio = 1/49	20	25	30	kHz	CL *8
	External	f_{CL}		3.33	4.17	5.00		
Voltage converter input voltage		V_{DD}	× 2	2.4	-	5.5	V	V_{DD}
			× 3	2.4	-	5.0		
			× 4	2.4	-	3.75		
			× 5	2.4	-	3.0		
Voltage converter output voltage		VOUT	×2 / ×3 / ×4 / ×5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage		VOUT		4.0	-	15.0	V	VOUT
Voltage follower operating voltage		V0		4.0	-	15.0	V	V0 *9
Reference voltage		V_{REF0}	V_{DD} = 3.0V, Ta = 25°C, -0.05%/°C	1.94	2.00	2.06	V	*10
		V_{REF1}	V_{DD} = 3.0V, Ta = 25°C, -0.2%/°C	1.94	2.00	2.06	V	*10

Dynamic Current Consumption (1) when the Built-in Power Circuit is OFF (At Operate Mode)

(Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V_{DD} = 3.0V V0 – V_{SS} = 11.0V 1/65 duty ratio Display pattern OFF	-	-	20	µA	*11

Dynamic Current Consumption (2) when the built-in power circuit is ON (At operate mode)

(Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	I_{DD2}	V_{DD} = 3.0V, quad boosting, V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern OFF, Normal power mode	-	70	100	µA	*12
		V_{DD} = 3.0V, quad boosting, V0 – V_{SS} = 11.0V, 1/65 duty ratio, Display pattern checker, Normal power mode	-	95	160	µA	*12

Current Consumption During Power Save Mode

(Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	I_{DDS1}	V_{DD} = 3.0V During sleep	-	-	2.0	µA	
Standby mode current	I_{DDS2}	V_{DD} = 3.0V During standby	-	-	10.0	µA	

Table 21. The Relationship between Oscillation Frequency and Frame Frequency

Duty Ratio	Item	f_{CL}	f_M
1/65	On-chip oscillator circuit is used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{8 \times 65}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 65}$
1/49	On-chip oscillator circuit is used	$\frac{f_{OSC}}{6}$	$\frac{f_{OSC}}{12 \times 49}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 49}$
1/33	On-chip oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{16 \times 33}$
	On-chip oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{2 \times 33}$

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_M: LCD AC signal frequency)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, MI, PS, INTRS, HPM, TEMPS, BSTS, DCDC5B, CLS, CL, M, DISP pins.
*4. DB0 to DB7, M, FRS, DISP, CL pins.
*5. CS1B, CS2, RS, DB [7:0], E_RD, RW_WR, RESETB, MS, MI, PS, INTRS, HPM, TEMPS, BSTS, DCDC5B, CLS, CL, M, DISP pins.
*6. Applies when the DB [7:0], M, DISP, and CL pins are in high impedance.
*7. Resistance value when ± 0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON= ΔV / 0.1 [kΩ] (ΔV: voltage change when ± 0.1[mA] is applied in the ON status.)
*8. See table 21 for the relationship between oscillation frequency and frame frequency.
*9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range
*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

REFERENCE DATA

I_{DD1} vs. V_{DD}

* Test Condition: Temperature: 25°C & 85°C, V0 = 11V (External), TEMPS = 'L', 1/65 duty, Normal Power Mode

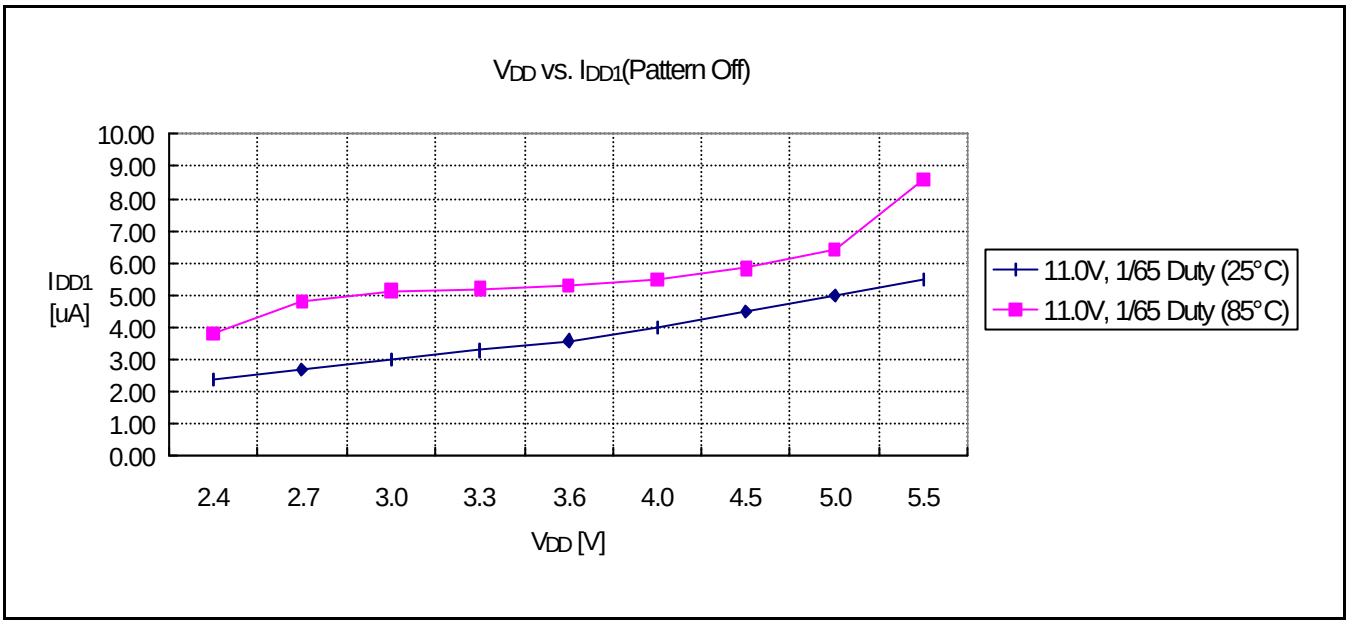


Figure 35. Display Pattern is OFF

IDD2 vs. VDD

* Test Condition: Temperature: 25°C & 85°C, 1/65 duty, Quad Boosting, RR = 6, EV = 32

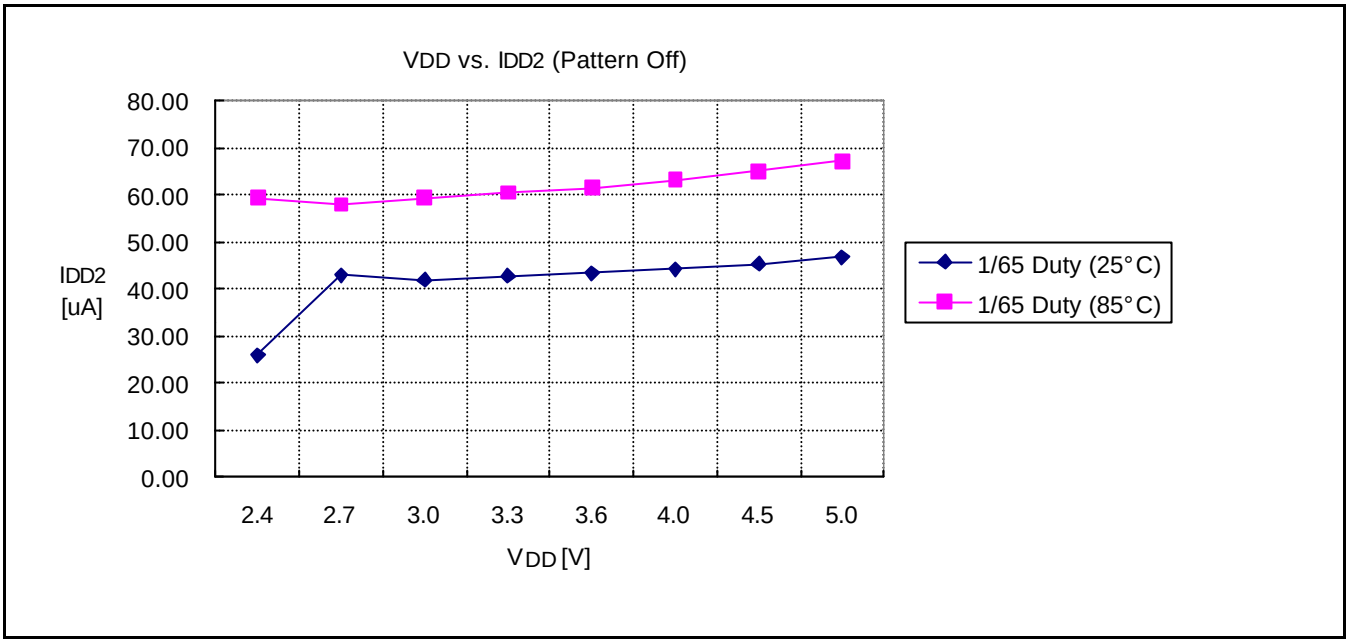


Figure 36. Display Pattern is OFF

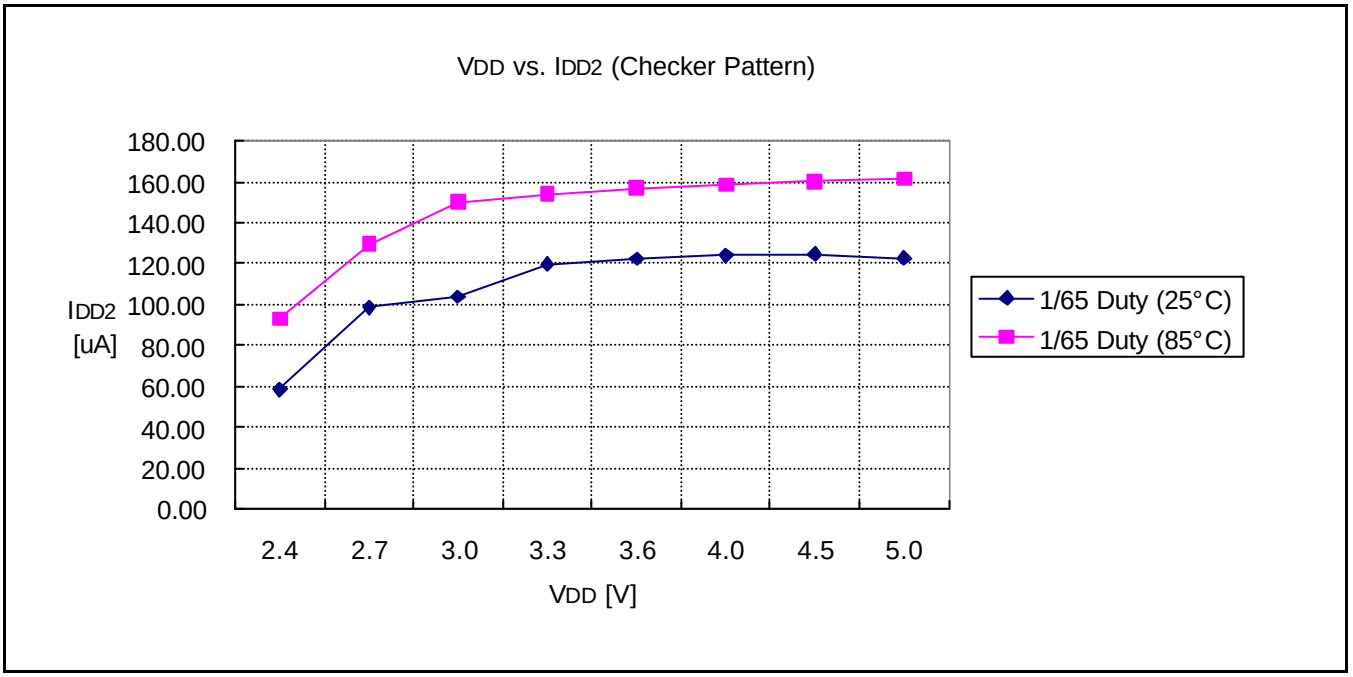
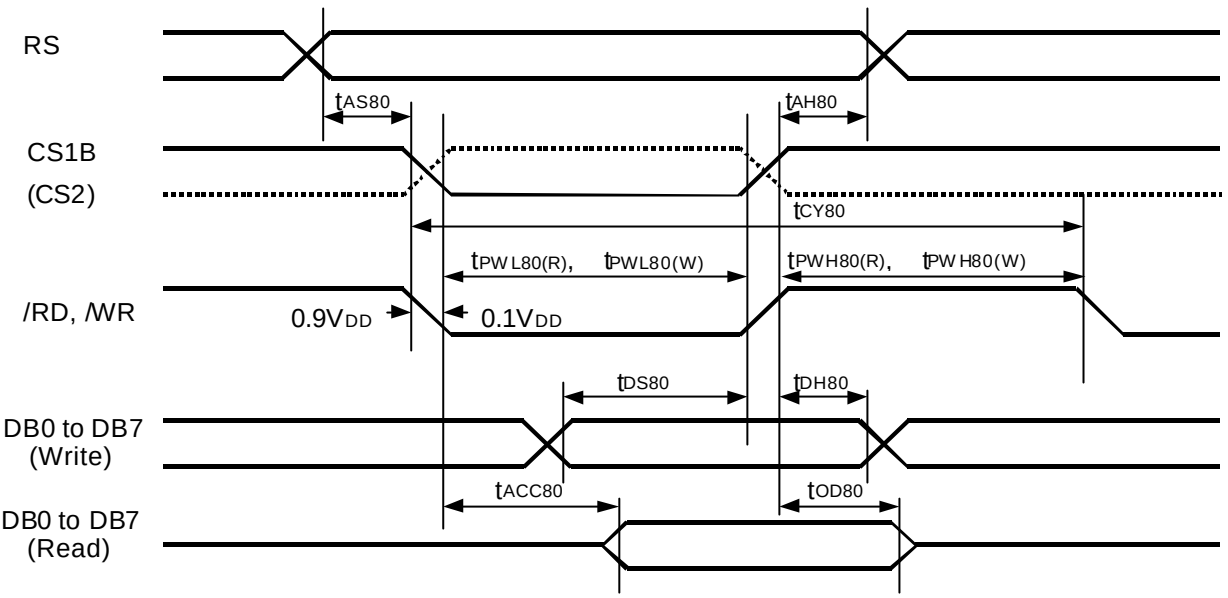


Figure 37. Display Pattern is Checker

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)



** $t_{PWL80(W)}$ and $t_{PWL80(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and /WR(/RD) is low.

Figure 38. Read / Write Characteristics (8080-series MPU)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

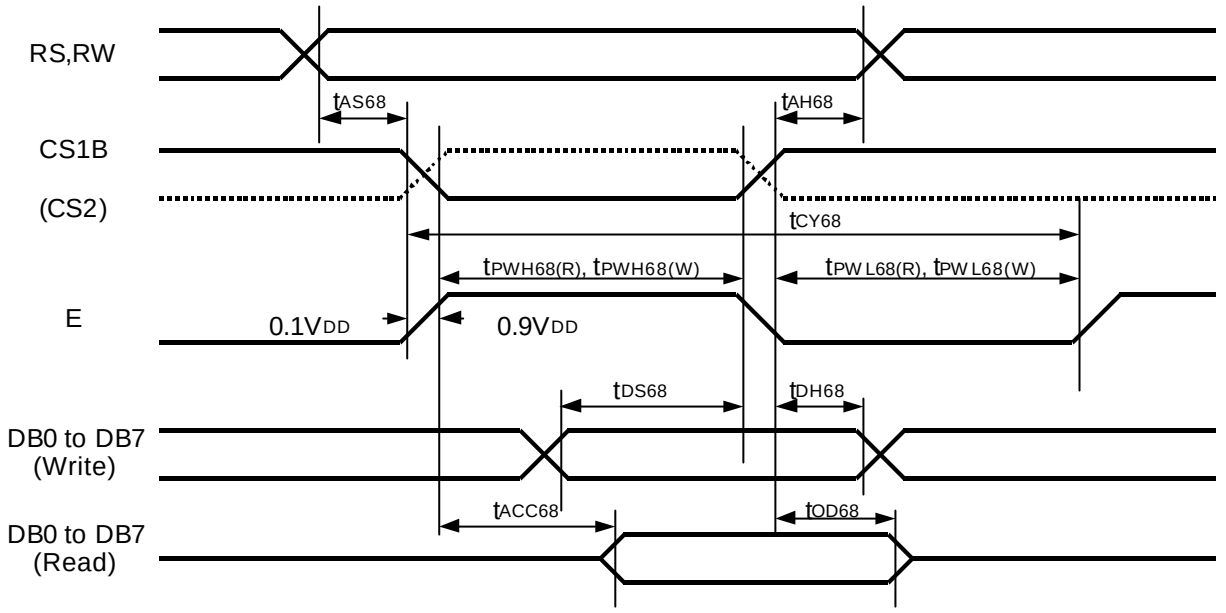
Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS80} t_{AH80}	13 17	-	-	ns	
System cycle time		/WR, /RD	t_{CY80}	400	-	-	ns	
Enable Pulse Low width	Read	/WR, /RD	$t_{PWL80\ (R)}$	125	-	-	ns	
	Write		$t_{PWL80\ (W)}$	55	-	-	ns	
Enable Pulse High width	Read	/WR, /RD	$t_{PWH80\ (R)}$	245	-	-	ns	
	Write		$t_{PWH80\ (W)}$	315	-	-	ns	
Data setup time Data hold time		DB7 To DB0	t_{DS80} t_{DH80}	35 13	-	-	ns	
Read access time Output disable time			t_{ACC80} t_{OD80}	- 10	-	125 90	ns	C_L = 100 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS80} t_{AH80}	10 10	-	-	ns	
System cycle time		/WR, /RD	t_{CY80}	160	-	-	ns	
Enable Pulse Low width	Read	/WR, /RD	$t_{PWL80\ (R)}$	65	-	-	ns	
	Write		$t_{PWL80\ (W)}$	25	-	-	ns	
Enable Pulse High width	Read	/WR, /RD	$t_{PWH80\ (R)}$	65	-	-	ns	
	Write		$t_{PWH80\ (W)}$	105	-	-	ns	
Data setup time Data hold time		DB7 To DB0	t_{DS80} t_{DH80}	18 10	-	-	ns	
Read access time Output disable time			t_{ACC80} t_{OD80}	- 10	-	65 45	ns	C_L = 100 pF

Note The input signal rising time and falling time (tr, tf) is specified at 15ns or less. Or (tr + tf) < (t_{CY80} – $t_{PWL80\ (W)}$ – $t_{PWH80\ (W)}$) for write, (tr + tf) < (t_{CY80} – $t_{PWL80\ (R)}$ – $t_{PWH80\ (R)}$) for read

Read / Write Characteristics (6800-series Microprocessor)



** $t_{PWH68(W)}$ and $t_{PWH68(R)}$ is specified in the overlapped period when CS1B is low (CS2 is high) and E is high.

Figure 39. Read / Write Characteristics (6800-series Microprocessor)

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	t_{AS68} t_{AH68}	13 17	-	-	ns	
System cycle time		E	t_{CY68}	400	-	-	ns	
Enable Pulse Low Width	Read	E	$t_{PWL68\ (R)}$	125	-	-	ns	
	Write		$t_{PWL68\ (W)}$	55	-	-		
Enable Pulse High Width	Read	E	$t_{PWH68\ (R)}$	245	-	-	ns	
	Write		$t_{PWH68\ (W)}$	315	-	-		
Data setup time Data hold time		DB7 To DB0	t_{DS68} t_{DH68}	35 13	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	125 90	ns	C_L = 100 pF

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS,RW	t_{AS68} t_{AH68}	10 10	-	-	ns	
System cycle time		E	t_{CY68}	160	-	-	ns	
Enable Pulse Low Width	Read	E	$t_{PWL68\ (R)}$	65	-	-	ns	
	Write		$t_{PWL68\ (W)}$	25	-	-		
Enable Pulse High Width	Read	E	$t_{PWH68\ (R)}$	65	-	-	ns	
	Write		$t_{PWH68\ (W)}$	105	-	-		
Data setup time Data hold time		DB7 To DB0	t_{DS68} t_{DH68}	18 10	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	65 45	ns	C_L = 100 pF

Note: 1. The input signal rising time and falling time (tr, tf) is specified at 15ns or less.
Or (tr + tf) < (t_{CY68} – $t_{PWL68\ (W)}$ – $t_{PWH68\ (W)}$) for write, (tr + tf) < (t_{CY68} – $t_{PWL68\ (R)}$ – $t_{PWH68\ (R)}$) for read.

Serial Interface Characteristics

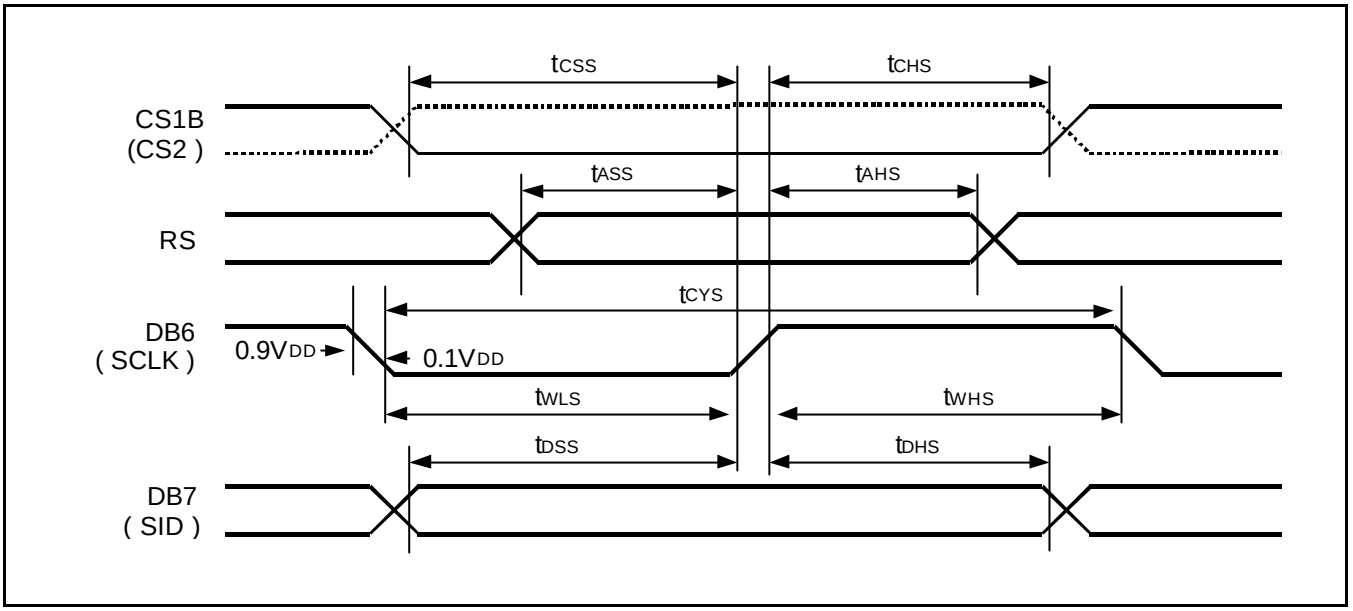


Figure 40. Serial Interface Characteristics

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	tCYS tWHS tWLS	450 180 135	- - -	- - -	ns	
Address setup time Address hold time	RS	tASS tAHS	90 360	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	tDSS tDHS	90 90	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	55 180	- -	- -	ns	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	tCYS tWHS tWLS	225 90 70	- - -	- - -	ns	
Address setup time Address hold time	RS	tASS tAHS	45 180	- -	- -	ns	
Data setup time Data hold time	DB7 (SID)	tDSS tDHS	45 45	- -	- -	ns	
CS1B setup time CS1B hold time	CS1B	tCSS tCHS	25 90	- -	- -	ns	

Reset Input Timing

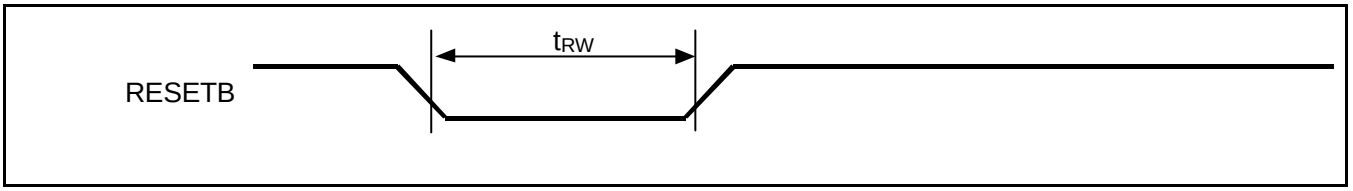


Figure 41. Reset Input Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	900	-	-	ns	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESETB	t_{RW}	450	-	-	ns	

Display Control Output Timing

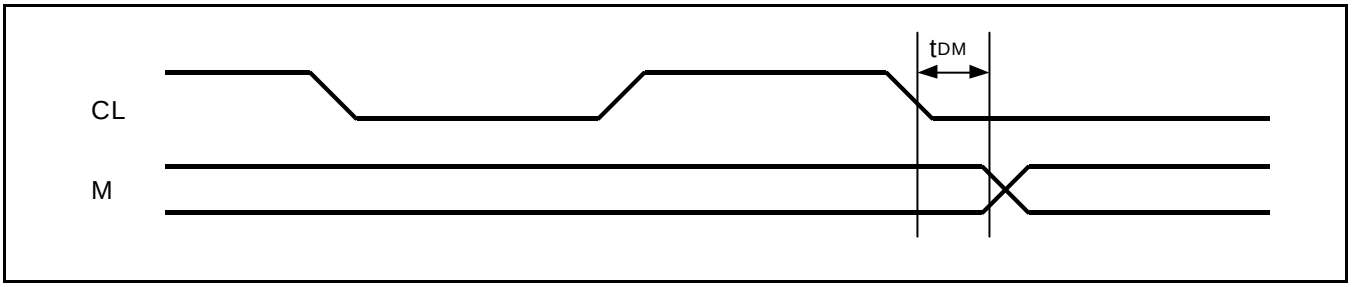


Figure 42. Display Control Output Timing

(V_{DD} = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
M delay time	M	t_{DM}	-	13	70	ns	

(V_{DD} = 4.5 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
M delay time	M	t_{DM}	-	10	35	ns	

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = “H”, MI = “H”)

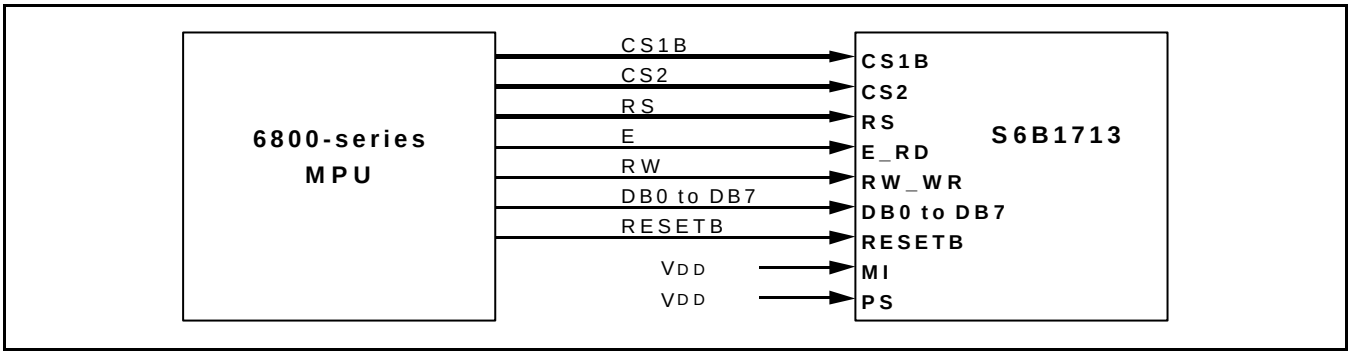


Figure 43. Interfacing with 6800-series (PS = “H”, MI = “H”)

In Case of Interfacing with 8080-series (PS = “H”, MI = “L”)

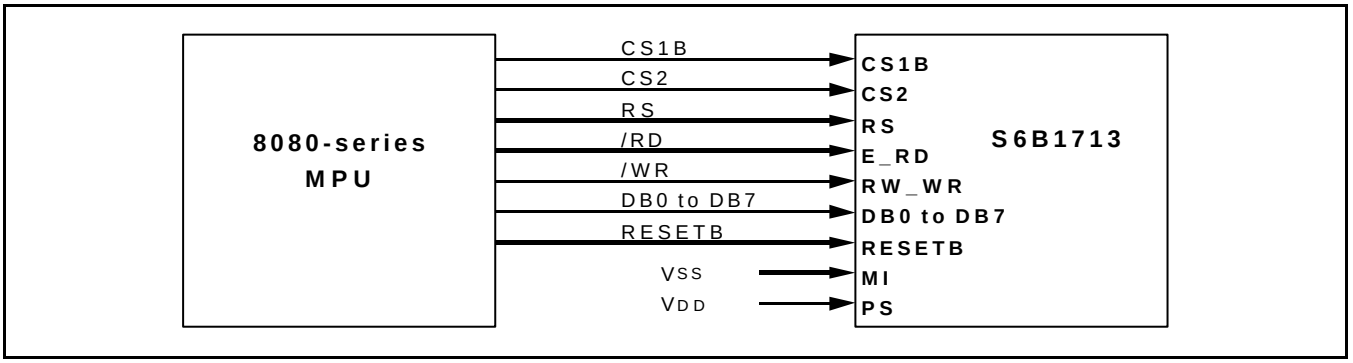


Figure 44. Interfacing with 8080-series (PS = “H”, MI = “L”)

In Case of Serial Interface (PS = “L”, MI = “H/L”)

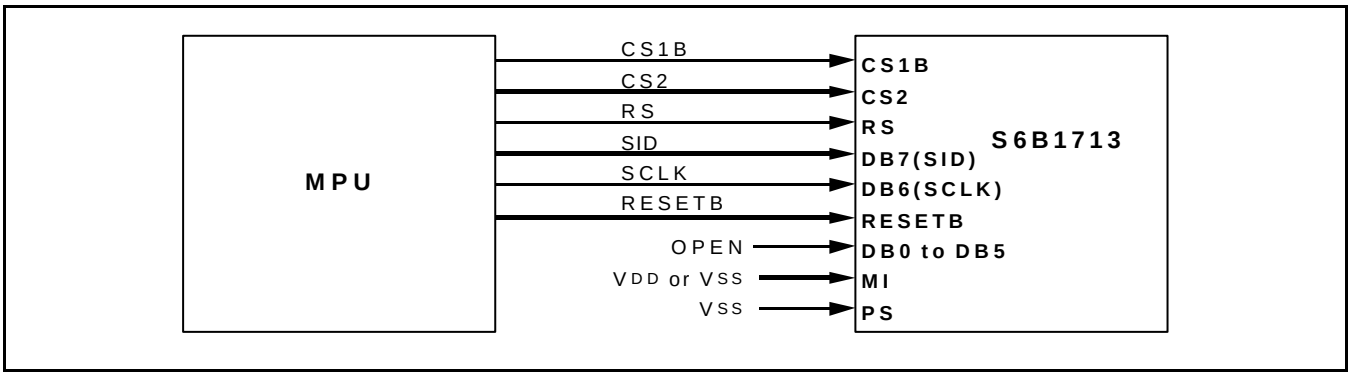


Figure 45. Serial Interface (PS = “L”, MI = “H/L”)

CONNECTIONS BETWEEN S6B1713 AND LCD PANEL

Single Chip Configuration (1/65 Duty Configurations)

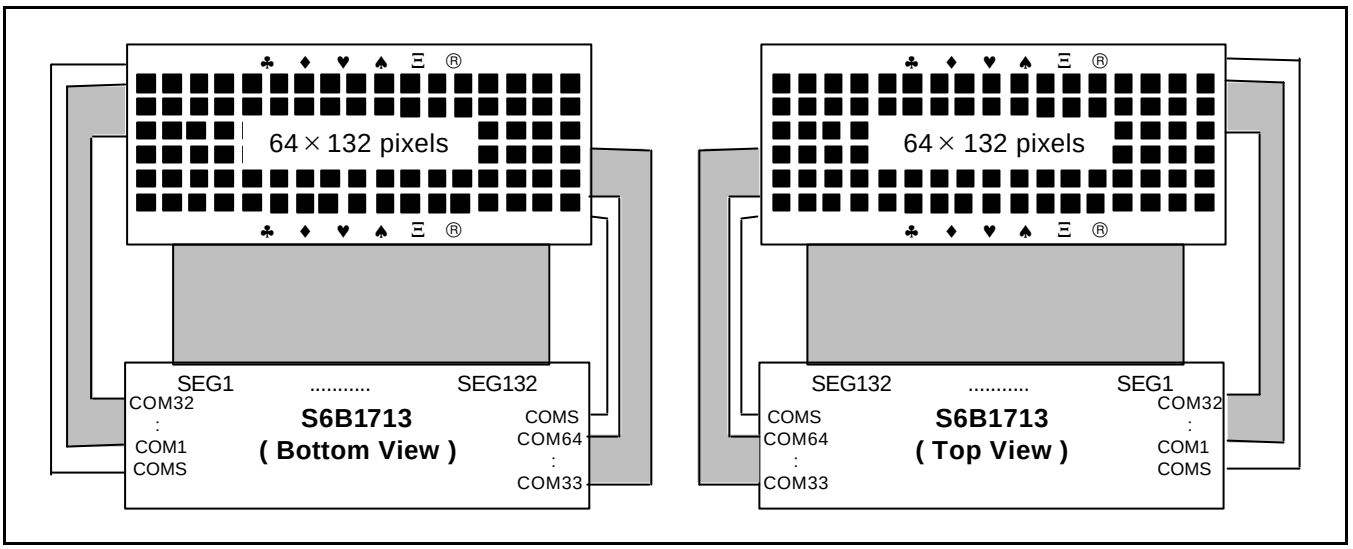


Figure 46. SHL = 0, ADC = 0

Figure 47. SHL = 0, ADC = 1

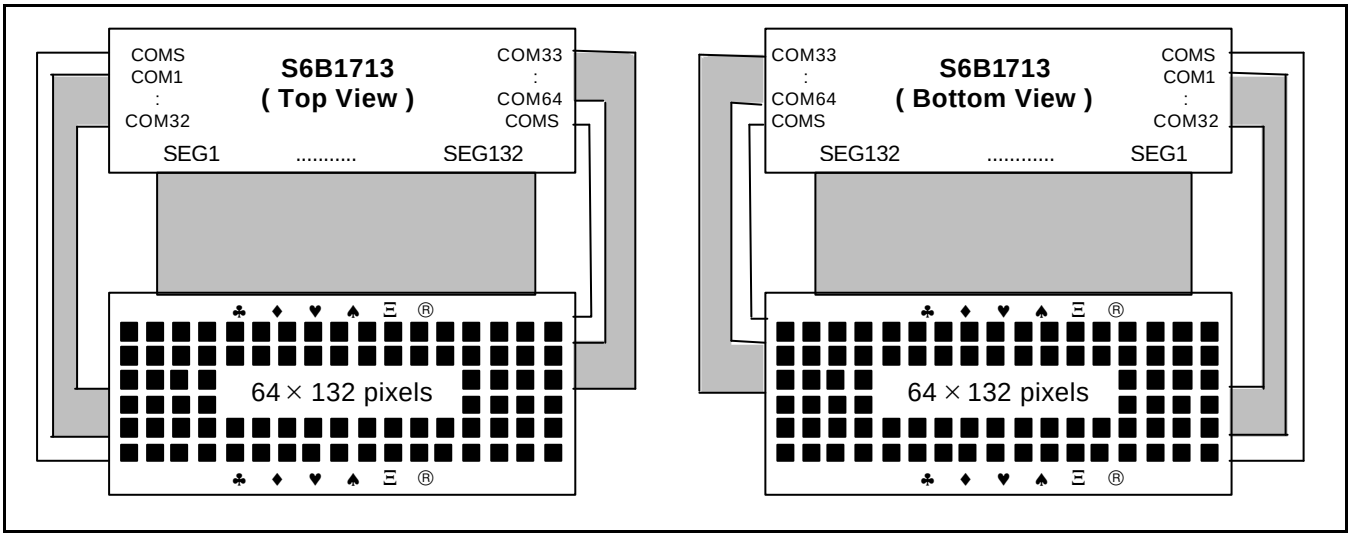


Figure 48. SHL = 1, ADC = 0

Figure 49. SHL = 1, ADC = 1

Single Chip Configuration (1/49 Duty Configurations)

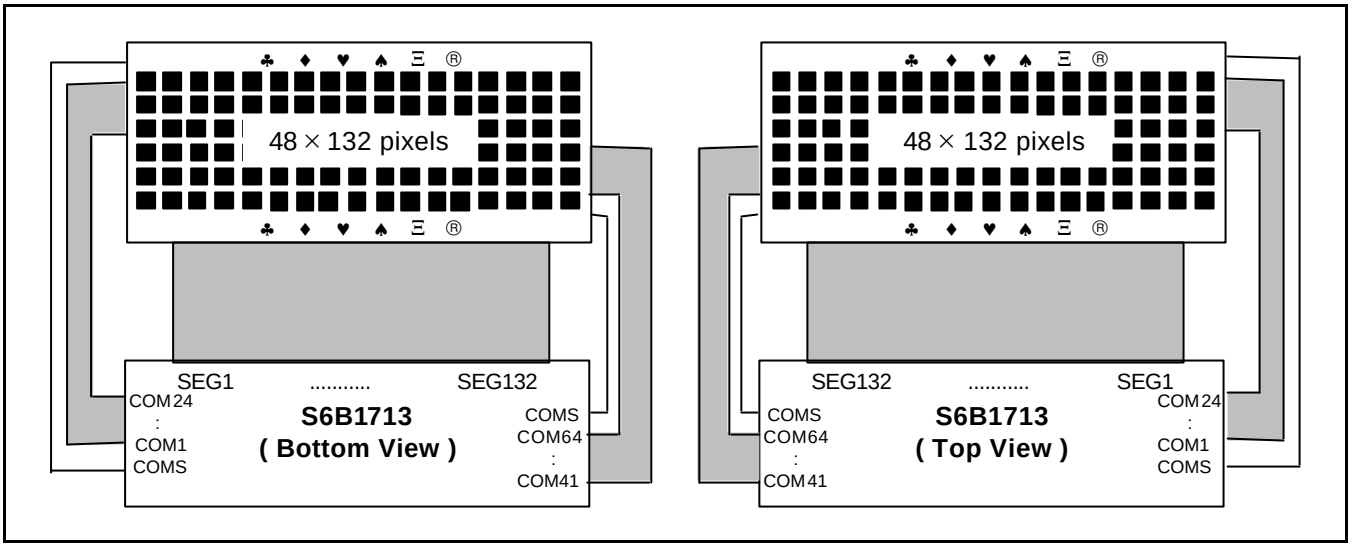


Figure 50. SHL = 0, ADC = 0

Figure 51. SHL = 0, ADC = 1

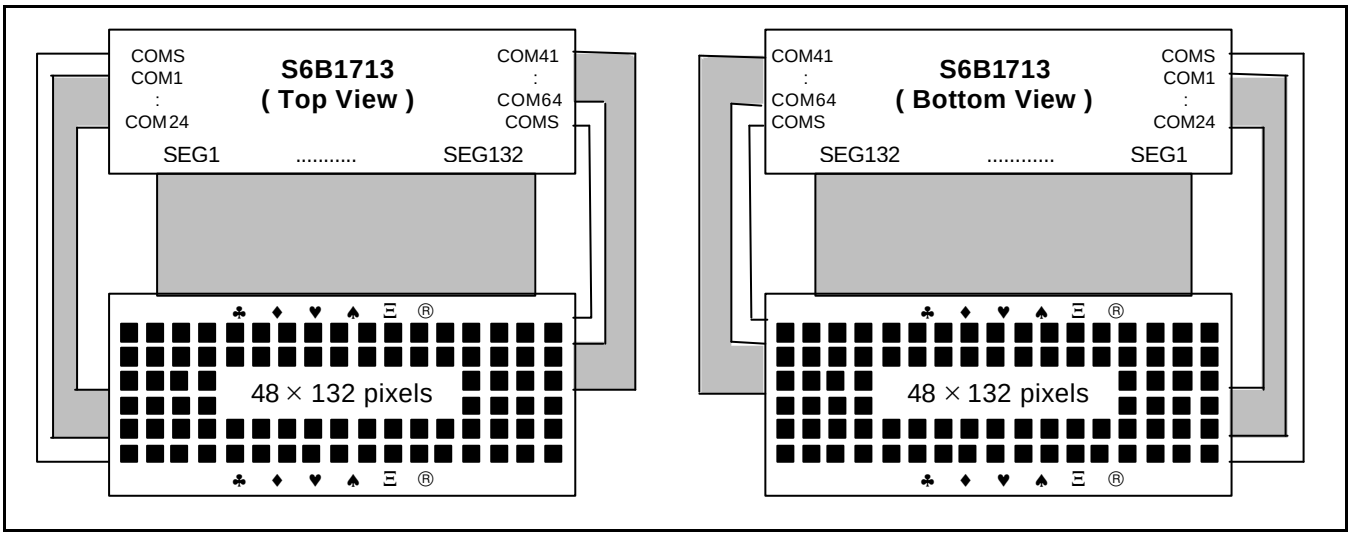


Figure 52. SHL = 1, ADC = 0

Figure 53. SHL = 1, ADC = 1

Single Chip Configuration (1/33 Duty Configurations)

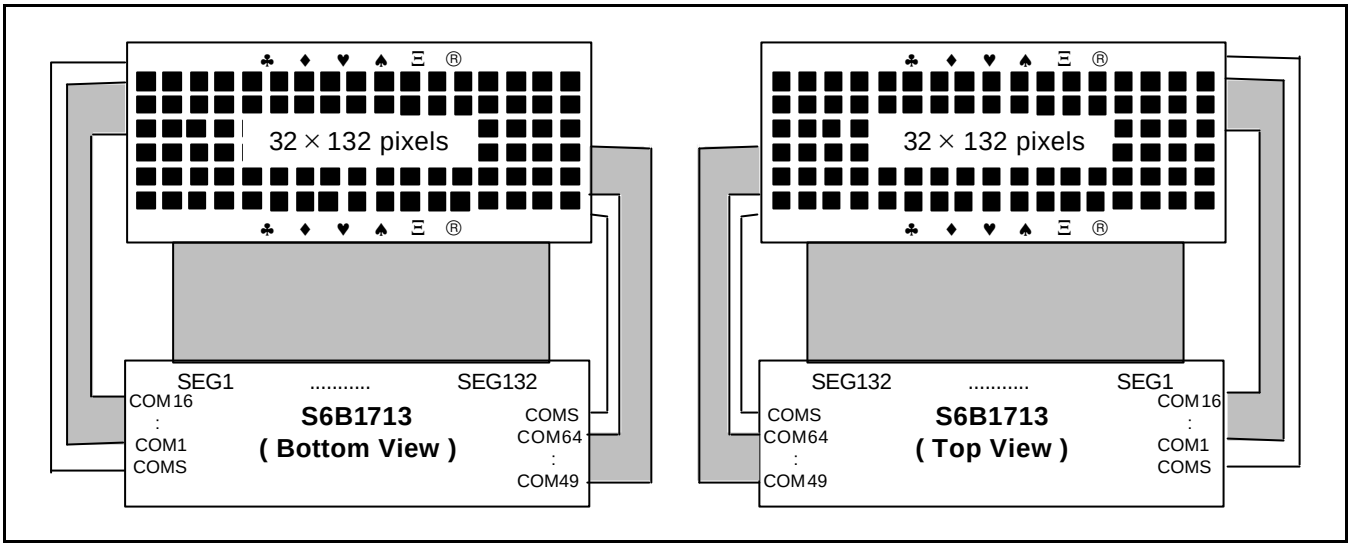


Figure 54. SHL = 0, ADC = 0

Figure 55. SHL = 0, ADC = 1

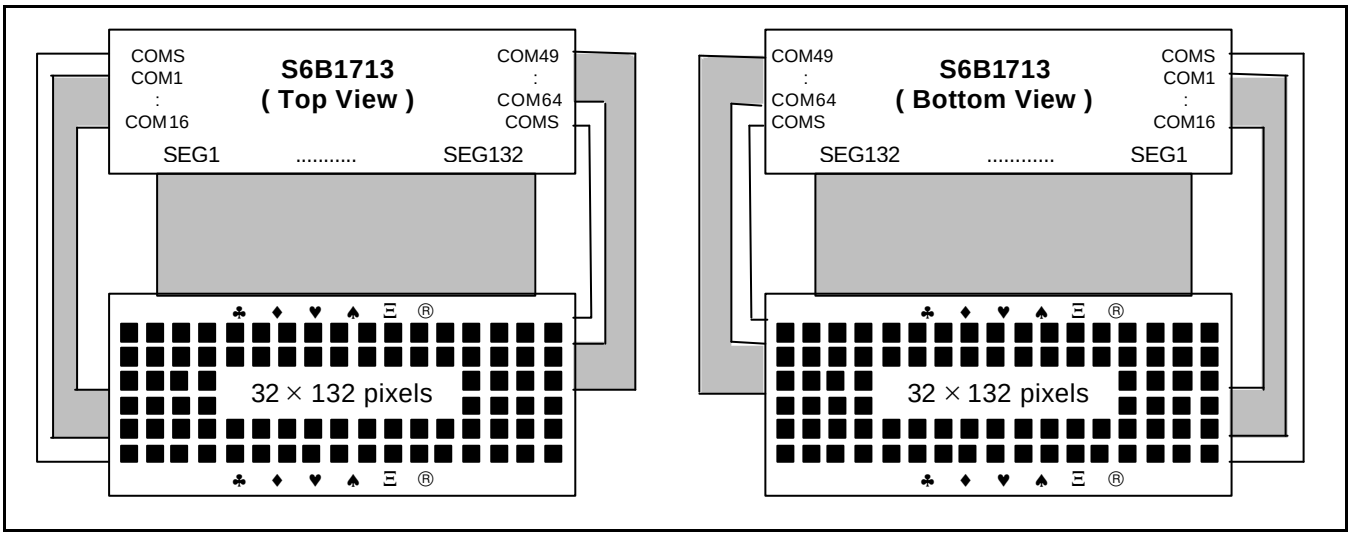


Figure 56. SHL = 1, ADC = 0

Figure 57. SHL = 1, ADC = 1

Multiple Chip Configuration

- **65COM (64COM + 1COMS) ´ 264SEG (132SEG ´ 2)**

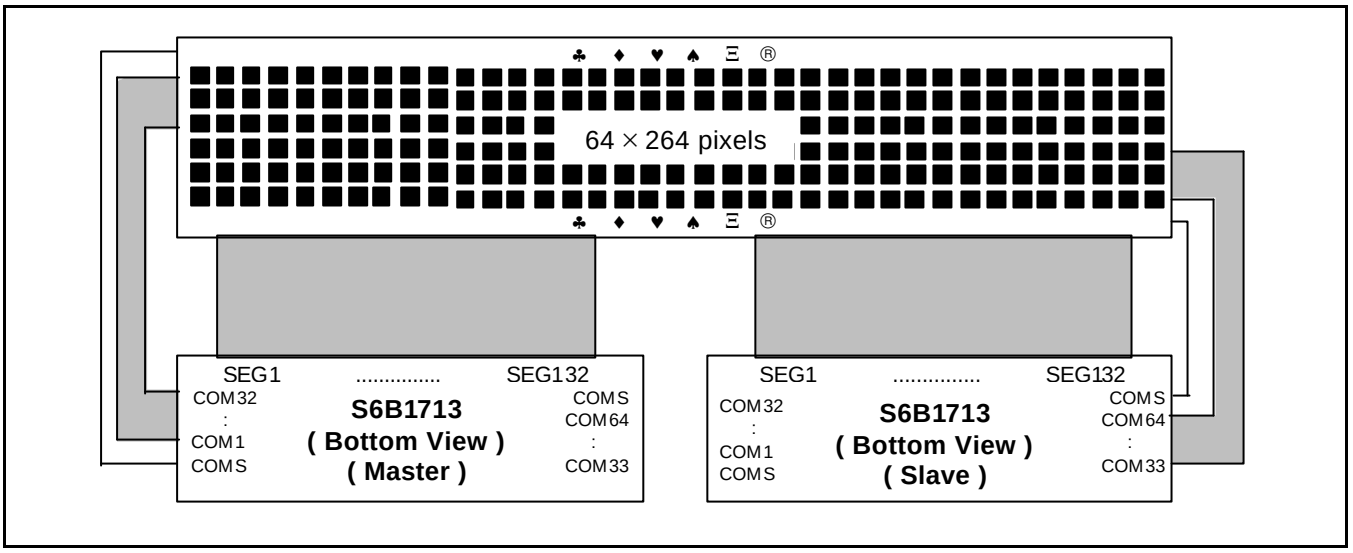


Figure 58. SHL = 0, ADC = 0

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

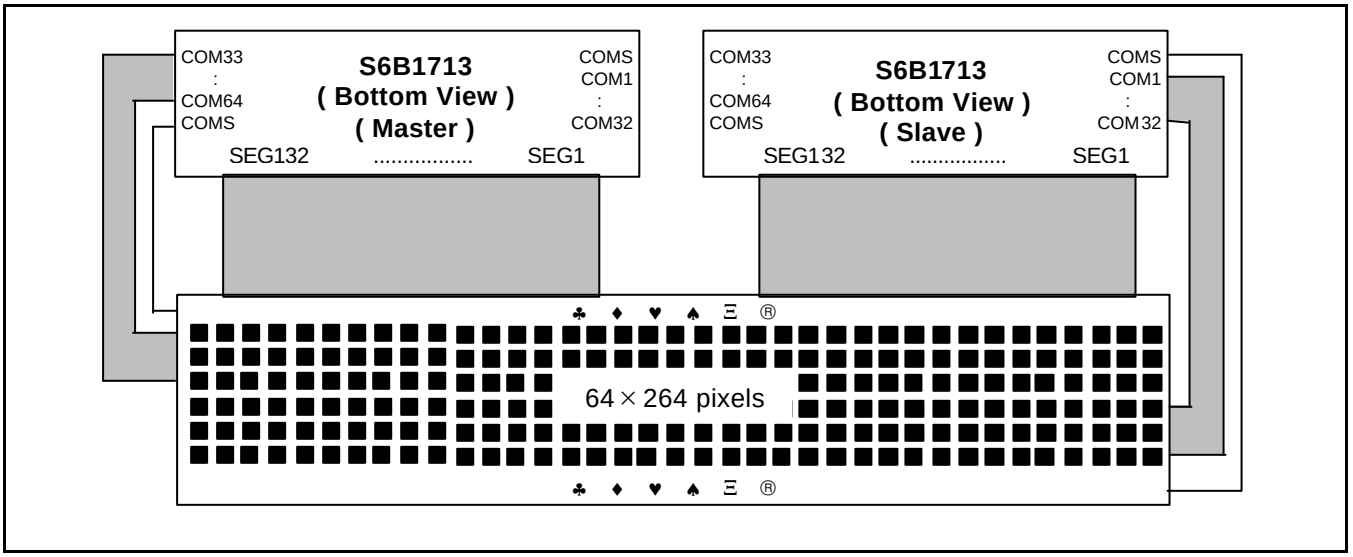


Figure 59. SHL = 1, ADC = 1

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- **130COM (128COM + 2COMS) ´ 132SEG**

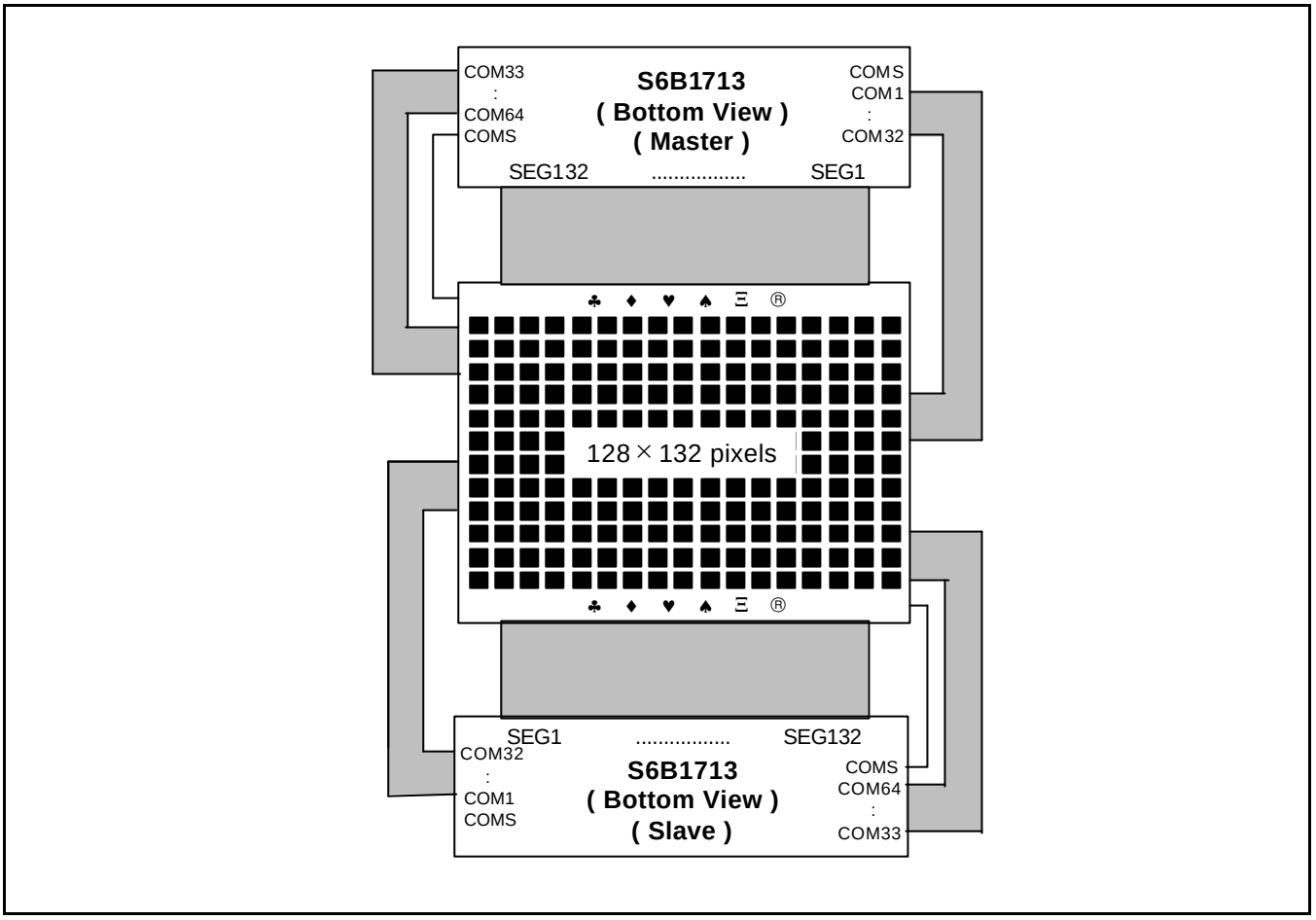


Figure 60. 130COM (128COM + 2COMS) ´ 132SEG

- Connect the following pins of two chips each other
  - Display clock pins: CL, M
  - Display control pin: DISP
  - LCD power pins: V0, V1, V2, V3, V4

- Common / Segment output direction select
  - Master chip: SHL = 1, ADC = 1
  - Slave chip: SHL = 0, ADC = 0

TCP PIN LAYOUT (SAMPLE)

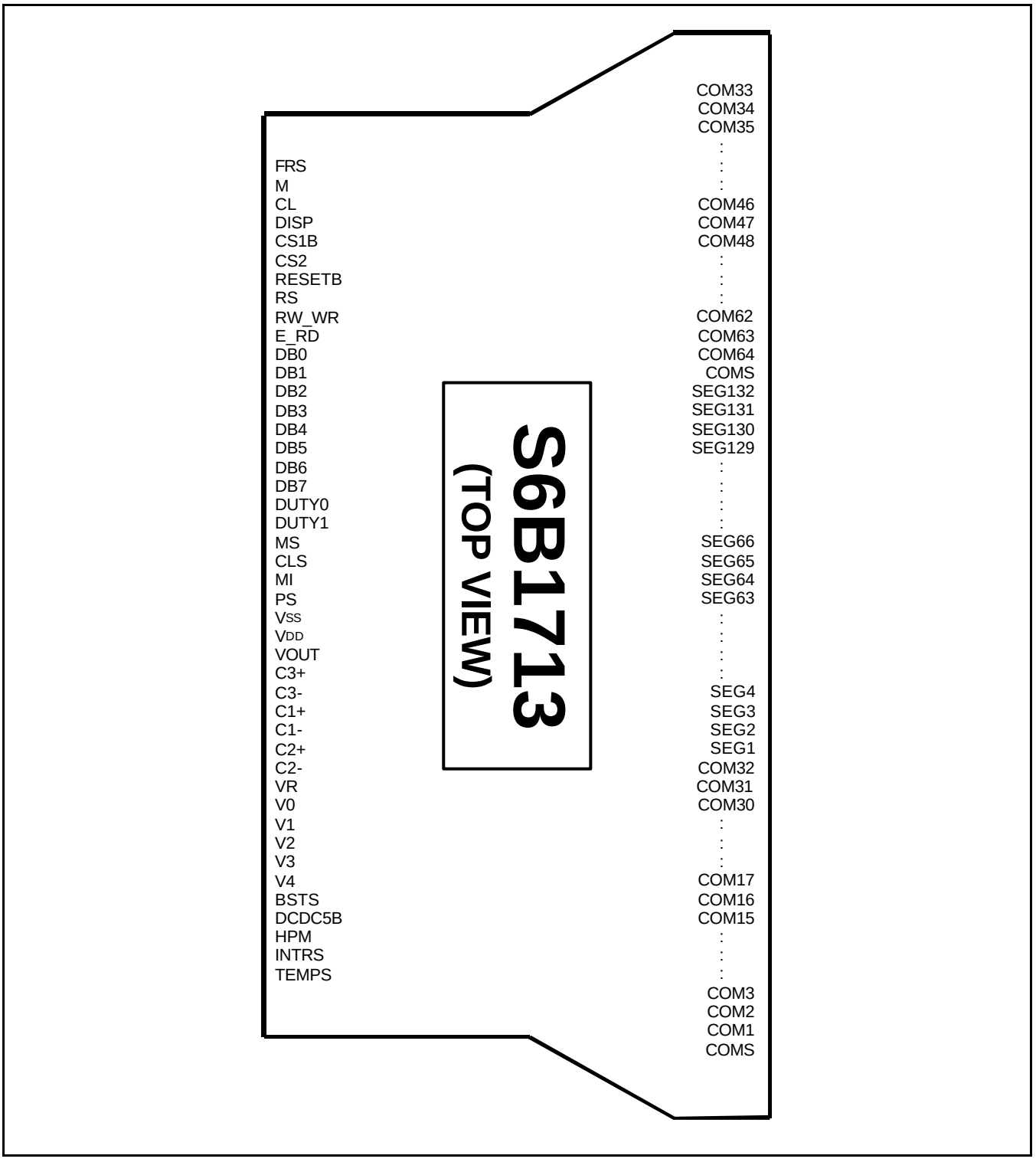


Figure 61. TCP Pin Layout