CMOS LSI

No. 4475A

LC7942ND

Dot-matrix LCD Driver

Overview

The LC7942ND is a common driver LSI for driving large, dot-matrix LCD displays. It features a built-in 64-bit bidirectional shift register and a 4-level LCD driver. It can also be connected in cascade to increase the number of bits.

The LC7942ND is designed to be used with LC7940ND (QFP100) or LC7941ND (QFP100) segment drivers to drive large LCD panels.

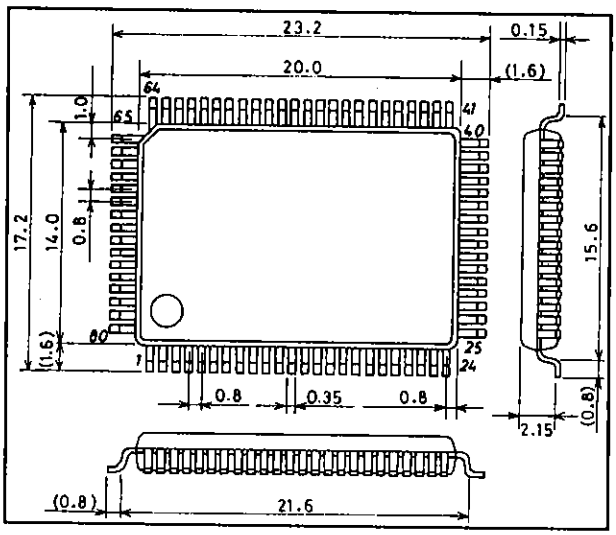
Features

- 64 built-in LCD display drive circuits
- 1/64 to 1/128 display duty cycle
- Input/outputs for cascade connection
- Bias supply voltages can be supplied externally
- Operating supply voltage and ambient temperature
  - 5 V ±10% logic supply (V_{DD}) at T_a = −20 to +85 °C
  - 8 to 20 V LCD supply (V_{DD} − V_{EE}) at T_a = −20 to +85 °C
- CMOS process
- 80-pin flat plastic package

Package Dimensions

Unit: mm

3177-QFP80D



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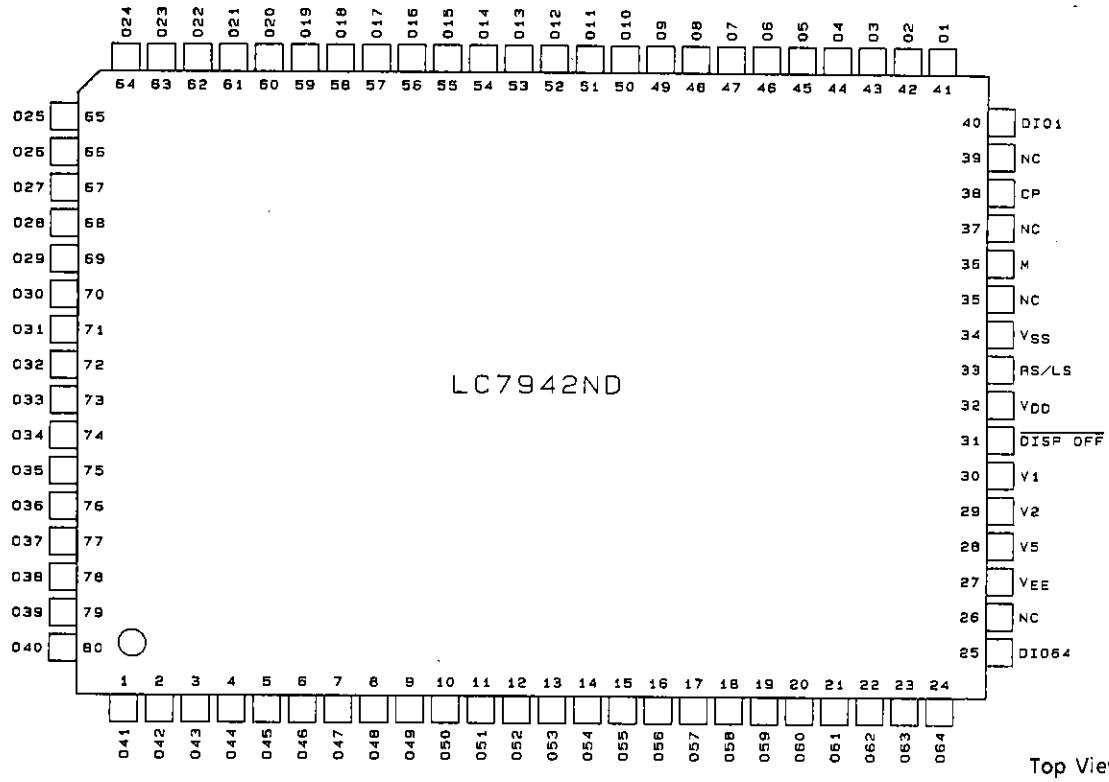
Pin Assignment



Top View

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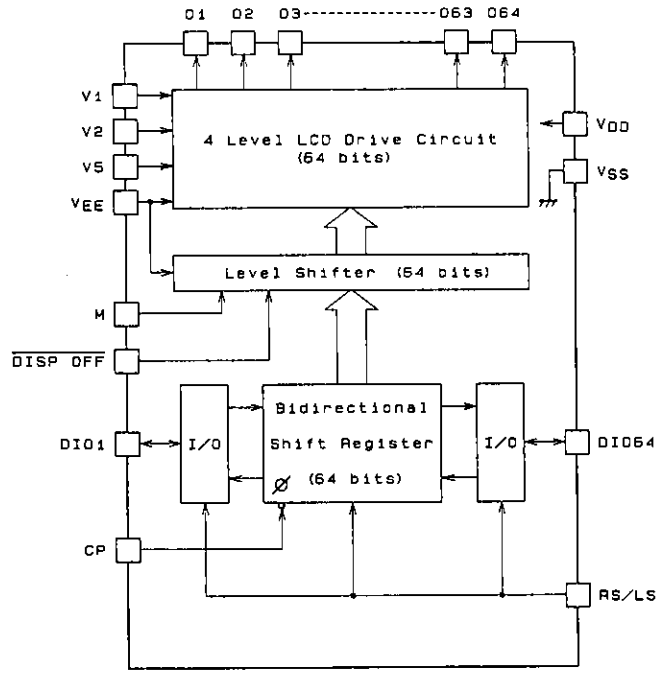
Block Diagram



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Pin Functions

<table>
<tr><th>Number</th><th>Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>32</td><td>VDD</td><td rowspan="3">Supply</td><td rowspan="3">V_{DD} – V_{SS} is the logic supply.
V_{DD} – V_{EE} is the LCD supply.</td></tr>
<tr><td>34</td><td>VSS</td></tr>
<tr><td>27</td><td>VEE</td></tr>
<tr><td>30</td><td>V1</td><td rowspan="3">Supply</td><td rowspan="3">LCD panel drive voltage supplies.
V_1 and V_{EE} are selected levels.
V_2 and V_5 are not-selected levels.</td></tr>
<tr><td>29</td><td>V2</td></tr>
<tr><td>28</td><td>V5</td></tr>
<tr><td>38</td><td>CP</td><td>I</td><td>Display data input clock (falling-edge trigger).</td></tr>
<tr><td>40</td><td>DIO1</td><td>I/O</td><td rowspan="3"><table><tr><th>RS/LS</th><th>DIO1</th><th>DIO64</th><th>Shift direction</th></tr><tr><td>LOW (right shift)</td><td>Input</td><td>Output</td><td>O1 → O64</td></tr><tr><td>HIGH (left shift)</td><td>Output</td><td>Input</td><td>O64 → O1</td></tr></table></td></tr>
<tr><td>25</td><td>DIO64</td><td>I/O</td></tr>
<tr><td>33</td><td>RS/LS</td><td>I</td></tr>
<tr><td>36</td><td>M</td><td>I</td><td>LCD panel drive voltage output alternation control signal.</td></tr>
<tr><td>31</td><td>$\overline{\text{DISP OFF}}$</td><td>I</td><td>O1 to O64 output control input pins.</td></tr>
<tr><td>41 to 80</td><td>O1 to O40</td><td rowspan="2">O</td><td rowspan="2">LCD drive outputs.
The output drive level is determined by the display data, M signal and $\overline{\text{DISP OFF}}$ input as shown below.<table><tr><th>M</th><th>Q</th><th>$\overline{\text{DISP OFF}}$</th><th>Output</th></tr><tr><td>LOW</td><td>LOW</td><td>HIGH</td><td>V_2</td></tr><tr><td>LOW</td><td>HIGH</td><td>HIGH</td><td>V_{EE}</td></tr><tr><td>HIGH</td><td>LOW</td><td>HIGH</td><td>V_5</td></tr><tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>V_1</td></tr><tr><td>×</td><td>×</td><td>LOW</td><td>V_1</td></tr></table>Note
× = don't care (tied HIGH or LOW)</td></tr>
<tr><td>1 to 24</td><td>O41 to O64</td></tr>
<tr><td>26</td><td>NC</td><td rowspan="4">–</td><td rowspan="4">No connection.</td></tr>
<tr><td>35</td><td>NC</td></tr>
<tr><td>37</td><td>NC</td></tr>
<tr><td>39</td><td>NC</td></tr>
</table>

Specifications

Absolute Maximum Ratings

T_a = 25 ±2 °C, V_{SS} = 0 V

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD} max	–0.3 to +7.0	V
LCD supply voltage. See note.	V_{DD} – V_{EE} max	0 to 22	V
Input voltage	V_I max	–0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	–20 to +85	°C
Storage temperature range	T_{stg}	–40 to +125	°C

Note

$V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$

Allowable Operating Ranges

T_a = −20 to +85 °C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Logic supply voltage	V_{DD}		4.5	–	5.5	V
LCD supply voltage	$V_{DD} - V_{EE}$	See notes 1 and 2.	8	–	20	V
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ HIGH-level input voltage	V_{IH}		0.8V_{DD}	–	–	V
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ LOW-level input voltage	V_{IL}		–	–	0.2V_{DD}	V
CP shift clock frequency	f_{CP}		–	–	1	MHz
CP pulsewidth	t_{WC}		125	–	–	ns
DIO1 and DIO64 to CP setup time	t_{SETUP}		100	–	–	ns
DIO1 and DIO64 to CP hold time	t_{HOLD}		100	–	–	ns
CP rise time	t_R		–	–	50	ns
CP fall time	t_F		–	–	50	ns

Notes

1. $V_{DD} \geq V_1 > V_2 > V_5 > V_{EE}$
2. At turn ON, the LCD supply should be energized after or simultaneously with the logic supply. At turn OFF, the logic supply should be cut after or simultaneously with the LCD supply.

Electrical Characteristics

T_a = 25 ±2 °C, V_{SS} = 0 V, V_{DD} = 5 V ±10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ HIGH-level input current	I_{IH}	$V_{IN} = V_{DD}$	–	–	1	μA
DIO1, DIO64, CP, M, RS/LS and $\overline{\text{DISPOFF}}$ LOW-level input current	I_{IL}	$V_{IN} = V_{SS}$	−1	–	–	μA
DIO1 and DIO64 HIGH-level output voltage	V_{OH}	I_{OH} = −400 μA	V_{DD} − 0.4	–	–	V
DIO1 and DIO64 LOW-level output voltage	V_{OL}	I_{OL} = 400 μA	–	–	0.4	V
O1 to O64 driver ON resistance	R_{ON}	$V_{DD} - V_{EE}$ = 18 V, $\lvert V_{DE} - V_O \rvert$ = 0.25 V, V_{DD} = 4.5 V	–	–	1.5	kΩ
VDD static supply current	I_{DD}	$V_{DD} - V_{EE}$ = 18 V, CP = V_{DD}	–	–	100	μA
CP input capacitance	C_I	f_{CP} = 1 MHz	–	5	–	pF

Note

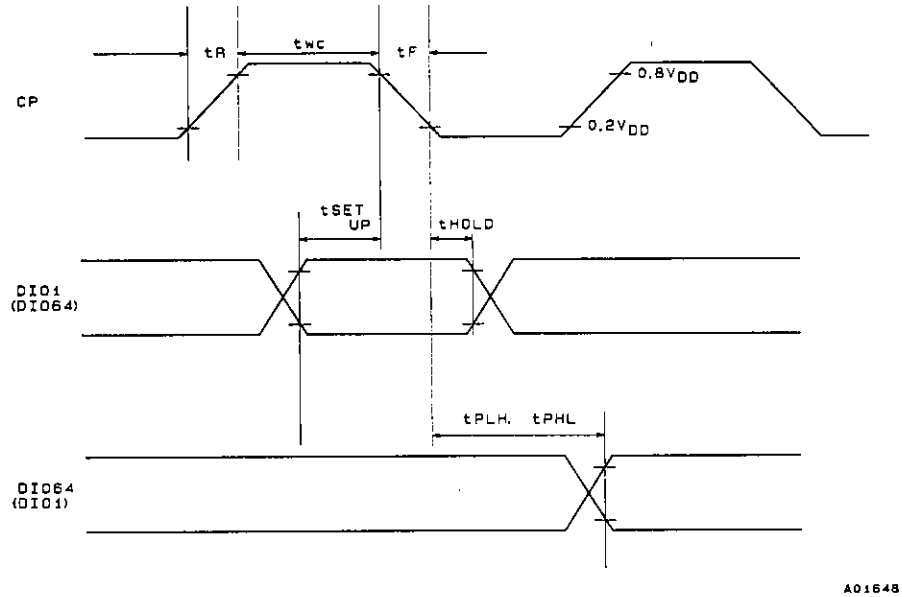
V_{DE} = V_1 or V_2 or V_5 or V_{EE}, $V_1 = V_{DD}$, $V_2 = 10/11 \times (V_{DD} - V_{EE})$, $V_5 = 1/11 \times (V_{DD} - V_{EE})$

Switching Characteristics

T_a = 25 ±2 °C, V_{SS} = 0 V, V_{DD} = 5 V ±10%

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output delay time	t_{PLH}	C_L = 30 pF	–	–	250	ns
	t_{PHL}		–	–	250	

Switching Characteristics Waveform



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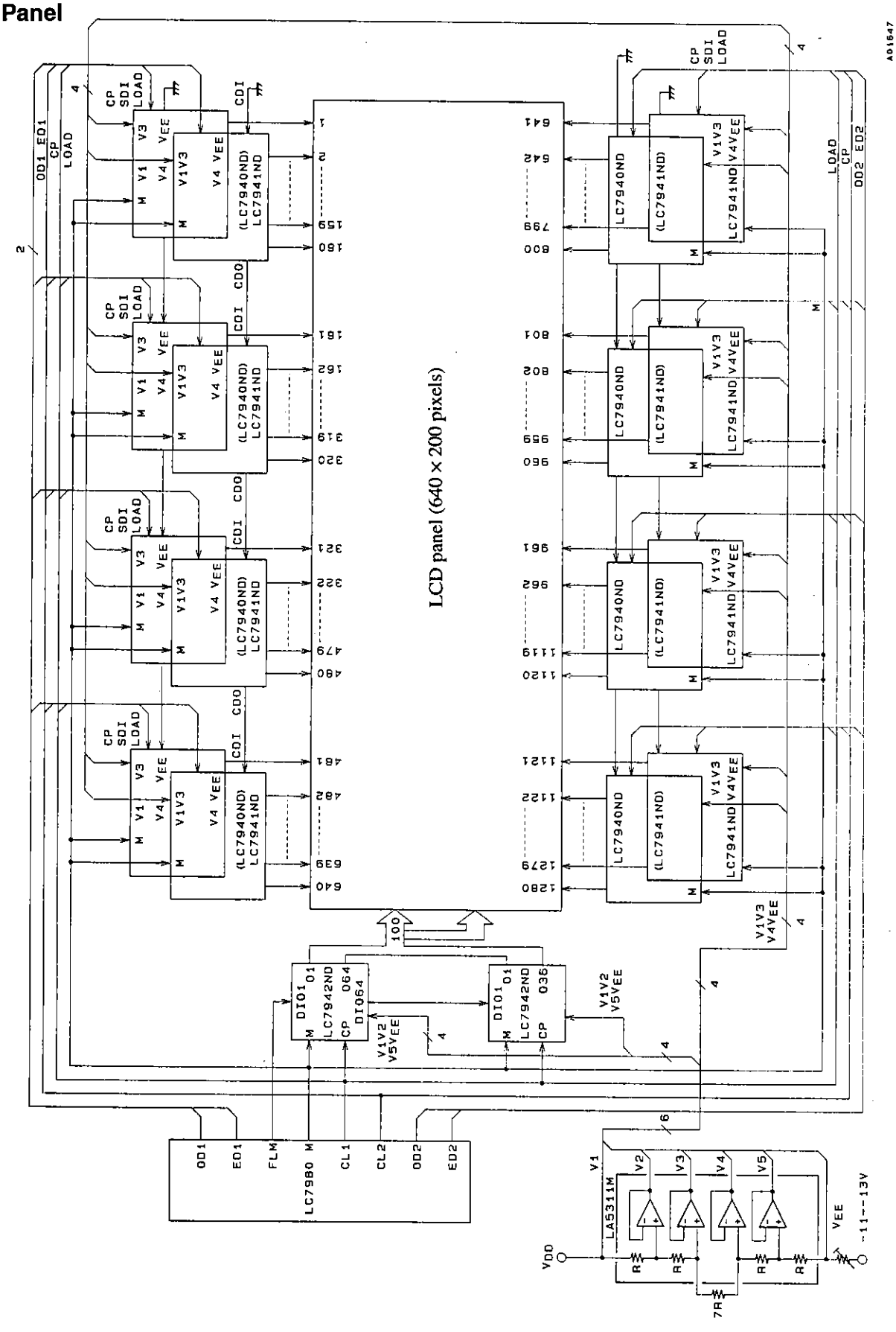
LCD Panel


LCD panel (640 × 200 pixels)
LC7940ND
(LC7941ND)
LC7941ND
(LC7940ND)
LC7941ND
LC7942ND
LC7980
LA5311M
CP
SDI
LOAD
CDI
CDO
OD1
ED1
FLM
CL1
CL2
OD2
ED2
V1
V2
V3
V4
V5
VEE
VDD
R
7R
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