Ordering number : EN5946

SANYO Semiconductors
DATA SHEET

LC7982A — CMOS IC
LCD Dot Matrix Graphics Display Controller

Overview

The LC7982A is an LCD dot matrix graphics display controller IC. It stores display data sent from an 8-bit microcontroller in external display RAM and generates dot matrix LCD drive signals. Applications can select either of two modes: graphics mode, in which each bit in external RAM controls the on/off state of an individual pixel (dot) on the LCD, and character mode, in which character codes are stored in external RAM and the dot pattern is generated using the built-in character generator ROM. Thus the LC7982A can support a wide range of applications. The LC7982A is fabricated in a CMOS process, and in conjunction with a CMOS microcontroller, can implement low-power LCD display systems. This device differs from the LC7981 only in the data stored in the built-in character generator ROM.

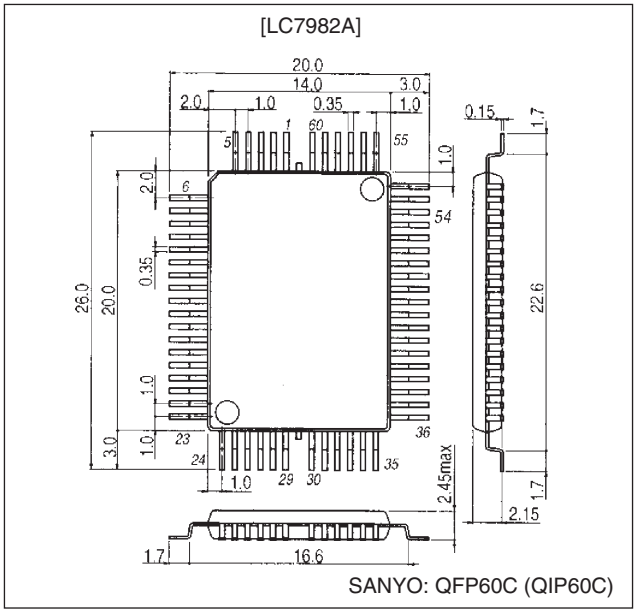
Features

- LCD dot matrix and graphics display controller
- Display control capacity
  - Graphics mode: 512 K dots (2^{16} bytes)
  - Character mode: 4096 characters (2^{12} bytes)
- Character generator ROM: 7360 bits
  - · European character support
    - Character font: 5 × 7 dots: 160 characters
    - Character font: 5 × 11 dots: 32 characters
    - (192 characters total)
    - (Can be expanded by up to 4 KB using external ROM.)
- Supports interfacing with 8-bit microcontrollers.
- Display duty (program selectable)
  - — From static to 1/256 duty
- Extensive set of command functions
  - — Scroll, cursor on/off/blink, character blinking, bit manipulation
- Display methods : Method A and method B (program selectable)
- Built-in oscillator circuit (Using an external resistor and capacitor)
- Low power
- +5V single-voltage power supply

Package Dimensions

unit: mm

3055A-QFP60C



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Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_I		–0.3 to V_{DD} +0.3	V
Output voltage	V_O		–0.3 to V_{DD} +0.3	V
Allowable power dissipation	Pd max	Ta = 75°C	200	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

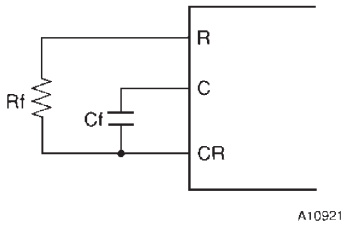
Allowable Operating Ranges at Ta = –20 to +75°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.75		5.25	V
High-level input voltage	$V_{IH}1$	Input and I/O pins other than $\overline{SYNC}$ and CR.	2.2		V_{DD}	V
Low-level input voltage	$V_{IL}1$	Input and I/O pins other than $\overline{SYNC}$ and CR.	0		0.8	V
High-level input voltage	$V_{IH}2$	$\overline{SYNC}$, CR	0.7 V_{DD}		V_{DD}	V
Low-level input voltage	$V_{IL}2$	$\overline{SYNC}$, CR	0		0.3 V_{DD}	V
High-level output voltage	$V_{OH}1$	I_{OH} = –0.6 mA, DB0 to DB7, $\overline{WE}$, MA0 to MA15, MD0 to MD7	2.4		V_{DD}	V
Low-level output voltage	$V_{OL}1$	I_{OL} = 1.6 mA, DB0 to DB7, $\overline{WE}$, MA0 to MA15, MD0 to MD7	0		0.4	V
High-level output voltage	$V_{OH}2$	I_{OH} = –0.6 mA, $\overline{SYNC}$, CPO, FLM, CL1, CL2, D1, D2, MA, MB	V_{DD} – 0.4		V_{DD}	V
Low-level output voltage	$V_{OL}2$	I_{OL} = 0.6 mA, $\overline{SYNC}$, CPO, FLM, CL1, CL2, D1, D2, MA, MB	0		0.4	V
[Internal Clock Operation]						
Clock oscillator frequency	f_{OSC}	Cf = 15 pF ±5%, Rf = 39 kΩ ±2%*1	500	600	700	kHz
[External Clock Operation]						
Clock operating frequency	f_{CP}	*2			2.5	MHz
Clock duty	Duty	*3	47.5	50	52.5	%
Clock rise time	trcp	*3			50	ns
Clock fall time	tfcp	*3			50	ns

Electrical Characteristics at Ta = –20 to +75°C, GND = 0 V, V_{DD} = 5 V ±5%

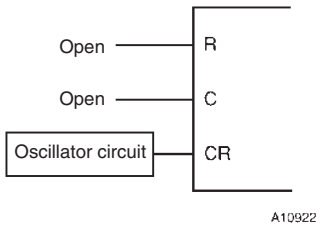
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input leakage current	I_{IN}	V_{IN} = 0 to V_{DD}, $\overline{CS}$, E, RS, R/W, $\overline{RES}$	–5		5	µA
Current drain	$I_{CC}1$	RC oscillator, f_{OSC} = 600 kHz		2	4	mA
	$I_{CC}2$	External clock, f_{CP} = 2.5 MHz		3	5	mA
Pull-up current	I_{PL}	V_{IN} = GND, DB0 to DB7, RD0 to RD7, MD0 to MD7		10	20	µA

(Note 1)

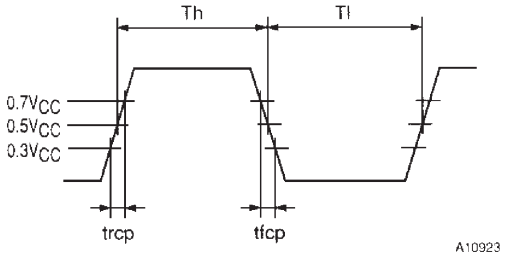


Cf = 15 pF ±5%
Rf = 39 kΩ ±2%
(When f_{OSC} = 600 kHz (typical))

(Note 2)



(Note 3)

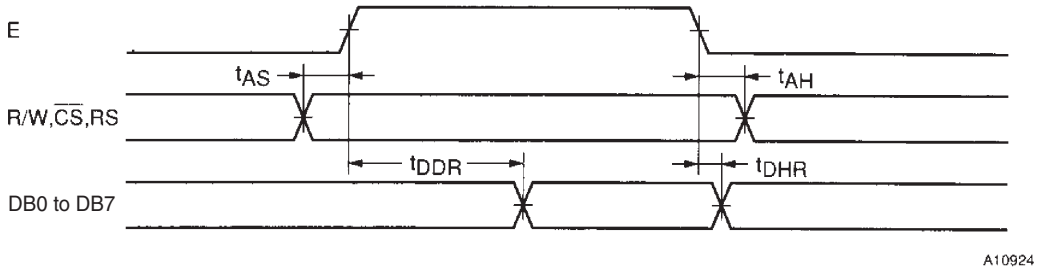


$$\text{Duty} = \frac{Th}{Th + T1} \times 100\%$$

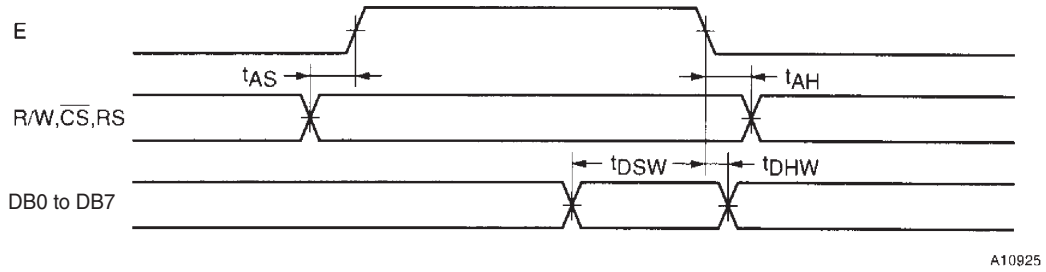
Timing Characteristics

- Bus read/write operation 1

Read cycle



Write cycle



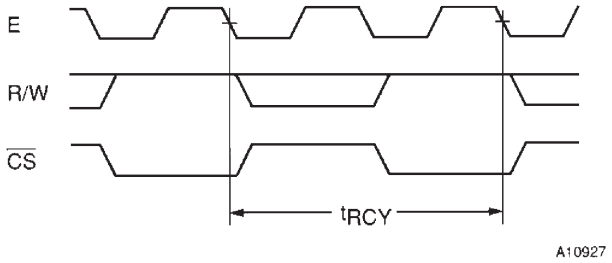
Ta = –20 to +75°C, V_{DD} = 5V ±5%, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Address setup time	t_{AS}		90			ns
Address hold time	t_{AH}		10			ns
Data delay time (read)	t_{DDR}	C_L = 50 pF			140	ns
Data hold time (read)	t_{DHR}		10			ns
Data setup time (write)	t_{DSW}		220			ns
Data hold time (write)	t_{DHW}		20			ns

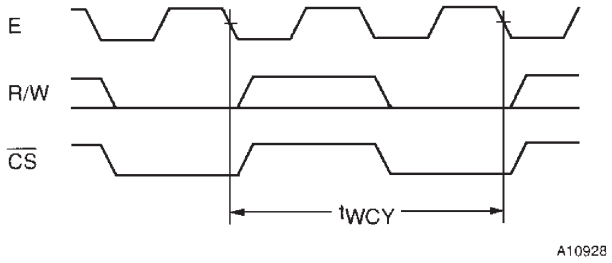
Note: Test waveform definition

Input pins are driven to 2.4 V and 0.45 V, and the timing is measured at 1.5 V

• Bus read/write operation 2
Data read cycle



Data write cycle

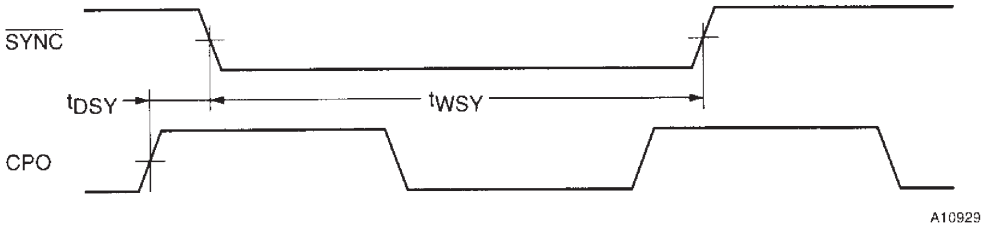


Ta = –20 to +75°C, V_{DD} = 5V ±5%, GND = 0 V

Parameter	Symbol	Instruction register value	Ratings			Unit
			min	typ	max	
Read cycle time	t_{RCY}	0DH			$\frac{(HP+2) \times 10^3}{f_{OSC}}$ +200	ns
Write cycle time	$t_{WCY}1$	0EH, 0FH			$\frac{(2HP+2) \times 10^3}{f_{OSC}}$ +200	ns
Write cycle time	$t_{WCY}2$	0CH			$\frac{(HP+2) \times 10^3}{f_{OSC}}$ +200	ns
Write cycle time	$t_{WCY}3$	00H, 01H, 02H, 03H, 04H, 08H, 09H, 0AH, 0BH			$\frac{2000}{f_{OSC}}$ +200	ns

Notes: • For character display, HP is the number of dots in the horizontal direction per character, and for graphics mode, HP is the number of bits shown on the display from each byte of display data.
• f_{OSC} is the oscillator frequency, in units of MHz.
• All measurements are made at 1.5 V.

• Parallel operation (master mode)

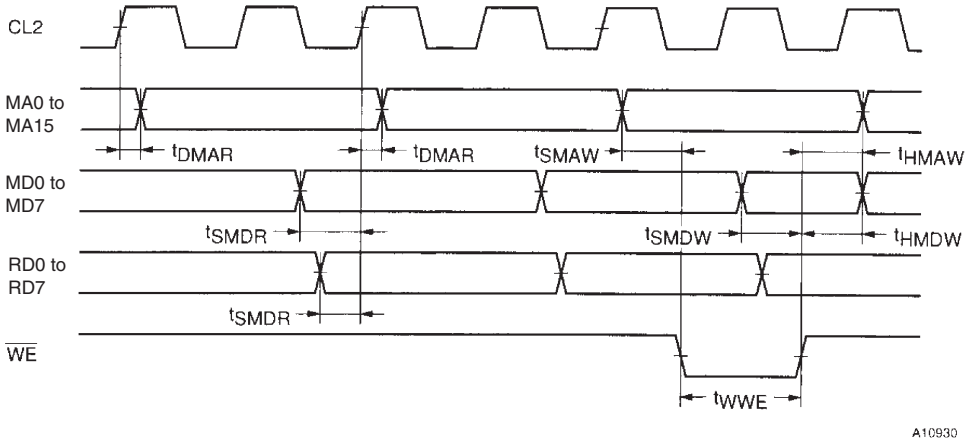


Ta = –20 to +75°C, V_{DD} = 5V ±5%, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
$\overline{SYNC}$ delay time	t_{DSY}				100	ns
$\overline{SYNC}$ pulse width	t_{WSY}		350			ns

Notes: • With no loads on any of the output pins.
• Measurements are made at 0.5 V_{DD}.

• External RAM and ROM interface



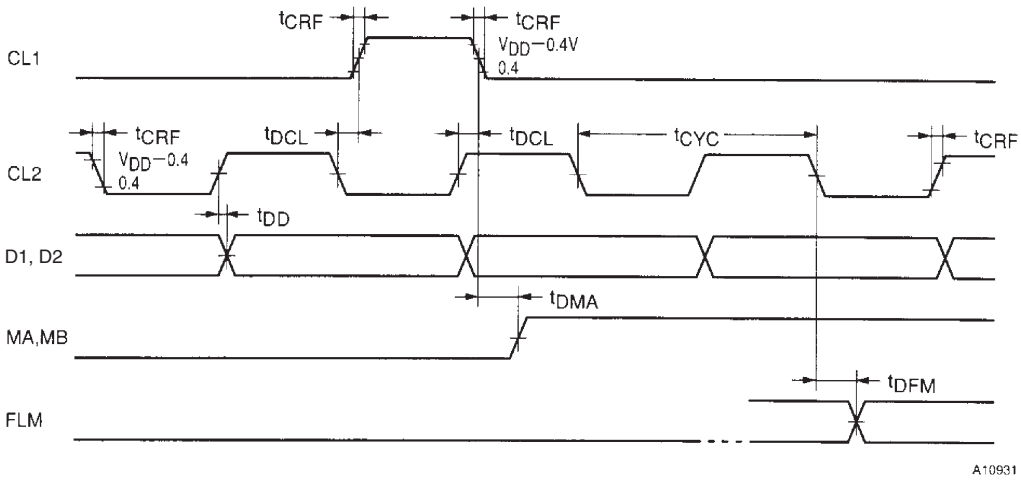
Read Cycle at Ta = –20 to +75°C, V_{DD} = 5 V ±5%, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
MA0 to MA15 read address delay time	t_{DMAR}				95	ns
MD0 to MD7, RD0 to RD7 setup time	t_{SMDR}		105			ns

Write Cycle at Ta = –20 to +75°C, V_{DD} = 5 V ±5%, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Memory address setup time	t_{SMAW}		50			ns
WE pulse width	t_{WWE}		350			ns
Memory data setup time	t_{SMDW}		250			ns
Memory address hold time	t_{HMAW}		50			ns
Memory data hold time	t_{HMDW}		50			ns

Notes: • With no loads on any of the output pins.
• All measurements are made at 1.5 V.



• Driver IC interface

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock cycle time	t_{CYC}		400			ns
Clock phase difference	t_{DCL}				100	ns
Clock rise and fall times	t_{CRF}				30	ns
D1 and D2 phase difference	t_{DD}				100	ns
MA and MB phase difference	t_{DMA}				200	ns
FLM phase difference	t_{DFM}				200	ns

Ta = –20 to +75°C, V_{DD} = 5 V ±5%, GND = 0 V