1. FEATURES

- 8-Bit Static Pipeline CPU
- ROM: 16K x 8 bits PROM(OTP)
- RAM: 192 x 8 bits
- 32-Level Deep Stack
- Operating Voltage : 2.4V ~ 5.5V
- Power-on Timer(PWRT)
  - Pin option to enable
- General-Purpose I/O (GPIO) Ports
  - 28 pins are programmable CMOS I/O (Port-A/B/C and Port-E low nibble), 20 pins (Port-A high nibble & Port-B/C) are shared with LCD Segments
  - 8 open drain output pins share with LCD COMs
  - Hardware de-bounce option for Port-A
  - Bit programmable pull-up for input pins
- 2 Input Pins
  - OTP option bit to select (shared with OSCX)
- 30 Output Pins
  - Eight are shared with LCD com and twenty are shared with LCD Segments, two are shared with PSG
- Timer / Counter
  - One 8-bit timer / 16-bit event counter
  - One 8-bit BASE timer
- Five Powerful Interrupt Sources
  - External interrupt (edge trigger) / RFC interrupt(Share with external interrupt)
  - TIMER1 interrupt
  - BASE timer interrupt
  - PORTA[7~0] interrupt (transition trigger)
  - DAC reload interrupt
- Watchdog Timer (WDT)
  - With its own low power internal oscillator for reliability
  - Four selectable time bases
  - WDT reset CPU only
  - OTP option bit to enable
- One option bit is selectable to reset or not in WAI1 and STP mode
- Dual Clock Source with Warm-up Timer
  - OSCX: Low frequency crystal oscillator with 32768Hz
  - OSC: High frequency RC oscillator from 500K ~ 8MHz
  - CPU clock 250K ~ 4MHz
- On-chip Internal Oscillator for WDT
  - < 5μA typical, 3V, 27°C
- LCD Controller Driver
  - 16 level contrast control
  - 320 (8x40) dots (1/8 duty, 1/4 bias, programmable)
  - 160 (4x40) dots (1/4 duty, 1/3 bias, programmable)
  - Two clock source options: RC and resonator oscillator
  - Keyboard scan function supported on 40 shared segment drives
  - Internal bias resistors(1/4 bias & 1/3 bias) with 32 level driving strength control
- Programmable Sound Generator (PSG)
  - Tone generator
  - Sound effect generator
  - 16 level volume control
  - Digital DAC for speech / tone
- Resistor Frequency Converter (RFC)
  - Up to 4 resistors measurement
  - Built-in one independent 16-bits counter without sharing with timer counter
  - 3 clock sources for RFC counter: SYSCCLK, OSCX and INTX
  - 5 scales of clock divider for RFC counter
- Carrier Wave Generator(CGR)
  - Built-in one digital PLL
  - Standard clock rate output for remote control
- Three Power Down Modes
  - WAI0 mode
  - WAI1 mode
  - STP mode
2. GENERAL DESCRIPTION

ST20P18 is a low-cost, high-performance, fully static, 8-bit microcontroller designed with CMOS silicon gate technology. It comes with 8-bit pipeline CPU core, SRAM, timer, LCD driver, I/O port, PSG, RFC, CGR, OTP program ROM and built-in dual oscillator. And also, some new functions have been added in the ST20P18 to enhance the performance of ST2016 for more system application.

Power bouncing during power-on is a major problem when designing a reliable system. After the power returns to normal level, the system may recover its original states and keeps working correctly. Furthermore, the Power-on Timer (PWRT) which is designed to provide a fixed delay time, keep the part in reset for longer after power-up or low-V reset released. With these two power management, the system may operate under more stable power supply.

A highly reliable Watchdog Timer(WDT) with its own low power internal oscillator which does not require any external components, provides protection against software lockup. Moreover, the feature of “WDT reset CPU only” make it possible to do the rapid system recovery after Watchdog timer reset. And the option bit is selectable to reset or not in WAI1 and STP mode for various application.

The Resistor Frequency Converter(RFC) which is also a new function added in the ST20P18, can compare three different sensors with the reference resistor separately. With one independent 16-bits counter, the RFC can count and stop automatically only if RFC is enabled. This make it easy for the humidity or thermometric application.

More and more remote control applications are used today. The ST20P18 also equips a Carrier Wave Generator(CGR) to support this application with one digital PLL and provide the standard clock rates output for remote control.

With these integrated functions inside, the ST20P18 single chip microcontroller is a right solution for business equipment and consumer applications. Such as watch, calculator, LCD games, thermometer, hygrometer, IR remote control and so on. ST20P18 is definitely a perfect solution for implementation.
3. BLOCK DIAGRAM
4. PAD DIAGRAM

ST20P18
## 5. PAD DESCRIPTION

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Designation</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12~9</td>
<td>SEG0/PA4 ~ SEG3/PA7</td>
<td>O  I/O</td>
<td>LCD Segment output Port-A bit programmable I/O</td>
</tr>
<tr>
<td>8~5</td>
<td>SEG4- SEG7</td>
<td>O</td>
<td>LCD Segment output Segment output port</td>
</tr>
<tr>
<td>4<del>1, 68</del>65</td>
<td>SEG8~SEG15</td>
<td>O</td>
<td>LCD Segment output Segment output port</td>
</tr>
<tr>
<td>64~57</td>
<td>SEG16-SEG23</td>
<td>O</td>
<td>LCD Segment output Segment output port</td>
</tr>
<tr>
<td>56~49</td>
<td>SEG24/PC0 ~ SEG31/PC7</td>
<td>O  I/O</td>
<td>LCD Segment output Port-C bit programmable I/O</td>
</tr>
<tr>
<td>48~41</td>
<td>SEG32/PB0 ~ SEG39/PB7</td>
<td>O  I/O</td>
<td>LCD Segment output Port-B bit programmable I/O</td>
</tr>
<tr>
<td>39~32</td>
<td>COM 0 ~ 7</td>
<td>O</td>
<td>LCD Common output Open drain output port</td>
</tr>
<tr>
<td>24</td>
<td>RESET</td>
<td>I</td>
<td>Pad reset input (HIGH Active)</td>
</tr>
<tr>
<td>29</td>
<td>GND</td>
<td>P</td>
<td>Ground Input and chip substrate</td>
</tr>
<tr>
<td>16</td>
<td>PA0/INTX</td>
<td>I/O I</td>
<td>Port-A bit programmable I/O Edge-trigger Interrupt. Transition-trigger Interrupt Programmable Timer1 clock source</td>
</tr>
<tr>
<td>15~9</td>
<td>PA 1-7</td>
<td>I/O I</td>
<td>Port-A bit programmable I/O Transition-trigger Interrupt</td>
</tr>
<tr>
<td>28~27</td>
<td>PSGO,PSGOB</td>
<td>O</td>
<td>PSG/DAC Output</td>
</tr>
<tr>
<td>26</td>
<td>VDD</td>
<td>P</td>
<td>Power supply</td>
</tr>
<tr>
<td>22</td>
<td>OSCXI/PD0</td>
<td>I</td>
<td>OSC input pin. For 32768Hz crystal Port-D input</td>
</tr>
<tr>
<td>21</td>
<td>OSCXO/PD1</td>
<td>O  I</td>
<td>OSC output pin. For 32768Hz crystal Port-D input</td>
</tr>
<tr>
<td>25</td>
<td>OSCI</td>
<td>I</td>
<td>OSC input pin. Toward to external resistor</td>
</tr>
<tr>
<td>20~17</td>
<td>PE0~PE3</td>
<td>I/O</td>
<td>Port-E bit programmable I/O RFC/CGR output</td>
</tr>
<tr>
<td>31</td>
<td>V2</td>
<td>O</td>
<td>Multi-level power supply for liquid crystal drive.</td>
</tr>
<tr>
<td>23</td>
<td>VPP</td>
<td>P</td>
<td>OTP programming power</td>
</tr>
<tr>
<td>40</td>
<td>TEST</td>
<td>I</td>
<td>Chip test function. Leave it open</td>
</tr>
<tr>
<td>30</td>
<td>PWRT</td>
<td>I</td>
<td>Power on timer enable control pin.</td>
</tr>
</tbody>
</table>

Legend:  
I = input,  
O = output,  
I/O = input/output,  
P = power.
6. OTP ROM Programming Interface

6.1 Interface Description

In order to program OTP ROM, several pins have to be reserved on the PCB which is bounding with ST20P18. These total are 8 pins that include following list TABLE 6-1: . It just be used to connect writer to program OTP ROM. After programming and disconnecting from writer, they can be used as original purpose.

<table>
<thead>
<tr>
<th>P18 Pad Name</th>
<th>(SPI Interface)</th>
<th>Pin Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPP</td>
<td>VPP</td>
<td>Power</td>
<td>High Voltage Power Supply</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1) OTP Program, Program Verify, VPP=&gt; 12V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2) OTP Read:VPP=&gt; Floating</td>
</tr>
<tr>
<td>GND</td>
<td>VSS</td>
<td>Power</td>
<td>Ground.</td>
</tr>
<tr>
<td>VCC</td>
<td>VDD</td>
<td>Power</td>
<td>Low Voltage (2.4V-5.4V) Power Supply.</td>
</tr>
<tr>
<td>PE3</td>
<td>SSB</td>
<td>Input</td>
<td>SPI signal</td>
</tr>
<tr>
<td>SEG4</td>
<td>MOSI</td>
<td>Input</td>
<td>SPI signal</td>
</tr>
<tr>
<td>SEG5</td>
<td>MISO</td>
<td>Output</td>
<td>SPI signal</td>
</tr>
<tr>
<td>PE2</td>
<td>SCK</td>
<td>Input</td>
<td>SPI signal</td>
</tr>
<tr>
<td>RESET</td>
<td>RESET</td>
<td>Input</td>
<td>SPI RESET</td>
</tr>
</tbody>
</table>

6.2 Programming Function Specification

There are reserved 5 option bits to select to apply or not the function we needed. It includes PD input, WDT enable, WDT stop at WAI-1 and Code Protection. To setup the options should program the OTP ROM by OTP writer by control register. The register OTP($37) is used to read contents of the option word.
TABLE 6-2: Option ward

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>WDTSTP</td>
<td>WDTEN</td>
<td>-</td>
<td>PD</td>
<td>1--1 11-1</td>
</tr>
</tbody>
</table>

Bit 7: **CP**: OTP ROM code protect.
0 = protect OTP data.
1 = Un-Protect OTP data.

Bit 3: **WDTSTP**: WDT stop control bit.
0 = WDT stop at WAI-1 and STP mode.
1 = WDT is always active if WDTEN is enabled.

Bit 2: **WDTEN**: WDT enable.
0 = WDT disable.
1 = WDT enable.

Bit 0: **PD**: Port function selection
0 = PD used as input port.
1 = OSC input pin for 32768Hz crystal.

TABLE 6-3: OTP option ward read back window

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>R/W</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>$037</td>
<td>OPT</td>
<td>R</td>
<td>CP</td>
<td>-</td>
<td>-</td>
<td>PWRT</td>
<td>WDTSTP</td>
<td>WDTEN</td>
<td>-</td>
<td>PD</td>
<td>1--1 11-1</td>
</tr>
</tbody>
</table>

7. Power On Timer

The Power-on Timer (PWRT) is offered necessary delays on power-up to keep the chip in reset until the crystal oscillator is stable, the typical delay time in 3v at 25℃ is 32ms, and operation in voltage 2.4V~5.5V ,60℃~ -10℃ is 4~640ms. The default state is high with one internal pull-up resistance.

TABLE 7-4: Power on timer pin option

<table>
<thead>
<tr>
<th>IC pad</th>
<th>option</th>
<th>Description</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWRT</td>
<td>0</td>
<td>disable power-on timer, tie to GND</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>enable power-on timer, tie to VCC</td>
<td>1:input pull-up</td>
</tr>
</tbody>
</table>
8. Application Circuits

8.1 APPLICATION CIRCUIT UNDER 3V OPERATING VOLTAGE

VDD : 3V
Clock : 32768Hz crystal and 4.0MHz RC oscillator
LCD : 1/8 duty
I/O : PORT A
ALARM : PSGO, PSGOB

FIGURE 8-1: APPLICATION CIRCUIT WITHOUT LCD KEYBOARD AWAKING PULSE
VDD : 3V
Clock : 32768Hz crystal and 4.0MHz RC oscillator
LCD : 1/8 duty
I/O : PORT A
ALARM : PSGO, PSGOB

Note:
1. COMs and SEGs output GND level, while the LCD is turned off.
2. If LCD is turned off, Keyboard Awaking Pulses must be turned off at the same time.
3. Connect one capacitor of 100PF to OSCI stabilize oscillation frequency. This capacitor must be placed close to OSCI.

FIGURE 8-2: APPLICATION CIRCUIT WITH LCD KEYBOARD AWAKING PULSE
9. PACKAGE INFORMATION

Dimensions in Millimeters

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>MILLIMETER</th>
<th>MIN.</th>
<th>NOM.</th>
<th>MAX.</th>
</tr>
</thead>
<tbody>
<tr>
<td>b</td>
<td>0.30</td>
<td>0.35</td>
<td>0.45</td>
<td></td>
</tr>
<tr>
<td>e</td>
<td>0.80 BSC.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>18.4 REF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td>12.0 REF</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TOLERANCE OF FORM AND POSITION

aaa  0.25
bbb  0.20
ccc  0.20
10. PIN CONFIGURATION (QFP80)

```
P P
C C
0 1
/ / 
S S S S S S S S S S S S S S
E E E E E E E E E E E E
N N G G G G G G G G G G G G
C C 1 1 1 1 1 1 1 1 1 1 1 1 1
2 3 4 5 6 7 8 9 0 1 2 3 4 5
80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65

NC 1
NC 2
SEG11 3
SEG10 4
SEG 9 5
SEG 8 6
SEG 7 7
SEG 6 8
SEG 5 9
SEG 4 10
PA7/SEG 3 11
PA6/SEG 2 12
PA5/SEG 1 13
PA4/SEG 0 14
PA3 15
PA2 16
PA1 17
PA0/INTX 18
PE3 19
PE2 20
PE1 21
PE0 22
NC 23
NC 24

PB7/SEG39 47
PB6/SEG38 48
PB5/SEG37 49
PB4/SEG36 50
PB3/SEG35 51
PB2/SEG34 52
PB1/SEG33 53
PB0/SEG32 54
PC7/SEG31 55
PC6/SEG30 56
PC5/SEG29 57
PC4/SEG28 58
PC3/SEG27 59
PC2/SEG26 60
NC 61
NC 62
NC 63
NC 64

COM0 45
COM1 44
COM2 43
NC 42
NC 41
NC 40
NC 39
NC 38
NC 37
NC 36
NC 35
NC 34
NC 33
NC 32
NC 31
NC 30
NC 29
NC 28
NC 27
PC2/SEG26
```

Ver 1.4 11/12 6/13/07
## REVISION

<table>
<thead>
<tr>
<th>Version</th>
<th>Page</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>8,9</td>
<td>modify Rosc 180k ohm to 226k ohm under 4Mhz condition</td>
<td>2006/3/1</td>
</tr>
<tr>
<td>1.3</td>
<td>1</td>
<td>add CPU clock 250K ~ 4MHz</td>
<td>2006/6/26</td>
</tr>
<tr>
<td>1.4</td>
<td>10,11</td>
<td>Move package information to page10,11</td>
<td>2006/8/8</td>
</tr>
</tbody>
</table>

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